THE DATASHEET OF

OPA2376AIDR

TEXAS INSTRUMENTS

OPA376, OPA2376, OPA4376

SBOS406G – JUNE 2007 – REVISED DECEMBER 2015

OPAx376 Low-Noise, Low Quiescent Current, Precision Operational Amplifier *e-trim* Series

1 Features

- Low Noise: 7.5 nV/√Hz at 1 kHz
- 0.1 Hz to 10 Hz Noise: 0.8 μV_{PP}
- Quiescent Current: 760 µA (typical)
- Low Offset Voltage: 5 µV (typ)
- Gain Bandwidth Product: 5.5 MHz
- Rail-to-Rail Input and Output
- Single-Supply Operation
- Supply Voltage: 2.2 V to 5.5 V
- Space-Saving Packages:
  - SC70, SOT-23, DSBGA, VSSOP, TSSOP

2 Applications

- ADC Buffer
- Audio Equipment
- Medical Instrumentation
- Handheld Test Equipment
- Active Filtering
- Sensor Signal Conditioning

3 Description

The OPA376 family represents a new generation of low-noise operational amplifiers with e-trim™, offering outstanding dc precision and ac performance. Rail-to-rail input and output, low offset (25 µV, maximum), low noise (7.5 nV/√Hz), quiescent current of 950 µA (maximum), and a 5.5-MHz bandwidth make this part very attractive for a variety of precision and portable applications. In addition, this device has a reasonably wide supply range with excellent PSRR, making it attractive for applications that run directly from batteries without regulation.

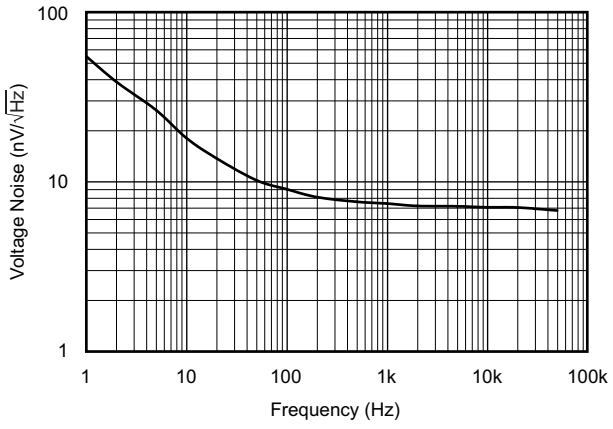
The OPA376 (single version) is available in *Micro*SIZE SC70-5, SOT-23-5, and SOIC-8 packages. The OPA2376 (dual) is offered in the DSBGA-8, VSSOP-8, and SOIC-8 packages. The OPA4376 (quad) is offered in a TSSOP-14 package. All versions are specified for operation from –40°C to +125°C.

Device Information(1)

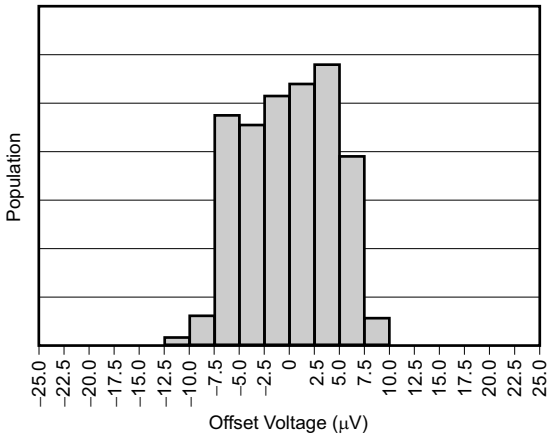
PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA376	SOIC (8)	4.90 mm × 3.91 mm
	SOT-23 (5)	2.90 mm × 1.60 mm
	SC70 (5)	2.00 mm × 1.25 mm
OPA2376	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm
	DSBGA (8)	1.30 mm × 2.30 mm
OPA4376	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

Input Noise Voltage Spectral Density



Offset Voltage Production Distribution



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (March 2013) to Revision G — **Page**

- Added *ESD Ratings*, *Thermal Information*, *Recommended Operating Conditions*, *Power Supply Recommendations*, and *Device and Documentation Support* sections; existing sections may have moved ... 1
- Changed *WCSP* to *DSBGA* and *MSOP* to *VSSOP* throughout data sheet ... 1
- Changed dimensions shown in YZD package pinout figure ... 4

Changes from Revision E (January 2013) to Revision F — **Page**

- Changed unit (typo) for Quiescent Current feature bullet ... 1
- Changed TSSOP-14 pinout for OPA4376 ... 5

Changes from Revision D (August 2010) to Revision E — **Page**

- Changed rail-to-rail feature bullet to show input and output ... 1
- Changed description text to show rail-to-rail input and output ... 1

Changes from Revision C (October 2008) to Revision D — **Page**

- Updated format of *Electrical Characteristics* table ... 8
- Updated Figure 11 ... 11

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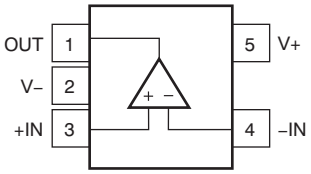
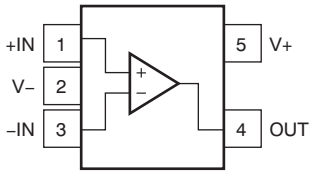
5 Pin Configuration and Functions

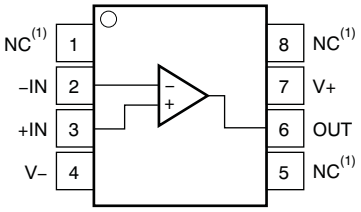
OPA376: DBV Package
5-Pin SOT23
Top View



OPA376: DCK Package
5-Pin SC70-5
Top View



OPA376: D Package
8-Pin SOIC
Top View



(1) NC denotes no internal connection.

Pin Functions: OPA376

PIN				I/O	DESCRIPTION
NAME	DBV	DCK	D		
+IN	3	1	3	I	Input signal $^{+}$
–IN	4	3	2	I	Input signal $^{-}$
NC	—	—	1, 5, 8	—	No connection
OUT	1	4	6	O	Output signal
V^{+}	5	5	7	—	Supply voltage^{+}
V^{-}	2	2	4	—	Supply voltage^{-}

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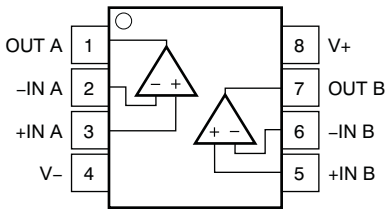
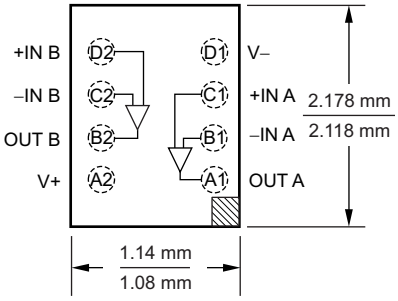
OPA2376: D and DGK Packages
8-Pin SOIC and 8-Pin VSSOP
Top View



OPA2376: YZD Package
8-Pin DSBGA
Top View



(Bump-Side Down)

Pin Functions: OPA2376

PIN			I/O	DESCRIPTION
NAME	D AND DGK	YZD		
+IN A	3	C1	I	Input signal A^+
–IN A	2	B1	I	Input signal $A^–$
+IN B	5	D2	I	Input signal B^+
–IN B	6	C2	I	Input signal $B^–$
OUT A	1	A1	O	Output signal A
OUT B	7	B2	O	Output signal B
V^+	8	A2	—	Supply voltage$^+$
$V^–$	4	D1	—	Supply voltage$^–$

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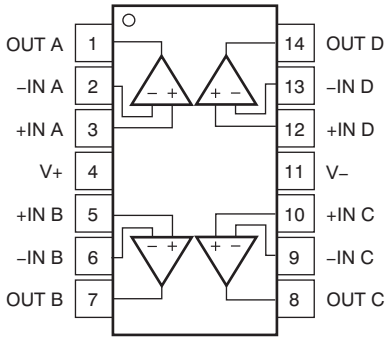
OPA4376: PW Package
14-Pin TSSOP
Top View



Pin Functions: OPA4376

PIN		I/O	DESCRIPTION
NAME	PW		
+IN A	3	I	Input signal A^+
–IN A	2	O	Input signal $A^–$
+IN B	5	I	Input signal B^+
–IN B	6	O	Input signal $B^–$
+IN C	10	I	Input signal C^+
–IN C	9	O	Input signal $C^–$
+IN D	12	I	Input signal D^+
–IN D	13	O	Input signal $D^–$
OUT A	1	O	Output signal A
OUT B	7	O	Output signal B
OUT C	8	O	Output signal C
OUT D	14	O	Output signal D
V^+	4	—	Supply voltage$^+$
$V^–$	11	—	Supply voltage$^–$

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply, $V_S = (V^+) – (V^–)$		7	V
	Signal input pin(2)	$(V^–) – 0.5$	$(V^+) + 0.5$	V
Current	Signal input pin(2)	–10	10	mA
	Output short-circuit(3)	Continuous		
Temperature	Operating range, T_A	–40	150	°C
	Junction, T_J		150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	
		Machine model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$(V^+) – (V^–)$	Supply voltage	2.2 (±1.1)		5.5 (±2.75)	V
T_A	Operating temperature	–40		150	°C

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6.4 Thermal Information: OPA376

THERMAL METRIC(1)		OPA376			UNIT
		DBV (SOT-23)	DCK (SC70)	D (SOIC)	
		5 PINS	5 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	273.8	267.0	100.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	126.8	80.9	42.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	85.9	54.8	41.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.9	1.2	4.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	84.9	54.1	40.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Thermal Information: OPA2376

THERMAL METRIC(1)		OPA2376			UNIT
		D (SOIC)	DGK (VSSOP)	YZD (DSBGA)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	111.1	171.2	119.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.7	63.9	0.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.7	92.8	27.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.5	9.2	4.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	51.2	91.2	27.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the*Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 Thermal Information: OPA4376

THERMAL METRIC(1)		OPA4376	UNIT
		PW	
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	51.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the*Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.7 Electrical Characteristics

At T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			5	25	µV
dV_{OS}/dT	Input offset voltage versus temperature	T_A = –40°C to +85°C		0.26	1	µV/°C
		T_A = –40°C to +125°C		0.32	2	µV/°C
PSRR	Input offset voltage versus power supply	T_A = 25°C, V_S = 2.2 V to 5.5 V, V_{CM} < (V^+) – 1.3 V		5	20	µV/V
		T_A = –40°C to +125°C, V_S = 2.2 V to 5.5 V, V_{CM} < (V^+) – 1.3 V		5		µV/V
	Channel separation, dc (dual, quad)			0.5		mV/V
INPUT BIAS CURRENT						
I_B	Input bias current	T_A = 25°C		0.2	10	pA
		T_A = –40°C to +125°C		See *Typical Characteristics*		pA
I_{OS}	Input offset current			0.2	10	pA
NOISE						
	Input voltage noise	f = 0.1 Hz to 10 Hz		0.8		$µV_{PP}$
e_n	Input voltage noise density	f = 1 kHz		7.5		$nV/\sqrt{Hz}$
i_n	Input current noise	f = 1 kHz		2		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		(V^-) – 0.1		(V^+) + 0.1	V
CMRR	Common-mode rejection ratio	(V^-) < V_{CM} < (V^+) – 1.3 V	76	90		dB
INPUT CAPACITANCE						
	Differential			6.5		pF
	Common-mode			13		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	50 mV < V_O < (V^+) – 50 mV, R_L = 10 kΩ	120	134		dB
		100 mV < V_O < (V^+) – 100 mV, R_L = 2 kΩ	120	126		dB
FREQUENCY RESPONSE C_L = 100 pF, V_S = 5.5 V						
GBW	Gain-bandwidth product			5.5		MHz
SR	Slew rate	G = 1		2		V/µs
t_S	Settling time	To 0.1%, 2-V step , G = 1		1.6		µs
		To 0.01%, 2-V step , G = 1		2		µs
	Overload recovery time	V_{IN} × gain > V_S		0.33		µs
THD+N	Total harmonic distortion + noise	V_O = 1 V_{RMS}, G = 1, f = 1 kHz, R_L = 10 kΩ		0.00027%		

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Electrical Characteristics (continued)

At T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
	Voltage output swing from rail	T_A = 25°C, R_L = 10 kΩ	SC70-5, SOT23-5, SO-8, VSSOP-8, and TSSOP-14 packages only		10	20	mV
			DSBGA package only		20	30	mV
		T_A = –40°C to +125°C, R_L = 10 kΩ				40	mV
		T_A = 25°C, R_L = 2 kΩ	SC70-5, SOT23-5, SO-8, VSSOP-8, and TSSOP-14 packages only		40	50	mV
			DSBGA package only		50	60	mV
		T_A = –40°C to +125°C, R_L = 2 kΩ				80	mV
I_{SC}	Short-circuit current				+30, –50		mA
C_{LOAD}	Capacitive load drive				See *Typical Characteristics*		
R_O	Open-loop output impedance				150		Ω
POWER SUPPLY							
V_S	Specified voltage range			2.2		5.5	V
	Operating voltage range				2 to 5.5		V
I_Q	Quiescent current per amplifier	T_A = 25°C, I_O = 0, V_S = 5.5 V, V_{CM} < (V^+) – 1.3 V			760	950	µA
		T_A = –40°C to +125°C				1	mA
TEMPERATURE							
	Specified range			–40		125	°C
	Operating range			–40		150	°C

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6.8 Typical Characteristics

At T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

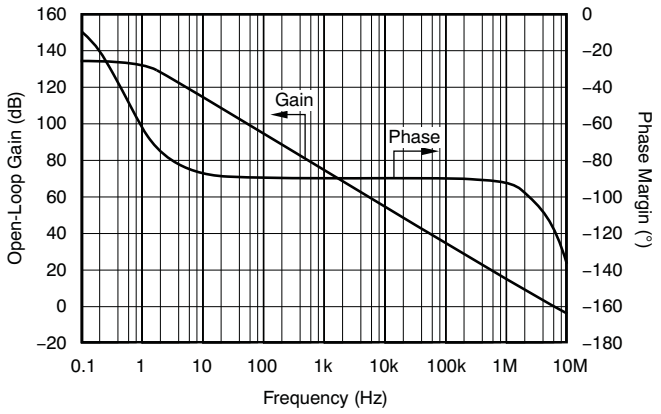

Figure 1. Open-Loop Gain and Phase vs Frequency

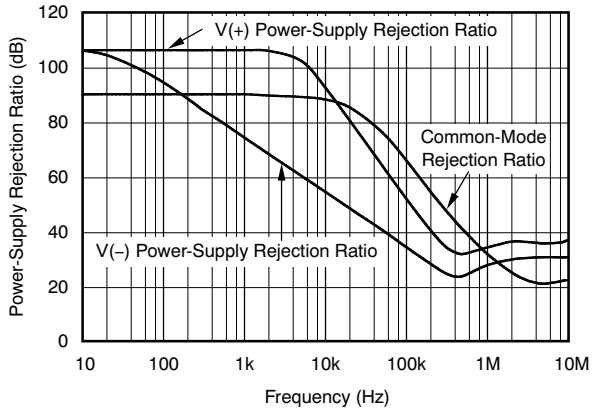

Figure 2. Power-Supply and Common-Mode Rejection Ratio vs Frequency

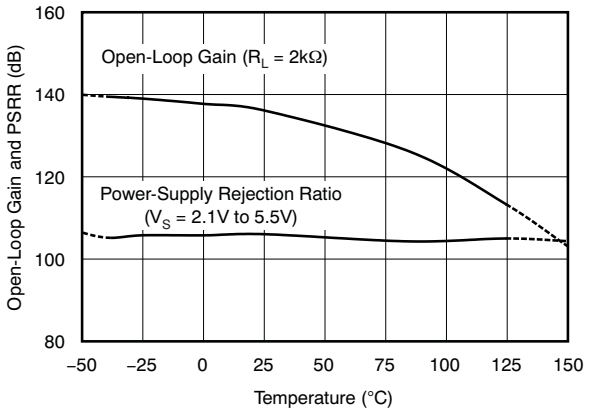

Figure 3. Open-Loop Gain and Power-Supply Rejection Ratio vs Temperature

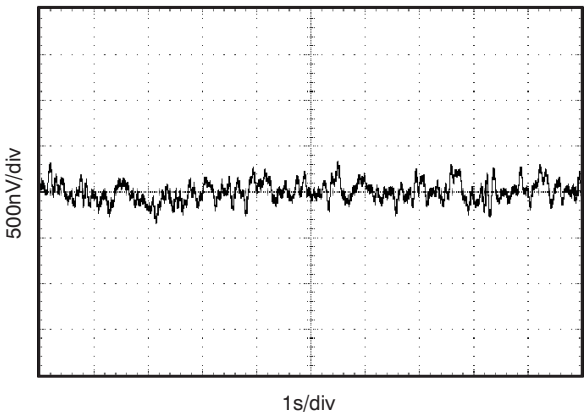

Figure 4. 0.1-Hz to 10-Hz Input Voltage Noise

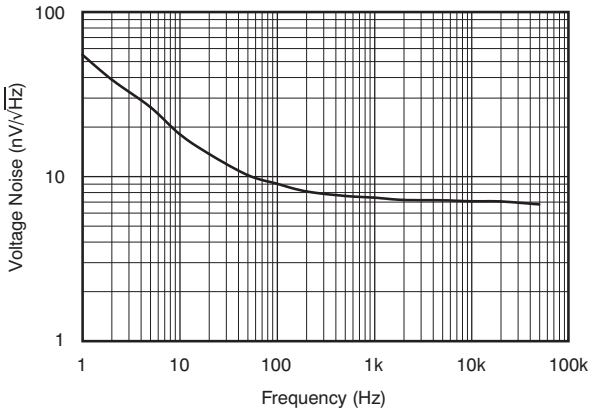

Figure 5. Input Voltage Noise Spectral Density

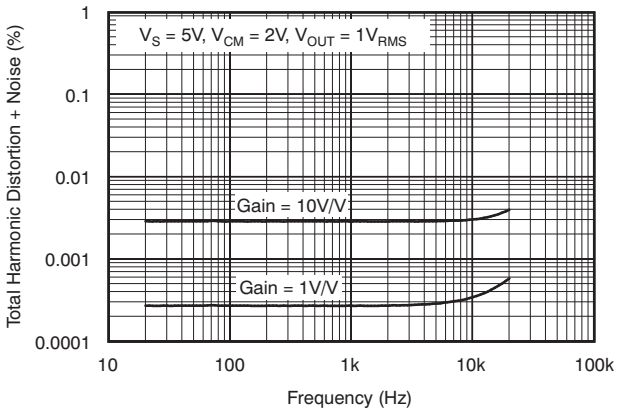

Figure 6. Total Harmonic Distortion + Noise vs Frequency

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Typical Characteristics (continued)

At T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

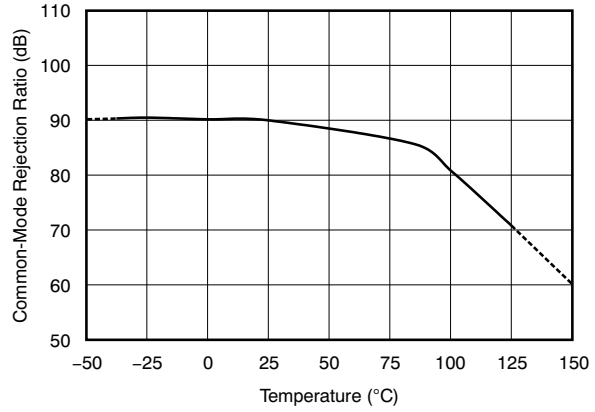

Figure 7. Common-Mode Rejection Ratio vs Temperature

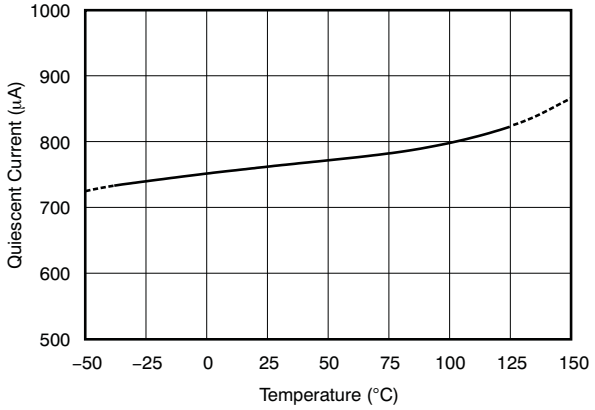

Figure 8. Quiescent Current vs Temperature

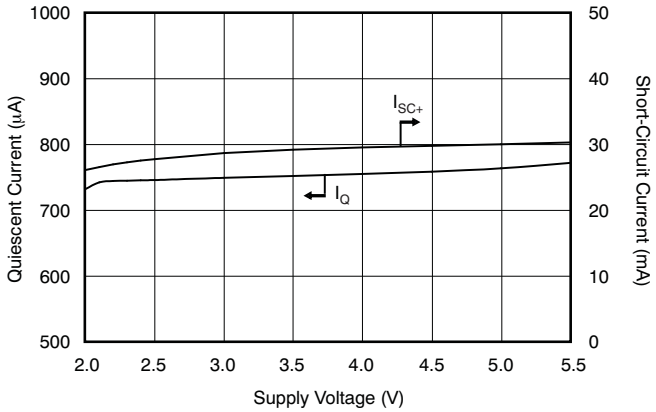

Figure 9. Quiescent and Short-Circuit Current vs Supply Voltage

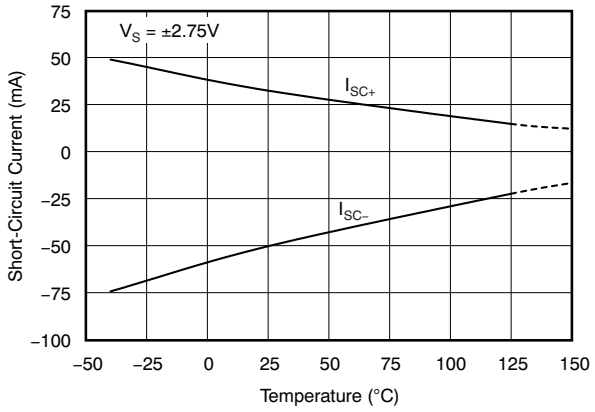

Figure 10. Short-Circuit Current vs Temperature

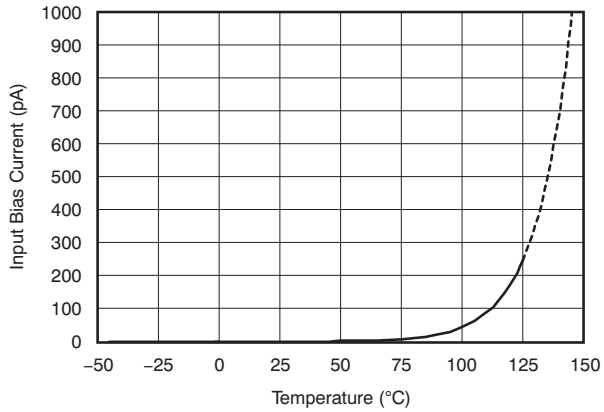

Figure 11. Input Bias Current vs Temperature

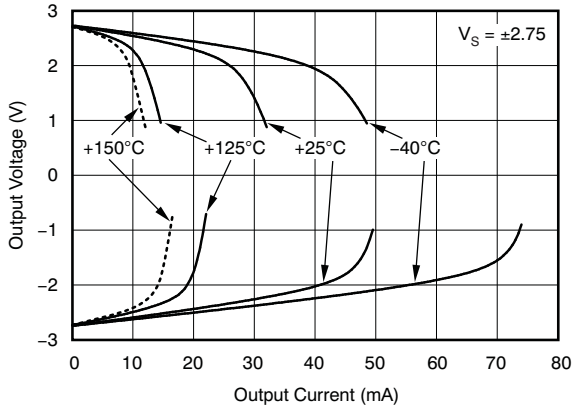

Figure 12. Output Voltage vs Output Current

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Typical Characteristics (continued)

At T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

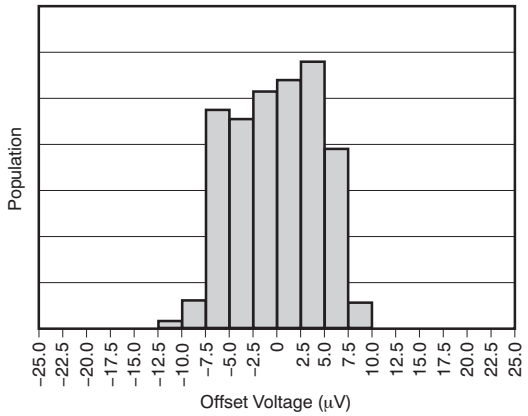

Figure 13. Offset Voltage Production Distribution

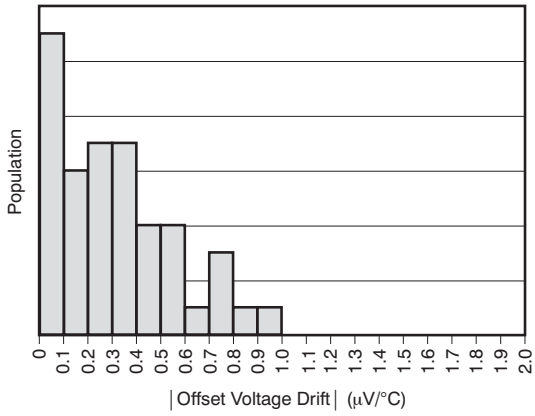

Figure 14. Offset Voltage Drift Production Distribution (–40°C to 125°C)

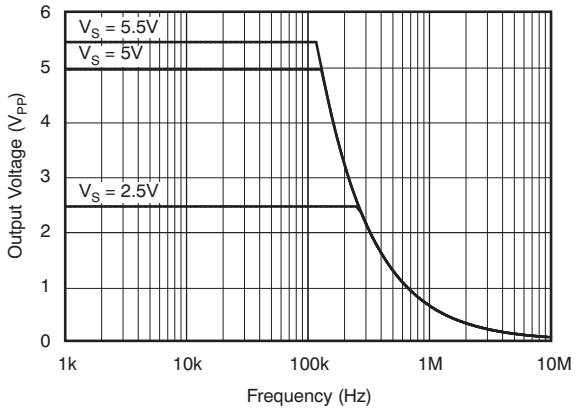

Figure 15. Maximum Output Voltage vs Frequency

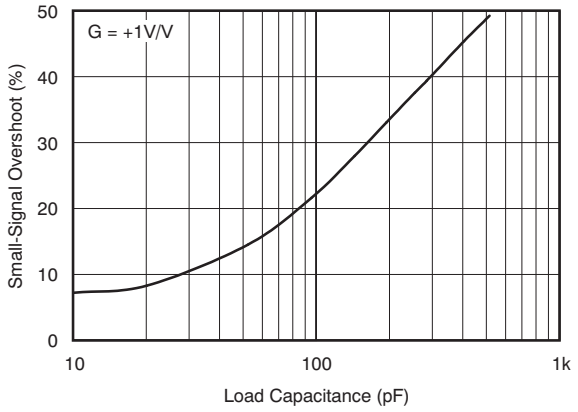

Figure 16. Small-Signal Overshoot vs Load Capacitance

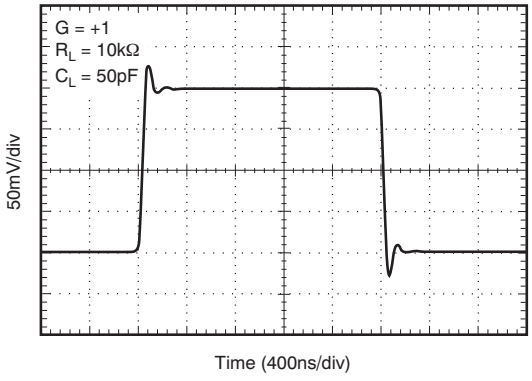

Figure 17. Small-Signal Pulse Response

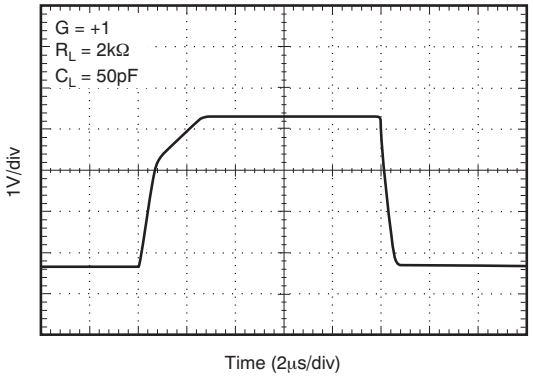

Figure 18. Large-Signal Pulse Response

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Typical Characteristics (continued)

At T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

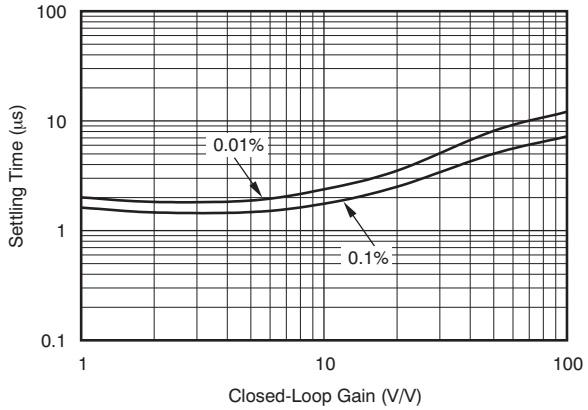


Figure 19. Settling Time vs Closed-Loop Gain

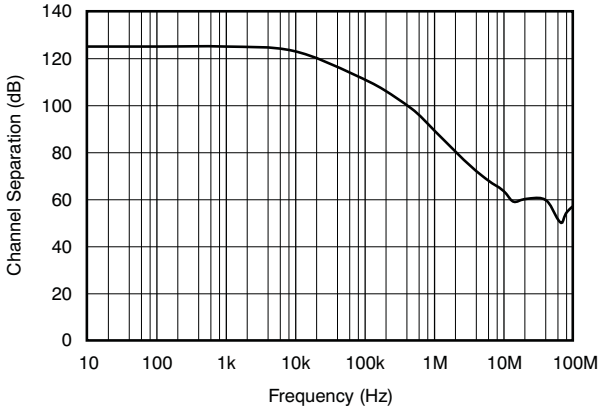


Figure 20. Channel Separation vs Frequency

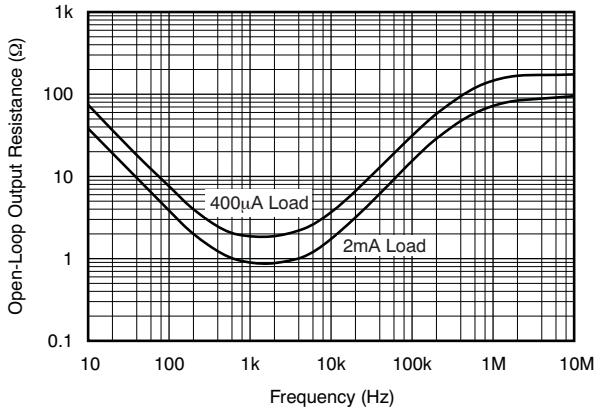


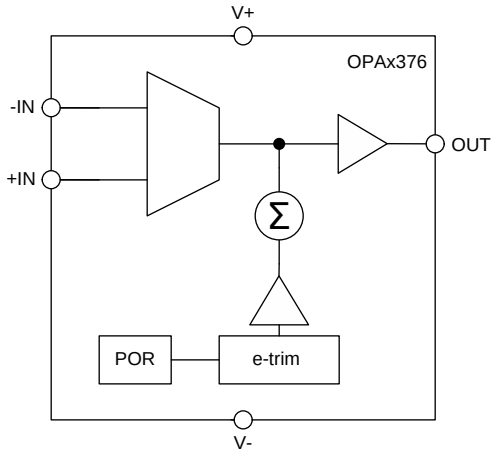
Figure 21. Open-Loop Output Resistance vs Frequency

7 Detailed Description

7.1 Overview

The OPA376 family belongs to a new generation of low-noise operational amplifiers with *e-trim*, giving customers outstanding dc precision and ac performance. Low noise, rail-to-rail input and output, and low offset, drawing a low quiescent current, make these devices ideal for a variety of precision and portable applications. In addition, this device has a wide supply range with excellent PSRR, making it a suitable option for applications that are battery-powered without regulation.

7.2 Functional Block Diagram



7.3 Feature Description

The OPAx376 family of precision amplifiers offers excellent dc performance as well as excellent ac performance. Operating from a single power-supply the OPAx376 is capable of driving large capacitive loads, has a wide input common-mode voltage range, and is well-suited to drive the inputs of SAR ADCs as well as 24-bit and higher resolution converters. Including internal ESD protection, the OPAx376 family is offered in a variety of industry-standard packages, including a wafer chip-scale package for applications that require space savings.

7.3.1 Operating Voltage

The OPA376 family of amplifiers operates over a power-supply range of 2.2 V to 5.5 V (±1.1 V to ±2.75 V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

7.3.2 Input Offset Voltage and Input Offset Voltage Drift

The OPAx376 family of operational amplifiers is manufactured using TI's e-trim technology. Each amplifier is trimmed in production, thereby minimizing errors associated with input offset voltage and input offset voltage drift. The e-trim technology is a TI proprietary method of trimming internal device parameters during either wafer probing or final testing.

7.3.3 Capacitive Load and Stability

The OPA376 series of amplifiers may be used in applications where driving a capacitive load is required. As with all op amps, there may be specific instances where the OPAx376 can become unstable, leading to oscillation. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation. An op amp in the unity-gain (+1-V/V) buffer configuration and driving a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the op amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases.

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Feature Description (continued)

The OPAx376 in a unity-gain configuration can directly drive up to 250 pF of pure capacitive load. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see the typical characteristic Figure 16. In unity-gain configurations, capacitive load drive can be improved by inserting a small (10-Ω to 20-Ω) resistor, R_S, in series with the output, as shown in Figure 22. This resistor significantly reduces ringing while maintaining dc performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created, introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_S / R_L, and is generally negligible at low output current levels.

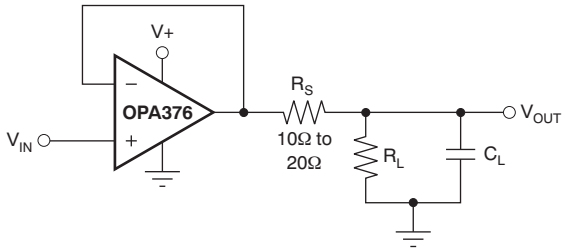

Figure 22. Improving Capacitive Load Drive

7.3.4 Common-Mode Voltage Range

The input common-mode voltage range of the OPA376 series extends 100 mV beyond the supply rails. The offset voltage of the amplifier is very low, from approximately (V^-) to (V^+) – 1 V, as shown in Figure 23. The offset voltage increases as common-mode voltage exceeds (V^+) –1 V. Common-mode rejection is specified from (V^-) to (V^+) – 1.3 V.

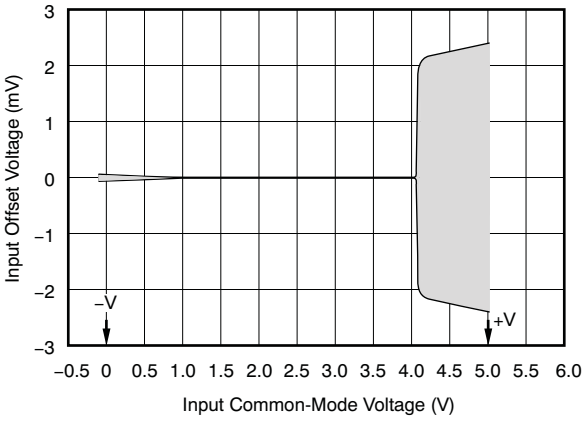

Figure 23. Offset and Common-Mode Voltage

Feature Description (continued)

7.3.5 Input and ESD Protection

The OPA376 family incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the *Absolute Maximum Ratings*. Figure 24 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value should be kept to a minimum in noise-sensitive applications.

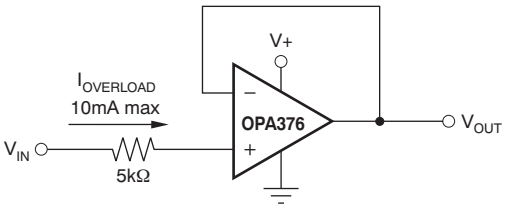

Figure 24. Input Current Protection

7.4 Device Functional Modes

The OPAx376 has a single functional mode and is operational when the power-supply voltage is greater than 2.2 V (±1.1 V). The maximum power supply voltage for the OPAx376 is 5.5 V (±2.75 V).

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPA376 family of operational amplifiers is built using *e-trim*, a proprietary technique in which offset voltage is adjusted during the final steps of manufacturing. This technique compensates for performance shifts that can occur during the molding process. Through *e-trim*, the OPA376 family delivers excellent offset voltage (5 µV, typical). Additionally, the amplifier boasts a fast slew rate, low drift, low noise, and excellent PSRR and A_{OL}. These 5.5-MHz CMOS op amps operate on 760-µA (typical) quiescent current.

8.1.1 Basic Amplifier Configurations

The OPA376 family is unity-gain stable. It does not exhibit output phase inversion when the input is overdriven. A typical single-supply connection is shown in Figure 25. The OPA376 is configured as a basic inverting amplifier with a gain of –10 V/V. This single-supply connection has an output centered on the common-mode voltage, V_{CM}. For the circuit shown, this voltage is 2.5 V, but may be any value within the common-mode input voltage range.

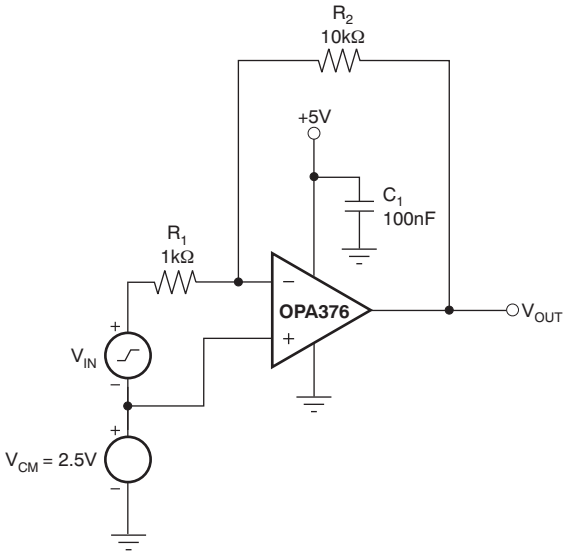


Figure 25. Basic Single-Supply Connection

Application Information (continued)

8.1.2 Active Filtering

The OPA376 series is well-suited for filter applications requiring a wide bandwidth, fast slew rate, low-noise, single-supply operational amplifier. Figure 26 shows a 50-kHz, 2nd-order, low-pass filter. The components have been selected to provide a maximally-flat Butterworth response. Beyond the cutoff frequency, roll-off is –40 dB/decade. The Butterworth response is ideal for applications requiring predictable gain characteristics such as the anti-aliasing filter used ahead of an analog-to-digital converter (ADC).

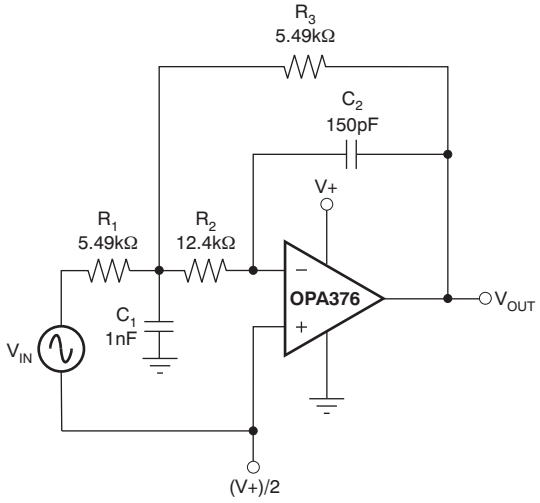
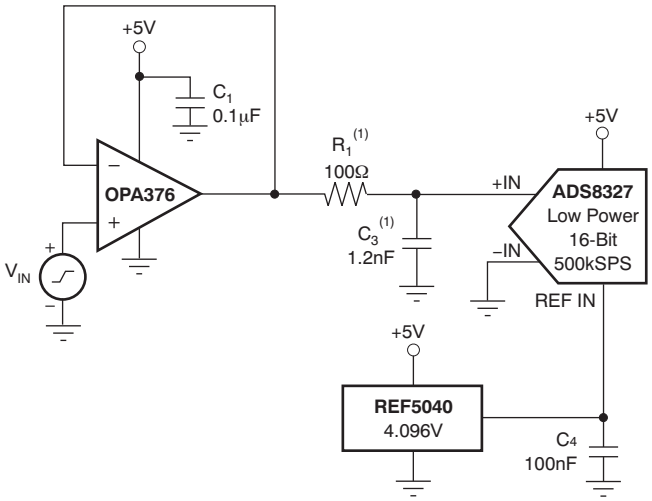


Figure 26. Second-Order, Butterworth, 50-kHz, Low-Pass Filter

8.1.3 Driving an Analog-to-Digital Converter

The low noise and wide gain bandwidth of the OPA376 family make it an ideal driver for ADCs. Figure 27 illustrates the OPA376 driving an ADS8327, a 16-bit, 250-kSPS converter. The amplifier is connected as a unity-gain, non-inverting buffer.



(1) Suggested value; may require adjustment based on specific application.

Figure 27. Driving an ADS8327

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Application Information (continued)

8.1.4 Phantom-Powered Microphone

The circuit shown in Figure 28 depicts how a remote microphone amplifier can be powered by a phantom source on the output side of the signal cable. The cable serves double duty, carrying both the differential output signal from and dc power to the microphone amplifier stage.

An OPA2376 serves as a single-ended input to a differential output amplifier with a 6-dB gain. Common-mode bias for the two op amps is provided by the dc voltage developed across the electret microphone element. A 48-V phantom supply is reduced to 5.1 V by the series 6.8-kΩ resistors on the output side of the cable, and the 4.7-kΩ resistor and zener diode on the input side of the cable. AC coupling blocks the different dc voltage levels from each other on each end of the cable.

An INA163 instrumentation amplifier provides differential inputs and receives the balanced audio signals from the cable. The INA163 gain may be set from 0 dB to 80 dB by selecting the R_G value. The INA163 circuit is typical of the input circuitry used in mixing consoles.

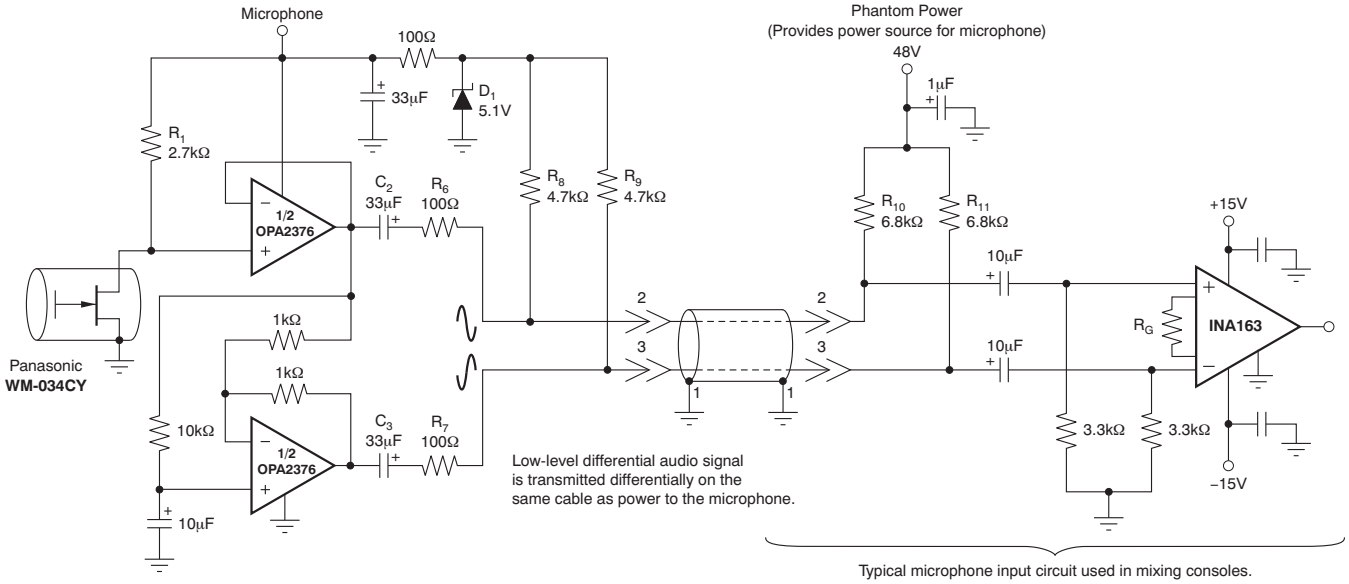
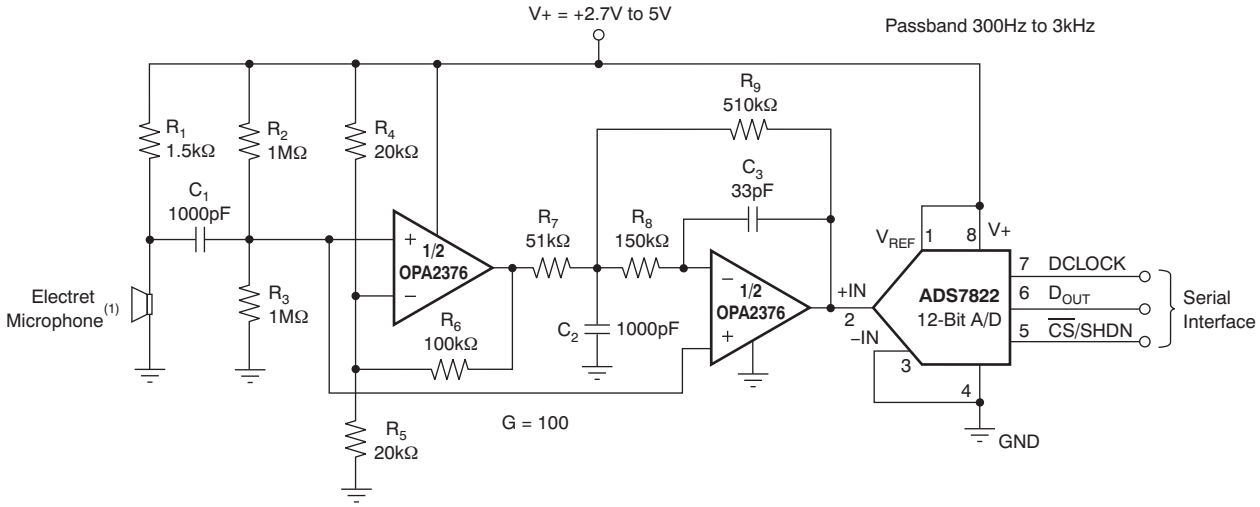


Figure 28. Phantom-Powered Electret Microphone



(1) Electret microphone powered by R_1.

Figure 29. OPA2376 as a Speech Bandpass-Filtered, Data Acquisition System

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8.2 Typical Application

Low-pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The OPA376 is ideally suited to construct high-speed, high-precision active filters. Figure 30 shows a second-order, low-pass filter commonly encountered in signal processing applications.

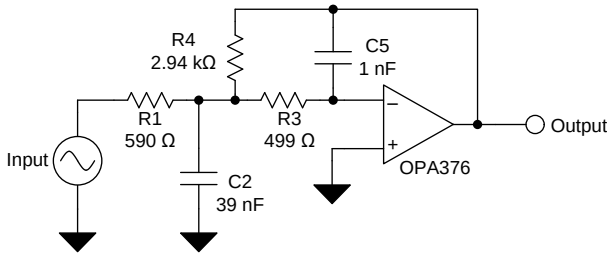

Figure 30. Typical Application Schematic

8.2.1 Design Requirements

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second-order Chebyshev filter response with 3-dB gain peaking in the passband

8.2.1.1 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in Figure 30. Use Equation 1 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1R_3C_2C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3R_4C_2C_5} \quad (1)$$

This circuit produces a signal inversion. For this circuit, the gain at dc and the low-pass cutoff frequency are calculated by Equation 2:

$$\text{Gain} = \frac{R_4}{R_1}$$

$$f_C = \frac{1}{2\pi}\sqrt{(1/R_3R_4C_2C_5)} \quad (2)$$

Software tools are readily available to simplify filter design. WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

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Typical Application (continued)

8.2.2 Application Curve

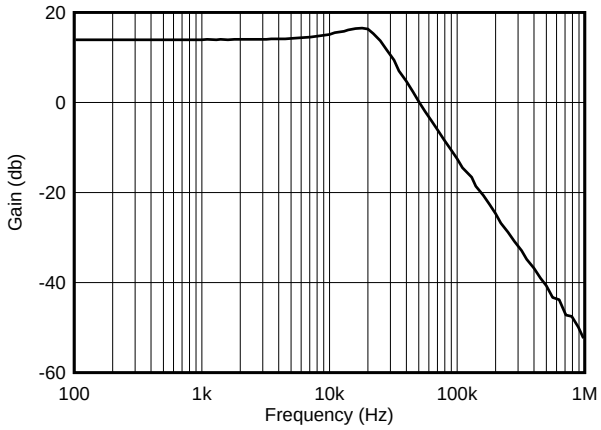

Figure 31. Low-Pass Filter Transfer Function

9 Power Supply Recommendations

The OPAx376 are specified for operation from 2.2 V to 5.5 V (±1.1 V to ±2.75 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, and the op amp itself. Bypass capacitors can reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat, and reduces EMI noise pickup. Physically separate the digital and analog grounds, paying attention to the flow of the ground current. For more detailed information refer to *Circuit Board Layout Techniques*, SLOA089.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is better than opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 32, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of the input traces as short as possible. The input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Clean the PCB following board assembly for best performance.
- Any precision-integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

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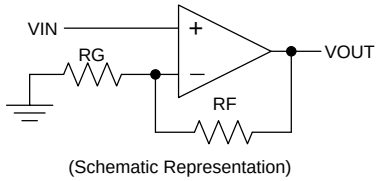
Layout Guidelines (continued)

10.1.1 Photosensitivity

Although the OPA2376YZD package has a protective backside coating that reduces the amount of light exposure on the die, unless fully shielded, ambient light can reach the active region of the device. Input bias current for the package is specified in the absence of light. Depending on the amount of light exposure in a given application, an increase in bias current, and possible increases in offset voltage, should be expected. Fluorescent lighting may introduce noise or hum because of the time-varying light output. Best layout practices include end-product packaging that provides shielding from possible light sources during operation.

10.2 Layout Example



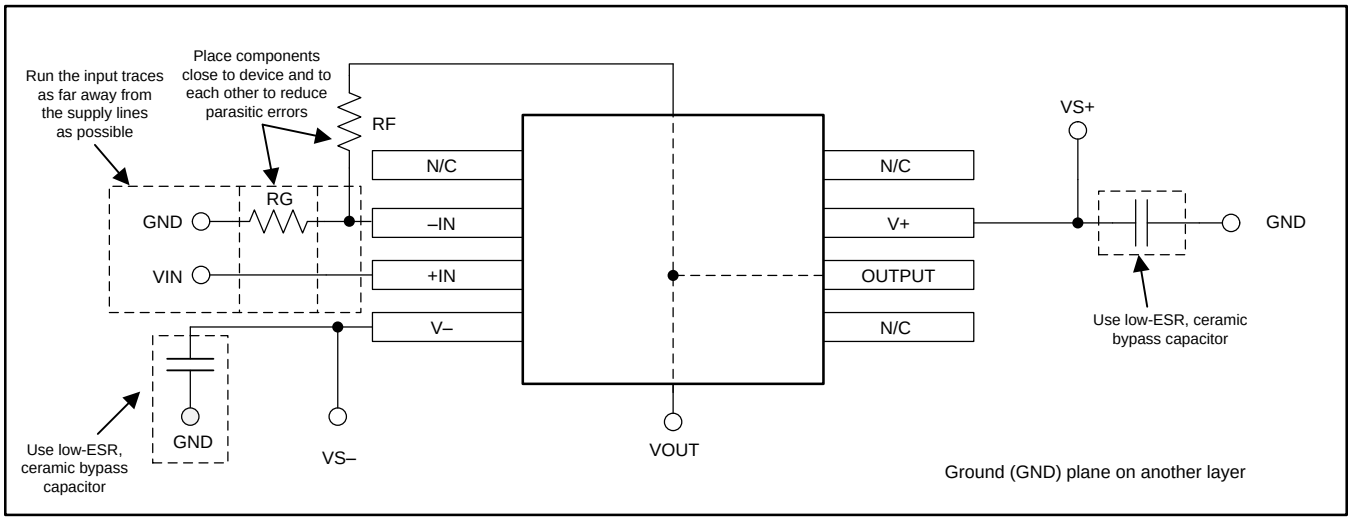


Figure 32. Layout Example

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

11.1.1.2 TI Precision Designs

TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI Precision Designs are available online at http://www.ti.com/ww/en/analog/precision-designs/.

11.1.1.3 WEBENCH® Filter Designer

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

11.2 Related Documentation

For related documentation, see the following:

Circuit Board Layout Techniques, SLOA089.

Operational Amplifier Gain stability, Part 3: AC Gain-Error Analysis, SLYT383.

Operational Amplifier Gain Stability, Part 2: DC Gain-Error Analysis, SLYT374.

Using infinite-gain, MFB filter topology in fully differential active filters, SLYT343.

Op Amp Performance Analysis, SBOS054.

Single-Supply Operation of Operational Amplifiers, SBOA059.

Tuning in Amplifiers, SBOA067.

Shelf-Life Evaluation of Lead-Free Component Finishes, SZZA046.

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11.3 Related Links

See Table 1 for a list of quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE AND BUY	TECHNICAL DOCUMENTS	TOOLS AND SOFTWARE	SUPPORT AND COMMUNITY
OPA376	Click here	Click here	Click here	Click here	Click here
OPA2376	Click here	Click here	Click here	Click here	Click here
OPA4376	Click here	Click here	Click here	Click here	Click here

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

e-trim, TINA-TI, E2E, NanoStar, NanoFree are trademarks of Texas Instruments.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

The OPAx376 are specified for operation from 2.2 V to 5.5 V (±1.1 V to ±2.75 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

The OPA2376YZD is a lead (Pb)-free, die-level, die-size ball grid array (DSBGA) package. Unlike devices that are in plastic packages, these devices have no molding compound, lead frame, wire bonds, or leads. Using standard surface-mount assembly procedures, the DSBGA can be mounted to a printed circuit board (PCB) without additional underfill. Figure 33 and Figure 34 detail the pinout and package marking. See Application Note SBVA017, *NanoStar™ and NanoFree™ 300 µm Solder Bump WCSP*, for more detailed information on package characteristics and PCB design.

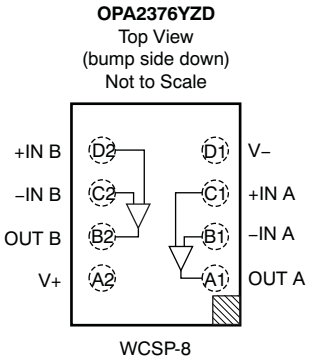


Figure 33. Pin Description

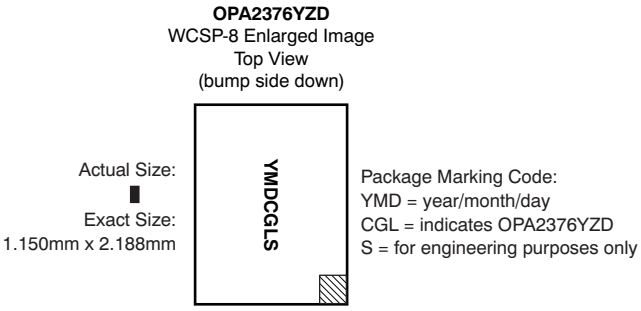


Figure 34. Top-View Package Marking

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2376AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2376	Samples
OPA2376AIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	Call TI | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OBBI	Samples
OPA2376AIDGKRG4	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 125	OBBI	Samples
OPA2376AIDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	Call TI | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OBBI	Samples
OPA2376AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2376	Samples
OPA2376AIDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 2376	Samples
OPA2376AIYZDR	ACTIVE	DSBGA	YZD	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	OPA2376	Samples
OPA2376AIYZDT	ACTIVE	DSBGA	YZD	8	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	OPA2376	Samples
OPA376AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 376	Samples
OPA376AIDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BUQ	Samples
OPA376AIDBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BUQ	Samples
OPA376AIDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BUQ	Samples
OPA376AIDBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BUQ	Samples
OPA376AIDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BUR	Samples
OPA376AIDCKRG4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BUR	Samples
OPA376AIDCKT	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BUR	Samples
OPA376AIDCKTG4	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BUR	Samples
OPA376AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 376	Samples
OPA376AIDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 376	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA4376AIPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4376	Samples
OPA4376AIPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4376	Samples
OPA4376AIPWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4376	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA2376, OPA376, OPA4376 :

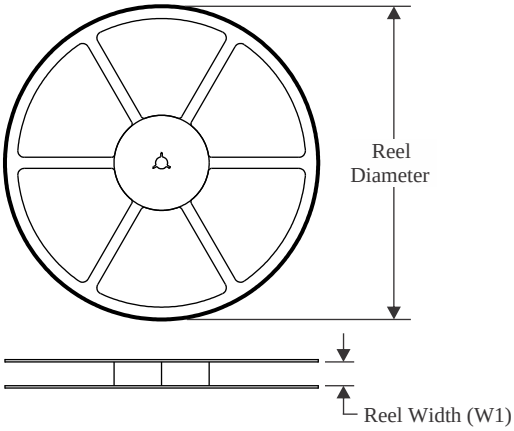
- Automotive : OPA2376-Q1, OPA376-Q1, OPA4376-Q1

NOTE: Qualified Version Definitions:

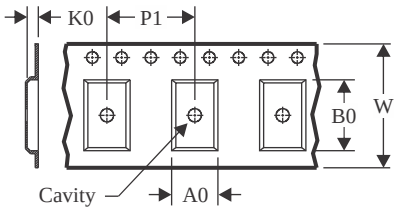
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

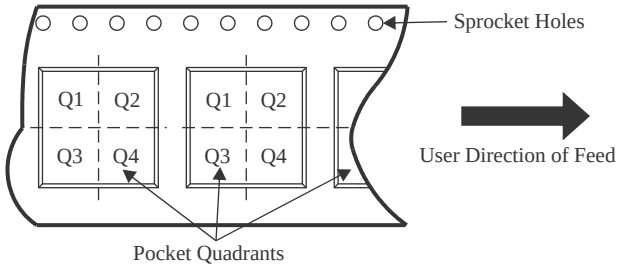


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

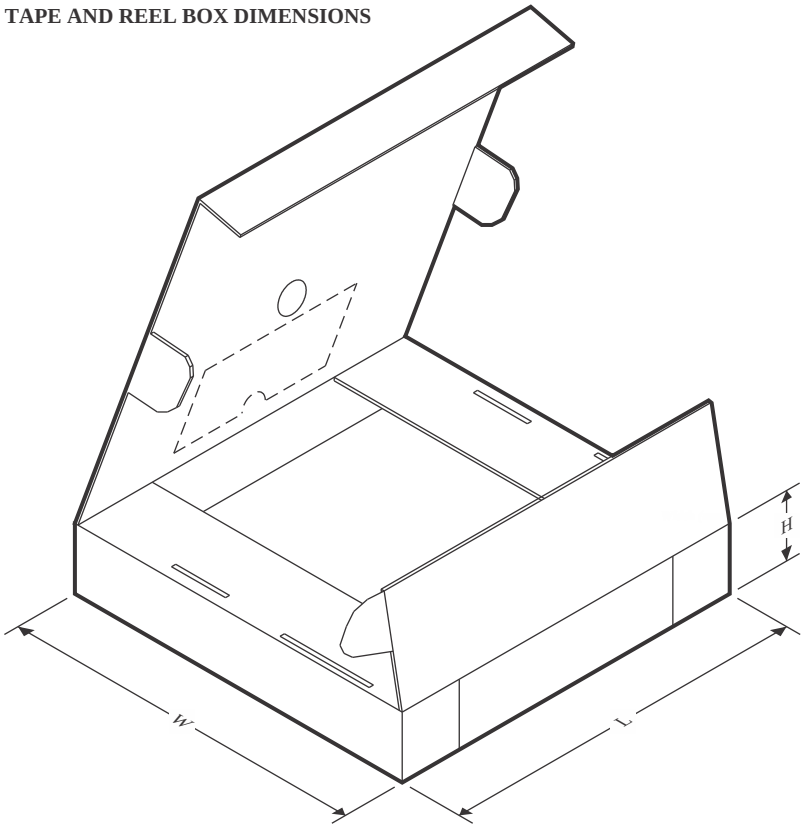
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2376AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2376AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2376AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2376AIYZDR	DSBGA	YZD	8	3000	180.0	8.4	1.24	2.29	0.81	4.0	8.0	Q1
OPA2376AIYZDT	DSBGA	YZD	8	250	180.0	8.4	1.24	2.29	0.81	4.0	8.0	Q1
OPA376AIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA376AIDBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA376AIDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA376AIDBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA376AIDCKR	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
OPA376AIDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA376AIDCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA376AIDCKT	SC70	DCK	5	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
OPA376AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4376AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

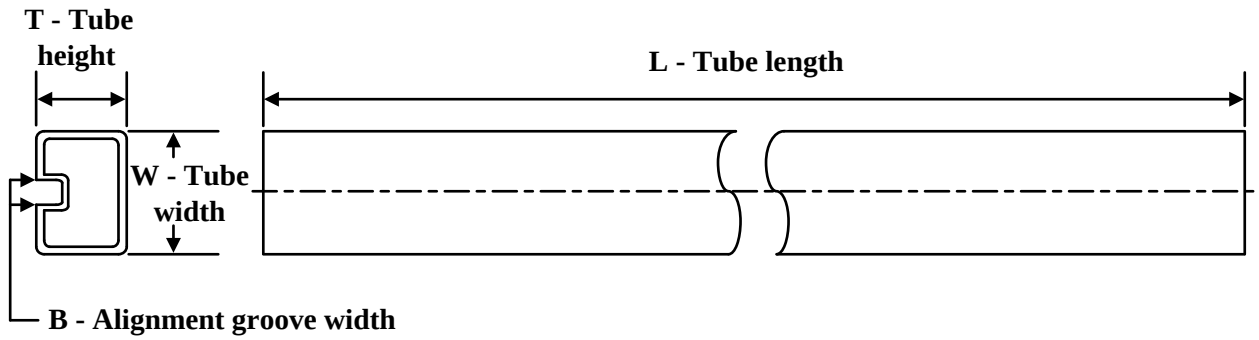
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2376AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2376AIDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA2376AIDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA2376AIYZDR	DSBGA	YZD	8	3000	182.0	182.0	20.0
OPA2376AIYZDT	DSBGA	YZD	8	250	182.0	182.0	20.0
OPA376AIDBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
OPA376AIDBVR	SOT-23	DBV	5	3000	213.0	191.0	35.0
OPA376AIDBVT	SOT-23	DBV	5	250	223.0	270.0	35.0
OPA376AIDBVT	SOT-23	DBV	5	250	213.0	191.0	35.0
OPA376AIDCKR	SC70	DCK	5	3000	213.0	191.0	35.0
OPA376AIDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
OPA376AIDCKT	SC70	DCK	5	250	180.0	180.0	18.0
OPA376AIDCKT	SC70	DCK	5	250	213.0	191.0	35.0
OPA376AIDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA4376AIPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

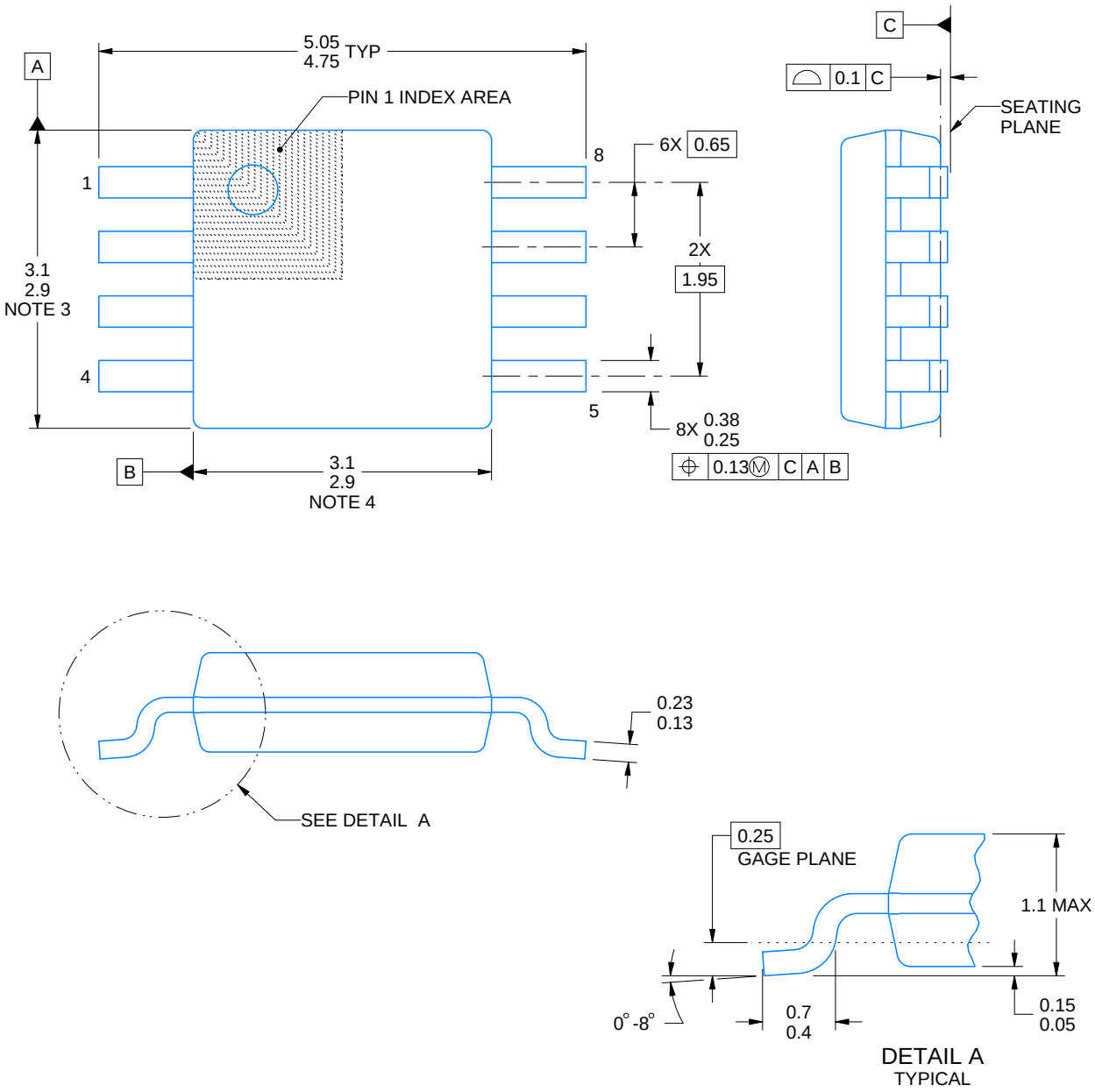
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2376AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA376AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA4376AIPW	PW	TSSOP	14	90	508	8.5	3250	2.8

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

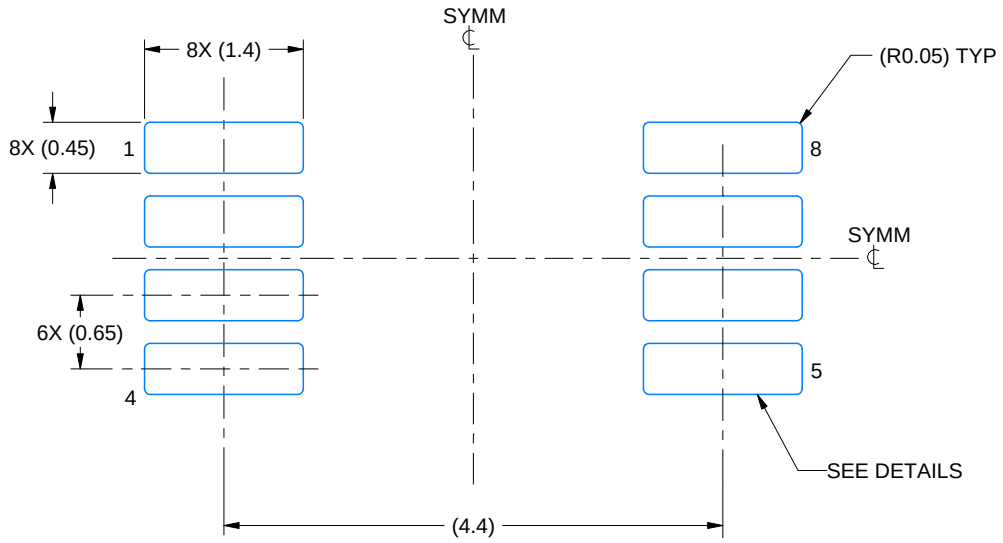
SMALL OUTLINE PACKAGE



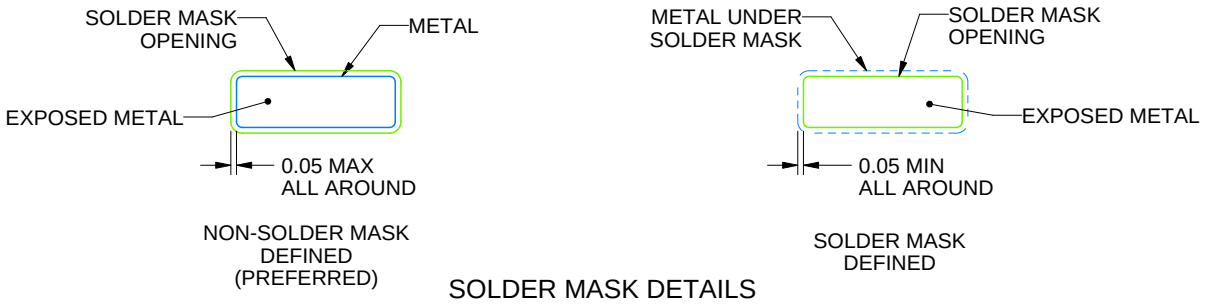
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

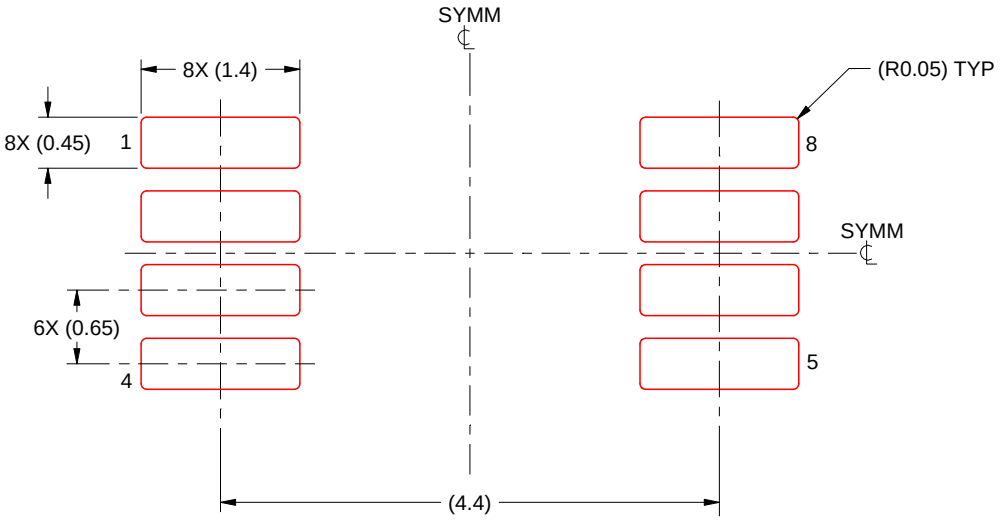


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

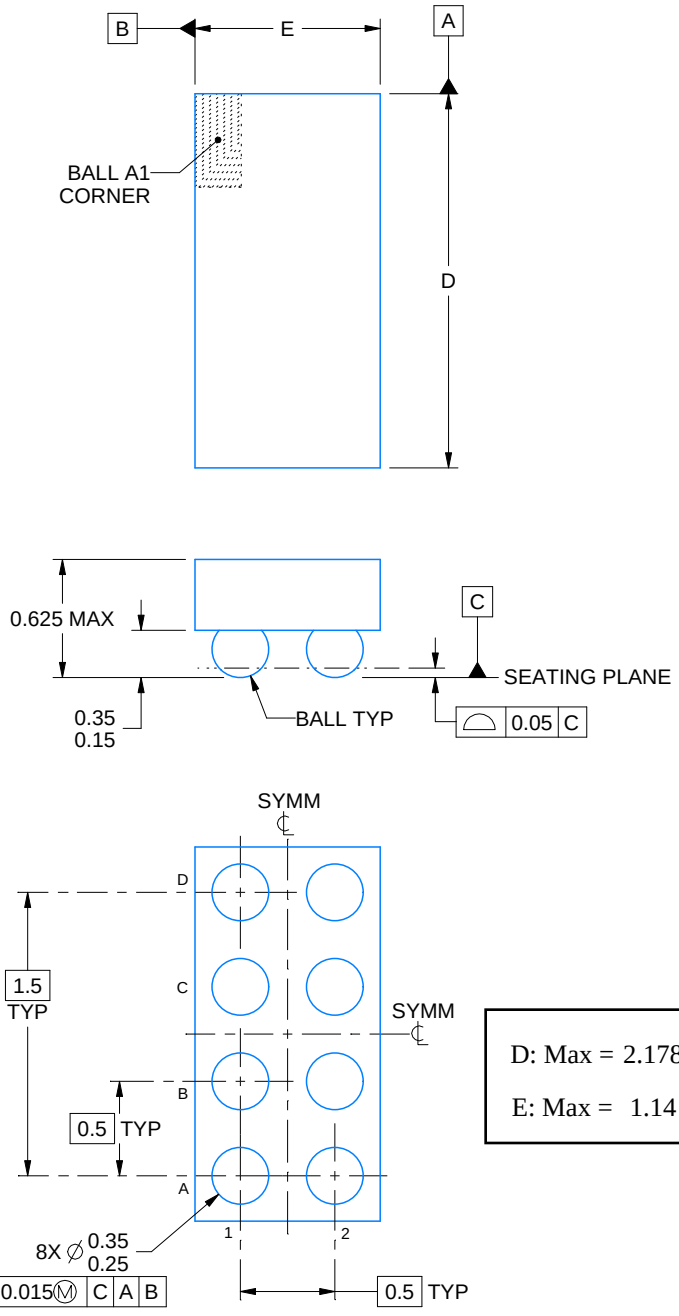
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

YZD0008

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



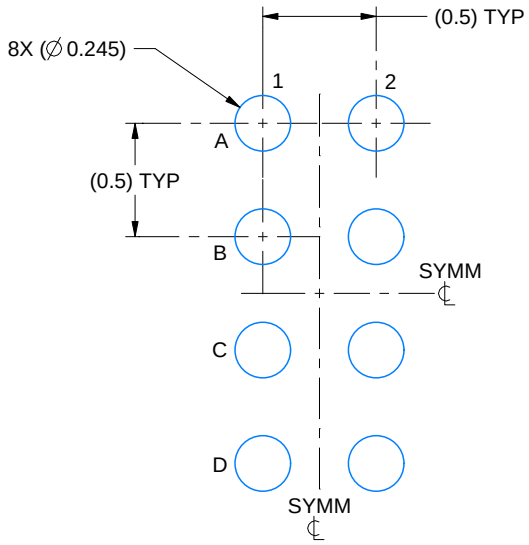
D: Max = 2.178 mm, Min =2.118 mm

E: Max = 1.14 mm, Min = 1.08 mm

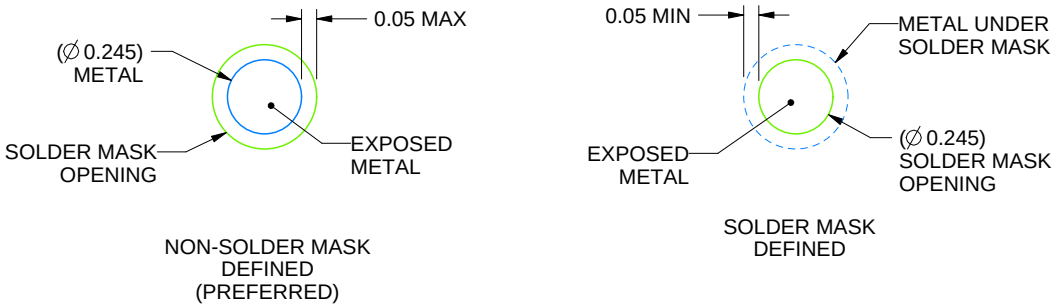
4219545/A 12/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X

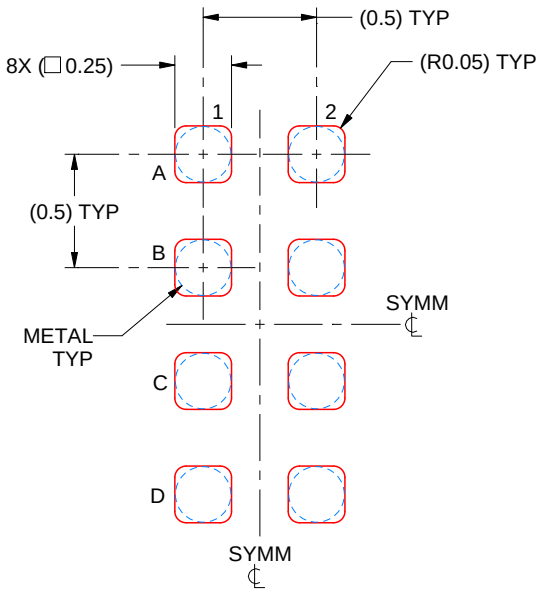


SOLDER MASK DETAILS
NOT TO SCALE

4219545/A 12/2018

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 30X

4219545/A 12/2018

NOTES: (continued)

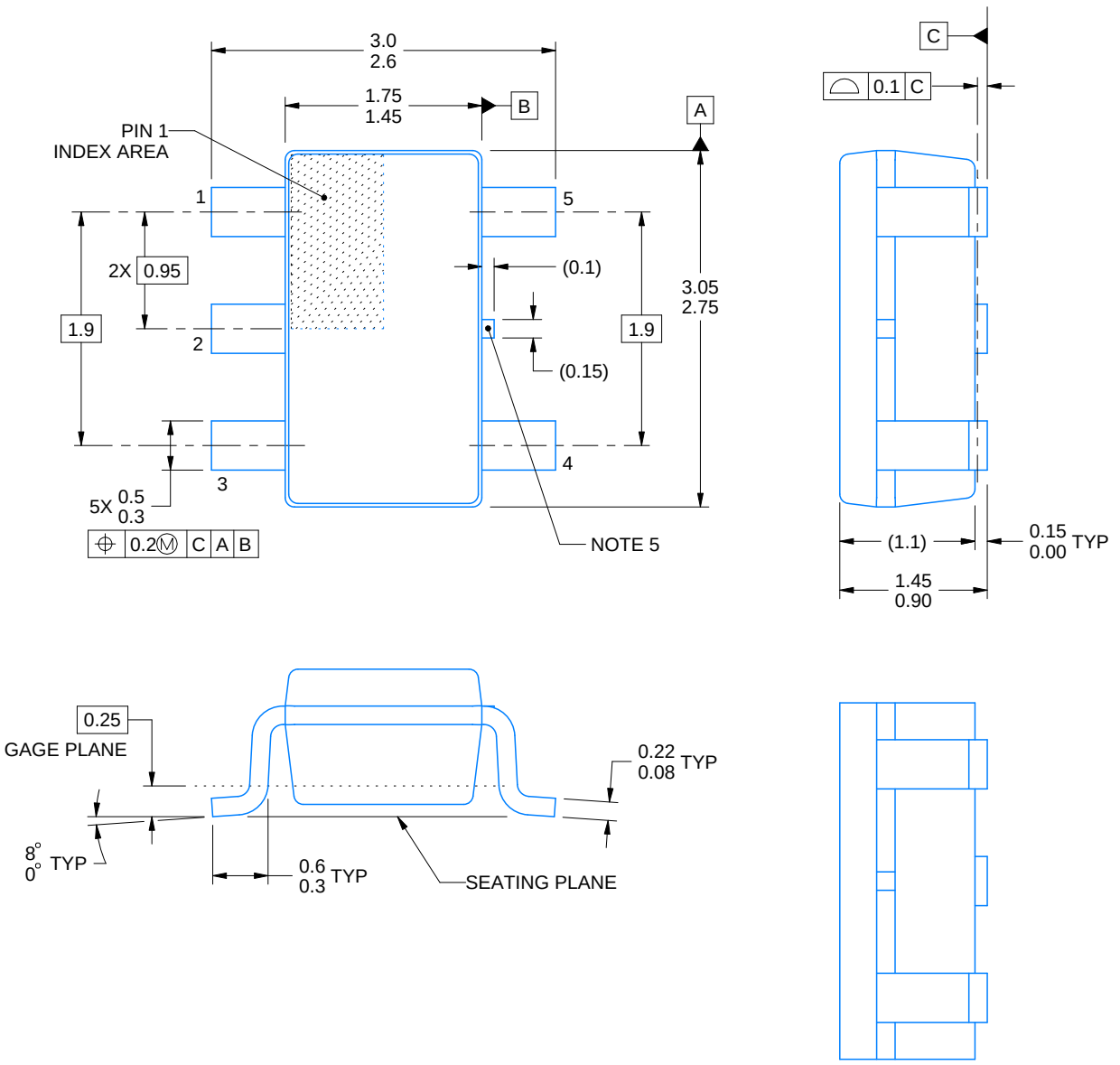
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

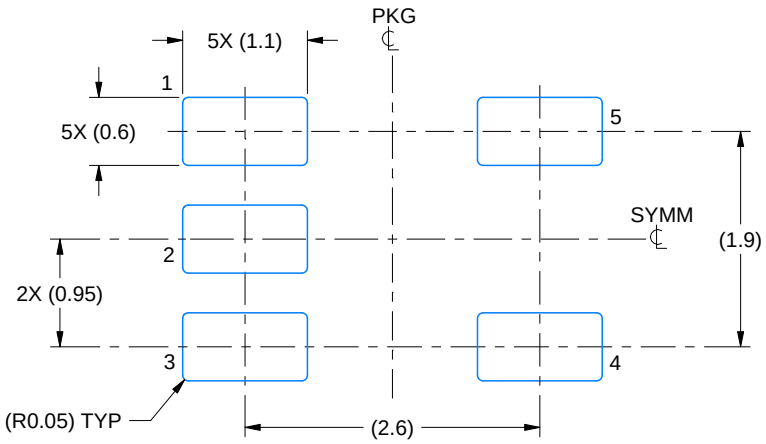


ALTERNATIVE PACKAGE SINGULATION VIEW

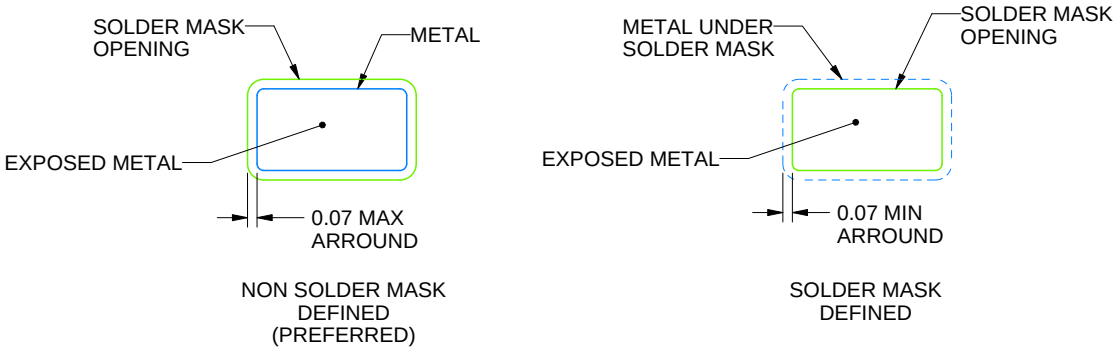
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

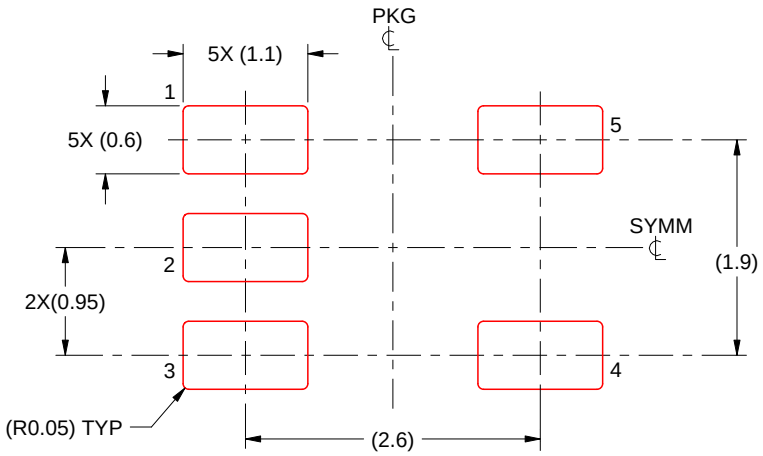


SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

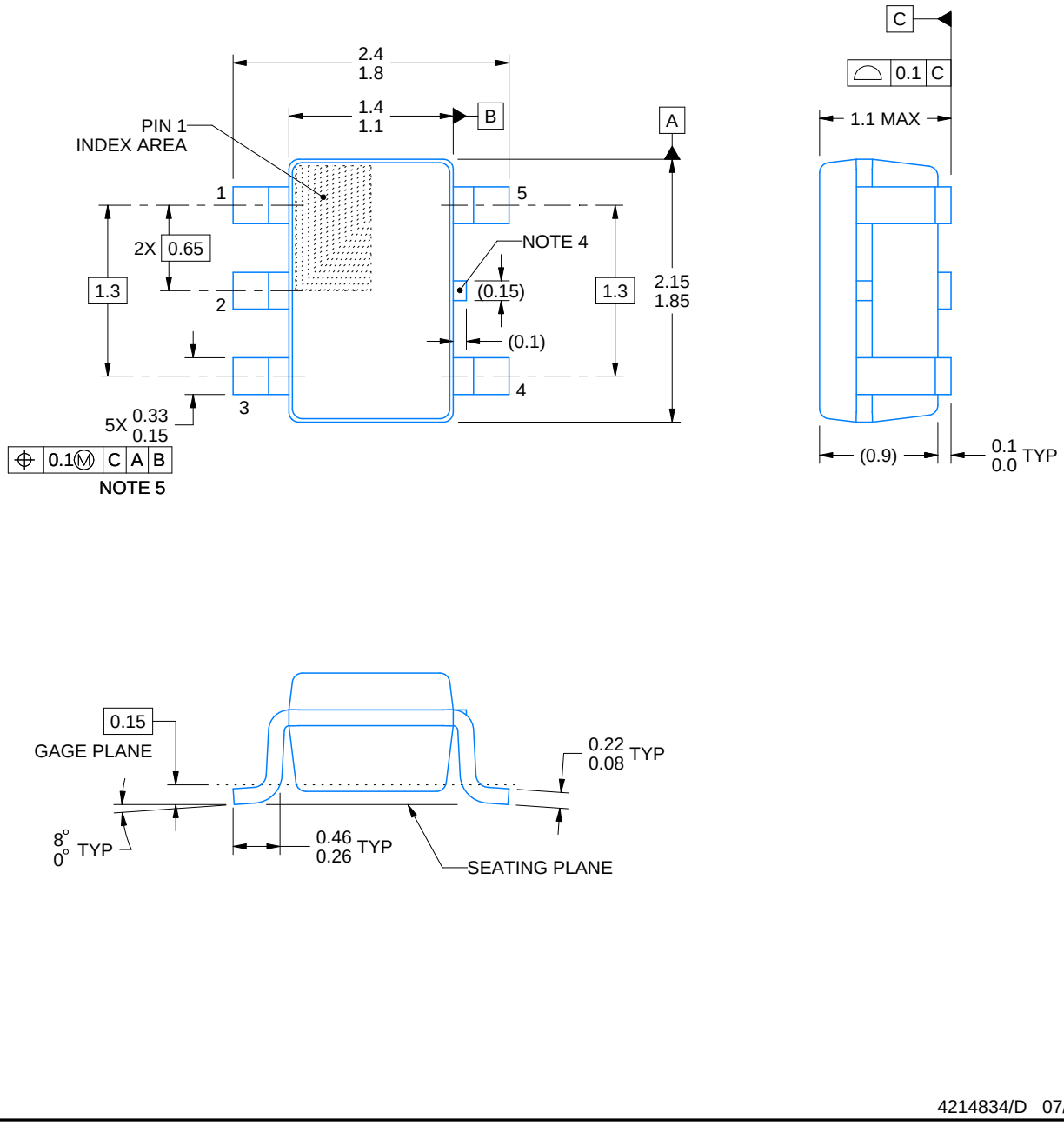
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

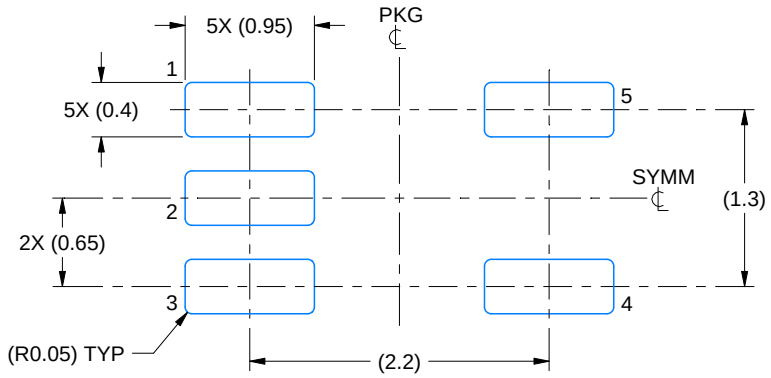
SMALL OUTLINE TRANSISTOR



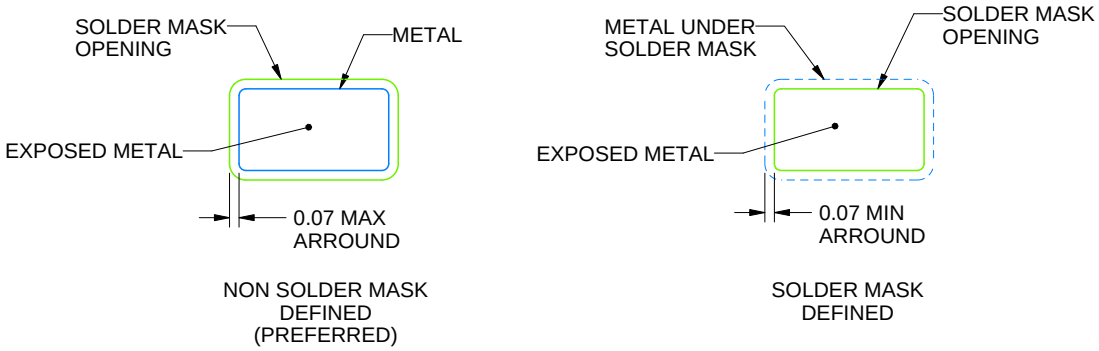
4214834/D 07/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

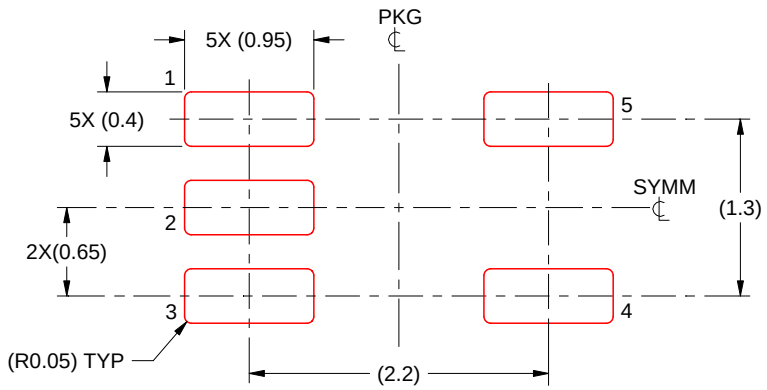


SOLDER MASK DETAILS

4214834/D 07/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



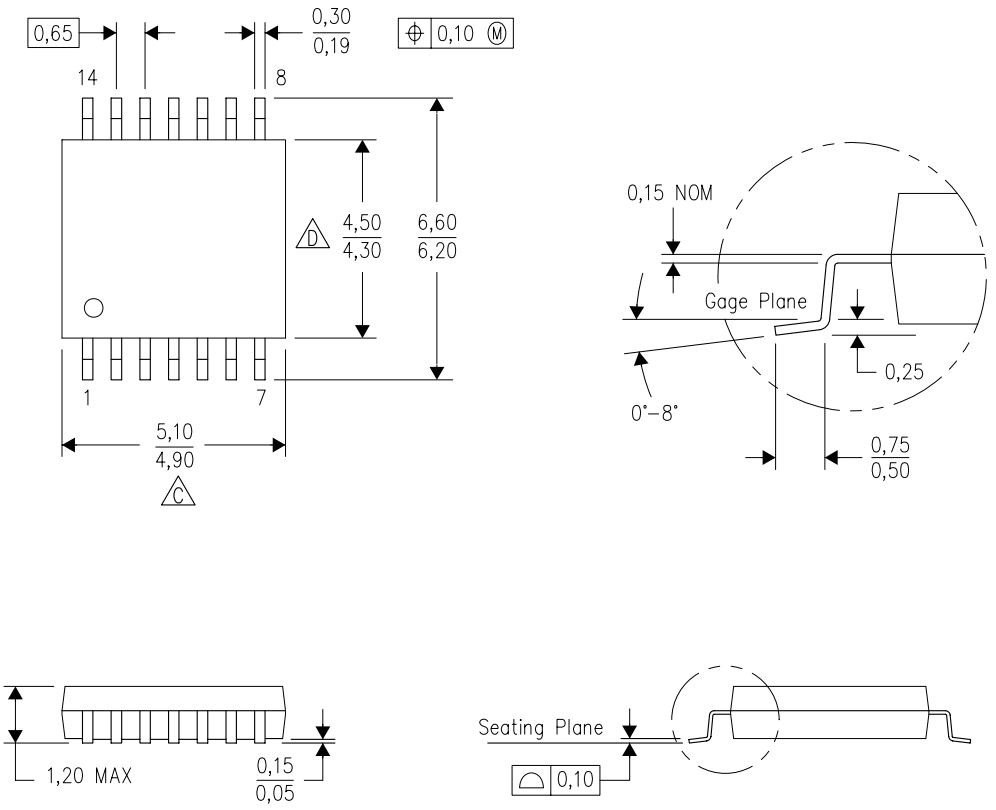
SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/D 07/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

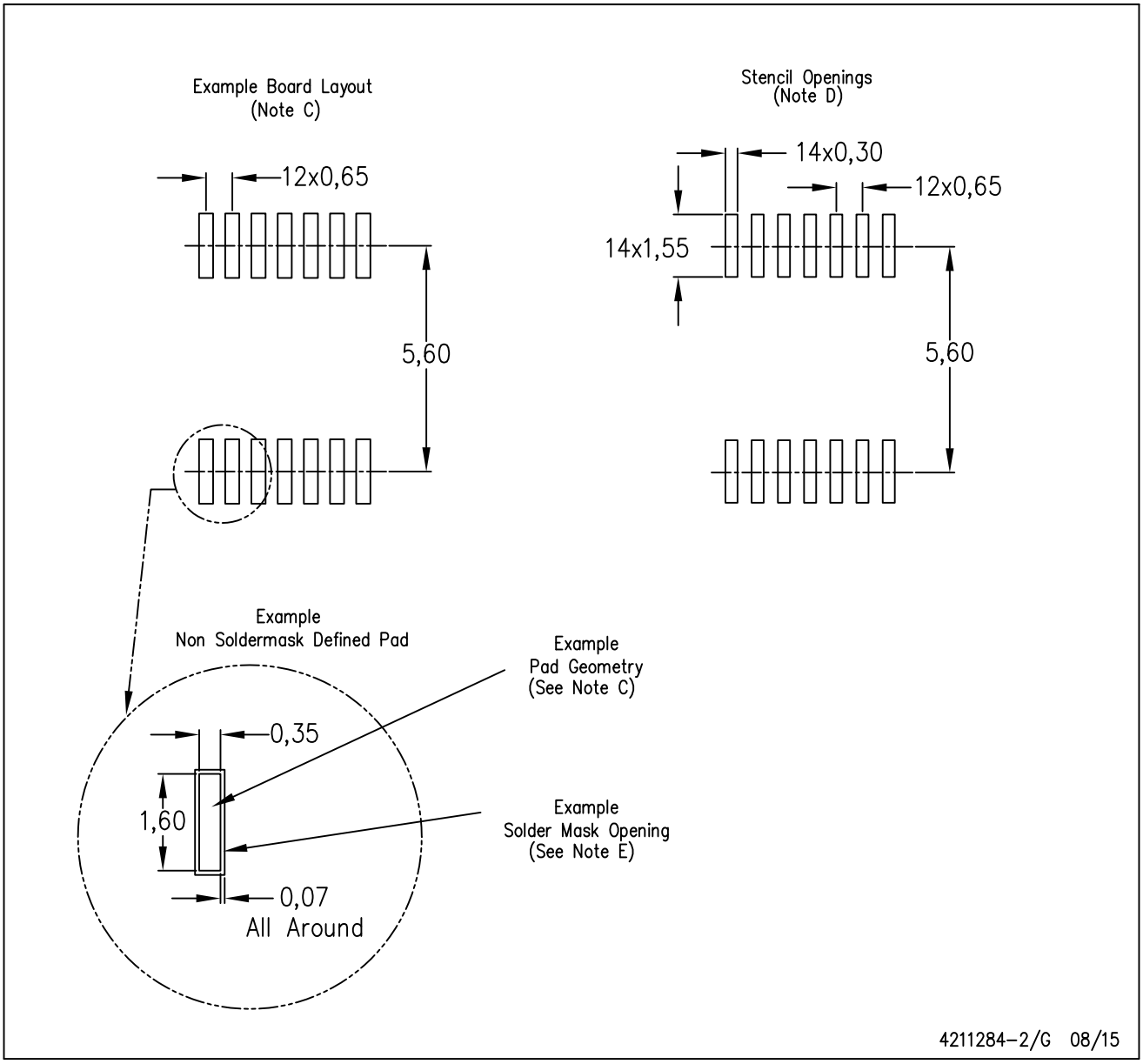
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



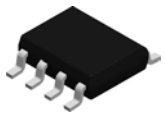
4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

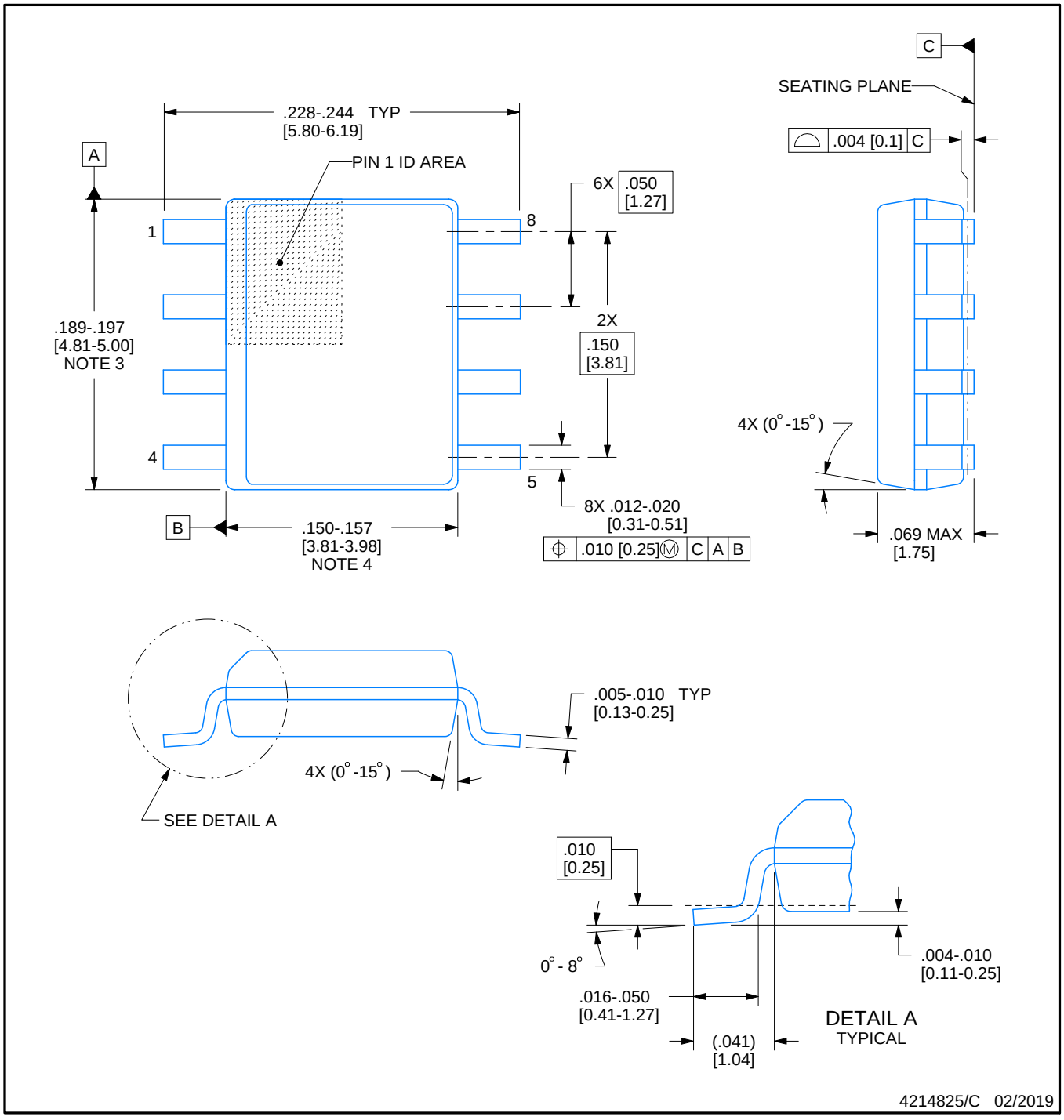


PACKAGE OUTLINE

D0008A

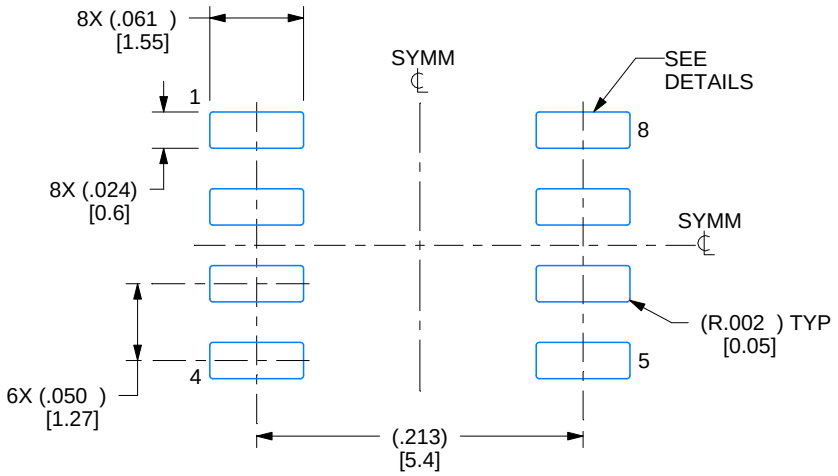
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

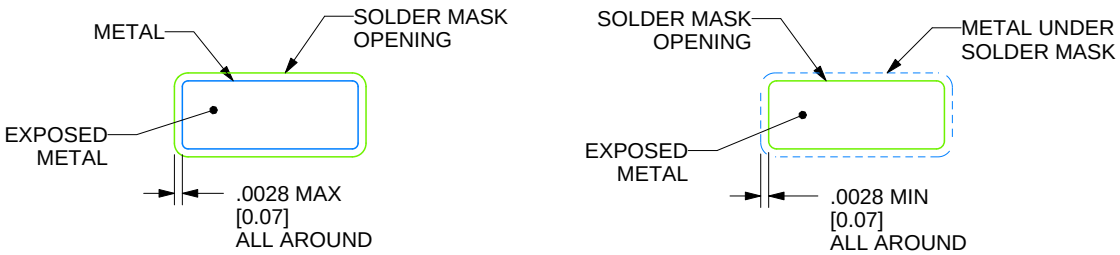


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

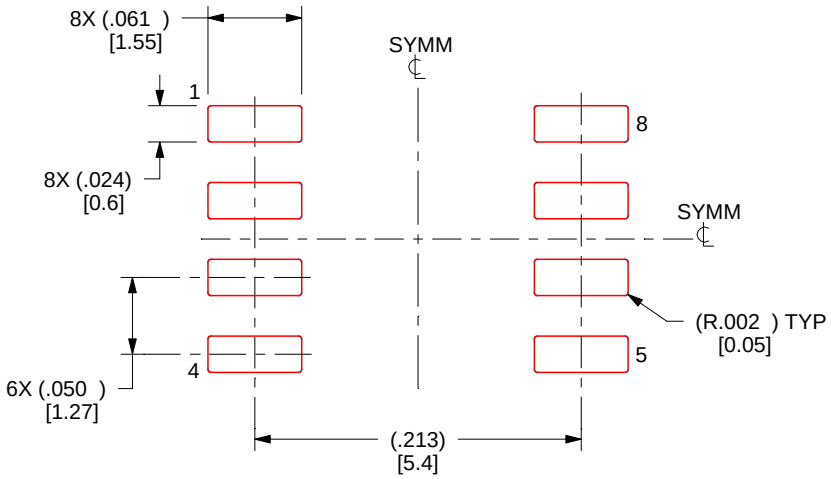
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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