



THE DATASHEET OF OPA121KU/2K5



OPA121

Low Cost Precision *Difet*[®] OPERATIONAL AMPLIFIER

FEATURES

- LOW NOISE: $6\text{nV}/\sqrt{\text{Hz}}$ typ at 10kHz
- LOW BIAS CURRENT: 5pA max
- LOW OFFSET: 2mV max
- LOW DRIFT: $3\mu\text{V}/^\circ\text{C}$ typ
- HIGH OPEN-LOOP GAIN: 110dB min
- HIGH COMMON-MODE REJECTION: 86dB min

APPLICATIONS

- OPTOELECTRONICS
- DATA ACQUISITION
- TEST EQUIPMENT
- MEDICAL EQUIPMENT
- RADIATION HARD EQUIPMENT

DESCRIPTION

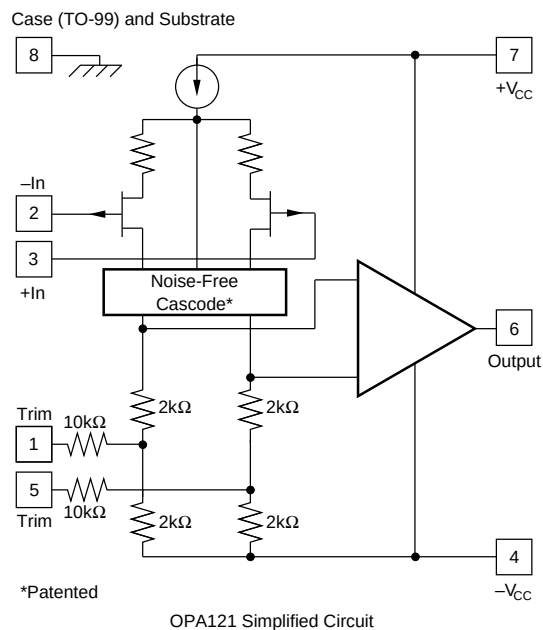
The OPA121 is a precision monolithic dielectrically-isolated FET (*Difet*[®]) operational amplifier. Outstanding performance characteristics are now available for low-cost applications.

Noise, bias current, voltage offset, drift, open-loop gain, common-mode rejection, and power supply rejection are superior to BIFET[®] amplifiers.

Very low bias current is obtained by dielectric isolation with on-chip guarding.

Laser-trimming of thin-film resistors gives very low offset and drift. Extremely low noise is achieved with new circuit design techniques (patented). A new cascode design allows high precision input specifications and reduced susceptibility to flicker noise.

Standard 741 pin configuration allows upgrading of existing designs to higher performance levels.



Difet[®], Burr-Brown Corp.
BIFET[®], National Semiconductor Corp.

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SPECIFICATIONS

ELECTRICAL

At $V_{CC} = \pm 15\text{VDC}$ and $T_A = +25^\circ\text{C}$ unless otherwise noted. Pin 8 connected to ground.

PARAMETER	CONDITIONS	OPA121KM			OPA121KP, KU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT NOISE Voltage, $f_o = 10\text{Hz}$ $f_o = 100\text{Hz}$ $f_o = 1\text{kHz}$ $f_o = 10\text{kHz}$ $f_B = 10\text{Hz}$ to 10kHz $f_B = 0.1\text{Hz}$ to 10Hz Current, $f_B = 0.1\text{Hz}$ to 10Hz $f_o = 0.1\text{Hz}$ thru 20kHz	(1) (1) (1) (1) (1) (1) (1) (1)		40 15 8 6 0.7 1.6 15 0.8			50 18 10 7 0.8 2 21 1.1		$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ μVrms $\mu\text{Vp-p}$ fA, p-p $\text{fA}/\sqrt{\text{Hz}}$
OFFSET VOLTAGE ⁽²⁾ Input Offset Voltage Average Drift Supply Rejection	$V_{CM} = 0\text{VDC}$ $T_A = T_{MIN}$ to T_{MAX}	86	± 0.5 ± 3 ± 6	± 2 ± 10 ± 50	86	± 0.5 ± 3 ± 6	± 3 ± 10 ± 50	mV $\mu\text{V}/^\circ\text{C}$ dB $\mu\text{V/V}$
BIAS CURRENT ⁽²⁾ Input Bias Current	$V_{CM} = 0\text{VDC}$ Device Operating		± 1	± 5		± 1	± 10	pA
OFFSET CURRENT ⁽²⁾ Input Offset Current	$V_{CM} = 0\text{VDC}$ Device Operating		± 0.7	± 4		± 0.7	± 8	pA
IMPEDANCE Differential Common-Mode			$10^{13} \parallel 1$ $10^{14} \parallel 3$			$10^{13} \parallel 1$ $10^{14} \parallel 3$		$\Omega \parallel \text{pF}$ $\Omega \parallel \text{pF}$
VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection	$V_{IN} = \pm 10\text{VDC}$	± 10 86	± 11 104		± 10 82	± 11 100		V dB
OPEN-LOOP GAIN, DC Open-Loop Voltage Gain	$R_L \geq 2\text{k}\Omega$	110	120		106	114		dB
FREQUENCY RESPONSE Unity Gain, Small Signal Full Power Response Slew Rate Settling Time, 0.1% 0.01% Overload Recovery, 50% Overdrive ⁽³⁾	20Vp-p, $R_L = 2\text{k}\Omega$ $V_O = \pm 10\text{V}$, $R_L = 2\text{k}\Omega$ Gain = -1, $R_L = 2\text{k}\Omega$ 10V Step Gain = -1		2 32 2 6 10 5			2 32 2 6 10 5		MHz kHz V/ μs μs μs μs
RATED OUTPUT Voltage Output Current Output Output Resistance Load Capacitance Stability Short Circuit Current	$R_L = 2\text{k}\Omega$ $V_O = \pm 10\text{VDC}$ DC, Open Loop Gain = +1	± 11 ± 5.5	± 12 ± 10 100 1000 40		± 11 ± 5.5	± 12 ± 10 100 1000 40		V mA Ω pF mA
POWER SUPPLY Rated Voltage Voltage Range, Derated Performance Current, Quiescent	$I_O = 0\text{mADC}$	± 5	± 15 2.5	± 18 4	± 5	± 15 2.5	± 18 4.5	VDC VDC mA
TEMPERATURE RANGE Specification Operating Storage θ Junction-Ambient	Ambient Temperature Ambient Temperature Ambient Temperature	0 -40 -65		+70 +85 +150	0 -25 -55		+70 +85 +125	$^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C/W}$
			200			150 ⁽⁴⁾		

NOTES: (1) Sample tested. (2) Offset voltage, offset current, and bias current are specified with the units fully warmed up. (3) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive. (4) 100°C/W for KU grade.

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ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At $V_{CC} = \pm 15\text{VDC}$ and $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.

PARAMETER	CONDITIONS	OPA121KM			OPA121KP, KU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE Specification Range	Ambient Temperature	0		+70	0		+70	°C
INPUT OFFSET VOLTAGE⁽¹⁾ Input Offset Voltage Average Drift Supply Rejection	$V_{CM} = 0\text{VDC}$		± 1 ± 3 94 ± 20	± 3 ± 10 ± 80		± 1 ± 3 94 ± 20	± 5 ± 10 ± 80	mV $\mu\text{V}/^\circ\text{C}$ dB $\mu\text{V}/\text{V}$
BIAS CURRENT⁽¹⁾ Input Bias Current	$V_{CM} = 0\text{VDC}$ Device Operating		± 23	± 115		± 23	± 250	pA
OFFSET CURRENT⁽¹⁾ Input Offset Current	$V_{CM} = 0\text{VDC}$ Device Operating		± 16	± 100		± 16	± 200	pA
VOLTAGE RANGE Common-Mode Input Range Common-Mode Rejection	$V_{IN} = \pm 10\text{VDC}$	± 10 82	± 11 98		± 10 80	± 11 96		V dB
OPEN-LOOP GAIN, DC Open-Loop Voltage Gain	$R_L \geq 2\text{k}\Omega$	106	116		100	110		dB
RATED OUTPUT Voltage Output Current Output Short Circuit Current	$R_L = 2\text{k}\Omega$ $V_O = \pm 10\text{VDC}$ $V_O = 0\text{VDC}$	± 10.5 ± 5.25 10	± 11 ± 10 40		± 10.5 ± 5.25 10	± 11 ± 10 40		V mA mA
POWER SUPPLY Current, Quiescent	$I_O = 0\text{mADC}$		2.5	4.5		2.5	5	mA

NOTE: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

ABSOLUTE MAXIMUM RATINGS

Supply	$\pm 18\text{VDC}$
Internal Power Dissipation ⁽¹⁾	500mW
Differential Input Voltage	$\pm 36\text{VDC}$
Input Voltage Range	$\pm 18\text{VDC}$
Storage Temperature Range	
M package	-65°C to $+150^\circ\text{C}$
P, U packages	-55°C to $+125^\circ\text{C}$
Operating Temperature Range	
M package	-40°C to $+85^\circ\text{C}$
P, U packages	-25°C to $+85^\circ\text{C}$
Lead Temperature	
M, P packages (soldering, 10s)	$+300^\circ\text{C}$
U package (soldering, 3s)	$+260^\circ\text{C}$
Output Short-Circuit Duration ⁽²⁾	Continuous
Junction Temperature	$+175^\circ\text{C}$

NOTES: (1) Packages must be derated based on $\theta_{JA} = 150^\circ\text{C}/\text{W}$ (P package); $\theta_{JA} = 200^\circ\text{C}/\text{W}$ (M package); $\theta_{JA} = 100^\circ\text{C}/\text{W}$ (U package).
(2) Short circuit may be to power supply common only. Rating applies to $+25^\circ\text{C}$ ambient. Observe dissipation limit and T_J .

PACKAGE INFORMATION

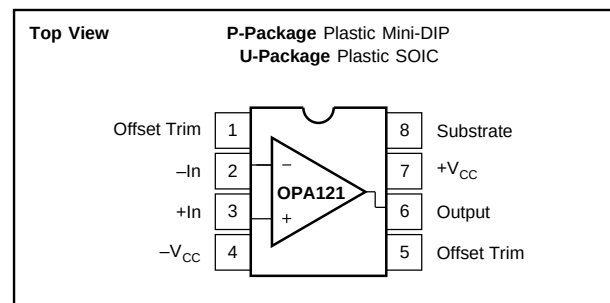
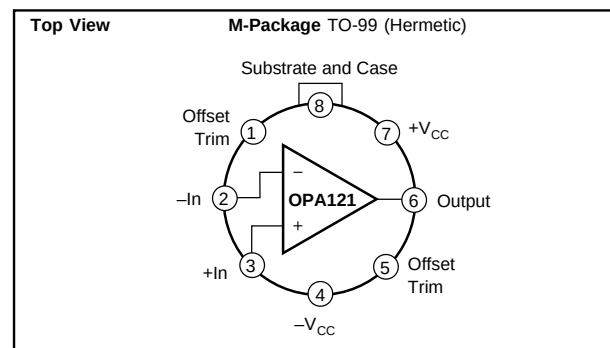
MODEL	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾
OPA121KM	TO-99	001
OPA121KP	8-Pin Plastic DIP	006
OPA121KU	8-Pin SOIC	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

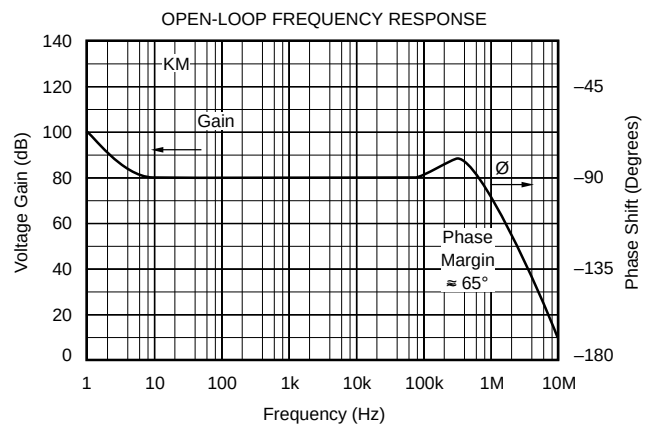
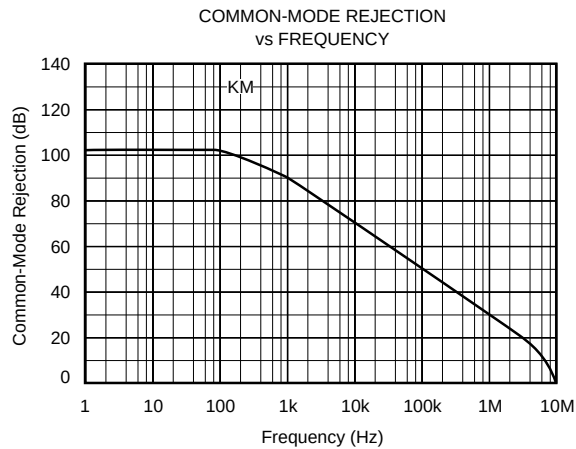
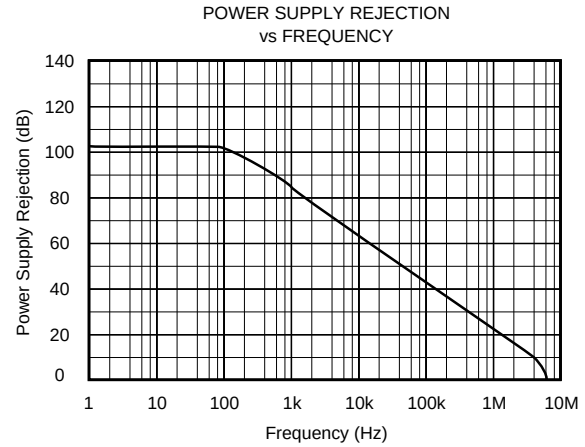
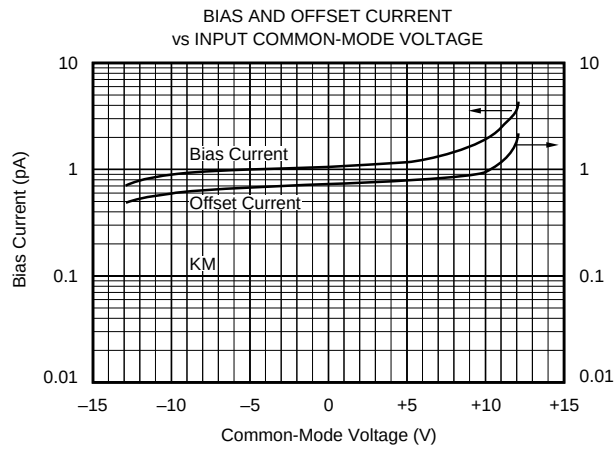
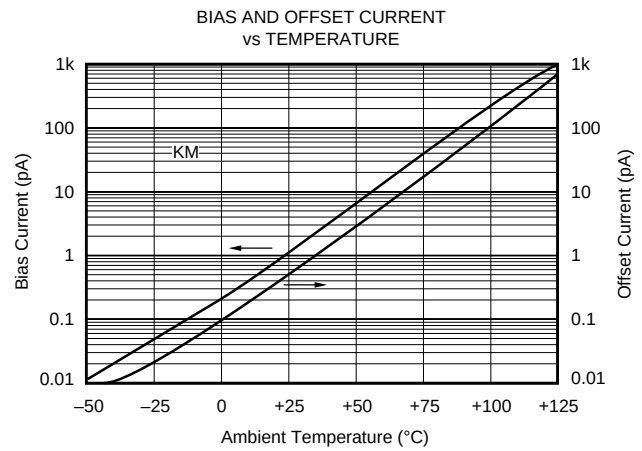
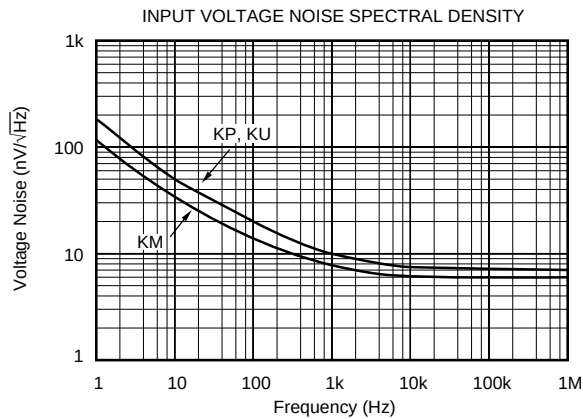
MODEL	PACKAGE	TEMPERATURE RANGE
OPA121KM	TO-99	0°C to $+70^\circ\text{C}$
OPA121KP	8-Pin Plastic DIP	0°C to $+70^\circ\text{C}$
OPA121KU	8-Pin SOIC	0°C to $+70^\circ\text{C}$

CONNECTION DIAGRAMS



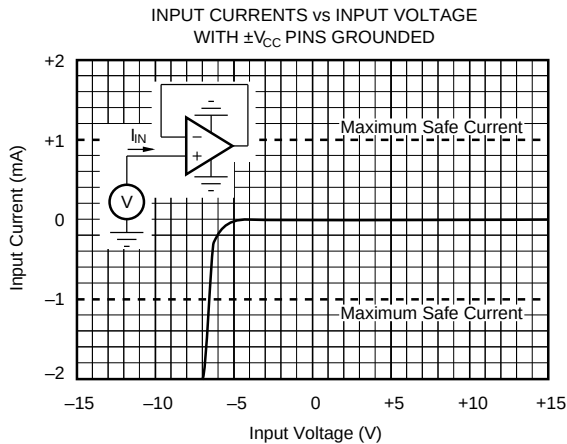
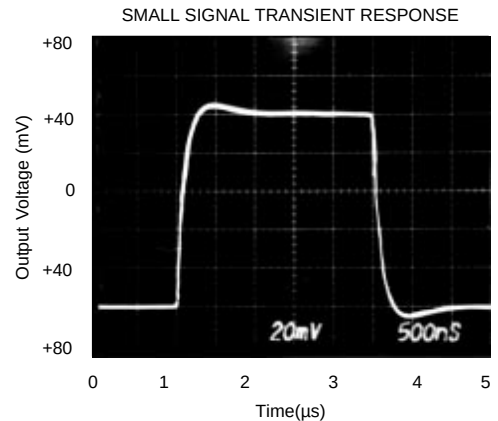
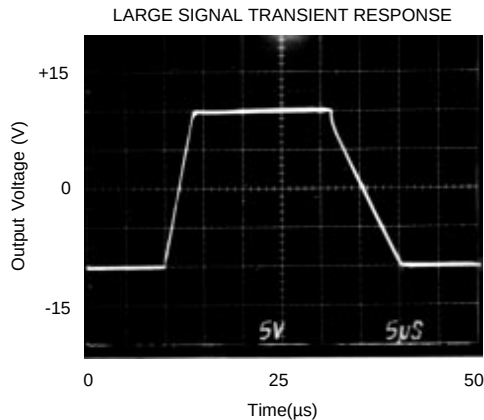
TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_{CC} = \pm 15\text{VDC}$ unless otherwise noted.



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA121 offset voltage is laser-trimmed and will require no further trim for most applications. As with most amplifiers, externally trimming the remaining offset can change drift performance by about $0.3\mu\text{V}/^\circ\text{C}$ for each $100\mu\text{V}$ of adjusted offset. Note that the trim (Figure 1) is similar to operational amplifiers such as 741 and AD547. The OPA121 can replace most BIFET amplifiers by leaving the external null circuit unconnected.

INPUT PROTECTION

Conventional monolithic FET operational amplifiers require external current-limiting resistors to protect their inputs against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET amplifiers can be destroyed by the loss of $-V_{CC}$.

Unlike BIFET amplifiers, the **Difet** OPA121 requires input current limiting resistors only if its input voltage is greater

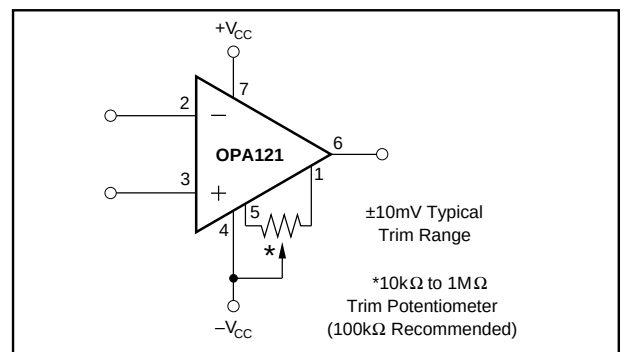


FIGURE 1. Offset Voltage Trim.

than 6V more negative than $-V_{CC}$. A $10\text{k}\Omega$ series resistor will limit input current to a safe level with up to $\pm 15\text{V}$ input levels even if both supply voltages are lost.

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types),

this may cause a noticeable degradation of offset voltage and drift.

Static protection is recommended when handling any precision IC operational amplifier.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce “hum” pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA121. To avoid leakage problems, it is recommended that the signal input lead of the OPA121 be wired to a Teflon™ standoff. If the OPA121 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A “guard” pattern should completely surround the high-impedance input leads and should be connected to a low-impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup (see Figure #2).

If guarding is not required, pin 8 (case) should be connected to ground.

BIAS CURRENT CHANGE VERSUS COMMON-MODE VOLTAGE

The input bias currents of most popular BIFET operational amplifiers are affected by common-mode voltage (Figure 3). Higher input FET gate-to-drain voltage causes leakage and ionization (bias) currents to increase. Due to its cascode input stage, the extremely-low bias current of the OPA121 is not compromised by common-mode voltage.

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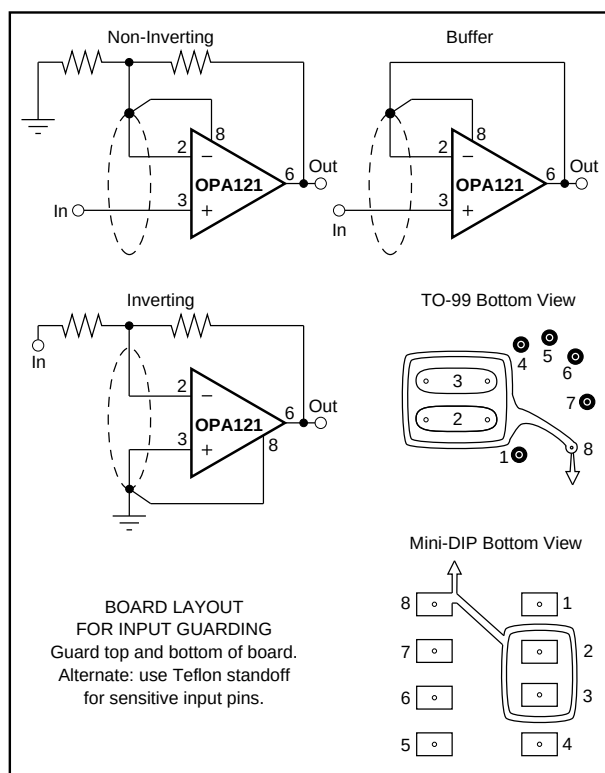


FIGURE 2. Connection of Input Guard.

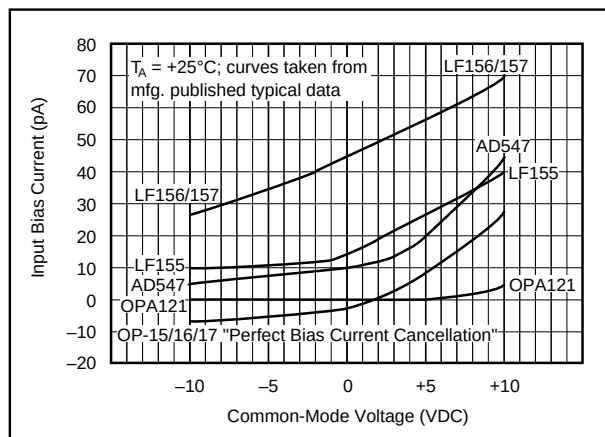


FIGURE 3. Input Bias Current vs Common-Mode Voltage.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA121KU	OBSOLETE	SOIC	D	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	OPA 121KU	
OPA121KU/2K5	OBSOLETE	SOIC	D	8		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	OPA 121KU	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

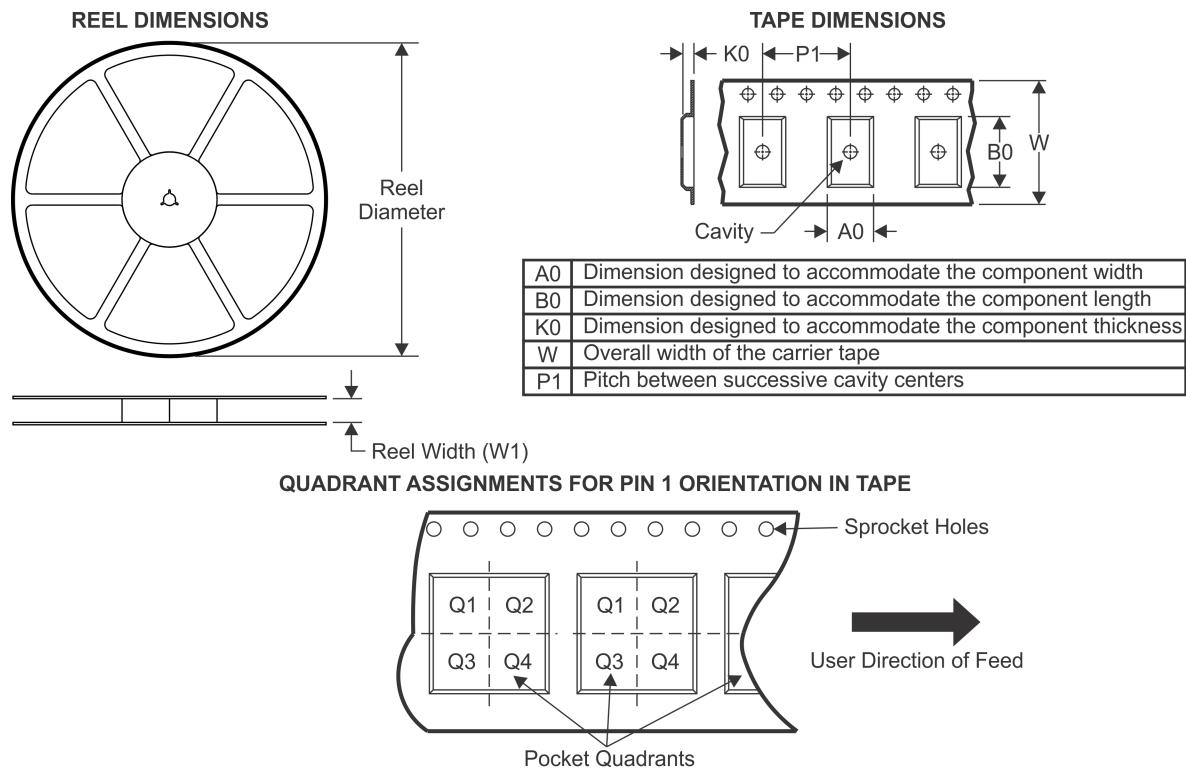
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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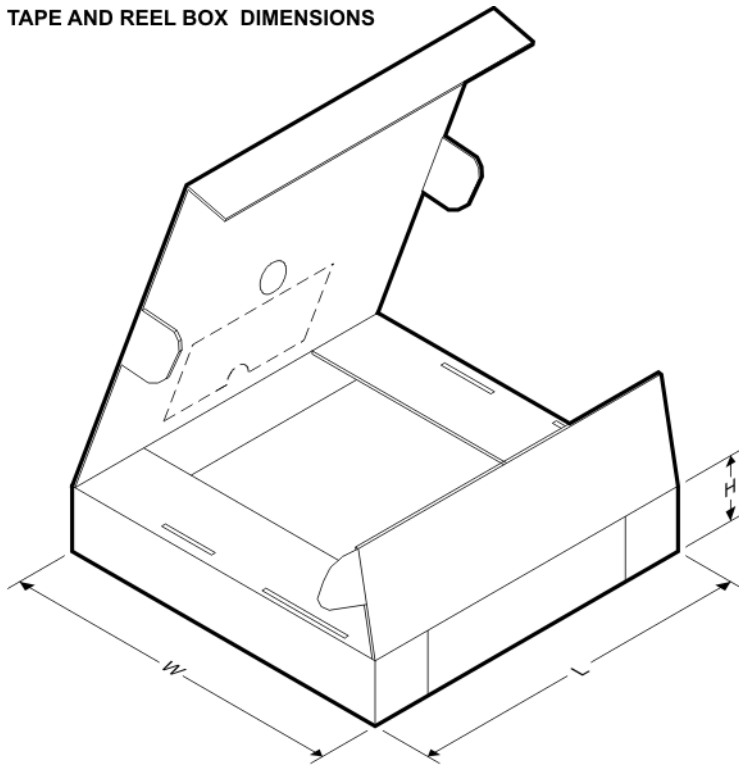
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TAPE AND REEL INFORMATION


*All dimensions are nominal

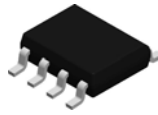
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA121KU/2K5	SOIC	D	8	0	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA121KU/2K5	SOIC	D	8	0	367.0	367.0	35.0

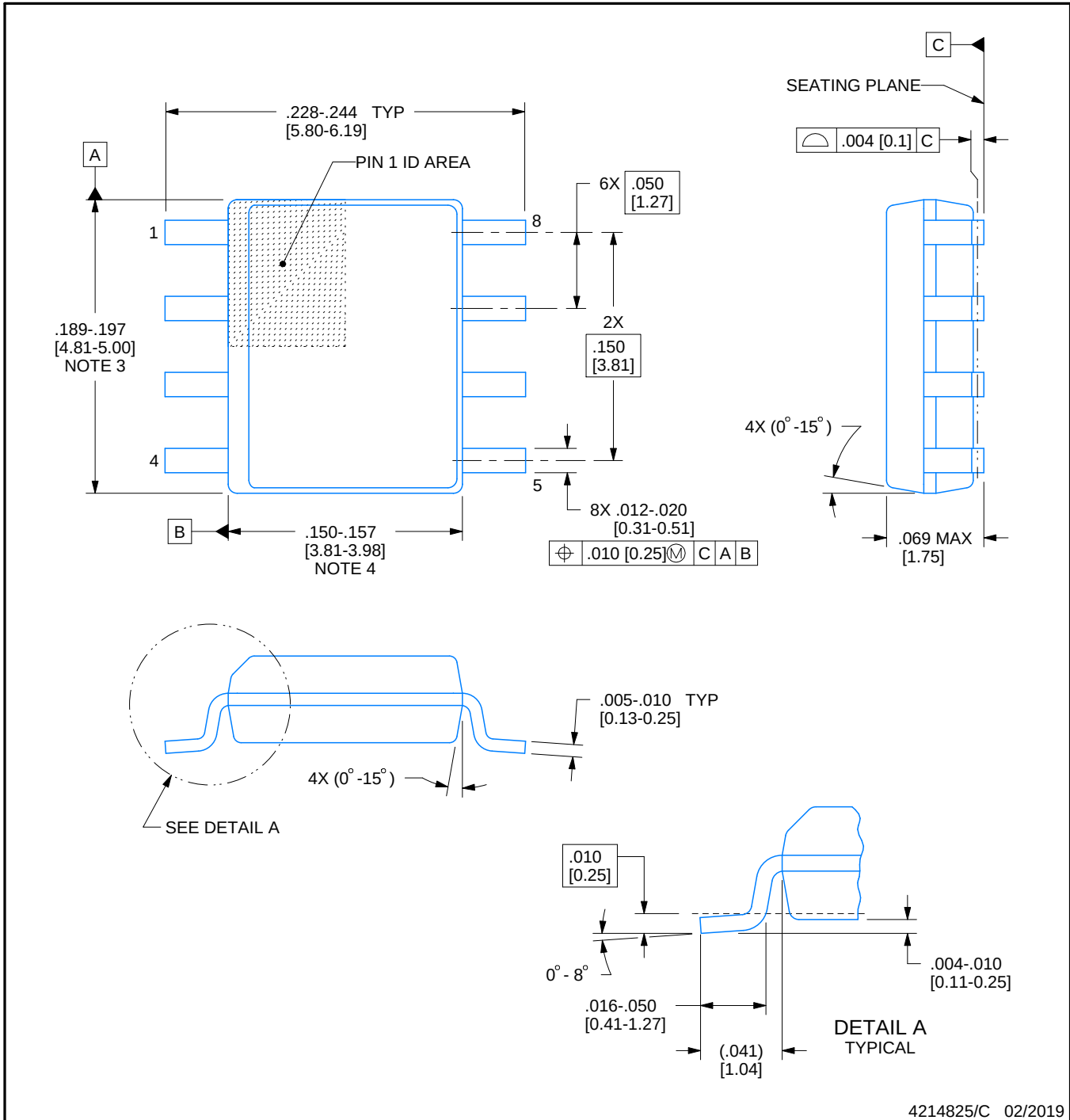


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

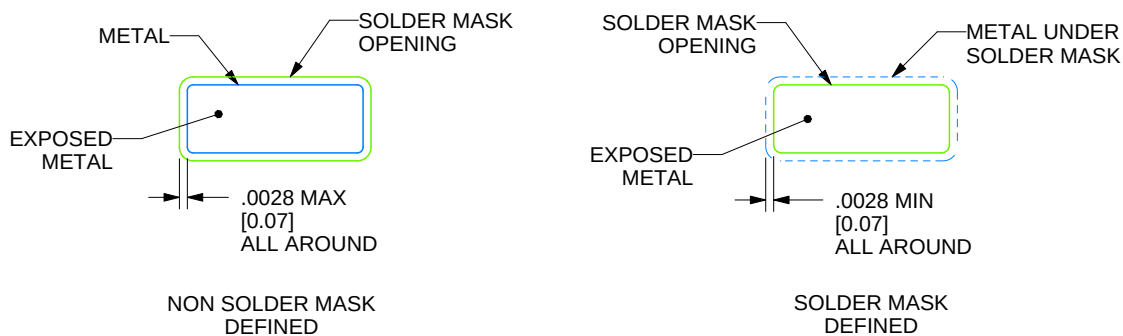
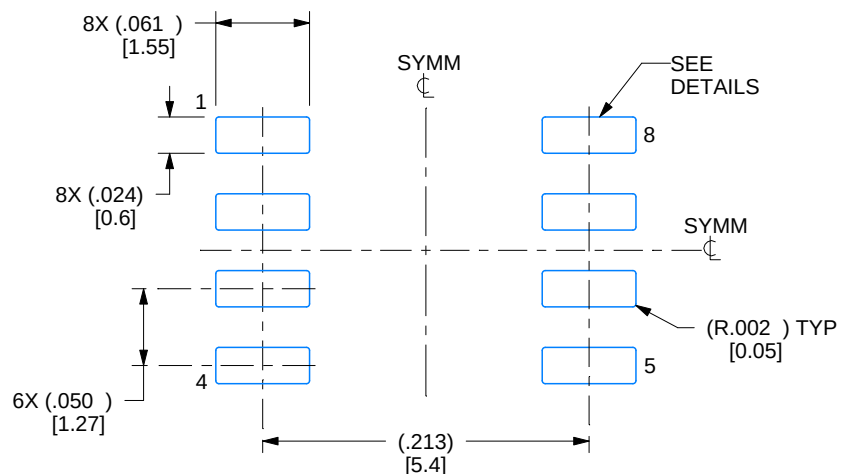
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

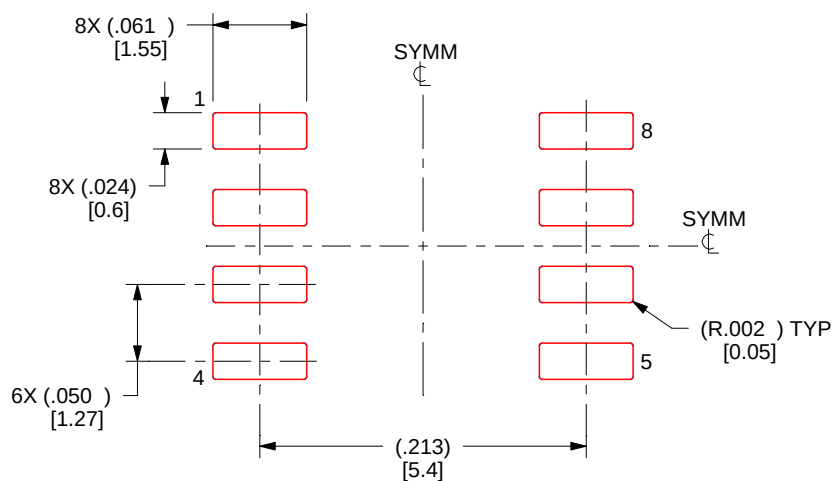
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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