



# THE DATASHEET OF OP285GSZ



## FEATURES

**Low offset voltage: 250  $\mu$ V**  
**Low noise: 6 nV/ $\sqrt{\text{Hz}}$**   
**Low distortion: 0.0006%**  
**High slew rate: 22 V/ $\mu$ s**  
**Wide bandwidth: 9 MHz**  
**Low supply current: 5 mA**  
**Low offset current: 2 nA**  
**Unity-gain stable**  
**8-lead SOIC\_N package**

## APPLICATIONS

**High performance audio**  
**Active filters**  
**Fast amplifiers**  
**Integrators**

## GENERAL DESCRIPTION

The OP285 is a precision high-speed amplifier featuring the Butler Amplifier front-end. This new front-end design combines the accuracy and low noise performance of bipolar transistors with the speed of JFETs. This yields an amplifier with high slew rates, low offset and good noise performance at low supply currents. Bias currents are also low compared to bipolar designs.

The OP285 offers the slew rate and low power of a JFET amplifier combined with the precision, low noise and low drift of a bipolar amplifier. Input offset voltage is laser-trimmed and guaranteed less than 250  $\mu$ V. This makes the OP285 useful in dc-coupled or summing applications without the need for special selections or the added noise of additional offset adjustment circuitry. Slew rates of 22 V/ $\mu$ s and a bandwidth of 9 MHz make the OP285 one of the most accurate medium speed amplifiers available.

## PIN CONNECTION



The combination of low noise, speed and accuracy can be used to build high speed instrumentation systems. Circuits such as instrumentation amplifiers, ramp generators, bi-quad filters and dc-coupled audio systems are all practical with the OP285. For applications that require long term stability, the OP285 has a guaranteed maximum long term drift specification.

The OP285 is specified over the XIND—extended industrial—(−40°C to +85°C) temperature range. The OP285 is available in an 8-lead SOIC\_N surface mount package.

# OP285—SPECIFICATIONS (@ $V_S = \pm 15.0\text{ V}$ , $T_A = 25^\circ\text{C}$ , unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$			35	250	$\mu\text{V}$
	$V_{OS}$	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			600	$\mu\text{V}$
Input Bias Current	$I_B$	$V_{CM} = 0\text{ V}$		100	350	nA
	$I_B$	$V_{CM} = 0\text{ V}, -40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			400	nA
Input Offset Current	$I_{OS}$	$V_{CM} = 0\text{ V}$		2	$\pm 50$	nA
	$I_{OS}$	$V_{CM} = 0\text{ V}, -40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		2	$\pm 100$	nA
Input Voltage Range	$V_{CM}$		-10.5		10.5	V
Common-Mode Rejection	CMRR	$V_{CM} = \pm 10.5\text{ V},$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	80	106		dB
Large-Signal Voltage Gain	$A_{VO}$	$R_L = 2\text{ k}\Omega$	250			V/mV
	$A_{VO}$	$R_L = 2\text{ k}\Omega, -40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	175			V/mV
	$A_{VO}$	$R_L = 600\ \Omega$		200		V/mV
Common-Mode Input Capacitance				7.5		pF
Differential Input Capacitance				3.7		pF
Long-Term Offset Voltage	$\Delta V_{OS}$	Note 1			300	$\mu\text{V}$
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			1		$\mu\text{V}/^\circ\text{C}$
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage Swing	$V_O$	$R_L = 2\text{ k}\Omega$	-13.5	+13.9	+13.5	V
	$V_O$	$R_L = 2\text{ k}\Omega, -40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	-13	+13.9	+13	V
		$R_L = 600\ \Omega, V_S = \pm 18\text{ V}$		-16/+14		V
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5\text{ V to } \pm 18\text{ V}$	85	111		dB
	PSRR	$V_S = \pm 4.5\text{ V to } \pm 18\text{ V},$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	80			dB
Supply Current	$I_{SY}$	$V_S = \pm 4.5\text{ V to } \pm 18\text{ V}, V_O = 0\text{ V},$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		4	5	mA
	$I_{SY}$	$V_S = \pm 22\text{ V}, V_O = 0\text{ V},$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			5.5	mA
Supply Voltage Range	$V_S$		$\pm 4.5$		$\pm 22$	V
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$	15	22		V/ $\mu\text{s}$
Gain Bandwidth Product	GBP			9		MHz
Phase Margin	$\theta_o$			62		Degrees
Settling Time	$t_s$	To 0.1%, 10 V Step		625		ns
	$t_s$	To 0.01%, 10 V Step		750		ns
Distortion		$A_V = 1, V_{OUT} = 8.5\text{ V p-p},$ $f = 1\text{ kHz}, R_L = 2\text{ k}\Omega$		-104		dB
Voltage Noise Density	$e_n$	$f = 30\text{ Hz}$		7		nV/ $\sqrt{\text{Hz}}$
	$e_n$	$f = 1\text{ kHz}$		6		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		0.9		pA/ $\sqrt{\text{Hz}}$
Headroom		THD + Noise $\leq 0.01\%$ , $R_L = 2\text{ k}\Omega, V_S = \pm 18\text{ V}$		>12.9		dBu

## NOTE

<sup>1</sup>Long-term offset voltage is guaranteed by a 1,000 hour life test performed on three independent wafer lots at 125°C, with an LTPD of 1.3.

Specifications subject to change without notice.

**ABSOLUTE MAXIMUM RATINGS<sup>1</sup>**

Supply Voltage	±22 V
Input Voltage <sup>2</sup>	±18 V
Differential Input Voltage <sup>2</sup>	±7.5 V
Output Short-Circuit Duration to Gnd <sup>3</sup>	Indefinite
Storage Temperature Range	
SOIC_N Package	-65°C to +150°C
Operating Temperature Range	
OP285G	-40°C to +85°C
Junction Temperature Range	
SOIC_N Package	-65°C to +150°C
Lead Temperature Range (Soldering 60 Sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Package Type	$\theta_{JA}$ <sup>4</sup>	$\theta_{JC}$	Unit
8-Lead SOIC_N	158	43	°C/W

**NOTES**

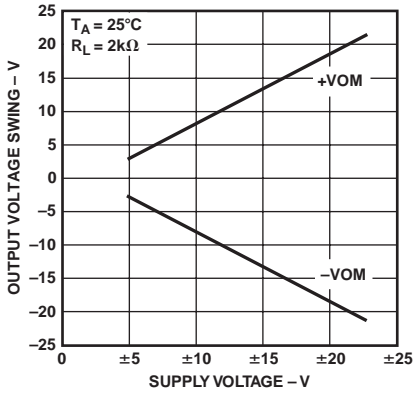
- <sup>1</sup>Absolute Maximum Ratings apply to packaged parts, unless otherwise noted.
- <sup>2</sup>For supply voltages less than ±7.5 V, the absolute maximum input voltage is equal to the supply voltage.
- <sup>3</sup>Shorts to either supply may destroy the device. See data sheet for full details.
- <sup>4</sup> $\theta_{JA}$  is specified for the worst case conditions, i.e.,  $\theta_{JA}$  is specified for device soldered in circuit board for SOIC package.

**ESD CAUTION**

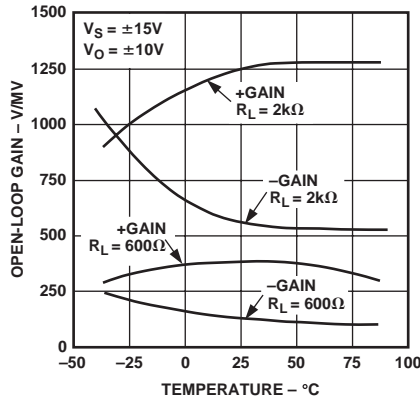


**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

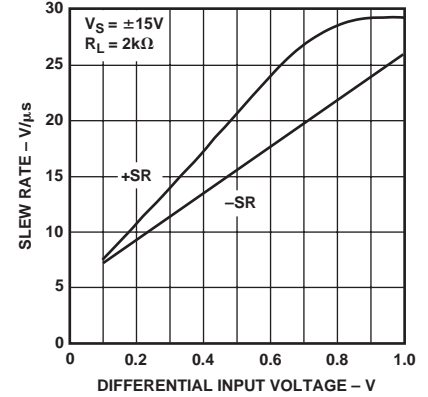
# OP285



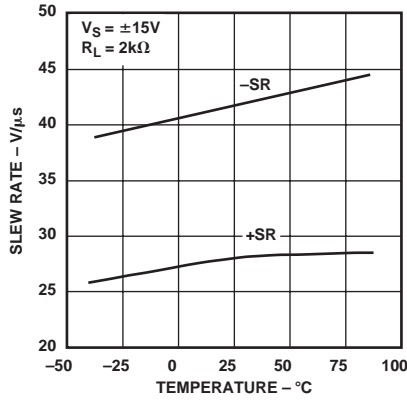
TPC 1. Output Voltage Swing vs. Supply Voltage



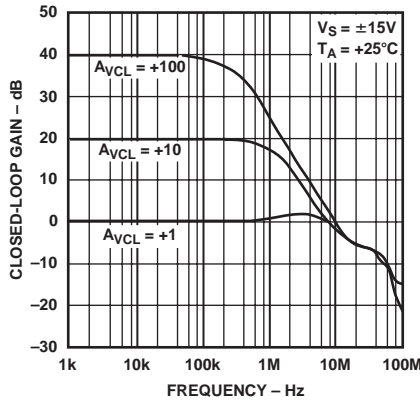
TPC 2. Open-Loop Gain vs. Temperature



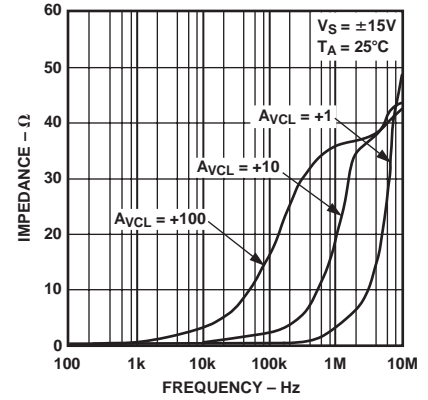
TPC 3. Slew Rate vs. Differential Input Voltage



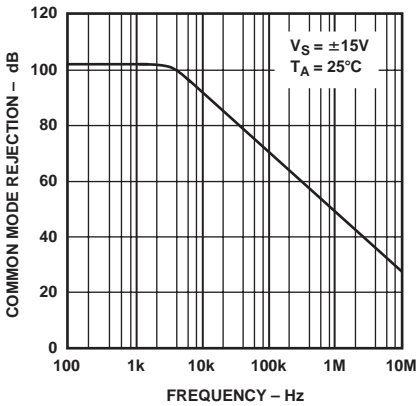
TPC 4. Slew Rate vs. Temperature



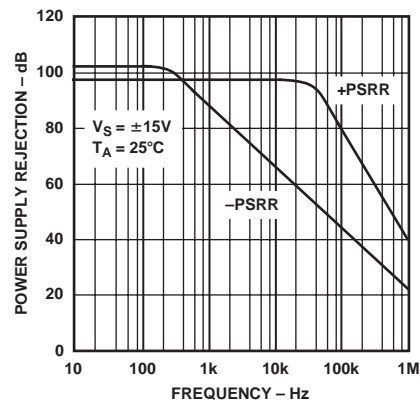
TPC 5. Closed-Loop Gain vs. Frequency



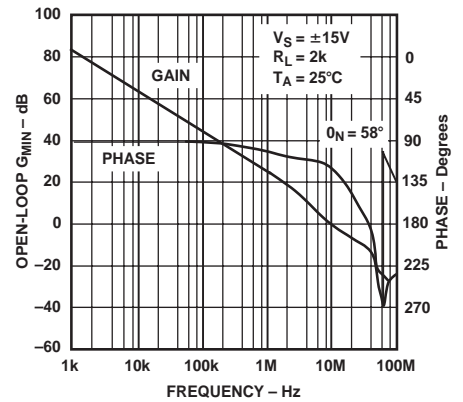
TPC 6. Closed-Loop Output Impedance vs. Frequency



TPC 7. Common-Mode Rejection vs. Frequency

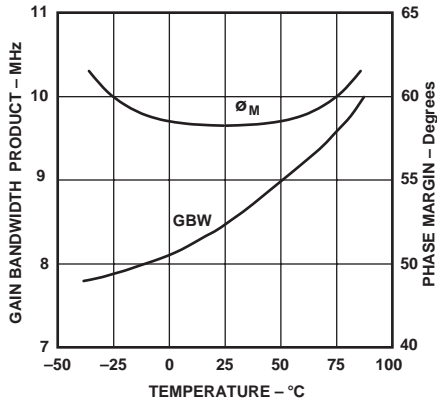


TPC 8. Power Supply Rejection vs. Frequency

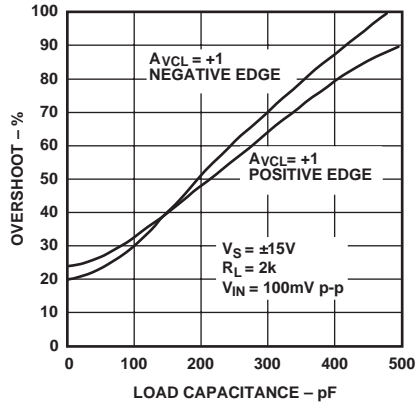


TPC 9. Open-Loop Gain, Phase vs. Frequency

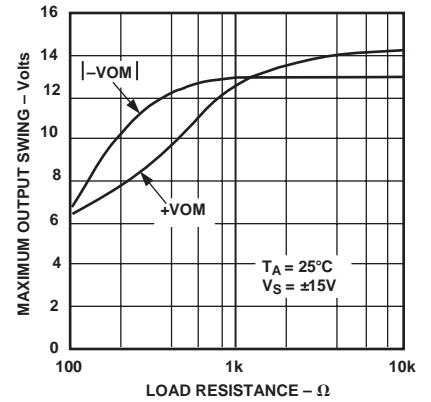
# Typical Performance Characteristics—OP285



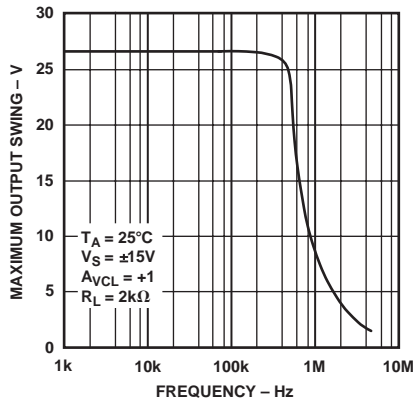
TPC 10. Gain Bandwidth Product, Phase Margin vs. Temperature



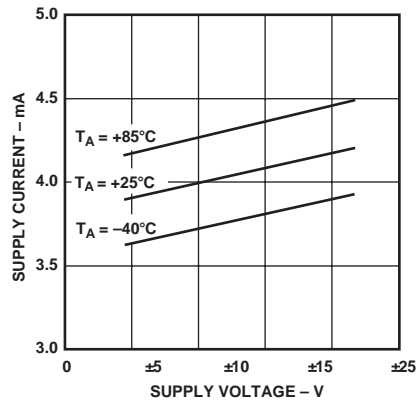
TPC 11. Small-Signal Overshoot vs./ Load Capacitance



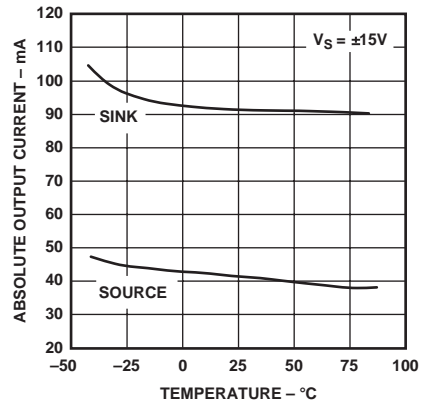
TPC 12. Maximum Output Voltage vs. Load Resistance



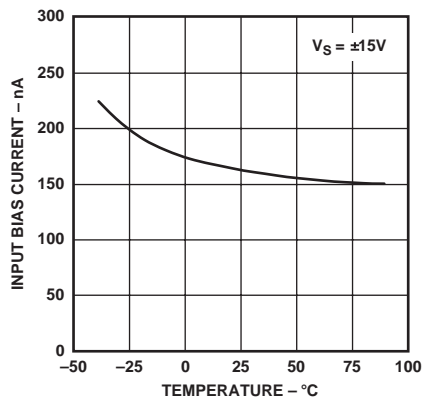
TPC 13. Maximum Output Swing vs. Frequency



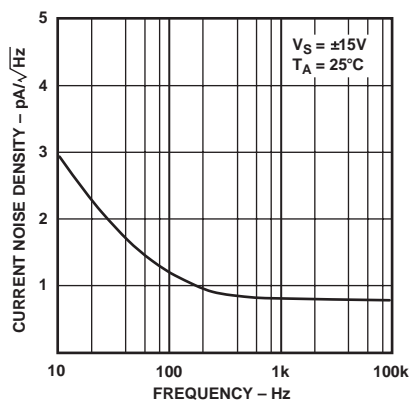
TPC 14. Supply Current vs. Supply Voltage



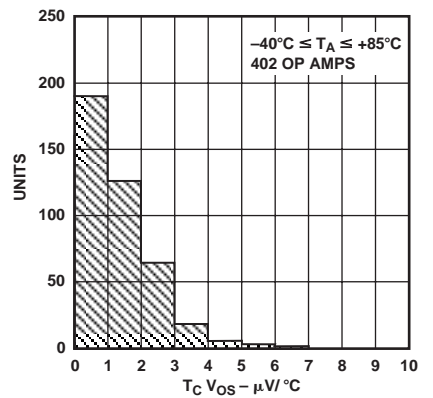
TPC 15. Short Circuit Current vs. Temperature



TPC 16. Input Bias Current vs. Temperature

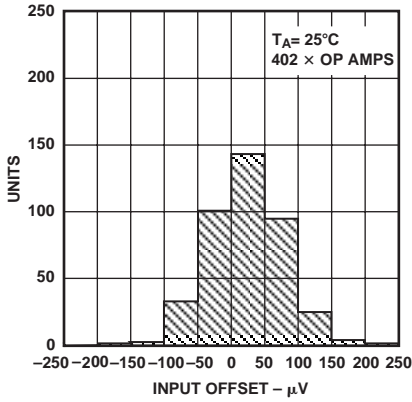


TPC 17. Current Noise Density vs. Frequency

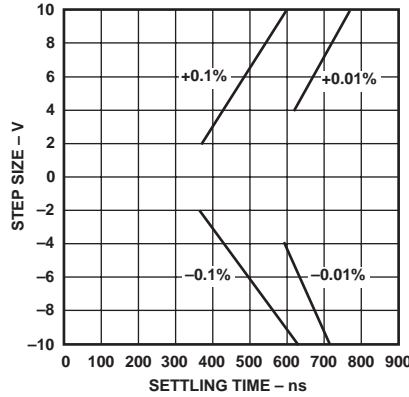


TPC 18.  $t_C V_{OS}$  Distribution

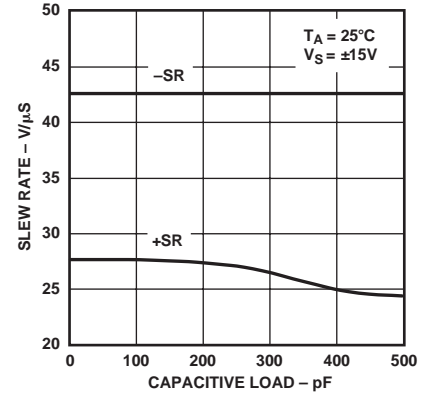
# OP285



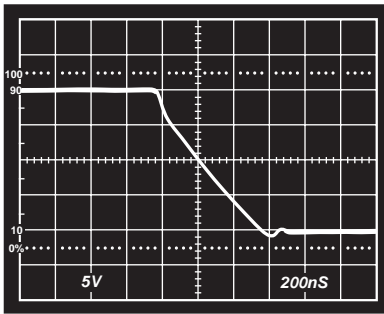
TPC 19. Input Offset ( $V_{OS}$ ) Distribution



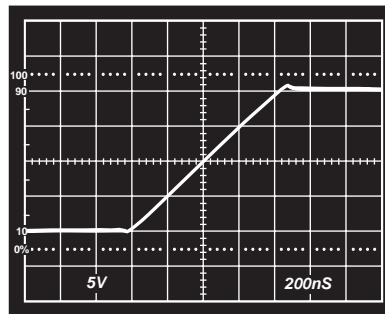
TPC 20. Settling Time vs. Step Size



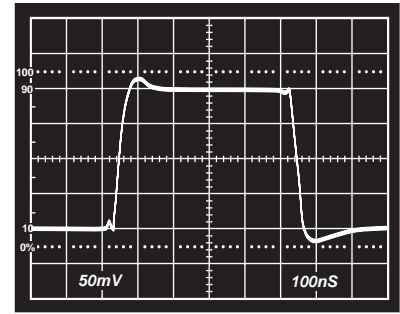
TPC 21. Slew Rate vs. Capacitive Load



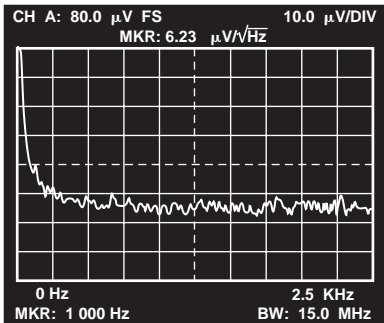
TPC 22. Negative Slew Rate  
 $R_L = 2 \text{ k}\Omega$ ,  $V_S = \pm 15 \text{ V}$ ,  $A_V = +1$



TPC 23. Positive Slew Rate  
 $R_L = 2 \text{ k}\Omega$ ,  $V_S = \pm 15 \text{ V}$ ,  $A_V = +1$



TPC 24. Small Signal Response  
 $R_L = 2 \text{ k}\Omega$ ,  $V_S = \pm 15 \text{ V}$ ,  $A_V = +1$



TPC 25. OP285 Voltage Noise Density vs. Frequency  $V_S = \pm 15 \text{ V}$ ,  $A_V = 1000$

## APPLICATIONS

### Short-Circuit Protection

The OP285 has been designed with inherent short-circuit protection to ground. An internal 30  $\Omega$  resistor, in series with the output, limits the output current at room temperature to  $I_{SC+} = 40$  mA and  $I_{SC-} = -90$  mA, typically, with  $\pm 15$  V supplies.

However, shorts to either supply may destroy the device when excessive voltages or current are applied. If it is possible for a user to short an output to a supply, for safe operation, the output current of the OP285 should be design-limited to  $\pm 30$  mA, as shown in Figure 1.

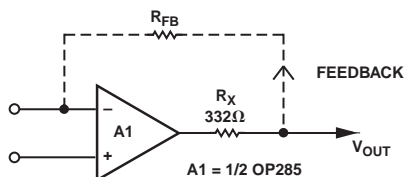


Figure 1. Recommended Output Short-Circuit Protection

### Input Over Current Protection

The maximum input differential voltage that can be applied to the OP285 is determined by a pair of internal Zener diodes connected across the inputs. They limit the maximum differential input voltage to  $\pm 7.5$  V. This is to prevent emitter-base junction breakdown from occurring in the input stage of the OP285 when very large differential voltages are applied. However, in order to preserve the OP285's low input noise voltage, internal resistance in series with the inputs were not used to limit the current in the clamp diodes. In small-signal applications, this is not an issue; however, in industrial applications, where large differential voltages can be inadvertently applied to the device, large transient currents can be made to flow through these diodes. The diodes have been designed to carry a current of  $\pm 8$  mA; and, in applications where the OP285's differential voltage were to exceed  $\pm 7.5$  V, the resistor values shown in Figure 2 safely limit the diode current to  $\pm 8$  mA.

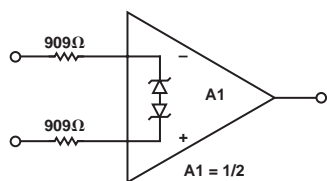


Figure 2. OP285 Input Over Current Protection

### Output Voltage Phase Reversal

Since the OP285's input stage combines bipolar transistors for low noise and p-channel JFETs for high speed performance, the output voltage of the OP285 may exhibit phase reversal if either of its inputs exceed its negative common-mode input voltage. This might occur in very severe industrial applications where a sensor or system fault might apply very large voltages on the inputs of the OP285. Even though the input voltage range of the OP285 is  $\pm 10.5$  V, an input voltage of approximately  $-13.5$  V will cause output voltage phase reversal. In inverting amplifier configurations, the OP285's internal 7.5 V input clamping diodes will prevent phase reversal; however, they will not prevent this effect from occurring in noninverting applications. For these

applications, the fix is a simple one and is illustrated in Figure 3. A 3.92 k $\Omega$  resistor in series with the noninverting input of the OP285 cures the problem.

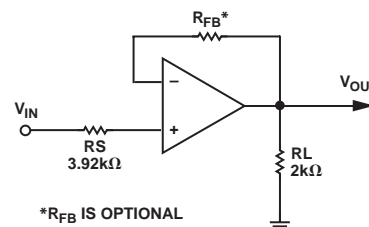


Figure 3. Output Voltage Phase Reversal Fix

### Overload or Overdrive Recovery

Overload or overdrive recovery time of an operational amplifier is the time required for the output voltage to recover to a rated output voltage from a saturated condition. This recovery time is important in applications where the amplifier must recover quickly after a large abnormal transient event. The circuit shown in Figure 4 was used to evaluate the OP285's overload recovery time. The OP285 takes approximately 1.2  $\mu$ s to recover to  $V_{OUT} = +10$  V and approximately 1.5  $\mu$ s to recover to  $V_{OUT} = -10$  V.

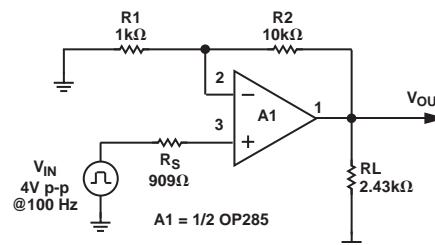


Figure 4. Overload Recovery Time Test Circuit

### Driving the Analog Input of an A/D Converter

Settling characteristics of operational amplifiers also include the amplifier's ability to recover, i.e., settle, from a transient output current load condition. When driving the input of an A/D converter, especially successive-approximation converters, the amplifier must maintain a constant output voltage under dynamically changing load current conditions. In these types of converters, the comparison point is usually diode clamped, but it may deviate several hundred millivolts resulting in high frequency modulation of the A/D input current. Amplifiers that exhibit high closed-loop output impedances and/or low unity-gain crossover frequencies recover very slowly from output load current transients. This slow recovery leads to linearity errors or missing codes because of errors in the instantaneous input voltage. Therefore, the amplifier chosen for this type of application should exhibit low output impedance and high unity-gain bandwidth so that its output has had a chance to settle to its nominal value before the converter makes its comparison.

The circuit in Figure 5 illustrates a settling measurement circuit for evaluating the recovery time of an amplifier from an output load current transient. The amplifier is configured as a follower with a very high speed current generator connected to its output. In this test, a 1 mA transient current was used. As shown in Figure 6, the OP285 exhibits an extremely fast recovery time of 139 ns to 0.01%. Because of its high gain-bandwidth product, high open-loop gain, and low output impedance, the OP285 is ideally suited to drive high speed A/D converters.

# OP285

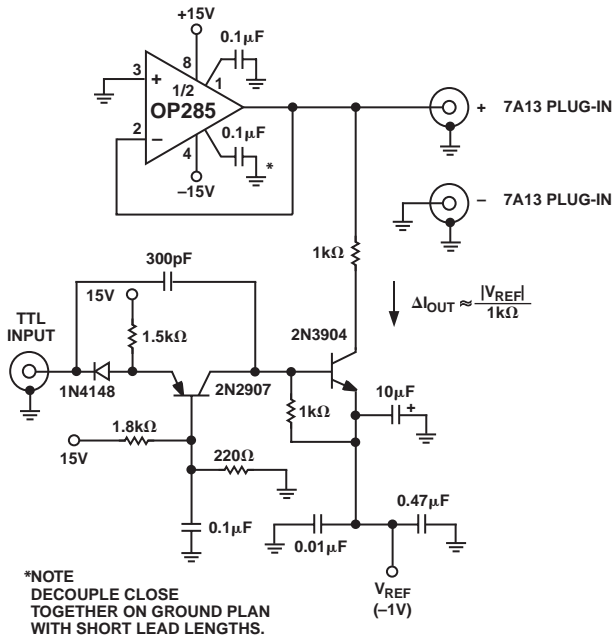


Figure 5. Transient Output Load Current Test Fixture

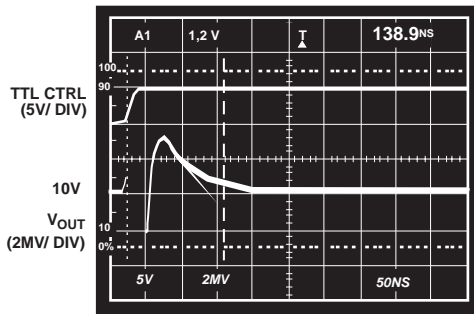


Figure 6. OP285's Output Load Current Recovery Time

## Measuring Settling Time

The design of OP285 combines high slew rate and wide gain-bandwidth product to produce a fast-settling ( $t_s < 1 \mu s$ ) amplifier for 8- and 12-bit applications. The test circuit designed to measure the settling time of the OP285 is shown in Figure 7. This test method has advantages over false-sum node techniques in that the actual output of the amplifier is measured, instead of an error voltage at the sum node. Common-mode settling effects are exercised in this circuit in addition to the slew rate and bandwidth effects measured by the false-sum-node method. Of course, a reasonably flat-top pulse is required as the stimulus.

The output waveform of the OP285 under test is clamped by Schottky diodes and buffered by the JFET source follower. The signal is amplified by a factor of ten by the OP260 and then Schottky-clamped at the output to prevent overloading the oscilloscope's input amplifier. The OP41 is configured as a fast integrator which provides overall dc offset nulling.

## High Speed Operation

As with most high speed amplifiers, care should be taken with supply decoupling, lead dress, and component placement. Recommended circuit configurations for inverting and noninverting applications are shown in Figures 8 and Figure 9.

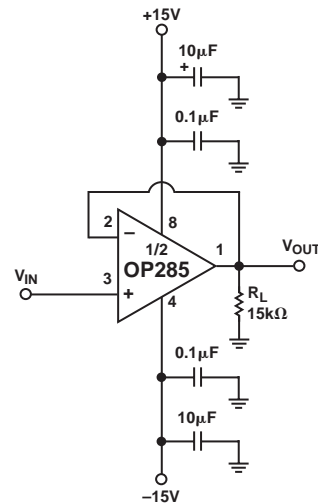


Figure 8. Unity Gain Follower

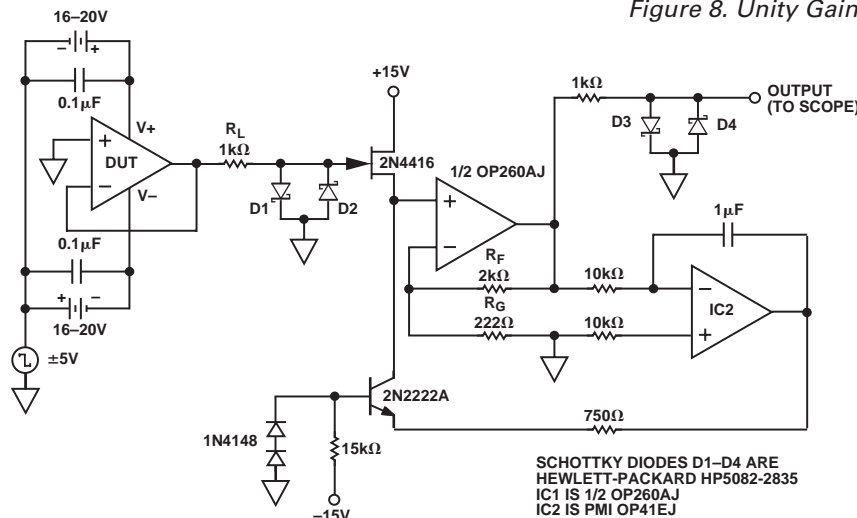


Figure 7. OP285's Settling Time Test Fixture

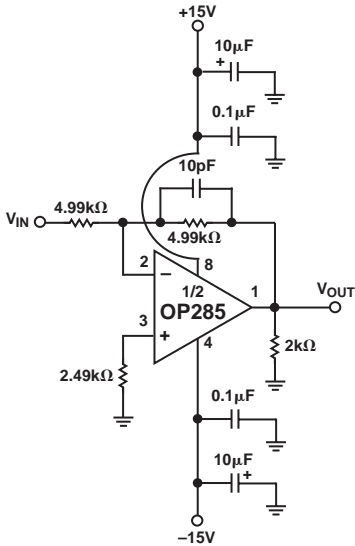


Figure 9. Unity-Gain Inverter

In inverting and noninverting applications, the feedback resistance forms a pole with the source resistance and capacitance ( $R_S$  and  $C_S$ ) and the OP285's input capacitance ( $C_{IN}$ ), as shown in Figure 10. With  $R_S$  and  $R_F$  in the kilohm range, this pole can create excess phase shift and even oscillation. A small capacitor,  $C_{FB}$ , in parallel with  $R_{FB}$  eliminates this problem. By setting  $R_S (C_S + C_{IN}) = R_{FB} C_{FB}$ , the effect of the feedback pole is completely removed.

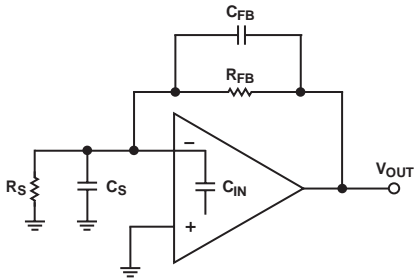


Figure 10. Compensating the Feedback Pole

**High-Speed, Low-Noise Differential Line Driver**

The circuit of Figure 11 is a unique line driver widely used in industrial applications. With  $\pm 18$  V supplies, the line driver can deliver a differential signal of 30 V p-p into a 2.5 k $\Omega$  load. The high slew rate and wide bandwidth of the OP285 combine to yield a full power bandwidth of 130 kHz while the low noise front end produces a referred-to-input noise voltage spectral density of 10 nV/ $\sqrt{\text{Hz}}$ . The design is a transformerless, balanced transmission system where output common-mode rejection of noise is of paramount importance. Like the transformer-based design, either output can be shorted to ground for unbalanced line driver applications without changing the circuit gain of 1. Other circuit gains can be set according to the equation in the diagram. This allows the design to be easily set to noninverting, inverting, or differential operation.

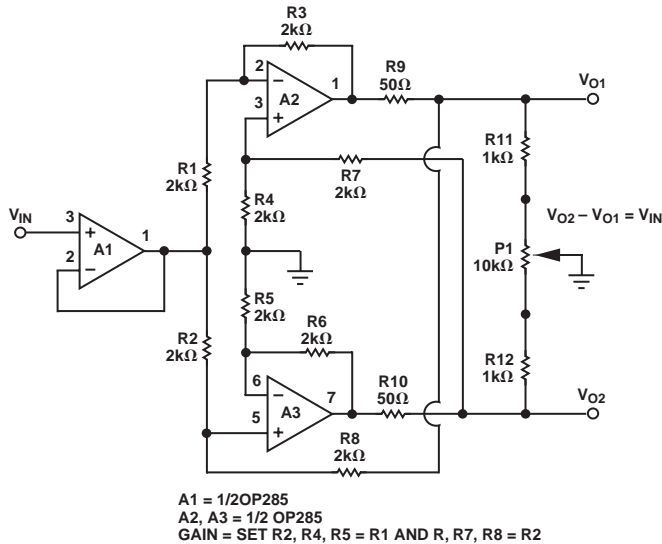


Figure 11. High-Speed, Low-Noise Differential Line Driver

**Low Phase Error Amplifier**

The simple amplifier configuration of Figure 12 uses the OP285 and resistors to reduce phase error substantially over a wide frequency range when compared to conventional amplifier designs. This technique relies on the matched frequency characteristics of the two amplifiers in the OP285. Each amplifier in the circuit has the same feedback network which produces a circuit gain of 10. Since the two amplifiers are set to the same gain and are matched due to the monolithic construction of the OP285, they will exhibit identical frequency response. Recall from feedback theory that a pole of a feedback network becomes a zero in the loop gain response. By using this technique, the dominant pole of the amplifier in the feedback loop compensates for the dominant pole of the main amplifier,

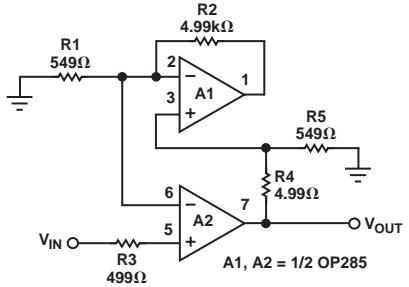


Figure 12. Cancellation of A2's Dominant Pole by A1

# OP285

thereby reducing phase error dramatically. This is shown in Figure 13 where the 10x composite amplifier's phase response exhibits less than 1.5° phase shift through 500 kHz. On the other hand, the single gain stage amplifier exhibits 25° of phase shift over the same frequency range. An additional benefit of the low phase error configuration is constant group delay, by virtue of constant phase shift at all frequencies below 500 kHz. Although this technique is valid for minimum circuit gains of 10, actual closed-loop magnitude response must be optimized for the amplifier chosen.

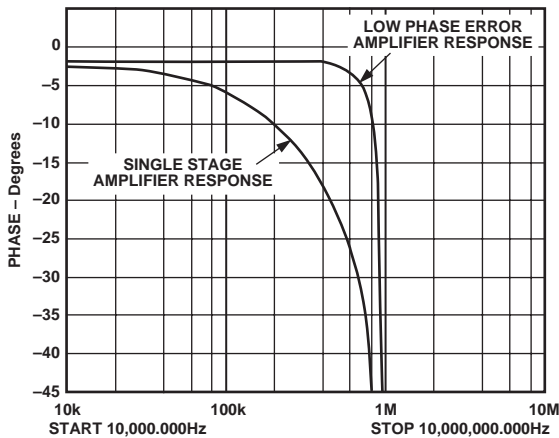


Figure 13. Phase Error Comparison

For a more detailed treatment on the design of low phase error amplifiers, see Application Note AN-107.

## Fast Current Pump

A fast, 30 mA current source, illustrated in Figure 14, takes advantage of the OP285's speed and high output current drive. This is a variation of the Howland current source where a second amplifier, A2, is used to increase load current accuracy and output voltage compliance. With supply voltages of ±15 V, the output voltage compliance of the current pump is ±8 V. To keep the output resistance in the MΩ range requires that 0.1% or better resistors be used in the circuit. The gain of the current pump can be easily changed according to the equations shown in the diagram.

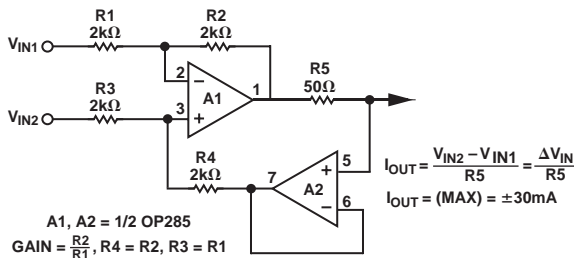


Figure 14. A Fast Current Pump

## A Low Noise, High Speed Instrumentation Amplifier

A high speed, low noise instrumentation amplifier, constructed with a single OP285, is illustrated in Figure 15. The circuit exhibits less than 1.2 μV p-p noise (RTI) in the 0.1 Hz to 10 Hz band and an input noise voltage spectral density of 9 nV/√Hz (1 kHz) at a gain of 1000. The gain of the amplifier is easily set by  $R_G$  according to the formula:

$$\frac{V_{OUT}}{V_{IN}} = \frac{9.98 \text{ k}\Omega}{R_G} + 2$$

The advantages of a two op amp instrumentation amplifier based on a dual op amp is that the errors in the individual amplifiers tend to cancel one another. For example, the circuit's input offset voltage is determined by the input offset voltage matching of the OP285, which is typically less than 250 μV.

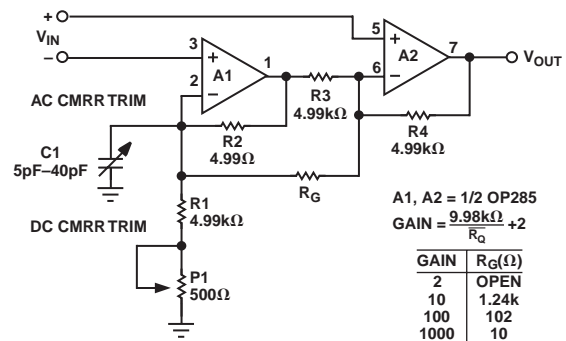


Figure 15. A High-Speed Instrumentation Amplifier

Common-mode rejection of the circuit is limited by the matching of resistors R1 to R4. For good common-mode rejection, these resistors ought to be matched to better than 1%. The circuit was constructed with 1% resistors and included potentiometer P1 for trimming the CMRR and a capacitor C1 for trimming the CMRR. With these two trims, the circuit's common-mode rejection was better than 95 dB at 60 Hz and better than 65 dB at 10 kHz. For the best common-mode rejection performance, use a matched (better than 0.1%) thin-film resistor network for R1 through R4 and use the variable capacitor to optimize the circuit's CMR.

The instrumentation amplifier exhibits very wide small- and large-signal bandwidths regardless of the gain setting, as shown in the table. Because of its low noise, wide gain-bandwidth product, and high slew rate, the OP285 is ideally suited for high speed signal conditioning applications.

Circuit Gain	$R_G$ (Ω)	Circuit Bandwidth	
		$V_{OUT} = 100 \text{ mV p-p}$	$V_{OUT} = 20 \text{ V p-p}$
2	Open	5 MHz	780 kHz
10	1.24 k	1 MHz	460 kHz
100	102	90 kHz	85 kHz
1000	10	10 kHz	10 kHz

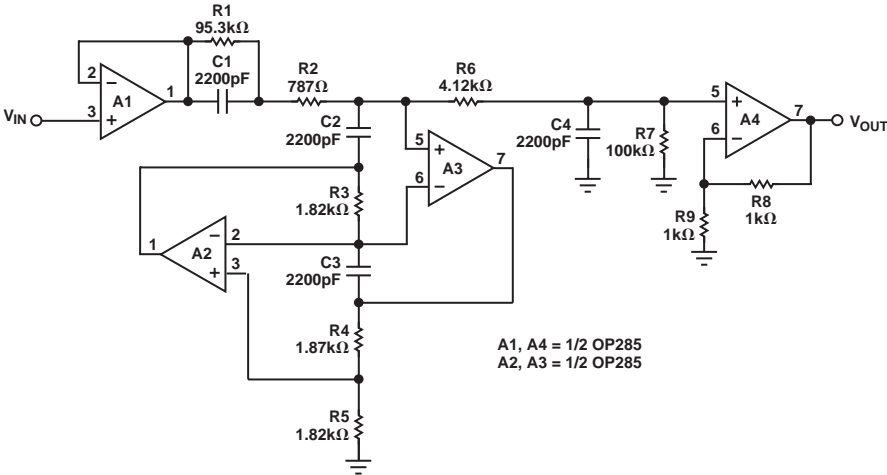


Figure 16. A 3-Pole, 40 kHz Low-Pass Filter

**A 3-Pole, 40 kHz Low-Pass Filter**

The closely matched and uniform ac characteristics of the OP285 make it ideal for use in GIC (Generalized Impedance Converter) and FDNR (Frequency Dependent Negative Resistor) filter applications. The circuit in Figure 16 illustrates a linear-phase, 3-pole, 40 kHz low-pass filter using an OP285 as an inductance simulator (gyrator). The circuit uses one OP285 (A2 and A3) for the FDNR and one OP285 (A1 and A4) as an input buffer and bias current source for A3. Amplifier A4 is configured in a gain of 2 to set the pass band magnitude response to 0 dB. The benefits of this filter topology over classical approaches are that the op amp used in the FDNR is not in the signal path and that the filter’s performance is relatively insensitive to component variations. Also, the configuration is such that large signal levels can be handled without overloading any of the filter’s internal nodes. As shown in Figure 17, the OP285’s symmetric slew rate and low distortion produce a clean, well-behaved transient response.

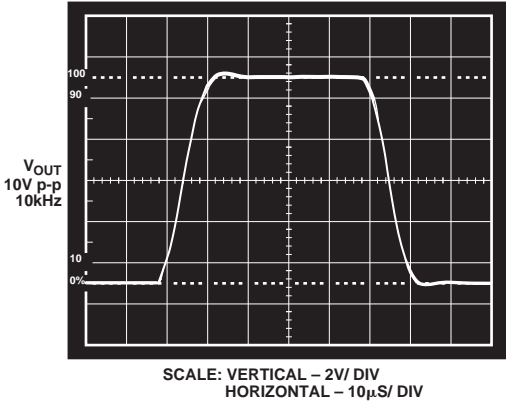


Figure 17. Low-Pass Filter Transient Response

**Driving Capacitive Loads**

The OP285 was designed to drive both resistive loads to 600 Ω and capacitive loads of over 1000 pF and maintain stability. While there is a degradation in bandwidth when driving capacitive loads, the designer need not worry about device stability. The graph in Figure 18 shows the 0 dB bandwidth of the OP285 with capacitive loads from 10 pF to 1000 pF.

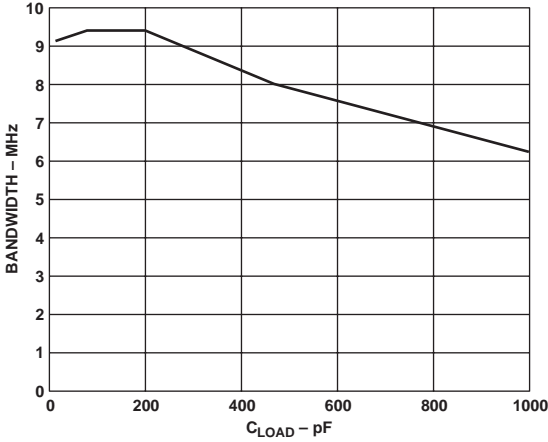
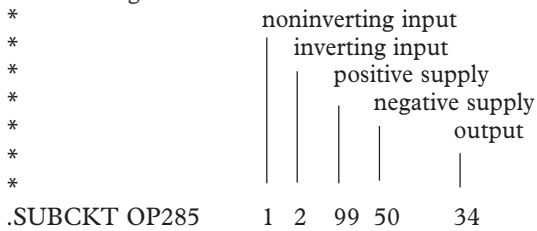


Figure 18. Bandwidth vs. C<sub>LOAD</sub>

# OP285

OP285 SPICE Model

\* Node assignments



\* INPUT STAGE & POLE AT 100 MHZ

R3 5 51 2.188  
R4 6 51 2.188  
CIN 1 2 1.5E-12  
C2 5 6 364E-12  
I1 97 4 100E-3  
IOS 1 2 1E-9  
EOS 9 3 POLY(1) 26 28 35E-6 1  
Q1 5 2 7 QX  
Q2 6 9 8 QX  
R5 7 4 1.672  
R6 8 4 1.672  
D1 2 36 DZ  
D2 1 36 DZ  
EN 3 1 100 1  
GN1 0 2 13 0 1  
GN20 1 16 0 1  
\*  
EREF 98 0 28 0 1  
EP 97 0 99 0 1  
EM 510 50 0 1

\* VOLTAGE NOISE SOURCE

DN1 35 10 DEN  
DN2 10 11 DEN  
VN1 35 0 DC 2  
VN2 0 11 DC 2

\* CURRENT NOISE SOURCE

DN3 12 13 DIN  
DN4 13 14 DIN  
VN3 12 0 DC 2  
VN4 0 14 DC 2  
CN1 13 0 7.53E-3

\* CURRENT NOISE SOURCE

DN5 15 16 DIN  
DN6 16 17 DIN  
VN5 15 0 DC 2  
VN6 0 17 DC 2  
CN2 16 0 7.53E-3

\* GAIN STAGE & DOMINANT POLE AT 32 HZ \*

R7 18 98 1.09E6  
C3 18 98 4.55E-9  
G1 98 18 5 6 4.57E-1  
V2 97 19 1.4  
V3 20 51 1.4  
D3 18 19 DX  
D4 20 18 DX

\* POLE/ZERO PAIR AT 1.5MHz/2.7MHz

R8 21 98 1E3  
R9 21 22 1.25E3  
C4 22 98 47.2E-12  
G2 98 21 18 28 1E-3

\* POLE AT 100 MHZ

R10 23 98 1  
C5 23 98 1.59E-9  
G3 98 23 21 28 1

\* POLE AT 100 MHZ

R11 24 98 1  
C6 24 98 1.59E-9  
G4 98 24 23 28 1

\* COMMON-MODE GAIN NETWORK WITH ZERO AT 1 kHz \*

R12 25 26 1E6  
C7 25 26 1.59E-12  
R13 26 98 1  
E2 25 98 POLY(2) 1 98 2 98 0 2.506 2.506

\* POLE AT 100 MHZ

R14 27 98 1  
C8 27 98 1.59E-9  
G5 98 27 24 28 1

\* OUTPUT STAGE

R15 28 99 100E3  
R16 28 50 100E3  
C9 28 50 1 E-6  
ISY 99 50 1.85E-3  
R17 29 99 100  
R18 29 50 100  
L2 29 34 1E-9  
G6 32 50 27 29 10E-3  
G7 33 50 29 27 10E-3  
G8 29 99 99 27 10E-3  
G9 50 29 27 50 10E-3  
V4 30 29 1.3  
V5 29 31 3.8  
F1 29 0 V4 1  
F2 0 29 V5 1  
D5 27 30 DX  
D6 31 27 DX  
D7 99 32 DX  
D8 99 33 DX  
D9 50 32 DY  
D10 50 33 DY

\* MODELS USED

.MODEL QX PNP(BF = 5E5)  
.MODEL DX D(IS = 1E-12)  
.MODEL DY D(IS = 1E-15 BV = 50)  
.MODEL DZ D(IS = 1E-15 BV = 7.0)  
.MODEL DEN D(IS = 1E-12 RS = 4.35K KF = 1.95E-15 AF = 1)  
.MODEL DIN D(IS = 1E-12 RS = 77.3E-6 KF = 3.38E-15 AF = 1) .ENDS OP-285

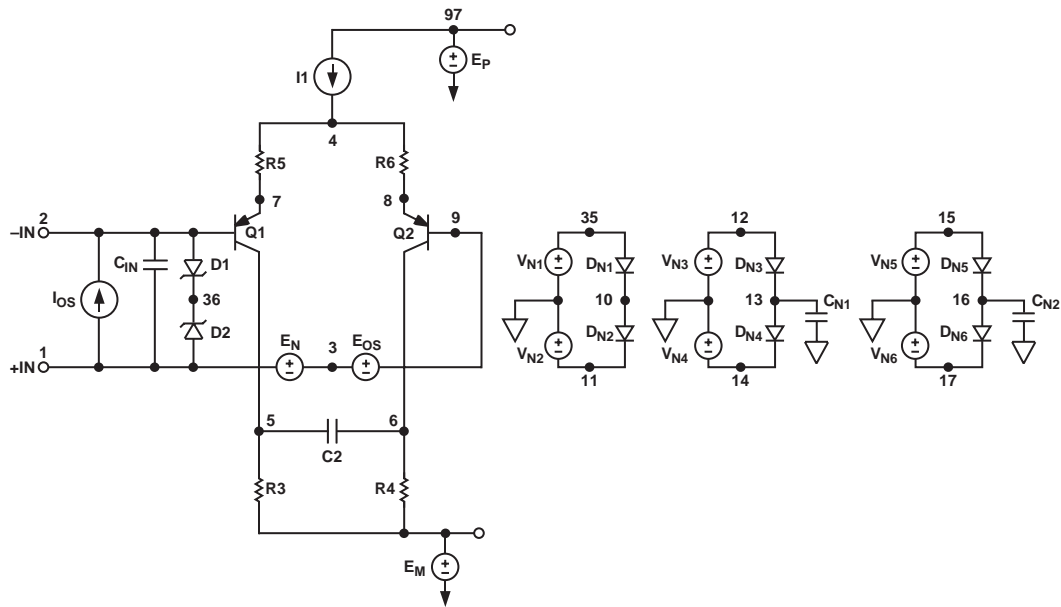


Figure 19a. Spice Diagram

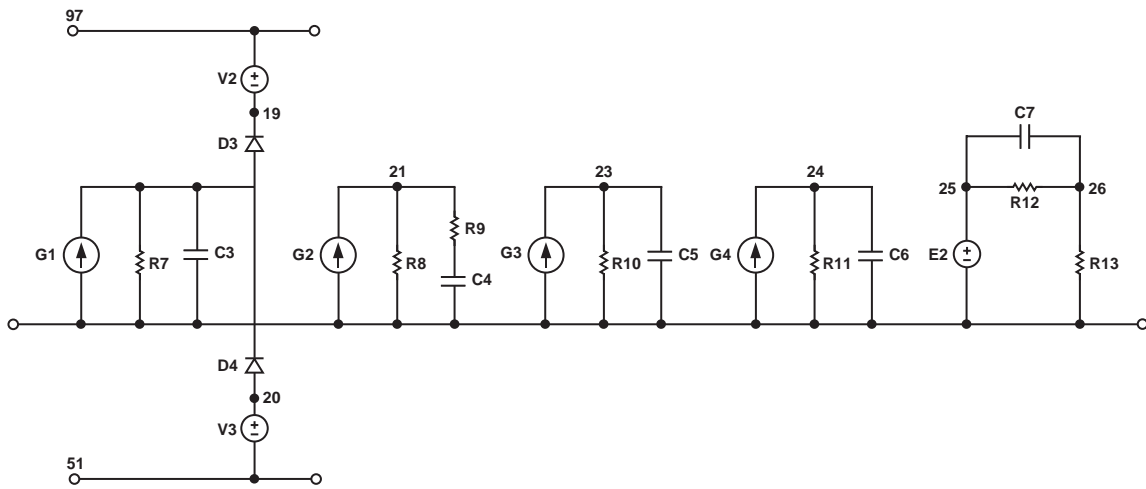


Figure 19b. Spice Diagram

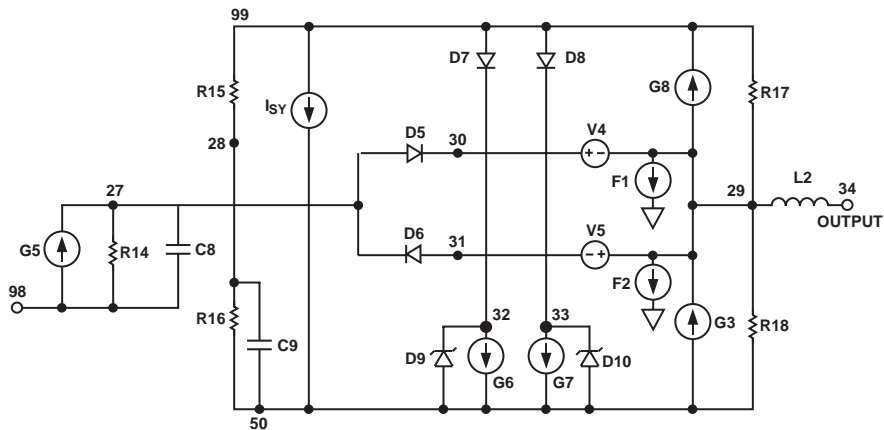
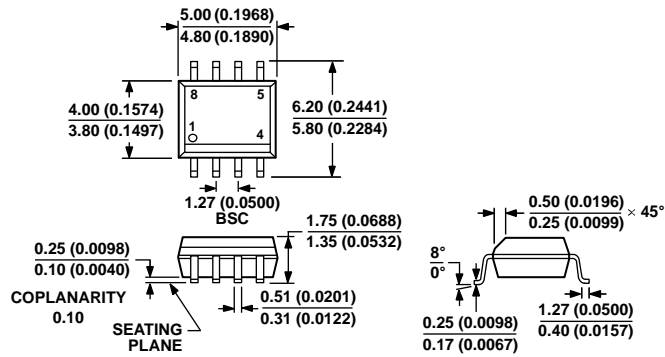


Figure 19c. Spice Diagram

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

8-Lead Standard Small Outline Package [SOIC\_N]  
 Narrow Body  
 (R-8)

Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
OP285GS	-40°C to +85°C	8-lead SOIC_N	R-8
OP285GS-REEL	-40°C to +85°C	8-lead SOIC_N	R-8
OP285GS-REEL7	-40°C to +85°C	8-lead SOIC_N	R-8
OP285GSZ	-40°C to +85°C	8-lead SOIC_N	R-8
OP285GSZ-REEL	-40°C to +85°C	8-lead SOIC_N	R-8
OP285GSZ-REEL7	-40°C to +85°C	8-lead SOIC_N	R-8

<sup>1</sup> Z = RoHS Compliant Part.

**REVISION HISTORY**

**1/2018—Rev. B to Rev. C**

Changes to Figure 1..... 1

**10/2017—Rev. A to Rev. B**

Changes to General Description Section and Pin Connection... 1  
Changes to Supply Current Parameter, Specifications Section ... 2  
Changes to Absolute Maximum Ratings Section..... 3  
Updated Outline Dimensions..... 14  
Moved Ordering Guide ..... 14  
Changes to Ordering Guide..... 14

**1/2002—Rev. 0 to Rev. A**

Edits to Ordering Guide ..... 3  
Deleted Wafer Test Limits ..... 3  
Deleted Dice Characteristics..... 3

**7/1992—Revision 0: Initial Version**

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