THE DATASHEET OF

OP281GRUZ-REEL

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Ultralow Power, Rail-to-Rail Output Operational Amplifiers

OP281/OP481

FEATURES

Low supply current: 4 µA/amplifier maximum
Single-supply operation: 2.7 V to 12 V
Wide input voltage range
Rail-to-rail output swing
Low offset voltage: 1.5 mV
No phase reversal

APPLICATIONS

Comparator
Battery-powered instrumentation
Safety monitoring
Remote sensors
Low voltage strain gage amplifiers

GENERAL DESCRIPTION

The OP281 and OP481 are dual and quad ultralow power single-supply amplifiers featuring rail-to-rail outputs. Each operates from supplies as low as 2.0 V and is specified at +3 V and +5 V single supplies as well as ±5 V dual supplies.

Fabricated on Analog Devices' CBCMOS process, the OP281/OP481 feature a precision bipolar input and an output that swings to within millivolts of the supplies, continuing to sink or source current up to a voltage equal to the supply voltage.

Applications for these amplifiers include safety monitoring, portable equipment, battery and power supply control, and signal conditioning and interfacing for transducers in very low power systems.

The output's ability to swing rail-to-rail and not increase supply current when the output is driven to a supply voltage enables the OP281/OP481 to be used as comparators in very low power systems. This is enhanced by their fast saturation recovery time. Propagation delays are 250 µs.

The OP281/OP481 are specified over the extended industrial temperature range (−40°C to +85°C). The OP281 dual amplifier is available in 8-lead SOIC surface-mount and TSSOP packages. The OP481 quad amplifier is available in narrow 14-lead SOIC and TSSOP packages.

PIN CONFIGURATIONS

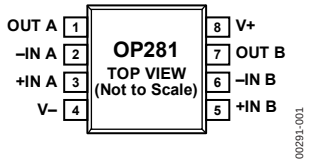

Figure 1. 8-Lead Narrow-Body SOIC (R Suffix)

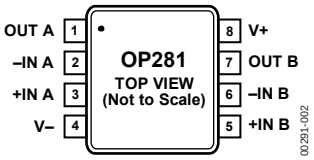

Figure 2. 8-Lead TSSOP (RU Suffix)

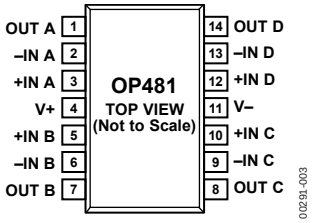

Figure 3. 14-Lead Narrow-Body SOIC (R Suffix)

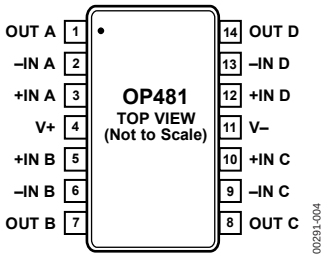

Figure 4. 14-Lead TSSOP (RU Suffix)

Rev. D
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10/07—Rev. B to Rev. C

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SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_S = 3.0 V, V_{CM} = 1.5 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage[1]	V_{OS}				1.5	mV
		−40°C ≤ T_A ≤ +85°C			2.5	mV
Input Bias Current	I_B	−40°C ≤ T_A ≤ +85°C		3	10	nA
Input Offset Current	I_{OS}	−40°C ≤ T_A ≤ +85°C		0.1	7	nA
Input Voltage Range			0		2	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 2.0 V, −40°C ≤ T_A ≤ +85°C	65	95		dB
Large-Signal Voltage Gain	A_{VO}	R_L = 1 MΩ, V_O = 0.3 V to 2.7 V	5	13		V/mV
		−40°C ≤ T_A ≤ +85°C	2			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C to +85°C		10		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			20		pA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$			2		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to GND, −40°C ≤ T_A ≤ +85°C	2.925	2.96		V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to V+, −40°C ≤ T_A ≤ +85°C		25	75	mV
Short-Circuit Limit	I_{SC}			±1.1		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 12 V, −40°C ≤ T_A ≤ +85°C	76	95		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		3	4	µA
		−40°C ≤ T_A ≤ +85°C			5	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 100 kΩ, C_L = 50 pF		25		V/ms
Turn-On Time		A_V = 1, V_O = 1 V		40		µs
		A_V = 20, V_O = 1 V		50		µs
Saturation Recovery Time				65		µs
Gain Bandwidth Product	GBP			95		kHz
Phase Margin	φ_M			70		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		10		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		75		nV/√Hz
Current Noise Density	i_n			<1		pA/√Hz

[1] V_{OS} is tested under a no load condition.

V_S = 5.0 V, V_{CM} = 2.5 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage[1]	V_{OS}			0.1	1.5	mV
		−40°C ≤ T_A ≤ +85°C			2.5	mV
Input Bias Current	I_B	−40°C ≤ T_A ≤ +85°C		3	10	nA
Input Offset Current	I_{OS}	−40°C ≤ T_A ≤ +85°C		0.1	7	nA
Input Voltage Range			0		4	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 4.0 V, −40°C ≤ T_A ≤ +85°C	65	90		dB
Large-Signal Voltage Gain	A_{VO}	R_L = 1 MΩ, V_O = 0.5 V to 4.5 V	5	15		V/mV
		−40°C ≤ T_A ≤ +85°C	2			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C to +85°C		10		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			20		pA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$			2		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to GND, −40°C ≤ T_A ≤ +85°C	4.925	4.96		V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to V+, −40°C ≤ T_A ≤ +85°C		25	75	mV
Short-Circuit Limit	I_{SC}			±3.5		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 12 V, −40°C ≤ T_A ≤ +85°C	76	95		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		3.2	4	µA
		−40°C ≤ T_A ≤ +85°C			5	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 100 kΩ, C_L = 50 pF		27		V/ms
Saturation Recovery Time				120		µs
Gain Bandwidth Product	GBP			100		kHz
Phase Margin	φ_M			74		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		10		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		75		nV/√Hz
Current Noise Density	i_n			<1		pA/√Hz

[1] V_{OS} is tested under a no load condition.

V_S = ±5.0 V, T_A = +25°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage[1]	V_{OS}			0.1	1.5	mV
		−40°C ≤ T_A ≤ +85°C			2.5	mV
Input Bias Current	I_B	−40°C ≤ T_A ≤ +85°C		3	10	nA
Input Offset Current	I_{OS}	−40°C ≤ T_A ≤ +85°C		0.1	7	nA
Input Voltage Range			−5		+4	V
Common-Mode Rejection	CMRR	V_{CM} = −5.0 V to +4.0 V, −40°C ≤ T_A ≤ +85°C	65	95		dB
Large-Signal Voltage Gain	A_{VO}	R_L = 1 MΩ, V_O = ±4.0 V,	5	13		V/mV
		−40°C ≤ T_A ≤ +85°C	2			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C to +85°C		10		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			20		pA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$			2		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 100 kΩ to GND, −40°C ≤ T_A ≤ +85°C	±4.925	±4.98		V
Short-Circuit Limit	I_{SC}			12		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±1.35 V to ±6 V, −40°C ≤ T_A ≤ +85°C	76	95		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		3.3	5	µA
		−40°C ≤ T_A ≤ +85°C			6	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 100 kΩ, C_L = 50 pF		28		V/ms
Gain Bandwidth Product	GBP			105		kHz
Phase Margin	φ_M			75		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		10		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		85		nV/√Hz
		f = 10 kHz		75		nV/√Hz
Current Noise Density	i_n			<1		pA/√Hz

[1] V_{OS} is tested under a no load condition.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	16 V
Input Voltage	GND to V_S + 10 V
Differential Input Voltage	±3.5 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 5. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}	Unit
8-Lead SOIC (R Suffix)	158	43	°C/W
8-Lead TSSOP (RU Suffix)	240	43	°C/W
14-Lead SOIC (R Suffix)	120	36	°C/W
14-Lead TSSOP (RU Suffix)	240	43	°C/W

[1] θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for device soldered in circuit board for TSSOP and SOIC packages.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

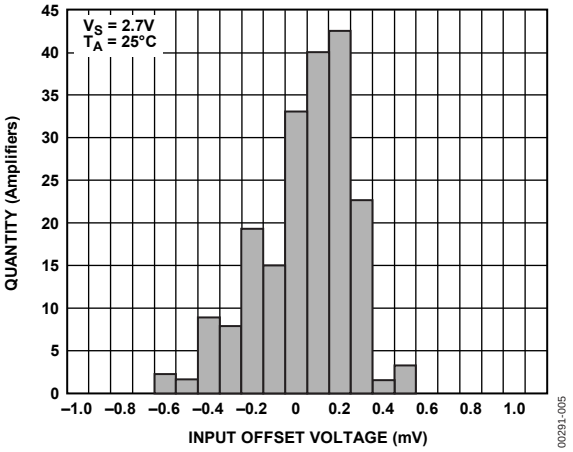


Figure 5. Input Offset Voltage Distribution

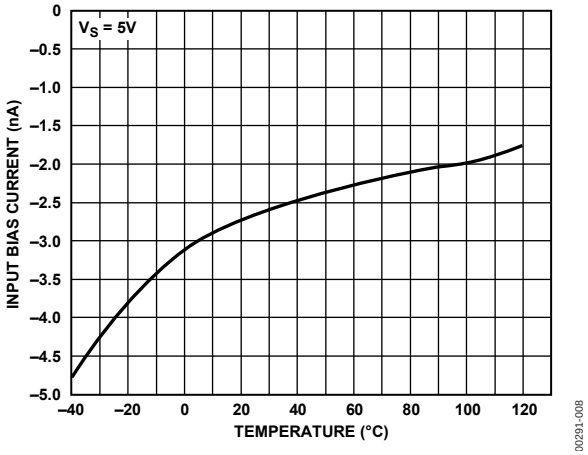


Figure 8. Input Bias Current vs. Temperature

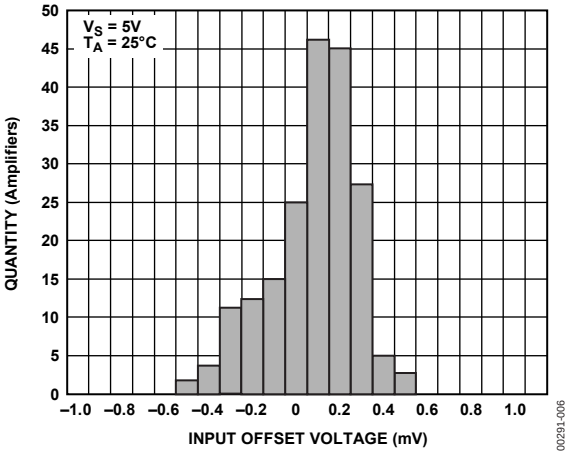


Figure 6. Input Offset Voltage Distribution

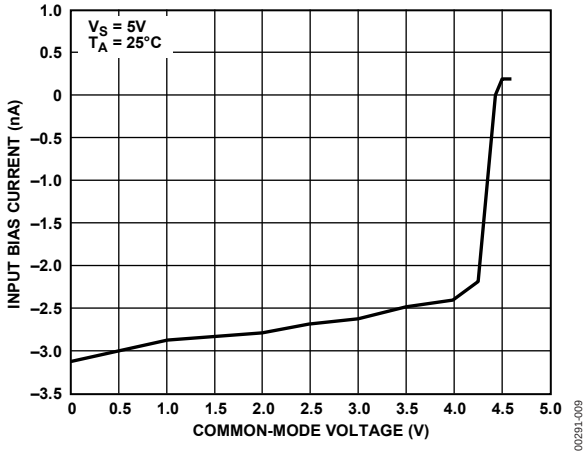


Figure 9. Input Bias Current vs. Common-Mode Voltage

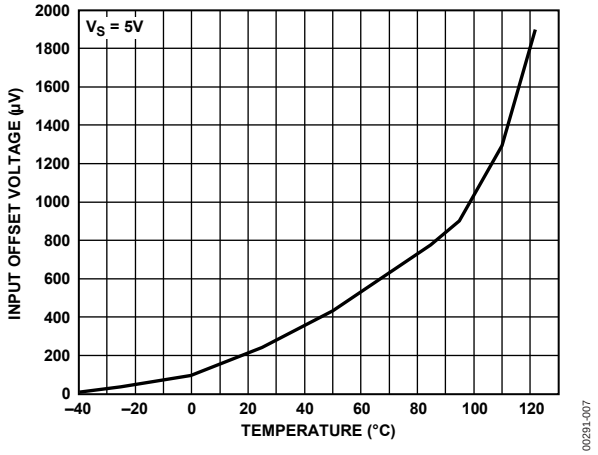


Figure 7. Input Offset Voltage vs. Temperature

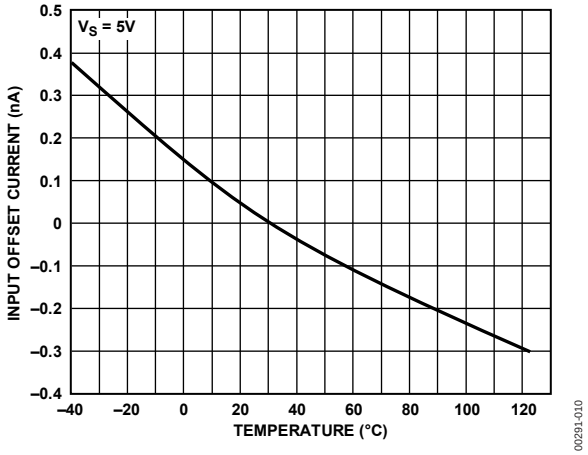


Figure 10. Input Offset Current vs. Temperature

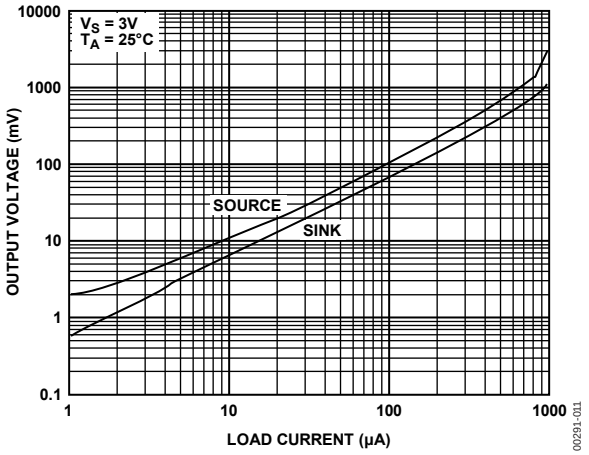


Figure 11. Output Voltage to Supply Rail vs. Load Current

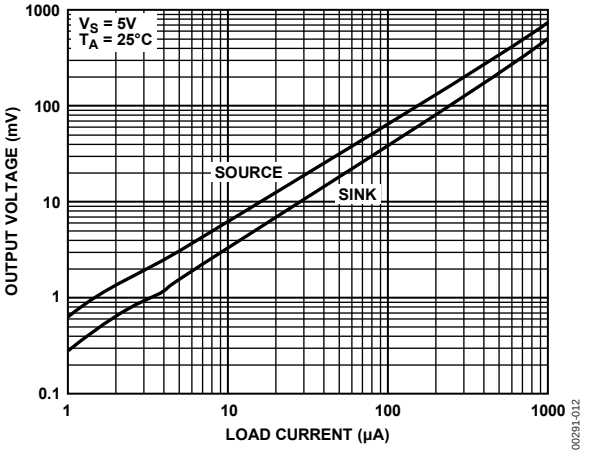


Figure 12. Output Voltage to Supply Rail vs. Load Current

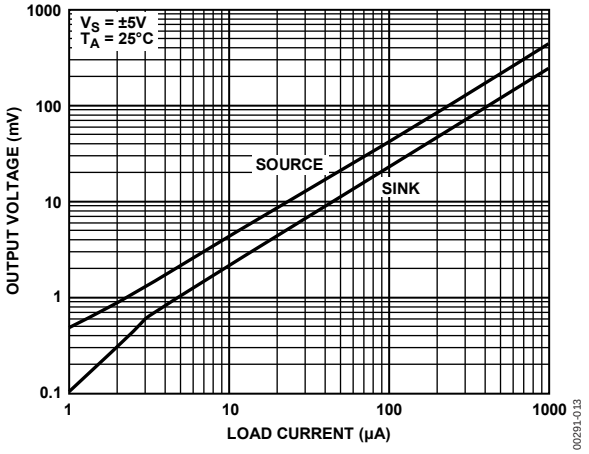


Figure 13. Output Voltage to Supply Rail vs. Load Current

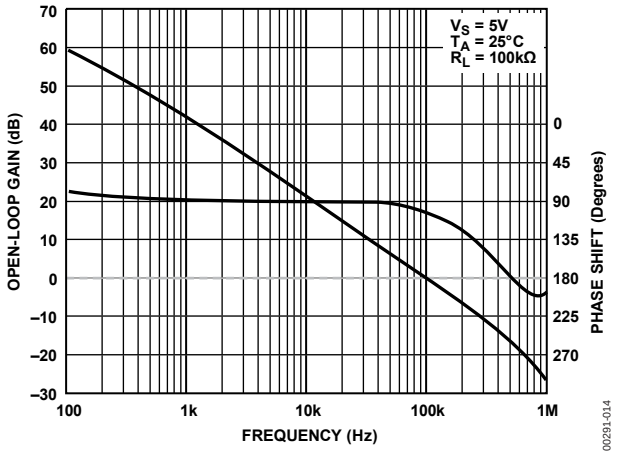


Figure 14. Open-Loop Gain and Phase vs. Frequency

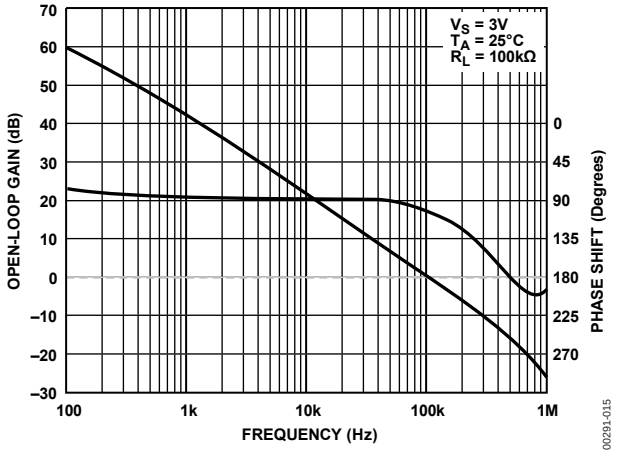


Figure 15. Open-Loop Gain and Phase vs. Frequency

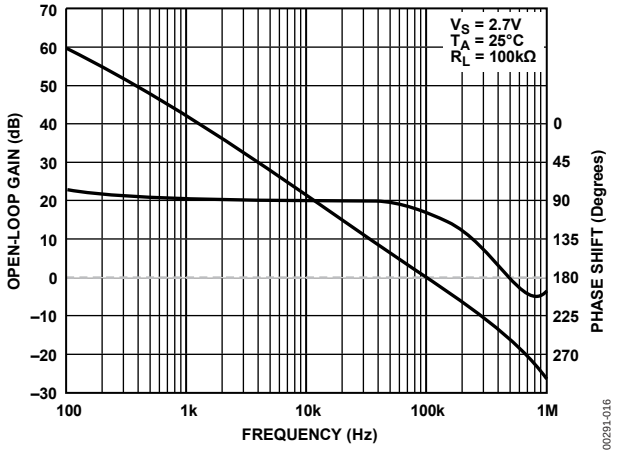


Figure 16. Open-Loop Gain and Phase vs. Frequency

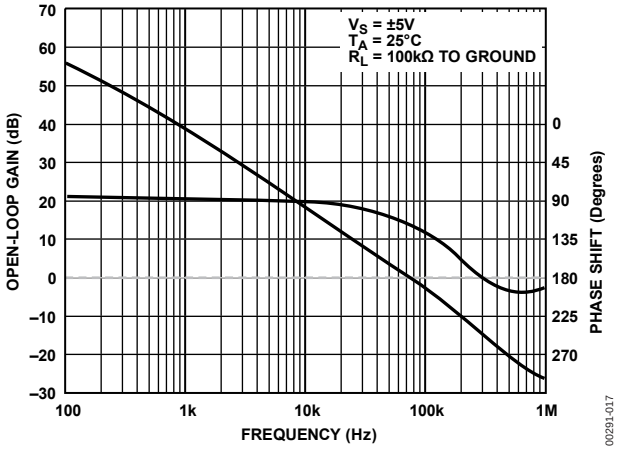


Figure 17. Open-Loop Gain and Phase vs. Frequency

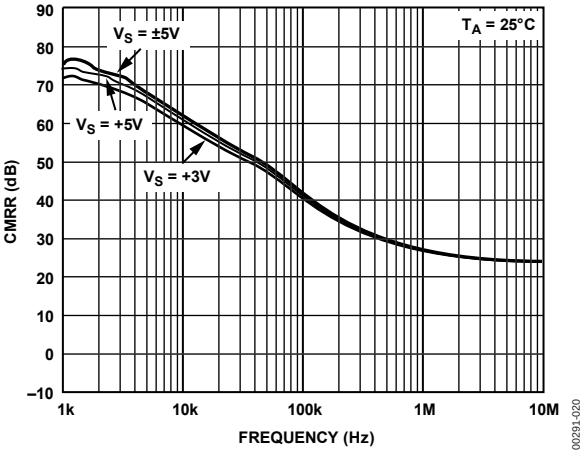


Figure 20. CMRR vs. Frequency

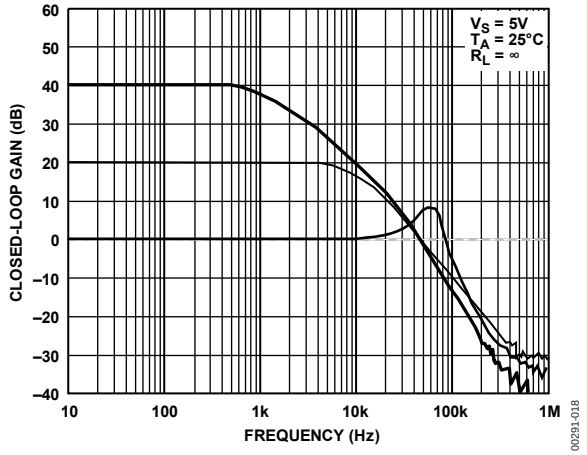


Figure 18. Closed-Loop Gain vs. Frequency

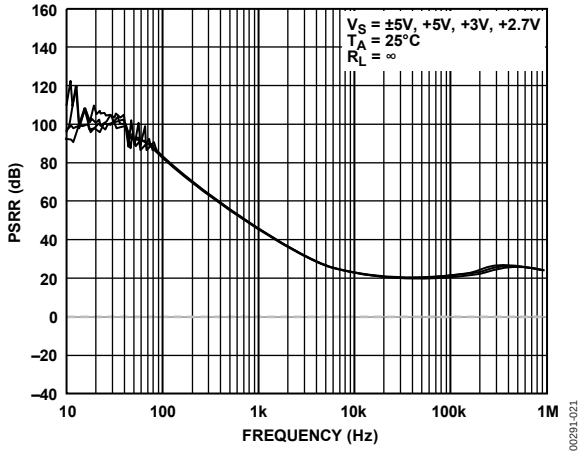


Figure 21. PSRR vs. Frequency

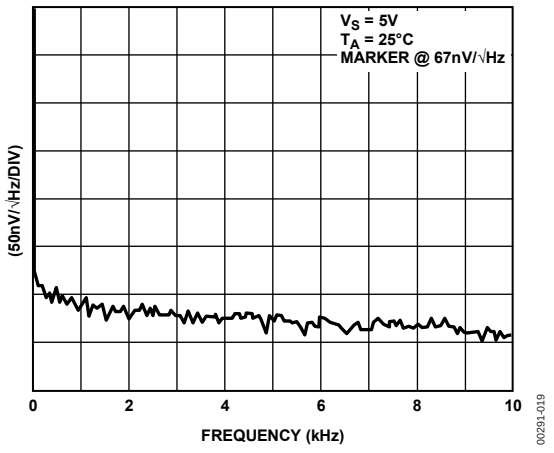


Figure 19. Voltage Noise Density vs. Frequency

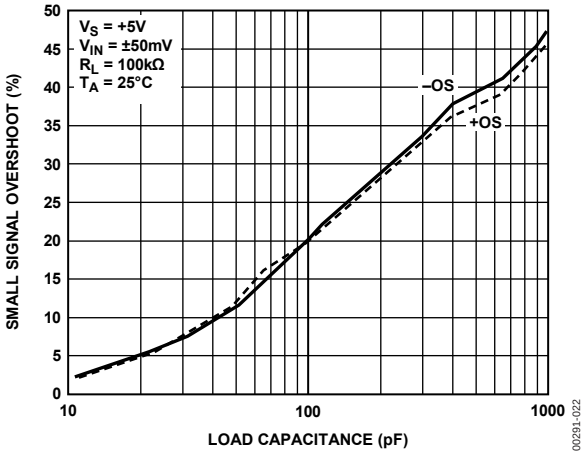


Figure 22. Small-Signal Overshoot vs. Load Capacitance

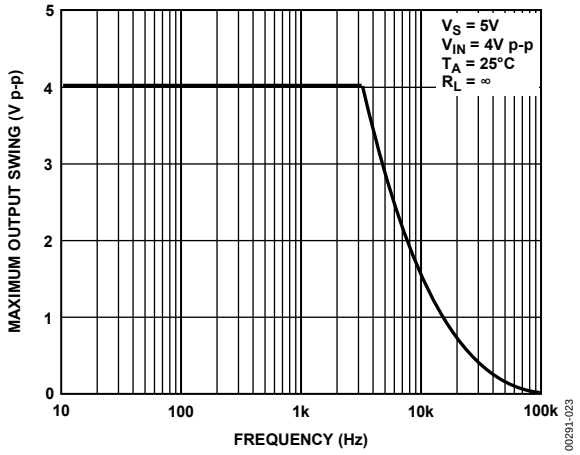


Figure 23. Maximum Output Swing vs. Frequency

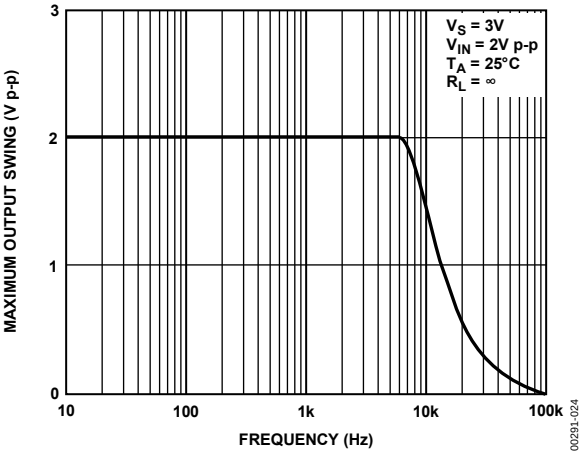


Figure 24. Maximum Output Swing vs. Frequency

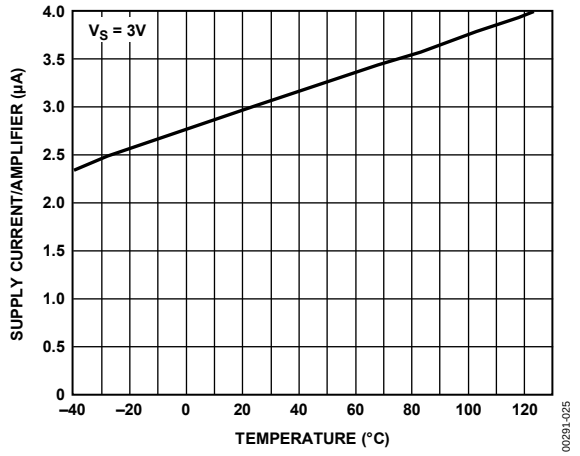


Figure 25. Supply Current/Amplifier vs. Temperature

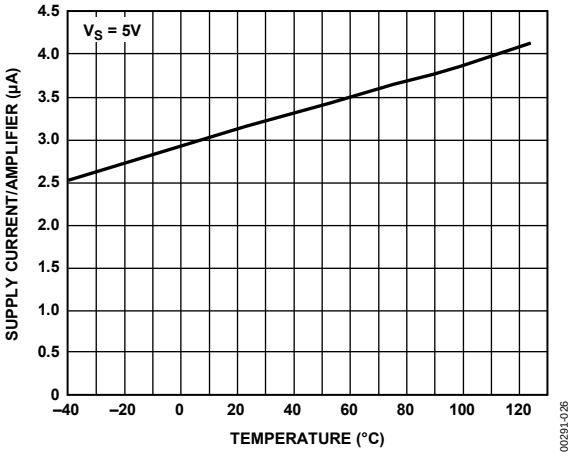


Figure 26. Supply Current/Amplifier vs. Temperature

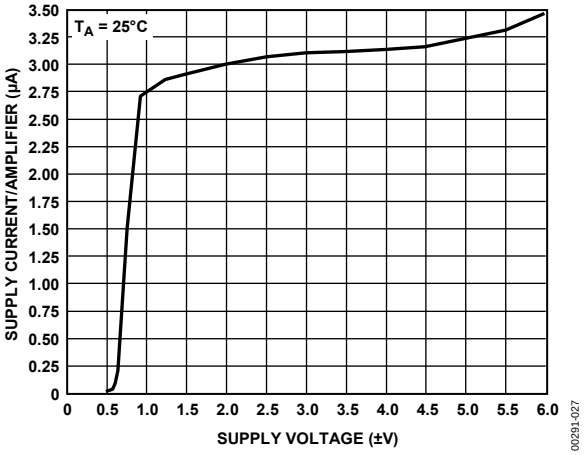


Figure 27. Supply Current/Amplifier vs. Supply Voltage

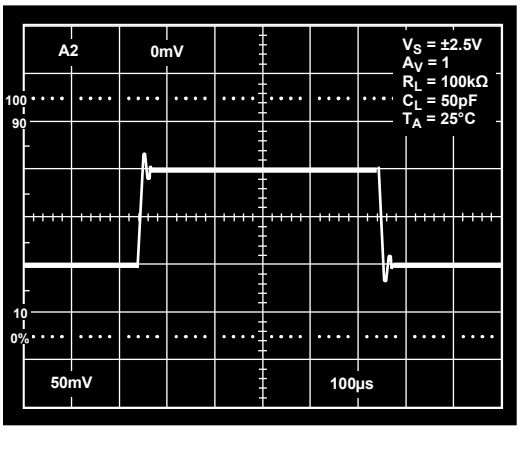


Figure 28. Small-Signal Transient Response

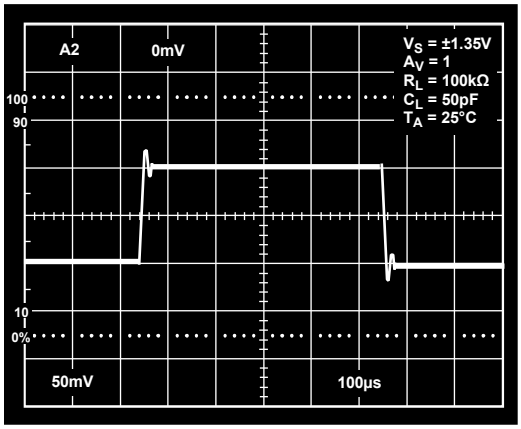


Figure 29. Small-Signal Transient Response

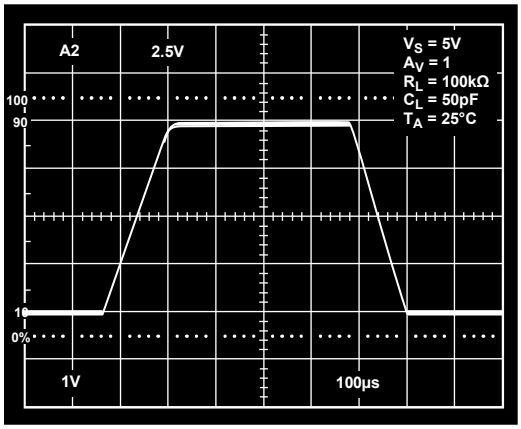


Figure 30. Large-Signal Transient Response

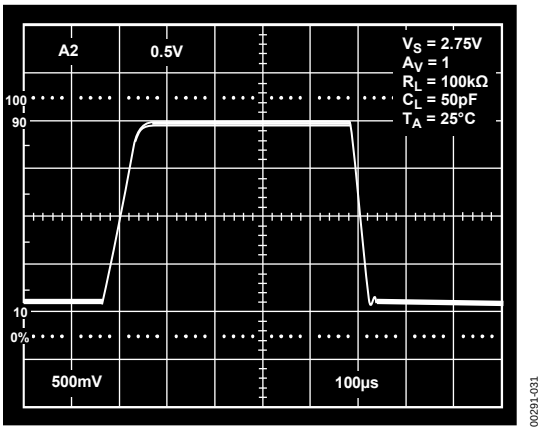


Figure 31. Large-Signal Transient Response

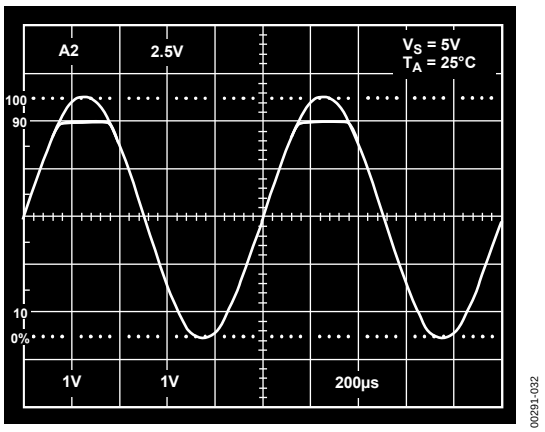


Figure 32. No Phase Reversal

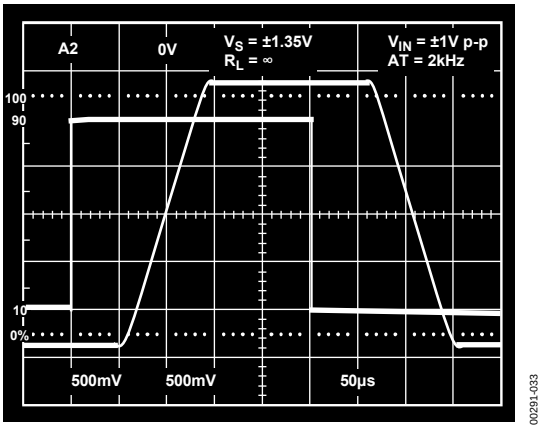


Figure 33. Saturation Recovery Time

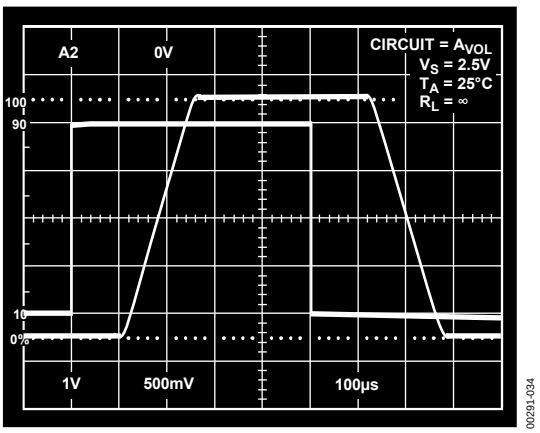


Figure 34. Saturation Recovery Time

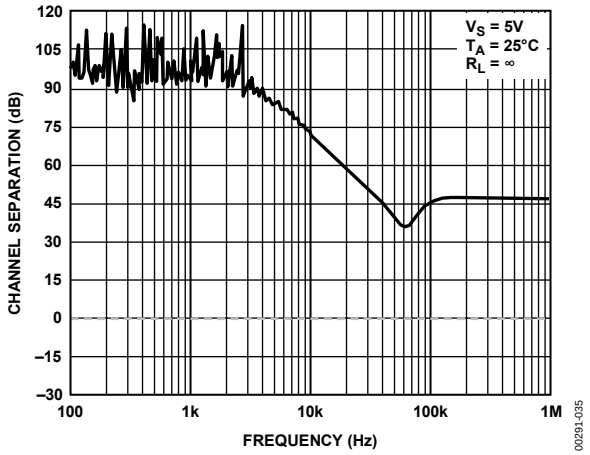


Figure 35. Channel Separation vs. Frequency

APPLICATIONS

THEORY OF OPERATION

The OPx81 family of op amps is comprised of extremely low powered, rail-to-rail output amplifiers, requiring less than 4 μA of quiescent current per amplifier. Many other competitors' devices may be advertised as low supply current amplifiers but draw significantly more current as the outputs of these devices are driven to a supply rail. The supply current of the OPx81 remains under 4 μA even when the output is driven to either supply rail. Supply currents should meet the specification as long as the inputs and outputs remain within the range of the power supplies.

Figure 36 shows a simplified schematic of a single channel for the OPx81. A bipolar differential pair is used in the input stage. PNP transistors are used to allow the input stage to remain linear with the common-mode range extending to ground. This is an important consideration for single-supply applications. The bipolar front end also contributes less noise than a MOS front end with only nanoamps of bias currents. The output of the op amp consists of a pair of CMOS transistors in a common source configuration. This setup allows the output of the amplifier to swing to within millivolts of either supply rail. The headroom required by the output stage is limited by the amount of current being driven into the load. The lower the output current, the closer the output can go to either supply rail. Figure 11, Figure 12, and Figure 13 show the output voltage headroom vs. the load current. This behavior is typical of rail-to-rail output amplifiers.

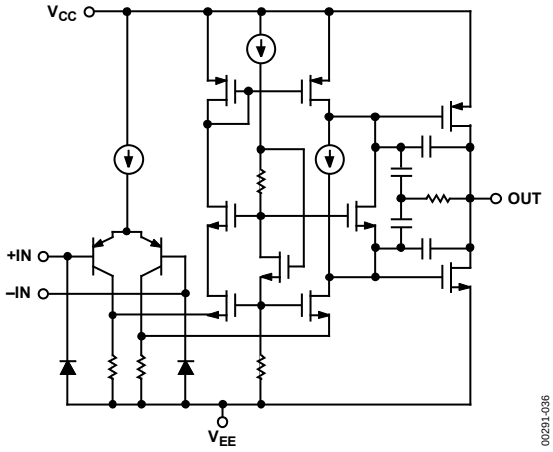


Figure 36. Simplified Schematic of a Single OPx81 Channel

INPUT OVERVOLTAGE PROTECTION

The input stage to the OPx81 family of op amps consists of a PNP differential pair. If the base voltage of either of these input transistors drops to more than 0.6 V below the negative supply, the input ESD protection diodes become forward-biased, and large currents begin to flow. In addition to possibly damaging the device, this creates a phase reversal effect at the output. To prevent this, the input current should be limited to less than 0.5 mA.

This can be done by simply placing a resistor in series with the input to the device. The size of the resistor should be proportional to the lowest possible input signal excursion and can be found using the following formula:

$$R = \frac{V_{EE} - V_{IN,MIN}}{0.5 \times 10^{-3}}$$

where:
V_{EE} is the negative power supply for the amplifier.
$V_{IN, MIN}$ is the lowest input voltage excursion expected.

For example, a single channel of the OPx81 should be used with a single-supply voltage of +5 V if the input signal may go as low as −1 V. Because the amplifier is powered from a single supply, V_{EE} is the ground; therefore, the necessary series resistance should be 2 kΩ.

INPUT OFFSET VOLTAGE

The OPx81 family of op amps was designed for low offset voltages (less than 1 mV).

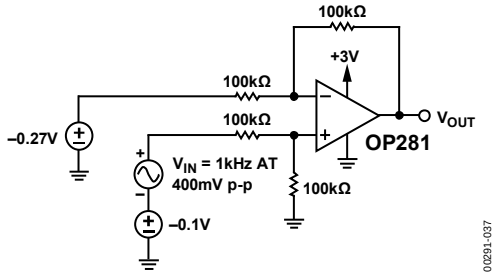


Figure 37. Single OPx81 Channel Configured as a Difference Amplifier Operating at V_{CM} < 0 V

INPUT COMMON-MODE VOLTAGE RANGE

The OPx81 is rated with an input common-mode voltage range from V_{EE} to 1 V less than V_{CC}. However, the op amp can operate with a common-mode voltage that is slightly less than V_{EE}. Figure 37 shows a single OPx81 channel configured as a difference amplifier with a single-supply voltage of 3 V. Negative dc voltages are applied at both input terminals, creating a common-mode voltage that is less than ground. A 400 mV p-p input signal is then applied to the noninverting input. Figure 38 shows the resulting input and output waves. Notice how the output of the amplifier also drops slightly negative without distortion.

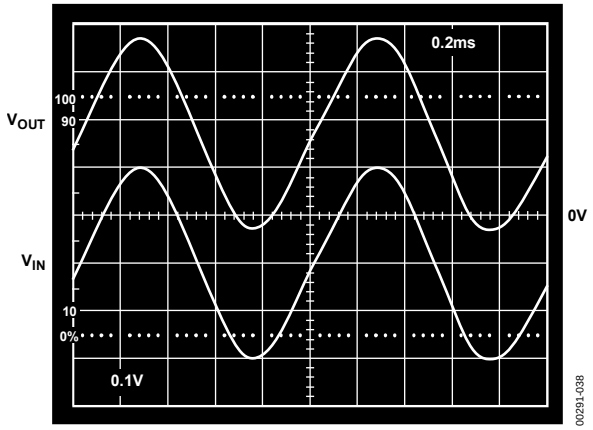


Figure 38. Input and Output Signals with V_{CM} < 0 V

CAPACITIVE LOADING

Most low supply current amplifiers have difficulty driving capacitive loads due to the higher currents required from the output stage for such loads. Higher capacitance at the output will increase the amount of overshoot and ringing in the amplifier's step response and may affect the stability of the device. However, through careful design of the output stage and its high phase margin, the OPx81 family can tolerate some degree of capacitive loading. Figure 39 shows the step response of a single channel with a 10 nF capacitor connected at the output. Notice that the overshoot of the output does not exceed more than 10% with such a load, even with a supply voltage of only 3 V.

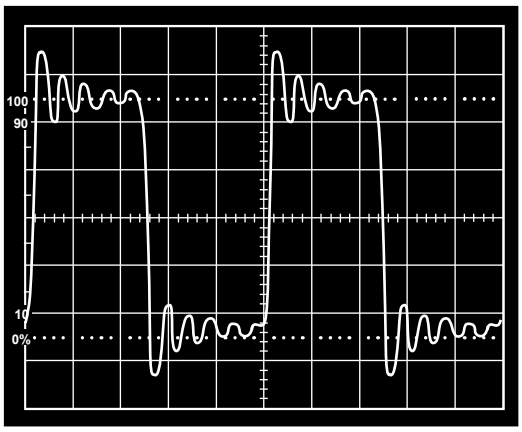


Figure 39. Ringing and Overshoot of the Output of the Amplifier

MICROPOWER REFERENCE VOLTAGE GENERATOR

Many single-supply circuits are configured with the circuit biased to half of the supply voltage. In these cases, a false ground reference can be created by using a voltage divider buffered by an amplifier. Figure 40 shows the schematic for such a circuit.

The two 1 MΩ resistors generate the reference voltage while drawing only 1.5 μA of current from a 3 V supply. A capacitor connected from the inverting terminal to the output of the op amp provides compensation to allow a bypass capacitor to be connected at the reference output. This bypass capacitor helps to establish an ac ground for the reference output. The entire reference generator draws less than 5 μA from a 3 V supply source.

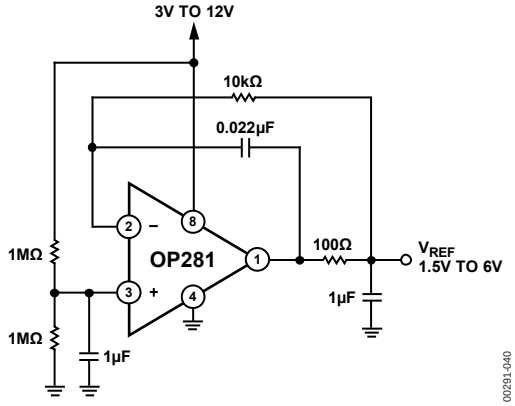


Figure 40. Single Channel Configured as a Micropower Bias Voltage Generator

WINDOW COMPARATOR

The extremely low power supply current demands of the OPx81 family make it ideal for use in long-life battery-powered applications such as a monitoring system. Figure 41 shows a circuit that uses the OP281 as a window comparator.

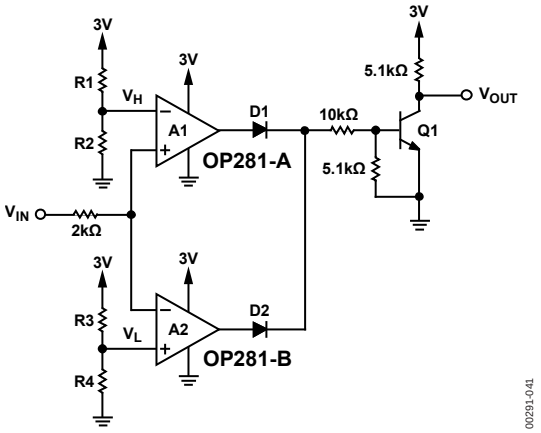


Figure 41. Using the OP281 as a Window Comparator

The threshold limits for the window are set by V_H and V_L, provided that $V_H > V_L$. The output of the first OP281 (A1) will stay at the negative rail, in this case ground, as long as the input voltage is less than V_H. Similarly, the output of the second OP281 (A2) will stay at ground as long the input voltage is higher than V_L. As long as V_{IN} remains between V_L and V_H, the outputs of both op amps will be 0 V. With no current flowing in either D1 or D2, the base of Q1 will stay at ground, putting the transistor in cutoff and forcing V_{OUT} to the positive supply rail. If the input voltage rises above V_H, the output of A2 stays at ground, but the output of A1 goes to the positive rail and D1 conducts current. This creates a base voltage that turns on Q1 and drives V_{OUT} low. The same condition occurs if V_{IN} falls below V_L with A2's output going high and D2 conducting current. Therefore, V_{OUT} is high if the input voltage is between V_L and V_H, but low if the input voltage moves outside of that range.

The R1 and R2 voltage divider sets the upper window voltage, and the R3 and R4 voltage divider sets the lower voltage for the window. For the window comparator to function properly, V_H must be a greater voltage than V_L.

$$V_H = \frac{R2}{R1 + R2}$$

$$V_L = \frac{R4}{R3 + R4}$$

The 2 kΩ resistor connects the input voltage of the input terminals to the op amps. This protects the OP281 from possible excess current flowing into the input stages of the devices. D1 and D2 are small-signal switching diodes (1N4446 or equivalent), and Q1 is a 2N2222 or an equivalent NPN transistor.

LOW-SIDE CURRENT MONITOR

In the design of power-supply control circuits, a great deal of design effort is focused on ensuring the long-term reliability of a pass transistor over a wide range of load current conditions. As a result, monitoring and limiting device power dissipation is of primary importance in these designs. Figure 42 shows an example of a 5 V, single-supply current monitor that can be incorporated into the design of a voltage regulator with fold-back current limiting or a high current power supply with crowbar protection. The design capitalizes on the OPx81's common-mode range extending to ground. Current is monitored in the power-supply return path, where a 0.1 Ω shunt resistor, R_{SENSE}, creates a very small voltage drop. The voltage at the inverting terminal becomes equal to the voltage at the noninverting terminal through the feedback of Q1, which is a 2N2222 or an equivalent NPN transistor. This makes the voltage drop across R1 equal to the voltage drop across R_{SENSE}. Therefore, the current through Q1 becomes directly proportional to the current through R_{SENSE}, and the output voltage is given by the following equation:

$$V_{OUT} = V_{CC} - \left(\frac{R2}{R1} \times R_{SENSE} \times I_L \right)$$

The voltage drop across R2 increases as I_L increases; therefore, V_{OUT} decreases if a higher supply current is sensed. For the element values shown, the V_{OUT} transfer characteristic is −2.5 V/A, decreasing from V_{CC}.

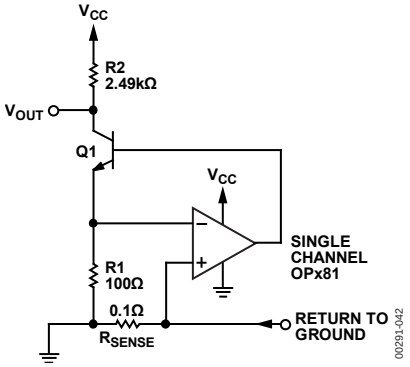


Figure 42. Low-Side Load Current Monitor

LOW VOLTAGE HALF-WAVE AND FULL-WAVE RECTIFIERS

Because of its quick overdrive recovery time, an OP281 can be configured as a full-wave rectifier for low frequency (<500 Hz) applications. Figure 43 shows the schematic.

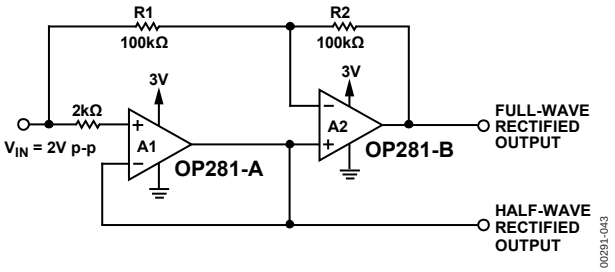


Figure 43. Single-Supply Full-Wave and Half-Wave Rectifiers Using an OP281

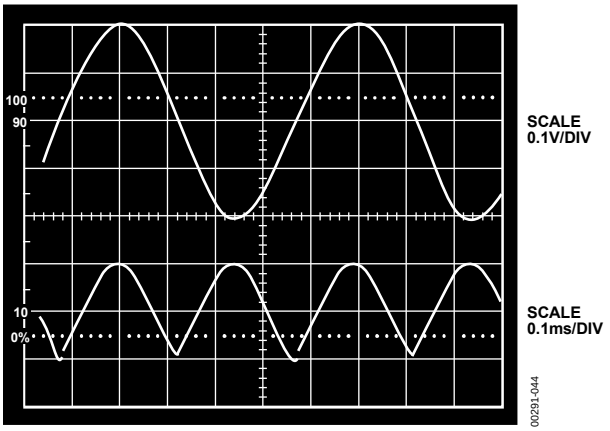


Figure 44. Full-Wave Rectified Signal

Amplifier A1 is used as a voltage follower that tracks the input voltage only when it is greater than 0 V. This provides a half-wave rectification of the input signal to the noninverting terminal of Amplifier A2. When A1's output is following the input, the inverting terminal of A2 also follows the input from the virtual ground between the inverting and noninverting terminals of A2. With no potential difference across R1, no current flows through either R1 or R2; therefore, the output of A2 also follows the input. When the input voltage goes below 0 V, the noninverting terminal of A2 becomes 0 V. This makes A2 work as an inverting amplifier with a gain of 1 and provides a full-wave rectified version of the input signal. A 2 kΩ resistor in series with A1's noninverting input protects the device when the input signal becomes less than ground.

BATTERY-POWERED TELEPHONE HEADSET AMPLIFIER

Figure 45 shows how the OP281 can be used as a two-way amplifier in a telephone headset. One side of the OP281 can be used as an amplifier for the microphone, and the other side can be used to drive the speaker. A typical telephone headset uses a 600 Ω speaker and an electret microphone that requires a supply voltage and a biasing resistor.

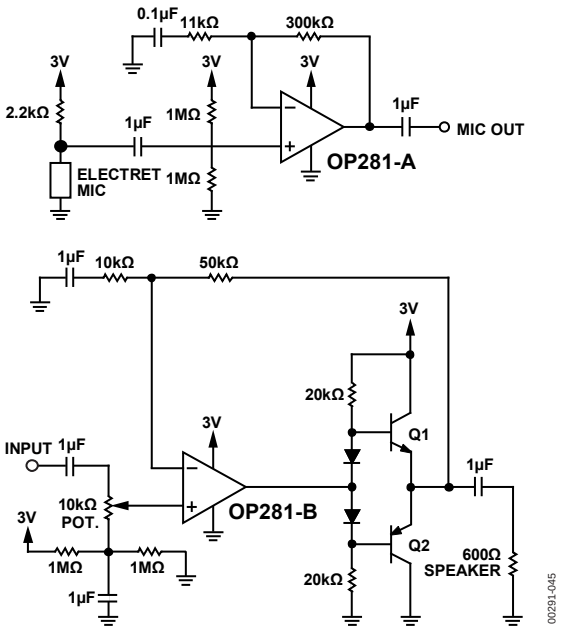


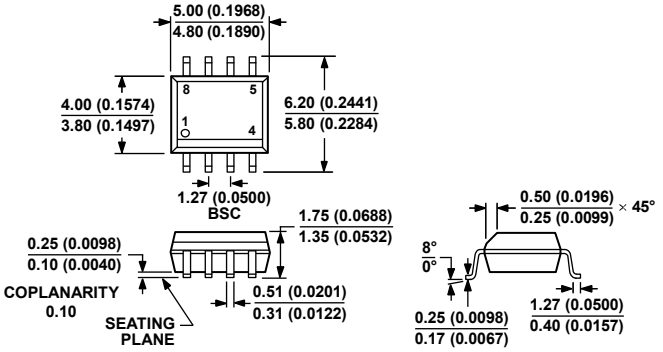
Figure 45. Two-Way Amplifier in a Battery-Powered Telephone Headset

The OP281-A op amp provides about 29 dB of gain for audio signals coming from the microphone. The gain is set by the 300 kΩ and 11 kΩ resistors. The gain bandwidth product of the amplifier is 95 kHz, which yields a −3 dB rolloff at 3.4 kHz for the set gain of 28. This is acceptable because telephone audio is band limited for 300 kHz to 3 kHz signals. If higher gain is required for the microphone, an additional gain stage should be used, because adding more gain to the OP281 would limit the audio bandwidth. A 2.2 kΩ resistor is used to bias the electret microphone. This resistor value may vary depending on the specifications of the microphone. The output of the microphone is ac-coupled to the noninverting terminal of the op amp. Two 1 MΩ resistors are used to provide the dc offset for single-supply use.

The OP281-B amplifier (see Figure 45) can provide up to 15 dB of gain for the headset speaker. Incoming audio signals are ac-coupled to a 10 kΩ potentiometer that is used to adjust the volume. Again, two 1 MΩ resistors provide the dc offset with a 1 µF capacitor establishing an ac ground for the volume-control potentiometer. Because the OP281 is a rail-to-rail output amplifier, it would have difficulty driving a 600 Ω speaker directly. Here, a Class AB buffer is used to isolate the load from the amplifier and to provide the necessary current to drive the speaker. By placing the buffer in the feedback loop of the op amp, crossover distortion can be minimized. Q1 and Q2 should have minimum betas of 100. The 600 Ω speaker is ac-coupled to the emitters to prevent quiescent current from flowing into the speaker. The 1 µF coupling capacitor makes an equivalent high-pass filter cutoff at 265 Hz with a 600 Ω load attached. Again, this does not pose a problem because it is outside the frequency range for telephone audio signals.

The circuit in Figure 45 draws around 250 µA of current. The Class AB buffer has a quiescent current of 140 µA, and roughly 100 µA is drawn by the microphone itself. A CR2032 3 V lithium battery has a life expectancy of 160 mA hours, which means this circuit can run continuously for 640 hours on a single battery.

OUTLINE DIMENSIONS



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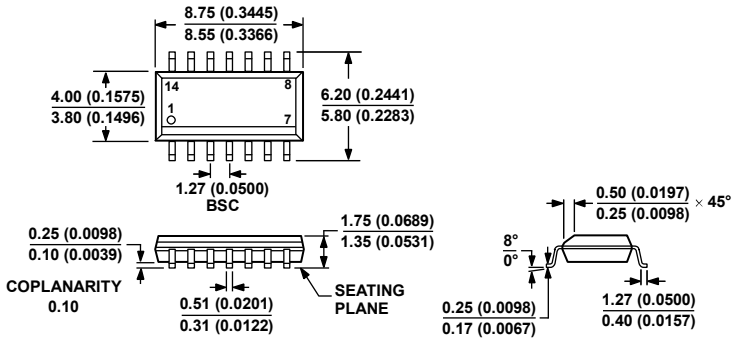
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 46. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012-AB
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(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

Figure 47. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-14)
Dimensions shown in millimeters and (inches)

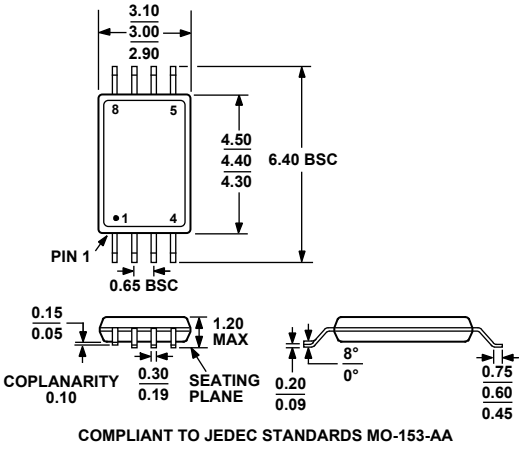

Figure 48. 8-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-8)
Dimensions shown in millimeters

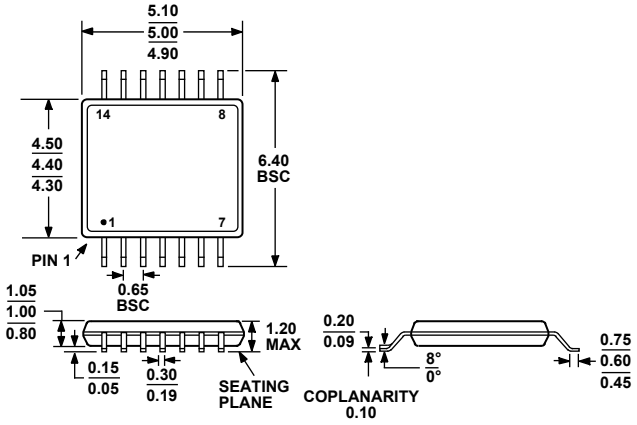

Figure 49. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
OP281GRU-REEL	–40°C to +85°C	8-Lead TSSOP	RU-8
OP281GRUZ-REEL[1]	–40°C to +85°C	8-Lead TSSOP	RU-8
OP281GS	–40°C to +85°C	8-Lead SOIC_N	R-8
OP281GS-REEL	–40°C to +85°C	8-Lead SOIC_N	R-8
OP281GS-REEL7	–40°C to +85°C	8-Lead SOIC_N	R-8
OP281GSZ[1]	–40°C to +85°C	8-Lead SOIC_N	R-8
OP281GSZ-REEL[1]	–40°C to +85°C	8-Lead SOIC_N	R-8
OP281GSZ-REEL7[1]	–40°C to +85°C	8-Lead SOIC_N	R-8
OP481GRU-REEL	–40°C to +85°C	14-Lead TSSOP	RU-14
OP481GRUZ-REEL[1]	–40°C to +85°C	14-Lead TSSOP	RU-14
OP481GS	–40°C to +85°C	14-Lead SOIC_N	R-14
OP481GS-REEL	–40°C to +85°C	14-Lead SOIC_N	R-14
OP481GS-REEL7	–40°C to +85°C	14-Lead SOIC_N	R-14
OP481GSZ[1]	–40°C to +85°C	14-Lead SOIC_N	R-14
OP481GSZ-REEL[1]	–40°C to +85°C	14-Lead SOIC_N	R-14
OP481GSZ-REEL7[1]	–40°C to +85°C	14-Lead SOIC_N	R-14

[1] Z = RoHS Compliant Part.

NOTES

NOTES

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