



# THE DATASHEET OF ONET4201LDRGET



## 155-Mbps to 4.25-Gbps LASER DRIVER

Check for Samples: [ONET4201LD](#)

### FEATURES

- **Multirate Operation From 155 Mbps up to 4.25 Gbps**
- **Bias Current Programmable From 1 mA to 100 mA**
- **Modulation Current Programmable From 5 mA to 85 mA**
- **APC and Fault Detection**
- **Fault Mode Selection**
- **Bias and Photodiode Current Monitors**
- **CML Data Inputs**
- **Temperature Compensation of Modulation Current**
- **Single 3.3-V Supply**
- **Active Back-Termination at the Output**
- **Surface-Mount, Small-Footprint, 4-mm × 4-mm, 24-Lead QFN Package**

### APPLICATIONS

- **SONET/SDH Transmission Systems**
- **Fibre Channel Optical Modules**
- **Fiber Optic Data Links**
- **Digital Cross-Connects**
- **Optical Transmitters**

### DESCRIPTION

The ONET4201LD is a laser driver for multiple fiber optic applications up to 4.25 Gbps. The device accepts CML input data and provides bias and modulation currents for driving a laser diode. Also provided are automatic power control (APC), temperature compensation of modulation current, fault detection, and current monitor features.

The device is available in a small-footprint, 4-mm × 4-mm, 24-pin, QFN package. The circuit requires a single 3.3-V supply.

This power-efficient laser driver is characterized for operation from –40°C to 85°C.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### DETAILED DESCRIPTION

#### BLOCK DIAGRAM

A simplified block diagram of the ONET4201LD is shown in Figure 1.

This compact, low-power, 4.25-Gbps laser driver circuit consists of a high-speed data path and a bias and control block.

The function of the data path is to buffer the input data and then modulate the laser diode current according to the input data stream.

The bias and control block generates the laser diode bias current, contains automatic power control (APC) to maintain constant optical output power, generates a modulation current that can be temperature compensated and controls power-on during start-up and shutdown after failure detection. The circuit design is optimized for high-speed and low-voltage operation (3.3 V).

The main circuit blocks are described in detail below.

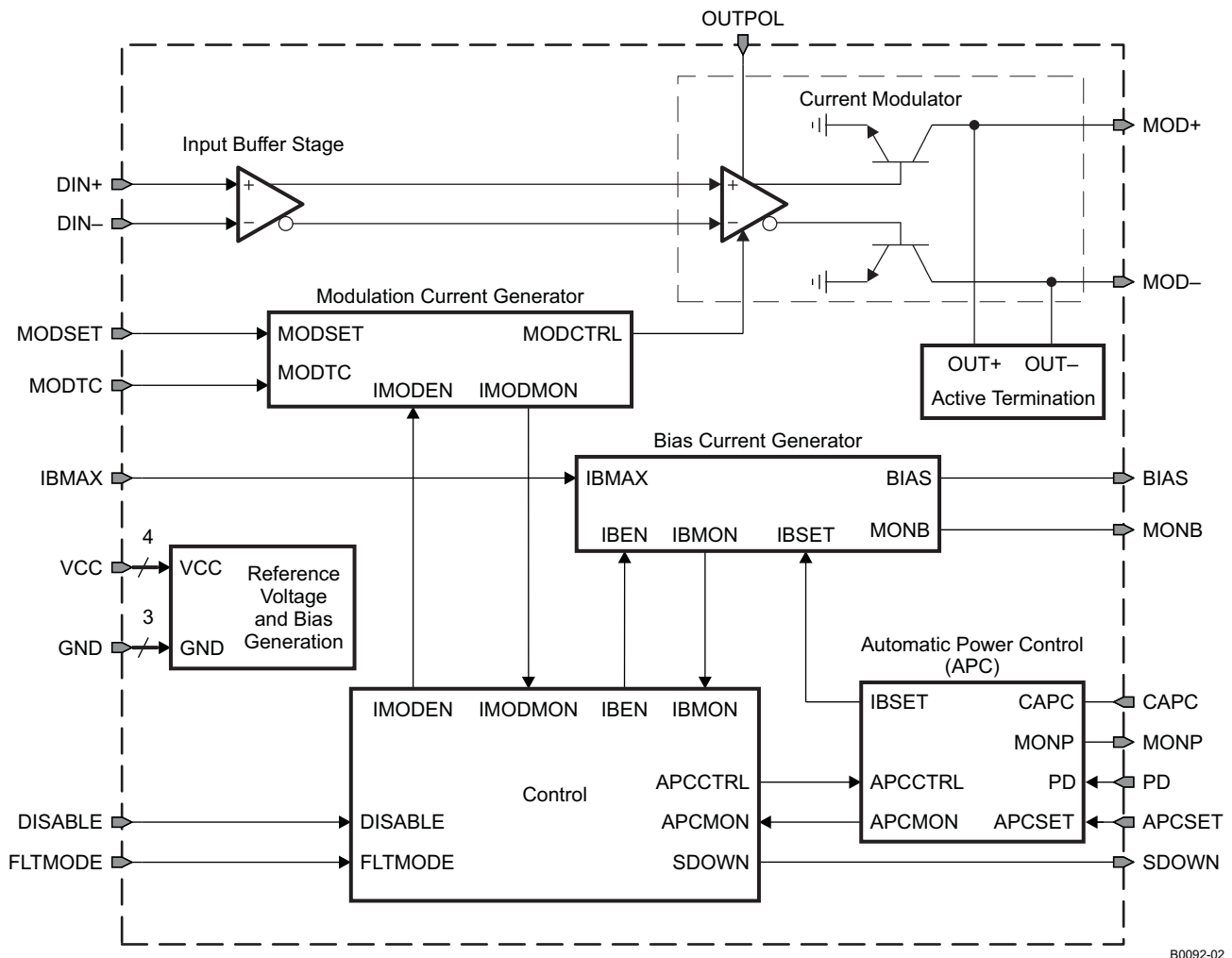


Figure 1. Simplified Block Diagram of the ONET4201LD

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## HIGH-SPEED DATA PATH

The high-speed data path consists of an input buffer stage and a current modulator.

The input buffer stage takes CML compatible differential signals. It provides on-chip 50-Ω termination to VCC. AC-coupling may be used at the DIN+ and DIN– inputs.

The laser diode current modulator mainly consists of two common-emitter output transistors and the required driver circuitry. Depending on the input data stream, the modulation current is sunk at the MOD+ or the MOD– pin.

Modulation current setting is performed by means of the modulation current generator block, which is supervised by the control circuit block.

The laser diode can be either ac- or dc-coupled. In both cases, the maximum modulation current is 85 mA. The modulation output is optimized for driving a 20-Ω load.

For optimum performance when driving a laser diode over a 20-Ω transmission line, the ONET4201LD provides active 20-Ω back-termination, which minimizes jitter caused by reflections.

## BIAS AND CONTROL

The bias and control circuitry consists of the bandgap voltage and bias generation block, the bias current generator, the automatic power control block and the supervising control circuitry.

### BANDGAP VOLTAGE AND BIAS GENERATION

The bandgap voltage reference provides process and temperature-independent reference voltages needed to set bias current, modulation current, and photodiode reference current. Additionally, this block provides the biasing for all internal circuits.

### AUTOMATIC POWER CONTROL

The ONET4201LD laser driver incorporates an APC loop to compensate for the changes in laser threshold current over temperature and lifetime. The internal APC is enabled when resistors are connected to the IBMAX and APCSET pins. A back-facet photodiode mounted in the laser package is used to detect the average laser output power. The photodiode current  $I_{PD}$ , which is proportional to the average laser power, can be calculated by using the laser-to-monitor transfer ratio,  $\rho_{MON}$ , and the average power,  $P_{AVG}$ :

$$I_{PD} [A] = P_{AVG} [W] \times \rho_{MON} [A/W] \quad (1)$$

In closed-loop operation, the APC modifies the laser diode bias current by comparing  $I_{PD}$  with a reference current  $I_{APCSET}$  and generates a bias compensation current.  $I_{PD}$  can be programmed by selecting the external resistor  $R_{APCSET}$  according to:

$$R_{APCSET} [\Omega] = \frac{4.69 V}{I_{PD} [A]} = \frac{4.69 V}{P_{AVG} [W] \times \rho_{MON} [A/W]} \quad (2)$$

The bias compensation current subtracts from the maximum bias current to maintain the monitor photodiode current. The maximum bias current is programmed by the resistor connected to IBMAX:

$$I_{BIASMAX} [A] = \frac{343 V}{R_{BIASMAX} [\Omega]} \quad (3)$$

This current limit establishes the maximum bias current available in closed loop mode, as well as in transient fault conditions such as shorts at the PD pin to ground or delayed laser power up.

An external pin MONB is provided as a bias current monitor output. A fraction of the bias current (1/68) is mirrored and develops a voltage drop across an external resistor to ground,  $R_{MONB}$ . The voltage at MONB is given as:

$$V_{MONB} [V] = \frac{R_{MONB} [\Omega] \times I_{BIAS} [A]}{68} \quad (4)$$

If the voltage at MONB is greater than the programmed threshold, a fault mode occurs.

The MONP is also provided as a photocurrent monitor output. The photodiode current,  $I_{PD}$ , is mirrored and develops a voltage across an external resistor to ground,  $R_{MONP}$ . The voltage at MONP is given as:

$$V_{MONP}[V] = R_{MONP}[\Omega] \times I_{PD}[A] \quad (5)$$

If the voltage at MONP is greater than the programmed threshold, a fault mode occurs.

As with any negative-feedback system design, care must be taken to assure stability of the loop. The loop bandwidth must not be too high in order to minimize pattern-dependent jitter. The dominant pole is determined by the capacitor  $C_{APC}$ . The recommended value for  $C_{APC}$  is 200 nF. The capacitance of the monitor photodiode  $C_{PD}$  adds another pole to the system, and thus it must be small enough to maintain stability. The recommended value for this capacitance is  $C_{PD} \leq 50$  pF.

The internal APC loop can be disabled by connecting a 100-k $\Omega$  resistor from APCSET to VCC and leaving PD open. In open-loop operation, the laser diode current is set by  $I_{BIASMAX}$  and  $I_{MODSET}$ .

## MODULATION-CURRENT GENERATOR

The modulation-current generator defines the tail current of the modulator, which is sunk from either MOD+ or MOD–, depending on the data pattern. The modulation current consists of a modulation current  $I_{MOD0}$  at a reference temperature  $T_0 = 60^\circ\text{C}$  (set by the resistor  $R_{MODSET}$ ) and a temperature-dependent modulation current defined by the resistor  $R_{MODTC}$ . The modulation current can be estimated as follows:

$$I_{MOD}[A] = \frac{265 \text{ V}}{R_{MODSET}[\Omega]} \times \left( 1 + \left( \frac{24 \Omega}{R_{MODTC}[\Omega]} + 630 \text{ ppm} \right) \times (T[^\circ\text{C}] - T_0[^\circ\text{C}]) \right) \quad (6)$$

Note that the reference temperature,  $T_0$ , and the temperature compensation set by  $R_{MODTC}$  vary from part to part. To reduce the variation,  $I_{MOD}$  can be calibrated over temperature and set with a microcontroller DAC or digital potentiometer.

## CONTROL

The functions of this block are to control the start-up sequence, detect faults, detect tracking failure of the APC loop, and provide disable control. The laser driver has a controlled start-up sequence, which helps prevent transient glitches from being applied to the laser during power on. At start-up, the laser diode is off, SDOWN is low, and the APC loop is open. Once  $V_{CC}$  reaches  $\sim 2.8$  V, the laser diode bias generator and modulation current generator circuitry are activated (if DISABLE is low). The slow-start circuitry gradually brings up the current delivered to the laser diode. From the time that  $V_{CC}$  reaches  $\sim 2.8$  V until the modulation current and bias current reach 95% of their steady state value, is considered the initialization time. If DISABLE is asserted during power on, the slow-start circuitry does not activate until DISABLE is negated.

## FAULT DETECTION

The fault-detection circuitry monitors the operation of the ONET4201LD. If FLTMODE is set to a low level, (hard-fault mode) this circuitry disables the bias and modulation circuits and latches the SDOWN output on detection of a fault. The fault mode is reset by toggling DISABLE (for a minimum time of  $T_{RES}$ ) or by toggling  $V_{CC}$ .

Once DISABLE is toggled, SDOWN is set low and the circuit is re-initialized.

If FLTMODE is set to a high level (soft-fault mode), a fault is indicated at the SDOWN output; however, the bias and modulation circuits are not disabled. The SDOWN output is reset once the fault causing condition disappears. Toggling DISABLE or  $V_{CC}$  is not required.

A functional representation of the fault detection circuitry is shown in [Figure 2](#).

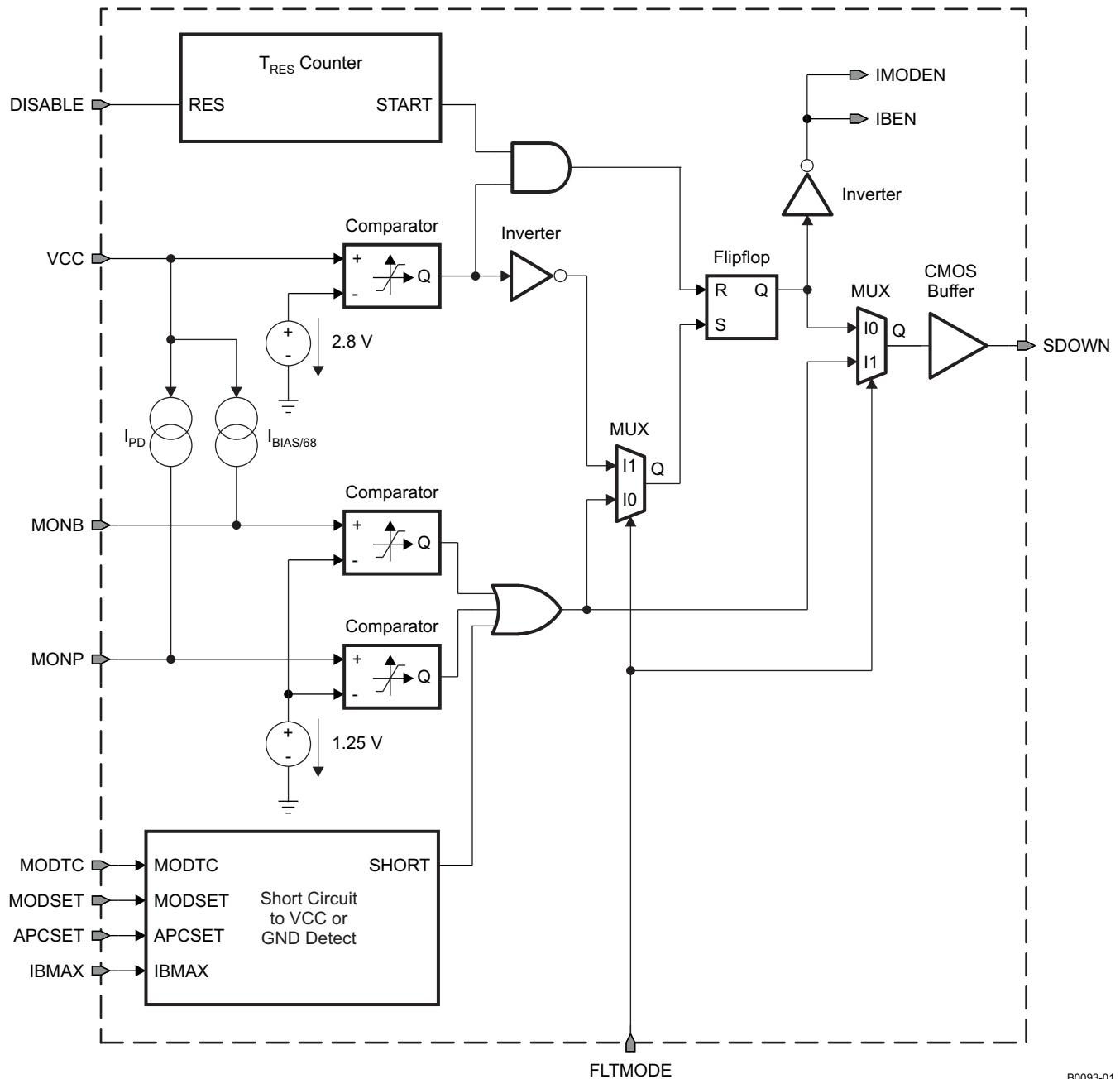


Figure 2. Functional Representation of the Fault Detection Circuitry

A fault mode is produced if the laser cathode is grounded and the photocurrent causes MONP to exceed its programmed threshold. Another fault mode can be produced if the laser diode end-of-life condition causes excessive bias current and photodiode current that results in monitor voltages (MONP, MONB) being greater than their programmed threshold. Other fault modes can occur if there are any I/O pin single-point failures (short to  $V_{CC}$  or GND) and the monitor voltages exceed their programmed threshold (see [Table 1](#)).

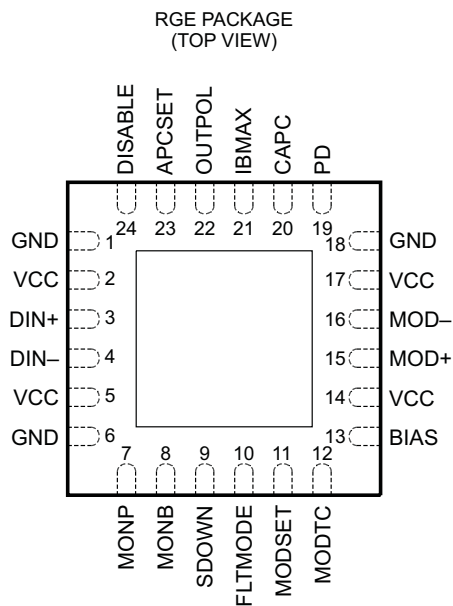
**Table 1. Response to I/O-Pin Shorts to VCC or GND**

PIN	FLTMODE = LOW		FLTMODE = HIGH	
	Response to Short to GND	Response to Short to V <sub>CC</sub>	Response to Short to GND	Response to Short to V <sub>CC</sub>
APCSET	SDOWN latched high, I <sub>BIAS</sub> and I <sub>MOD</sub> disabled	No fault, I <sub>MOD</sub> unaffected	SDOWN high, I <sub>BIAS</sub> and I <sub>MOD</sub> unaffected	No fault
BIAS	SDOWN latched high, I <sub>MOD</sub> disabled	No fault, I <sub>BIAS</sub> goes to zero	SDOWN high, I <sub>MOD</sub> unaffected	No fault, I <sub>MOD</sub> unaffected
CAPC	No fault	No fault, I <sub>BIAS</sub> goes to zero	No fault, I <sub>MOD</sub> unaffected	No fault, I <sub>BIAS</sub> goes to zero
DIN+	No fault, I <sub>MOD</sub> disabled	No fault	No fault, I <sub>MOD</sub> disabled	No fault
DIN-	No fault, I <sub>MOD</sub> disabled	No fault	No fault, I <sub>MOD</sub> disabled	No fault
DISABLE	Normal circuit operation	Normal circuit operation	Normal circuit operation	Normal circuit operation
IBMAX	SDOWN latched high, I <sub>BIAS</sub> and I <sub>MOD</sub> disabled	SDOWN latched high, I <sub>BIAS</sub> and I <sub>MOD</sub> disabled	SDOWN high, I <sub>MOD</sub> unaffected	SDOWN high, I <sub>MOD</sub> unaffected
MOD+	SDOWN latched high, I <sub>BIAS</sub> and I <sub>MOD</sub> disabled	No fault	SDOWN high, I <sub>BIAS</sub> unaffected	No fault
MOD-	SDOWN latched high, I <sub>BIAS</sub> and I <sub>MOD</sub> disabled	No fault	SDOWN high, I <sub>BIAS</sub> unaffected	No fault
MODSET	SDOWN latched high, I <sub>BIAS</sub> and I <sub>MOD</sub> disabled	No fault, disables I <sub>MOD</sub>	SDOWN high, I <sub>BIAS</sub> unaffected	No fault, disables I <sub>MOD</sub>
MODTC	SDOWN latched high, I <sub>BIAS</sub> and I <sub>MOD</sub> disabled	No fault	SDOWN high, I <sub>BIAS</sub> and I <sub>MOD</sub> unaffected	No fault
MONB	No fault	SDOWN latched high, I <sub>BIAS</sub> and I <sub>MOD</sub> disabled	No fault	SDOWN high, I <sub>BIAS</sub> and I <sub>MOD</sub> unaffected
MONP	No fault	SDOWN latched high, I <sub>BIAS</sub> and I <sub>MOD</sub> disabled	No fault	SDOWN high, I <sub>BIAS</sub> and I <sub>MOD</sub> unaffected
OUTPOL	No fault, polarity reverses	No fault	No fault, polarity reverses	No fault
PD	No fault, I <sub>MOD</sub> unaffected	No fault, I <sub>BIAS</sub> goes to zero	No fault, I <sub>MOD</sub> unaffected	No fault, I <sub>BIAS</sub> goes to zero
SDOWN	No fault	No fault	No fault	No fault

## PACKAGE

For the ONET4201LD, a small-footprint, 4-mm x 4-mm, 24-lead QFN package is used, with a lead pitch of 0,5 mm. The pinout is shown in [Figure 3](#).

In order to achieve the required low thermal resistance of about 38 K/W, which keeps the maximum junction temperature below 115°C, a good thermal connection of the exposed die pad is mandatory.



P0024-03

Figure 3. Pinout of the ONET4201LD in a 4-mm x 4-mm, 24-Lead QFN Package (Top View)

### TERMINAL FUNCTIONS

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
APCSET	23	Analog-in	Set photodiode reference current with resistor to GND.
BIAS	13	Analog-out	Laser diode bias current sink. Connect to laser cathode.
CAPC	20	Analog	APC loop capacitor
DIN+	3	CML-in	Noninverted data input. On-chip, 50-Ω terminated to VCC.
DIN-	4	CML-in	Inverted data input. On-chip, 50-Ω terminated to VCC.
DISABLE	24	LVTTL-in	Disable modulation and bias current outputs.
FLTMODE	10	CMOS-in	Fault mode selection input. If a low level is applied to this pin, any fault event is latched and the bias and modulation currents are disabled in a fault condition. Toggling of DISABLE or VCC resets the fault condition. If pin is set to a high level, fault events are flagged at the SDOWN output but not latched. The bias and modulation currents are not disabled. SDOWN is reset once the fault condition disappears.
GND	1, 6, 18, EP	Supply	Circuit ground. The exposed die pad (EP) must be grounded.
IBMAX	21	Analog-in	Set maximum laser diode current with resistor to GND.
MOD+	15	Analog-out	Laser modulation current output. Connect to laser cathode. Avoid usage of vias on board.
MOD-	16	Analog-out	Complementary laser modulation current output. Connect to VCC adjacent to anode of laser diode. Avoid usage of vias on board.
MODSET	11	Analog-in	Set temperature-independent modulation current with resistor to GND.
MODTC	12	Analog-in	Set modulation-current temperature compensation with resistor to GND.
MONB	8	Analog-out	Bias current monitor sources 1/68 of the bias current
MONP	7	Analog-out	Photodiode current monitor sources a current identical to the photodiode current
OUTPOL	22	LVTTL-in	Alters modulation current output polarity. Open or high: normal polarity, low: inverted polarity. OUTPOL is pulled up internally. Normal polarity: when DIN+ is high, current is sunk into MOD+.
PD	19	Analog-in	Monitor photodiode input. Connect to photodiode anode for APC. Sinks the photodiode current to GND.
SDOWN	9	LVTTL-out	Fault detection flag
VCC	2, 5, 14, 17	Supply	3.3 V ±10% supply voltage

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		VALUE	UNIT
V <sub>CC</sub>	Supply voltage <sup>(2)</sup>	–0.3 to 4	V
I <sub>BIAS</sub>	Current into BIAS	–20 to 120	mA
I <sub>IMOD+</sub> , I <sub>IMOD–</sub>	Current into MOD+, MOD–	–20 to 120	mA
I <sub>PD</sub>	Current into PD	–5 to 5	mA
V <sub>DIN+</sub> , V <sub>DIN–</sub> , V <sub>DISABLE</sub> , V <sub>MONB</sub> , V <sub>MONP</sub> , V <sub>FLTMODE</sub> , V <sub>SDOWN</sub>	Voltage at DIN+, DIN–, DISABLE, MONB, MONP, FLTMODE, SDOWN <sup>(2)</sup>	–0.3 to 4	V
V <sub>CAPC</sub> , V <sub>IBMAX</sub> , V <sub>MODSET</sub> , V <sub>APCSET</sub> , V <sub>MODTC</sub>	Voltage at CAPC, IBMAX, MODSET, APCSET, MODTC <sup>(2)</sup>	–0.3 to 3	V
V <sub>MOD+</sub> , V <sub>MOD–</sub>	Voltage at MOD+, MOD– <sup>(2)</sup>	0.6 to V <sub>CC</sub> +1.5	V
V <sub>BIAS</sub>	Voltage at BIAS <sup>(2)</sup>	1 to 3.5	V
ESD	ESD rating at all pins except MOD+, MOD–	2	kV (HBM)
	ESD rating at MOD+, MOD–	1	
T <sub>J,max</sub>	Maximum junction temperature	150	°C
T <sub>stg</sub>	Storage temperature range	–65 to 150	°C
T <sub>A</sub>	Characterized free-air operating temperature range	–40 to 85	°C
T <sub>LEAD</sub>	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	3	3.3	3.6	V
T <sub>A</sub>	Operating free-air temperature	–40		85	°C

## DC ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>CC</sub>	Supply voltage		3	3.3	3.6	V
I <sub>VCC</sub>	Supply current	I <sub>MOD</sub> = 30 mA, I <sub>BIAS</sub> = 20 mA (excluding I <sub>MOD</sub> , I <sub>BIAS</sub> )	32			mA
		I <sub>MOD</sub> = 60 mA, I <sub>BIAS</sub> = 100 mA (excluding I <sub>MOD</sub> , I <sub>BIAS</sub> )	55			mA
I <sub>BIAS</sub>	Bias current range		100			mA
I <sub>BIAS-OFF</sub>	Bias off-current	DISABLE = high or hard-fault mode; V <sub>BIAS</sub> ≤ 3.5 V	25			μA
	Bias overshoot	During module hot plugging. V <sub>CC</sub> turn on time must be ≤ 0.8 s	10%			
	Bias current temperature stability	APC open loop	-480	480		ppm/°C
	Bias current absolute accuracy <sup>(1)</sup>	I <sub>BIAS</sub> ≥ 1 mA	-15%	15%		
		I <sub>BIAS</sub> = 1 mA, T <sub>A</sub> = 25°C	±15%			
	Bias current monitor gain	I <sub>BIAS</sub> /I <sub>MONB</sub>	68			mA/ mA
	MONB and MONP threshold range	A fault is never detected for V <sub>MONB/P</sub> ≤ 1 V and a fault always occurs for V <sub>MONB/P</sub> ≥ 1.35 V	1	1.25	1.35	V
	PD current monitor gain	I <sub>PD</sub> /I <sub>MONP</sub>	1			mA/mA
V <sub>ID</sub>	Differential input signal		200	1600		mVp-p
	SDOWN output high voltage	I <sub>OH</sub> = 100 μA sourcing	2.4			V
	SDOWN output low voltage	I <sub>OL</sub> = 1 mA sinking	0.4			V
	DISABLE input impedance		4.7	7.4	10	kΩ
	DISABLE input high voltage		2			V
	DISABLE input low voltage		0.8			V
V <sub>PD</sub>	Monitor diode voltage		1.6			V
	Monitor diode dc current range		18	1500		μA

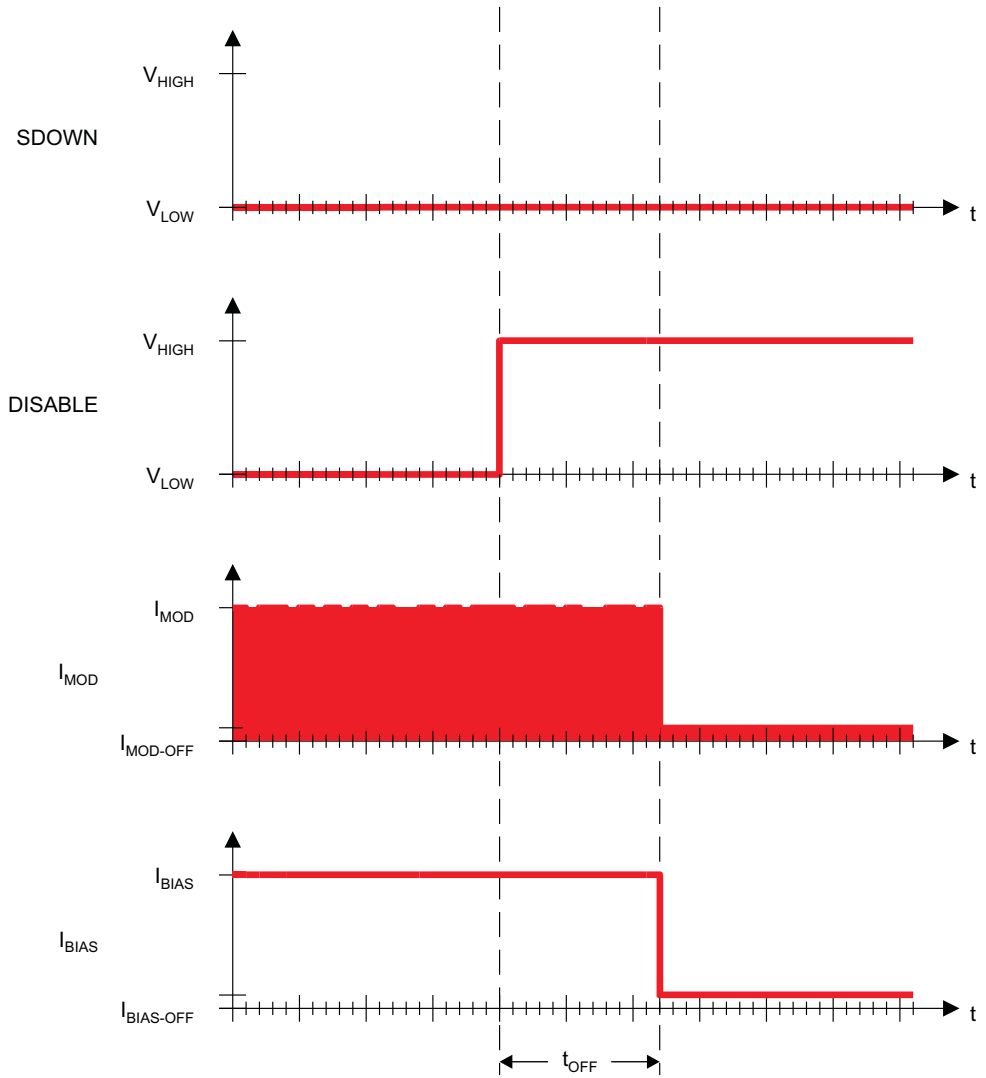
(1) Absolute accuracy refers to part-to-part variation.

### AC ELECTRICAL CHARACTERISTICS

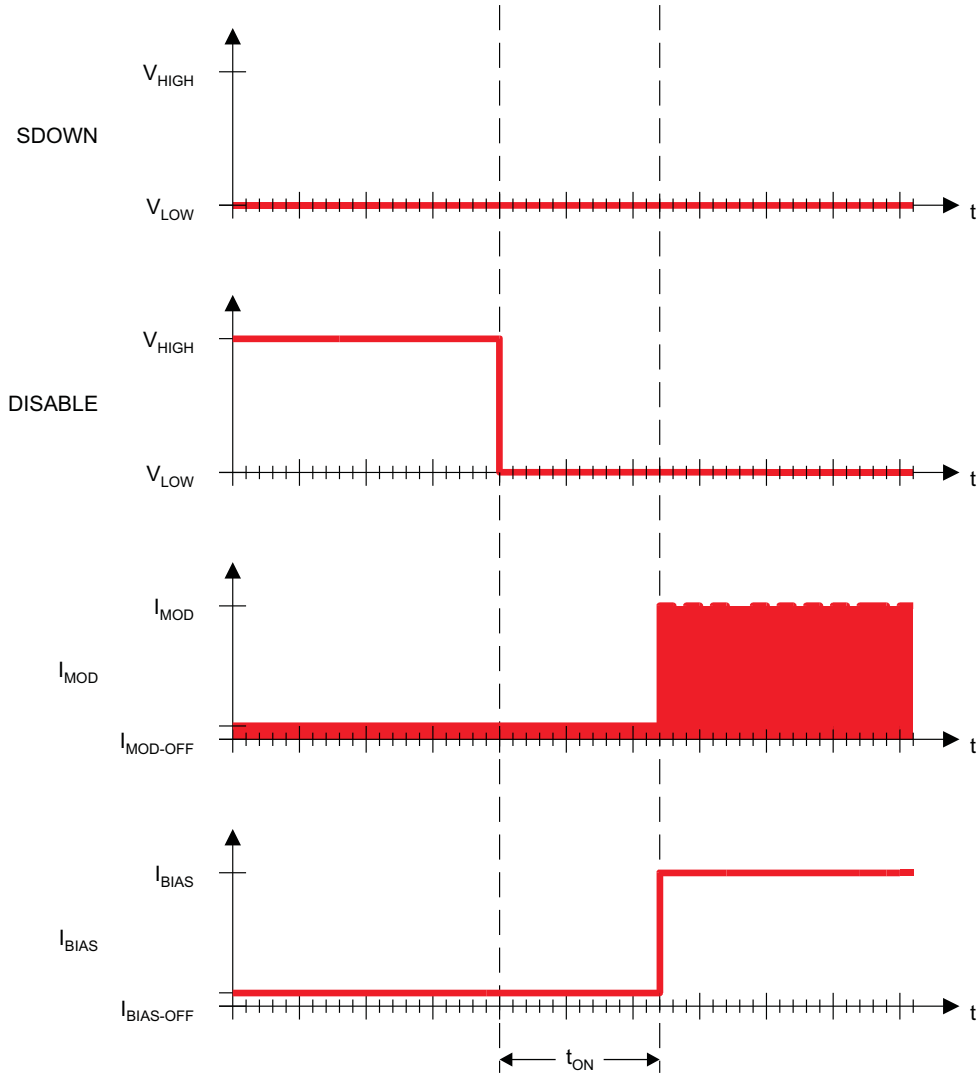
Typical operating condition is at  $V_{CC} = 3.3\text{ V}$ ,  $I_{MOD} = 30\text{ mA}$ ,  $I_{BIAS} = 20\text{ mA}$  and  $T_A = 25^\circ\text{C}$ , over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Data Rate		4.25			Gbps
$I_{MOD}$	Modulation current range	Current into MOD+/MOD- pin; $V_{MOD+}, V_{MOD-} \geq 0.6\text{ V}$	5		85	mA
$I_{MOD-OFF}$	Modulation off-current	DISABLE = high or hard-fault occurred			25	$\mu\text{A}$
	Modulation current stability		-600		600	ppm/ $^\circ\text{C}$
	Modulation current absolute accuracy <sup>(1)</sup>	$I_{MOD} = 10\text{ mA}$		$\pm 40\%$		
		$I_{MOD} = 50\text{ mA}$		$\pm 25\%$		
		$I_{MOD} = 80\text{ mA}$		$\pm 20\%$		
	Modulation current temperature compensation <sup>(2)</sup>	$R_{MODTC} = 3.125\text{ k}\Omega$		8300		ppm/ $^\circ\text{C}$
		$R_{MODTC} = \text{Open}$		630		
$t_r$	Output rise time (20% to 80%)	$V_{MOD+} \geq 1\text{ V}$ , $V_{MOD-} \geq 1\text{ V}$ , $I_{MOD} = 30\text{ mA}$		55	75	ps
$t_f$	Output fall time (20% to 80%)	$V_{MOD+} \geq 1\text{ V}$ , $V_{MOD-} \geq 1\text{ V}$ , $I_{MOD} = 30\text{ mA}$		55	75	ps
$t_{OFF}$	Disable assert time (see Figure 4)	Time from rising edge of DISABLE to when output currents fall below the maximum limits of $I_{MOD-OFF}$ and $I_{BIAS-OFF}$		0.06	5	$\mu\text{s}$
$t_{ON}$	Disable negate time (see Figure 5)	Time from falling edge of DISABLE to when output is 90% of nominal		80		$\mu\text{s}$
$t_{INIT}$	Time to initialize	From power on or negation of SDOWN using DISABLE		80		$\mu\text{s}$
$t_{FAULT}$	Fault assert time	Time from fault to SDOWN rising edge		3.3	50	$\mu\text{s}$
$t_{RESET}$	DISABLE reset (see Figure 6)	Maximum spike pulse length at DISABLE being ignored			0.8	$\mu\text{s}$
		Time DISABLE must be high to reset SDOWN			6	$\mu\text{s}$
	Output overshoot/undershoot		-13.5%		13.5%	
	Random jitter	$I_{MOD} = 60\text{ mA}$		0.6	0.9	ps <sub>RMS</sub>
DJ	Deterministic jitter <sup>(3)</sup>	$10\text{ mA} \leq I_{MOD} \leq 60\text{ mA}$ , with K28.5 pattern at 4.25 Gbps		15	30	ps <sub>p-p</sub>
		$10\text{ mA} \leq I_{MOD} \leq 60\text{ mA}$ , with $2^{23} - 1$ PRBS or equivalent pattern at 2.67 Gbps		13	32	ps <sub>p-p</sub>
		K28.5 pattern at 1.06 Gbps		5		ps <sub>p-p</sub>
		$2^{23} - 1$ PRBS or equivalent pattern at 155 Mbps		10		ps <sub>p-p</sub>

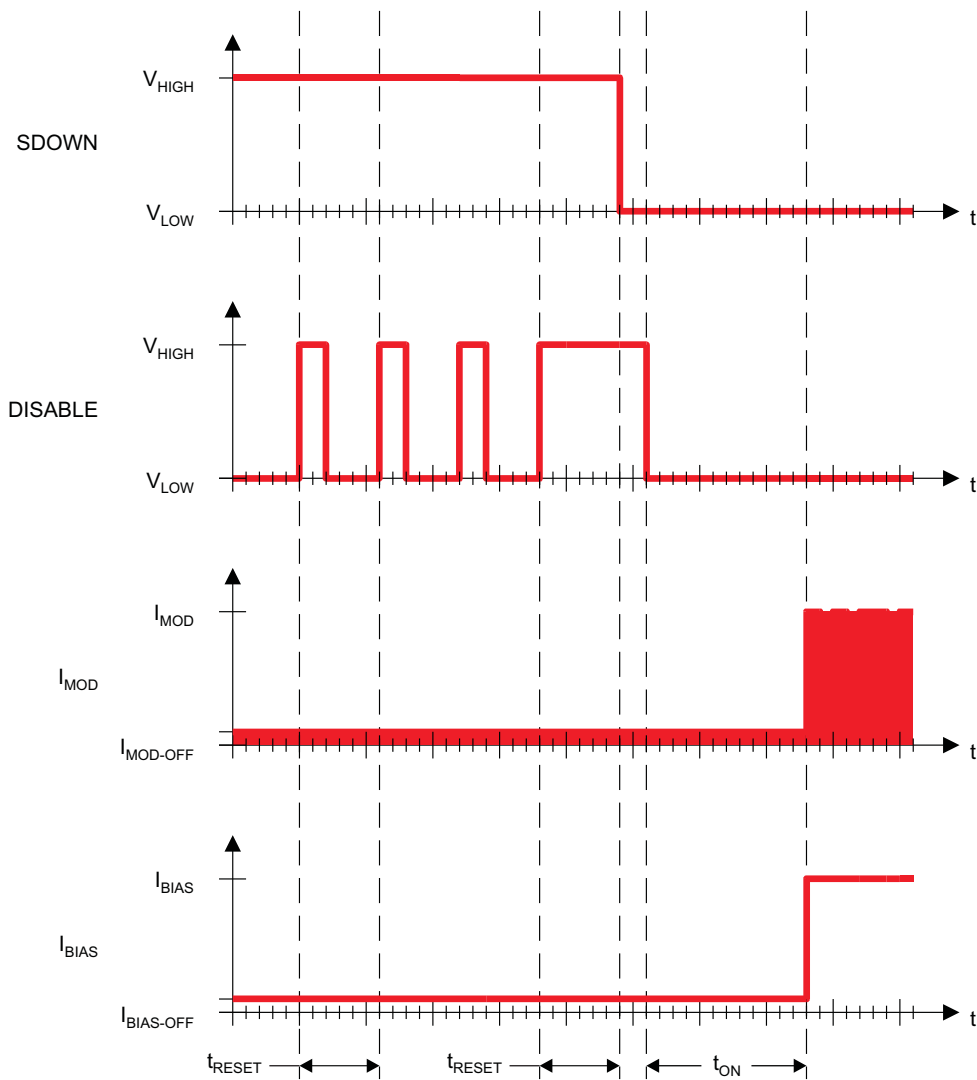
- (1) Absolute accuracy refers to part-to-part variation.
- (2) For a given external resistor connected to the MODTC pin, the modulation current temperature compensation will vary due to part-to-part variations.
- (3) Jitter measured at positive edge and negative edge crossing of eye diagram.



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T0103-01

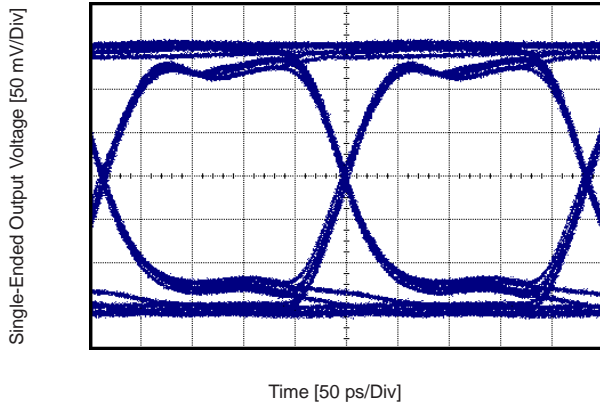


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**TYPICAL CHARACTERISTICS**

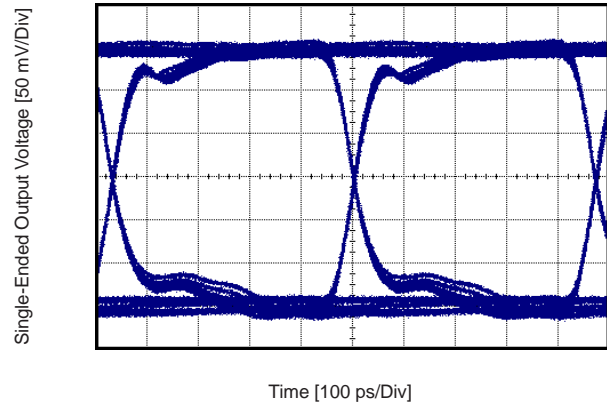
Typical operating condition is at  $V_{CC} = 3.3\text{ V}$ ,  $I_{MOD} = 30\text{ mA}$ ,  $I_{BIAS} = 20\text{ mA}$  and  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

**ELECTRICAL EYE-DIAGRAM AT 4.25 Gbps  
WITH K28.5 PATTERN,  $I_{MOD} = 30\text{ mA}$**



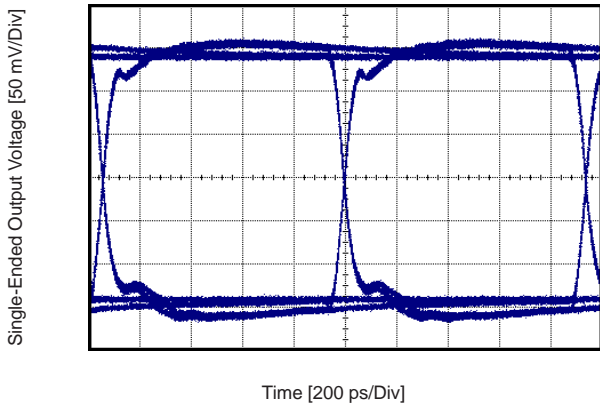
Time [50 ps/Div] G001  
**Figure 7.**

**ELECTRICAL EYE-DIAGRAM AT 2.125 Gbps  
WITH K28.5 PATTERN,  $I_{MOD} = 30\text{ mA}$**



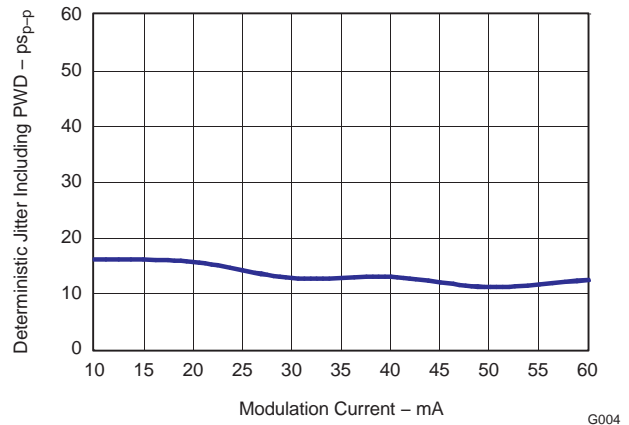
Time [100 ps/Div] G002  
**Figure 8.**

**ELECTRICAL EYE-DIAGRAM AT 1.0625 Gbps  
WITH K28.5 PATTERN,  $I_{MOD} = 30\text{ mA}$**



Time [200 ps/Div] G003  
**Figure 9.**

**DETERMINISTIC JITTER  
vs  
MODULATION CURRENT**



**Figure 10.**

**TYPICAL CHARACTERISTICS (continued)**

Typical operating condition is at  $V_{CC} = 3.3\text{ V}$ ,  $I_{MOD} = 30\text{ mA}$ ,  $I_{BIAS} = 20\text{ mA}$  and  $T_A = 25^\circ\text{C}$  (unless otherwise noted)



Figure 11.

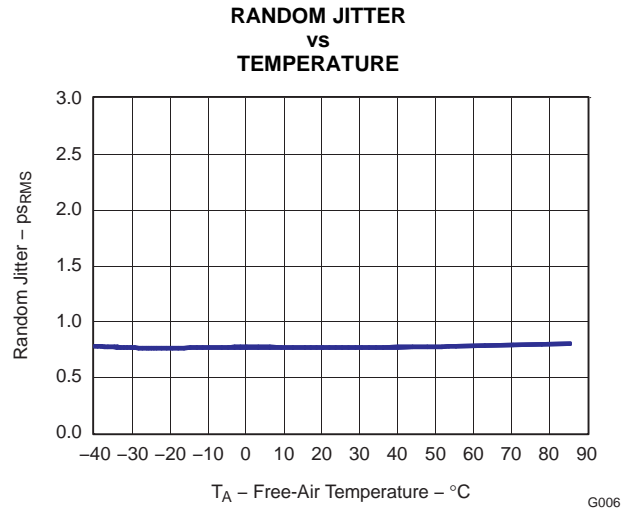


Figure 12.

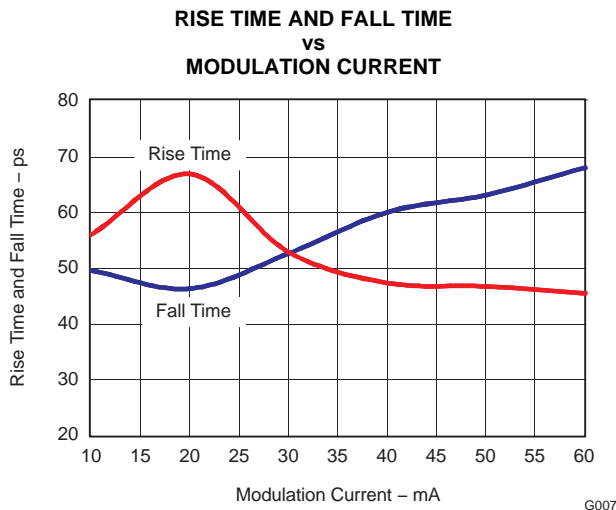


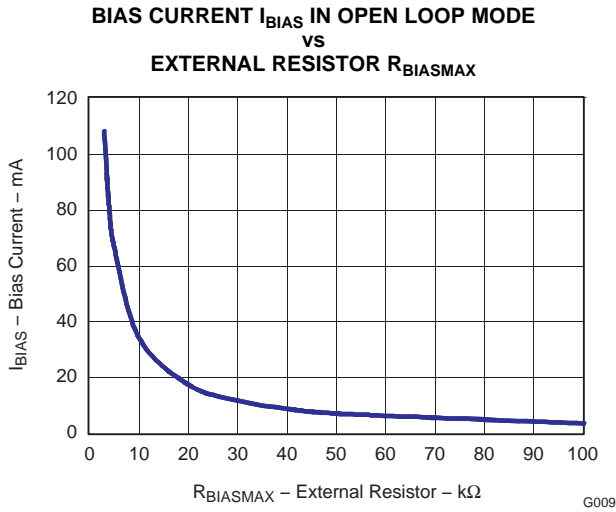
Figure 13.



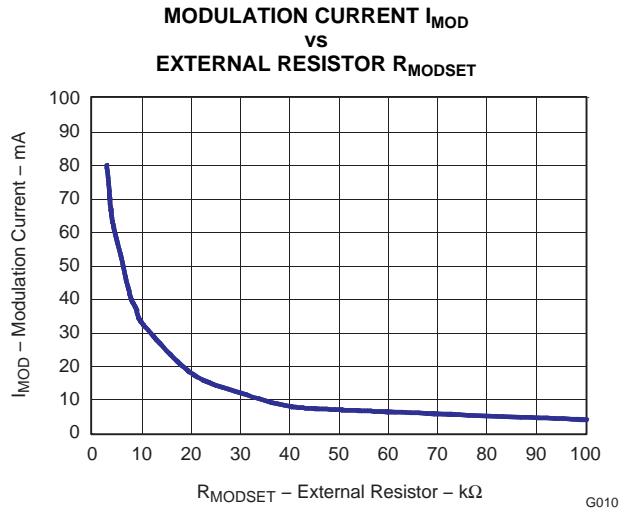
Figure 14.

**TYPICAL CHARACTERISTICS (continued)**

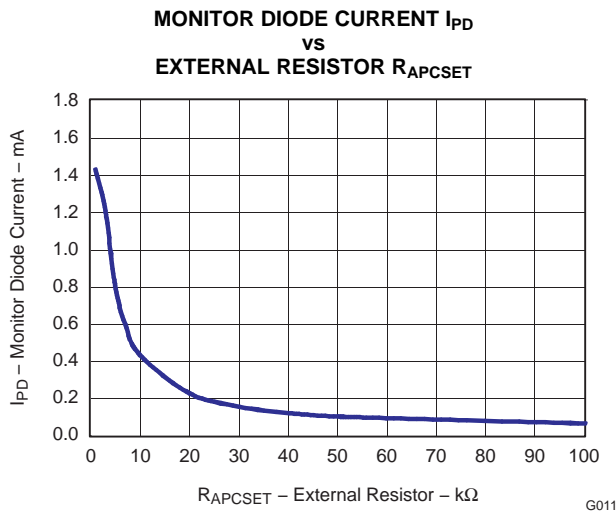
Typical operating condition is at  $V_{CC} = 3.3\text{ V}$ ,  $I_{MOD} = 30\text{ mA}$ ,  $I_{BIAS} = 20\text{ mA}$  and  $T_A = 25^\circ\text{C}$  (unless otherwise noted)



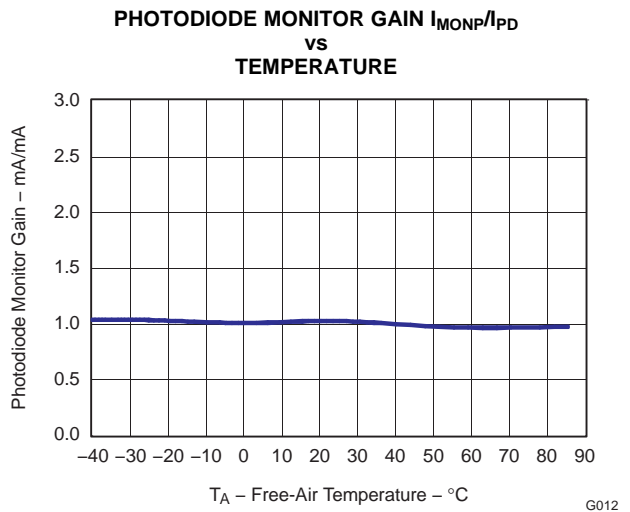
**Figure 15.**



**Figure 16.**



**Figure 17.**



**Figure 18.**

**TYPICAL CHARACTERISTICS (continued)**

Typical operating condition is at  $V_{CC} = 3.3\text{ V}$ ,  $I_{MOD} = 30\text{ mA}$ ,  $I_{BIAS} = 20\text{ mA}$  and  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

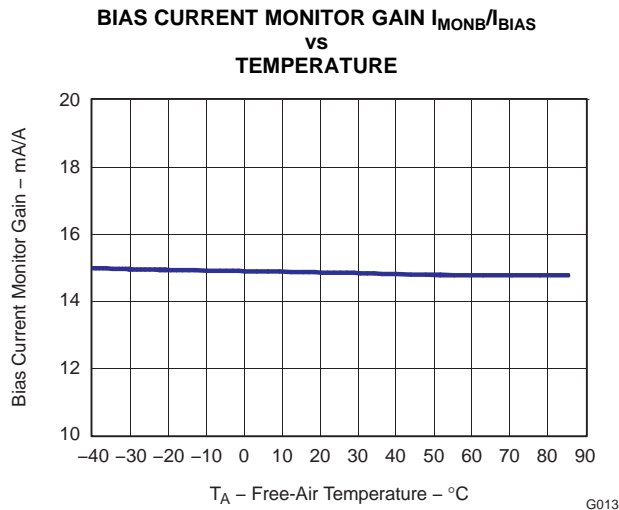


Figure 19.

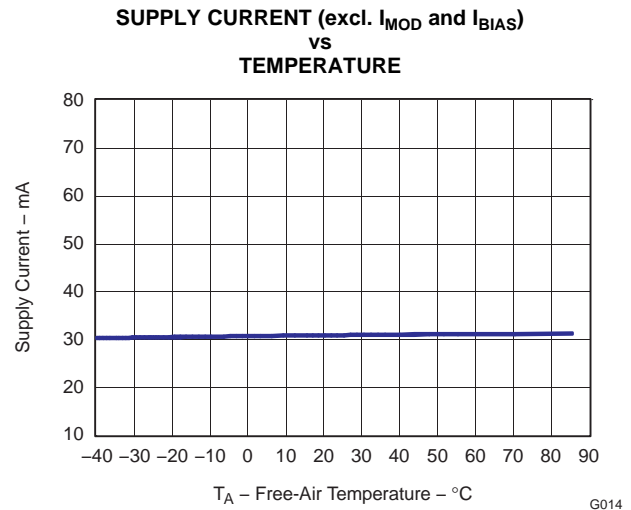


Figure 20.

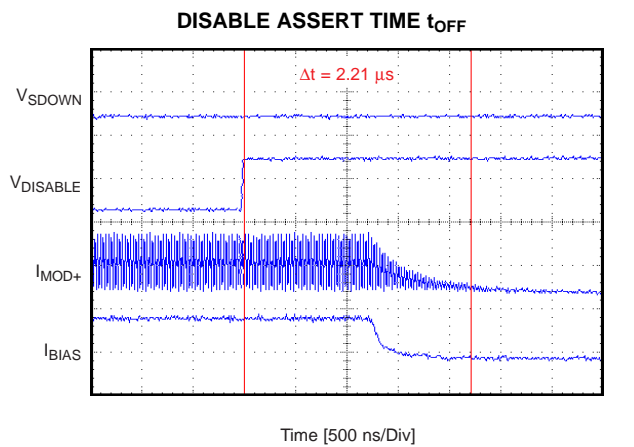


Figure 21.

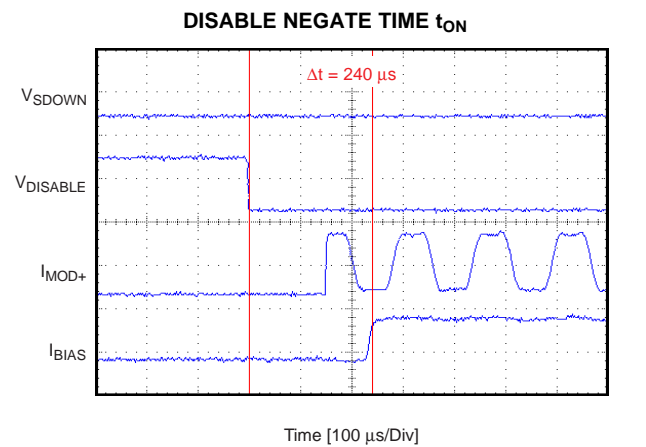


Figure 22.

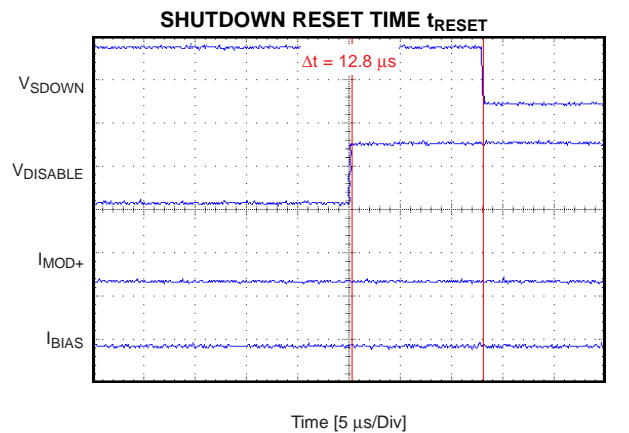
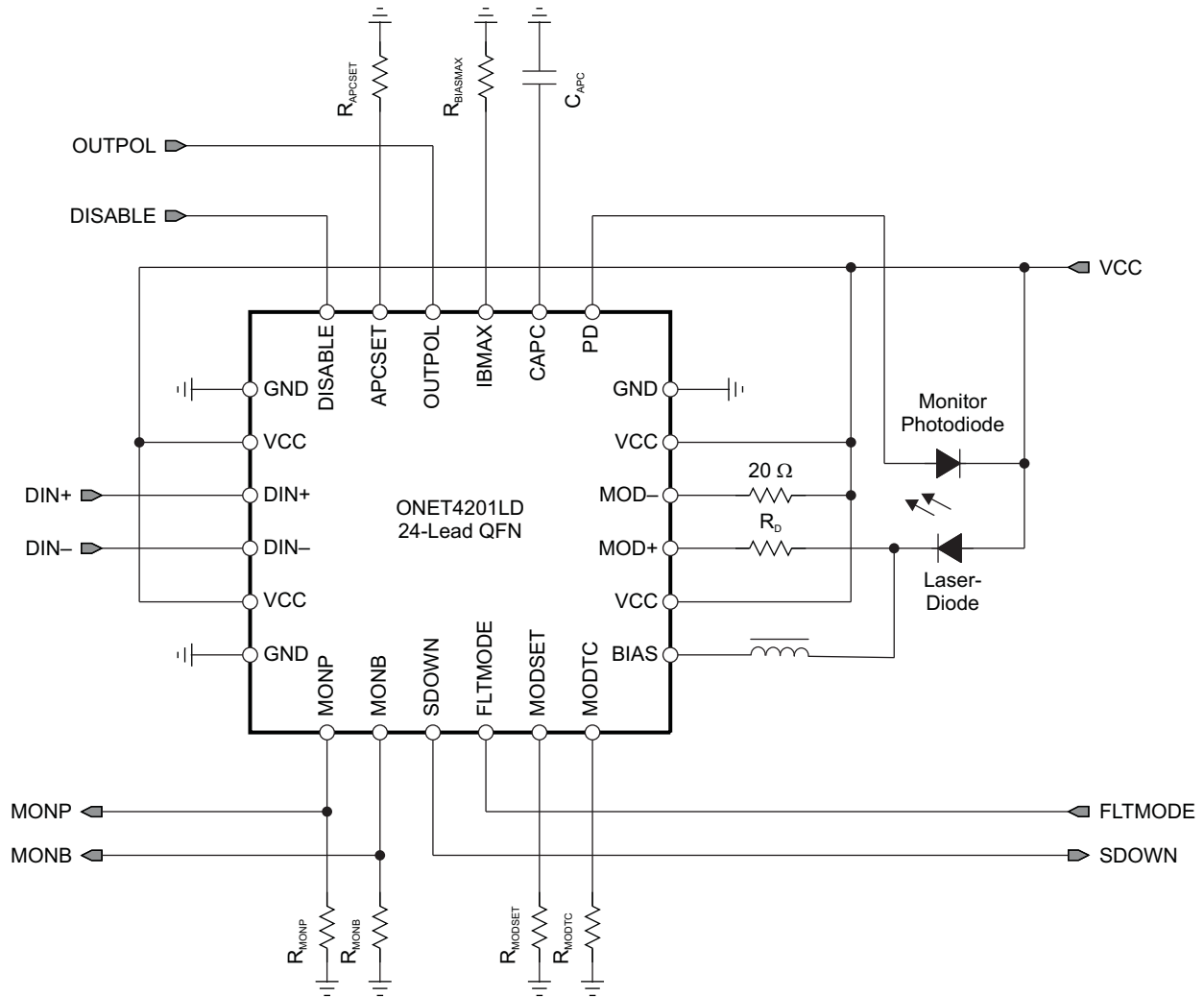


Figure 23.

APPLICATION INFORMATION

Figure 24 shows the ONET4201LD connected with a dc-coupled interface to the laser diode, alternatively the ONET4201LD laser driver can be ac-coupled.



S0154-02

Figure 24. Basic Application Circuit With DC-Coupled Interface Between the ONET4201LD and the Laser Diode

APC loop instability may occur with large inductive loading on the BIAS pin. To ensure loop stability in this case, it is recommended to connect a 1-nF capacitor to ground at the BIAS pin.

## SELECT A LASER

In the design example according to [Figure 24](#), the ONET4201LD is dc coupled to a typical communication-grade laser diode capable of operating at 4.25 Gbps with the specifications shown in [Table 2](#).

**Table 2. Laser Diode Specifications**

PARAMETER		VALUE	UNITS
$\lambda$	Wavelength	1310	nm
$P_{AVG}$	Average optical output power	5	mW
$I_{TH}$	Threshold current	10	mA
$\rho_{MON}$	Laser-to-monitor transfer	0.05	mA/mW
$\eta$	Laser slope efficiency	0.2	mW/mA

## SELECT APCSET RESISTOR

When the APC loop is activated, the desired average optical output power  $P_{AVG}$  is defined by characteristics of the monitor diode and by the APCSET resistor  $R_{APCSET}$ . The relation between the monitor photodiode current  $I_{PD}$  and the average optical output power  $P_{AVG}$  is given by [Equation 7](#):

$$I_{PD} [A] = P_{AVG} [W] \times \rho_{MON} [A/W] \quad (7)$$

The  $R_{APCSET}$  resistor is calculated by [Equation 8](#):

$$R_{APCSET} [\Omega] = \frac{4.69 \text{ V}}{I_{PD} [A]} = \frac{4.69 \text{ V}}{P_{AVG} [W] \times \rho_{MON} [A/W]} \quad (8)$$

For the laser diode specified in [Table 2](#) and the desired average optical output power of 5 mW,  $R_{APCSET}$  is calculated as seen in [Equation 9](#):

$$R_{APCSET} [\Omega] = \frac{4.69 \text{ V}}{P_{AVG} [W] \times \rho_{MON} [A/W]} = \frac{4.69 \text{ V}}{5 \text{ mW} \times 0.05 \text{ mA/mW}} = 18.75 \text{ k}\Omega \quad (9)$$

Note that the monitor photodiode current  $I_{PD}$  must not exceed 1.5 mA corresponding to a minimum APCSET resistor  $R_{APCSET,MIN} = 3.1 \text{ k}\Omega$ .

## SELECT MODSET RESISTOR

Modulation current  $I_{MOD}$  is dependent on the required optical output peak-to-peak power  $P_{p-p}$  or the average optical power  $P_{AVG}$ .  $I_{MOD}$  can be calculated using the laser slope efficiency  $\eta$  and the desired extinction ratio  $r_e$ :

$$I_{MOD} [A] = \frac{P_{p-p} [W]}{\eta [W/A]} = \frac{2 \times P_{AVG} [W] \times \frac{r_e - 1}{r_e + 1}}{\eta [W/A]} \quad (10)$$

Using the laser diode parameters from [Table 2](#) and assuming an extinction ratio  $r_e = 8 \text{ dB}$  ( 6.3) for an average optical power  $P_{AVG} = 5 \text{ mW}$  the required modulation current results as:

$$I_{MOD} = \frac{2 \times 5 \text{ mW} \times \frac{6.3 - 1}{6.3 + 1}}{0.2 \text{ mW/mA}} = 36.3 \text{ mA} \quad (11)$$

The modulation current is adjustable with a selectable temperature coefficient TC according to the relation:

$$I_{MOD} [A] = I_{MOD0} [A] \times \left( 1 + TC \times (T [^\circ\text{C}] - T_0 [^\circ\text{C}]) \right) \quad (12)$$

where T is the ambient temperature in  $^\circ\text{C}$  and  $T_0$  is the reference temperature ( $T_0 = 60^\circ\text{C}$ ).

The temperature coefficient of the modulation current TC is typically adjustable between 630 ppm/ $^\circ\text{C}$  and 8300 ppm/ $^\circ\text{C}$ .

For calculation of the required external resistor  $R_{MODSET}$  for a given modulation current and a given temperature, the formula can be modified as follows:

$$R_{\text{MODSET}}[\Omega] = \frac{265 \text{ V}}{I_{\text{MOD}}[\text{A}]} \times \left( 1 + \text{TC} \times (T[\text{°C}] - T_0[\text{°C}]) \right) \quad (13)$$

If 4000 ppm/°C is the desired temperature coefficient and the modulation current from the example above, 36.3 mA, is required at a temperature of 25°C, the MODSET resistor  $R_{\text{MODSET}}$  is given by [Equation 14](#).

$$R_{\text{MODSET}}[\Omega] = \frac{265 \text{ V}}{36.3 \text{ mA}} \times \left( 1 + \frac{4000 \text{ ppm}}{\text{°C}} \times (25\text{°C} - 60\text{°C}) \right) = 6.3 \text{ k}\Omega \quad (14)$$

Note that the modulation current  $I_{\text{MOD}}$  must not exceed 85 mA over the complete temperature range, corresponding to a minimum MODSET resistor  $R_{\text{MODSET,MIN}} = 3.1 \text{ k}\Omega$ .

## SELECT MODTC RESISTOR

The  $R_{\text{MODTC}}$  resistor is used to program a modulation temperature coefficient that can be used to compensate for the decreased slope efficiency of the laser at a higher temperature. The temperature coefficient  $\text{TC}_{\text{LD}}$  of the laser can be calculated using the slope efficiency  $\eta_1$  at temperature  $T_1$  and  $\eta_2$  at temperature  $T_2$  as shown in [Equation 15](#):

$$\text{TC}_{\text{LD}} \left[ \frac{1}{\text{°C}} \right] = \frac{\eta_2[\text{W/A}] - \eta_1[\text{W/A}]}{\eta_1[\text{W/A}] \times (T_2[\text{°C}] - T_1[\text{°C}])} \times 10^6 \quad (15)$$

As an example, for the laser in [Table 2](#), the slope efficiency at temperature  $T_1 = 25\text{°C}$  is  $\eta_1 = 0.2 \text{ mW/mA}$ . At temperature  $T_2 = 85\text{°C}$  the slope efficiency is  $\eta_2 = 0.15 \text{ mW/mA}$ . The corresponding temperature coefficient  $\text{TC}_{\text{LD}}$  laser can be calculated:

$$\text{TC}_{\text{LD}} = \frac{0.15 \text{ mW/mA} - 0.2 \text{ mW/mA}}{0.2 \text{ mW/mA} \times (85\text{°C} - 25\text{°C})} \times 10^6 = -4167 \frac{1}{\text{°C}} \quad (16)$$

The MODTC resistor  $R_{\text{MODTC}}$  can be used to compensate the laser temperature coefficient  $\text{TC}_{\text{LD}}$  in order to maintain the same optical output swing within a range of 630 ppm up to 8300 ppm. For this,  $R_{\text{MODTC}}$  may be programmed as follows:

$$R_{\text{MODTC}} = \frac{24 \Omega}{(\text{TC} - 630 \text{ ppm}) \left[ \frac{1}{\text{°C}} \right] \times \text{°C}} \quad (17)$$

To compensate for the decreased slope efficiency of the laser in [Table 2](#),  $T_C$  must be 4167 ppm/°C.

This leads to the following MODTC resistor  $R_{\text{MODTC}}$ :

$$R_{\text{MODTC}} = \frac{24 \Omega}{\frac{4167 \text{ ppm} - 630 \text{ ppm}}{\text{°C}} \times \text{°C}} = 6.8 \text{ k}\Omega \quad (18)$$

## SELECT BIASMAX RESISTOR

The BIASMAX resistor  $R_{\text{BIASMAX}}$  is used to limit the bias current applied to the laser diode.

To calculate  $R_{\text{BIASMAX}}$ , the maximum threshold current at 85°C and end of life must be determined. The maximum bias current for the dc-coupled interface can be approximated by [Equation 19](#).

$$I_{\text{BIASMAX}}[\text{A}] = I_{\text{THMAX}}[\text{A}] \quad (19)$$

$R_{\text{BIASMAX}}$  can be set by [Equation 20](#).

$$R_{\text{BIASMAX}}[\Omega] = \frac{343 \text{ V}}{I_{\text{BIASMAX}}[\text{A}]} = \frac{343 \text{ V}}{I_{\text{THMAX}}[\text{A}]} \quad (20)$$

For the example laser diode, the maximum threshold current is 40 mA at 85°C. Therefore,  $R_{\text{BIASMAX}}$  can be approximated by [Equation 21](#).

$$R_{\text{BIASMAX}} = \frac{343 \text{ V}}{40 \text{ mA}} = 8.6 \text{ k}\Omega \quad (21)$$

### SELECT $V_{\text{MONB}}$ AND $V_{\text{MONP}}$ RANGE

Monitoring the bias current is achieved by taking the fractional (1/68) bias current and developing a voltage across an external resistor to ground. [Equation 22](#) provides the value for  $V_{\text{MONB}}$  for a resistor value equal to 768  $\Omega$ .

$$V_{\text{MONB}}[\text{V}] = \frac{R_{\text{MONB}}[\Omega] \times I_{\text{BIAS}}[\text{A}]}{68} = \frac{768 \Omega \times I_{\text{BIAS}}[\text{A}]}{68} = 11.29 \Omega \times I_{\text{BIAS}}[\text{A}] \quad (22)$$

Monitoring of the photodiode current is achieved by taking a mirror of  $I_{\text{PD}}$  and developing a voltage across an external resistor to ground. [Equation 23](#) provides the value for  $V_{\text{MONP}}$  for a resistor equal to 200  $\Omega$ .

$$V_{\text{MONP}}[\text{V}] = R_{\text{MONP}}[\Omega] \times I_{\text{PD}}[\text{A}] = 200 \Omega \times I_{\text{PD}}[\text{A}] \quad (23)$$

### LASER DIODE INTERFACE

The output stage of the ONET4201LD is optimized for driving a 20- $\Omega$  load. The combination of a damping resistor,  $R_{\text{D}}$ , along with the resistance of the laser diode must be 20  $\Omega$  for impedance matching. The suggested typical value for  $R_{\text{D}}$  is 6  $\Omega$  to 15  $\Omega$ . A bypass capacitor of 10 nF placed close to the laser anode also helps to optimize performance.

## REVISION HISTORY

Changes from Original (November 2005) to Revision A	Page
• Changed 200us to 80us for typ value of $t_{ON}$ .....	10
• Changed 200us to 80us for typ value of $t_{INIT}$ .....	10
• Changed 10us to 0.8us for max value of $t_{RESET}$ max spike .....	10
• Changed 20us min to 6us max value of $t_{RESET}$ time DISABLE .....	10

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ONET4201LDRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ONET 4201L	<a href="#">Samples</a>
ONET4201LDRGERG4	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ONET 4201L	<a href="#">Samples</a>
ONET4201LDRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ONET 4201L	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ONET4201LDRGER	VQFN	RGE	24	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
ONET4201LDRGET	VQFN	RGE	24	250	180.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

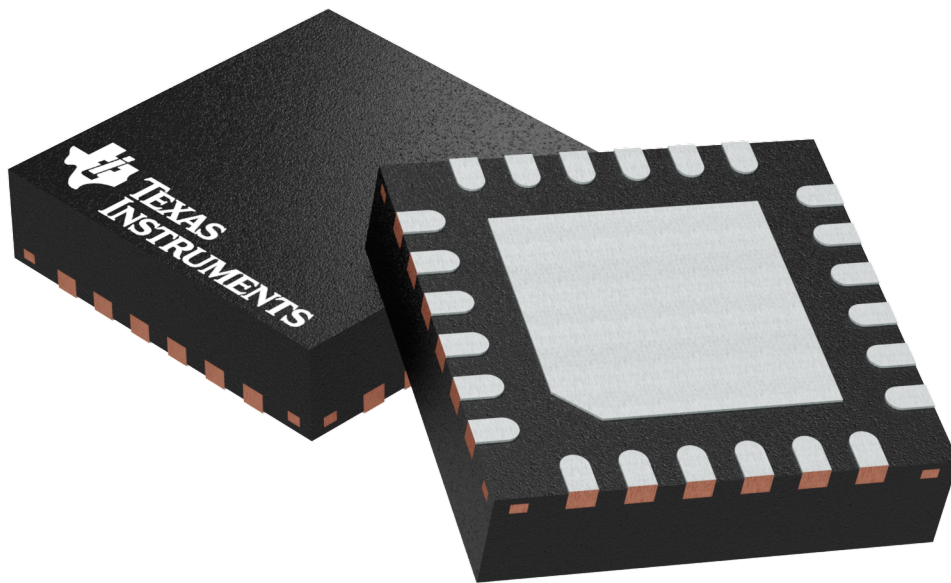
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ONET4201LDRGER	VQFN	RGE	24	3000	350.0	350.0	43.0
ONET4201LDRGET	VQFN	RGE	24	250	210.0	185.0	35.0

**RGE 24**

**GENERIC PACKAGE VIEW**

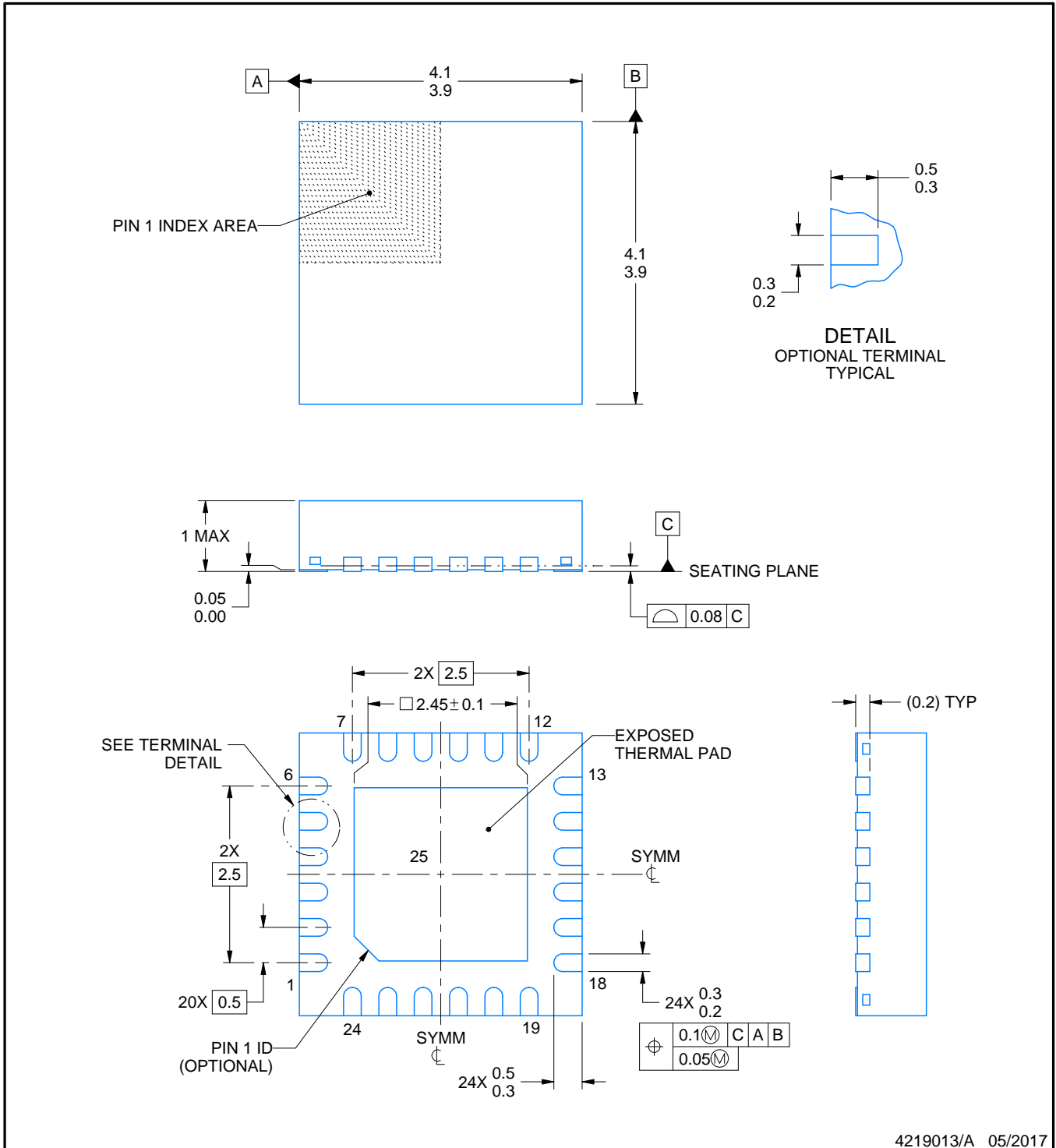
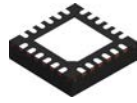
**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4204104/H



4219013/A 05/2017

NOTES:

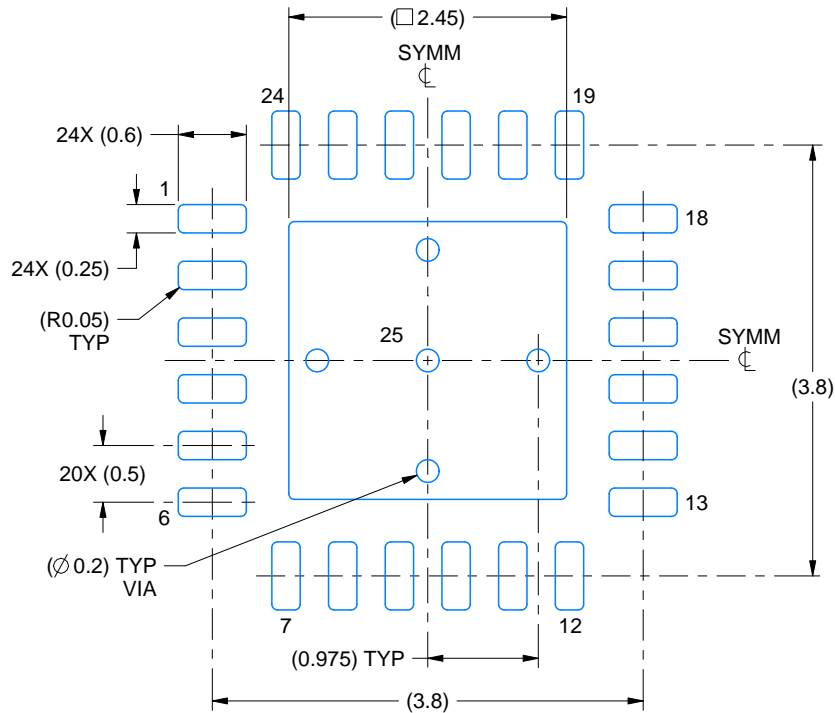
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

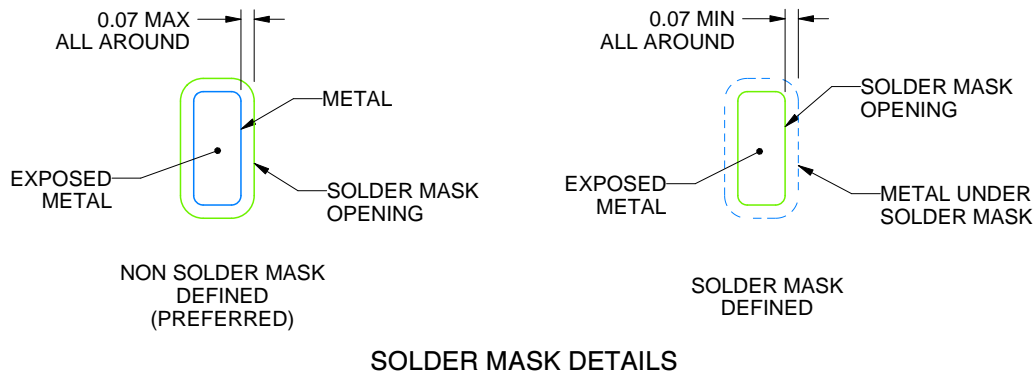
RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

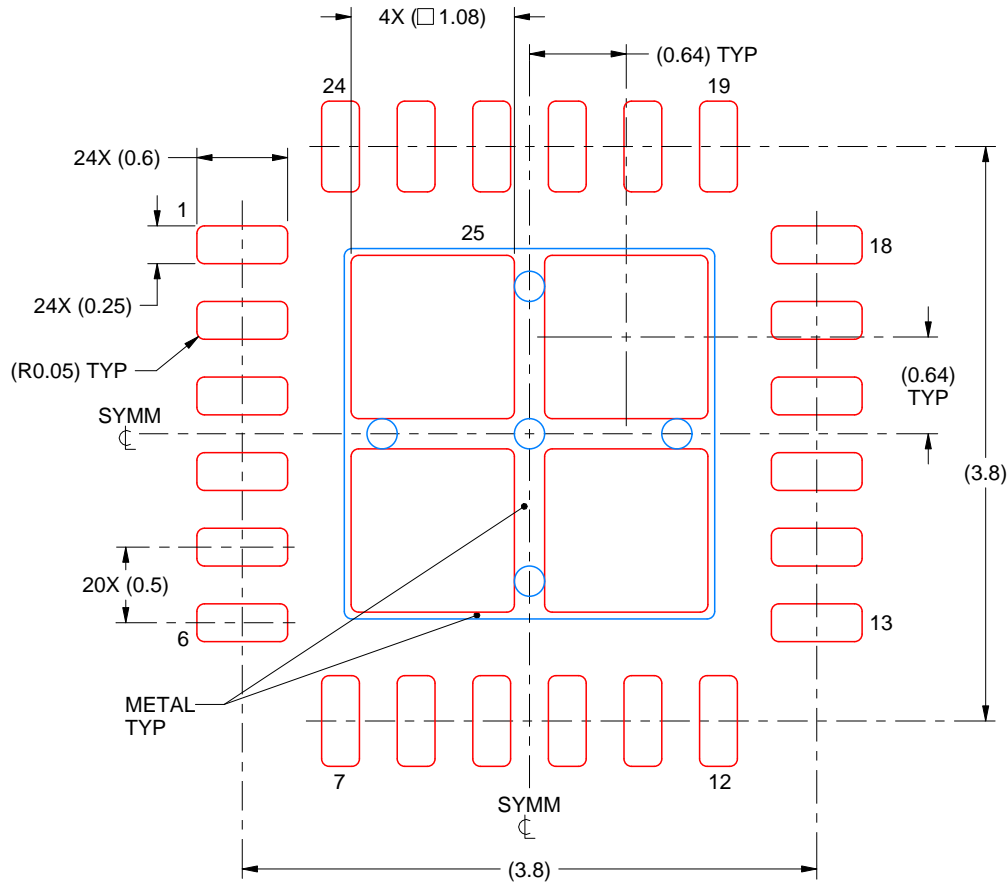
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sl原因271](http://www.ti.com/lit/sl原因271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25  
 78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
 SCALE:20X

4219013/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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