THE DATASHEET OF

ONET1101LRGET

11.3 Gbps Laser Diode Driver

FEATURES

- **Up to 11.3 Gbps Operation**
- **Two-Wire Digital Interface**
- **Digitally Selectable Modulation Current up to 80 mA**
- **Digitally Selectable Bias Current up to 100 mA Source or Sink**
- **Automatic Power Control (APC) Loop**
- **Supports Transceiver Management System (TMS)**
- **Programmable Input Equalizer**
- **Cross-point Control**
- **Includes Laser Safety Features**
- **Adjustable Coupling Ratio**
- **Single +3.3 V Supply**
- **Case Temperature –25°C to 100°C**
- **Small Surface Mount Footprint 4mm × 4mm 24-Pin, RoHS-compliant QFN Package**

APPLICATIONS

- **10 Gigabit Ethernet Optical Transmitters**
- **8x and 10x Fibre Channel Optical Transmitters**
- **SONET OC-192/SDH STM-64 Optical Transmitters**
- **XFP and SFP+ Transceiver Modules**
- **XENPAK, XPAK, X2 and 300-pin MSA Transponder Modules**

DESCRIPTION

The ONET1101L is a high-speed, 3.3 -V laser driver designed to directly modulate a laser at data rates from 2 Gbps to 11.3 Gbps.

The device provides a two-wire serial interface that helps digital control of the modulation, plus bias currents and cross point, eliminating the need for external components. An optional input equalizer can be used for equalization of up to 300 mm (12”) of microstrip or stripline transmission line on FR4 printed circuit boards.

The ONET1101L includes an integrated automatic power control (APC) loop, plus circuitry to support laser safety and transceiver management systems.

The laser driver is characterized for operation from –25°C to 100°C case temperature and is available in a small footprint using a 4mm × 4mm, 24-pin RoHS-compliant QFN package.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

BLOCK DIAGRAM

Figure 1 shows a block diagram of the ONET1101L device. The laser driver consists of an equalizer, a limiter, an output driver, DC offset cancellation with cross point control, power-on reset circuitry, a 2-wire serial interface (including a control logic block and modulation current generator), a bias current generator and automatic power control loop, and an analog reference block.

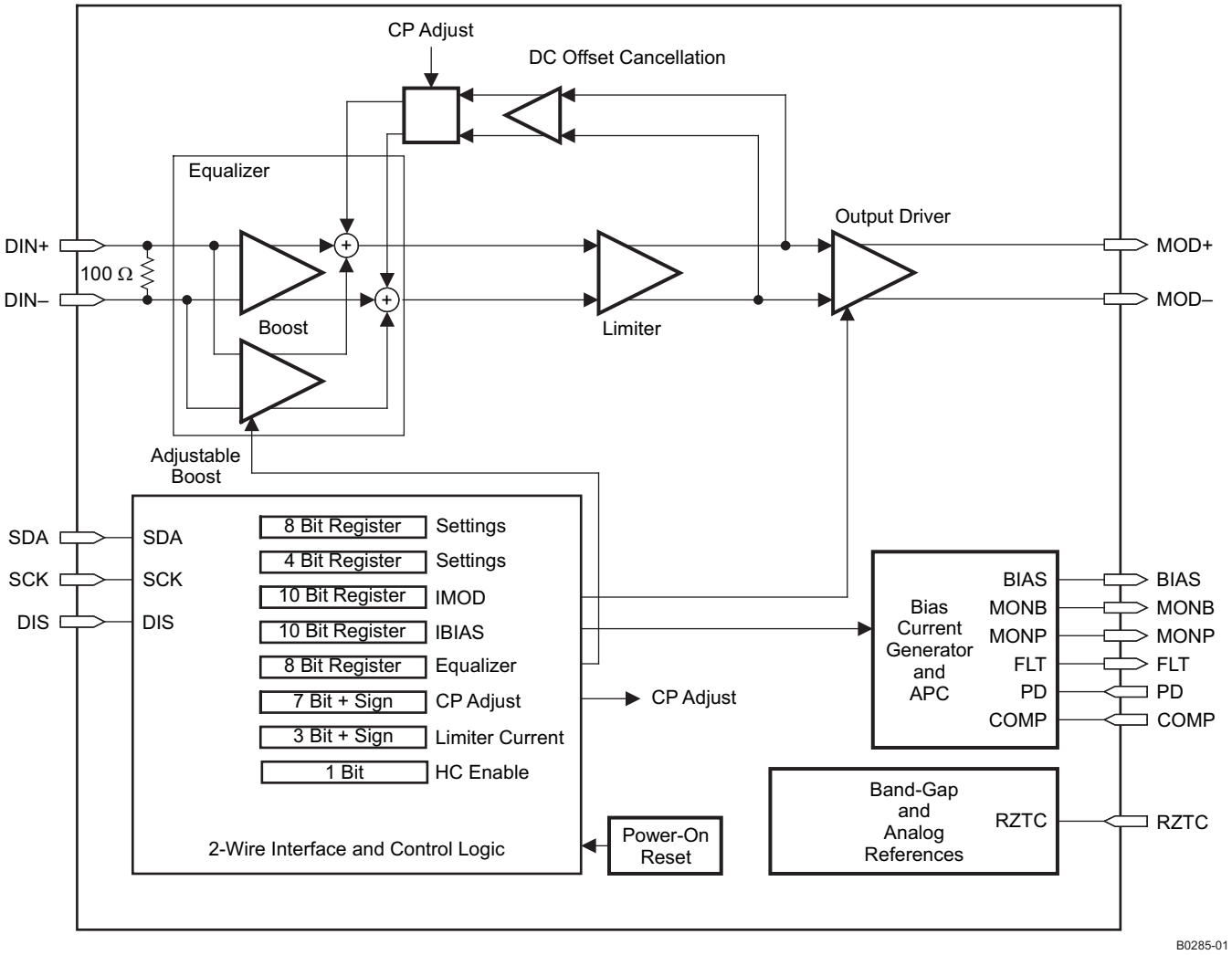
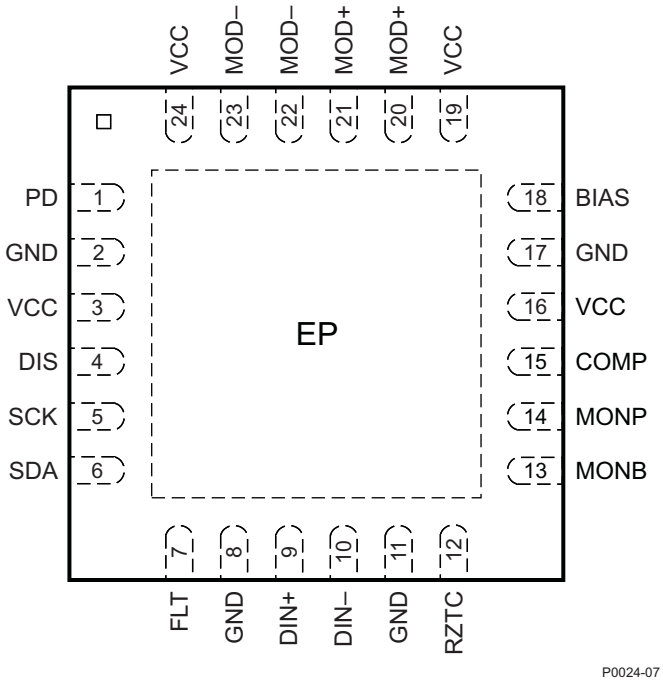


Figure 1. Block Diagram of the ONET1101L

PACKAGE

The ONET1101L is packaged in a small footprint 4mm × 4mm 24-pin, RoHS-compliant QFN package, with a lead pitch of 0.5 mm. The 24-pin QFN Package top view and pin description follow.

RGE Package
(Top View)



24-Pin QFN Package, 4mm × 4mm (Top View)

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	PD	Analog	Photodiode input. Pin can source or sink current dependent on register setting.
2, 8, 11, 17, EP	GND	Supply	Circuit ground. Exposed die pad (EP) must be grounded.
3, 16, 19, 24	VCC	Supply	3.3 V ± 10% supply voltage
4	DIS	Digital-in	Disables the bias and modulation currents when set to high state. Toggle to reset a fault condition.
5	SCK	Digital-in	2-wire interface serial clock. Connect a pull-up resistor (10 kΩ typical) to VCC.
6	SDA	Digital-in	2-wire interface serial data input. Connect a pull-up resistor (10 kΩ typical) to VCC.
7	FLT	Digital-out	Fault detection flag.
9	DIN+	Analog-in	Non-inverted data input. On-chip differentially 100 Ω terminated to DIN–. Must be AC coupled.
10	DIN–	Analog-in	Inverted data input. On-chip differentially 100 Ω terminated to DIN+. Must be AC coupled.
12	RZTC	Analog	Connect external zero TC 28.7 kΩ resistor to ground (GND). Used to generate a defined zero TC reference current for internal DACs.
13	MONB	Analog-out	Bias current monitor. Supplies a 1% replica of the bias current. Connect an external resistor to ground (GND). If the voltage at this pin exceeds 1.16 V, a fault is triggered. Choose a resistor that yields a MONB voltage of 0.8 V at the maximum desired bias current.
14	MONP	Analog-out	Photodiode current monitor. Supplies a 12.5% replica of the photodiode current when PDRNG = 1X, a 25% replica when PDRNG = 01 and a 50% replica when PDRNG = 00. Connect an external resistor (5 kΩ typical) to ground (GND).
15	COMP	Analog	Compensation pin used to control the bandwidth of the automatic power control (APC) loop. Connect a 0.01 µF capacitor to ground.
18	BIAS	Analog	Sinks or sources average bias current for laser in both APC and open loop modes.
20, 21	MOD+	CML-out	Non-inverted modulation current output. IMOD flows into this pin when input data is high (current).
22, 23	MOD–	CML-out	Inverted modulation current output. IMOD flows into this pin when input data is low (current).

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
V_{CC}	Supply voltage(2)	–0.3 to 4.0	V
V_{DIS}, V_{RZTC}, V_{SCK}, V_{SDA}, V_{FLT}, V_{MONB}, V_{MONP}, V_{COMP}, V_{PD}, V_{BIAS}	Voltage at DIS, RZTC, SCK, SDA, DIN+, DIN–, FLT, MONB, MONP, COMP, PD, BIAS, MOD+, MOD– (2)	–0.3 to 4.0	V
IDIN–, IDIN+	Maximum current at input pins	25	mA
IMOD+, IMOD–	Maximum current at output pins	120	mA
ESD	ESD rating at all pins	2	kV (HBM)
$T_{J,max}$	Maximum junction temperature	125	°C
T_{STG}	Storage temperature range	–65 to 150	°C
T_C	Case Temperature	–40 to 110	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Device exposure to conditions outside the Absolute Maximum Ratings ranges for an extended duration can affect device reliability.
(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2.97	3.3	3.63	V
V_{IH}	Digital input high voltage	DIS, SCK, SDA	2.0			V
V_{IL}	Digital input low voltage	DIS, SCK, SDA			0.8	V
	Photodiode current range	Control bit PDRNG = 1X, step size = 3 µA		3080		µA
		Control bit PDRNG = 01, step size = 1.5 µA		1540		
		Control bit PDRNG = 00, step size = 0.75 µA		770		
R_{RZTC}	Zero TC resistor value(1)	1.16 V bandgap bias across resistor, E96, 1% accuracy	28.4	28.7	29	kΩ
V_{IN}	Differential input voltage swing	EQENA = 0	100		1200	mV_{p-p}
t_{R-IN}	Input rise time	20% to 80%		30	55	ps
t_{F-IN}	Input fall time	20% to 80%		30	55	ps
T_C	Case Temperature		–25		100	°C

(1) Changing the value alters the DAC ranges.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions with a 25 Ω output load, open loop operation, I_{MOD} = 40 mA, I_{BIAS} = 40 mA, and R_{RZTC} = 28.7 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		2.97	3.3	3.63	V
I_{VCC}	Supply current	I_{MOD} = 40 mA, I_{BIAS}= 40 mA, excluding I_{MOD} and I_{BIAS}, EQENA = 0		66	85	mA
		I_{MOD} = 80 mA, I_{BIAS} = 80 mA, excluding I_{MOD} and I_{BIAS}, EQENA = 0		95	118	
		I_{MOD} = 40 mA, I_{BIAS} = 40 mA, excluding I_{MOD} and I_{BIAS}, EQENA = 1		73	95	
		Output off (DIS = HIGH), I_{MOD} = 40 mA, I_{BIAS} = 40 mA, EQENA = 0		42		
R_{IN}	Data input resistance	Differential between DIN+ / DIN–	80	100	120	Ω
	Digital input current	SCK, SDA, pull up to VCC	–10		10	µA
		DIS, pull down to GND	–10		10	µA
V_{OH}	Digital output high voltage	FLT, pull-up to V_{CC}, I_{SOURCE} = 50 µA	2.4			V
V_{OL}	Digital output low voltage	FLT, pull-up to V_{CC}, I_{SINK} = 350 µA			0.4	V
$I_{BIAS-MIN}$	Minimum bias current	See table note (1)			5	mA
$I_{BIAS-MAX}$	Maximum bias current	Sink, BIASPOL = 0 DAC set to maximum, open and closed loop	85	100		mA
		Source, BIASPOL = 1 DAC set to maximum, open and closed loop	80	100		
$I_{BIAS-DIS}$	Bias current during disable				100	µA
	Bias pin compliance voltage	BIASPOL = 0	0.8			V
		BIASPOL = 1			V_{CC}–0.8	
V_{PD}	Photodiode reverse bias voltage	APC active, I_{PD} = max	1.3	2.3		V
	Photodiode fault current level	Percent of target I_{PD} (2)		150%		
	Photodiode current monitor ratio	I_{MONP} / I_{PD} with control bit PDRNG = 1X	10%	12.5%	15%	
		I_{MONP} / I_{PD} with control bit PDRNG = 01	20%	25%	30%	
		I_{MONP} / I_{PD} with control bit PDRNG = 00	40%	50%	60%	
	Bias current monitor ratio	I_{MONB} / I_{BIAS} (nominal 1/100 = 1%)	0.9%	1.0%	1.2%	
V_{CC-RST}	V_{CC} reset threshold voltage	V_{CC} voltage level which triggers power-on reset		2.5	2.8	V
$V_{CC-RSTHYS}$	V_{CC} reset threshold voltage	Hysteresis		100		mV
$V_{MONB-FLT}$	Fault voltage at MONB	Fault occurs if voltage at MONB exceeds value	1.1	1.16	1.22	V

(1) The bias current can be set below the specified minimum according to the corresponding register setting; however in closed loop operation settings below the specified value the bias current can trigger a fault.
(2) Assured by simulation over process, supply, and temperature variation.

AC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions with 25 Ω output load, open loop operation, I_{MOD} = 40 mA, I_{BIAS} = 40 mA, and R_{RZTC} = 28.7 kΩ. Typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SDD11	Differential input return gain	0.01 GHz < f < 3.9 GHz		–16		dB
		3.9 GHz < f < 12.1 GHz		See note (1)		
SCD11	Differential to common mode conversion gain	f < 8.25 GHz		–45		dB
		8.25 GHz < f < 20 GHz		–35		
t_{R-OUT}	Output rise time	20% to 80%, t_{R-IN} < 40 ps, 25 Ω load, single-ended		25	35	ps
t_{F-OUT}	Output fall time	20% to 80%, t_{F-IN} < 40 ps, 25 Ω load, single-ended		25	35	ps
$I_{MOD-MIN}$	Minimum modulation current				10	mA
$I_{MOD-MAX}$	Maximum modulation current	AC Coupled Outputs	70	85		mA
$I_{MOD-STEP}$	Modulation current step size	10 Bit Register		83		µA
DJ	Deterministic output jitter	EQENA = 0, K28.5 pattern at 11.3 Gbps, 100 mVpp, 600 mVpp, 1200 mVpp differential input voltage		5	10	ps_{p-p}
		EQENA = 1, K28.5 pattern at 11.3 Gbps, maximum equalization with 12” transmission line at the input, 400 mVpp at input to transmission line		7		
RJ	Random output jitter			0.4	0.8	ps_{RMS}
τ_{APC}	APC time constant	C_{APC} = 0.01 µF, I_{PD} = 100 µA, PD coupling ratio, CR = 40 (2)		120		µs
	Cross Point Control Range		30%		70%	
T_{OFF}	Transmitter disable time	Rising edge of DIS to $I_{BIAS} \le 0.1 \times I_{BIAS-NOMINAL}$ (2)		0.05	5	µs
T_{ON}	Disable negate time	Falling edge of DIS to $I_{BIAS} \ge 0.9 \times I_{BIAS-NOMINAL}$ (2)			1	ms
T_{INIT1}	Power-on to initialize	Power-on to registers ready to be loaded		1	10	ms
T_{INIT2}	Initialize to transmit	Register load STOP command to part ready to transmit valid data (2)			2	ms
T_{RESET}	DIS pulse width	Time DIS must be held high to reset part (2)	100			ns
T_{FAULT}	Fault assert time	Time from fault condition to FLT high (2)			50	µs

(1) Differential Return Gain given by SDD11, SDD22 = –11.6 + 13.33× $\log_{10}$(f÷8.25), f expressed in GHz
(2) Assured by simulation over process, supply, and temperature variation.

DETAILED DESCRIPTION

EQUALIZER

The data signal can be applied to an input equalizer by means of the input signal pins DIN+ / DIN–, which provide on-chip differential 100 Ω line-termination. The equalizer is enabled by setting EQENA = 1 (bit 1 of register 0). Equalization of up to 300 mm (12") of microstrip or stripline transmission line on FR4 printed circuit boards can be achieved. The amount of equalization is digitally controlled by the two-wire interface and control logic block, and is dependant on the register settings EQADJ[0...7] (register 6). The equalizer can also be turned off and bypassed by setting EQENA = 0. For details about the equalizer settings, see Table 12 - Register Functionality.

LIMITER

By limiting the output signal of the equalizer to a fixed value, the limiter removes any overshoot after the input equalization and provides the input signal for the output driver.

HIGH-SPEED OUTPUT DRIVER

The modulation current is sunk from the common emitter node of the limiting output driver differential pair by means of a modulation current generator, which is digitally controlled by the 2-wire serial interface.

The collector nodes of the output stages are connected to the output pins MOD+ and MOD–. The laser diode can be AC- or DC-coupled, depending on the required modulation current. To obtain the maximum modulation current of 80 mA, AC coupling is required. The modulation outputs are optimized for driving a 25 Ω load.

MODULATION CURRENT GENERATOR

The modulation current generator provides the current for the current modulator described above. The circuit is digitally controlled by the 2-wire interface block.

A 10-bit control bus, MODC[0...9] (register 2 and register 3), is used to set the desired modulation current.

The modulation current can be disabled by setting the DIS input pin high or setting ENA = 0 (bit 7 of register 0). The modulation current is also disabled in a fault condition if the internal fault detection enable register flag FLTEN is set (bit 3 of register 0).

DC OFFSET CANCELLATION AND CROSS POINT CONTROL

The ONET1101L has DC offset cancellation to compensate for internal offset voltages. The offset cancellation can be disabled by setting OCDIS = 1 (bit 3 of register 1). Disabling the offset cancellation permits the output crossing point to be adjusted from a minimum of 30% to 70% of the output eye diagram. The crossing point can be moved toward the one level be setting CPSGN = 1 (bit 7 of register 7) and it can be moved toward the zero level by setting CPSGN = 0. The shift percentage depends upon the register settings CPADJ[0...6] (register 7) and the cross point adjustment range bits CPRNG[0...1] (register 1). Setting CPRNG1 = 0 and CPRNG0 = 0 results in minimum adjustment (fine) capability and setting CPRNG1 = 1 and CPRNG0 = 1 results in maximum (coarse) adjustment capability.

BIAS CURRENT GENERATION AND APC LOOP

The bias current generation and APC loop are controlled by means of the 2-wire interface. In open loop operation, selected with OLENA = 1 (bit 4 of register 0), the bias current is set directly by the 10-bit control word BIASC[0...9] (register 4 and register 5). In automatic power control mode (select with OLENA = 0), the bias current depends on the register settings BIASC[0...9] and the coupling ratio (CR) between the laser bias current and the photodiode current. CR = I_{BIAS} / I_{PD}. If the photodiode anode is connected to the PD pin, set PDPOL = 1 (bit 0 of register 0) and if the photodiode cathode is connected to the PD pin, set PDPOL = 0.

Three photodiode current ranges can be selected by means of the PDRNG[1...0] bits (register 0). The photodiode range should be chosen to keep the laser bias control DAC, BIASC[0...9], close to its range center. This keeps the laser bias current set point resolution high. For details regarding the bias current setting in open- and closed-loop mode, see Table 12.

The ONET1101L has the ability to source or sink the bias current. For the BIAS pin to act as a source set BIASPOL = 1 (bit 2 of register 1) and for the BIAS pin to act as a sink set BIASPOL = 0.

The bias current is monitored using a current mirror with a gain value equal to 0.01 (1 %). By connecting a resistor between MONB and GND, the bias current can be monitored as a voltage across the resistor. A low temperature coefficient precision resistor should be used.

ANALOG REFERENCE

The ONET1101L laser driver is supplied by a single 3.3 V±10% supply voltage connected to the VCC pins. This voltage is referenced to ground (GND).

On-chip bandgap voltage circuitry generates a reference voltage, independent of the supply voltage, from which all other internally required voltages and bias currents are derived.

An external zero temperature coefficient resistor must be connected from the RZTC pin of the device to ground (GND). This resistor is used to generate a precise, zero TC current, which is required as a reference current for the on-chip DACs.

POWER-ON RESET

The ONET1101L has power-on reset circuitry that ensures all registers are reset to zero during startup. After the power-on to initialize time (t_{INIT1}), the internal registers are ready to load. The part is ready to transmit data after the initialize to transmit time (t_{INIT2}), assuming that the chip enable bit ENA is set to 1 and the disable pin DIS is low.

The ONET1101L can be disabled using the ENA control register bit or the disable pin DIS. In both cases the internal registers are not reset. After the disable pin DIS is set low or the enable bit ENA is set back to 1, the part returns to its prior output settings.

2-WIRE INTERFACE AND CONTROL LOGIC

The ONET1101L uses a 2-wire serial interface for digital control. The two circuit inputs, SDA and SCK, are driven, respectively, by the serial data and serial clock from a microprocessor, for example. For driving these inputs, TI recommends an open drain output.

The 2-wire interface provides write access to the internal memory map to modify control registers and read access to read out the control signals. The ONET1101L is a slave device only, which means that it cannot initiate a transmission itself; it always relies on the availability of the SCK signal for the duration of the transmission. The master device provides the clock signal plus the START and STOP commands. The protocol for a data transmission is:

1. START command
2. 7-bit slave address (0001000) followed by an eighth bit which is the data direction bit (R/W). A zero indicates a WRITE and a 1 indicates a READ.
3. 8-bit register address
4. 8-bit register data word
5. STOP command

Regarding timing, the ONET1101L is I^2C compatible. A typical timing diagram, shown in Figure 2 and Figure 3, describes a complete data transfer. Table 1 provides definitions of parameters for the Figure 2, I^2C Timing Diagram.

Bus Idle: Both SDA and SCK lines remain HIGH

Start Data Transfer: A change in the state of the SDA line, from HIGH to LOW, while the SCK line is HIGH, defines a START condition (S). Each data transfer begins with a START condition.

Stop Data Transfer: A change in the state of the SDA line from LOW to HIGH while the SCK line is HIGH defines a STOP condition (P). Each data transfer ends with a STOP condition; however, if the master still wishes to communicate on the bus, it can generate a repeated START condition and address another slave without first generating a STOP condition.

Data Transfer: Only one data byte can be transferred between a START and a STOP condition. The receiver acknowledges the transfer of data.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledgment bit. The transmitter releases the SDA line and a device that acknowledges, must pull down the SDA line during the acknowledge clock pulse simultaneously so the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Set-up and hold times must be taken into account. When a slave-receiver fails to acknowledge the slave address, the data line must be left HIGH by the slave. The master can generate a STOP condition to prevent the transfer. If the slave-receiver does acknowledge the slave address but some time later in the transfer cannot receive any more data bytes, the master must cancel the transfer. This is indicated by the slave generating the not acknowledge on the first following byte. The slave leaves the data line HIGH and the master generates the STOP condition.

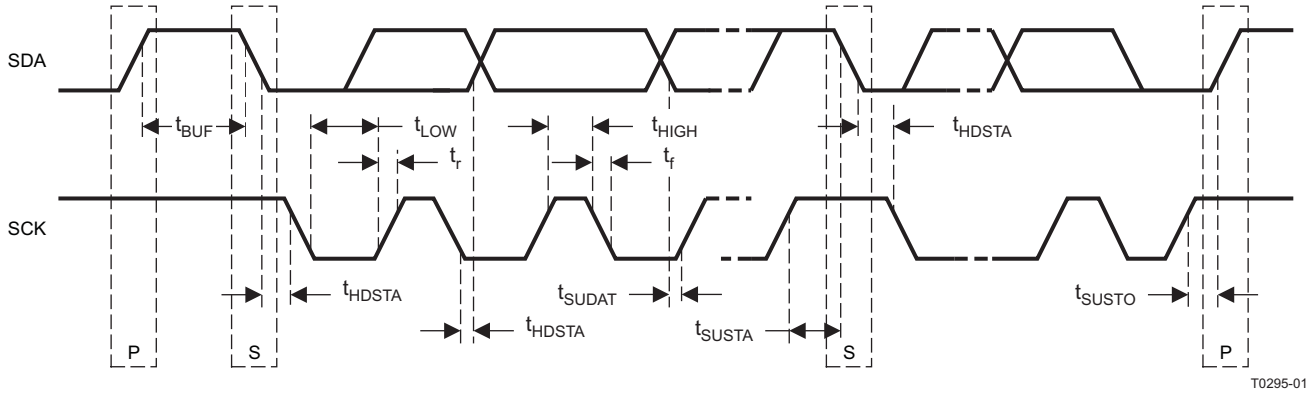


Figure 2. I²C Timing Diagram

Table 1. Timing Diagram Definitions

PARAMETER		MIN	MAX	UNIT
f_{SCK}	SCK clock frequency		400	kHz
t_{BUF}	Bus free time between START and STOP conditions	1.3		µs
t_{HDSTA}	Hold time after repeated START condition. After this period, the first clock pulse is generated	0.6		µs
t_{LOW}	Low period of the SCK clock	1.3		µs
t_{HIGH}	High period of the SCK clock	0.6		µs
t_{SUSTA}	Setup time for a repeated START condition	0.6		µs
t_{HDDAT}	Data HOLD time	0		µs
t_{SUDAT}	Data setup time	100		ns
t_R	Rise time of both SDA and SCK signals		300	ns
t_F	Fall time of both SDA and SCK signals		300	ns
t_{SUSTO}	Setup time for STOP condition	0.6		µs

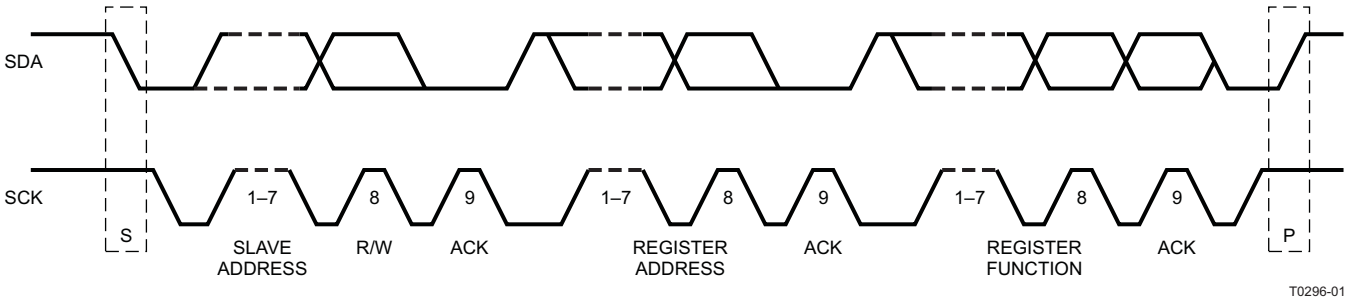


Figure 3. I²C Data Transfer

REGISTER MAPPING

The register mapping for register addresses 0 (0x00) through 9 (0x09) are shown in Table 2 through Table 11.

Table 12 describes the circuit functionality based on the register settings.

Table 2. Register 0 (0x00) Mapping – Control Settings

register address 0 (0x00)							
bit 7	**bit 6**	**bit 5**	**bit4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
ENA	PDRNG1	PDRNG0	OLENA	FLTEN	POL	EQENA	PDPOL

Table 3. Register 1 (0x01) Mapping – Control Settings

register address 1 (0x01)							
bit 7	**bit 6**	**bit 5**	**bit4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
–	–	–	–	OCDIS	BIASPOL	CPRNG1	CPRNG0

Table 4. Register 2 (0x02) Mapping – Modulation Current

register address 2 (0x02)							
bit 7	**bit 6**	**bit 5**	**bit4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
–	–	–	–	–	–	MODC1	MODC0

Table 5. Register 3 (0x03) Mapping – Modulation Current

register address 3 (0x03)							
bit 7	**bit 6**	**bit 5**	**bit4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
MODC9	MODC8	MODC7	MODC6	MODC5	MODC4	MODC3	MODC2

Table 6. Register 4 (0x04) Mapping – Bias Current

register address 4 (0x04)							
bit 7	**bit 6**	**bit 5**	**bit4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
–	–	–	–	–	–	BIASC1	BIASC0

Table 7. Register 5 (0x05) Mapping – Bias Current

register address 5 (0x05)							
bit 7	**bit 6**	**bit 5**	**bit4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
BIASC9	BIASC8	BIASC7	BIASC6	BIASC5	BIASC4	BIASC3	BIASC2

Table 8. Register 6 (0x06) Mapping – Equalizer Adjust

register address 6 (0x06)							
bit 7	**bit 6**	**bit 5**	**bit4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
EQADJ7	EQADJ6	EQADJ5	EQADJ4	EQADJ3	EQADJ2	EQADJ1	EQADJ0

Table 9. Register 7 (0x07) Mapping – Cross Point Adjust

register address 7 (0x07)							
bit 7	**bit 6**	**bit 5**	**bit4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
CPSGN	CPADJ6	CPADJ5	CPADJ4	CPADJ3	CPADJ2	CPADJ1	CPADJ0

Table 10. Register 8 (0x08) Mapping – Limiter Bias Current Adjust

register address 8 (0x08)							
bit 7	**bit 6**	**bit 5**	**bit4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
–	–	–	–	LIMCSGN	LIMC2	LIMC1	LIMC0

Table 11. Register 9 (0x09) Mapping – High Current Enable

register address 9 (0x09)							
bit 7	**bit 6**	**bit 5**	**bit4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
–	–	–	–	–	–	–	HMCENA

Table 12. Register Functionality

SYMBOL	REGISTER BIT	FUNCTION
ENA	Enable bit 7	**Enable chip bit** 1 = chip enabled. Can be toggled low to reset a fault condition. 0 = chip disabled
PDRNG1 PDRNG0	Photodiode current range bit 6 Photodiode current range bit 5	**Photodiode current range bits** 1X: up to 3080 µA / 3 µA resolution 01: up to 1540 µA / 1.5 µA resolution 00: up to 770 µA / 0.75 µA resolution
OLENA	Open loop enable bit 4	**Open loop enable bit** 1 = open loop bias current control 0 = closed loop bias current control
FLTEN	Fault detection enable bit 3	**Fault detection enable bit** 1 = fault detection on 0 = fault detection off
POL	Output polarity switch bit 2	**Output polarity switch bit** 1: pins 20 and 21 = MOD– and pins 22 and 23 = MOD+ 0: pins 20 and 21 = MOD+ and pins 22 and 23 = MOD–
EQENA	Equalizer enable bit 1	**Equalizer enable bit** 1 = equalizer enabled 0 = equalizer disabled
PDPOL	Photodiode polarity bit 0	**Photodiode polarity bit** 1 = photodiode cathode connected to V_{CC} 0 = photodiode anode connected to GND
OCDIS	Offset cancellation disable bit 3	**Offset cancellation disable bit** 1 = DC offset cancellation is disabled and cross point adjust is enabled 0 = DC offset cancellation is enabled and cross point adjust is disabled
BIASPOL	Bias current polarity bit 2	**Bias current polarity bit** 1 = Bias pin sources current 0 = Bias pin sinks current
CPRNG1 CPRNG0	Cross point range bit 1 Cross point range bit 0	**Cross point adjustment range bits:** Minimum adjustment range for 00 Maximum adjustment range for 11
MODC9	Modulation current bit 9 (MSB)	**Modulation current setting**
MODC8	Modulation current bit 8	
MODC7	Modulation current bit 7	
MODC6	Modulation current bit 6	
MODC5	Modulation current bit 5	
MODC4	Modulation current bit 4	Modulation current: 85 mA / 83 µA steps
MODC3	Modulation current bit 3	
MODC2	Modulation current bit 2	
MODC1	Modulation current bit 1	
MODC0	Modulation current bit 0 (LSB)	
BIASC9	Bias current bit 9 (MSB)	**Closed loop (APC)**
BIASC8	Bias current bit 8	Coupling ratio CR = I_{BIAS} / I_{PD}, BIASC = 0...1023, I_{BIAS} ≤ 100 mA
BIASC7	Bias current bit 7	
BIASC6	Bias current bit 6	PDRNG = 00 (see Photodiode current range bits); I_{BIAS} = 0.75 µA × CR × BIASC
BIASC5	Bias current bit 5	PDRNG = 01 (see Photodiode current range bits); I_{BIAS} = 1.5 µA × CR × BIASC
BIASC4	Bias current bit 4	PDRNG = 1X (see Photodiode current range bits); I_{BIAS} = 3 µA × CR × BIASC
BIASC3	Bias current bit 3	
BIASC2	Bias current bit 2	**Open loop**
BIASC1	Bias current bit 1	I_{BIAS} = 98 µA × BIASC
BIASC0	Bias current bit 0 (LSB)	

Table 12. Register Functionality (continued)

SYMBOL	REGISTER BIT	FUNCTION
EQADJ7	Equalizer adjustment bit 7 (MSB)	**Equalizer adjustment setting**
EQADJ6	Equalizer adjustment bit 6	
EQADJ5	Equalizer adjustment bit 5	EQENA = 0 (see Equalizer Enable Bit)
EQADJ4	Equalizer adjustment bit 4	Equalizer is turned off and bypassed
EQADJ3	Equalizer adjustment bit 3	
EQADJ2	Equalizer adjustment bit 2	EQENA = 1 (see Equalizer Enable Bit)
EQADJ1	Equalizer adjustment bit 1	Maximum equalization for 00000000
EQADJ0	Equalizer adjustment bit 0 (LSB)	Minimum equalization for 11111111
CPSGN	Eye crossing sign bit 7	**Eye cross-point adjustment setting**
CPADJ6	Eye crossing adjustment bit 6 (MSB)	CPSGN = 1 (positive shift)
CPADJ5	Eye crossing adjustment bit 5	Maximum shift for 1111111
CPADJ4	Eye crossing adjustment bit 4	Minimum shift for 0000000
CPADJ3	Eye crossing adjustment bit 3	CPSGN = 0 (negative shift)
CPADJ2	Eye crossing adjustment bit 2	Maximum shift for 1111111
CPADJ1	Eye crossing adjustment bit 1	Minimum shift for 0000000
CPADJ0	Eye crossing adjustment bit 0 (LSB)	
LIMCSGN	Limiter current sign bit 3	**Limiter bias current setting**
LIMC2	Limiter current bit 2 (MSB)	LIMCSGN = 1: decrease current
LIMC1	Limiter current bit 1	LIMCSGN = 0: increase current
LIMC0	Limiter current bit 0 (LSB)	No change for 000 and maximum change for 111
HMCENA	High modulation current enable bit 0	**High modulation current enable bit** 1 = high modulation current capability up to 100 mA 0 = modulation current capability up to 80 mA

LASER SAFETY FEATURES AND FAULT RECOVERY PROCEDURE

The ONET1101L provides built-in laser safety features and can detect these fault conditions:

- Voltage at MONB exceeds the voltage at RZTC (1.16 V)
- Photodiode current exceeds 150% of its set value
- Bias control DAC drops in value by more than 50% in one step

If one or more fault conditions happen and the fault enable bit FLTEN is set to 1, the ONET1101L responds by:

- Setting the bias current to zero.
- Setting the modulation current to zero.
- Asserting and latching the FLT pin.

ONET1101L Fault recovery happens using this procedure:

1. The disable pin DIS or the internal enable control bit ENA are toggled for at least the fault latch reset time.
2. The FLT pin de-asserts while the disable pin DIS is asserted or the enable bit ENA is de-asserted.
3. If the fault condition is no longer present, the part returns to normal operation with its prior output settings after the disable negate time.
4. If the fault condition is still present, FLT re-asserts once DIS is set to a low level and the part does not return to normal operation.

TYPICAL OPERATION CHARACTERISTICS

Typical operating condition is at V_{CC} = 3.3 V, T_A = 25°C, I_{BIAS} = 40 mA, I_{MOD} = 40 mA, V_{IN} = 600 mVpp (unless otherwise noted).

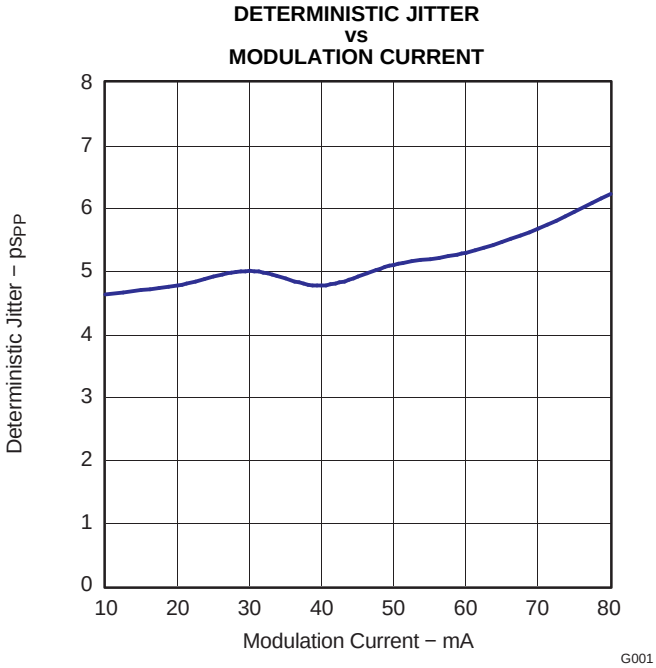


Figure 4.

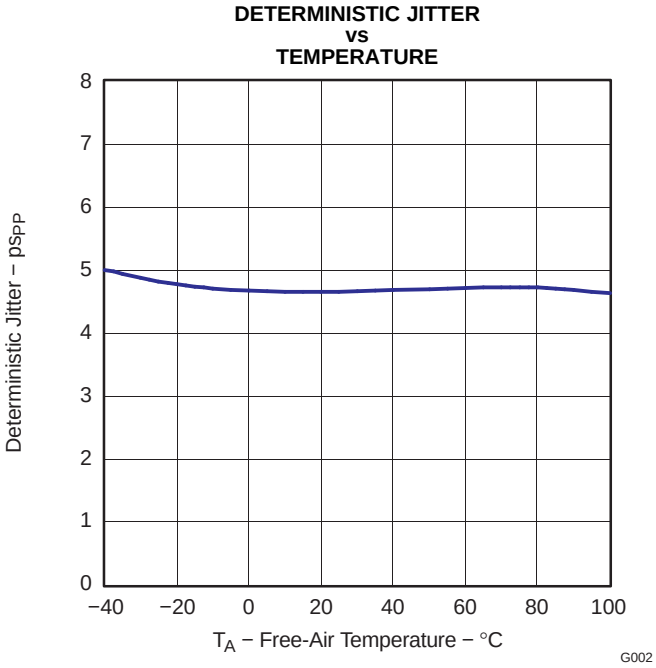


Figure 5.

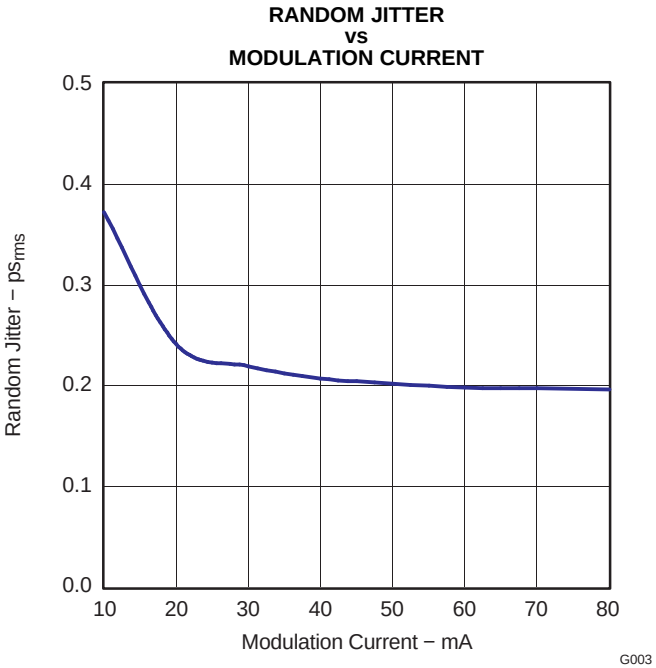


Figure 6.

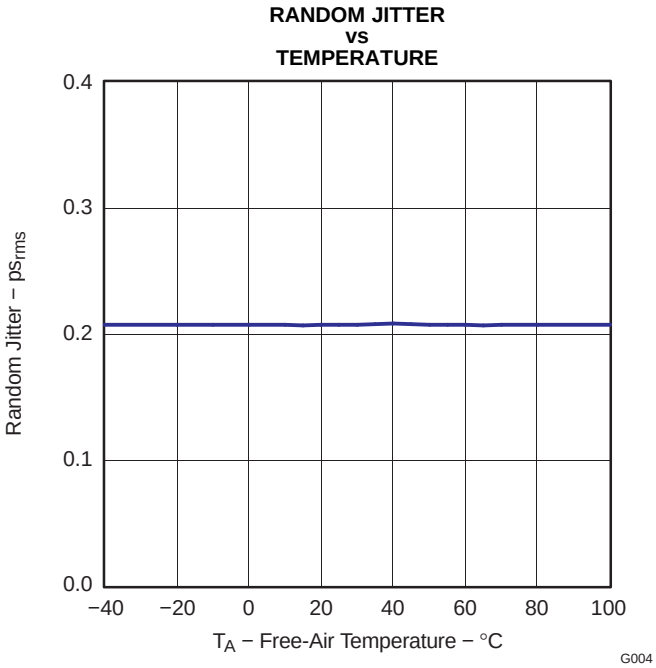


Figure 7.

TYPICAL OPERATION CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3 V, T_A = 25°C, I_{BIAS} = 40 mA, I_{MOD} = 40 mA, V_{IN} = 600 mVpp (unless otherwise noted).

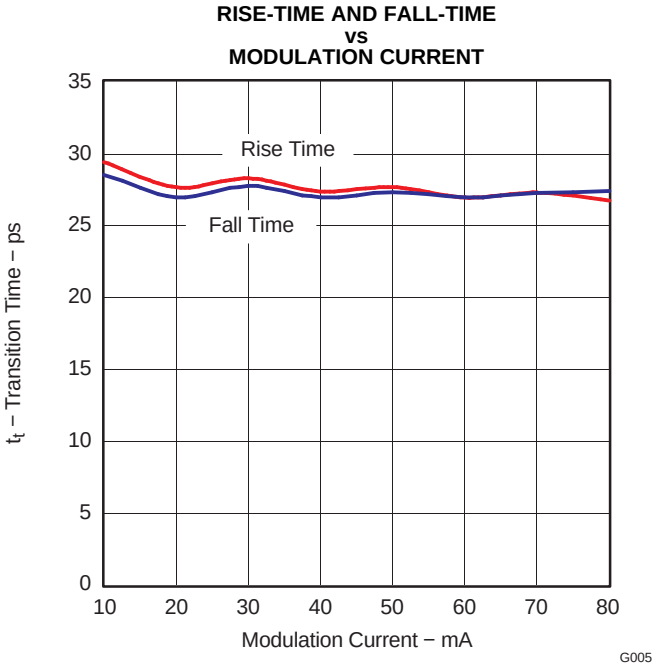


Figure 8.

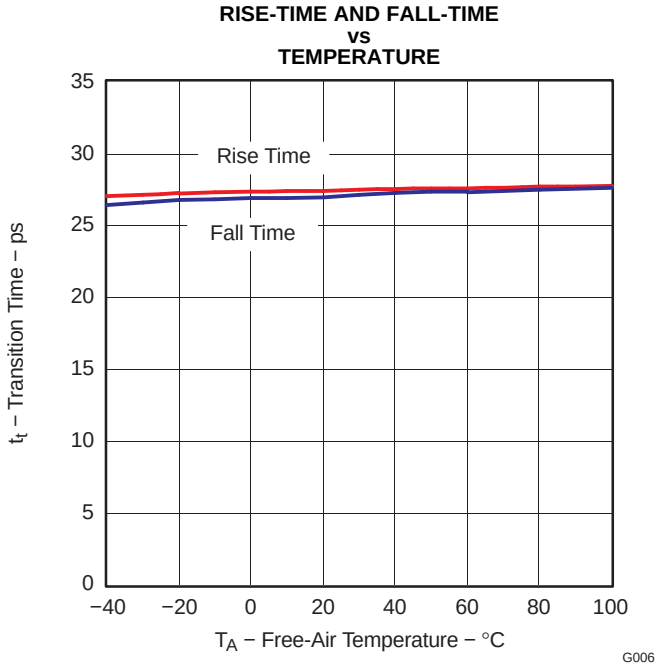


Figure 9.

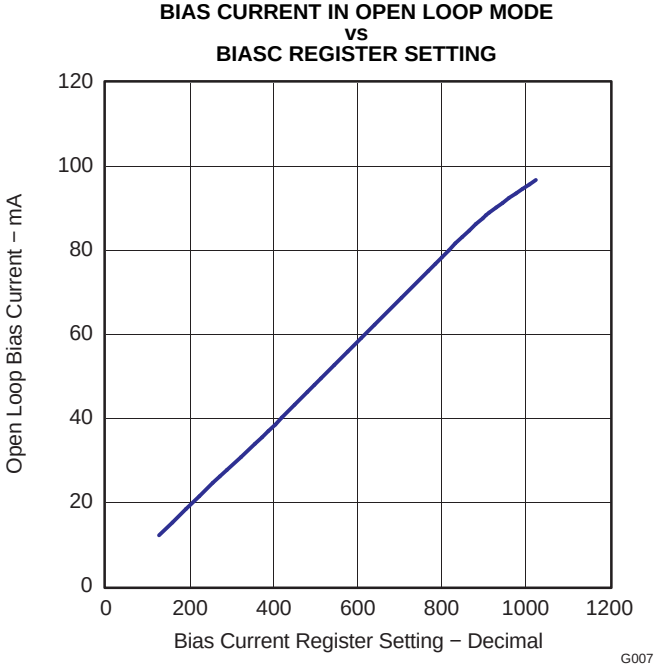


Figure 10.

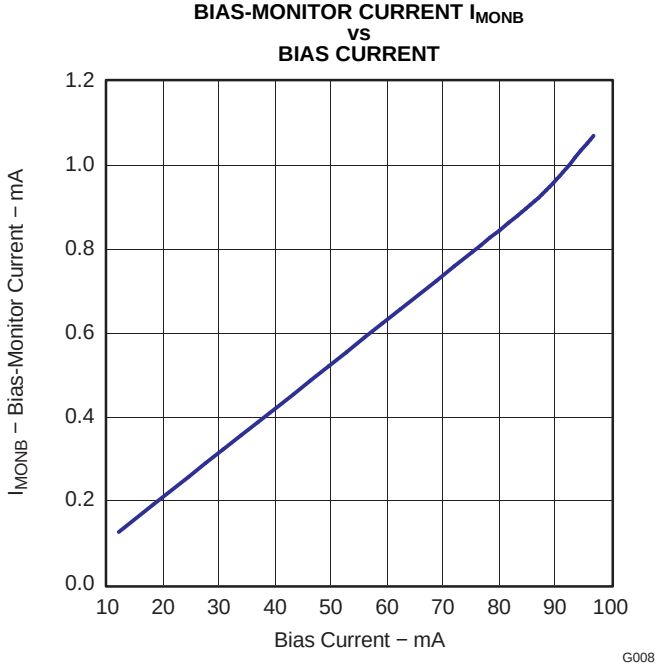


Figure 11.

TYPICAL OPERATION CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3 V, T_A = 25°C, I_{BIAS} = 40 mA, I_{MOD} = 40 mA, V_{IN} = 600 mVpp (unless otherwise noted).

PHOTODIODE-MONITOR CURRENT I_{MONP} VS PD CURRENT

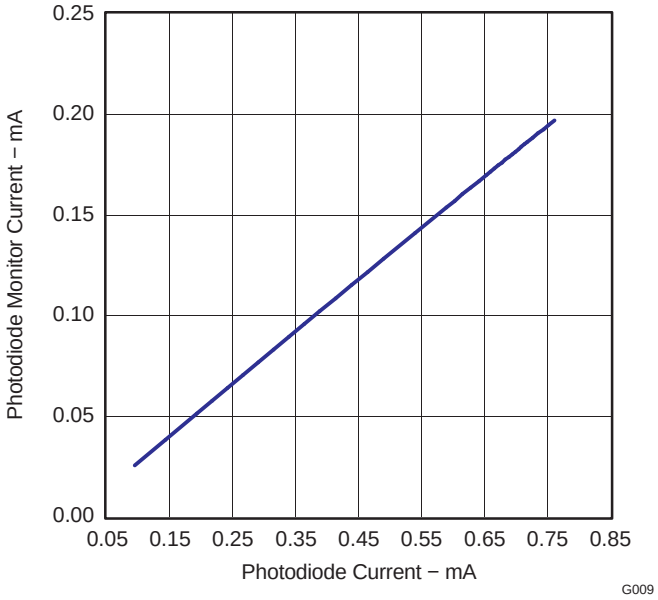


Figure 12.

MODULATION CURRENT VS MODC REGISTER SETTING

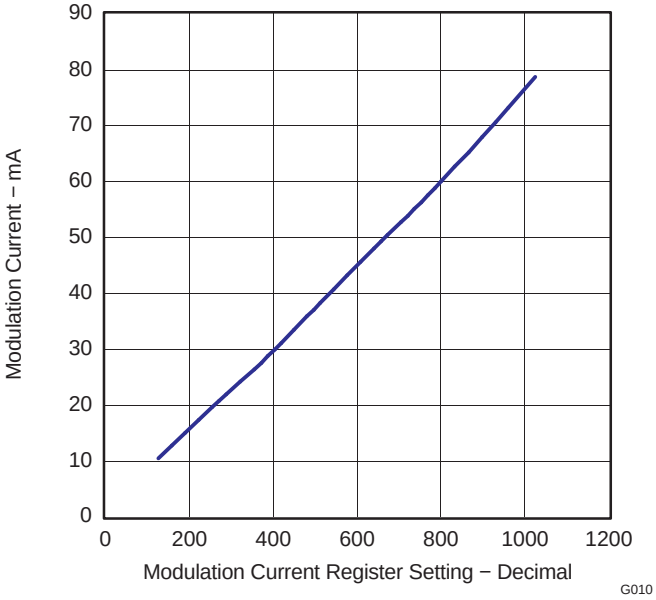


Figure 13.

SUPPLY CURRENT (includes I_{BIAS} and I_{MOD}) VS TEMPERATURE

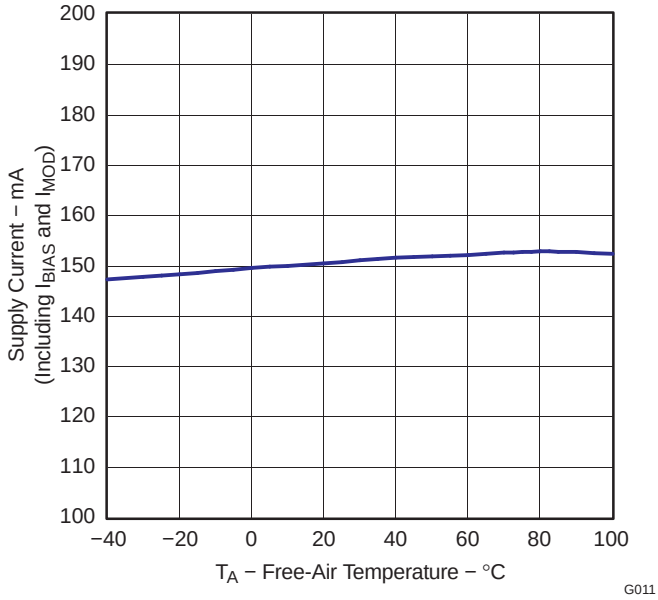


Figure 14.

EYE-DIAGRAM AT 11.3 GBPS, PRBS-31 PATTERN I_{MOD} = 20 mA, EQENA = 0

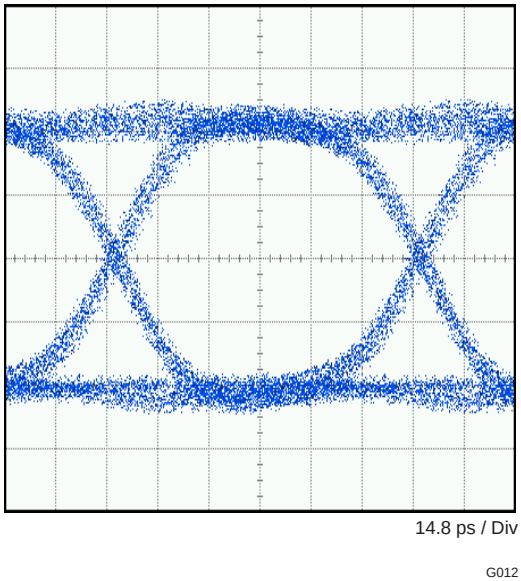


Figure 15.

TYPICAL OPERATION CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3 V, T_A = 25°C, I_{BIAS} = 40 mA, I_{MOD} = 40 mA, V_{IN} = 600 mVpp (unless otherwise noted).

EYE-DIAGRAM AT 11.3GBPS, PRBS-31 PATTERN
I_{MOD} = 40 mA, EQENA = 0

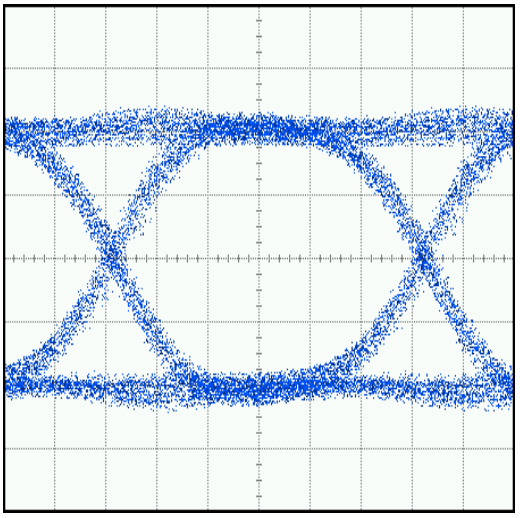


Figure 16.

EYE-DIAGRAM AT 11.3GBPS, PRBS-31 PATTERN
I_{MOD} = 60 mA, EQENA = 0

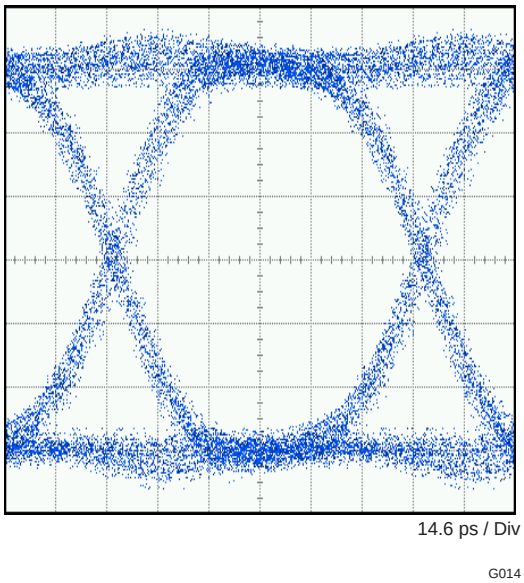


Figure 17.

EYE-DIAGRAM AT 11.3GBPS, PRBS-31 PATTERN
I_{MOD} = 40 mA, EQENA = 1
12" OF FR4 AT INPUTS

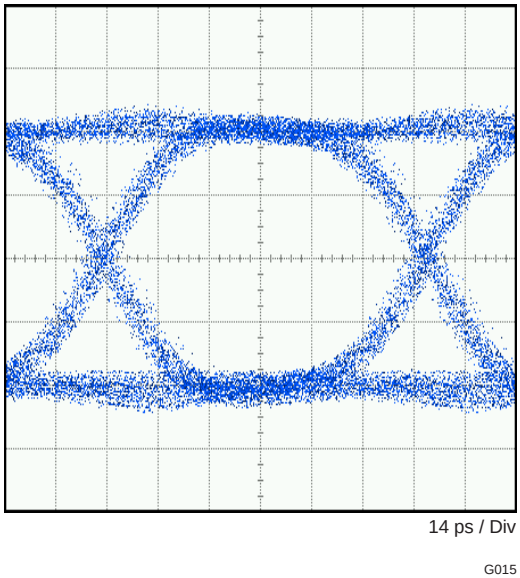
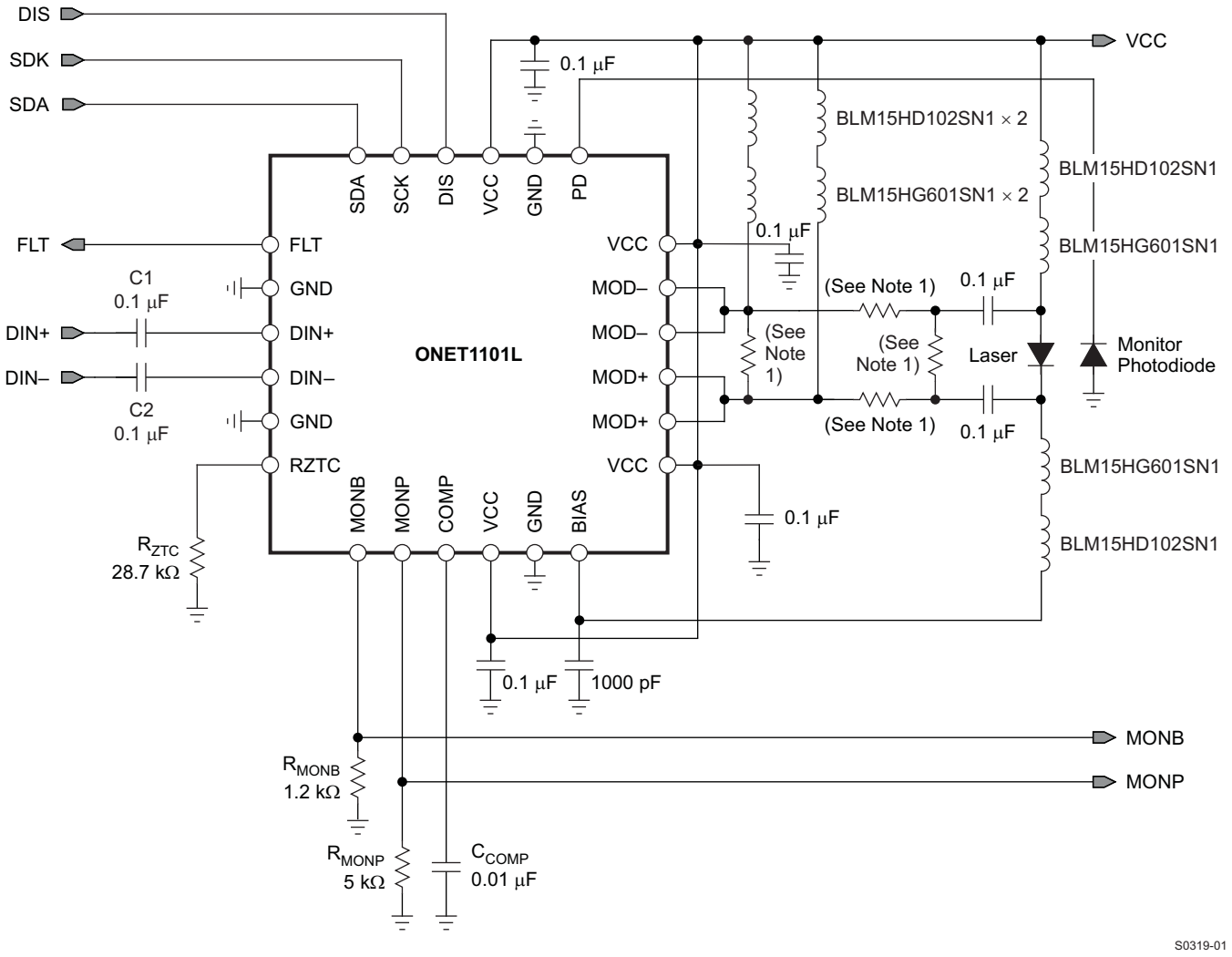


Figure 18.

APPLICATION INFORMATION

Figure 19 and Figure 20 show typical application circuits using the ONET1101L with a laser biased to VCC (BIAS pin sink) and driven differentially or single-ended. The laser driver is controlled using the 2-wire interface SDA/SCK by a microcontroller. In a typical application, the FLT, MONB, and MONP outputs are also connected to the microcontroller for transceiver management purposes.

The component values in Figure 19 and Figure 20 are typical examples and may be varied according to the intended application.



(1) Resistor values depend on the TOSA diode used.

Figure 19. AC Coupled Differential Drive

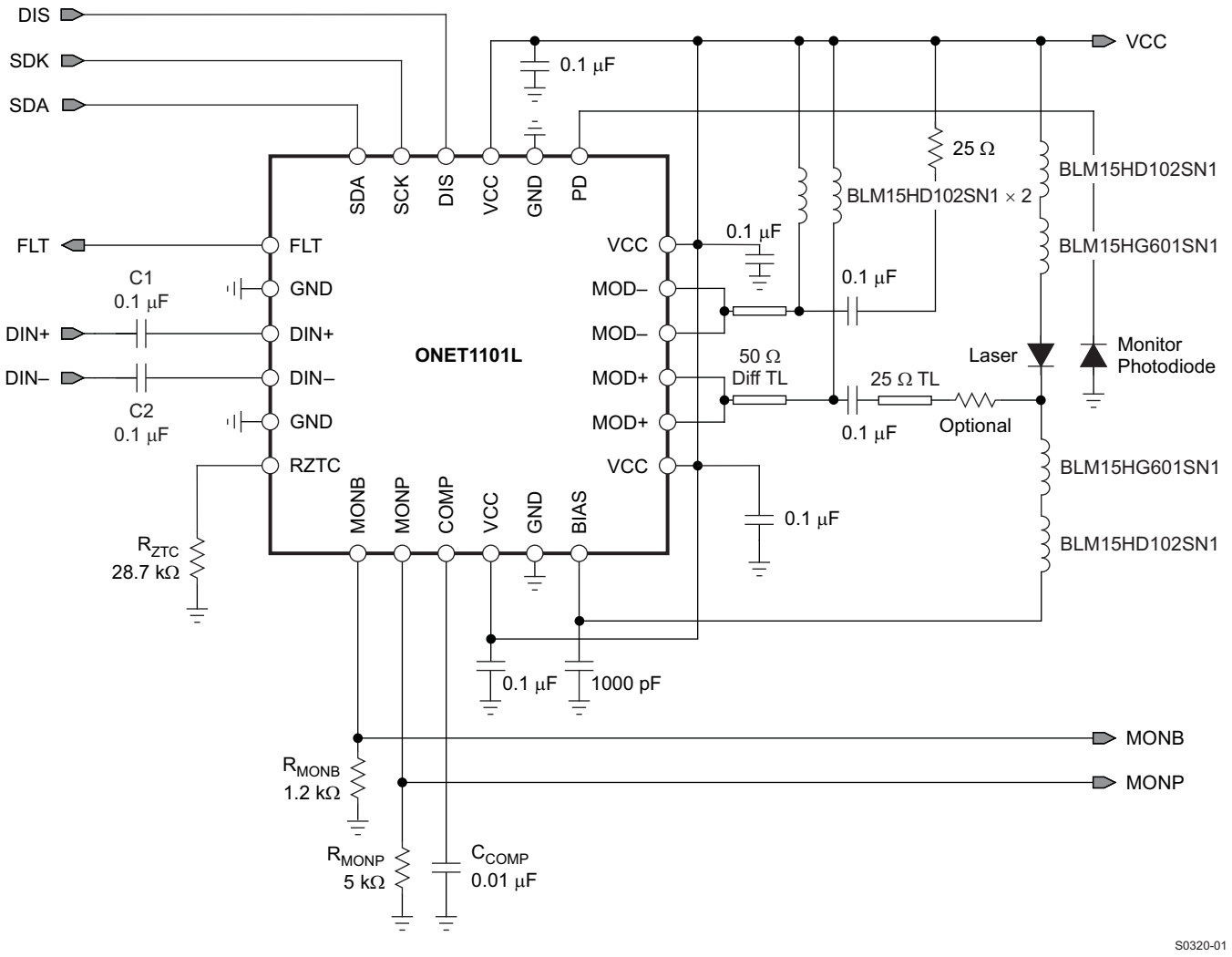


Figure 20. AC Coupled Single-Ended Drive

CALCULATING POWER CONSUMPTION

The power dissipation is different, depending if the BIAS pin is sourcing or sinking current. Lower power dissipation in the ONET1101L can be achieved if the BIAS pin sinks the bias current because the BIAS pin compliance voltage is typically less than 1 V.

The power dissipation is calculated as:

$$P = V_{CC} \times (I_{VCC} + I_{MOD}) + (V_{BIAS} \times I_{BIAS})$$

Where:

V_{CC} is the power supply voltage
I_{VCC} is the supply current excluding modulation and bias current
I_{MOD} is the modulation current
V_{BIAS} is the voltage at the BIAS pin
I_{BIAS} is the bias current

LAYOUT GUIDELINES

For optimum performance, use 50 Ω transmission lines (100 Ω differential) for connecting the signal source to the DIN+ and DIN– pins and 25 Ω transmission lines (50 Ω differential) for connecting the modulation current outputs, MOD+ and MOD–, to the laser. The length of the transmission lines should be kept as short as possible to reduce loss and pattern-dependent jitter. It is recommended to assemble the series matching resistor as close as possible to the TOSA diode, if required.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ONET1101LRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-25 to 100	ONET 1101L	Samples
ONET1101LRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-25 to 100	ONET 1101L	Samples
ONET1101LRGETG4	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-25 to 100	ONET 1101L	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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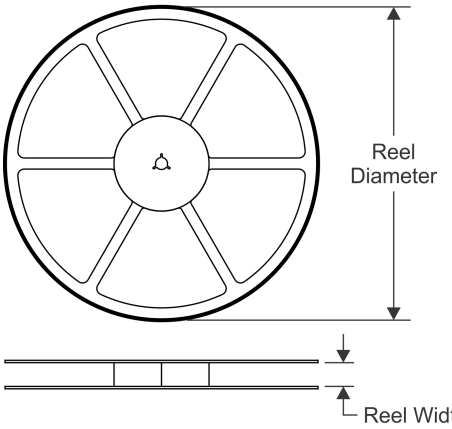
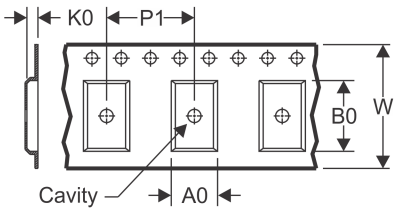
TAPE AND REEL INFORMATION

REEL DIMENSIONS

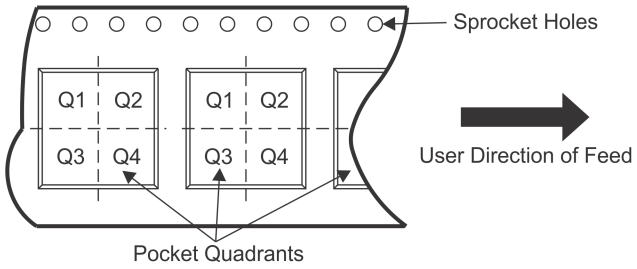


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

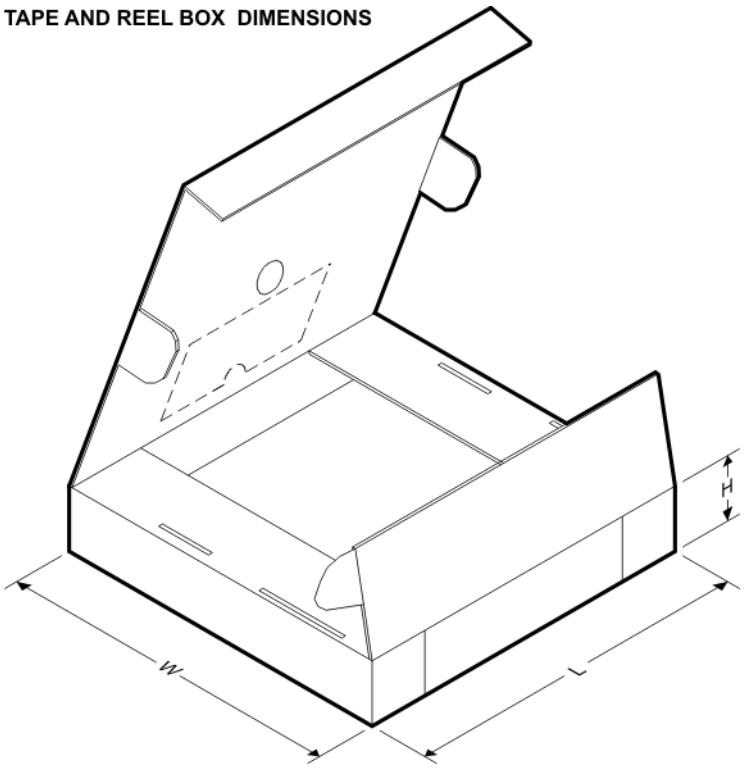
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ONET1101LRGER	VQFN	RGE	24	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
ONET1101LRGET	VQFN	RGE	24	250	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



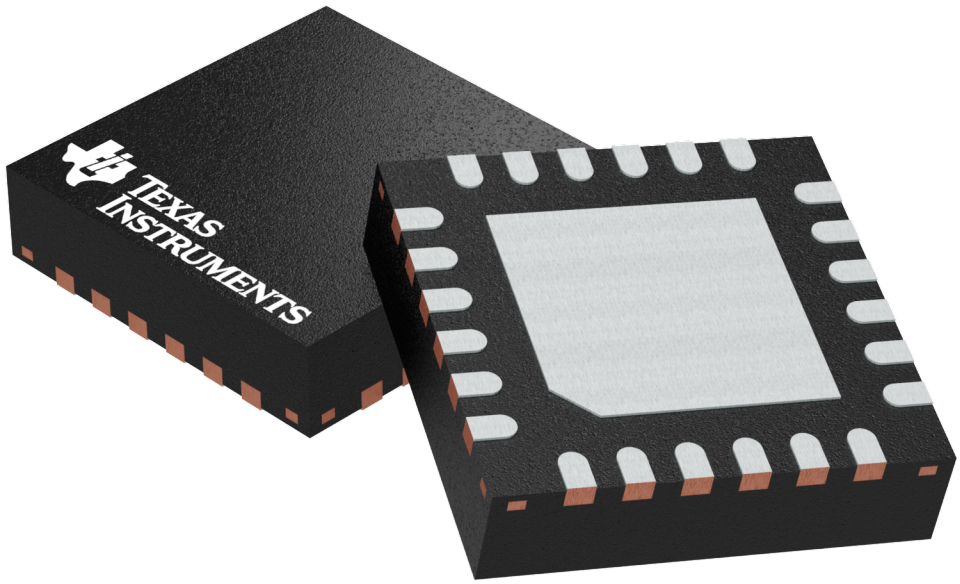
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ONET1101LRGER	VQFN	RGE	24	3000	338.1	338.1	20.6
ONET1101LRGET	VQFN	RGE	24	250	367.0	367.0	38.0

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

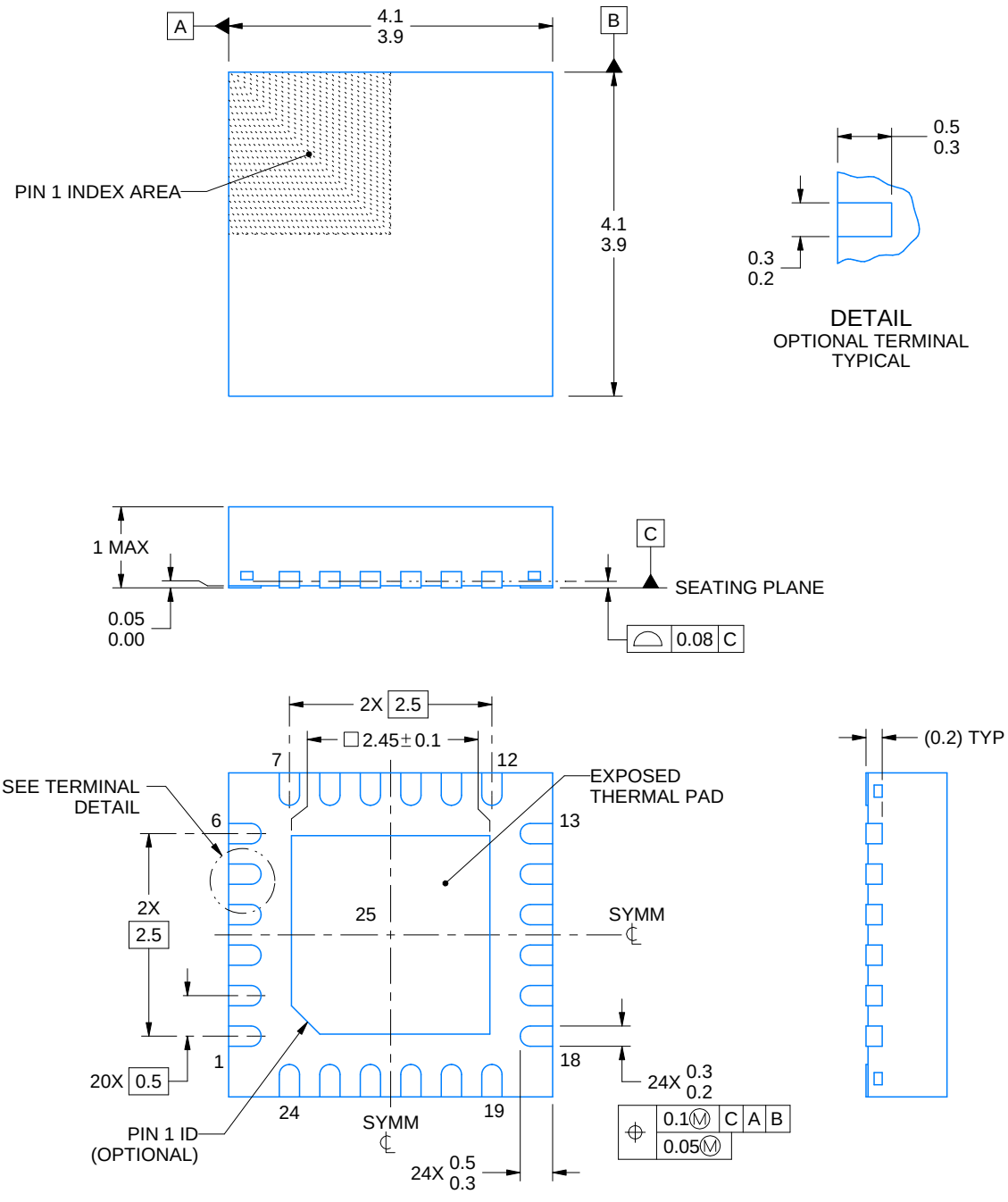
4204104/H

PACKAGE OUTLINE

RGE0024B

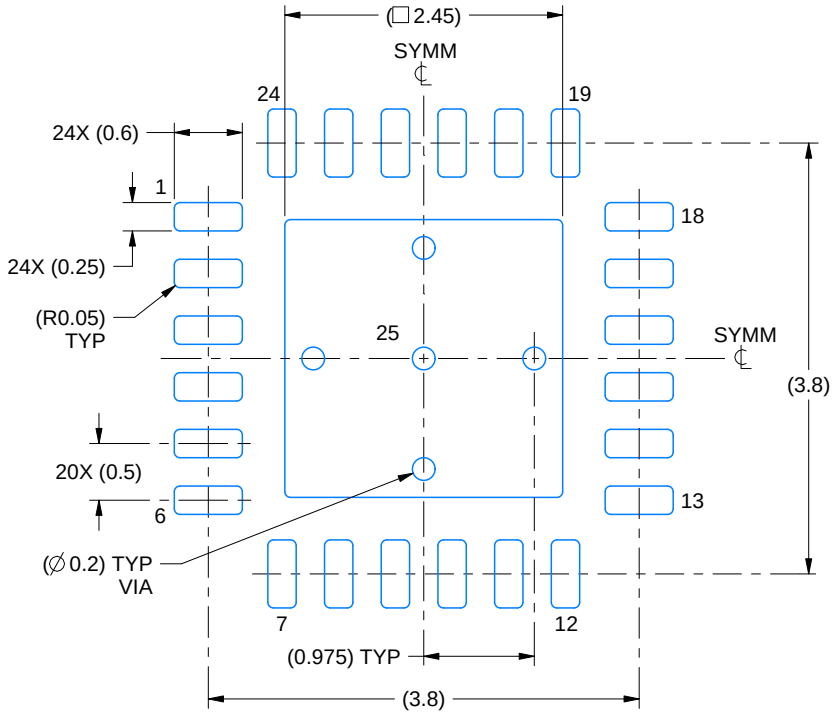
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

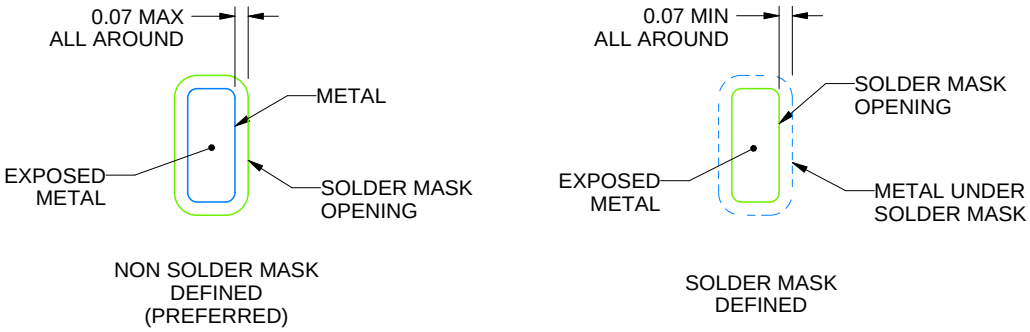


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

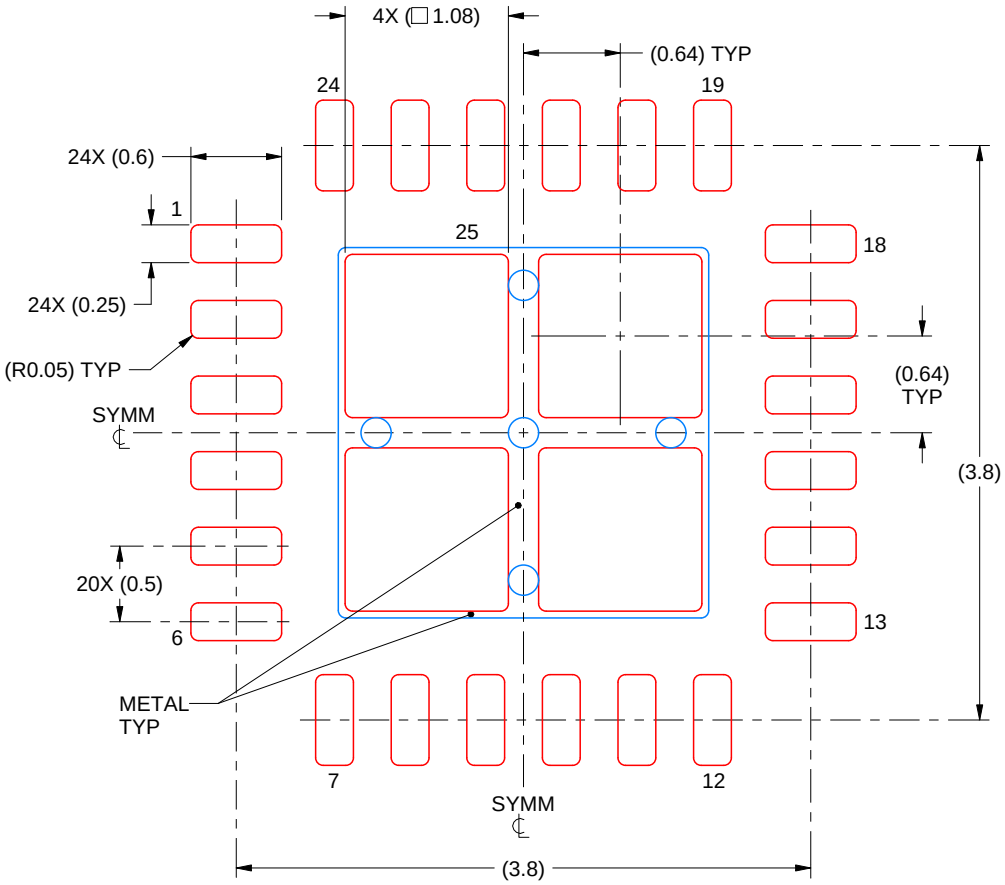


SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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