



**THE DATASHEET OF  
NLSX3013BFCT1G**



# NLSX3013

## 8-Bit 100 Mb/s Configurable Dual-Supply Level Translator

The NLSX3013 is a 8-bit configurable dual-supply bidirectional level translator without a direction control pin. The I/O  $V_{CC}$  and I/O  $V_L$  ports are designed to track two different power supply rails,  $V_{CC}$  and  $V_L$  respectively. The  $V_{CC}$  supply rail is configurable from 1.3 V to 4.5 V while the  $V_L$  supply rail is configurable from 0.9 V to ( $V_{CC} - 0.4$ ) V. This allows lower voltage logic signals on the  $V_L$  side to be translated into higher voltage logic signals on the  $V_{CC}$  side, and vice-versa. Both I/O ports are auto-sensing; thus, no direction pin is required.

The Output Enable (EN) input, when Low, disables both I/O ports by putting them in 3-state. This significantly reduces the supply currents from both  $V_{CC}$  and  $V_L$ . The EN signal is designed to track  $V_L$ .

### Features

- Wide High-Side  $V_{CC}$  Operating Range: 1.3 V to 4.5 V  
Wide Low-Side  $V_L$  Operating Range: 0.9 V to ( $V_{CC} - 0.4$ ) V
- High-Speed with 100 Mb/s Guaranteed Data Rate for  $V_L > 1.8$  V
- Low Bit-to-Bit Skew
- Overvoltage Tolerant Enable and I/O Pins
- Non-preferential Powerup Sequencing
- Small packaging: 2.03 mm x 2.54 mm 20 Pin Flip-Chip
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- Mobile Phones, PDAs, Other Portable Devices
- PC and Laptops
- ESD Protection for All Pins: Human Body Model (HBM) > 6000 V



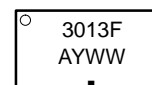
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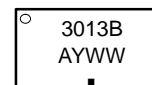
### MARKING DIAGRAM for NLSX3013FCT1G



A1  
20 PIN FLIP-CHIP  
CASE 766AK

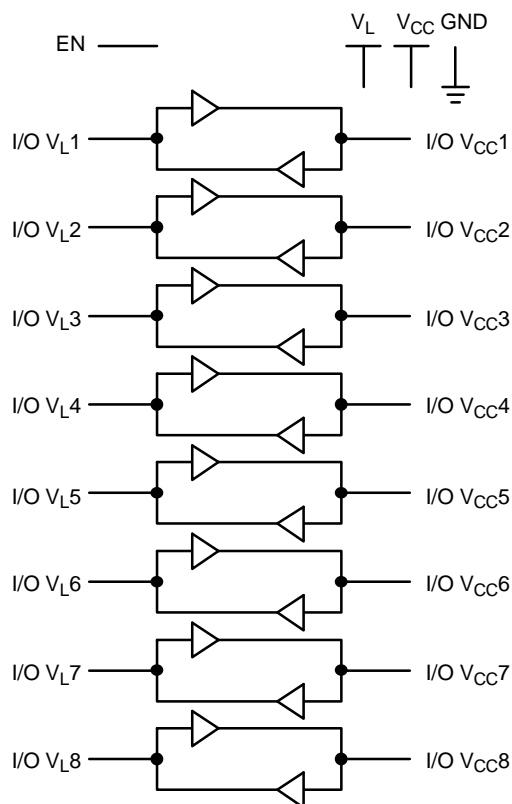


### for NLSX3013BFCT1G



A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

### LOGIC DIAGRAM



### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

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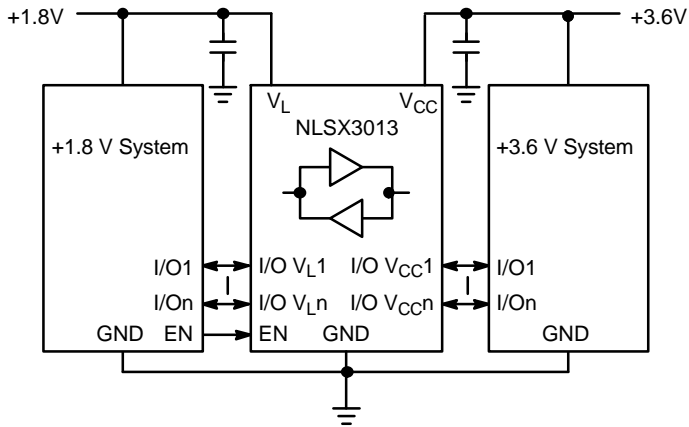


Figure 1. Typical Application Circuit

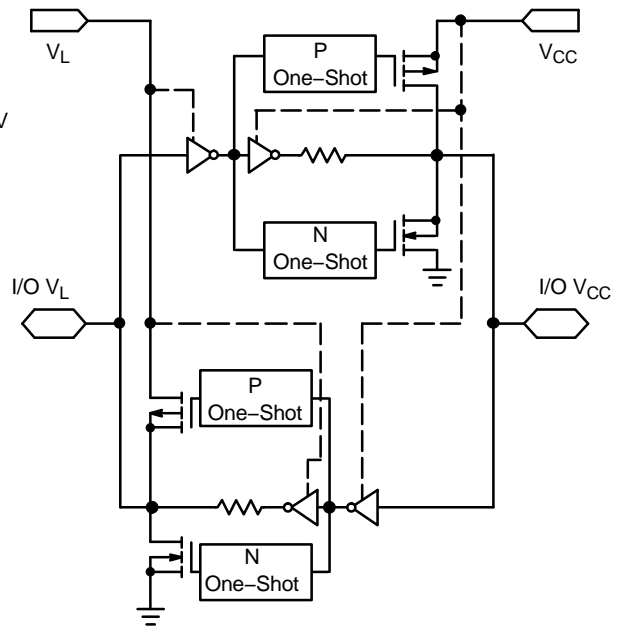


Figure 2. Simplified Functional Diagram (1 I/O Line)  
(EN = 1)

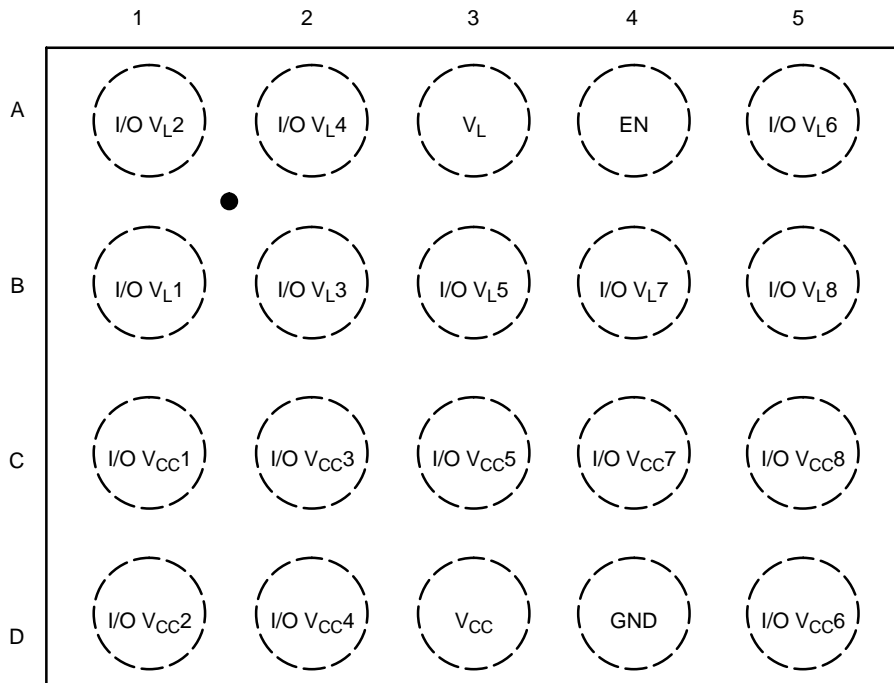
## PIN ASSIGNMENT

Pins	Description
V <sub>CC</sub>	V <sub>CC</sub> Input Voltage
V <sub>L</sub>	V <sub>L</sub> Input Voltage
GND	Ground
EN	Output Enable
I/O V <sub>CCn</sub>	I/O Port, Referenced to V <sub>CC</sub>
I/O V <sub>Ln</sub>	I/O Port, Referenced to V <sub>L</sub>

## FUNCTION TABLE

EN	Operating Mode
L	Hi-Z
H	I/O Buses Connected

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**Figure 3. 20 Flip-Chip (2.54 mm x 2.03 mm)**  
(Top View)

## PIN ASSIGNMENT

Pin	Name	Description
A1	I/O VL2	I/O Port 2, Referenced to VL
A2	I/O VL4	I/O Port 4, Referenced to VL
A3	VL	VL Input Voltage
A4	EN	Output Enable
A5	I/O VL6	I/O Port 6, Referenced to VL
B1	I/O VL1	I/O Port 1, Referenced to VL
B2	I/O VL3	I/O Port 3, Referenced to VL
B3	I/O VL5	I/O Port 5, Referenced to VL
B4	I/O VL7	I/O Port 7, Referenced to VL
B5	I/O VL8	I/O Port 8, Referenced to VL
C1	I/O VCC1	I/O Port 1, Referenced to VCC
C2	I/O VCC3	I/O Port 3, Referenced to VCC
C3	I/O VCC5	I/O Port 5, Referenced to VCC
C4	I/O VCC7	I/O Port 7, Referenced to VCC
C5	I/O VCC8	I/O Port 8, Referenced to VCC
D1	I/O VCC2	I/O Port 2, Referenced to VCC
D2	I/O VCC4	I/O Port 4, Referenced to VCC
D3	VCC	VCC Input Voltage
D4	GND	Ground
D5	I/O VCC6	I/O Port 6, Referenced to VCC

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## MAXIMUM RATINGS

Symbol	Parameter	Condition	Value	Unit
$V_{CC}$	$V_{CC}$ Supply Voltage		-0.5 to +5.5	V
$V_L$	$V_L$ Supply Voltage		-0.5 to +5.5	V
I/O $V_{CC}$	$V_{CC}$ -Referenced DC Input/Output Voltage		-0.5 to ( $V_{CC} + 0.3$ )	V
I/O $V_L$	$V_L$ -Referenced DC Input/Output Voltage		-0.5 to ( $V_L + 0.3$ )	V
$V_{EN}$	Enable Control Pin DC Input Voltage		-0.5 to +5.5	V
$I_{IK}$	Input Diode Clamp Current	$V_I < GND$	-50	mA
$I_{OK}$	Output Diode Clamp Current	$V_O < GND$	-50	mA
$I_{CC}$	DC Supply Current Through $V_{CC}$		$\pm 100$	mA
$I_L$	DC Supply Current Through $V_L$		$\pm 100$	mA
$I_{GND}$	DC Ground Current Through Ground Pin		$\pm 100$	mA
$T_{STG}$	Storage Temperature Range		-65 to +150	$^{\circ}C$
$\theta_{JA}$	Junction-to-Ambient Thermal Resistance (Note 1)		53	$^{\circ}C/W$
$\Psi_{JC(top)}$	Junction-to-Case (Top) Thermal Resistance		<10	$^{\circ}C/W$
$T_J$	Junction Temperature		+125	$^{\circ}C$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured per JESD51-7, with minimum pad spacing on FR-4 board, using 200 mm<sup>2</sup> copper area, two 80 mm x 80 mm ground planes and 2.0 ounce copper traces with no air flow.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
$V_{CC}$	$V_{CC}$ Supply Voltage		1.3	4.5	V
$V_L$	$V_L$ Supply Voltage		0.9	$V_{CC} - 0.4$	V
$V_{EN}$	Enable Control Pin Voltage		GND	4.5	V
$V_{IO}$	Bus Input/Output Voltage	I/O $V_{CC}$ I/O $V_L$	GND GND	4.5 4.5	V
$T_A$	Operating Temperature Range		-40	+85	$^{\circ}C$
$\Delta I/\Delta V$	Input Transition Rise or Rate $V_I, V_{IO}$ from 30% to 70% of $V_{CC}$ ; $V_{CC} = 3.3 V \pm 0.3 V$		0	10	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions (Note 2)	V <sub>CC</sub> (V) (Note 3)	V <sub>L</sub> (V) (Note 4)	-40°C to +85°C			Unit
					Min	Typ (Note 5)	Max	
V <sub>IHC</sub>	I/O V <sub>CC</sub> Input HIGH Voltage		1.3 to 4.5	0.9 to (V <sub>CC</sub> - 0.4)	0.8 * V <sub>CC</sub>	-	-	V
V <sub>ILC</sub>	I/O V <sub>CC</sub> Input LOW Voltage		1.3 to 4.5	0.9 to (V <sub>CC</sub> - 0.4)	-	-	0.2 * V <sub>CC</sub>	V
V <sub>IHL</sub>	I/O V <sub>L</sub> Input HIGH Voltage		1.3 to 4.5	0.9 to (V <sub>CC</sub> - 0.4)	0.8 * V <sub>L</sub>	-	-	V
V <sub>ILL</sub>	I/O V <sub>L</sub> Input LOW Voltage		1.3 to 4.5	0.9 to (V <sub>CC</sub> - 0.4)	-	-	0.2 * V <sub>L</sub>	V
V <sub>IH</sub>	Control Pin Input HIGH Voltage	T <sub>A</sub> = +25°C	1.3 to 4.5	0.9 to (V <sub>CC</sub> - 0.4)	0.8 * V <sub>L</sub>	-	-	V
V <sub>IL</sub>	Control Pin Input LOW Voltage	T <sub>A</sub> = +25°C	1.3 to 4.5	0.9 to (V <sub>CC</sub> - 0.4)	-	-	0.2 * V <sub>L</sub>	V
V <sub>OHC</sub>	I/O V <sub>CC</sub> Output HIGH Voltage	I/O V <sub>CC</sub> Source Current = 20 μA	1.3 to 4.5	0.9 to (V <sub>CC</sub> - 0.4)	0.8 * V <sub>CC</sub>	-	-	V
V <sub>OLC</sub>	I/O V <sub>CC</sub> Output LOW Voltage	I/O V <sub>CC</sub> Sink Current = 20 μA	1.3 to 4.5	0.9 to (V <sub>CC</sub> - 0.4)	-	-	0.2 * V <sub>CC</sub>	V
V <sub>OHL</sub>	I/O V <sub>L</sub> Output HIGH Voltage	I/O V <sub>L</sub> Source Current = 20 μA	1.3 to 4.5	0.9 to (V <sub>CC</sub> - 0.4)	0.8 * V <sub>L</sub>	-	-	V
V <sub>OLL</sub>	I/O V <sub>L</sub> Output LOW Voltage	I/O V <sub>L</sub> Sink Current = 20 μA	1.3 to 4.5	0.9 to (V <sub>CC</sub> - 0.4)	-	-	0.2 * V <sub>L</sub>	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Normal test conditions are V<sub>EN</sub> = 0 V, C<sub>IOVCC</sub> = 15 pF and C<sub>IOVL</sub> = 15 pF, unless otherwise specified.
- V<sub>CC</sub> is the supply voltage associated with the high voltage port, and V<sub>CC</sub> ranges from +1.3 V to 4.5 V under normal operating conditions.
- V<sub>L</sub> is the supply voltage associated with the low voltage port. V<sub>L</sub> must be less than or equal to (V<sub>CC</sub> - 0.4) V during normal operation. However, during startup and shutdown conditions, V<sub>L</sub> can be greater than (V<sub>CC</sub> - 0.4) V.
- Typical values are for V<sub>CC</sub> = +2.8 V, V<sub>L</sub> = +1.8 V and T<sub>A</sub> = +25°C. All units are production tested at T<sub>A</sub> = +25°C. Limits over the operating temperature range are guaranteed by design.

POWER CONSUMPTION

Symbol	Parameter	Test Conditions (Note 6)	V <sub>CC</sub> (V) (Note 7)	V <sub>L</sub> (V) (Note 8)	-40°C to +85°C			Unit
					Min	Typ	Max	
I <sub>Q-VCC</sub>	Supply Current from V <sub>CC</sub>	EN = V <sub>L</sub> ; I/O V <sub>CCn</sub> = 0 V, I/O V <sub>Ln</sub> = 0 V, I/O V <sub>CCn</sub> = V <sub>CC</sub> or I/O V <sub>Ln</sub> = V <sub>L</sub> and I <sub>o</sub> = 0	1.3 to 3.6	0.9 to (V <sub>CC</sub> - 0.4)	-	-	1.0	μA
I <sub>Q-VL</sub>	Supply Current from V <sub>L</sub>	EN = V <sub>L</sub> ; I/O V <sub>CCn</sub> = 0 V, I/O V <sub>Ln</sub> = 0 V, I/O V <sub>CCn</sub> = V <sub>CC</sub> or I/O V <sub>Ln</sub> = V <sub>L</sub> and I <sub>o</sub> = 0	1.3 to 3.6	0.9 to (V <sub>CC</sub> - 0.4)	-	-	1.0	μA
		EN = V <sub>L</sub> ; I/O V <sub>CCn</sub> = 0 V, I/O V <sub>Ln</sub> = 0 V, I/O V <sub>CCn</sub> = V <sub>CC</sub> or I/O V <sub>Ln</sub> = (V <sub>CC</sub> - 0.2 V) and I <sub>o</sub> = 0		< (V <sub>CC</sub> - 0.2)				
I <sub>TS-VCC</sub>	V <sub>CC</sub> Tristate Output Mode Supply Current	EN = 0 V	1.3 to 3.6	0.9 to (V <sub>CC</sub> - 0.4)	-	-	1.0	μA
I <sub>TS-VL</sub>	V <sub>L</sub> Tristate Output Mode Supply Current	EN = 0 V	1.3 to 3.6	0.9 to (V <sub>CC</sub> - 0.4)	-	-	0.2	μA
		EN = 0 V		V <sub>CC</sub> - 0.2				
I <sub>OZ</sub>	I/O Tristate Output Mode Leakage Current	EN = 0 V	1.3 to 3.6	0.9 to (V <sub>CC</sub> - 0.4)	-	-	0.15	μA
		EN = 0 V		V <sub>CC</sub> - 0.2				
I <sub>EN</sub>	Output Enable Pin Input Current	-	1.3 to 3.6	0.9 to (V <sub>CC</sub> - 0.4)	-	-	1.0	μA

- Normal test conditions are V<sub>EN</sub> = 0 V, C<sub>IOVCC</sub> = 15 pF and C<sub>IOVL</sub> = 15 pF, unless otherwise specified.
- V<sub>CC</sub> is the supply voltage associated with the high voltage port, and V<sub>CC</sub> ranges from +1.3 V to 4.5 V under normal operating conditions.
- V<sub>L</sub> is the supply voltage associated with the low voltage port. V<sub>L</sub> must be less than or equal to (V<sub>CC</sub> - 0.4) V during normal operation. However, during startup and shutdown conditions, V<sub>L</sub> can be greater than (V<sub>CC</sub> - 0.4) V.

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## TIMING CHARACTERISTICS

Symbol	Parameter	Test Conditions (Note 9)	V <sub>CC</sub> (V) (Note 10)	V <sub>L</sub> (V) (Note 11)	-40°C to +85°C			Unit
					Min	Typ (Note 12)	Max	
t <sub>R-VCC</sub>	I/O V <sub>CC</sub> Rise Time (Output = I/O_V <sub>CC</sub> )	C <sub>I<sub>O</sub>V<sub>CC</sub></sub> = 15 pF	1.3 to 4.5	0.9 to (V <sub>CC</sub> - 0.4)		0.7	2.4	ns
t <sub>F-VCC</sub>	I/O V <sub>CC</sub> Falltime (Output = I/O_V <sub>CC</sub> )	C <sub>I<sub>O</sub>V<sub>CC</sub></sub> = 15 pF	1.3 to 4.5	0.9 to (V <sub>CC</sub> - 0.4)		0.5	1.0	ns
t <sub>R-VL</sub>	I/O V <sub>L</sub> Risetime (Output = I/O_V <sub>L</sub> )	C <sub>I<sub>O</sub>V<sub>L</sub></sub> = 15 pF	1.3 to 4.5	0.9 to (V <sub>CC</sub> - 0.4)		1.0	3.8	ns
t <sub>F-VL</sub>	I/O V <sub>L</sub> Falltime (Output = I/O_V <sub>L</sub> )	C <sub>I<sub>O</sub>V<sub>L</sub></sub> = 15 pF	1.3 to 4.5	0.9 to (V <sub>CC</sub> - 0.4)		0.6	1.2	ns
Z <sub>O-VCC</sub>	I/O V <sub>CC</sub> One-Shot Output Impedance		1.3 to 4.5	0.9 to (V <sub>CC</sub> - 0.4)		30		Ω
Z <sub>O-VL</sub>	I/O V <sub>L</sub> One-Shot Output Impedance		1.3 to 4.5	0.9 to (V <sub>CC</sub> - 0.4)		30		Ω
t <sub>PD_VL-VCC</sub>	Propagation Delay (Output = I/O_V <sub>CC</sub> , t <sub>PHL</sub> , t <sub>PLH</sub> )	C <sub>I<sub>O</sub>V<sub>CC</sub></sub> = 15 pF	1.3 to 4.5	0.9 to (V <sub>CC</sub> - 0.4)		4.5	9.3	ns
t <sub>PD_VCC-VL</sub>	Propagation Delay (Output = I/O_V <sub>L</sub> , t <sub>PHL</sub> , t <sub>PLH</sub> )	C <sub>I<sub>O</sub>V<sub>L</sub></sub> = 15 pF	1.3 to 4.5	0.9 to (V <sub>CC</sub> - 0.4)		3.0	6.5	ns
t <sub>SK_VL-VCC</sub>	Channel-to-Channel Skew (Output = I/O_V <sub>CC</sub> )	C <sub>I<sub>O</sub>V<sub>CC</sub></sub> = 15 pF	1.3 to 4.5	0.9 to (V <sub>CC</sub> - 0.4)		0.2	0.3	nS
t <sub>SK_VCC-VL</sub>	Channel-to-Channel Skew (Output = I/O_V <sub>L</sub> )	C <sub>I<sub>O</sub>V<sub>CC</sub></sub> = 15 pF	1.3 to 4.5	0.9 to (V <sub>CC</sub> - 0.4)		0.2	0.3	nS
	Maximum Data Rate	(Output = I/O_V <sub>CC</sub> , C <sub>I<sub>O</sub>V<sub>CC</sub></sub> = 15 pF) (Output = I/O_V <sub>L</sub> , C <sub>I<sub>O</sub>V<sub>L</sub></sub> = 15 pF)	1.3 to 4.5	0.9 to (V <sub>CC</sub> - 0.4)	110			Mb/s
			> 2.2	> 1.8	140			

9. Normal test conditions are V<sub>EN</sub> = 0 V, C<sub>I<sub>O</sub>V<sub>CC</sub></sub> = 15 pF and C<sub>I<sub>O</sub>V<sub>L</sub></sub> = 15 pF, unless otherwise specified.

10. V<sub>CC</sub> is the supply voltage associated with the high voltage port, and V<sub>CC</sub> ranges from +1.3 V to 4.5 V under normal operating conditions.

11. V<sub>L</sub> is the supply voltage associated with the low voltage port. V<sub>L</sub> must be less than or equal to (V<sub>CC</sub> - 0.4) V during normal operation. However, during startup and shutdown conditions, V<sub>L</sub> can be greater than (V<sub>CC</sub> - 0.4) V.

12. Typical values are for V<sub>CC</sub> = +2.8 V, V<sub>L</sub> = +1.8 V and T<sub>A</sub> = +25°C. All units are production tested at T<sub>A</sub> = +25°C. Limits over the operating temperature range are guaranteed by design.

ENABLE / DISABLE TIME MEASUREMENTS

Symbol	Parameter	Test Conditions (Note 13)	V <sub>CC</sub> (V) (Note 14)	V <sub>L</sub> (V) (Note 15)	-40°C to +85°C			Unit
					Min	Typ (Note 16)	Max	
t <sub>EN-VCC</sub>	Turn-On Enable Time (Output = I/O_V <sub>CC</sub> , t <sub>pZH</sub> )	C <sub>IOVCC</sub> = 15 pF	1.3 to 4.5	0.9 to (V <sub>CC</sub> - 0.4)		130	180	ns
	Turn-On Enable Time (Output = I/O_V <sub>L</sub> , t <sub>pZL</sub> )	C <sub>IOVL</sub> = 15 pF	1.3 to 4.5	0.9 to (V <sub>CC</sub> - 0.4)		100	150	ns
t <sub>EN-VL</sub>	Turn-On Enable Time (Output = I/O_V <sub>L</sub> , t <sub>pZH</sub> )	C <sub>IOVCC</sub> = 15 pF	1.3 to 4.5	0.9 to (V <sub>CC</sub> - 0.4)		95	185	ns
	Turn-On Enable Time (Output = I/O_V <sub>L</sub> , t <sub>pZL</sub> )	C <sub>IOVL</sub> = 15 pF	1.3 to 4.5	0.9 to (V <sub>CC</sub> - 0.4)		70	110	ns
t <sub>DIS-VCC</sub>	Turn-Off Disable Time (Output = I/O_V <sub>CC</sub> , t <sub>pHZ</sub> )	C <sub>IOVCC</sub> = 15 pF	1.3 to 4.5	0.9 to (V <sub>CC</sub> - 0.4)		175	250	ns
	Propagation Delay (Output = I/O_V <sub>CC</sub> , t <sub>pLZ</sub> )	C <sub>IOVL</sub> = 15 pF	1.3 to 4.5	0.9 to (V <sub>CC</sub> - 0.4)		150	190	ns
t <sub>DIS-VL</sub>	Turn-Off Disable Time (Output = I/O_V <sub>L</sub> , t <sub>pHZ</sub> )	C <sub>IOVCC</sub> = 15 pF	1.3 to 4.5	0.9 to (V <sub>CC</sub> - 0.4)		180	250	ns
	Propagation Delay (Output = I/O_V <sub>L</sub> , t <sub>pLZ</sub> )	C <sub>IOVL</sub> = 15 pF	1.3 to 4.5	0.9 to (V <sub>CC</sub> - 0.4)		160	220	ns

- 13. Normal test conditions are V<sub>EN</sub> = 0 V, C<sub>IOVCC</sub> = 15 pF and C<sub>IOVL</sub> = 15 pF, unless otherwise specified.
- 14. V<sub>CC</sub> is the supply voltage associated with the high voltage port, and V<sub>CC</sub> ranges from +1.3 V to 4.5 V under normal operating conditions.
- 15. V<sub>L</sub> is the supply voltage associated with the low voltage port. V<sub>L</sub> must be less than or equal to (V<sub>CC</sub> - 0.4) V during normal operation. However, during startup and shutdown conditions, V<sub>L</sub> can be greater than (V<sub>CC</sub> - 0.4) V.
- 16. Typical values are for V<sub>CC</sub> = +2.8 V, V<sub>L</sub> = +1.8 V and T<sub>A</sub> = +25 °C. All units are production tested at T<sub>A</sub> = +25 °C. Limits over the operating temperature range are guaranteed by design.

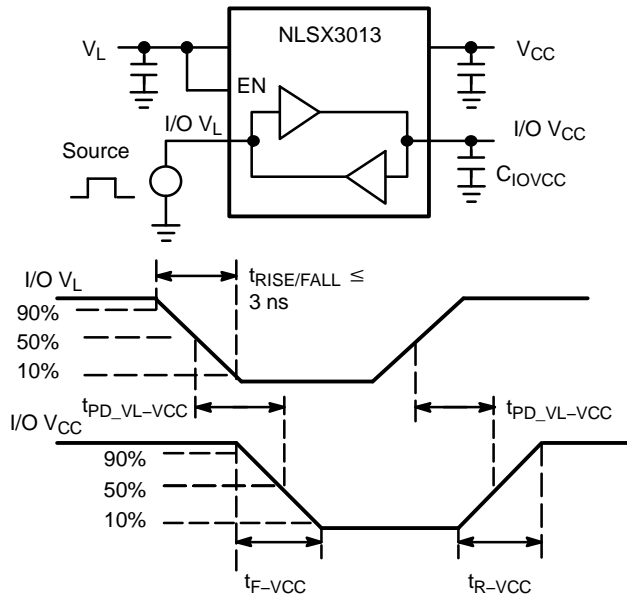


Figure 4. Driving I/O V<sub>L</sub> Test Circuit and Timing

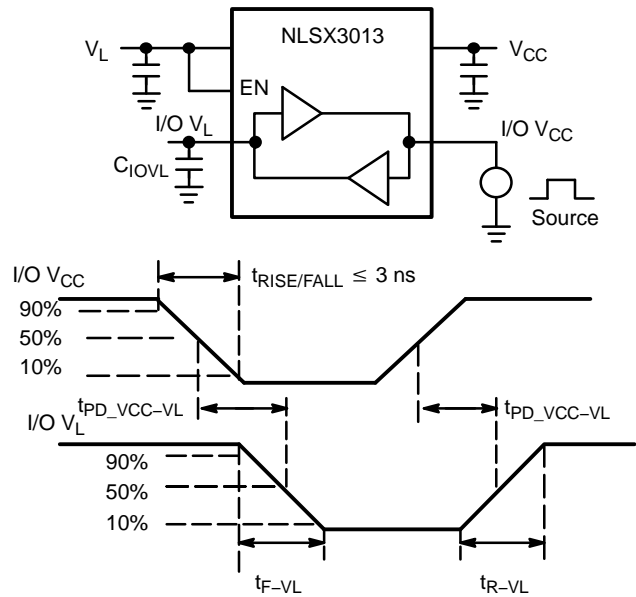
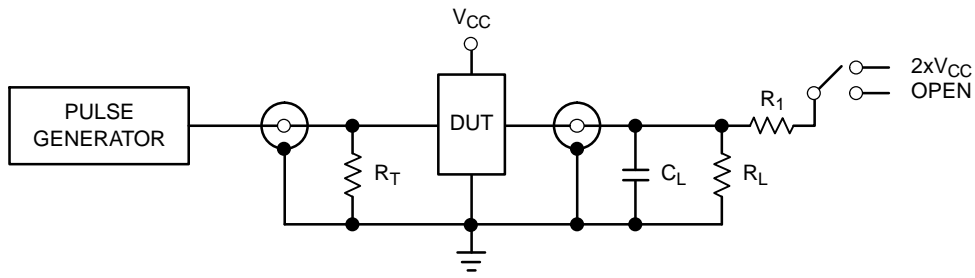


Figure 5. Driving I/O V<sub>CC</sub> Test Circuit and Timing

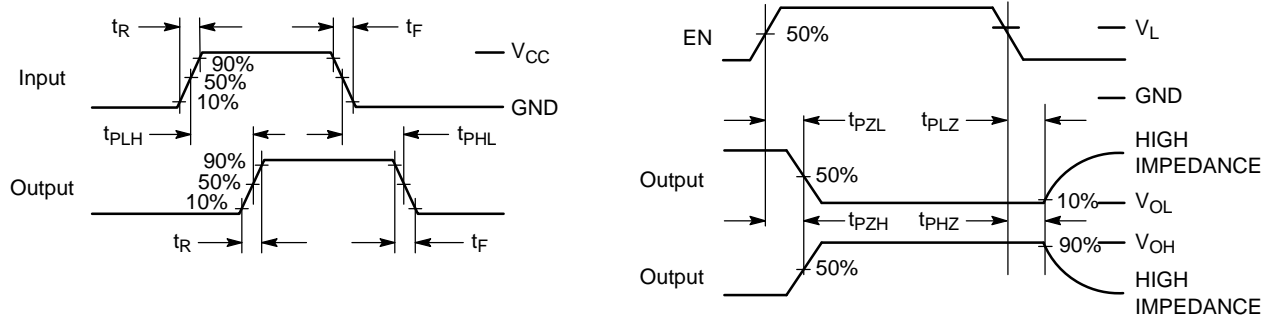
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Test	Switch
$t_{PZH}$ , $t_{PHZ}$	Open
$t_{PZL}$ , $t_{PLZ}$	$2 \times V_{CC}$

$C_L = 15 \text{ pF}$  or equivalent (Includes jig and probe capacitance)  
 $R_L = R_1 = 50 \text{ k}\Omega$  or equivalent  
 $R_T = Z_{OUT}$  of pulse generator (typically  $50 \Omega$ )

**Figure 6. Test Circuit for Enable/Disable Time Measurement**



**Figure 7. Timing Definitions for Propagation Delays and Enable/Disable Measurement**

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## IMPORTANT APPLICATIONS INFORMATION

### Level Translator Architecture

The NLSX3013 auto sense translator provides bi-directional voltage level shifting to transfer data in multiple supply voltage systems. This device has two supply voltages,  $V_L$  and  $V_{CC}$ , which set the logic levels on the input and output sides of the translator. When used to transfer data from the  $V_L$  to the  $V_{CC}$  ports, input signals referenced to the  $V_L$  supply are translated to output signals with a logic level matched to  $V_{CC}$ . In a similar manner, the  $V_{CC}$  to  $V_L$  translation shifts input signals with a logic level compatible to  $V_{CC}$  to an output signal matched to  $V_L$ .

The NLSX3013 consists of four bi-directional channels that independently determine the direction of the data flow without requiring a directional pin. The one-shot circuits are used to detect the rising or falling input signals. In addition, the one shots decrease the rise and fall time of the output signal for high-to-low and low-to-high transitions.

### Input Driver Requirements

Auto sense translators such as the NLSX3013 have a wide bandwidth, but a relatively small DC output current rating. The high bandwidth of the bi-directional I/O circuit is used to quickly transform from an input to an output driver and vice versa. The I/O ports have a modest DC current output specification so that the output driver can be over driven when data is sent to in the opposite direction.

For proper operation, the input driver to the auto sense translator should be capable of driving 20 mA of peak output current with an output impedance less than 25  $\Omega$ . The bi-directional configuration of the translator results in both input stages being active for a very short time period. Although the peak current from the input signal circuit is relatively large, the average current is small and consistent with a standard CMOS input stage.

### Output Load Requirements

The NLSX3013 is designed to drive CMOS inputs. Resistive pullup or pulldown loads of less than 50 k $\Omega$  should not be used with this device. The NLSX3373 or NLSX3378 open-drain auto sense translators are alternate translator options for an application such as the I<sup>2</sup>C bus that requires pullup resistors.

### Enable Input (EN)

The NLSX3013 has an Enable pin (EN) that provides tri-state operation at the I/O pins. Driving the Enable pin to a low logic level minimizes the power consumption of the device and drives the I/O  $V_{CC}$  and I/O  $V_L$  pins to a high impedance state. Normal translation operation occurs when the EN pin is equal to a logic high signal. The EN pin is referenced to the  $V_L$  supply and has Over-Voltage Tolerant (OVT) protection.

### Uni-Directional versus Bi-Directional Translation

The NLSX3013 can function as a non-inverting uni-directional translator. One advantage of using the translator as a uni-directional device is that each I/O pin can be configured as either an input or output. The configurable input or output feature is especially useful in applications such as SPI that use multiple uni-directional I/O lines to send data to and from a device. The flexible I/O port of the auto sense translator simplifies the trace connections on the PCB.

### Power Supply Guidelines

During normal operation, supply voltage  $V_L$  should be less than or equal to  $V_{CC}$ . The sequencing of the power supplies will not damage the device during the power up operation.

The enable pin should be used to enter the low current tri-state mode, rather than setting either the  $V_L$  or  $V_{CC}$  supplies to 0 V. The NLSX3013 will not be damaged if either  $V_L$  or  $V_{CC}$  is equal to 0 V while the other supply voltage is at a nominal operating value; however, the operation of the translator cannot be guaranteed during single supply operation.

For optimal performance, 0.01 to 0.1  $\mu$ F decoupling capacitors should be used on the  $V_L$  and  $V_{CC}$  power supply pins. Ceramic capacitors are a good design choice to filter and bypass any noise signals on the power supply voltage lines to the ground plane of the PCB. The noise immunity will be maximized by placing the capacitors as close as possible to the supply and ground pins, along with minimizing the PCB connection traces.

## ORDERING INFORMATION

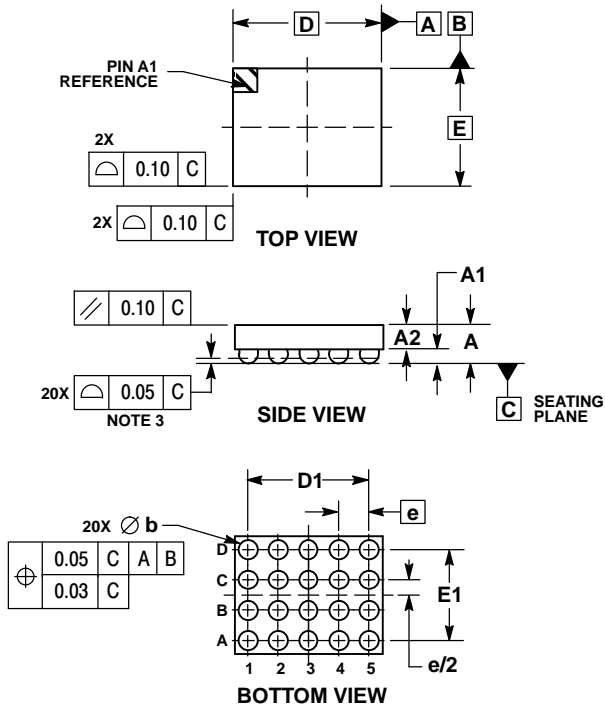
Device	Package	Shipping†
NLSX3013FCT1G	20 Pin Flip-Chip (Pb-Free)	3000 / Tape & Reel
NLSX3013BFCT1G	20 Pin Flip-Chip (Backside Laminate Coating) (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NLSX3013

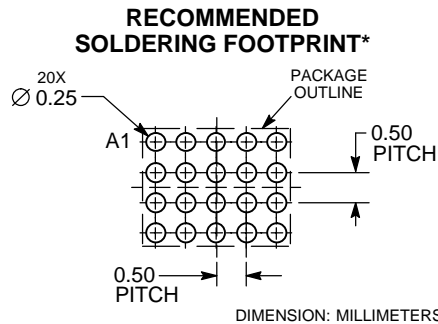
## PACKAGE DIMENSIONS

### 20 PIN FLIP-CHIP CSP, 2.54x2.03, 0.5P CASE 766AK ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

DIM	MILLIMETERS	
	MIN	MAX
A	---	0.66
A1	0.21	0.27
A2	0.33	0.39
b	0.29	0.34
D	2.54 BSC	
D1	2.00 BSC	
E	2.03 BSC	
E1	1.50 BSC	
e	0.50 BSC	



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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