





**■ TERMINALS DESCRIPTION**

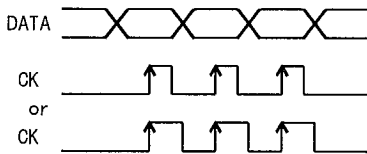
No.		SYMBOL	FUNCTIONS	No.		SYMBOL	FUNCTIONS	
DIP	DMP			DIP	DMP			
1	1	$V_{EE}$	Negative Voltage Supply	15	16	CK	Clock input	
2	2	L1	Analog switch input/output	16	17	DATA	Data input	
3	3	L2		17	19	R-COM3	R7, L8 Common	
4	4	L3		18	20	R8	Analog switch input/output	
5	5	L-COM1		19	21	R7		
6	6	L4	Analog switch input/output	20	22	R-COM2	R4, R5, R6 Common	
7	7	L5		21	23	R6	Analog switch input/output	
8	8	L6	22	24	R5			
9	9	L-COM2	L4, L5, L6 Common	23	25	R4	Analog switch input/output	
10	10	L7	Analog switch input/output	24	26	R-COM1		R1, R2, R3 Common
11	11	L8		25	27	R3		
12	12	L-COM3	L7, L8 Common	26	28	R2	Analog switch input/output	
13	14	ST	Chip enable	27	29	R1		
14	15	$V_{SS}$	GND	28	30	$V_{DD}$	Positive voltage supply	

**■ FUNCTIONAL DESCRIPTION**
**(1) Timing of DATA, CK, ST**

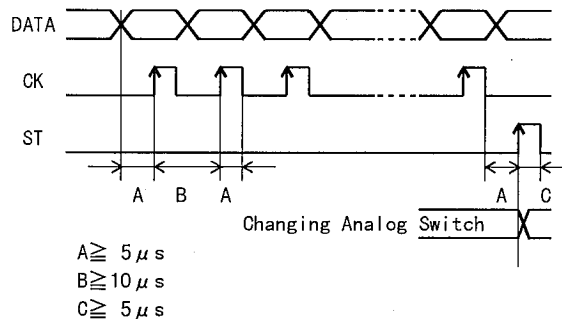
The Serial Input Data is input to internal shift register sequentially synchronized by clock signal rising edge input from CK terminal (100 kHz max.).

The Serial Input Data in the shift register is transferred to latch circuit and renew by synchronized rising edge of Chip enable signal input from ST terminal.

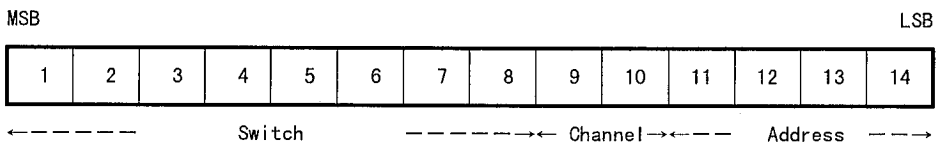
(Timing Chart)



(Detailed Timing)


**(2) Data Format**

The 14-bit serial data strings format from MSB to LSB are 8-bit analog switch control data, 2-bit right and left channel selection data and 4-bit address data.



**(Switch)**

Bit1 ~ bit8 select the analog switch ON and OFF    0: switch off  
 1: switch on

**(Channel)**

Bit9 and 10 select the channel.

bit9	bit10	CHANNEL
1	1	L and R
1	0	R only
0	1	L only

**(Address)**

Bit11 to 14 select the address. This address select is used for chip selection when this LSI is connected to the common bus line.

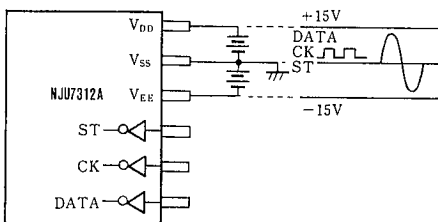
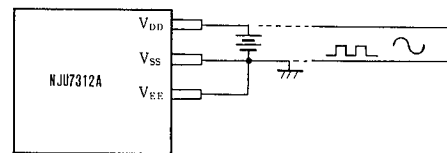
Type No.	bit11	bit12	bit13	bit14
NJU7311A	0	0	0	0
NJU7312A	1	0	0	0
NJU7313A	0	1	0	0

**(3) Supply Voltage**

The power supply of NJU7312A is divided into two portions of analog switch part and control part. The analog switch part operate by dual power supply (+ and -) and control part is operated by single power supply (+) only.

The analog switch part can be also operated by single power supply. In this case, the supply voltage should be half of dual supply operation mode.

Furthermore, the CK, DATA and ST terminals realize direct interface with 5V operated family because of its input threshold level is adjusted.

**Dual Power Supply (+ and -)**

**Single Power Supply (+)**


**■ ABSOLUTE MAXIMUM RATINGS**

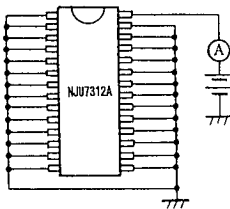
(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V_{DD} - V_{EE}$ $V_{DD} - V_{SS}$ $V_{EE} - V_{SS}$	34 +17 -17	V
Input Voltage	$V_{IN}$	$V_{SS}-0.3 \sim V_{DD}+0.3$	V
Power Dissipation	$P_D$	300	mW
Operating Temperature	$T_{opr}$	-30 ~ +75	°C
Storage Temperature	$T_{stg}$	-40 ~ +125	°C

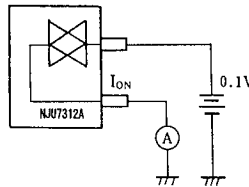
**■ ELECTRICAL CHARACTERISTICS**

 (V<sub>DD</sub>=+16V, V<sub>SS</sub>=0V, V<sub>EE</sub>=-16V, Ta=25°C)

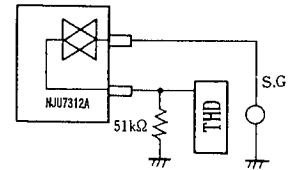
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage	$V_{DD}-V_{SS}$ $V_{EE}-V_{SS}$		8 -16		16 -8	V
Operating Current	$I_{DD}$	V <sub>DD</sub> =+16V, V <sub>EE</sub> =-16V, V <sub>SS</sub> =0V			3	mA
Back-Up Voltage	$V_B$		4		16	V
Back-Up Current	$I_B$	V <sub>DD</sub> =+4V, V <sub>SS</sub> =V <sub>EE</sub> =0V, Circ.1			10	μA
High-Level Input Voltage	$V_{IH}$	CK, DATA, ST Terminals	4		16	V
Low-Level Input Voltage	$V_{IL}$	CK, CATA, ST Terminals	0		1	V
Min. Operating Pulse Width	$t_{MIN}$		5			μS
Switch ON Resistance	$R_{ON}$	Circ.2		100	200	Ω
Total Harmonic Distortion	THD	f <sub>IN</sub> =20~20kHz, V <sub>IN</sub> =1V <sub>rms</sub> Circ.3		0.002	0.005	%

**■ MEASUREMENT CIRCUIT DIAGRAMS**


( Circ.1 )



( Circ.2 )



( Circ.3 )



## MEMO

[CAUTION]






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