



**THE DATASHEET OF
NCP1393BDR2G**



NCP1393B

High-Voltage Half-Bridge MOSFET Driver with Inbuilt Oscillator

The NCP1393B is a self-oscillating high voltage MOSFET driver primarily tailored for the applications using half-bridge topology. Due to its proprietary high-voltage technology, the driver accepts bulk voltages up to 600 V. Operating frequency of the driver can be adjusted from 25 kHz to 250 kHz using a single resistor. Adjustable brown-out protection assures correct bulk voltage operating range. An internal 100 ms PFC delay timer guarantees that the main downstream converter will be turned on in the time the bulk voltage is fully stabilized. The device provides fixed dead-time which helps to lower the shoot-through current.

Features

- Wide Operating Frequency Range – from 25 kHz to 250 kHz
- Minimum Frequency Adjust Accuracy $\pm 3\%$
- Fixed Dead Time – 0.6 μs
- Adjustable Brown-out Protection for a Simple PFC Association
- 100 ms PFC Delay Timer
- Latched Input for Severe Fault Conditions, e.g. Overtemperature or OVP
- Internal 16 V V_{CC} Clamp
- Low Startup Current of 50 μA Maximum
- 1 A / 0.5 A Peak Current Sink / Source Drive Capability
- Operation up to 600 V Bulk Voltage
- Internal Temperature Shutdown
- SOIC-8 Package
- These are Pb-Free Devices

Typical Applications

- Flat Panel Display Power Converters
- Low Cost Resonant SMPS
- High Power AC/DC Adapters for Notebooks
- Offline Battery Chargers
- Lamp Ballasts



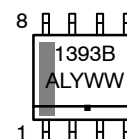
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<http://onsemi.com>

MARKING DIAGRAMS

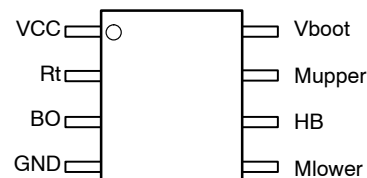


SOIC-8
CASE 751



A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
▪ = Pb-Free Package

PINOUT



ORDERING INFORMATION

Device	Package	Shipping†
NCP1393BDR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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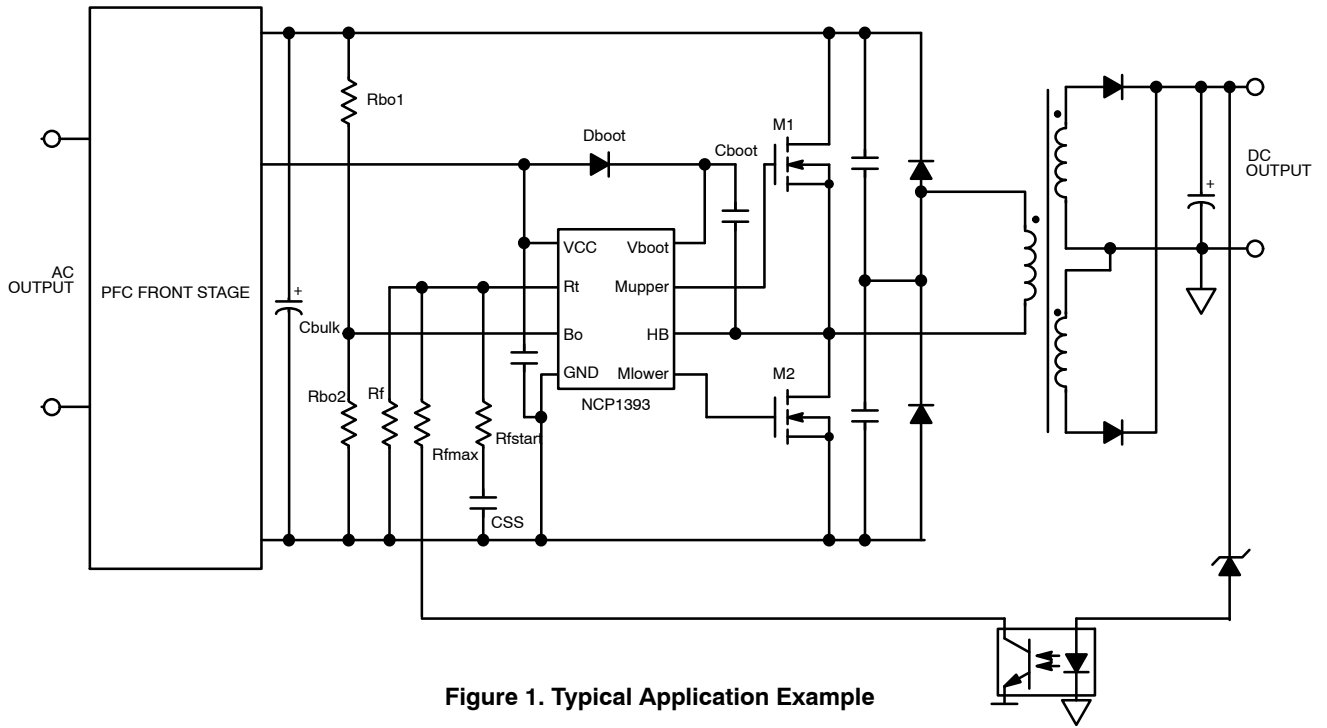


Figure 1. Typical Application Example

NCP1393B

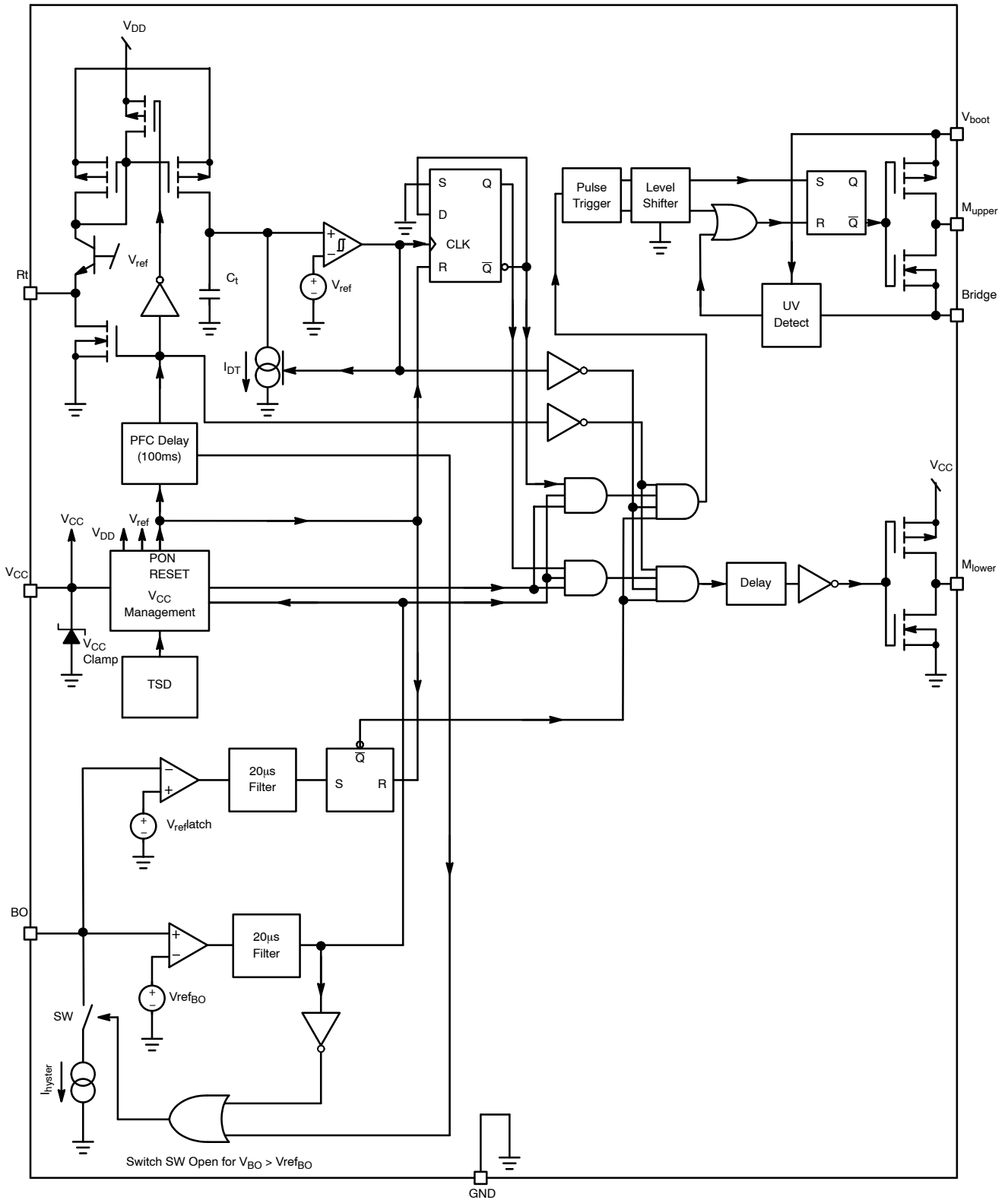


Figure 2. Internal Circuit Architecture

NCP1393B

PIN FUNCTION DESCRIPTION

Pin #	Pin Name	Function	Pin Description
1	V _{CC}	Supplies the Driver	The driver accepts up to 16 V (given by internal zener clamp).
2	Rt	Timing Resistor	Connecting a resistor between this pin and GND, sets the operating frequency
3	BO	Brown-Out	Detects low input voltage conditions. When brought above V _{latch} , it fully latches off the driver.
4	GND	IC Ground	–
5	M _{lower}	Low-Side Driver Output	Drives the lower side MOSFET.
6	HB	Half-Bridge Connection	Connects to the half-bridge output.
7	M _{upper}	High-Side Driver Output	Drives the higher side MOSFET.
8	V _{boot}	Bootstrap Pin	The floating supply terminal for the upper stage.

MAXIMUM RATINGS TABLE

Symbol	Rating	Value	Unit
V _{bridge}	High Voltage Bridge Pin – Pin 6	–1 to +600	V
V _{boot} – V _{bridge}	Floating Supply Voltage	0 to 20	V
VDRV_HI	High-Side Output Voltage	V _{bridge} – 0.3 to V _{boot} + 0.3	V
VDRV_LO	Low-Side Output Voltage	–0.3 to V _{CC} + 0.3	V
dV _{bridge} /dt	Allowable Output Slew Rate	± 50	V/ns
I _{CC}	Maximum Current that Can Flow into V _{CC} Pin (Pin 1), (Note 1)	20	mA
V _{Rt}	Rt Pin Voltage	–0.3 to 5	V
	Maximum Voltage, All Pins (Except Pins 4 and 5)	–0.3 to 10	V
R _{θJA}	Thermal Resistance Junction-to-Air, IC Soldered on 50 mm ² Cooper 35 μm	178	°C/W
R _{θJA}	Thermal Resistance Junction-to-Air, IC Soldered on 200 mm ² Cooper 35 μm	147	°C/W
	Storage Temperature Range	–60 to +150	°C
	ESD Capability, Human Body Model (All Pins Except Pins 1, 6, 7 and 8)	2	kV
	ESD Capability, Machine Model (All Pins Except Pins 1, 6, 7 and 8)	200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device contains internal zener clamp connected between V_{CC} and GND terminals. Current flowing into the V_{CC} pin has to be limited by an external resistor when device is supplied from supply which voltage is higher than V_{CCclamp} (16 V typically). The I_{CC} parameter is specified for V_{BO} = 0 V.

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ELECTRICAL CHARACTERISTICS (For typical values $T_J = 25^\circ\text{C}$, for min/max values $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, Max $T_J = 150^\circ\text{C}$, $V_{CC} = 12\text{ V}$, unless otherwise noted)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
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SUPPLY SECTION

Turn-On Threshold Level, V_{CC} Going Up	1	$V_{CC_{ON}}$	10	11	12	V
Minimum Operating Voltage after Turn-On	1	$V_{CC_{min}}$	8	9	10	V
Startup Voltage on the Floating Section	1	$V_{boot_{ON}}$	7.8	8.8	9.8	V
Cutoff Voltage on the Floating Section	1	$V_{boot_{min}}$	7	8	9	V
V_{CC} Level at which the Internal Logic gets Reset	1	$V_{CC_{reset}}$	-	6.5	-	V
Startup Current, $V_{CC} < V_{CC_{ON}}$, $0^\circ\text{C} \leq T_{amb} \leq +125^\circ\text{C}$	1	I_{CC}	-	-	50	μA
Startup Current, $V_{CC} < V_{CC_{ON}}$, $-40^\circ\text{C} \leq T_{amb} < 0^\circ\text{C}$	1	I_{CC}	-	-	65	μA
Internal IC Consumption, No Output Load on Pins 8/7 - 5/4, $F_{sw} = 100\text{ kHz}$	1	I_{CC1}	-	2.2	-	mA
Internal IC Consumption, 1 nF Output Load on Pins 8/7 - 5/4, $F_{sw} = 100\text{ kHz}$	1	I_{CC2}	-	3.4	-	mA
Consumption in Fault Mode (Drivers Disabled, $V_{CC} > V_{CC_{(min)}}$, $R_T = 3.5\text{ k}\Omega$)	1	I_{CC3}	-	2.56	-	mA
Consumption During PFC Delay Period, $0^\circ\text{C} \leq T_{amb} \leq +125^\circ\text{C}$		I_{CC4}	-	-	400	μA
Consumption During PFC Delay Period, $-40^\circ\text{C} \leq T_{amb} < 0^\circ\text{C}$		I_{CC4}	-	-	470	μA
Internal IC Consumption, No Output Load on Pin 8/7 $F_{WS} = 100\text{ kHz}$	8	I_{boot1}	-	0.3	-	mA
Internal IC Consumption, 1 nF Output Load on Pin 8/7 $F_{WS} = 100\text{ kHz}$	8	I_{boot2}	-	1.44	-	mA
Consumption in Fault Mode (Drivers Disabled, $V_{boot} > V_{boot_{min}}$)	8	I_{boot3}	-	0.1	-	mA
V_{CC} Zener Clamp Voltage @ 20 mA	1	$V_{CC_{clamp}}$	15.4	16	17.5	V

INTERNAL OSCILLATOR

Minimum Switching Frequency, $R_T = 35\text{ k}\Omega$ on Pin 2, $D_T = 600\text{ ns}$	2	$F_{SW\ min}$	24.25	25	25.75	kHz
Maximum Switching Frequency, $R_T = 3.5\text{ k}\Omega$ on Pin 2, $D_T = 600\text{ ns}$	2	$F_{SW\ max}$	208	245	282	kHz
Reference Voltage for all Current Generations	2	$V_{ref\ RT}$	3.33	3.5	3.67	V
Internal Resistance Discharging $C_{soft-start}$	2	$R_{t_{discharge}}$	-	500	-	Ω
Operating Duty Cycle Symmetry	5, 7	DC	48	50	52	%

NOTE: Maximum capacitance directly connected to Pin 2 must be under 100 pF.

DRIVE OUTPUT

Output Voltage Rise Time @ $CL = 1\text{ nF}$, 10-90% of Output Signal	5, 7	T_r	-	40	-	ns
Output Voltage Fall Time @ $CL = 1\text{ nF}$, 10-90% of Output Signal	5, 7	T_f	-	20	-	ns
Source Resistance	5, 7	R_{OH}	-	12	-	Ω
Sink Resistance	5, 7	R_{OL}	-	5	-	Ω
Dead-Time (Measured Between 50% of Rise and Fall Edge)	5, 7	T_{dead}	540	610	720	ns
Leakage Current on High Voltage Pins to GND (600 Vdc)	6, 7, 8	I_{HV_Leak}	-	-	5	μA

PROTECTION

Brown-Out Input Bias Current	3	$I_{BO_{bias}}$	-	0.01	-	μA
Brown-Out Level	3	V_{BO}	0.95	1	1.05	V
Hysteresis Current, $V_{pin3} < V_{BO}$	3	I_{BO}	15.6	18.2	20.7	μA
Latching Voltage on BO Pin	3	V_{latch}	1.9	2	2.1	V
Propagation Delay Before Drivers are Stopped	3	EN Delay	-	20	-	μs
Delay Before Any Driver Restart	-	PFC Delay	-	100	-	ms
Temperature Shutdown	-	TSD	140	-	-	$^\circ\text{C}$
Hysteresis	-	TSD_{hyste}	-	30	-	$^\circ\text{C}$

2. Maximum capacitance directly connected to Pin 2 must be under 100 pF.

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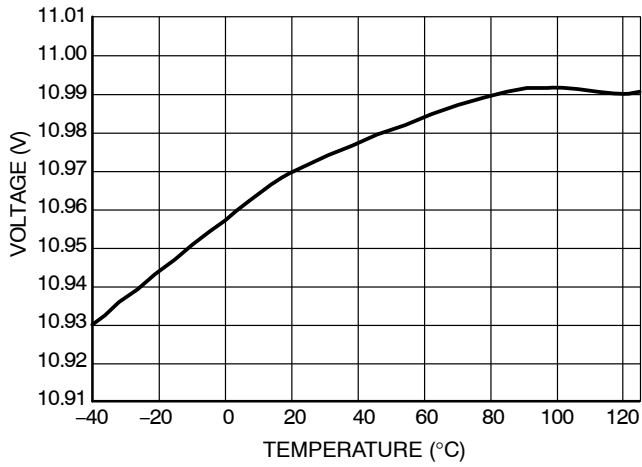


Figure 3. V_{CCon}

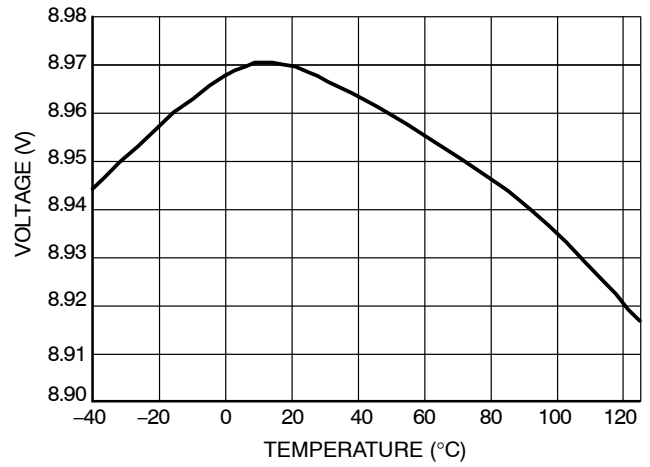


Figure 4. V_{CCmin}

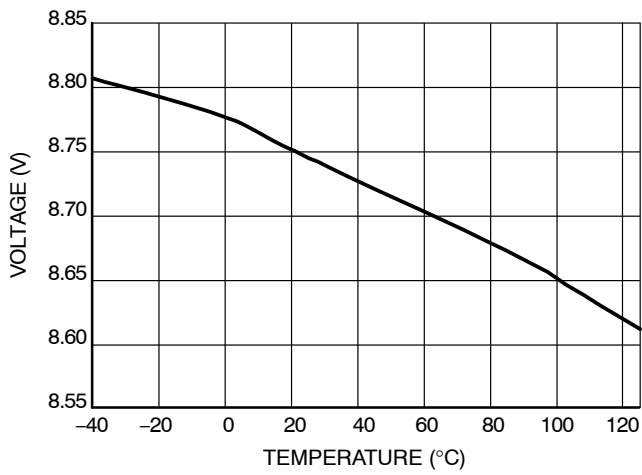


Figure 5. V_{BOOTon}

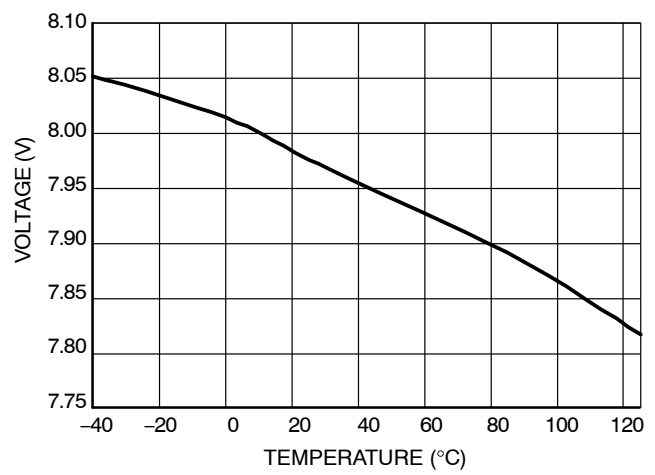


Figure 6. V_{BOOTmin}

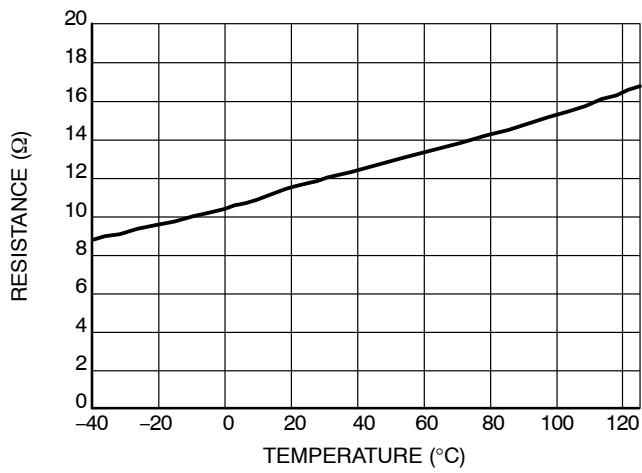


Figure 7. R_{OH}

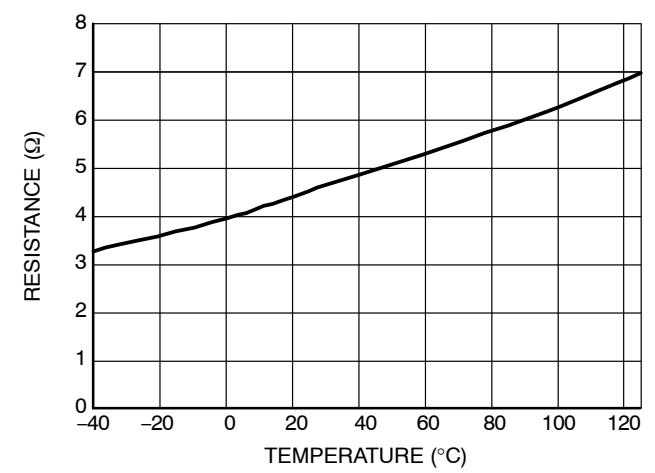


Figure 8. R_{OL}

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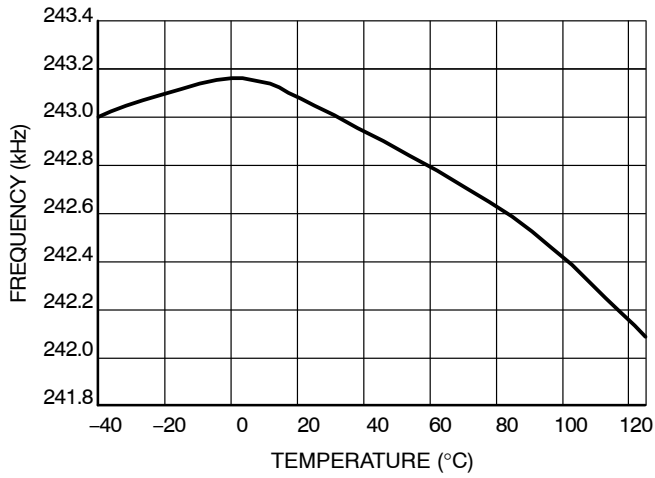


Figure 9. F_{swmax}

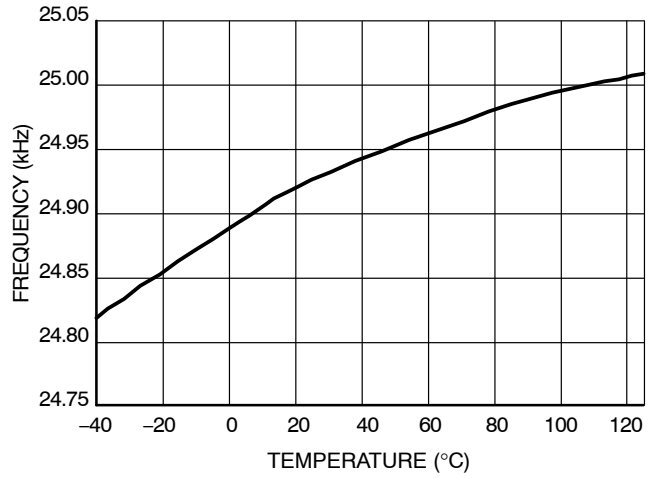


Figure 10. F_{swmin}

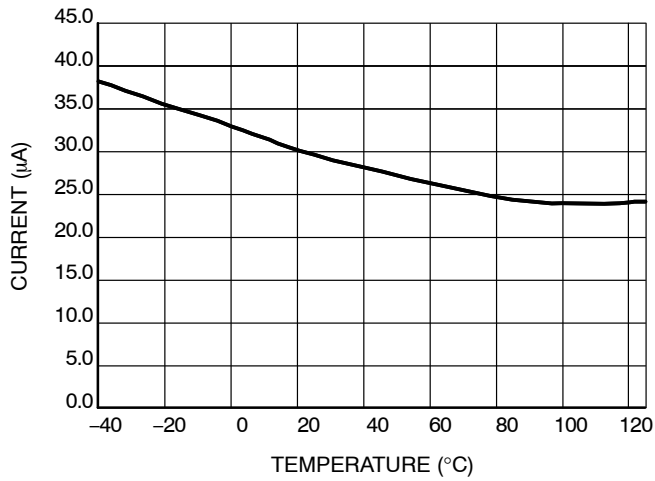


Figure 11. I_{cc_startup}

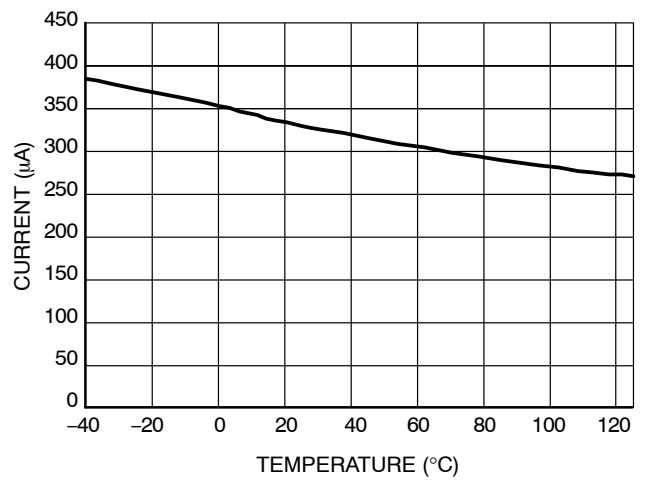


Figure 12. I_{cc4}

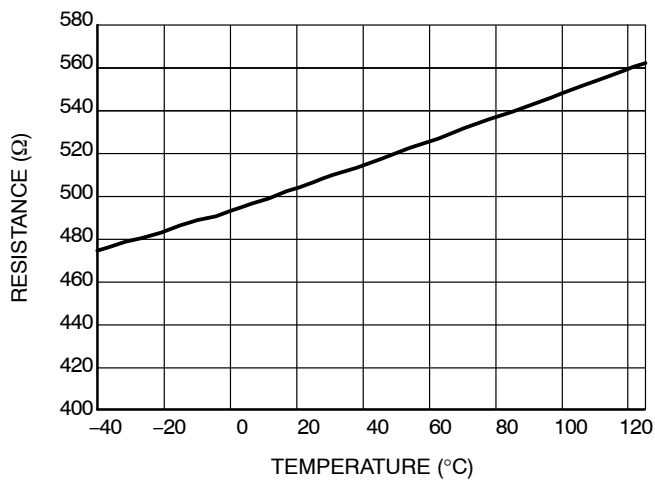


Figure 13. R_{t_discharge}

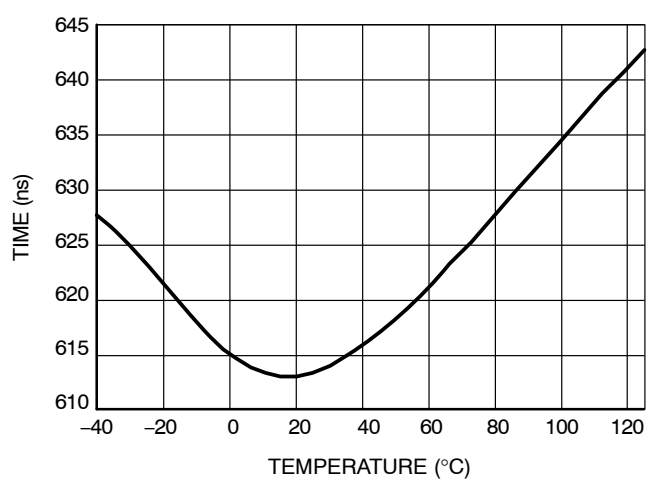


Figure 14. T_{dead}

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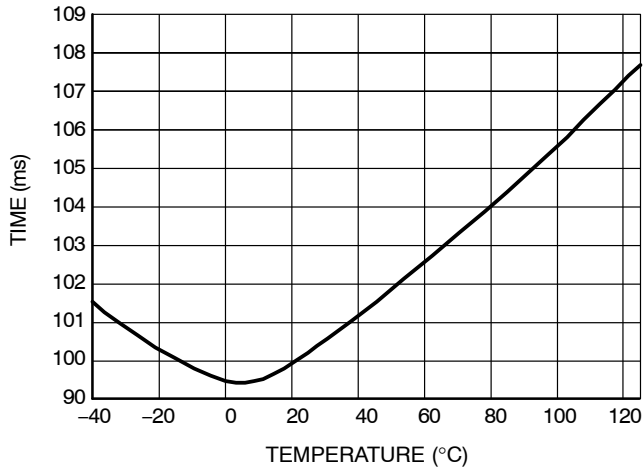


Figure 15. PFC_{delay}

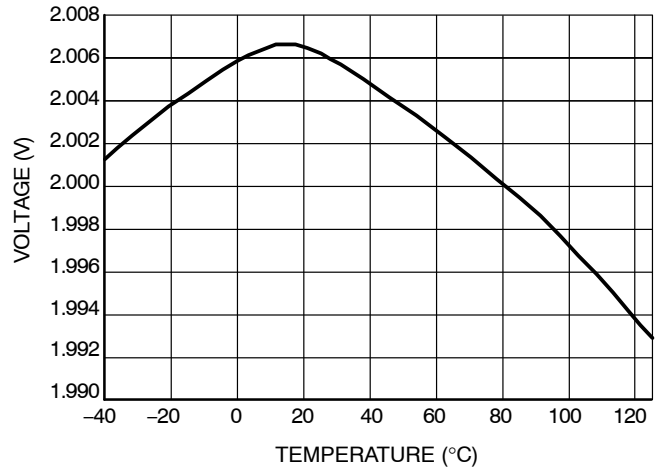


Figure 16. V_{LATCH}

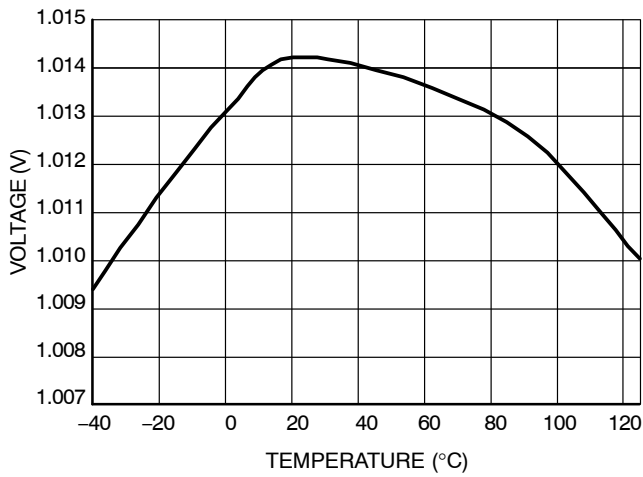


Figure 17. V_{BO}

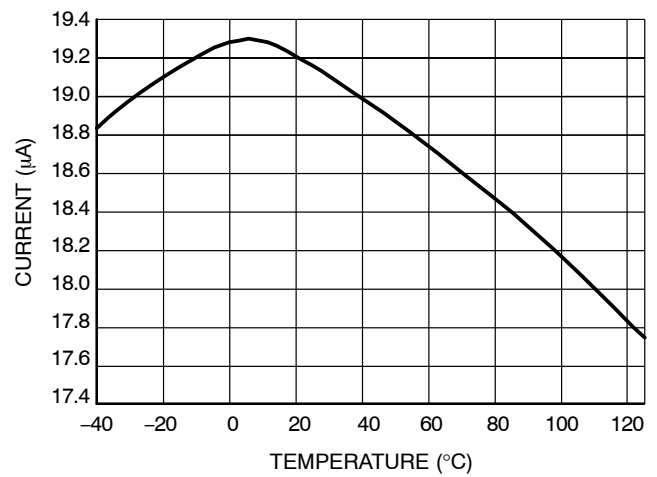


Figure 18. I_{BO}

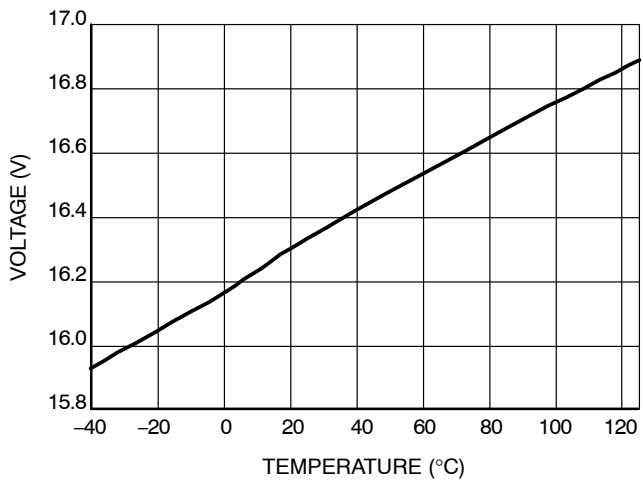


Figure 19. V_{CC_clamp}

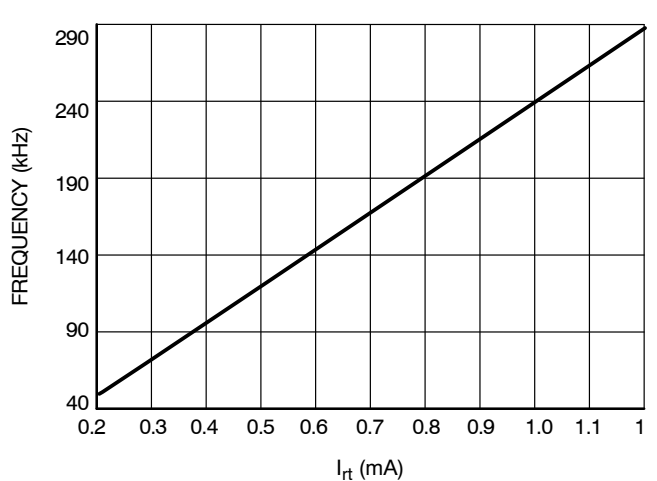


Figure 20. I_{rt} and Appropriate Frequency

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The internal timing capacitor C_t is charged by current which is proportional to the current flowing out from the R_t pin. The discharging current I_{DT} is applied when voltage on this capacitor reaches 2.5 V. The output drivers are disabled during discharge period so the dead time length is given by the discharge current sink capability. Discharge sink is disabled when voltage on the timing capacitor reaches zero and charging cycle starts again. The charging current and thus also whole oscillator is disabled during the PFC delay period to keep the IC consumption below 400 μ A.

This is valuable for applications that are supplied from auxiliary winding and V_{CC} capacitor is supposed to provide energy during PFC delay period.

For the resonant applications and light ballast applications it is necessary to adjust minimum operating frequency with high accuracy. The designer also needs to limit maximum operating and startup frequency. All these parameters can be adjusted using few external components connected to the R_t pin as depicted in Figure 22.

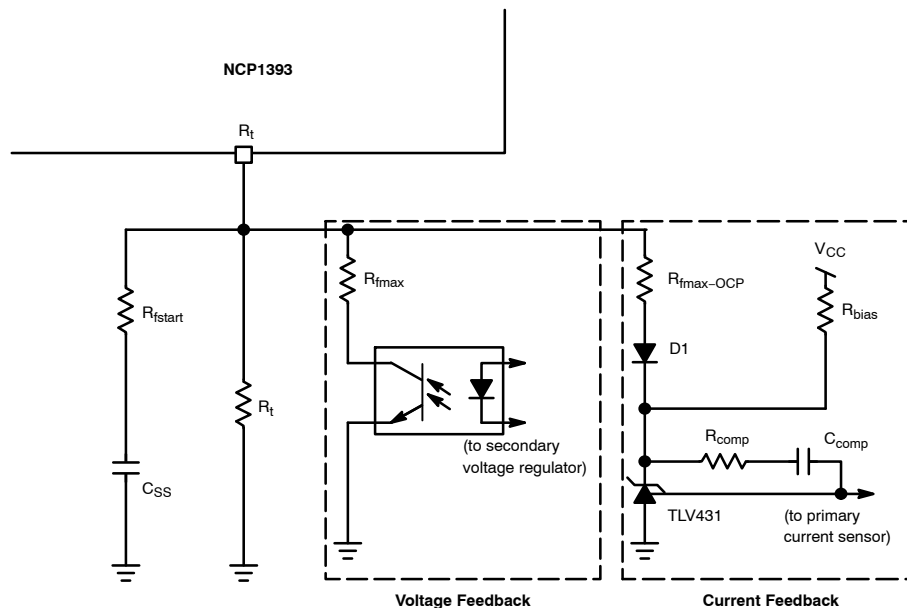


Figure 22. Typical R_t Pin Connection

The minimum switching frequency is given by the R_t resistor value. This frequency is reached if there is no optocoupler or current feedback action and soft start period has been already finished. The maximum switching frequency excursion is limited by the $R_{f_{max}}$ selection. Note that the F_{max} value is influenced by the optocoupler saturation voltage value. Resistor $R_{f_{start}}$ together with capacitor C_{SS} prepares the soft start period after PFC timer elapses. The R_t pin is grounded via an internal switch during the PFC delay period to assure that the soft start capacitor will be fully discharged via $R_{f_{start}}$ resistor.

There is a possibility to connect other control loops (like current control loop) to the R_t pin. The only one limitation lies in the R_t pin reference voltage which is $V_{ref_{R_t}} = 3.5$ V. Used regulator has to be capable to work with voltage lower than $V_{ref_{R_t}}$.

The TLV431 shunt regulator is used in the example from Figure 22 to prepare current feedback loop. Diode D1 is used to enable regulator biasing via resistor R_{bias} . Total saturation voltage of this solution is $1.25 + 0.6 = 1.85$ V for room temperature. Schottky diode will further decrease saturation voltage. $R_{f_{max}} - OCP$ resistor value, limits the maximum frequency that can be pushed by this regulation loop. This parameter is not temperature stable because of the D1 temperature drift.

Brown-Out Protection

The Brown-Out circuitry (BO) offers a way to protect the application from low DC input voltages. Below a given level, the controller blocks the output pulses, above it, it authorizes them. The internal circuitry, depicted by Figure 23, offers a way to observe the high-voltage (HV) rail.

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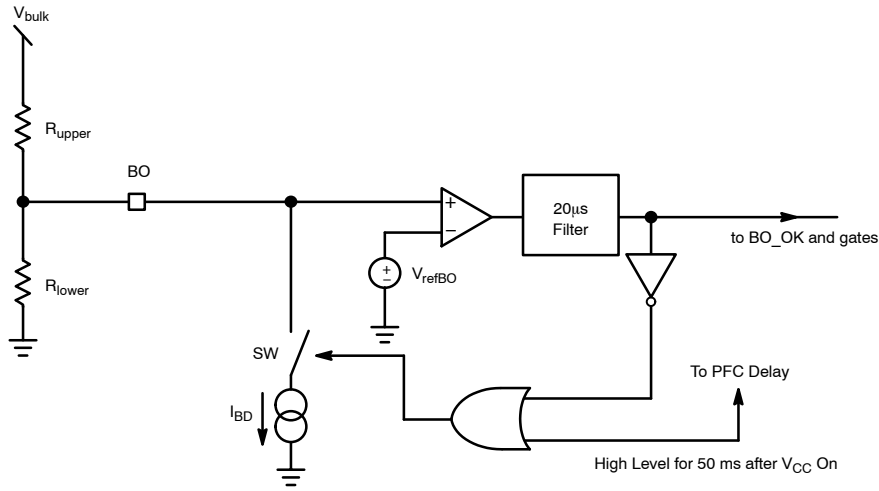


Figure 23. The internal Brown-Out Configuration with an Offset Current Sink

A resistive divider made of R_{upper} and R_{lower} , brings a portion of the HV rail on Pin 3. Below the turn-on level, the $18.2\ \mu\text{A}$ current sink (I_{BO}) is on. Therefore, the turn-on level is higher than the level given by the division ratio brought by the resistive divider. To the contrary, when the

internal BO_OK signal is high (PFC timer runs or M_{lower} and M_{upper} pulse), the I_{BO} sink is deactivated. As a result, it becomes possible to select the turn-on and turn-off levels via a few lines of algebra:

I_{BO} is ON

$$V_{ref_{BO}} = V_{bulk1} \cdot \frac{R_{lower}}{R_{lower} + R_{upper}} - I_{BO} \cdot \left(\frac{R_{lower} \cdot R_{upper}}{R_{lower} + R_{upper}} \right) \quad (\text{eq. 1})$$

I_{BO} is OFF

$$V_{ref_{BO}} = V_{bulk2} \cdot \frac{R_{lower}}{R_{lower} + R_{upper}} \quad (\text{eq. 2})$$

We can extract R_{lower} from Equation 2 and plug it into Equation 1, then solve for R_{upper} :

$$R_{lower} = V_{ref_{BO}} \cdot \frac{V_{bulk1} - V_{bulk2}}{I_{BO} \cdot (V_{bulk2} - V_{ref_{BO}})} \quad (\text{eq. 3})$$

$$R_{upper} = R_{lower} \cdot \frac{V_{bulk2} - V_{ref_{BO}}}{V_{ref_{BO}}} \quad (\text{eq. 4})$$

If we decide to turn-on our converter for V_{bulk1} equals 350 V and turn it off for V_{bulk2} equals 250 V, then for $I_{BO} = 18.2\ \mu\text{A}$ and $V_{ref_{BO}} = 1.0\ \text{V}$ we obtain:

$$R_{upper} = 5.494\ \text{M}\Omega$$

$$R_{lower} = 22.066\ \text{V}$$

The bridge power dissipation is $400^2 / 5.517\ \text{M}\Omega = 29\ \text{mW}$ when front-end PFC stage delivers 400 V. Figure 24 simulation result confirms our calculations.

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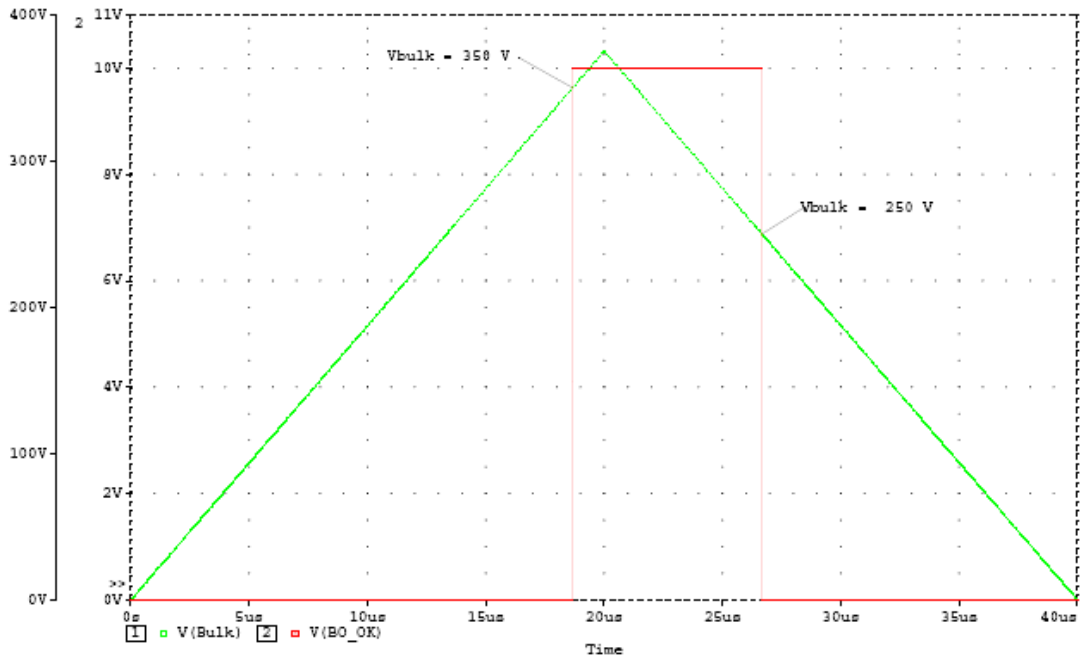


Figure 24. Simulation Results for 350/250 ON/OFF Brown-Out Levels

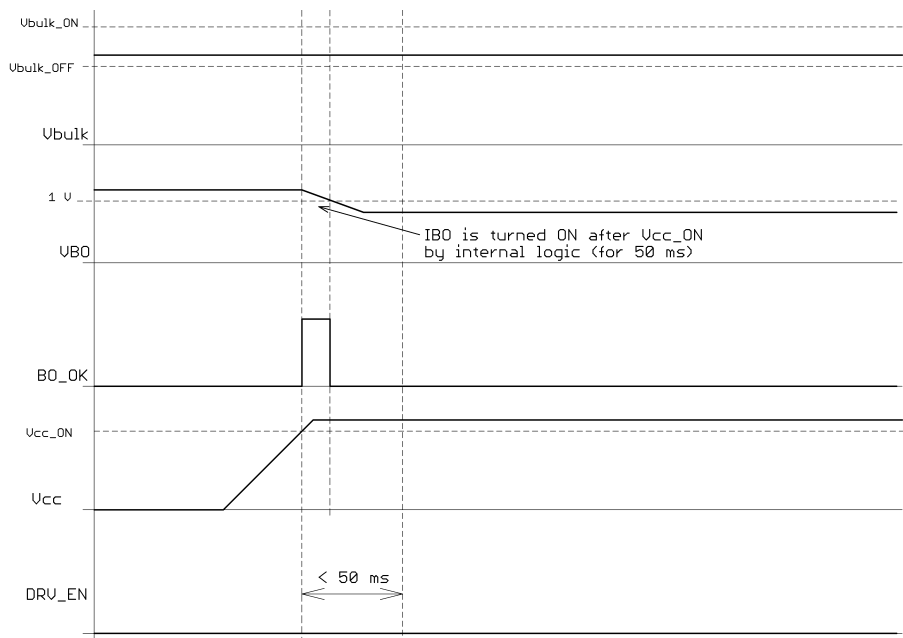


Figure 25. BO Input Functionality – $V_{bulk2} < V_{bulk} < V_{bulk1}$

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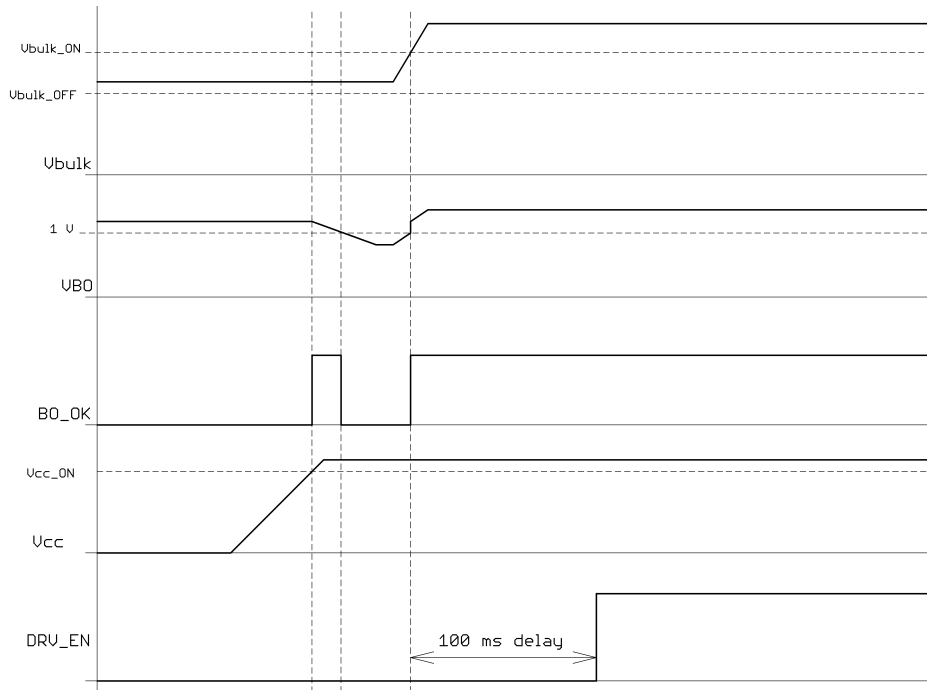


Figure 26. BO Input Functionality – $-V_{bulk2} < V_{bulk} < V_{bulk1}$, PFC Start Follows

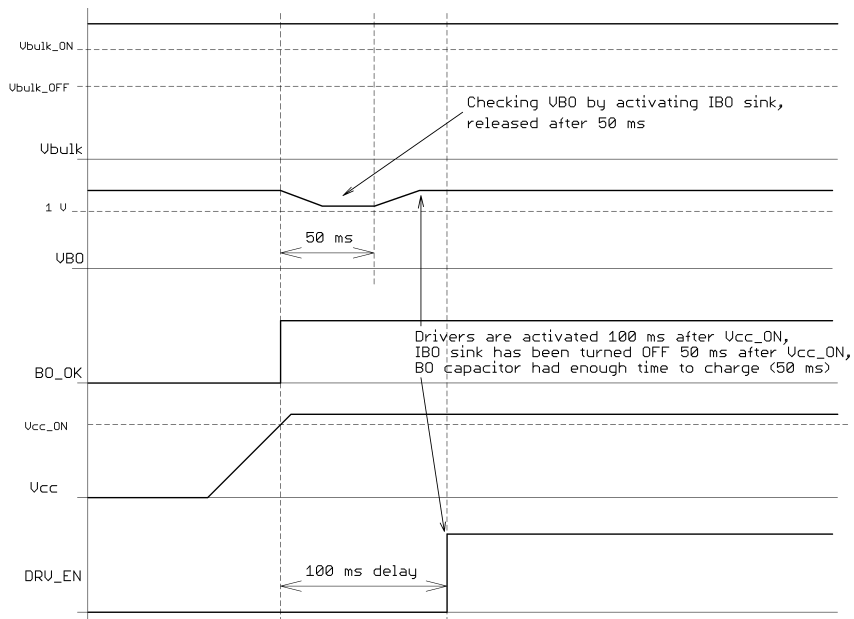


Figure 27. BO Input Functionality – $V_{bulk} > V_{bulk1}$

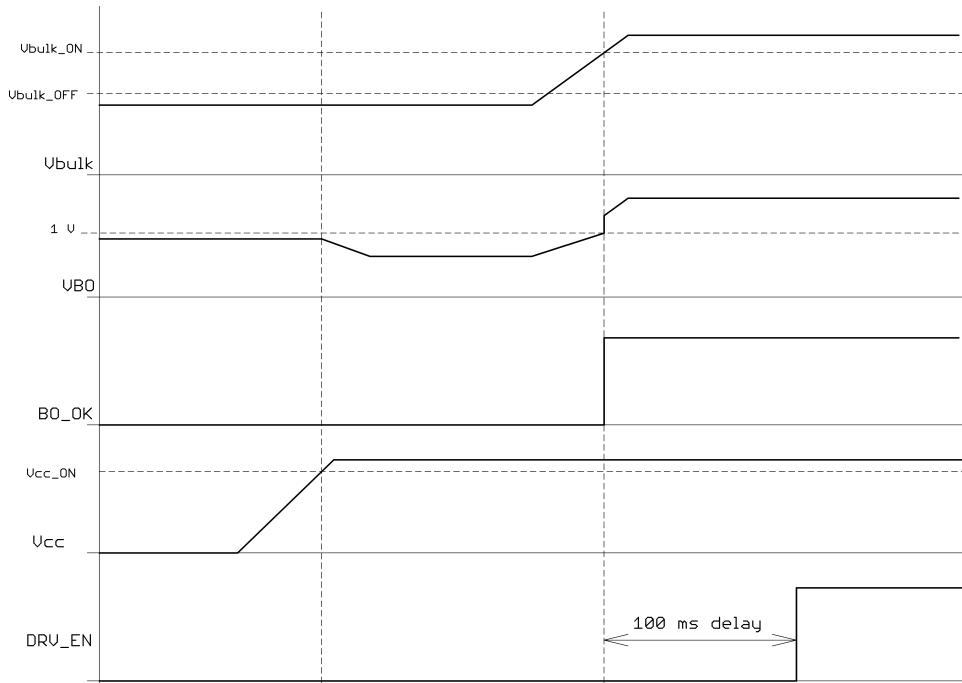


Figure 28. BO Input Functionality – $V_{bulk} < V_{bulk2}$, PFC Start Follows

The I_{BO} current sink is turned ON for 50 ms after any controller restart to let the BO input voltage stabilize (there can be connected big capacitor to the BO input and the I_{BO} is only 18.2 μA so it will take some time to discharge). Once the 50 ms one shoot pulse ends the BO comparator is supposed to either hold the I_{BO} sink turned ON (if the bulk voltage level is not sufficient) or let it turned OFF (if the bulk voltage is higher than V_{bulk1}). See Figures 25 through 28 for better understanding on how the BO input works.

Latched-Off Protection

There are some situations where the converter shall be fully turned-off and stay latched. This can happen in presence of an overvoltage (the feedback loop is drifting) or when an overtemperature is detected. Due to the addition of a comparator on the BO Pin, a simple external circuit can lift up this pin above V_{latch} (2 V typical) and permanently disable pulses. The V_{CC} needs to be cycled down below 6.5 V typically to reset the controller.

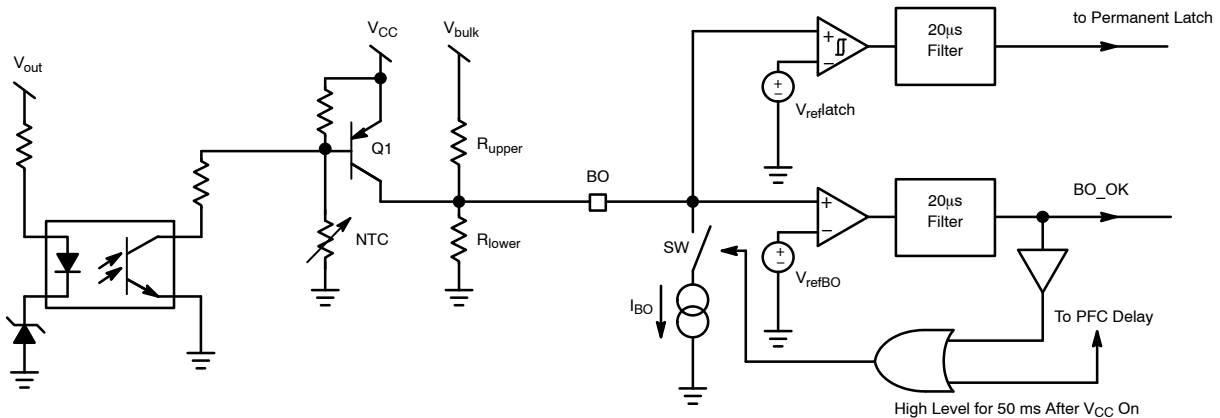


Figure 29. Adding a Comparator on the BO Pin Offers a Way to Latch-Off the Controller

On Figure 29, Q1 is blocked and does not bother the BO measurement as long as the NTC and the optocoupler are not activated. As soon as the secondary optocoupler senses an

OVP condition, or the NTC reacts to a high ambient temperature, Q1 base is brought to ground and the BO Pin goes up, permanently latching off the controller.

The High-Voltage Driver

Figure 30 shows the internal architecture of the high-voltage section. The device incorporates an upper

UVLO circuitry that makes sure enough V_{gs} is available for the upper side MOSFET. The V_{CC} for floating driver section

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is provided by C_{boot} capacitor that is refilled by external bootstrap diode.

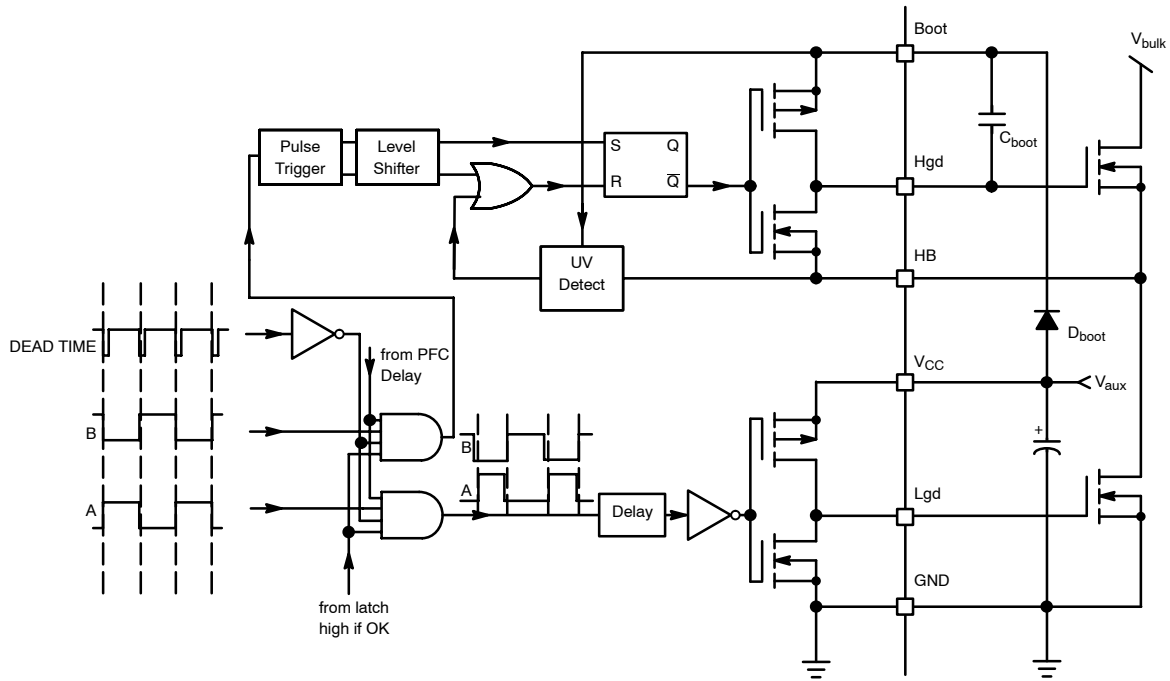


Figure 30. The Internal High-Voltage Section of the NCP1393

The A and B outputs are delivered by the internal logic, as depicted in block diagram. This logic is constructed in such a way that the M_{lower} driver starts to pulse first after any driver restart. The bootstrap capacitor is thus charged during first pulse. A delay is inserted in the lower rail to ensure good

matching between these propagating signals. As stated in the maximum rating section, the floating portion can go up to 600 Vdc and makes the IC perfectly suitable for offline applications featuring a 400 V PFC front-end stage.

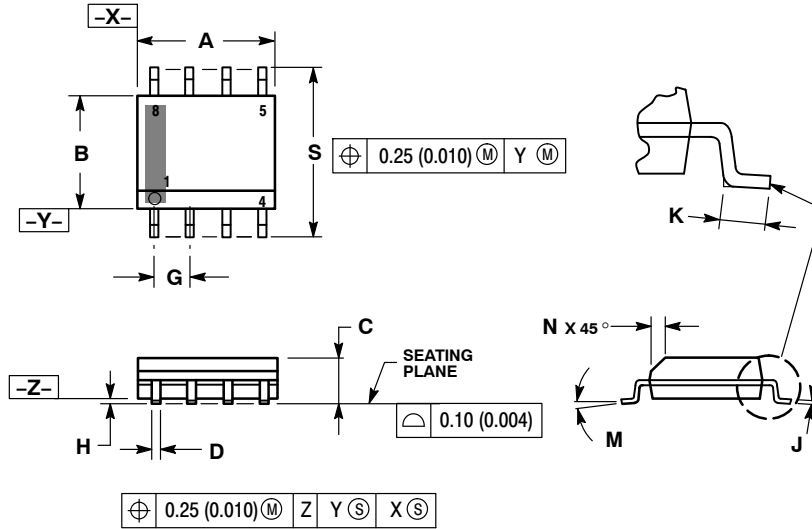
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

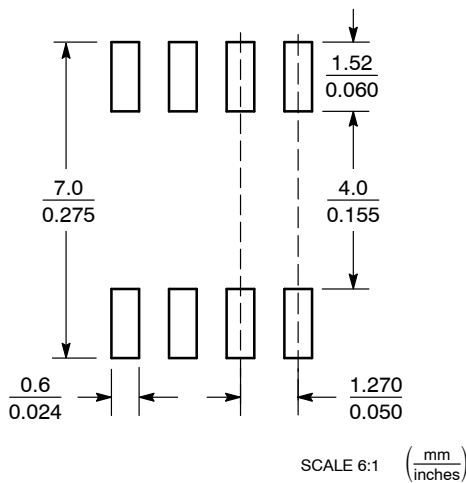
DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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ISSUE AK

DATE 16 FEB 2011

- | | | | |
|---|--|--|--|
| <p>STYLE 1:
 PIN 1. EMITTER
 2. COLLECTOR
 3. COLLECTOR
 4. EMITTER
 5. EMITTER
 6. BASE
 7. BASE
 8. EMITTER</p> | <p>STYLE 2:
 PIN 1. COLLECTOR, DIE, #1
 2. COLLECTOR, #1
 3. COLLECTOR, #2
 4. COLLECTOR, #2
 5. BASE, #2
 6. EMITTER, #2
 7. BASE, #1
 8. EMITTER, #1</p> | <p>STYLE 3:
 PIN 1. DRAIN, DIE #1
 2. DRAIN, #1
 3. DRAIN, #2
 4. DRAIN, #2
 5. GATE, #2
 6. SOURCE, #2
 7. GATE, #1
 8. SOURCE, #1</p> | <p>STYLE 4:
 PIN 1. ANODE
 2. ANODE
 3. ANODE
 4. ANODE
 5. ANODE
 6. ANODE
 7. ANODE
 8. COMMON CATHODE</p> |
| <p>STYLE 5:
 PIN 1. DRAIN
 2. DRAIN
 3. DRAIN
 4. DRAIN
 5. GATE
 6. GATE
 7. SOURCE
 8. SOURCE</p> | <p>STYLE 6:
 PIN 1. SOURCE
 2. DRAIN
 3. DRAIN
 4. SOURCE
 5. SOURCE
 6. GATE
 7. GATE
 8. SOURCE</p> | <p>STYLE 7:
 PIN 1. INPUT
 2. EXTERNAL BYPASS
 3. THIRD STAGE SOURCE
 4. GROUND
 5. DRAIN
 6. GATE 3
 7. SECOND STAGE Vd
 8. FIRST STAGE Vd</p> | <p>STYLE 8:
 PIN 1. COLLECTOR, DIE #1
 2. BASE, #1
 3. BASE, #2
 4. COLLECTOR, #2
 5. COLLECTOR, #2
 6. EMITTER, #2
 7. EMITTER, #1
 8. COLLECTOR, #1</p> |
| <p>STYLE 9:
 PIN 1. EMITTER, COMMON
 2. COLLECTOR, DIE #1
 3. COLLECTOR, DIE #2
 4. EMITTER, COMMON
 5. EMITTER, COMMON
 6. BASE, DIE #2
 7. BASE, DIE #1
 8. EMITTER, COMMON</p> | <p>STYLE 10:
 PIN 1. GROUND
 2. BIAS 1
 3. OUTPUT
 4. GROUND
 5. GROUND
 6. BIAS 2
 7. INPUT
 8. GROUND</p> | <p>STYLE 11:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. DRAIN 2
 7. DRAIN 1
 8. DRAIN 1</p> | <p>STYLE 12:
 PIN 1. SOURCE
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 13:
 PIN 1. N.C.
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> | <p>STYLE 14:
 PIN 1. N-SOURCE
 2. N-GATE
 3. P-SOURCE
 4. P-GATE
 5. P-DRAIN
 6. P-DRAIN
 7. N-DRAIN
 8. N-DRAIN</p> | <p>STYLE 15:
 PIN 1. ANODE 1
 2. ANODE 1
 3. ANODE 1
 4. ANODE 1
 5. CATHODE, COMMON
 6. CATHODE, COMMON
 7. CATHODE, COMMON
 8. CATHODE, COMMON</p> | <p>STYLE 16:
 PIN 1. EMITTER, DIE #1
 2. BASE, DIE #1
 3. EMITTER, DIE #2
 4. BASE, DIE #2
 5. COLLECTOR, DIE #2
 6. COLLECTOR, DIE #2
 7. COLLECTOR, DIE #1
 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:
 PIN 1. VCC
 2. V2OUT
 3. V1OUT
 4. TXE
 5. RXE
 6. VEE
 7. GND
 8. ACC</p> | <p>STYLE 18:
 PIN 1. ANODE
 2. ANODE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. CATHODE
 8. CATHODE</p> | <p>STYLE 19:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. MIRROR 2
 7. DRAIN 1
 8. MIRROR 1</p> | <p>STYLE 20:
 PIN 1. SOURCE (N)
 2. GATE (N)
 3. SOURCE (P)
 4. GATE (P)
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 21:
 PIN 1. CATHODE 1
 2. CATHODE 2
 3. CATHODE 3
 4. CATHODE 4
 5. CATHODE 5
 6. COMMON ANODE
 7. COMMON ANODE
 8. CATHODE 6</p> | <p>STYLE 22:
 PIN 1. I/O LINE 1
 2. COMMON CATHODE/VCC
 3. COMMON CATHODE/VCC
 4. I/O LINE 3
 5. COMMON ANODE/GND
 6. I/O LINE 4
 7. I/O LINE 5
 8. COMMON ANODE/GND</p> | <p>STYLE 23:
 PIN 1. LINE 1 IN
 2. COMMON ANODE/GND
 3. COMMON ANODE/GND
 4. LINE 2 IN
 5. LINE 2 OUT
 6. COMMON ANODE/GND
 7. COMMON ANODE/GND
 8. LINE 1 OUT</p> | <p>STYLE 24:
 PIN 1. BASE
 2. EMITTER
 3. COLLECTOR/ANODE
 4. COLLECTOR/ANODE
 5. CATHODE
 6. CATHODE
 7. COLLECTOR/ANODE
 8. COLLECTOR/ANODE</p> |
| <p>STYLE 25:
 PIN 1. VIN
 2. N/C
 3. REXT
 4. GND
 5. IOUT
 6. IOUT
 7. IOUT
 8. IOUT</p> | <p>STYLE 26:
 PIN 1. GND
 2. dv/dt
 3. ENABLE
 4. ILIMIT
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. VCC</p> | <p>STYLE 27:
 PIN 1. ILIMIT
 2. OVLO
 3. UVLO
 4. INPUT+
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. DRAIN</p> | <p>STYLE 28:
 PIN 1. SW_TO_GND
 2. DASIC_OFF
 3. DASIC_SW_DET
 4. GND
 5. V_MON
 6. VBULK
 7. VBULK
 8. VIN</p> |
| <p>STYLE 29:
 PIN 1. BASE, DIE #1
 2. EMITTER, #1
 3. BASE, #2
 4. EMITTER, #2
 5. COLLECTOR, #2
 6. COLLECTOR, #2
 7. COLLECTOR, #1
 8. COLLECTOR, #1</p> | <p>STYLE 30:
 PIN 1. DRAIN 1
 2. DRAIN 1
 3. GATE 2
 4. SOURCE 2
 5. SOURCE 1/DRAIN 2
 6. SOURCE 1/DRAIN 2
 7. SOURCE 1/DRAIN 2
 8. GATE 1</p> | | |

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