



**THE DATASHEET OF  
NC7SZ373P6X**



# TinyLogic UHS D-Type Latch with 3-STATE Output NC7SZ373

## Description

The NC7SZ373 is a single positive edge-triggered D-type CMOS Latch with 3-STATE output from onsemi's Ultra High Speed Series of TinyLogic in the space saving SC70 6-lead package. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad  $V_{CC}$  operating range. The device is specified to operate over the 1.65 V to 5.5 V  $V_{CC}$  range. The inputs and output are high impedance when  $V_{CC}$  is 0 V. Inputs tolerate voltages up to 5.5 V independent of  $V_{CC}$  operating voltage. The latch appears transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. The output tolerates voltages above  $V_{CC}$  in the 3-STATE condition.

## Features

- Space Saving SC-88 6-Lead Package
- Ultra Small MicroPak™ Leadless Package
- Ultra High Speed:  $t_{PD} = 2.6$  ns Typ into 50 pF at 5 V  $V_{CC}$
- High Output Drive:  $\pm 24$  mA at 3 V  $V_{CC}$
- Broad  $V_{CC}$  Operating Range: 1.65 V to 5.5 V
- Matches the Performance of LCX when Operated at 3.3 V  $V_{CC}$
- Power Down High Impedance Inputs / Output
- Overvoltage Tolerant Inputs Facilitate 5 V to 3 V Translation
- Patented Noise / EMI Reduction Circuitry Implemented
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

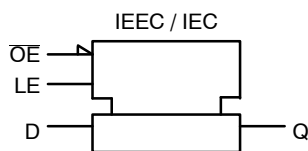
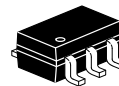
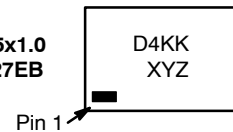


Figure 1. Logic Symbol

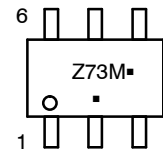
## MARKING DIAGRAMS



SIP6 1.45x1.0  
CASE 127EB



SC-88  
CASE 419B-02



- D4, Z73 = Specific Device Code
- KK = 2-Digit Lot Run Traceability Code
- XY = 2-Digit Date Code Format
- Z = Assembly Plant Code
- M = Date Code\*
- = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation and/or position may vary depending upon manufacturing location.

## ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 7 of this data sheet.

Connection Diagrams

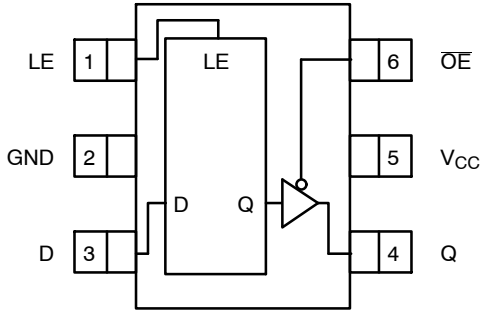


Figure 2. SC-88 (Top View)

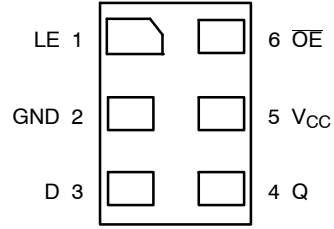
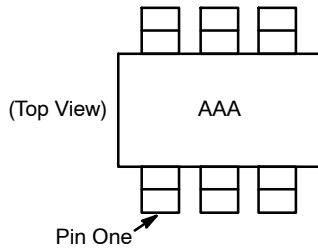


Figure 4. MicroPak (Top Through View)



AAA = Product Code Top Mark – see ordering code

NOTE: Orientation of Top Mark determines Pin One location.  
Read the top product code mark left to right, Pin One is the lower left pin (see diagram).

Figure 3. Pin 1 Orientation

PIN DESCRIPTIONS

Pin Name	Description
D	Data Input
CP	Latch Enable Input
OE	Output Enable Input
Q	Latch Output

FUNCTION TABLE

Inputs			Output
LE	D	OE	Q
H	L	L	L
H	H	L	H
L	X	L	Q <sub>n-1</sub>
X	X	H	Z

H = HIGH Logic Level                      X = Immaterial  
L = LOW Logic Level                        Z = HIGH Impedance  
Q<sub>n-1</sub> = Previous state prior to HIGH-to-LOW transition of latch enable

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## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V <sub>CC</sub>	Supply Voltage		-0.5	+6.5	V
V <sub>IN</sub>	DC Input Voltage		-0.5	+6.5	V
V <sub>OUT</sub>	DC Output Voltage		-0.5	+6.5	V
I <sub>IK</sub>	DC Input Diode Current	V <sub>IN</sub> < 0 V	-	-50	mA
I <sub>OK</sub>	DC Output Diode Current	V <sub>OUT</sub> < 0 V	-	-50	mA
I <sub>OUT</sub>	DC Output Source / Sink Current		-	±50	mA
I <sub>CC</sub> / I <sub>GND</sub>	DC V <sub>CC</sub> / GND Current		-	±50	mA
T <sub>STG</sub>	Storage Temperature Range		-65	+150	°C
T <sub>J</sub>	Junction Temperature under Bias		-	150	°C
T <sub>L</sub>	Junction Lead Temperature (Soldering, 10 Seconds)		-	260	°C
P <sub>D</sub>	Power Dissipation in Still Air	SC-88	-	332	mW
		MicroPak	-	812	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	Supply Voltage Operating		1.65	5.5	V
	Supply Voltage Data Retention		1.5	5.5	
V <sub>IN</sub>	Input Voltage		0	5.5	V
V <sub>OUT</sub>	Output Voltage	Active State	0	V <sub>CC</sub>	V
		3-STATE	0	5.5	V
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time	V <sub>CC</sub> = 1.8 V, 2.5 V ±0.2 V	0	20	ns/V
		V <sub>CC</sub> = 3.3 V ±0.3 V	0	10	
		V <sub>CC</sub> = 5.5 V ±0.5 V	0	5	
T <sub>A</sub>	Operating Temperature		-40	+85	°C
θ <sub>JA</sub>	Thermal Resistance	SC-88	-	377	°C/W
		MicroPak	-	154	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. Unused inputs must be held HIGH or LOW. They may not float.

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## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions		T <sub>A</sub> = +25°C			T <sub>A</sub> = -40 to +85°C		Unit
					Min	Typ	Max	Min	Max	
V <sub>IH</sub>	HIGH Level Control Input Voltage	1.65 to 1.95			0.65 V <sub>CC</sub>	-	-	0.65 V <sub>CC</sub>	-	V
		2.3 to 5.5			0.7 V <sub>CC</sub>	-	-	0.7 V <sub>CC</sub>	-	
V <sub>IL</sub>	LOW Level Control Input Voltage	1.65 to 1.95			-	-	0.35 V <sub>CC</sub>	-	0.35 V <sub>CC</sub>	V
		2.3 to 5.5			-	-	0.3 V <sub>CC</sub>	-	0.3 V <sub>CC</sub>	
V <sub>OH</sub>	HIGH Level Control Output Voltage	1.65	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -100 μA	1.55	1.65	-	1.55	-	V
		1.8			1.7	1.8	-	1.7	-	
		2.3			2.2	2.3	-	2.2	-	
		3.0			2.9	3.0	-	2.9	-	
		4.5			4.4	4.5	-	4.4	-	
		1.65		I <sub>OH</sub> = -4 mA	1.24	1.52	-	1.29	-	
		2.3		I <sub>OH</sub> = -8 mA	1.9	2.15	-	1.9	-	
		3.0		I <sub>OH</sub> = -16 mA	2.4	2.8	-	2.4	-	
		3.0		I <sub>OH</sub> = -24 mA	2.3	2.68	-	2.3	-	
		4.5		I <sub>OH</sub> = -32 mA	3.8	4.2	-	3.8	-	
V <sub>OL</sub>	LOW Level Control Output Voltage	1.65	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 100 μA	-	0.0	0.08	-	0.0	V
		1.8			-	0.0	0.1	-	0.1	
		2.3			-	0.0	0.1	-	0.1	
		3.0			-	0.0	0.1	-	0.1	
		4.5			-	0.0	0.1	-	0.1	
		1.65		I <sub>OL</sub> = 4 mA	-	0.08	0.24	-	0.24	
		2.3		I <sub>OL</sub> = 8 mA	-	0.10	0.3	-	0.3	
		3.0		I <sub>OL</sub> = 16 mA	-	0.15	0.4	-	0.4	
		3.0		I <sub>OL</sub> = 24 mA	-	0.22	0.55	-	0.55	
		4.5		I <sub>OL</sub> = 32 mA	-	0.22	0.55	-	0.55	
I <sub>IN</sub>	Input Leakage Current	1.65 to 5.5	0 ≤ V <sub>IN</sub> ≤ 5.5 V		-	-	±0.1	-	±1.0	μA
I <sub>OZ</sub>	3-STATE Output Leakage	1.65 to 5.5	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> 0 ≤ V <sub>OUT</sub> ≤ 5.5 V		-	-	±0.5	-	±5.0	μA
I <sub>OFF</sub>	Power Off Leakage Current	0.0	V <sub>IN</sub> or V <sub>OUT</sub> = 5.5 V		-	-	1.0	-	10	μA
I <sub>CC</sub>	Quiescent Supply Current	1.65 to 5.5	V <sub>IN</sub> = 5.5 V, GND		-	-	1.0	-	10	μA

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## AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40 to +85°C		Unit
				Min	Typ	Max	Min	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay D to Q	1.65	C <sub>L</sub> = 15 pF, R <sub>D</sub> = 1 MΩ, S <sub>1</sub> = Open (Figures 5, 7)	-	9.0	15.0	-	16.0	ns
		1.8		-	6.1	10.0	-	10.5	
		2.5 ±0.2		-	3.6	6.5	-	6.8	
		3.3 ±0.3		-	2.7	4.6	-	5.0	
		5.0 ±0.5		-	2.0	3.4	-	3.7	
		3.3 ±0.3		C <sub>L</sub> = 50 pF, R <sub>D</sub> = 500 Ω S <sub>1</sub> = Open (Figures 5, 7)	-	3.3	5.5	-	
5.0 ±0.5	-	2.6	4.3		-	4.8			
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LE to Q	1.65	C <sub>L</sub> = 15 pF, R <sub>D</sub> = 1 MΩ, S <sub>1</sub> = Open (Figures 5, 7)	-	9.0	1.45	-	15.0	ns
		1.8		-	6.0	9.6	-	10.0	
		2.5 ±0.2		-	3.5	6.1	-	6.6	
		3.3 ±0.3		-	2.6	4.4	-	4.8	
		5.0 ±0.5		-	2.0	3.2	-	3.5	
		3.3 ±0.3		C <sub>L</sub> = 50 pF, R <sub>D</sub> = 500 Ω, S <sub>1</sub> = Open (Figures 5, 8)	-	3.3	5.3	-	
5.0 ±0.5	-	2.6	4.2		-	4.6			
t <sub>PZL</sub> t <sub>PZH</sub>	Output Enable Time	1.65	C <sub>L</sub> = 50 pF, V <sub>I</sub> = 2 × V <sub>CC</sub> , R <sub>U</sub> , R <sub>D</sub> = 500 Ω, S <sub>1</sub> = GND for t <sub>PZH</sub> S <sub>1</sub> = V <sub>I</sub> for t <sub>PZL</sub> (Figures 5, 8)	-	9.0	13.5	-	14.6	ns
		1.8		-	6.0	9.0	-	9.5	
		2.5 ±0.2		-	3.7	6.0	-	6.6	
		3.3 ±0.3		-	2.8	5.0	-	5.3	
		5.0 ±0.5		-	2.2	3.7	-	3.9	
t <sub>PLZ</sub> t <sub>PHZ</sub>	Output Disable Time	1.65	C <sub>L</sub> = 50 pF, V <sub>I</sub> = 2 × V <sub>CC</sub> , R <sub>U</sub> , R <sub>D</sub> = 500 Ω, S <sub>1</sub> = GND for t <sub>PHZ</sub> S <sub>1</sub> = V <sub>I</sub> for t <sub>PLZ</sub> (Figures 5, 8)	-	7.7	12.0	-	13.0	ns
		1.8		-	5.1	8.0	-	8.5	
		2.5 ±0.2		-	3.5	6.0	-	6.3	
		3.3 ±0.3		-	2.8	4.5	-	4.7	
		5.0 ±0.5		-	2.3	3.7	-	3.9	
t <sub>S</sub>	Setup Time, D to LE	2.5 ±0.2	C <sub>L</sub> = 50 pF, R <sub>D</sub> = 500 Ω, S <sub>1</sub> = Open (Figures 5, 9)	-	-	-	2.0	-	ns
		3.3 ±0.3		-	-	-	1.5	-	
		5.0 ±0.5		-	-	-	1.5	-	
t <sub>H</sub>	Hold Time, D to LE	2.5 ±0.2	C <sub>L</sub> = 50 pF, R <sub>D</sub> = 500 Ω, S <sub>1</sub> = Open (Figures 5, 9)	-	-	-	1.5	-	ns
		3.3 ±0.3		-	-	-	1.5	-	
		5.0 ±0.5		-	-	-	1.5	-	
t <sub>W</sub>	Pulse Width, LE	2.5 ±0.2	C <sub>L</sub> = 50 pF, R <sub>D</sub> = 500 Ω, S <sub>1</sub> = Open (Figures 5, 9)	-	-	-	3.0	-	ns
		3.3 ±0.3		-	-	-	3.0	-	
		5.0 ±0.5		-	-	-	3.0	-	

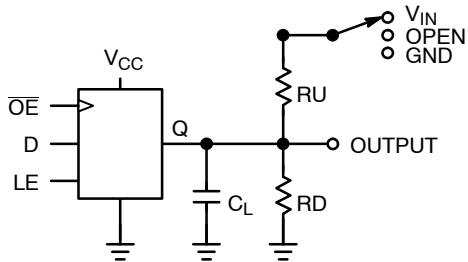
**CAPACITANCE** ( $T_A = +25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ )

Symbol	Parameter	Condition	Typ	Max	Units
$C_{IN}$	Input Capacitance	$V_{CC} = \text{Open}, V_{IN} = 0\text{ V or } V_{CC}$	3	-	pF
$C_{OUT}$	Output Capacitance	$V_{CC} = 3.3\text{ V}, V_{IN} = 0\text{ V or } V_{CC}$	4	-	pF
$C_{PD}$	Power Dissipation Capacitance (Note 2)	$V_{CC} = 3.3\text{ V}$	14	-	pF
		$V_{CC} = 5.0\text{ V}$	17	-	

2.  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption ( $I_{CCD}$ ) at no output loading and operating at 50% duty cycle. (See Figure 6)

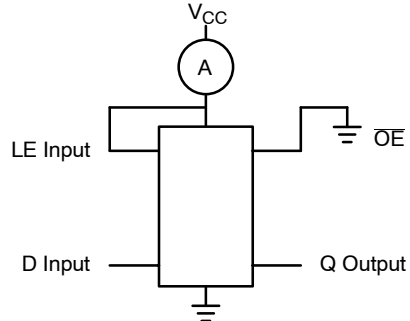
$C_{PD}$  is related to  $I_{CCD}$  dynamic operating current by the expression:  $I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CCstatic})$ .

**AC Loading and Waveforms**



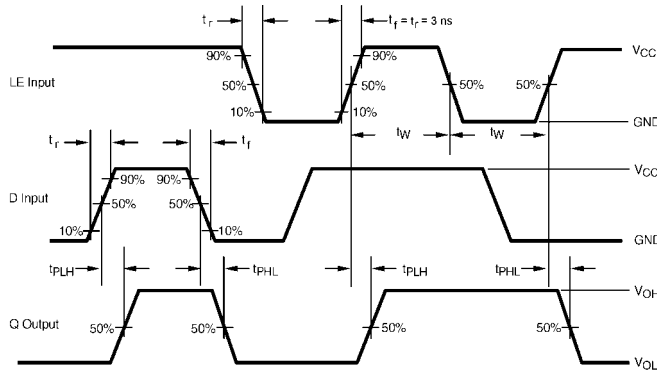
$C_L$  includes load and stray capacitance  
 Input PRR = 1.0 MHz,  $t_{W} = 500\text{ ns}$ .

**Figure 5. AC Test Circuit**

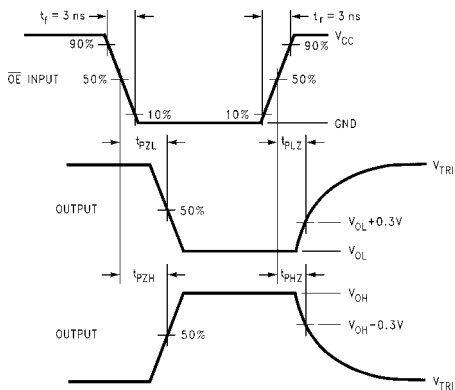


D Input = AC Waveform;  $t_r = t_f = 1.8\text{ ns}$ ;  
 D Input PRR = 10 MHz; Duty Cycle = 50%.

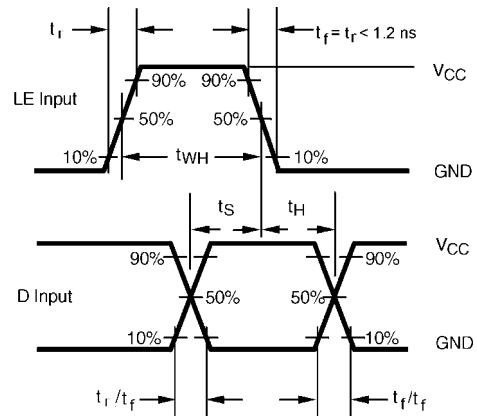
**Figure 6.  $I_{CCD}$  Test Circuit**



**Figure 7. AC Waveforms**



**Figure 8. AC Waveforms**



**Figure 9. AC Waveforms**

# NC7SZ373

## ORDERING INFORMATION

Device	Top Mark	Packages	Shipping <sup>†</sup>
NC7SZ373P6X	Z73	6-Lead SC70, EIAJ SC88, 1.25 mm Wide	3000 / Tape & Reel
NC7SZ373P6X-L22347	Z73	6-Lead SC70, EIAJ SC88, 1.25 mm Wide	3000 / Tape & Reel
NC7SZ373L6X	D4	6-Lead MicroPak, 1.00 mm Wide	5000 / Tape & Reel

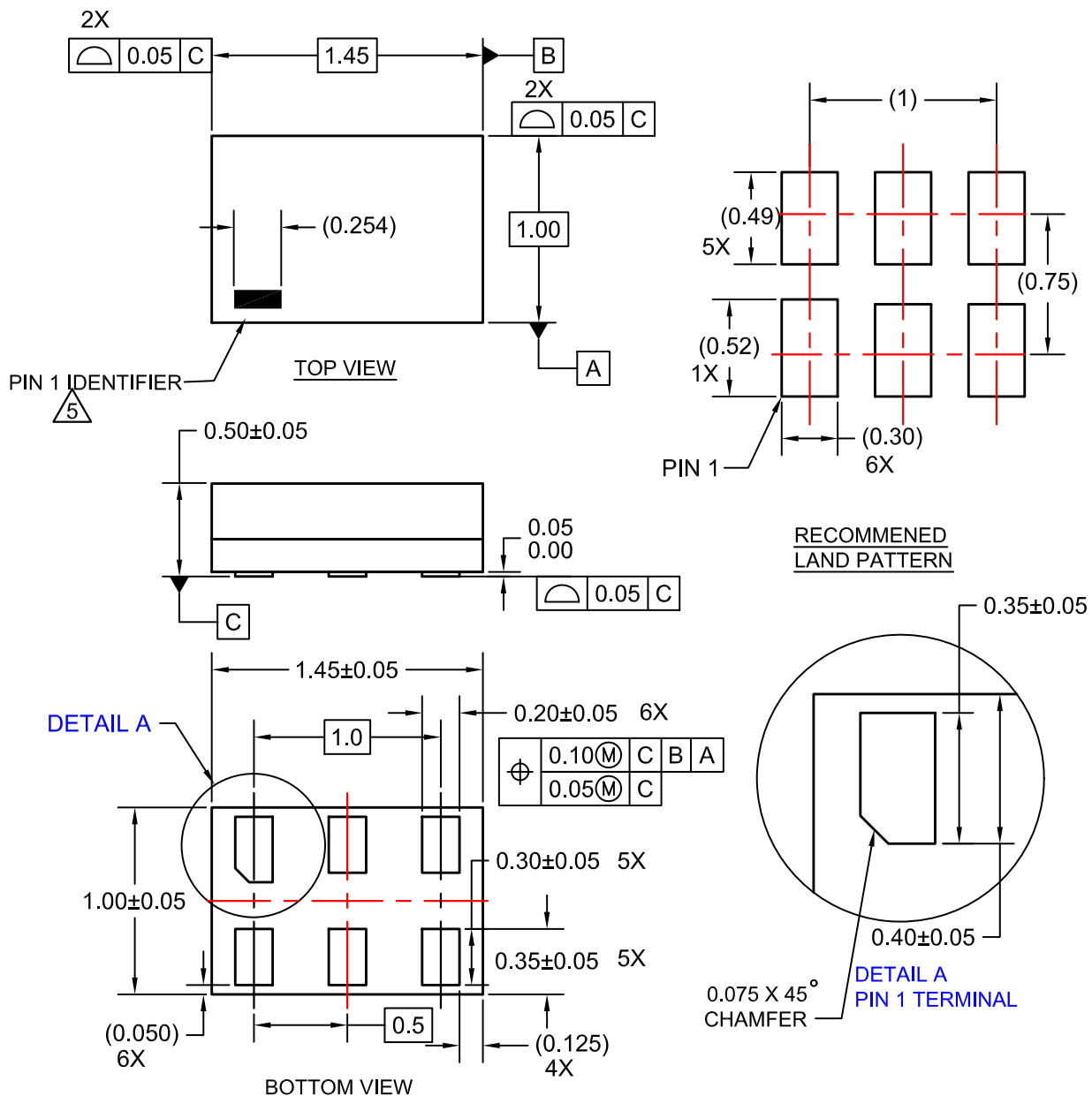
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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**SIP6 1.45X1.0**  
CASE 127EB  
ISSUE O

DATE 31 AUG 2016



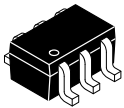
**NOTES:**

1. CONFORMS TO JEDEC STANDARD MO-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-2009
4. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

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<b>DESCRIPTION:</b>	<b>SIP6 1.45X1.0</b>	<b>PAGE 1 OF 1</b>

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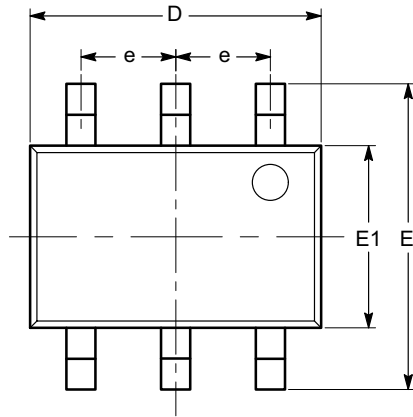
**MECHANICAL CASE OUTLINE**  
**PACKAGE DIMENSIONS**



1

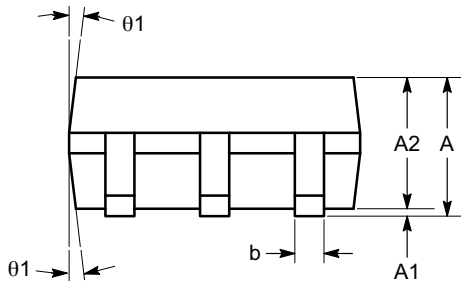
**SC-88 (SC-70 6 Lead), 1.25x2**  
**CASE 419AD**  
**ISSUE A**

DATE 07 JUL 2010

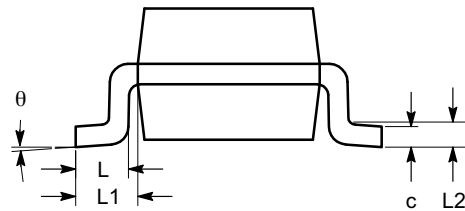


**TOP VIEW**

SYMBOL	MIN	NOM	MAX
A	0.80		1.10
A1	0.00		0.10
A2	0.80		1.00
b	0.15		0.30
c	0.10		0.18
D	1.80	2.00	2.20
E	1.80	2.10	2.40
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.26	0.36	0.46
L1	0.42 REF		
L2	0.15 BSC		
$\theta$	0°		8°
$\theta_1$	4°		10°



**SIDE VIEW**



**END VIEW**

**Notes:**

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-203.

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<b>DESCRIPTION:</b>	<b>SC-88 (SC-70 6 LEAD), 1.25X2</b>	<b>PAGE 1 OF 1</b>

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

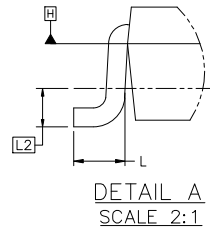
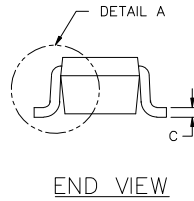
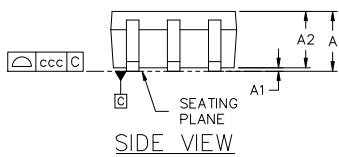
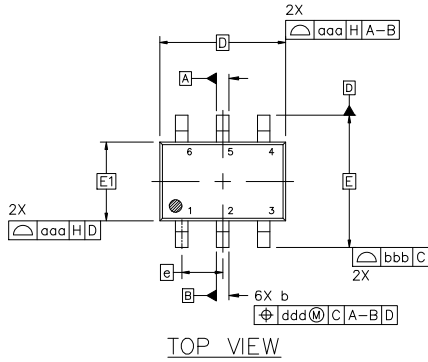


**SC-88 2.00x1.25x0.90, 0.65P**  
CASE 419B-02  
ISSUE Z

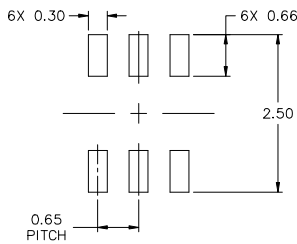
DATE 18 APR 2024

NOTES:

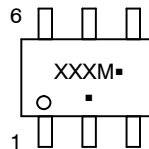
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.00	---	0.10
A2	0.70	0.90	1.00
b	0.15	0.20	0.25
c	0.08	0.15	0.22
D	2.00 BSC		
E	2.10 BSC		
E1	1.25 BSC		
e	0.65 BSC		
L	0.26	0.36	0.46
L2	0.15 BSC		
aaa	0.15		
bbb	0.30		
ccc	0.10		
ddd	0.10		



**GENERIC MARKING DIAGRAM\***



- XXX = Specific Device Code
- M = Date Code\*
- = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation and/or position may vary depending upon manufacturing location.

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

**STYLES ON PAGE 2**

FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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**SC-88 2.00x1.25x0.90, 0.65P**  
**CASE 419B-02**  
**ISSUE Z**

DATE 18 APR 2024

<b>STYLE 1:</b> PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2	<b>STYLE 2:</b> CANCELLED	<b>STYLE 3:</b> CANCELLED	<b>STYLE 4:</b> PIN 1. CATHODE 2. CATHODE 3. COLLECTOR 4. EMITTER 5. BASE 6. ANODE	<b>STYLE 5:</b> PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	<b>STYLE 6:</b> PIN 1. ANODE 2 2. N/C 3. CATHODE 1 4. ANODE 1 5. N/C 6. CATHODE 2
<b>STYLE 7:</b> PIN 1. SOURCE 2 2. DRAIN 2 3. GATE 1 4. SOURCE 1 5. DRAIN 1 6. GATE 2	<b>STYLE 8:</b> CANCELLED	<b>STYLE 9:</b> PIN 1. EMITTER 2 2. EMITTER 1 3. COLLECTOR 1 4. BASE 1 5. BASE 2 6. COLLECTOR 2	<b>STYLE 10:</b> PIN 1. SOURCE 2 2. SOURCE 1 3. GATE 1 4. DRAIN 1 5. DRAIN 2 6. GATE 2	<b>STYLE 11:</b> PIN 1. CATHODE 2 2. CATHODE 2 3. ANODE 1 4. CATHODE 1 5. CATHODE 1 6. ANODE 2	<b>STYLE 12:</b> PIN 1. ANODE 2 2. ANODE 2 3. CATHODE 1 4. ANODE 1 5. ANODE 1 6. CATHODE 2
<b>STYLE 13:</b> PIN 1. ANODE 2. N/C 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE	<b>STYLE 14:</b> PIN 1. VREF 2. GND 3. GND 4. IOUT 5. VEN 6. VCC	<b>STYLE 15:</b> PIN 1. ANODE 1 2. ANODE 2 3. ANODE 3 4. CATHODE 3 5. CATHODE 2 6. CATHODE 1	<b>STYLE 16:</b> PIN 1. BASE 1 2. EMITTER 2 3. COLLECTOR 2 4. BASE 2 5. EMITTER 1 6. COLLECTOR 1	<b>STYLE 17:</b> PIN 1. BASE 1 2. EMITTER 1 3. COLLECTOR 2 4. BASE 2 5. EMITTER 2 6. COLLECTOR 1	<b>STYLE 18:</b> PIN 1. VIN1 2. VCC 3. VOUT2 4. VIN2 5. GND 6. VOUT1
<b>STYLE 19:</b> PIN 1. IOUT 2. GND 3. GND 4. V CC 5. V EN 6. V REF	<b>STYLE 20:</b> PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR	<b>STYLE 21:</b> PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. N/C 6. CATHODE 1	<b>STYLE 22:</b> PIN 1. D1 (i) 2. GND 3. D2 (i) 4. D2 (c) 5. VBUS 6. D1 (c)	<b>STYLE 23:</b> PIN 1. Vn 2. CH1 3. Vp 4. N/C 5. CH2 6. N/C	<b>STYLE 24:</b> PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE
<b>STYLE 25:</b> PIN 1. BASE 1 2. CATHODE 3. COLLECTOR 2 4. BASE 2 5. EMITTER 6. COLLECTOR 1	<b>STYLE 26:</b> PIN 1. SOURCE 1 2. GATE 1 3. DRAIN 2 4. SOURCE 2 5. GATE 2 6. DRAIN 1	<b>STYLE 27:</b> PIN 1. BASE 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. EMITTER 2 6. COLLECTOR 2	<b>STYLE 28:</b> PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN	<b>STYLE 29:</b> PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE/ANODE 6. CATHODE	<b>STYLE 30:</b> PIN 1. SOURCE 1 2. DRAIN 2 3. DRAIN 2 4. SOURCE 2 5. GATE 1 6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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