

DATA SHEET

74F85

4-bit magnitude comparator

Product specification

1994 Sep 27

IC15 Data Handbook

Philips Semiconductors



PHILIPS

4-bit magnitude comparator

74F85

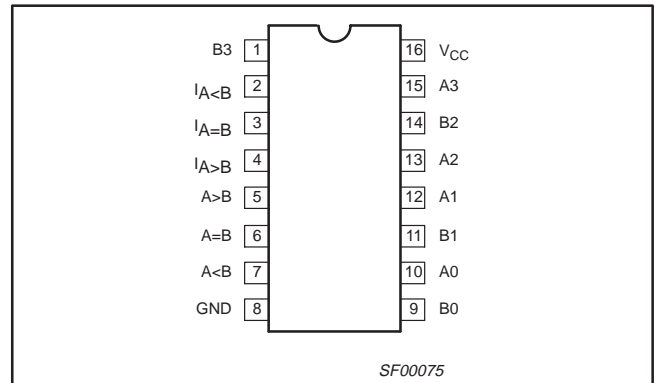
FEATURES

- High-impedance NPN base inputs for reduced loading (20µA in High and Low states)
- Magnitude comparison of any binary words
- Serial or parallel expansion without extra gating

DESCRIPTION

The 74F85 is a 4-bit magnitude comparator that can be expanded to almost any length. It compares two 4-bit binary, BCD, or other monotonic codes and presents the three possible magnitude results at the outputs. The 4-bit inputs are weighted (A0–A3) and (B0–B3) where A3 and B3 are the most significant bits. The operation of the 74F85 is described in the Function Table, showing all possible logic conditions. The upper part of the table describes the normal operation under all conditions that will occur in a single device or in a series expansion scheme. In the upper part of the table the three outputs are mutually exclusive. In the lower part of the table, the outputs reflect the feed-forward conditions that exist in the parallel expansion scheme. The expansion inputs $I_{A>B}$, $I_{A=B}$ and $I_{A<B}$ are the least significant bit positions. When used for series expansion, the $A>B$, $A=B$ and $A<B$ outputs of the least significant word are connected to the corresponding $I_{A>B}$, $I_{A=B}$ and $I_{A<B}$ inputs of the next higher stage. Stages can be added in this manner to any length, but a propagation delay penalty of about 15ns is added with each additional stage. For proper operation, the expansion inputs of the least significant word should be tied as follows: $I_{A>B}$ = Low, $I_{A=B}$ = High, and $I_{A<B}$ = Low.

PIN CONFIGURATION



| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|-------|---------------------------|--------------------------------|
| 74F85 | 7.0ns | 40mA |

ORDERING INFORMATION

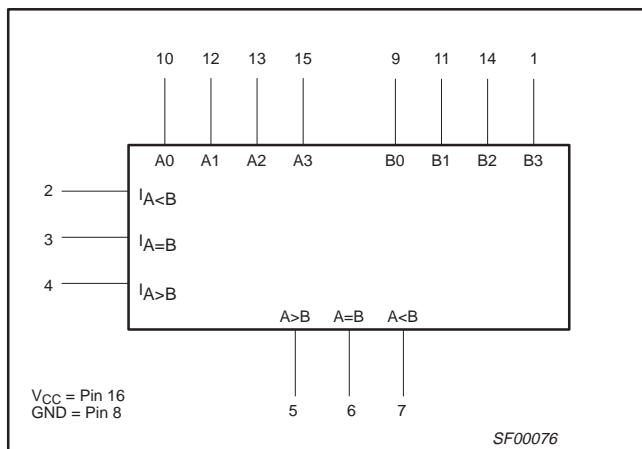
| DESCRIPTION | COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$ | PKG DWG # |
|--------------------|--|-----------|
| 16-pin plastic DIP | N74F85N | SOT38-4 |
| 16-pin plastic SO | N74F85D | SOT162-1 |

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

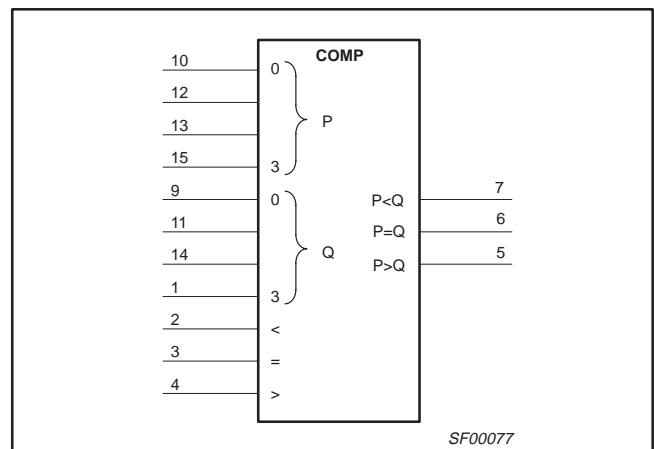
| PINS | DESCRIPTION | 74F (U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW |
|-----------------------------------|--------------------------------|---------------------|---------------------|
| A0–A3 | Comparing inputs | 1.0/0.033 | 20µA/20µA |
| B0–B3 | Comparing inputs | 1.0/0.033 | 20µA/20µA |
| $I_{A<B}$, $I_{A=B}$, $I_{A>B}$ | Expansion inputs (active High) | 1.0/0.033 | 20µA/20µA |
| $A<B$, $A=B$, $A>B$ | Data outputs (active High) | 50/33 | 1.0mA/20mA |

NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

LOGIC SYMBOL



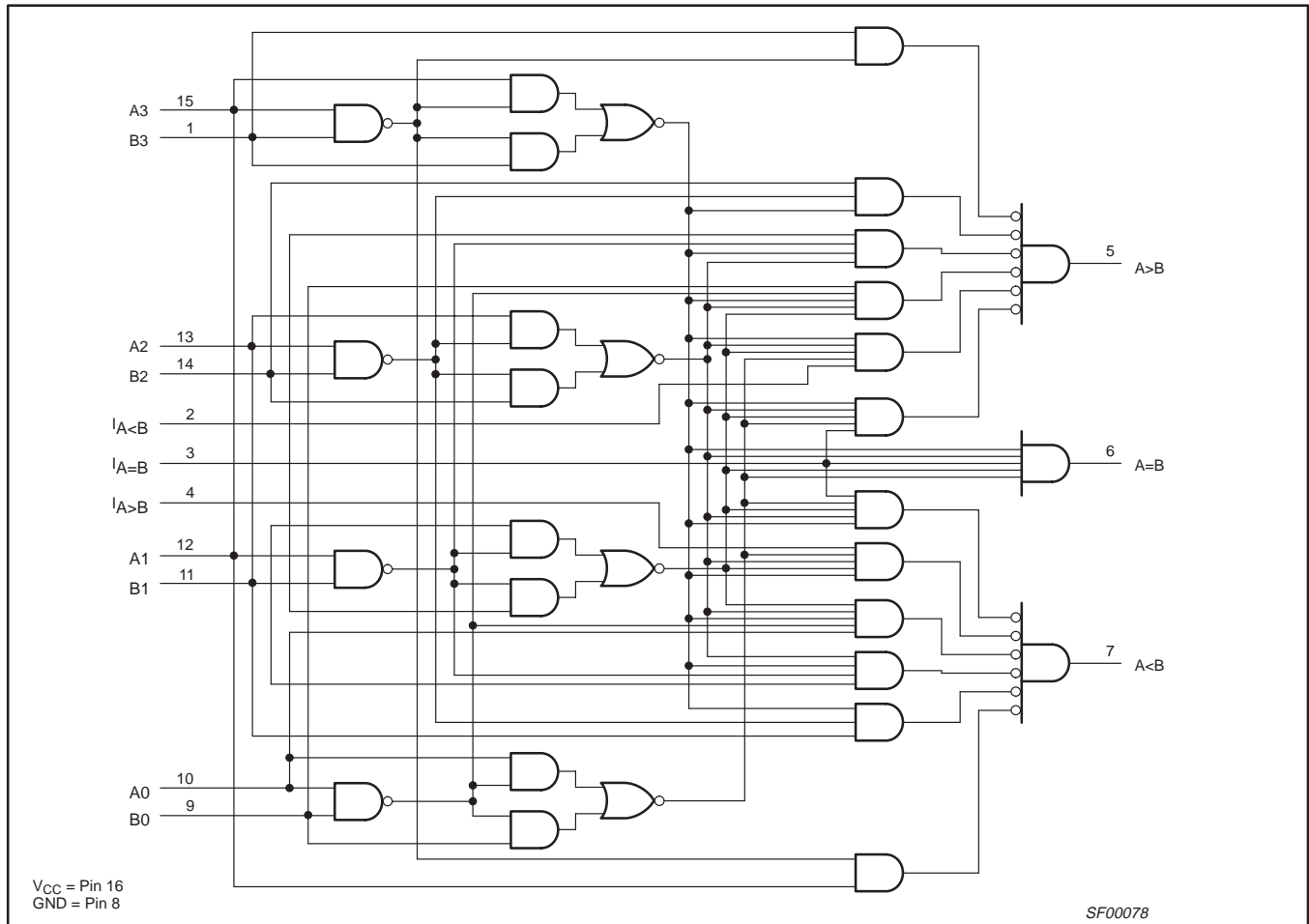
IEC/IEEE SYMBOL



4-bit magnitude comparator

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LOGIC DIAGRAM



FUNCTION TABLE

| COMPARING INPUTS | | | | EXPANSION INPUTS | | | OUTPUTS | | |
|------------------|-------|-------|-------|---------------------|---------------------|------------------|---------|-----|-----|
| A3,B3 | A2,B2 | A1,B1 | A0,B0 | I _{A>B} | I _{A<B} | I _{A=B} | A>B | A<B | A=B |
| A3>B3 | X | X | X | X | X | X | H | L | L |
| A3<B3 | X | X | X | X | X | X | L | H | L |
| A3=B3 | A2>B2 | X | X | X | X | X | H | L | L |
| A3=B3 | A2<B2 | X | X | X | X | X | L | H | L |
| A3=B3 | A2=B2 | A1>B1 | X | X | X | X | H | L | L |
| A3=B3 | A2=B2 | A1<B1 | X | X | X | X | L | H | L |
| A3=B3 | A2=B2 | A1=B1 | A0>B0 | X | X | X | H | L | L |
| A3=B3 | A2=B2 | A1=B1 | A0<B0 | X | X | X | L | H | L |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | H | L | L | H | L | L |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | L | H | L | L | H | L |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | L | L | H | L | L | H |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | X | X | H | L | L | H |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | H | H | L | L | L | L |
| A3=B3 | A2=B2 | A1=B1 | A0=B0 | L | L | L | H | H | L |

H = High voltage level
L = Low voltage level
X = Don't care

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APPLICATION

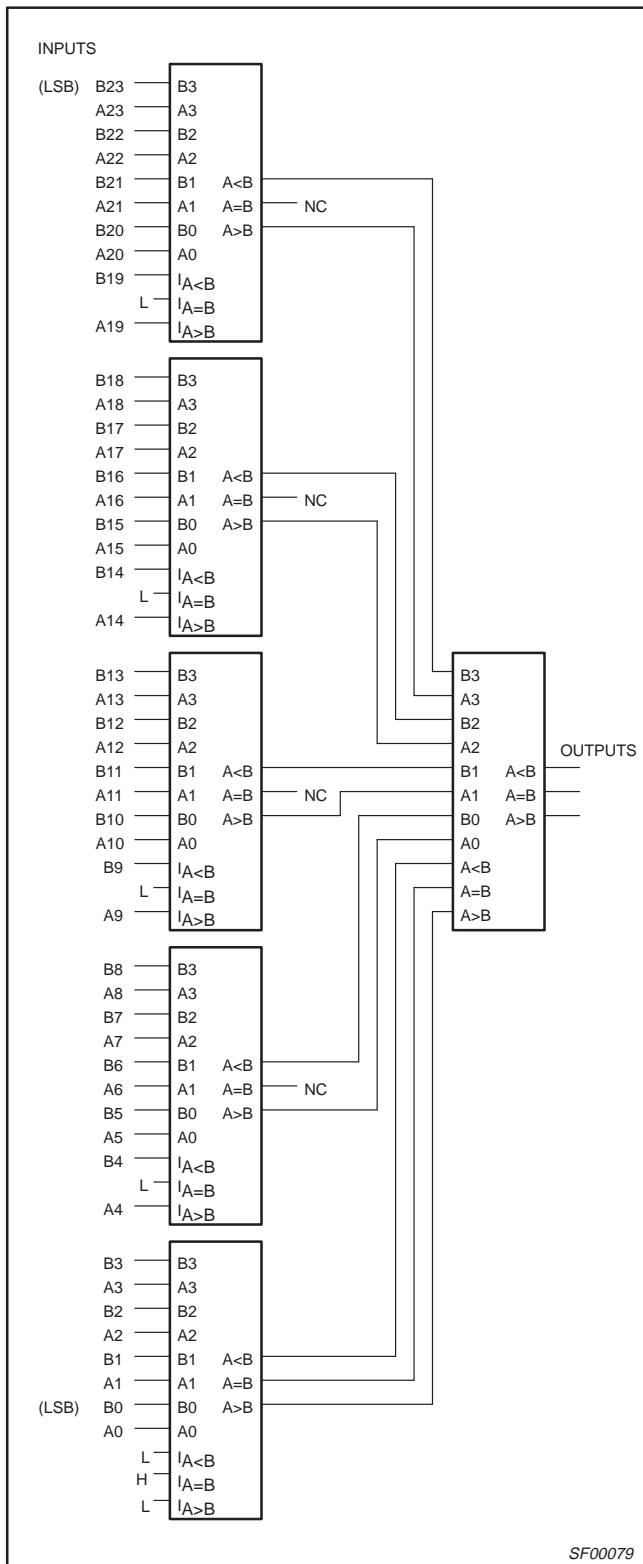


Figure 1. Comparison of Two 24-Bit Words

The parallel expansion scheme shown in Figure 1 demonstrates the most efficient general use of these comparators. The expansion inputs can be used as a fifth input bit position except on the least significant device, which must be connected as in the serial scheme. The expansion inputs used by labeling $I_{A>B}$ as an "A" input, $I_{A<B}$ as a "B" input and setting $I_{A=B}$ = Low. The 74F85 can be used as a 5-bit comparator only when the outputs are used to drive the (A0–A3) and (B0–B3) inputs of another 74F85 device. The parallel technique can be expanded to any number of bits as shown in Table 1.

Table 1.

| WORD LENGTH | NUMBER OF PACKAGES | TYPICAL SPEEDS 74F |
|-------------|--------------------|--------------------|
| 1–4 bits | 1 | 12ns |
| 5–24 bits | 2–6 | 22ns |
| 25–120 bits | 8–31 | 34ns |

4-bit magnitude comparator

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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

| SYMBOL | PARAMETER | RATING | UNIT |
|------------------|--|-------------------------|------|
| V _{CC} | Supply voltage | -0.5 to +7.0 | V |
| V _{IN} | Input voltage | -0.5 to +7.0 | V |
| I _{IN} | Input current | -30 to +5 | mA |
| V _{OUT} | Voltage applied to output in High output state | -0.5 to V _{CC} | V |
| I _{OUT} | Current applied to output in Low output state | 40 | mA |
| T _{amb} | Operating free-air temperature range | 0 to +70 | °C |
| T _{stg} | Storage temperature range | -65 to +150 | °C |

RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|------------------|--------------------------------------|--------|-----|-----|------|
| | | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| V _{IH} | High-level input voltage | 2.0 | | | V |
| V _{IL} | Low-level input voltage | | | 0.8 | V |
| I _{IK} | Input clamp current | | | -18 | mA |
| I _{OH} | High-level output current | | | -1 | mA |
| I _{OL} | Low-level output current | | | 20 | mA |
| T _{amb} | Operating free-air temperature range | 0 | | +70 | °C |

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

| SYMBOL | PARAMETER | TEST CONDITIONS ¹ | LIMITS | | | UNIT | |
|-----------------|---|--|--|------------------|------|------|----|
| | | | MIN | TYP ² | MAX | | |
| V _{OH} | High-level output voltage | V _{CC} = MIN, V _{IL} = MAX V _{IH} = MIN, I _{OH} = MAX | ±10%V _{CC} | 2.5 | | V | |
| | | | ±5%V _{CC} | 2.7 | 3.4 | | |
| V _{OL} | Low-level output voltage | V _{CC} = MIN, V _{IL} = MAX V _{IH} = MIN, I _{OL} = MAX | ±10%V _{CC} | | 0.30 | 0.50 | V |
| | | | ±5%V _{CC} | | 0.30 | 0.50 | |
| V _{IK} | Input clamp voltage | V _{CC} = MIN, I _I = I _{IK} | | -0.73 | -1.2 | V | |
| I _I | Input current at maximum input voltage | V _{CC} = 0.0V, V _I = 7.0V | | | 100 | μA | |
| I _{IH} | High-level input current | V _{CC} = MAX, V _I = 2.7V | | | 20 | μA | |
| I _{IL} | Low-level input current | V _{CC} = MAX, V _I = 0.5V | | | -20 | μA | |
| I _{OS} | Short-circuit output current ³ | V _{CC} = MAX | -60 | | -150 | mA | |
| I _{CC} | Supply current (total) | V _{CC} = MAX | V _{IN} = GND An = Bn = I _{A=B} = GND, I _{A>B} = I _{A<B} = 4.5V | | 36 | 50 | mA |
| | | | | | 40 | 54 | |

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

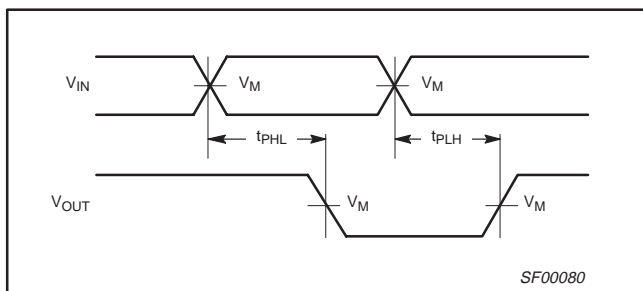
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AC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITION | LIMITS | | | | | UNIT |
|------------------------|---|------------------------------|---|-----|------|---|------|------|
| | | | $V_{CC} = +5.0V$ $T_{amb} = +25^{\circ}C$ $C_L = 50pF, R_L = 500\Omega$ | | | $V_{CC} = +5.0V \pm 10\%$ $T_{amb} = 0^{\circ}C \text{ to } +70^{\circ}C$ $C_L = 50pF, R_L = 500\Omega$ | | |
| | | | MIN | TYP | MAX | MIN | MAX | |
| t_{PLH} t_{PHL} | Propagation delay A or B to A<B, A>B | Waveform 1 3 logic levels | 6.0 | 8.5 | 11.0 | 5.5 | 13.0 | ns |
| t_{PLH} t_{PHL} | Propagation delay A or B to A=B | Waveform 1 4 logic levels | 6.5 | 9.0 | 11.5 | 6.0 | 14.0 | |
| t_{PLH} t_{PHL} | Propagation delay $I_{A<B}$ and $I_{A=B}$ to A>B | Waveform 1 1 logic level | 3.0 | 5.0 | 7.5 | 2.5 | 9.0 | ns |
| t_{PLH} t_{PHL} | Propagation delay $I_{A=B}$ to A=B | Waveform 1 2 logic levels | 2.5 | 4.5 | 7.0 | 2.0 | 9.0 | |
| t_{PLH} t_{PHL} | Propagation delay $I_{A>B}$ and $I_{A=B}$ to A<B | Waveform 1 1 logic level | 3.0 | 5.0 | 8.0 | 3.0 | 9.5 | ns |
| t_{PLH} t_{PHL} | | | 3.0 | 6.0 | 9.0 | 2.0 | 9.5 | |

AC WAVEFORMS



Waveform 1. Propagation Delay Input to Output

NOTE:

For all waveforms, $V_M = 1.5V$.

TEST CIRCUIT AND WAVEFORMS

Test Circuit for Totem-Pole Outputs

Input Pulse Definition

DEFINITIONS:

- R_L = Load resistor;
see AC ELECTRICAL CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance;
see AC ELECTRICAL CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

| family | INPUT PULSE REQUIREMENTS | | | | | |
|--------|--------------------------|-------|-----------|-------|-----------|-----------|
| | amplitude | V_M | rep. rate | t_w | t_{TLH} | t_{THL} |
| 74F | 3.0V | 1.5V | 1MHz | 500ns | 2.5ns | 2.5ns |

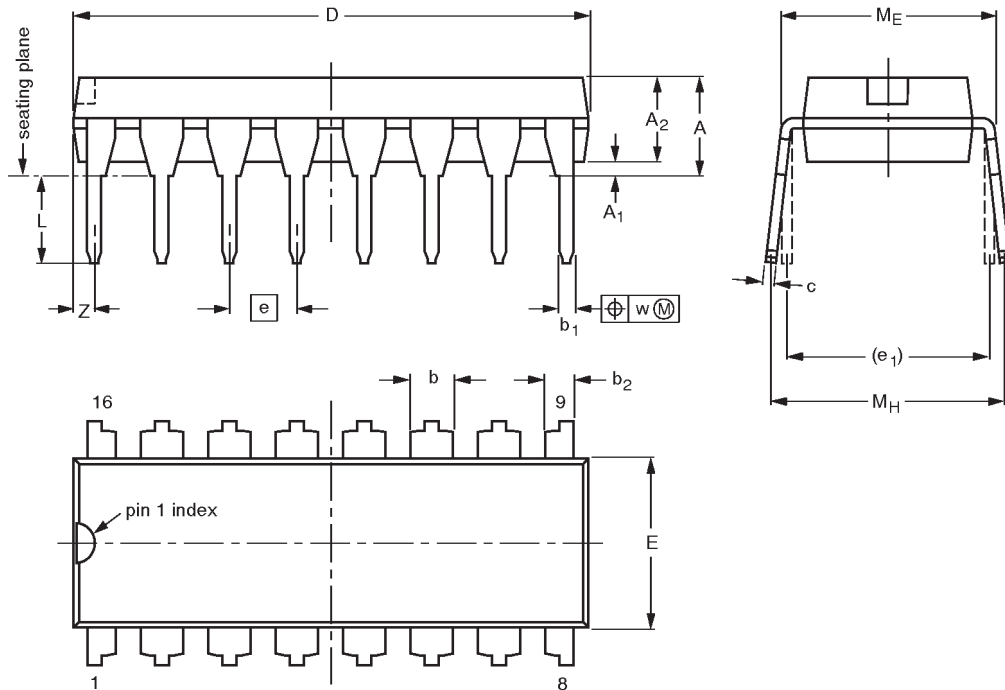
SF00006

4-bit magnitude comparator

74F85

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ min. | A ₂ max. | b | b ₁ | b ₂ | c | D ⁽¹⁾ | E ⁽¹⁾ | e | e ₁ | L | M _E | M _H | w | Z ⁽¹⁾ max. |
|--------|--------|---------------------|---------------------|----------------|----------------|----------------|----------------|------------------|------------------|------|----------------|--------------|----------------|----------------|-------|-----------------------|
| mm | 4.2 | 0.51 | 3.2 | 1.73 1.30 | 0.53 0.38 | 1.25 0.85 | 0.36 0.23 | 19.50 18.55 | 6.48 6.20 | 2.54 | 7.62 | 3.60 3.05 | 8.25 7.80 | 10.0 8.3 | 0.254 | 0.76 |
| inches | 0.17 | 0.020 | 0.13 | 0.068 0.051 | 0.021 0.015 | 0.049 0.033 | 0.014 0.009 | 0.77 0.73 | 0.26 0.24 | 0.10 | 0.30 | 0.14 0.12 | 0.32 0.31 | 0.39 0.33 | 0.01 | 0.030 |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

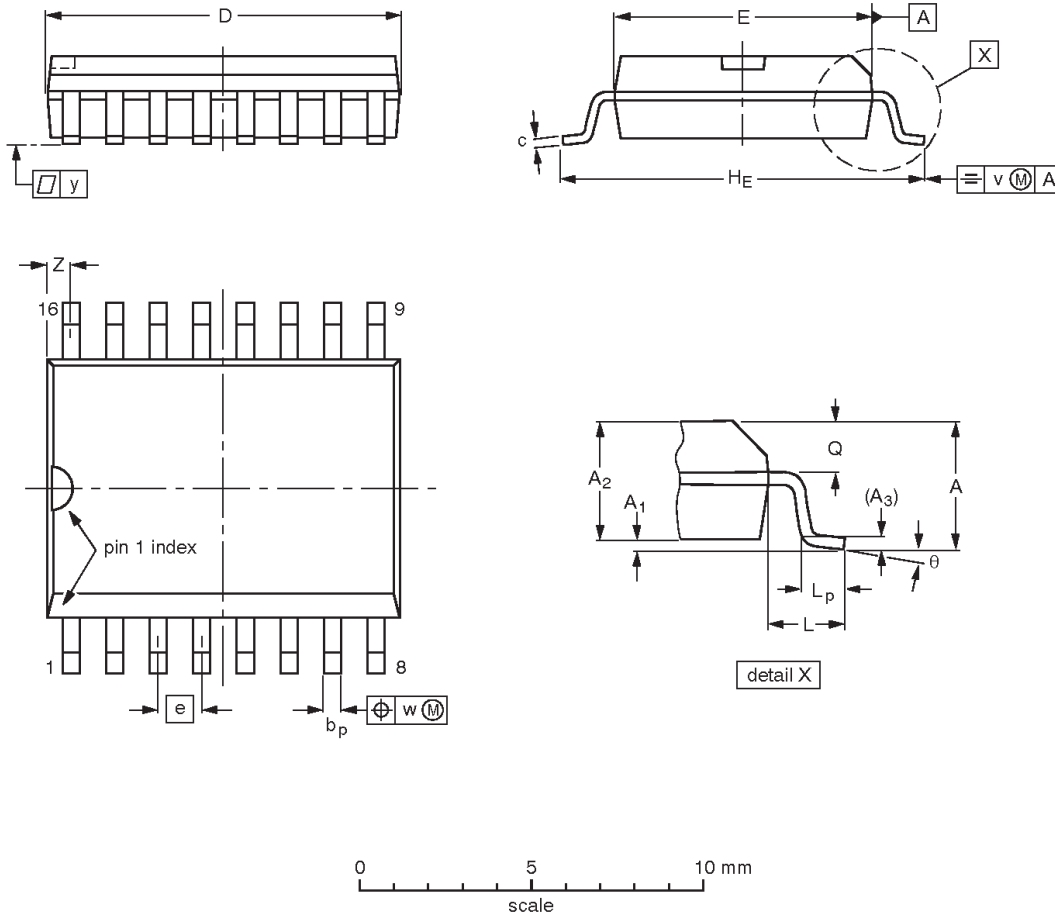
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|-------|------|--|---------------------|-----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT38-4 | | | | | | -92-11-17 95-01-14 |

4-bit magnitude comparator

74F85

SO16: plastic small outline package; 16 leads; body width 7.5 mm

SOT162-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | z ⁽¹⁾ | θ |
|--------|--------|----------------|----------------|----------------|----------------|----------------|------------------|------------------|-------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm | 2.65 | 0.30 0.10 | 2.45 2.25 | 0.25 | 0.49 0.36 | 0.32 0.23 | 10.5 10.1 | 7.6 7.4 | 1.27 | 10.65 10.00 | 1.4 | 1.1 0.4 | 1.1 1.0 | 0.25 | 0.25 | 0.1 | 0.9 0.4 | 8° 0° |
| inches | 0.10 | 0.012 0.004 | 0.096 0.089 | 0.01 | 0.019 0.014 | 0.013 0.009 | 0.41 0.40 | 0.30 0.29 | 0.050 | 0.419 0.394 | 0.055 | 0.043 0.016 | 0.043 0.039 | 0.01 | 0.01 | 0.004 | 0.035 0.016 | |

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT162-1 | 075E03 | MS-013AA | | | | 95-01-24 97-05-22 |

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NOTES

4-bit magnitude comparator

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Data sheet status

| Data sheet status | Product status | Definition [1] |
|---------------------------|----------------|--|
| Objective specification | Development | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice. |
| Preliminary specification | Qualification | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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