THE DATASHEET OF

MX7576KEQP+

19-0876; Rev 1; 5/96

MAXIM

CMOS, µP-Compatible, 5µs/10µs, 8-Bit ADCs

General Description

Maxim's MX7575/MX7576 are high-speed (5µs/10µs), microprocessor (µP) compatible, 8-bit analog-to-digital converters (ADCs). The MX7575 provides an on-chip track/hold function that allows full-scale signals up to 50kHz (386mV/µs slew rate) to be acquired and digitized accurately. Both ADCs use a successive-approximation technique to achieve their fast conversions and low power dissipation. The MX7575/MX7576 operate with a +5V supply and a 1.23V external reference. They accept input voltages ranging from 0V to $2V_{REF}$.

The MX7575/MX7576 are easily interfaced to all popular 8-bit µPs through standard $\overline{CS}$ and $\overline{RD}$ control signals. These signals control conversion start and data access. A $\overline{BUSY}$ signal indicates the beginning and end of a conversion. Since all the data outputs are latched and three-state buffered, the MX7575/MX7576 can be directly tied to a µP data bus or system I/O port.

Maxim also makes the **MAX165**, a plug-in replacement for the MX7575 with an internal 1.23V reference. For applications that require a differential analog input and an internal reference, the **MAX166** is recommended.

Applications

Digital Signal Processing
High-Speed Data Acquisition
Telecommunications
Audio Systems
High-Speed Servo Loops
Low-Power Data Loggers

Features

- ♦ **Fast Conversion Time: 5µs (MX7575)**
  10µs (MX7576)
- ♦ **Built-In Track/Hold Function (MX7575)**
- ♦ **Low Total Unadjusted Error (±1LSB max)**
- ♦ **50kHz Full-Power Signal Bandwidth (MX7575)**
- ♦ **Single +5V Supply Operation**
- ♦ **8-Bit µP Interface**
- ♦ **100ns Data-Access Time**
- ♦ **Low Power: 15mW**
- ♦ **Small-Footprint Packages**

Ordering Information

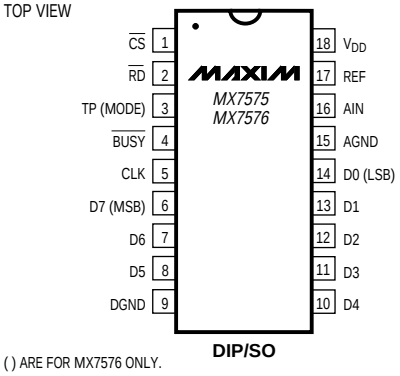
PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MX7575JN	0°C to +70°C	18 Plastic DIP	±1
MX7575KN	0°C to +70°C	18 Plastic DIP	±1/2
MX7575JCWN	0°C to +70°C	18 Wide SO	±1
MX7575KCWN	0°C to +70°C	18 Wide SO	±1/2
MX7575JP	0°C to +70°C	20 PLCC	±1
MX7575KP	0°C to +70°C	20 PLCC	±1/2
MX7575J/D	0°C to +70°C	Dice*	±1
MX7575AQ	-25°C to +85°C	18 CERDIP**	±1
MX7575BQ	-25°C to +85°C	18 CERDIP**	±1/2

Ordering Information continued at end of data sheet.

** Contact factory for dice specifications.*

*** Contact factory for availability.*

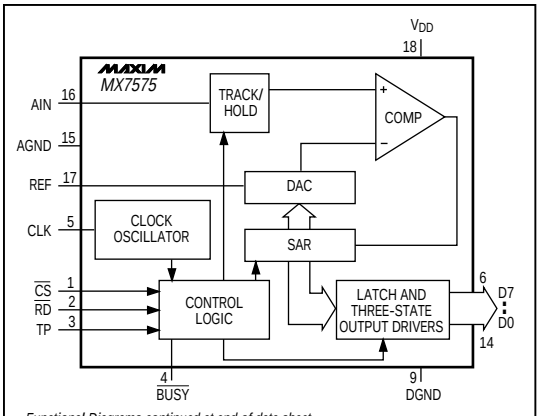
Pin Configurations



( ) ARE FOR MX7576 ONLY.

Pin Configurations continued at end of data sheet.

Functional Diagrams



Functional Diagrams continued at end of data sheet.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND.....-0.3V, +7V
V_{DD} to DGND .....-0.3V, +7V
AGND to DGND.....-0.3V, V_{DD} + 0.3V
Digital Input Voltage to DGND
($\overline{CS}$, $\overline{RD}$, TP, MODE).....-0.3V, V_{DD} + 0.3V
Digital Output Voltage to DGND
($\overline{BUSY}$, D0–D7) .....-0.3V, V_{DD} + 0.3V
CLK Input Voltage to DGND.....-0.3V, V_{DD} + 0.3V
REF to AGND.....-0.3V, V_{DD} + 0.3V
AIN to AGND.....-0.3V, V_{DD} + 0.3V

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
Wide SO (derate 9.52mW/°C above +70°C).....762mW
CERDIP (derate 10.53mW/°C above +70°C).....842mW
PLCC (derate 10.00mW/°C above +70°C) 800mW
Operating Temperature Ranges
MX757_J/K.....0°C to +70°C
MX757_A/B .....-25°C to +85°C
MX757_JE/KE .....-40°C to +85°C
MX757_S/T.....-55°C to +125°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering,10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V; V_{REF} = 1.23V; AGND = DGND = 0V; f_{CLK} = 4MHz external for MX7575; f_{CLK} = 2MHz external for MX7576; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY							
Resolution				8			Bits
Total Unadjusted Error	TUE	MX757_K/B/T				±1	LSB
		MX757_J/A/S				±2	
Relative Accuracy	INL	MX757_K/B/T				±1/2	LSB
		MX757_J/A/S				±1	
No-Missing-Codes Resolution				8			Bits
Full-Scale Error						±1	LSB
Full-Scale Tempco					±5		ppm/°C
Offset Error (Note 1)						±1/2	LSB
Offset Tempco					±5		ppm/°C
ANALOG INPUT							
Voltage Range		1LSB = $2V_{REF}/256$		0		$2V_{REF}$	V
DC Input Impedance				10			MΩ
Slew Rate, Tracking		MX7575				0.386	V/µs
Signal-to-Noise Ratio (Note 2)	SNR	MX7575, V_{IN} = $2.46V_{p-p}$ at 10kHz, Figure 13		45			dB
REFERENCE INPUT							
Reference Voltage	V_{REF}	±5% variation for specified performance			1.23		V
Reference Current	I_{REF}					500	µA
LOGIC INPUTS $\overline{CS}$, $\overline{RD}$, MODE							
Input Low Voltage	V_{INL}					0.8	V
Input High Voltage	V_{INH}			2.4			V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}	T_A = +25°C			±1	µA
			T_A = T_{MIN} to T_{MAX}			±10	
Input Capacitance (Note 2)	C_{IN}					10	pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V; V_{REF} = 1.23V; AGND = DGND = 0V; f_{CLK} = 4MHz external for MX7575; f_{CLK} = 2MHz external for MX7576; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CLOCK							
Input Low Voltage	V_{INL}					0.8	V
Input High Voltage	V_{INH}			2.4			V
Input Low Current	I_{INL}	V_{IN} = 0V	MX757_J/A/K/B			700	µA
			MX757_S/T			800	
Input High Current	I_{INH}	$V_{IN} = V_{DD}$	MX757_J/A/K/B			700	µA
			MX757_S/T			800	
LOGIC OUTPUTS (D0–D7, $\overline{BUSY}$)							
Output Low Voltage	V_{OL}	I_{SINK} = 1.6mA				0.4	V
Output High Voltage	V_{OH}	I_{SOURCE} = 40µA		4.0			V
Floating State Leakage Current		V_{OUT} = 0V to V_{DD}, D0–D7	T_A = +25°C			±1	µA
			$T_A = T_{MIN}$ to T_{MAX}			±10	
Floating State Output Capacitance (Note 2)		D0–D7				10	pF
CONVERSION TIME (Note 3)							
Conversion Time with External Clock		MX7575: f_{CLK} = 4MHz			5		µs
		MX7576: f_{CLK} = 2MHz			10		
Conversion Time with Internal Clock		Using recommended clock components: R_{CLK} = 100kΩ, C_{CLK} = 100pF; T_A = +25°C	MX7575	5		15	µs
			MX7576	10		30	
POWER REQUIREMENTS (Note 4)							
Supply Voltage	V_{DD}	±5% for specified performance			5		V
Supply Current	I_{DD}	MX757_J/A/K/B			3	6	mA
		MX757_S/T				7	
Power Dissipation					15		mW
Power-Supply Rejection		4.75V < V_{DD} < 5.25V				±1/4	LSB

Note 1: Offset Error is measured with respect to an ideal first-code transition that occurs at 1/2LSB.
Note 2: Sample tested at +25°C to ensure compliance.
Note 3: Accuracy may degrade at conversion times other than those specified.
Note 4: Power-supply current is measured when MX7575/MX7576 are inactive, i.e.:
For MX7575 $\overline{CS}$ = $\overline{RD}$ = $\overline{BUSY}$ = high;
For MX7576 $\overline{CS}$ = $\overline{RD}$ = $\overline{BUSY}$ = MODE = high.

TIMING CHARACTERISTICS (Note 5)

(V_{DD} = +5V, V_{REF} = 1.23V, AGND = DGND = 0V.)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C		T_A = T_{MIN} to T_{MAX}				UNITS
			ALL		J/K/A/B		S/T		
			MIN	MAX	MIN	MAX	MIN	MAX	
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_1		0		0		0		ns
$\overline{RD}$ to $\overline{BUSY}$ Propagation Time	t_2			100		100		120	ns
Data-Access Time after $\overline{RD}$	t_3	(Note 6)		100		100		120	ns
$\overline{RD}$ Pulse Width	t_4		100		100		120		ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_5		0		0		0		ns
Data-Access Time after $\overline{BUSY}$	t_6	(Note 6)		80		80		100	ns
Data-Hold Time	t_7	(Note 7)	10	80	10	80	10	100	ns
$\overline{BUSY}$ to $\overline{CS}$ Delay	t_8		0		0		0		ns

Note 5: Timing specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with t_r = t_f = 20ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.

Note 6: t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.

Note 7: t_7 is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.

Pin Description

PIN		NAME	FUNCTION
DIP/SO	PLCC		
1	2	$\overline{CS}$	Chip Select Input. $\overline{CS}$ must be low for the device to be selected or to recognize the $\overline{RD}$ input.
2	3	$\overline{RD}$	Read Input. $\overline{RD}$ must be low to access data. $\overline{RD}$ is also used to start conversions. See the *Microprocessor Interface* section.
3	4	TP (MX7575)	Test Point. Connect to V_{DD}.
		MODE (MX7576)	Mode Input. MODE = low puts the ADC into its asynchronous conversion mode. MODE has to be tied high for the synchronous conversion mode and the ROM interface mode.
4	5	$\overline{BUSY}$	$\overline{BUSY}$ Output. $\overline{BUSY}$ going low indicates the start of a conversion. $\overline{BUSY}$ going high indicates the end of a conversion.
5	6	CLK	External Clock Input/Internal Oscillator Pin for frequency setting RC components.
6	7	D7	Three-State Data Output, bit 7 (MSB)
7, 8	8, 9	D6, D5	Three-State Data Outputs, bits 6 and 5
9	10	DGND	Digital Ground
10–13	12–15	D4–D1	Three-State Data Outputs, bits 4–1
14	16	D0	Three-State Data Output, bit 0 (LSB)
15	17	AGND	Analog Ground
16	18	AIN	Analog Input. 0V to 2V_{REF} input range.
17	19	REF	Reference Input. +1.23V nominal.
18	20	V_{DD}	Power-Supply Voltage. +5V nominal.
—	1, 11	N.C.	No Connect

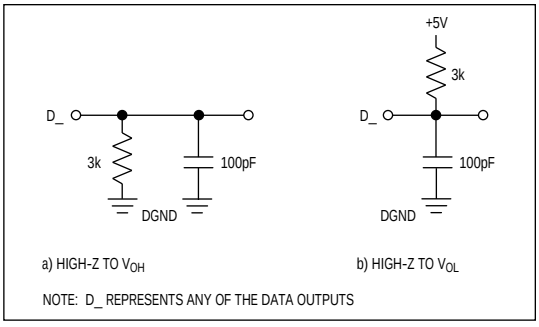


Figure 1. Load Circuits for Data-Access Time Test

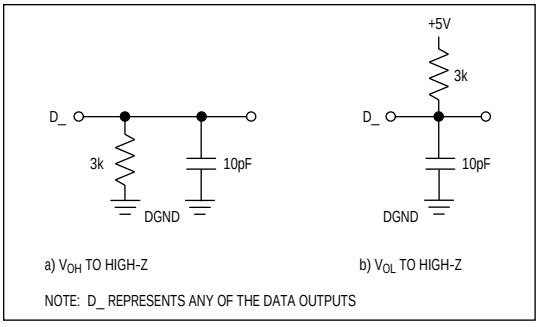


Figure 2. Load Circuits for Data-Hold Time Test

Detailed Description

Converter Operation

The MX7575 and MX7576 use the successive-approximation technique to convert an unknown analog input voltage to an 8-bit digital output code (see *Functional Diagrams*). The MX7575 samples the input voltage on an internal capacitor once (at the beginning of the conversion), while the MX7576 samples the input signal eight times during the conversion (see *MX7575 Track/Hold* and *MX7576 Analog Input* sections). The internal DAC is initially set to half scale, and the comparator determines whether the input signal is larger than or smaller than half scale. If it is larger than half scale, the DAC MSB is kept. But if it is smaller, the MSB is dropped. At the end of each comparison phase, the SAR (successive-approximation register) stores the results of the previous decision and determines the next trial bit. This information is then loaded into the DAC after each decision. As the conversion proceeds, the analog input is approximated more closely by comparing it to the combination of the previous DAC bits and a new DAC trial bit. After eight comparison cycles, the eight bits stored in the SAR are latched into the output latches. At the end of the conversion, the $\overline{BUSY}$ signal goes high, and the data in the output latches is ready for microprocessor (µP) access. Furthermore, the DAC is reset to half scale in preparation for the next conversion.

Microprocessor Interface

The $\overline{CS}$ and $\overline{RD}$ logic inputs are used to initiate conversions and to access data from the devices. The MX7575 and MX7576 have two common interface modes: slow-memory interface mode and ROM interface mode. In addition, the MX7576 has an asynchronous conversion mode (MODE pin = low) where continuous conversions are performed. In the slow-memory interface mode, $\overline{CS}$ and $\overline{RD}$ are taken low to start a conversion and they remain low until the conversion ends, at which time the conversion result is latched. This mode is designed for µPs that can be forced into a wait state. In the ROM interface mode, however, the µP is not forced into a wait state. A conversion is started by taking $\overline{CS}$ and $\overline{RD}$ low, and data from the previous conversion is read. At the end of the most recent conversion, the µP executes a read instruction and starts another conversion.

For the MX7575, TP should be hard-wired to V_{DD} to ensure proper operation of the device. Spurious signals may occur on TP, or excessive currents may be drawn from V_{DD} if TP is left open or tied to a voltage other than V_{DD}.

Slow-Memory Mode

Figure 3 shows the timing diagram for slow-memory interface mode. This is used with µPs that have a wait-state capability of at least 10µs (such as the 8085A), where a read instruction is extended to accommodate slow-memory devices. A conversion is started by executing a memory read to the device (taking $\overline{CS}$ and $\overline{RD}$ low). The $\overline{BUSY}$ signal (which is connected to the µP READY input) then goes low and forces the µP into a wait state. The MX7575 track/hold, which had been tracking the analog input signal, holds the signal on the third falling clock edge after $\overline{RD}$ goes low (Figure 12). The MX7576, however, samples the analog input eight times during a conversion (once before each comparator decision). At the end of the conversion, $\overline{BUSY}$ returns high, the output latches and buffers are updated with the new conversion result, and the µP completes the memory read by acquiring this new data.

The fast conversion time of the MX7575/MX7576 ensures that the µP is not forced into a wait state for an excessive amount of time. Faster versions of many µPs,

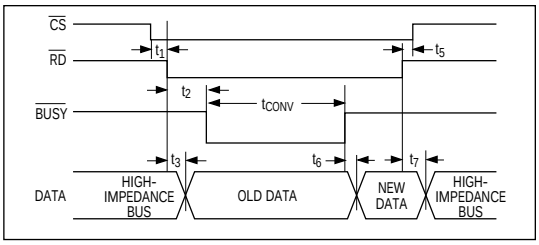


Figure 3. Slow-Memory Interface Timing Diagram

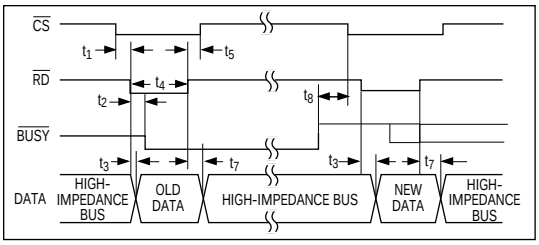


Figure 5. ROM Interface Timing Diagram

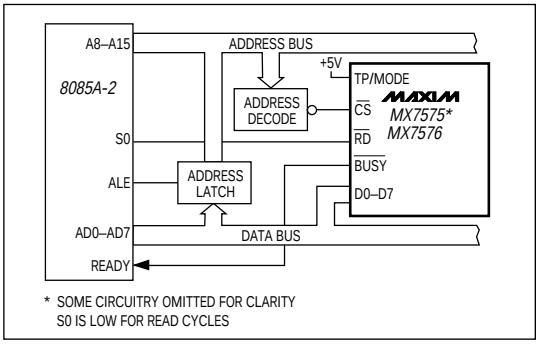


Figure 4. MX7575/MX7576 to 8085A-2 Slow-Memory Interface

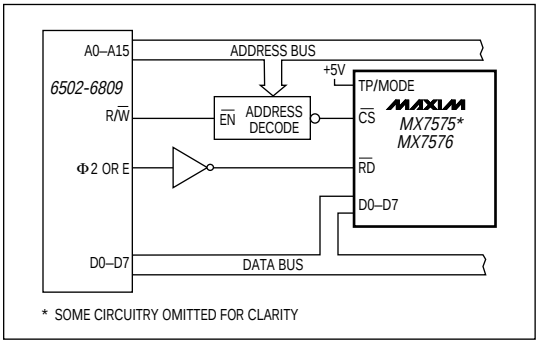


Figure 6. MX7575/MX7576 to 6502/6809 ROM Interface

including the 8085A-2, test the status of the READY input immediately after the start of an instruction cycle. Therefore, if the MX7575/MX7576 are to be effective in placing the µP in a wait state, their $\overline{BUSY}$ output should go low very early in the cycle. When using the 8085A-2, the earliest possible indication of an upcoming read operation is provided by the S0 status signal. Thus, S0, which is low for a read cycle, should be connected to the $\overline{RD}$ input of the MX7575/MX7576. Figure 4 shows the connection diagram for the 8085A-2 to the MX7575/MX7576 in slow-memory interface mode.

ROM Interface Mode

Figure 5 shows the timing diagram for ROM interface mode. In this mode, the µP does not need to be placed in a wait state. A conversion is started with a read instruction ($\overline{RD}$ and $\overline{CS}$ go low), and old data is accessed. The $\overline{BUSY}$ signal then goes low to indicate the start of a conversion. As before, the MX7575 track/hold acquires the signal on the third falling clock edge after $\overline{RD}$ goes low, while the MX7576 samples it eight times during a conversion. At the end of a conversion ($\overline{BUSY}$ going high), another read instruction always accesses the new data and normally starts a second conversion. However, if $\overline{RD}$ and $\overline{CS}$ go low within one external clock period of $\overline{BUSY}$ going high, then the second conversion is not started. Furthermore, for correct operation in this mode, $\overline{RD}$ and $\overline{CS}$ should not go low before $\overline{BUSY}$ returns high.

Figures 6 and 7 show the connection diagrams for interfacing the MX7575/MX7576 in the ROM interface mode. Figure 6 shows the connection diagram for the 6502/6809 µPs, and Figure 7 shows the connections for the Z-80.

Due to their fast interface timing, the MX7575/MX7576 will interface to the TMS32010 running at up to 18MHz. Figure 8 shows the connection diagram for the TMS32010. In this example, the MX7575/MX7576 are mapped as a port address. A conversion is initiated by using an IN A and a PA instruction, and the conversion result is placed in the TMS32010 accumulator.

Asynchronous Conversion Mode (MX7576)

Tying the MODE pin low places the MX7576 into a continuous conversion mode. The $\overline{RD}$ and $\overline{CS}$ inputs are only used for reading data from the converter. Figure 9 shows the timing diagram for this mode of operation, and Figure 10 shows the connection diagram for the 8085A. In this mode, the MX7576 looks like a ROM to

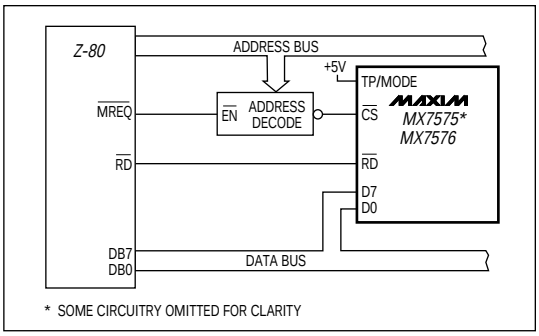


Figure 7. MX7575/MX7576 to Z-80 ROM Interface

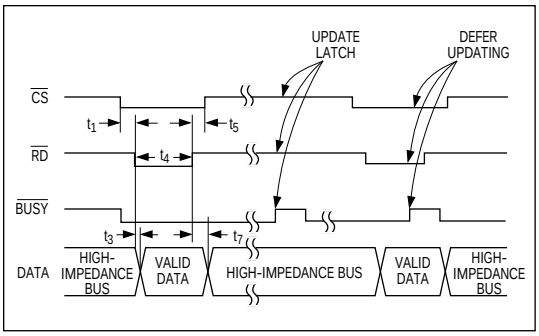


Figure 9. MX7576 Asynchronous Conversion Mode Timing Diagram

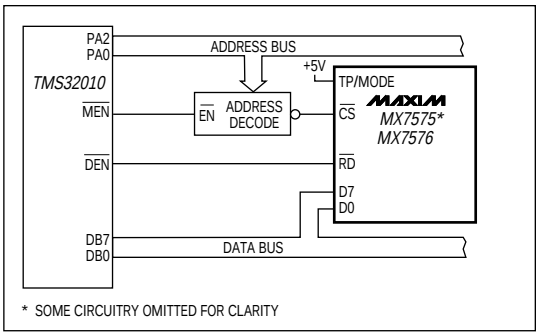


Figure 8. MX7575/MX7576 to TMS32010 ROM Interface

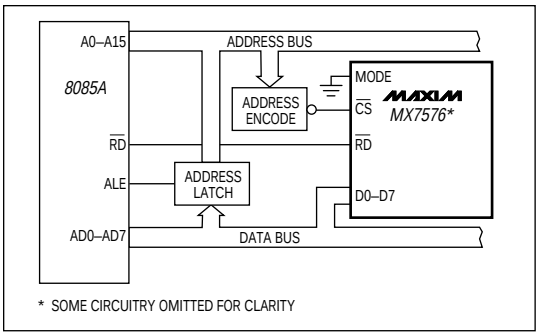


Figure 10. MX7576 to 8085A Asynchronous Conversion Mode Interface

the µP, in that data can be accessed independently of the clock. The output latches are normally updated on the rising edge of $\overline{BUSY}$. But if $\overline{CS}$ and $\overline{RD}$ are low when $\overline{BUSY}$ goes high, the data latches are not updated until one of these inputs returns high. Additionally, the MX7576 stops converting and $\overline{BUSY}$ stays high until $\overline{RD}$ or $\overline{CS}$ goes high. This mode of operation allows a simple interface to the µP.

Processor Interface for Signal Acquisition (MX7575)

In many applications, it is necessary to sample the input signal at exactly equal intervals to minimize errors due to sampling uncertainty or jitter. In order to achieve this objective with the previously discussed interfaces, the user must match software delays or count the number of elapsed clock cycles. This becomes difficult in interrupt-driven systems where the uncertainty in interrupt servicing delays is another complicating factor.

The solution is to use a real-time clock to control the start of a conversion. This should be synchronous with the CLK input to the ADC (both should be derived from the same source), because the sampling instants occur three clock cycles after $\overline{CS}$ and $\overline{RD}$ go low. Therefore, the sampling instants occur at exactly equal intervals if the conversions are started at equal intervals. In this scheme, the output data is fed into a FIFO latch, which allows the µP to access data at its own rate. This guarantees that data is not read from the ADC in the middle of a conversion. If data is read from the ADC during a conversion, the conversion in progress may be disturbed, but the accessed data that belonged to the previous conversion will be correct.

The track/hold starts holding the input on the third falling edge of the clock after $\overline{CS}$ and $\overline{RD}$ go low. If $\overline{CS}$ and $\overline{RD}$ go low within 20ns of a falling clock edge, the ADC may or may not consider this falling edge as the first of the three edges that determine the sampling instant. Therefore, the $\overline{CS}$ and $\overline{RD}$ should not be allowed to go low within this period when sampling accuracy is required.

MX7575 Track/Hold

The track/hold consists of a sampling capacitor and a switch to capture the input signal. The simplified diagram of this block is shown in Figure 11. At the beginning of the conversion, switch S1 is closed, and the input signal is tracked. The input signal is held (switch S1 opens) on the third falling edge of clock after $\overline{CS}$ and $\overline{RD}$ go low (Figure 12). This allows a minimum of two clock cycles for the input capacitor to be charged to the input voltage through the switch resistance. The time required for the hold capacitor to settle to ±1/4LSB is typically 7ns. Therefore, the input signal is allowed ample time to settle before it is acquired by the track/hold. When a conversion ends, switch S1 closes, and the input signal is tracked.

The track/hold is capable of acquiring signals with slew rates of up to 386mV/µs (or equivalently a 50kHz sine wave with 2.46Vp-p amplitude). Figure 13 shows the signal-to-noise ratio (SNR) versus input frequency for the ADC. The SNR plot is generated at a sampling rate of 200kHz using sinusoidal inputs with a peak-to-peak amplitude of 2.46V. The reconstructed sine wave is passed through a 50kHz 8th-order Chebychev filter. The improvement in SNR at high frequencies is due to the filter cutoff.

The switching nature of the analog input results in transient currents that charge the input capacitance of the track/hold. Keep the driving source impedance low (below 2kΩ), so that the settling characteristics of the track/hold are not degraded. A low driving impedance also minimizes undesirable noise pickup and reduces DC errors caused by transient currents at the analog input. As with any ADC, it is important to keep external sources of noise to a minimum during a conversion. Therefore, keep the data bus as quiet as possible during a conversion, especially when the track/hold is making the transition to the hold mode.

For conversion times that are significantly longer than 5µs, the device's accuracy may degrade slightly, as shown in Figure 14. This degradation is due to the charge that is lost from the hold capacitor in the presence of small on-chip leakage currents.

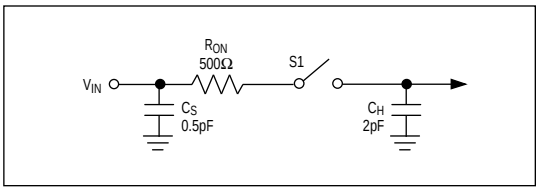


Figure 11. Equivalent Input Circuit

MX7576 Analog Input

The MX7576 analog input can also be modeled with the switch and capacitor as shown in Figure 11. However, unlike the MX7575, the MX7576 samples the input voltage eight times during a conversion (once before each comparator decision). Therefore, the precautions that apply to the MX7575 also apply to the MX7576. These include minimizing the analog source impedance and reducing noise coupling from the digital circuitry during a conversion, especially near a sampling instant.

Reference Input

The high speed of this ADC can be partially attributed to the "inverted voltage output" topology of the DAC that it uses. This topology provides low offset and gain errors and fast settling times. The input current to the DAC, however, is not constant. During a conversion, as different DAC codes are tried, the DC impedance of the DAC can vary between 6kΩ and 18kΩ. Furthermore, when the DAC codes change, small amounts of transient current are drawn from the reference input. These characteristics require a low DC and AC driving impedance for the reference circuitry to minimize conversion errors.

Figure 15 shows the reference circuitry recommended to drive the reference input of the MX7575/MX7576.

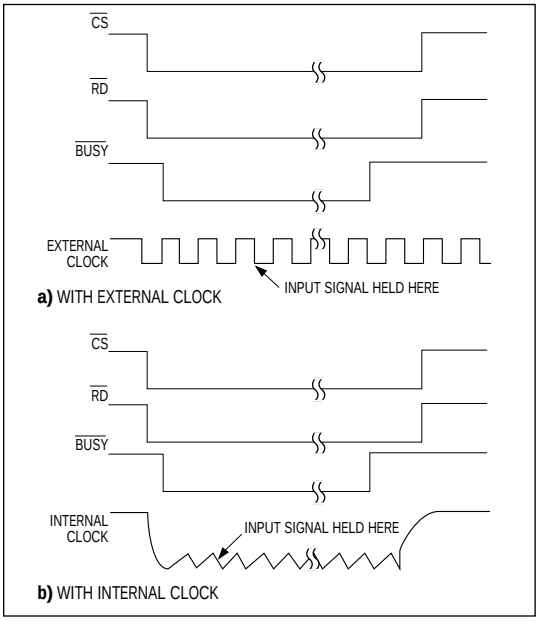


Figure 12. MX7575 Track/Hold (Slow-Memory Interface) Timing Diagrams

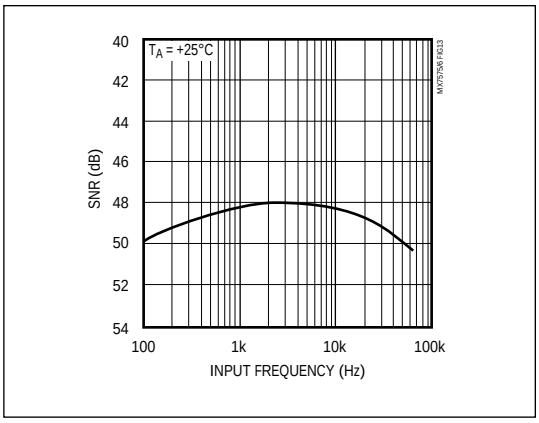


Figure 13. MX7575 SNR vs. Input Frequency

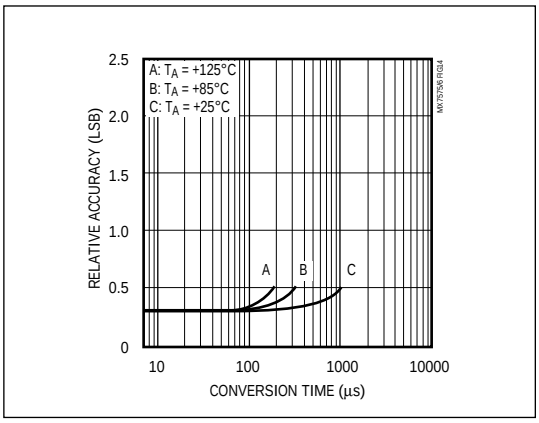


Figure 14. MX7575 Accuracy vs. Conversion Time

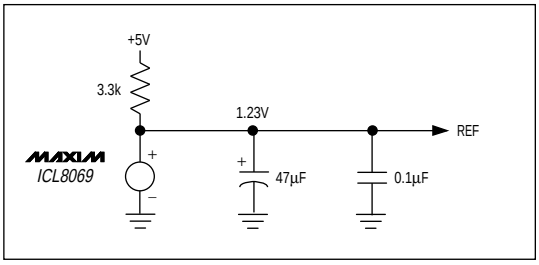


Figure 15. External Reference Circuit

The decoupling capacitors are necessary to provide a low AC source impedance.

Internal/External Clock

The MX7575/MX7576 can be run with either an externally applied clock or their internal clock. In either case, the signal appearing at the clock pin is internally divided by two to provide an internal clock signal that is relatively insensitive to the input clock duty cycle. Therefore, a single conversion takes 20 input clock cycles, which corresponds to 10 internal clock cycles.

Internal Clock

The internal oscillator frequency is set by an external capacitor, C_{CLK}, and an external resistor, R_{CLK}, which are connected as shown in Figure 16a. During a conversion, a sawtooth waveform is generated on the CLK pin by charging C_{CLK} through R_{CLK} and discharging it through an internal switch. At the end of a conversion, the internal oscillator is shut down by clamping the CLK pin to V_{DD} through an internal switch. The circuit for the internal oscillator can easily be overdriven with an external clock source.

The internal oscillator provides a convenient clock source for the MX7575. Figure 17 shows typical conversion times versus temperature for the recommended R_{CLK} and C_{CLK} combination. Due to process variations, the oscillation frequency for this R_{CLK}/C_{CLK} combination may vary by as much as ±50% from the nominal value shown in Figure 17. Therefore, an external clock should be used in the following situations:

1) Applications that require the conversion time to be within 50% of the minimum conversion time for the specified accuracy (5µs MX7575/10µs MX7576).
2) Applications in which time-related software constraints cannot accommodate conversion-time differences that may occur from unit to unit or over temperature for a given device.

External Clock

The CLK input of the MX7575/MX7576 may be driven directly by a 74HC or 4000B series buffer (e g., 4049), or by an LS TTL output with a 5.6kΩ pull-up resistor. At the end of a conversion, the device ignores the clock input and disables its internal clock signal. Therefore, the external clock may continue to run between conversions without being disabled. The duty cycle of the external clock may vary from 30% to 70%. As discussed previously, in order to maintain accuracy, clock rates significantly lower than the data sheet limits (4MHz for MX7575 and 2MHz for MX7576) should not be used.

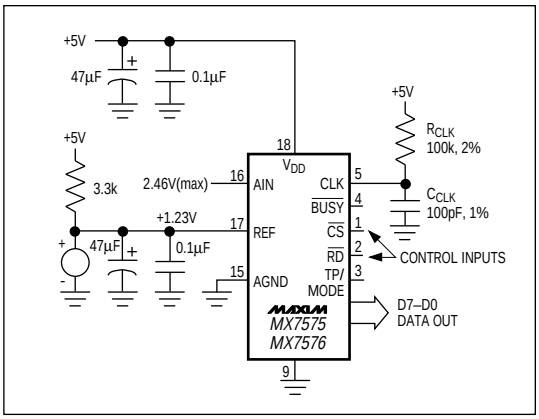


Figure 16a. Unipolar Configuration

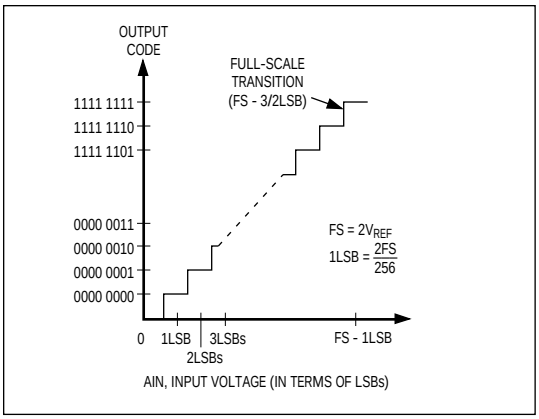


Figure 16b. Nominal Transfer Characteristic for Unipolar Operation

Typical Applications

Unipolar Operation

Figure 16a shows the analog circuit connections for unipolar operation, and Figure 16b shows the nominal transfer characteristic for unipolar operation. Since the offset and full-scale errors of the MX7575/MX7576 are very small, it is not necessary to null these errors in most cases. If calibration is required, follow the steps in the sections below.

Offset Adjust

The offset error can be adjusted by using the offset trim capability of an op amp (when it is used as a voltage follower) to drive the analog input, AIN. The op amp should have a common-mode input range that includes 0V. Set its initial input to 4.8mV (1/2LSB), while varying its offset until the ADC output code flickers between 0000 0000 and 0000 0001.

Full-Scale Adjustment

Make the full-scale adjustment by forcing the analog input, AIN, to 2.445V (FS - 3/2LSB). Then vary the reference input voltage until the ADC output code flickers between 1111 1110 and 1111 1111.

Bipolar Operation

Figure 18a shows an example of the circuit connection for bipolar operation, and Figure 18b shows the nominal transfer characteristic for bipolar operation. The output code provided by the MX7575 is offset binary. The analog input range for this circuit is ±2.46V (1LSB = 19.22mV), even though the voltage appearing at AIN is in the 0V to 2.46V range. In most cases, the MX7575 is accurate enough that calibration will not be necessary. If calibration is not needed, resistors R1–R7 should have a 0.1% tolerance, with R4 and R5 replaced by one 10kΩ resistor, and R2 and R3 with one 1kΩ resistor. If calibration is required, follow the steps in the sections below.

Offset Adjust

Adjust the offset error by applying an analog input voltage of 2.43V (+FS - 3/2LSB). Then adjust resistor R5 until the output code flickers between 1111 1110 and 1111 1111.

Full-Scale Adjust

Null the full-scale error by applying an analog input voltage of -2.45V (-FS + 1/2LSB). Then adjust resistor R3 until the output code flickers between 0000 0000 and 0000 0001.

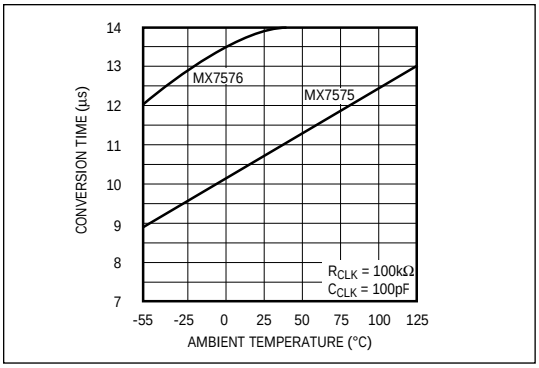


Figure 17. Typical Conversion Times vs. Temperature Using Internal Clock

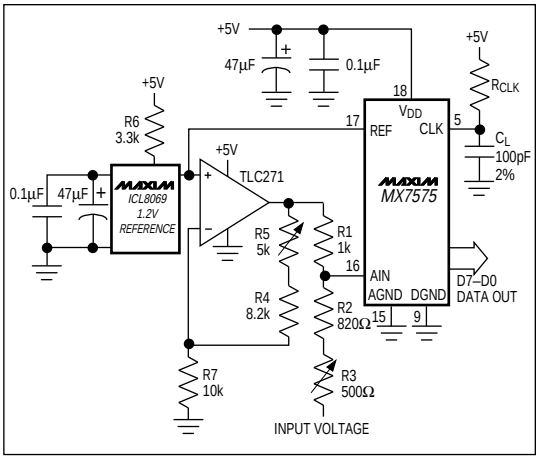


Figure 18a. MX7575 Bipolar Configuration

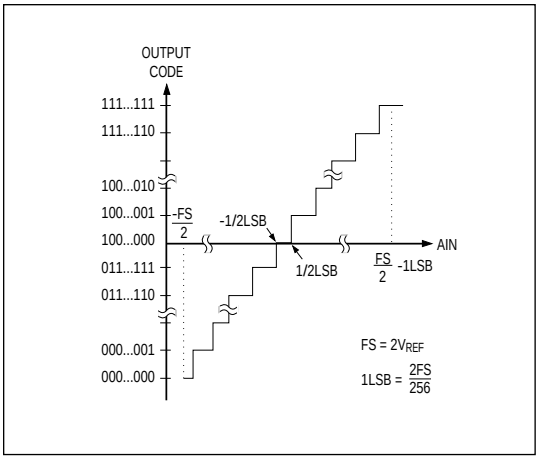


Figure 18b. Nominal Transfer Characteristic for Bipolar Operation

Applications Information

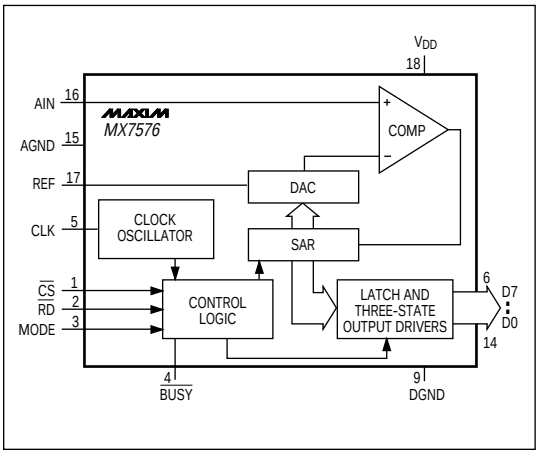
Noise

To minimize noise coupling, keep both the input signal lead to AIN and the signal return lead from AGND as short as possible. If this is not possible, a shielded cable or a twisted-pair transmission line is recommended. Additionally, potential differences between the ADC ground and the signal-source ground should be minimized, since these voltage differences appear as errors superimposed on the input signal. To minimize system noise pickup, keep the driving source resistance below 2kΩ.

Proper Layout

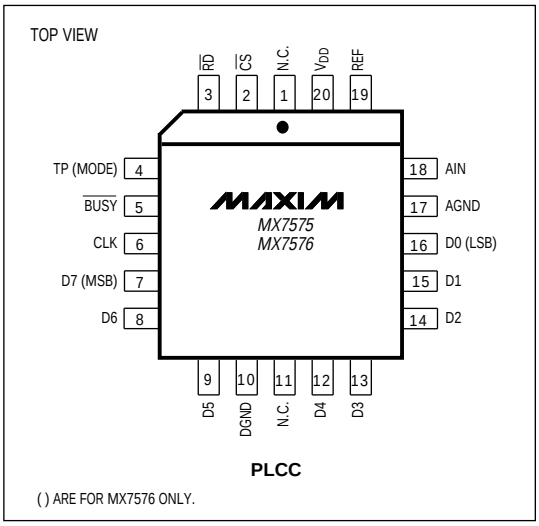
For PC board layouts, take care to keep digital lines well separated from any analog lines. Establish a single-point, analog ground (separate from the digital system ground) near the MX7575/MX7576. This analog ground point should be connected to the digital system ground through a single-track connection only. Any supply or reference bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point.

Functional Diagrams (continued)



CMOS, µP-Compatible, 5µs/10µs, 8-Bit ADCs

Pin Configurations (continued)



PLCC

( ) ARE FOR MX7576 ONLY.

Ordering Information (continued)

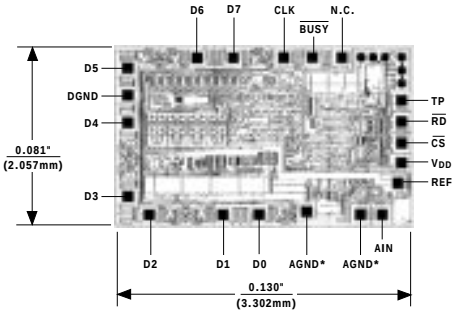
PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MX7575JEWN	-40°C to +85°C	18 Wide SO	±1
MX7575KEWN	-40°C to +85°C	18 Wide SO	±1/2
MX7575JEQP	-40°C to +85°C	20 PLCC	±1
MX7575KEQP	-40°C to +85°C	20 PLCC	±1/2
MX7575SQ	-55°C to +125°C	18 CERDIP**	±1
MX7575TQ	-55°C to +125°C	18 CERDIP**	±1/2
MX7576JN	0°C to +70°C	18 Plastic DIP	±1
MX7576KN	0°C to +70°C	18 Plastic DIP	±1/2
MX7576JCWN	0°C to +70°C	18 Wide SO	±1
MX7576KCWN	0°C to +70°C	18 Wide SO	±1/2
MX7576JP	0°C to +70°C	20 PLCC	±1
MX7576KP	0°C to +70°C	20 PLCC	±1/2
MX7576J/D	0°C to +70°C	Dice*	±1
MX7576AQ	-25°C to +85°C	18 CERDIP**	±1
MX7576BQ	-25°C to +85°C	18 CERDIP**	±1/2
MX7576JEWN	-40°C to +85°C	18 Wide SO	±1
MX7576KEWN	-40°C to +85°C	18 Wide SO	±1/2
MX7576JEQP	-40°C to +85°C	20 PLCC	±1
MX7576KEQP	-40°C to +85°C	20 PLCC	±1/2
MX7576SQ	-55°C to +125°C	18 CERDIP**	±1
MX7576TQ	-55°C to +125°C	18 CERDIP**	±1/2

** Contact factory for dice specifications.*

*** Contact factory for availability.*

Chip Topographies

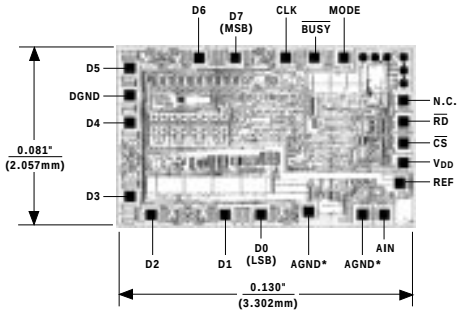
MX7575



*The two AGND pads must both be used (bonded together).

TRANSISTOR COUNT: 768
SUBSTRATE CONNECTED TO VDD

MX7576



*The two AGND pads must both be used (bonded together).

TRANSISTOR COUNT: 768
SUBSTRATE CONNECTED TO VDD

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View MX7576KEQP+ on WIN SOURCE
- Maxim Integrated Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management