ELECTRONICS

THE DATASHEET OF

MW7IC2220NBR1

Freescale Semiconductor
Technical Data

Document Number: MW7IC2220N
Rev. 2, 5/2011

RF LDMOS Wideband Integrated Power Amplifiers

MW7IC2220NR1
MW7IC2220GNR1
MW7IC2220NBR1

The MW7IC2220N wideband integrated circuit is designed with on-chip matching that makes it usable from 2000 to 2200 MHz. This multi-stage structure is rated for 24 to 32 Volt operation and covers all typical cellular base station modulation formats including TD-SCDMA.

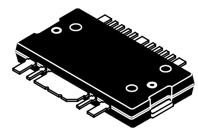
- Typical Single-Carrier W-CDMA Performance: V_{DD} = 28 Volts, I_{DQ1} = 80 mA, I_{DQ2} = 300 mA, P_{out} = 2 Watts Avg., f = 2167.5 MHz, IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.
  - Power Gain — 31 dB
  - Power Added Efficiency — 13%
  - ACPR @ 5 MHz Offset — -50 dBc in 3.84 MHz Bandwidth
- Capable of Handling 5:1 VSWR, @ 28 Vdc, 2140 MHz, 20 Watts CW Output Power
- Stable into a 5:1 VSWR. All Spurs Below -60 dBc @ 100 mW to 5 Watts CW P_{out}.
- Typical P_{out} @ 1 dB Compression Point $\simeq$ 20 Watts CW

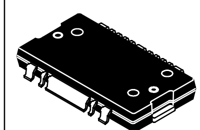
Features

- Characterized with Series Equivalent Large-Signal Impedance Parameters and Common Source S-Parameters
- On-Chip Matching (50 Ohm Input, DC Blocked, >3 Ohm Output)
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function [1]
- Integrated ESD Protection
- 225°C Capable Plastic Package
- RoHS Compliant
- In Tape and Reel. R1 Suffix = 500 Units, 44 mm Tape Width, 13 inch Reel.

2110-2170 MHz, 2 W Avg., 28 V SINGLE W-CDMA RF LDMOS WIDEBAND INTEGRATED POWER AMPLIFIERS

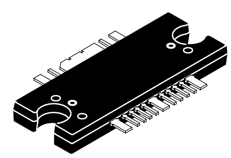
CASE 1886-01
TO-270 WB-16
PLASTIC
MW7IC2220NR1





CASE 1887-01
TO-270 WB-16 GULL
PLASTIC
MW7IC2220GNR1

CASE 1329-09
TO-272 WB-16
PLASTIC
MW7IC2220NBR1



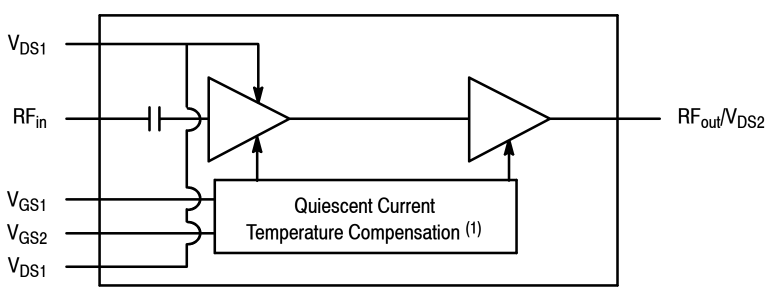
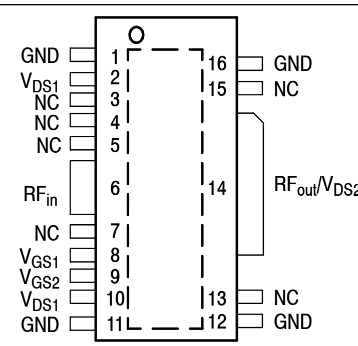


Figure 1. Functional Block Diagram



(Top View)

Note: Exposed backside of the package is the source terminal for the transistors.

Figure 2. Pin Connections

1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1977 or AN1987.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +5	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature [1,2]	T_J	225	°C
Input Power	P_{in}	20	dBm

Table 2. Thermal Characteristics

Characteristic		Symbol	Value [2,3]	Unit
Thermal Resistance, Junction to Case		$R_{\theta JC}$		°C/W
2 W Avg. (P_{out} = 2 W CW, Case Temperature = 78°C)	Stage 1, 28 Vdc, I_{DQ1} = 80 mA		4.3	
	Stage 2, 28 Vdc, I_{DQ2} = 300 mA		1.5	
20 W Avg. (P_{out} = 20 W CW, Case Temperature = 82°C)	Stage 1, 28 Vdc, I_{DQ1} = 80 mA		4.3	
	Stage 2, 28 Vdc, I_{DQ2} = 300 mA		1.25	

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	0 (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	III (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Stage 1 — Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Stage 1 — On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 23 μAdc)	$V_{GS(th)}$	1.2	2	2.7	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_{DQ1} = 80 mAdc)	$V_{GS(Q)}$	—	2.8	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DQ1} = 80 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	9.5	12.2	16.5	Vdc

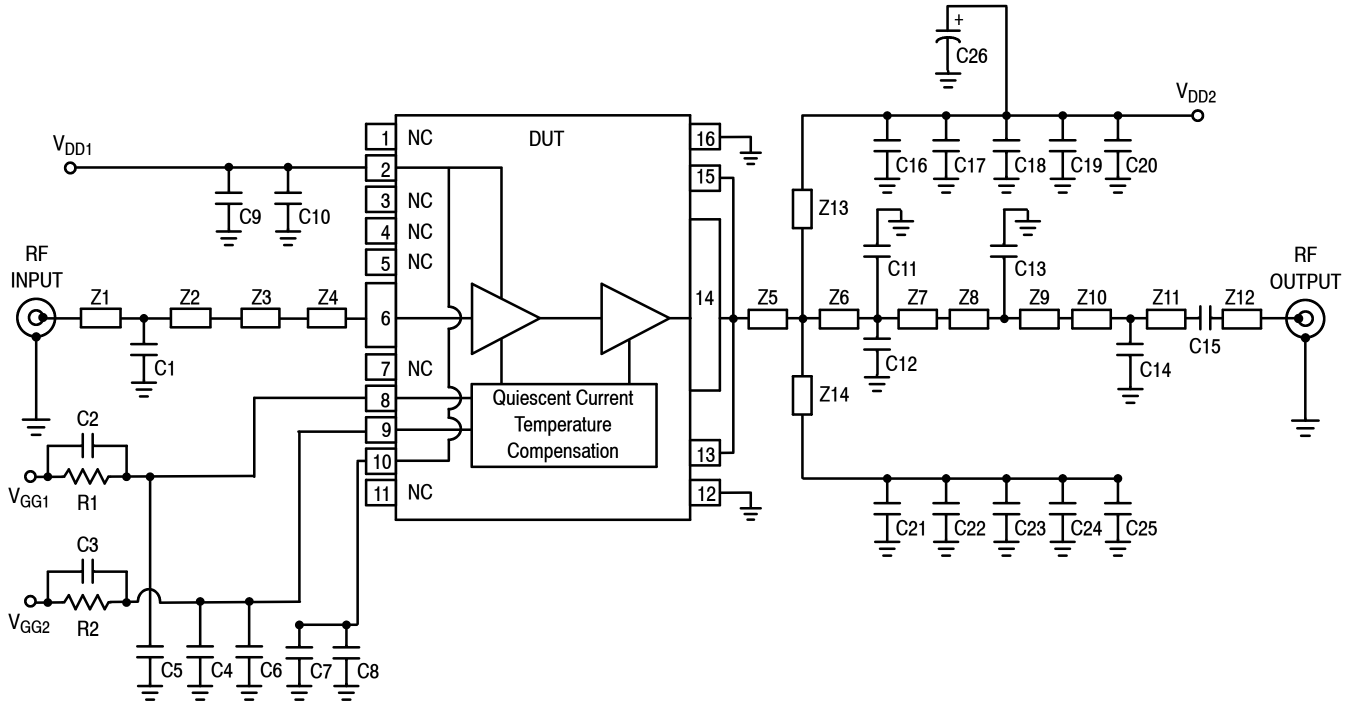
1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

(continued)

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Stage 2 — Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Stage 2 — On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 150 μAdc)	$V_{GS(th)}$	1.2	2	2.7	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_{DQ2} = 300 mAdc)	$V_{GS(Q)}$	—	2.7	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DQ2} = 300 mAdc, Measured in Functional Test)	$V_{GG(Q)}$	7	8	12.5	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	0.2	0.39	1.2	Vdc
Stage 2 — Dynamic Characteristics (1)					
Output Capacitance (V_{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	205	—	pF
Functional Tests (In Freescale Wideband 2110-2170 MHz Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1} = 80 mA, I_{DQ2} = 300 mA, P_{out} = 2 W Avg., f = 2167.5 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	29	31	34	dB
Power Added Efficiency	PAE	11	13	—	%
Adjacent Channel Power Ratio	ACPR	—	-50	-47	dBc
Input Return Loss	IRL	—	-14	-12	dB
Typical Performances (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ1} = 80 mA, I_{DQ2} = 300 mA, 2110-2170 MHz					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	20	—	W
IMD Symmetry @ 18 W PEP, P_{out} where IMD Third Order Intermodulation ≅ 30 dBc (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands > 2 dB)	IMD_{sym}	—	40	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	70	—	MHz
Gain Flatness in 60 MHz Bandwidth @ P_{out} = 2 W Avg.	G_F	—	0.6	—	dB
Average Deviation from Linear Phase in 60 MHz Bandwidth @ P_{out} = 20 W CW	Φ	—	1.2	—	°
Average Group Delay @ P_{out} = 20 W CW, f = 2140 MHz	Delay	—	2.5	—	ns
Part-to-Part Insertion Phase Variation @ P_{out} = 20 W CW, f = 2140 MHz, Six Sigma Window	ΔΦ	—	15	—	°
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.036	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	ΔP1dB	—	0.003	—	dB/°C

1. Part internally matched both on input and output.



Z1	0.090″ x 0.083″ Microstrip	Z8	0.263″ x 0.123″ Microstrip
Z2	2.107″ x 0.083″ Microstrip	Z9	0.125″ x 0.123″ Microstrip
Z3	0.016″ x 0.083″ x 0.055″ Taper	Z10	0.280″ x 0.083″ Microstrip
Z4	0.106″ x 0.055″ Microstrip	Z11	0.373″ x 0.083″ Microstrip
Z5	0.570″ x 0.322″ Microstrip	Z12	0.364″ x 0.083″ Microstrip
Z6	0.204″ x 0.322″ Microstrip	Z13, Z14	1.042″ x 0.083″ Microstrip
Z7	0.050″ x 0.322″ Microstrip	PCB	Arlon CuClad 250GX-0300-55-22, 0.030″, ε_r = 2.55

Figure 3. MW7IC2220NR1(GNR1)(NBR1) Test Circuit Schematic

Table 6. MW7IC2220NR1(GNR1)(NBR1) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	0.1 pF Chip Capacitor	ATC100B0R1JT500XT	ATC
C2, C3	8.2 pF Chip Capacitors	ATC100B8R2BT500XT	ATC
C4	4.7 μF, 50 V Chip Capacitor	C4532X7R1H475KT	TDK
C5, C6	0.4 pF Chip Capacitors	ATC100B0R4JT500XT	ATC
C7, C9	10 μF, 50 V Chip Capacitors	C3225Y5V1H106ZT	TDK
C8, C10	5.6 pF Chip Capacitors	ATC100B5R6JT500XT	ATC
C11, C12	0.3 pF Chip Capacitors	ATC100B0R3JT500XT	ATC
C13	0.8 pF Chip Capacitor	ATC100B0R8JT500XT	ATC
C14	1.1 pF Chip Capacitor	ATC100B1R1JT500XT	ATC
C15, C16, C21	9.1 pF Chip Capacitors	ATC100B9R1JT500XT	ATC
C17, C22	0.1 μF, 250 V Chip Capacitors	C3216X7R2E104KT	TDK
C18, C23	6.8 μF, 50 V Chip Capacitors	C4532X7R1H685KT	TDK
C19, C24	4.7 μF, 50 V Chip Capacitors	C4532X7R1H475KT	TDK
C20, C25	10 μF, 50 V Chip Capacitors	C3225Y5V1H106ZT	TDK
C26	470 μF, 63 V Electrolytic Capacitor	477KXM063M	Illinois Capacitor
R1, R2	10 kΩ, 1/4 W Chip Resistors	CRCW12061002FKEA	Vishay

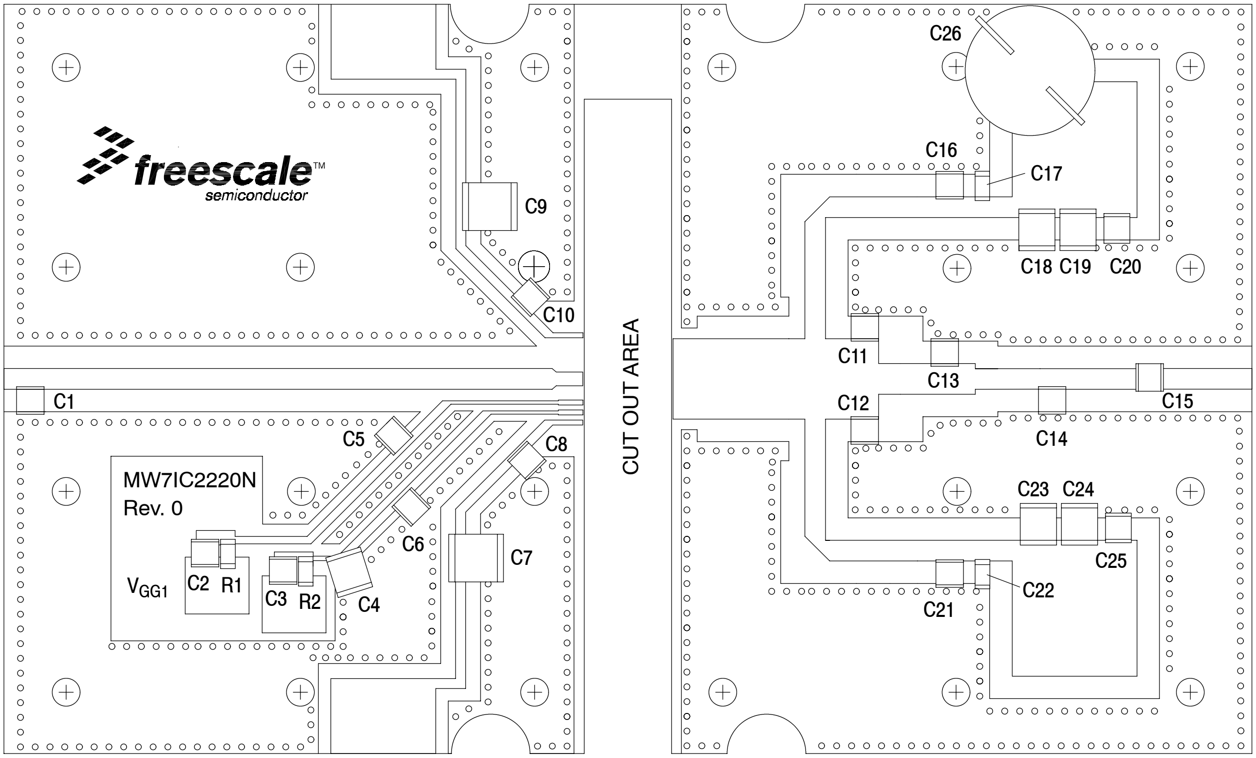


Figure 4. MW7IC2220NR1(GNR1)(NBR1) Test Circuit Component Layout

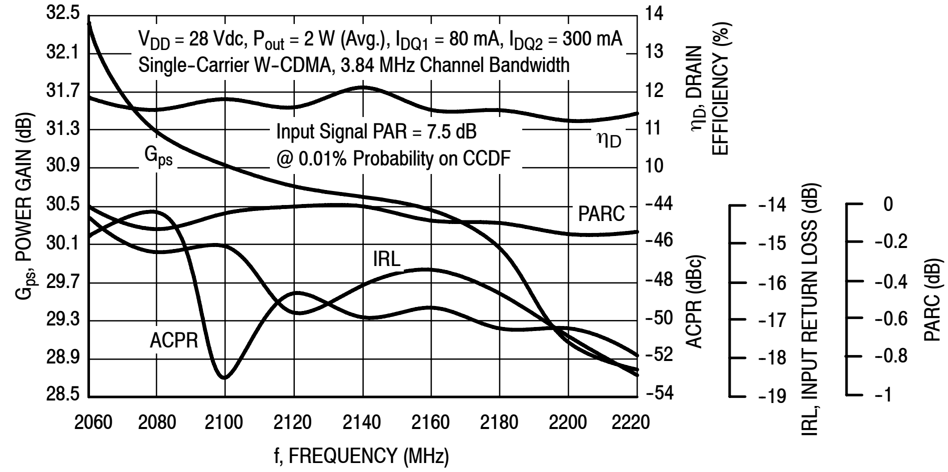


Figure 5. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 2 Watts Avg.

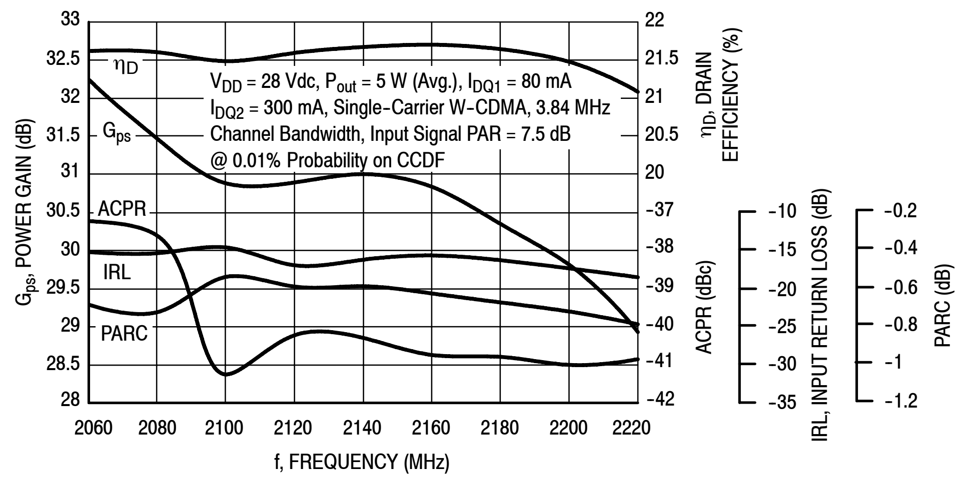


Figure 6. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 5 Watts Avg.

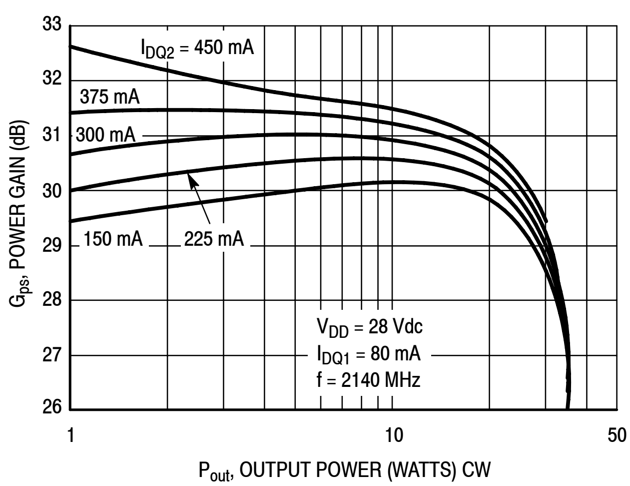


Figure 7. Power Gain versus Output Power @ I_{DQ1} = 80 mA

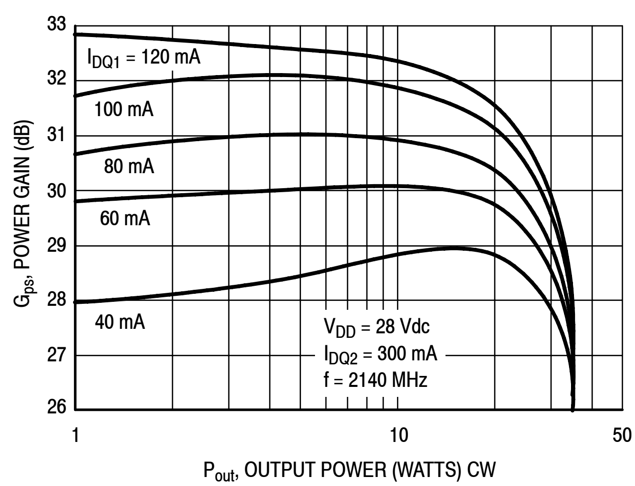


Figure 8. Power Gain versus Output Power @ I_{DQ2} = 300 mA

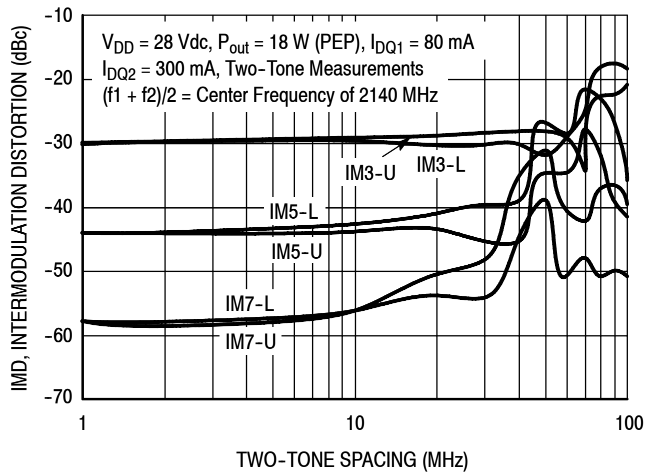


Figure 9. Intermodulation Distortion Products versus Tone Spacing

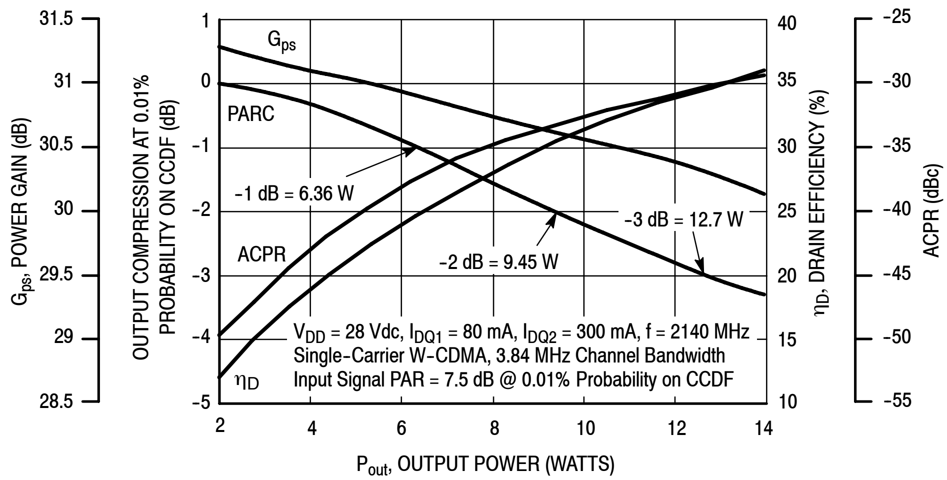


Figure 10. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

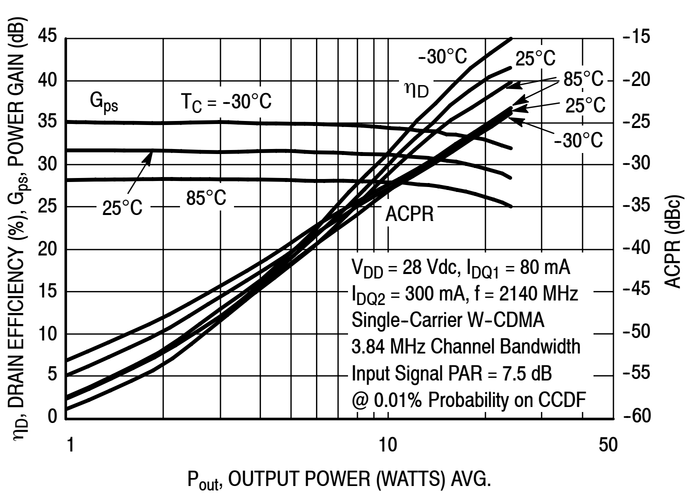


Figure 11. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

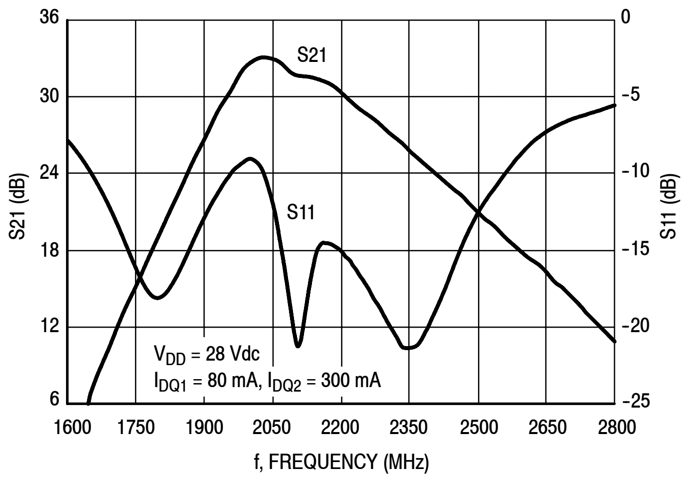


Figure 12. Broadband Frequency Response

W-CDMA TEST SIGNAL

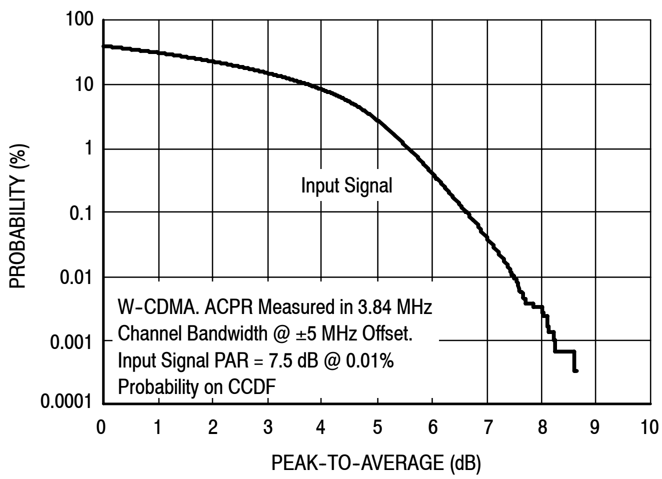


Figure 13. CCDF W-CDMA IQ Magnitude Clipping, Single-Carrier Test Signal

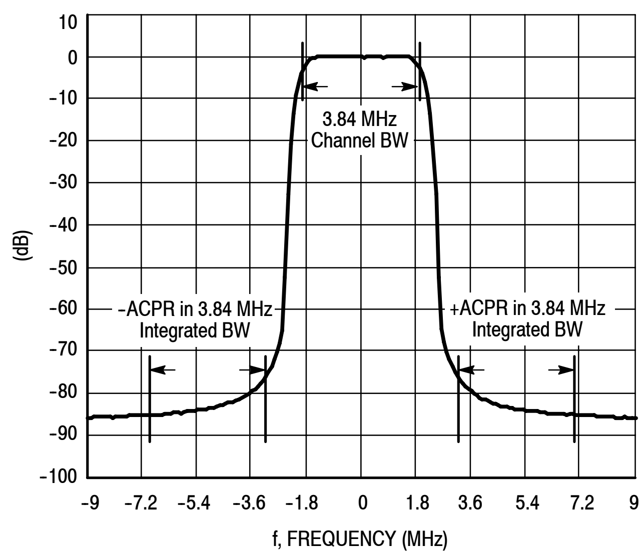
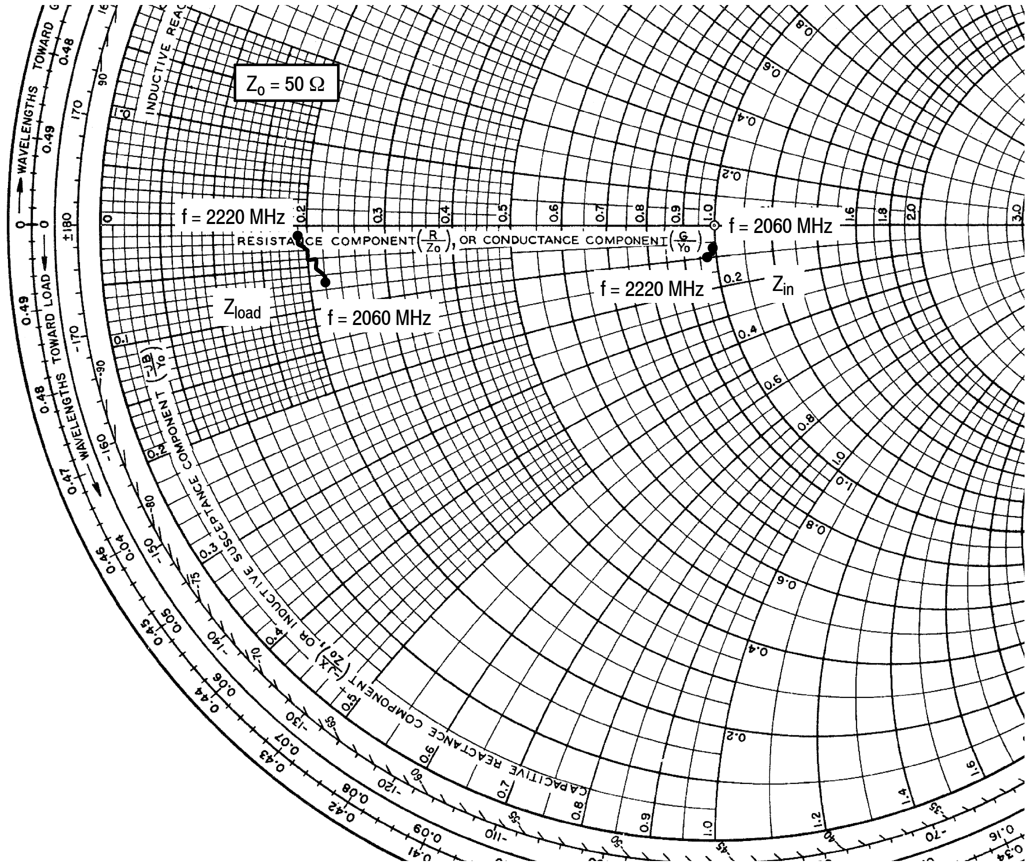


Figure 14. Single-Carrier W-CDMA Spectrum



V_{DD} = 28 Vdc, I_{DQ1} = 80 mA, I_{DQ2} = 300 mA, P_{out} = 2 W Avg.

f MHz	Z_{in} Ω	Z_{load} Ω
2060	49.57 – j3.62	11.06 – j3.26
2080	49.49 – j3.77	10.83 – j2.96
2100	49.42 – j3.94	10.55 – j2.62
2120	49.35 – j4.12	10.30 – j2.23
2140	49.30 – j4.29	10.08 – j1.86
2160	49.25 – j4.48	9.86 – j1.51
2180	49.21 – j4.67	9.65 – j1.13
2200	49.17 – j4.86	9.45 – j0.76
2220	49.15 – j5.06	9.25 – j0.40

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

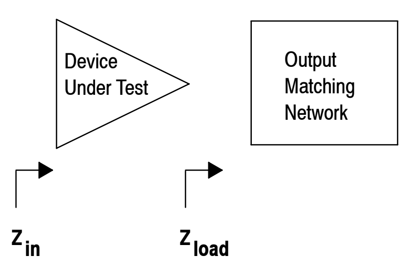


Figure 15. Series Equivalent Input and Load Impedance

Table 7. Common Source S-Parameters (V_{DD} = 28 V, I_{DQ1} = 90 mA, I_{DQ2} = 420 mA, T_A = 25°C, 50 Ohm System)

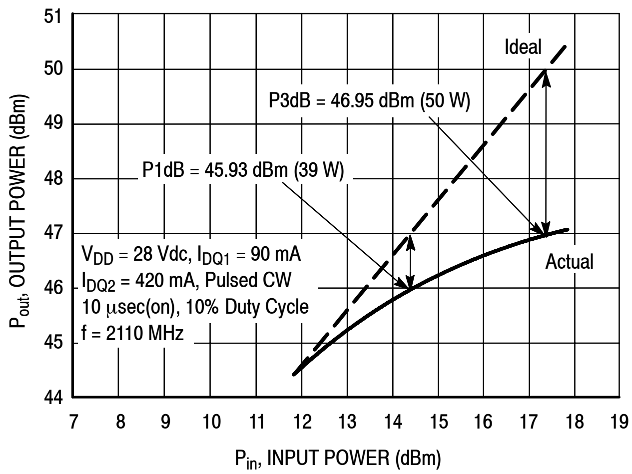
f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
1500	0.452	134	0.356	7.81	0.001	-108	0.979	160
1550	0.407	117	0.757	-7.8	0.000	-67.7	0.969	157
1600	0.354	96.5	1.430	-31	0.000	-65.8	0.955	154
1650	0.316	85.1	2.330	-52.1	0.001	-27.1	0.935	151
1700	0.279	68	3.690	-73.6	0.001	-43.4	0.909	148
1750	0.222	49.5	5.800	-93.3	0.002	-21.9	0.878	143
1800	0.140	30.4	9.570	-113	0.003	-24.8	0.833	137
1850	0.046	21.9	17.000	-137	0.004	-33.7	0.737	124
1900	0.094	135	33.600	-173	0.007	-41.8	0.476	91.7
1950	0.238	56.4	58.300	124	0.009	-86.4	0.396	-79.7
2000	0.254	-29.2	47.800	59.5	0.006	-118	0.873	-149
2050	0.241	-84.1	34.300	22.9	0.004	-122	0.927	-171
2100	0.252	-120	27.700	-3.98	0.004	-125	0.911	-179
2150	0.201	-142	23.900	-28.2	0.003	-128	0.891	177
2200	0.174	-162	21.100	-51.8	0.003	-130	0.878	175
2250	0.148	168	18.800	-75.9	0.003	-131	0.872	175
2300	0.135	103	15.800	-100	0.003	-139	0.882	175
2350	0.197	35.4	12.600	-118	0.003	-155	0.906	174
2400	0.244	1.73	11.100	-132	0.002	-156	0.919	173
2450	0.291	-11.1	10.400	-147	0.002	-157	0.926	171
2500	0.340	-19	9.750	-163	0.002	-147	0.933	170
2550	0.391	-26.9	9.230	-179	0.001	-150	0.938	169
2600	0.435	-35.2	8.760	164	0.001	-144	0.942	168
2650	0.475	-44.4	8.290	146	0.001	-137	0.945	166
2700	0.455	-46	7.050	129	0.001	-90.2	0.950	166
2750	0.535	-60.2	6.690	112	0.001	-106	0.955	164
2800	0.571	-71.2	5.980	95.1	0.001	-103	0.955	163
2850	0.598	-82	5.170	78.5	0.002	-96.5	0.954	162
2900	0.623	-92.9	4.370	63.1	0.002	-103	0.955	162
2950	0.643	-102	3.690	48.7	0.002	-96.2	0.954	161
3000	0.668	-109	3.100	35.4	0.002	-106	0.951	161
3050	0.681	-116	2.580	22.7	0.002	-107	0.952	161
3100	0.694	-121	2.130	11	0.002	-87.9	0.957	160
3150	0.712	-124	1.760	-0.057	0.002	-96.1	0.959	160
3200	0.724	-127	1.440	-10.9	0.002	-99.6	0.959	160
3250	0.726	-130	1.170	-21.1	0.002	-82.4	0.962	159
3300	0.705	-130	0.928	-28.7	0.003	-66.9	0.963	159
3350	0.743	-132	0.780	-37	0.003	-77.2	0.959	158
3400	0.748	-135	0.652	-44.3	0.003	-88	0.955	157
3450	0.753	-137	0.555	-50.3	0.003	-78.6	0.955	156

(continued)

Table 7. Common Source S-Parameters (V_{DD} = 28 V, I_{DQ1} = 90 mA, I_{DQ2} = 420 mA, T_A = 25°C, 50 Ohm System) **(continued)**

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$\|S_{11}\|$	∠ φ	$\|S_{21}\|$	∠ φ	$\|S_{12}\|$	∠ φ	$\|S_{22}\|$	∠ φ
3500	0.759	-140	0.486	-56.1	0.004	-81.1	0.954	155
3550	0.765	-144	0.440	-62.4	0.004	-82	0.946	154
3600	0.770	-148	0.401	-69.7	0.004	-85.9	0.941	153
3650	0.774	-153	0.370	-77.4	0.005	-96.4	0.941	151
3700	0.780	-159	0.338	-85.1	0.006	-94.9	0.940	150
3750	0.795	-164	0.306	-93.2	0.006	-99.3	0.933	148
3800	0.810	-170	0.273	-101	0.008	-110	0.928	146
3850	0.821	-175	0.239	-107	0.008	-113	0.934	145
3900	0.839	-178	0.207	-111	0.008	-112	0.936	144
3950	0.855	179	0.178	-114	0.008	-117	0.927	144
4000	0.862	176	0.156	-116	0.008	-123	0.935	144

ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS

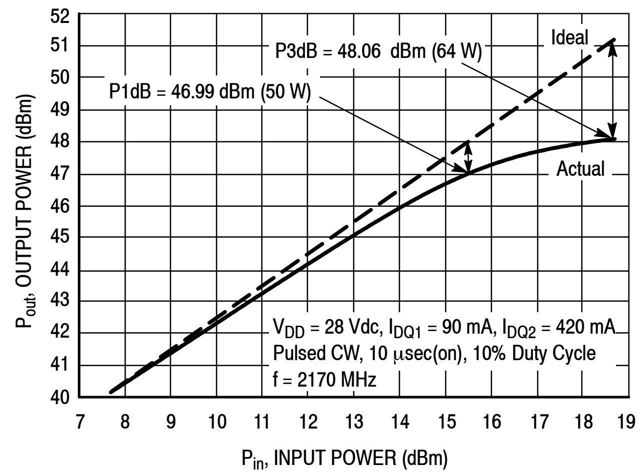


NOTE: Load Pull Test Fixture Tuned for Peak P1dB Output Power @ 28 V

Test Impedances per Compression Level

	Z_{source} Ω	Z_{load} Ω
P1dB	40.41 + j2.31	3.13 − j4.89

Figure 16. Pulsed CW Output Power versus Input Power @ 28 V @ 2110 MHz

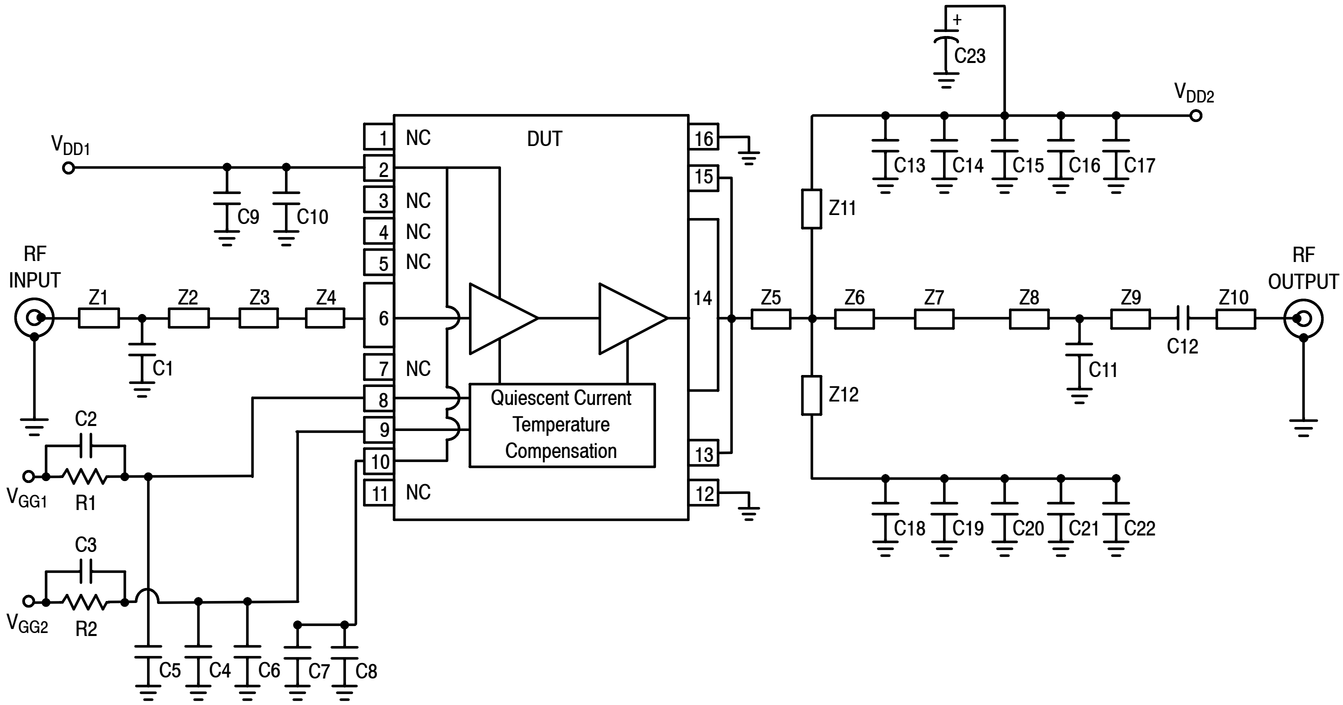


NOTE: Load Pull Test Fixture Tuned for Peak P1dB Output Power @ 28 V

Test Impedances per Compression Level

	Z_{source} Ω	Z_{load} Ω
P1dB	44.66 − j5.79	3.06 − j5.22

Figure 17. Pulsed CW Output Power versus Input Power @ 28 V @ 2170 MHz



Z1	0.090″ x 0.083″ Microstrip	Z7	0.388″ x 0.123″ Microstrip
Z2	2.107″ x 0.083″ Microstrip	Z8	0.330″ x 0.083″ Microstrip
Z3	0.016″ x 0.083″ x 0.055″ Taper	Z9	0.323″ x 0.083″ Microstrip
Z4	0.106″ x 0.055″ Microstrip	Z10	0.364″ x 0.083″ Microstrip
Z5	0.570″ x 0.322″ Microstrip	Z11, Z12	1.042″ x 0.083″ Microstrip
Z6	0.254″ x 0.322″ Microstrip	PCB	Arlon CuClad 250GX-0300-55-22, 0.030″, ε_r = 2.55

Figure 18. MW7IC2220NR1(GNR1)(NBR1) Test Circuit Schematic — TD-SCDMA

Table 8. MW7IC2220NR1(GNR1)(NBR1) Test Circuit Component Designations and Values — TD-SCDMA

Part	Description	Part Number	Manufacturer
C1	1 pF Chip Capacitor	ATC100B1R0JT500XT	ATC
C2, C3	8.2 pF Chip Capacitors	ATC100B8R2BT500XT	ATC
C4	4.7 μF, 50 V Chip Capacitor	C4532X7R1H475KT	TDK
C5, C6	0.4 pF Chip Capacitors	ATC100B0R4JT500XT	ATC
C7, C9	10 μF, 50 V Chip Capacitors	C3225Y5V1H106ZT	TDK
C8, C10	5.6 pF Chip Capacitors	ATC100B5R6JT500XT	ATC
C11	1.1 pF Chip Capacitor	ATC100B1R1JT500XT	ATC
C12, C13, C18	9.1 pF Chip Capacitors	ATC100B9R1JT500XT	ATC
C14, C19	0.1 μF, 250 V Chip Capacitors	C3216X7R2E104KT	TDK
C15, C20	6.8 μF, 50 V Chip Capacitors	C4532X7R1H685KT	TDK
C16, C21	4.7 μF, 50 V Chip Capacitors	C4532X7R1H475KT	TDK
C17, C22	10 μF, 50 V Chip Capacitors	C3225Y5V1H106ZT	TDK
C23	470 μF, 63 V Electrolytic Capacitor	477KXM063M	Illinois Capacitor
R1, R2	11 Ω, 1/4 W Chip Resistors	CRCW120611R0FKEA	Vishay

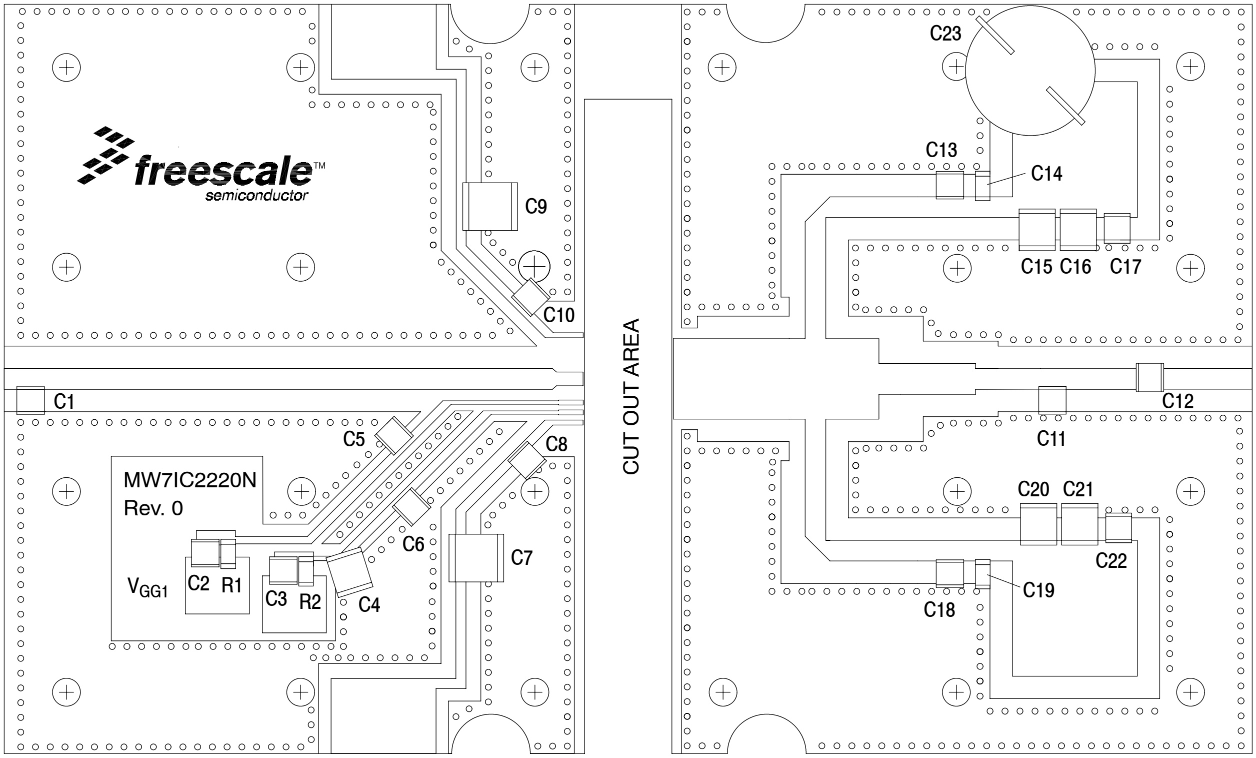


Figure 19. MW7IC2220NR1(GNR1)(NBR1) Test Circuit Component Layout — TD-SCDMA

TYPICAL CHARACTERISTICS

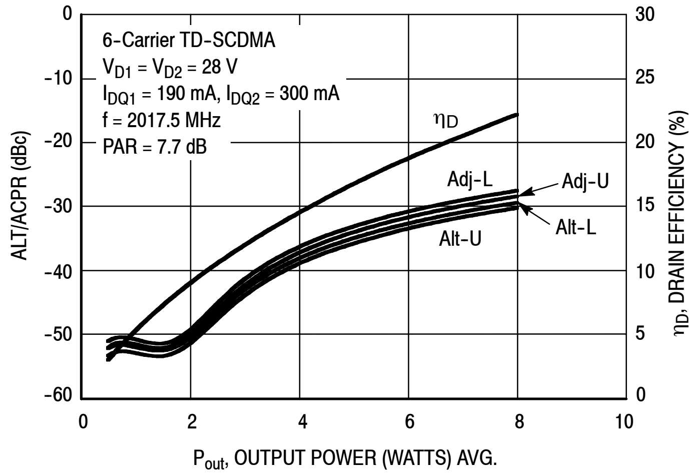


Figure 20. 6-Carrier TD-SCDMA ACPR, ALT and Drain Efficiency versus Output Power

TD-SCDMA TEST SIGNAL

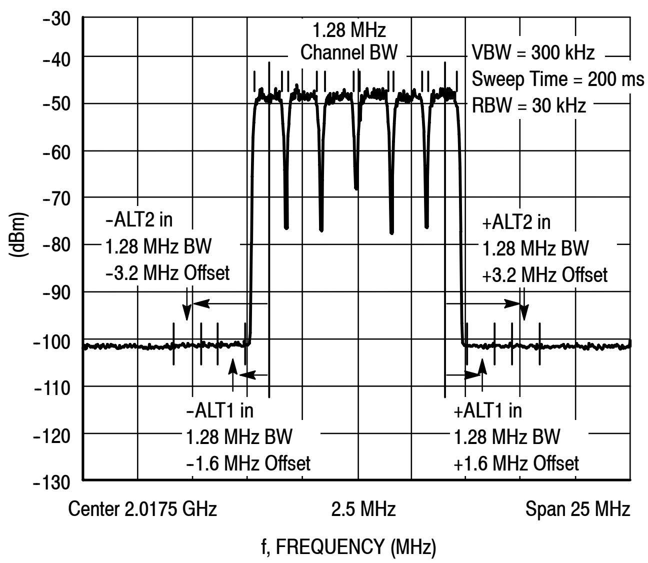
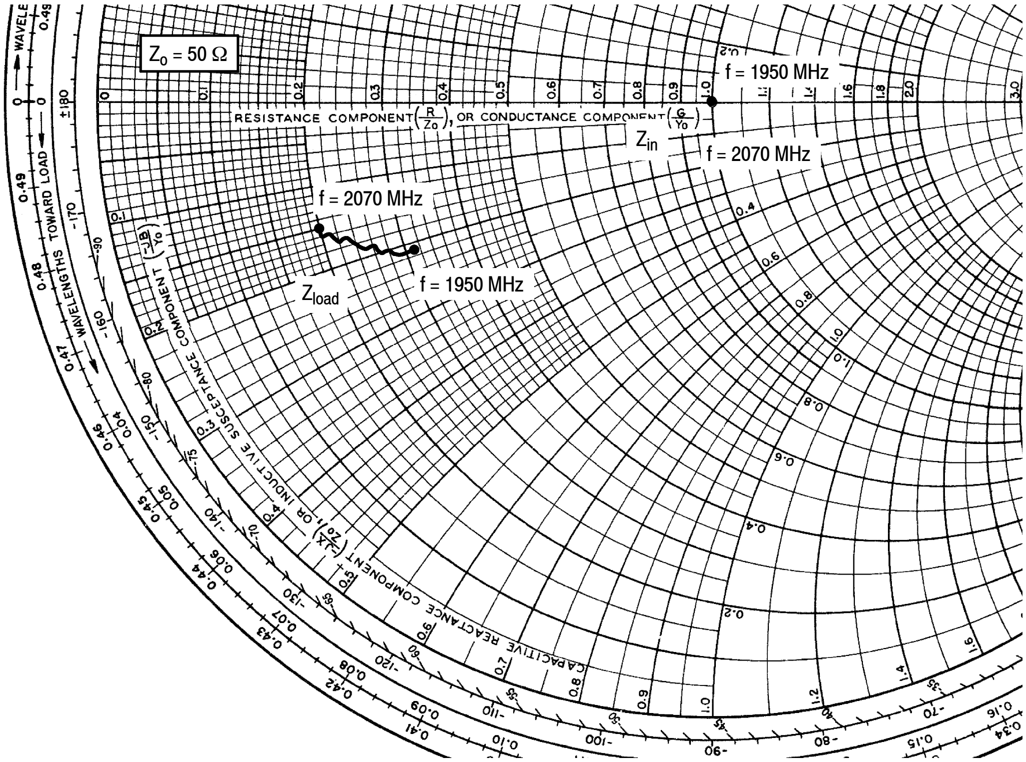


Figure 21. 6-Carrier TD-SCDMA Spectrum



V_{DD} = 28 Vdc, I_{DQ1} = 190 mA, I_{DQ2} = 300 mA

f MHz	Z_{in} Ω	Z_{load} Ω
1950	50 + j0	15.539 - j10.702
1960	50 + j0	14.953 - j10.522
1970	50 + j0	14.373 - j10.327
1980	50 + j0	13.837 - j10.120
1990	50 + j0	13.294 - j9.886
2000	50 + j0	12.768 - j9.608
2010	50 + j0	12.275 - j9.298
2020	50 + j0	11.832 - j9.000
2030	50 + j0	11.422 - j8.708
2040	50 + j0	11.015 - j8.441
2050	50 + j0	10.621 - j8.175
2060	50 + j0	10.235 - j7.916
2070	50 + j0	9.868 - j7.644

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

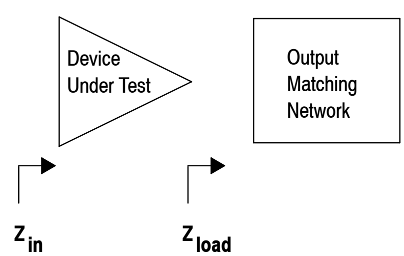
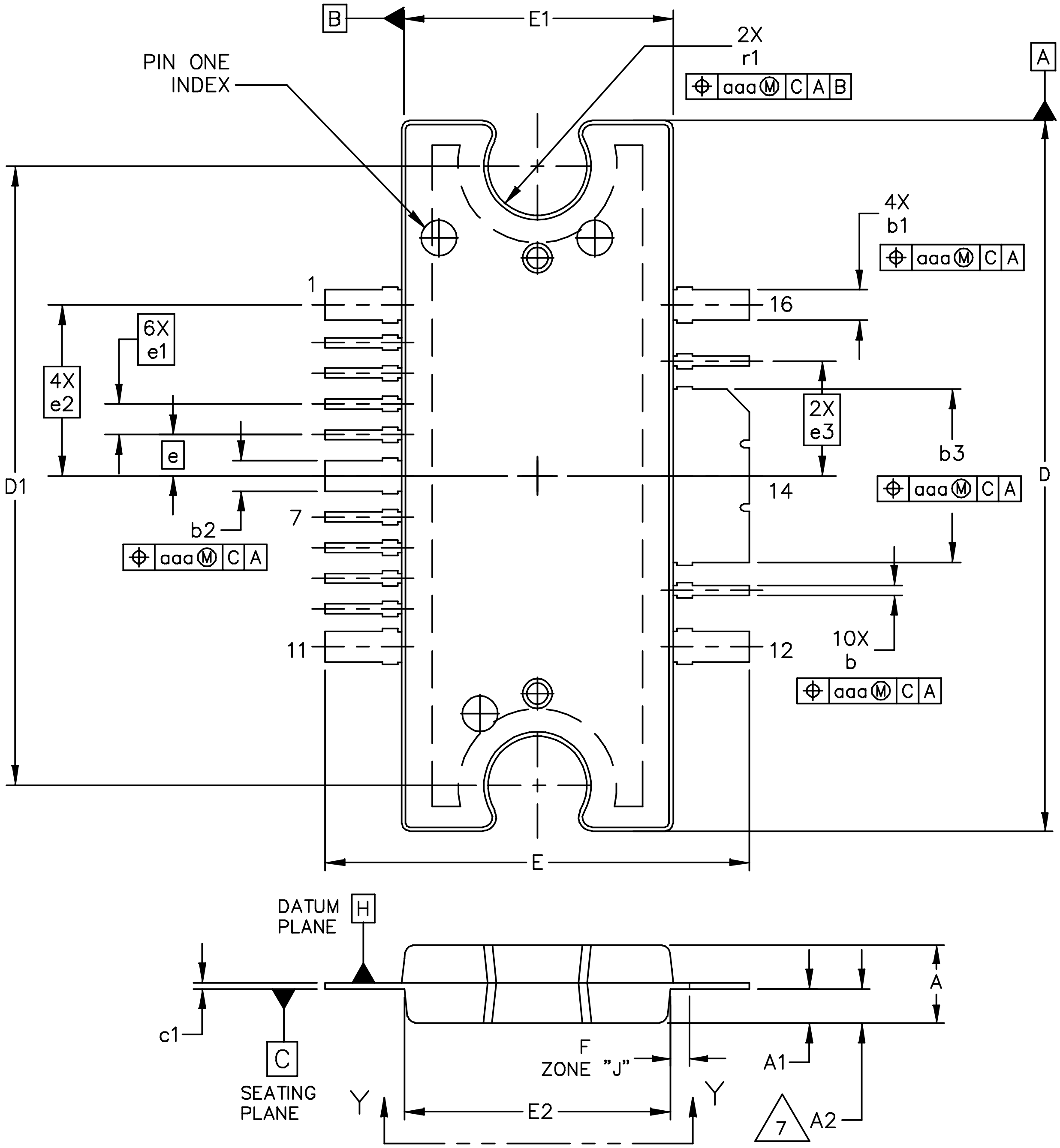


Figure 22. Series Equivalent Input and Load Impedance — TD-SCDMA

PACKAGE DIMENSIONS



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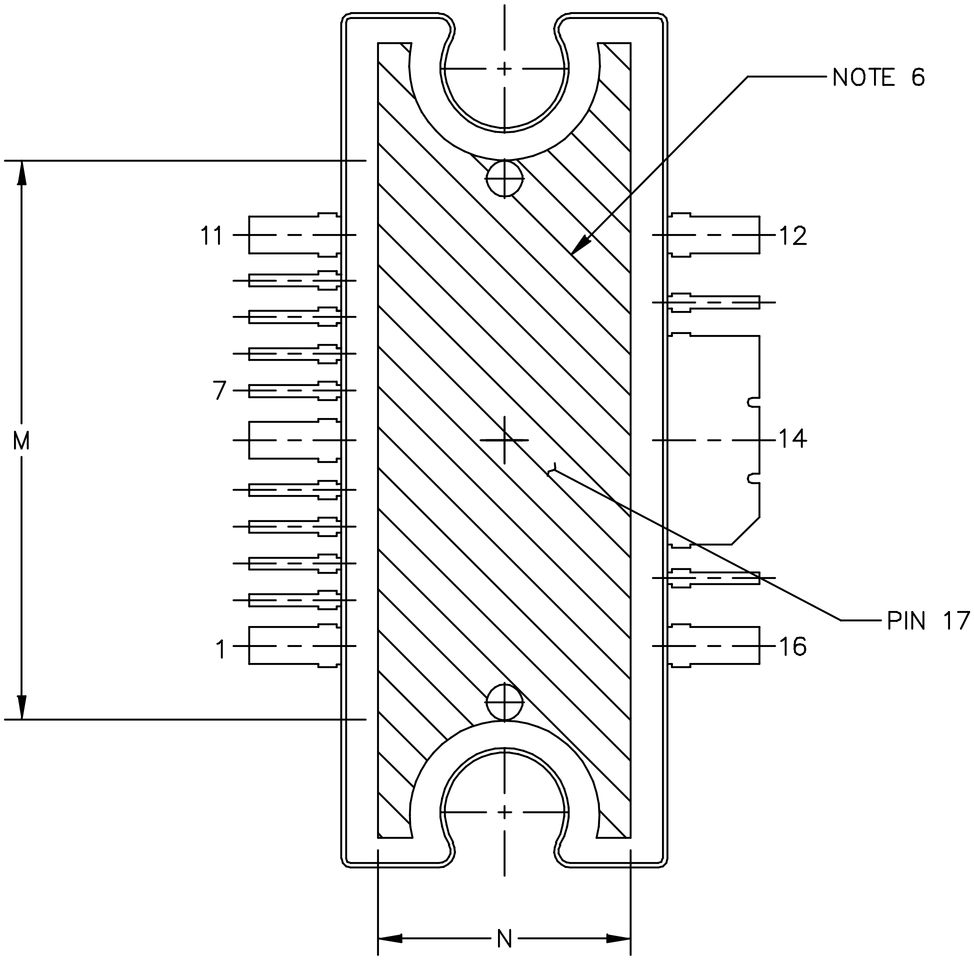
	CASE NUMBER: 1329–09	18 MAY 2010
	STANDARD: NON–JEDEC	



VIEW Y–Y

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	CASE NUMBER: 1329–09	18 MAY 2010
	STANDARD: NON–JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M—1994.

3. DATUM PLANE —H— IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE —H—.

5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. HATCHING REPRESENTS THE EXPOSED AREA OFTHE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

7. DIM A2 APPLIES WITHIN ZONE "J" ONLY.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.100	.104	2.54	2.64	b	.011	.017	0.28	0.43
A1	.038	.044	0.96	1.12	b1	.037	.043	0.94	1.09
A2	.040	.042	1.02	1.07	b2	.037	.043	0.94	1.09
D	.928	.932	23.57	23.67	b3	.225	.231	5.72	5.87
D1	.810 BSC		20.57 BSC		c1	.007	.011	.18	.28
E	.551	.559	14.00	14.20	e	.054 BSC		1.37 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e2	.224 BSC		5.69 BSC	
F	.025 BSC		0.64 BSC		e3	.150 BSC		3.81 BSC	
M	.600	----	15.24	----	r1	.063	.068	1.6	1.73
N	.270	----	6.86	----					
					aaa	.004		.10	

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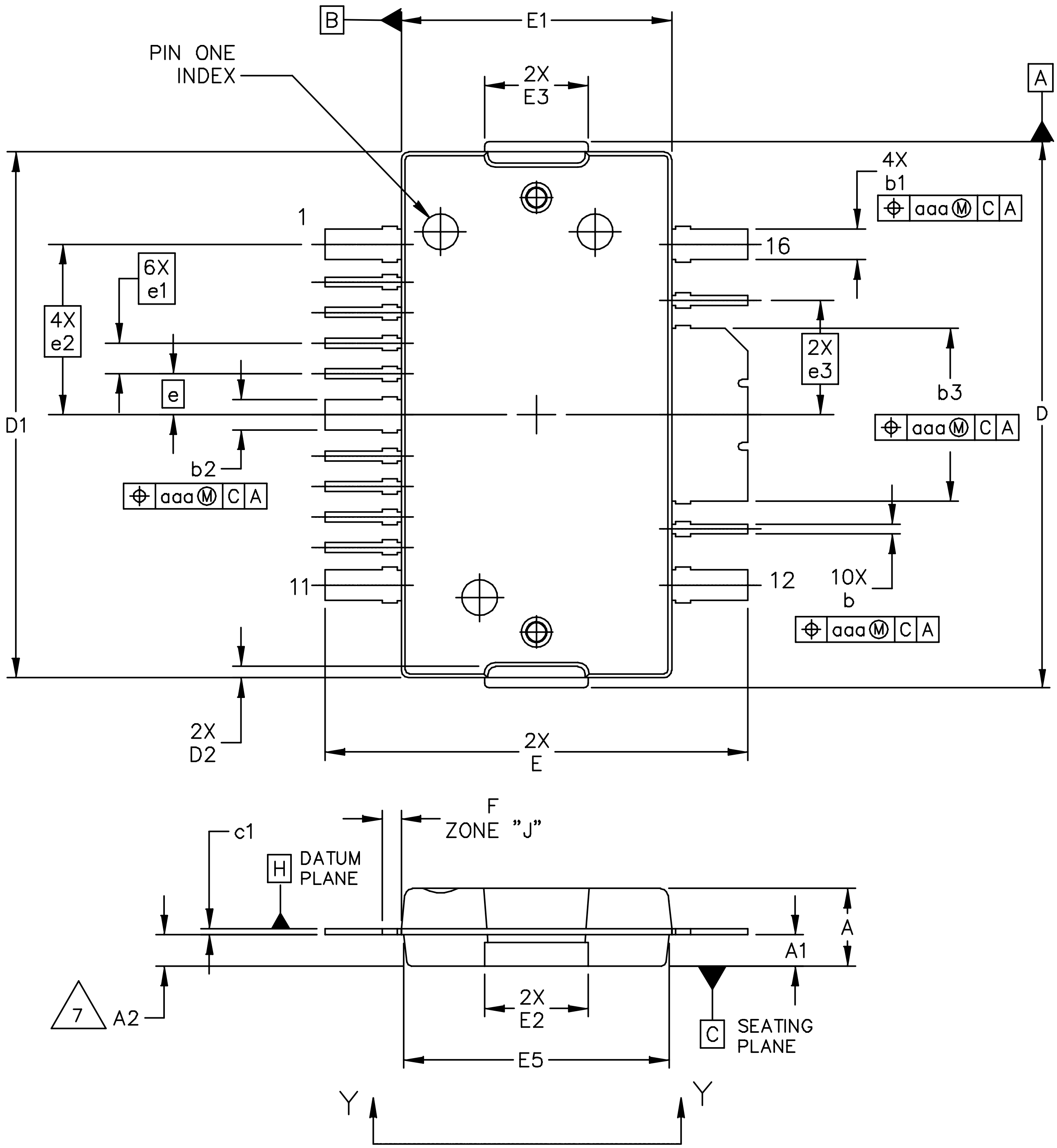
	CASE NUMBER: 1329—09	18 MAY 2010
	STANDARD: NON—JEDEC	



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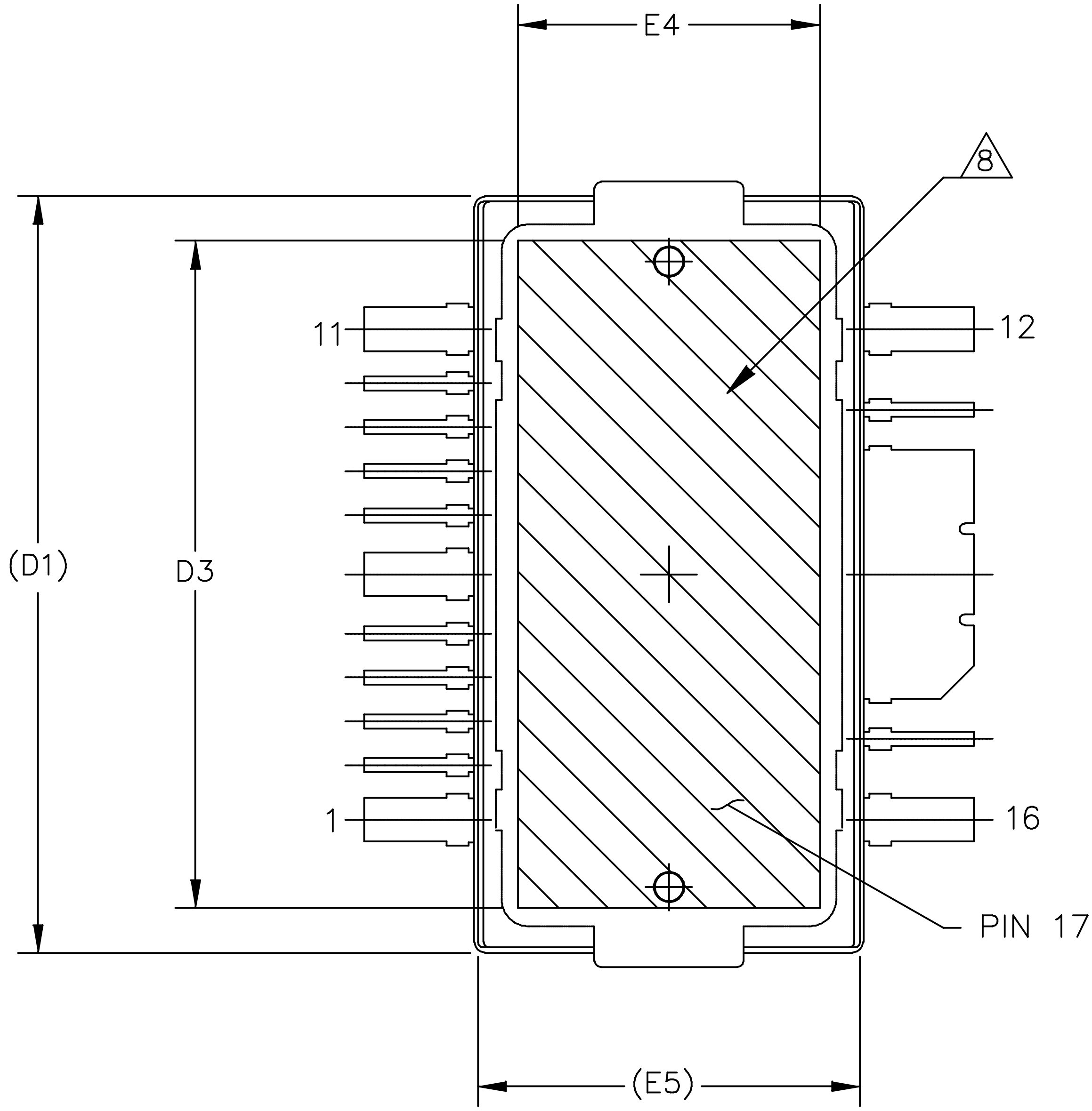
	STANDARD: NON–JEDEC		



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	CASE NUMBER: 1886–01		31 AUG 2007
	STANDARD: NON–JEDEC		

NOTES:

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6. DATUM −A− AND −B− TO BE DETERMINED AT DATUM PLANE −H−.

7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.

8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.100	.104	2.54	2.64	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b	.011	.017	0.28	0.43
A2	.040	.042	1.02	1.07	b1	.037	.043	0.94	1.09
D	.712	.720	18.08	18.29	b2	.037	.043	0.94	1.09
D1	.688	.692	17.48	17.58	b3	.225	.231	5.72	5.87
D2	.011	.019	0.28	0.48	c1	.007	.011	.18	.28
D3	.600	−−−	15.24	−−−	e	.054 BSC		1.37 BSC	
E	.551	.559	14	14.2	e1	.040 BSC		1.02 BSC	
E1	.353	.357	8.97	9.07	e2	.224 BSC		5.69 BSC	
E2	.132	.140	3.35	3.56	e3	.150 BSC		3.81 BSC	
E3	.124	.132	3.15	3.35	aaa	.004		.10	
E4	.270	−−−	6.86	−−−					
E5	.346	.350	8.79	8.89					

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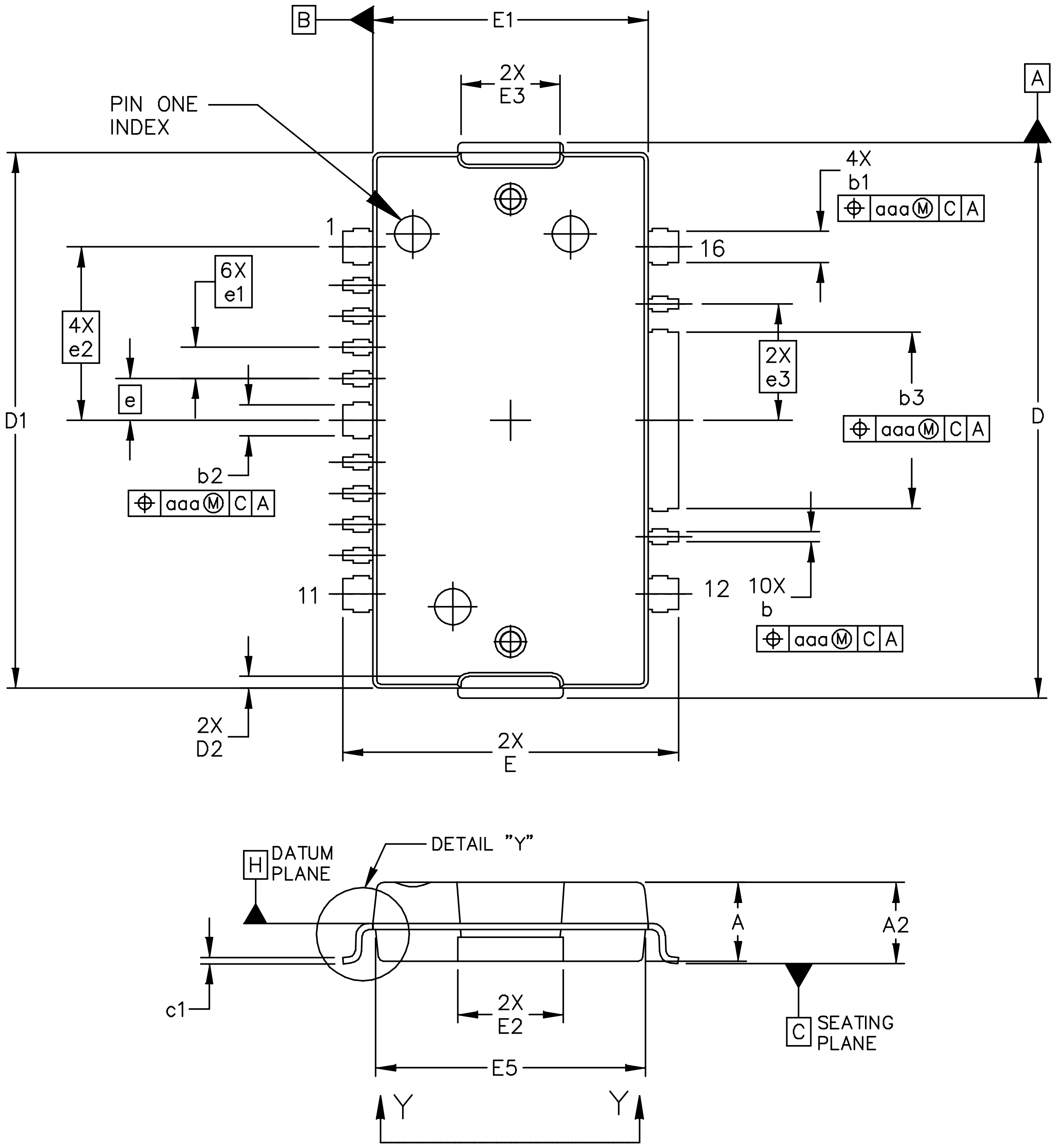

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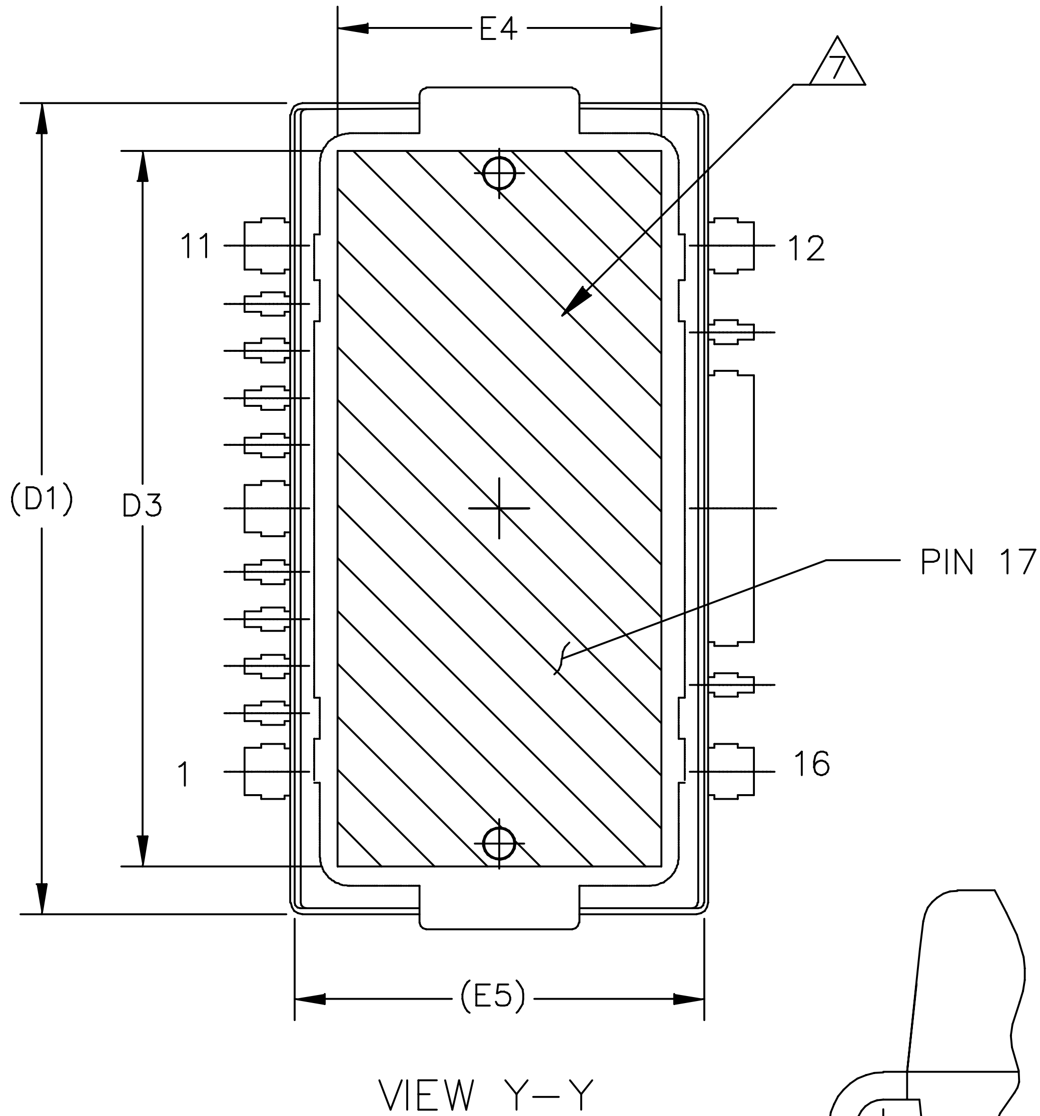
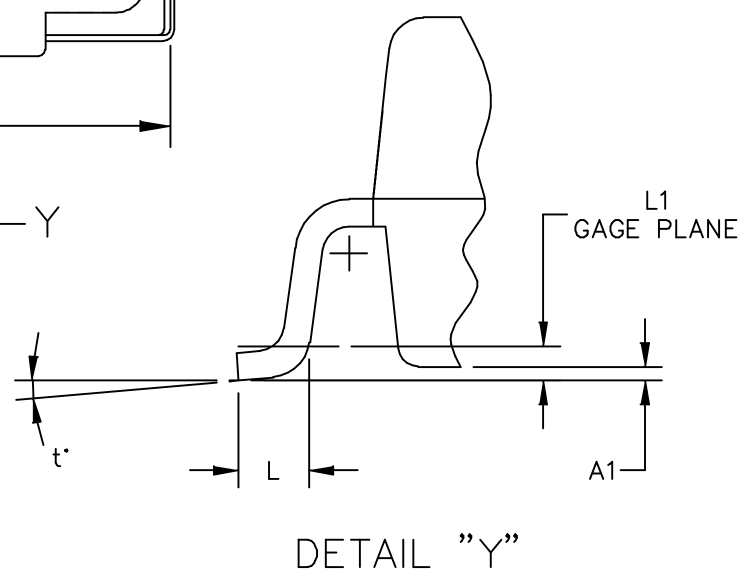
	CASE NUMBER: 1887−01	31 AUG 2007	
	STANDARD: NON−JEDEC		





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DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	L	.018	.024	0.46	0.61
A1	.001	.004	0.02	0.10	L1	.010 BSC		0.25 BSC	
A2	.099	.110	2.51	2.79	b	.011	.017	0.28	0.43
D	.712	.720	18.08	18.29	b1	.037	.043	0.94	1.09
D1	.688	.692	17.48	17.58	b2	.037	.043	0.94	1.09
D2	.011	.019	0.28	0.48	b3	.225	.231	5.72	5.87
D3	.600	---	15.24	---	c1	.007	.011	0.18	0.28
E	.429	.437	10.9	11.1	e	.054 BSC		1.37 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.132	.140	3.35	3.56	e2	.224 BSC		5.69 BSC	
E3	.124	.132	3.15	3.35	e3	.150 BSC		3.81 BSC	
E4	.270	---	6.86	---	t	2°	8°	2°	8°
E5	.346	.350	8.79	8.89	aaa	.004		0.10	

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PRODUCT DOCUMENTATION AND SOFTWARE

Refer to the following documents and software to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages
- AN3789: Clamping of High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator

For Software, do a Part Number search at http://www.freescale.com, and select the "Part Number" link. Go to the Software & Tools tab on the part's Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Sept. 2008	• Initial Release of Data Sheet
1	Jan. 2009	• Added Fig. 13, MTTF versus Junction Temperature, p. 8
2	May 2011	• Modified data sheet to reflect RF Test Reduction described in Product and Process Change Notification number, PCN13628, p. 1, 3 • Fig. 3, Test Circuit Schematic, Z-list, changed Z13, Z14 from 0.564″ x 0.083″ Microstrip to 1.042″ x 0.083″ Microstrip, p. 4 • Fig. 18, Test Circuit Schematic, Z-list, changed Z11, Z12 from 0.564″ x 0.083″ Microstrip to 1.042″ x 0.083″ Microstrip, p. 13 • Changed ESD Human Body Model rating from Class 1B to Class 0 to reflect recent ESD test results of the device, p. 2 • Fig. 13, MTTF versus Junction Temperature removed, p. 8. Refer to the device's MTTF Calculator available at freescale.com/RFpower. Go to Design Resources > Software and Tools. • Updated Fig. 14, CCDF W-CDMA IQ Magnitude Clipping, Single-Carrier Test Signal to better represent production test signal, p. 8 (renumbered as Fig. 13 after Fig. 13 removed) • Updated Fig. 15, Single-Carrier W-CDMA Spectrum to show the undistorted input test signal, p. 8 (renumbered as Fig. 14 after Fig. 13 removed) • Added AN3789, Clamping of High Power RF Transistors and RFICs in Over-Molded Plastic Packages to Product Documentation, Application Notes, p. 26 • Added Electromigration MTTF Calculator availability to Product Software, p. 26

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