



## Features

September 2011

- Internal control latches and address decoder
- Short set-up and hold times
- Wide operating voltage: 4.5 V to 13.2 V
- 12Vpp analog signal capability
- $R_{ON}$  65  $\Omega$  max. @  $V_{DD} = 12$  V, 25°C
- $\Delta R_{ON} \leq 10$   $\Omega$  @  $V_{DD} = 12$  V, 25°C
- Full CMOS switch for low distortion
- Minimum feedthrough and crosstalk
- Separate analog and digital reference supplies
- Low power consumption ISO-CMOS technology

## Applications

- Key systems
- PBX systems
- Mobile radio
- Test equipment/instrumentation
- Analog/digital multiplexers
- Audio/Video switching

### Ordering Information

MT8816AP1	44 Pin PLCC*	Tubes
MT8816APR1	44 Pin PLCC*	Tape & Reel
MT8816AE1	40 Pin PDIP*	Tubes
MT8816AF1	44 Pin TQFP*	Trays

\* Pb Free Matte Tin

-40°C to +85°C

## Description

The Zarlink MT8816 is fabricated in Zarlink's ISO-CMOS technology providing low power dissipation and high reliability. The device contains a 8 x 16 array of crosspoint switches along with a 7 to 128 line decoder and latch circuits. Any one of the 128 switches can be addressed by selecting the appropriate seven address bits. The selected switch can be turned on or off by applying a logical one or zero to the DATA input.  $V_{SS}$  is the ground reference of the digital inputs. The range of the analog signal is from  $V_{DD}$  to  $V_{EE}$ . Chip Select (CS) allows the crosspoint array to be cascaded for matrix expansion.

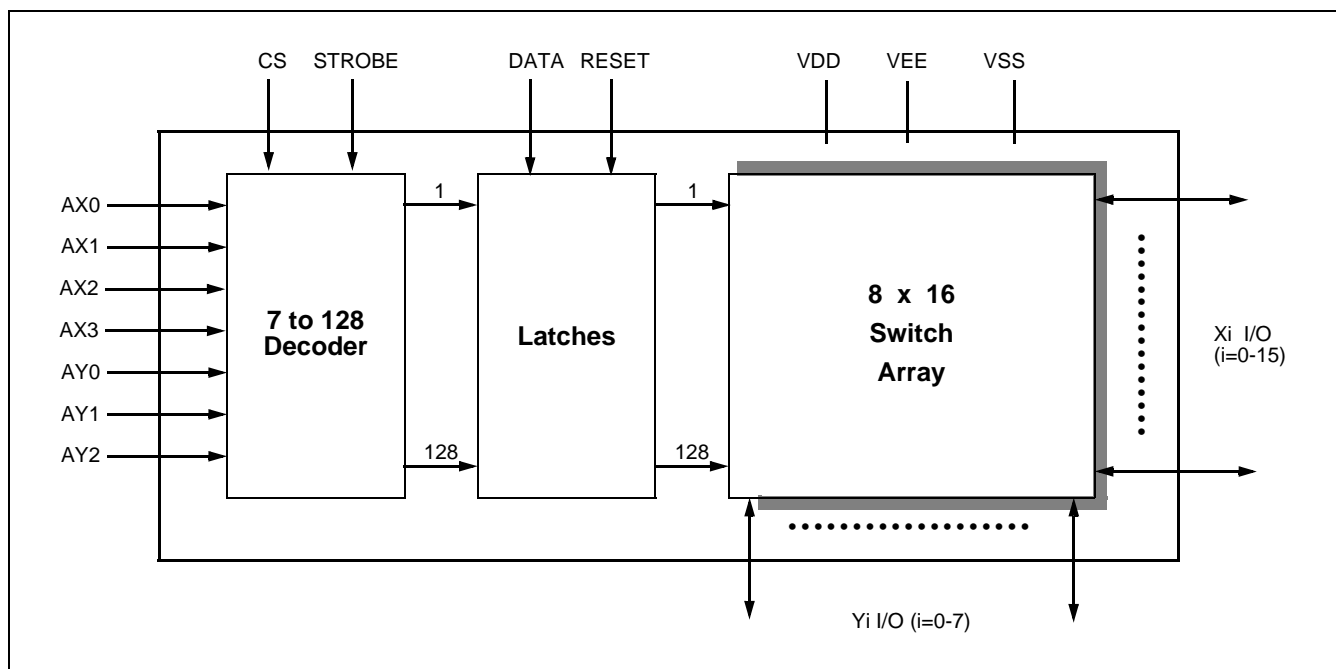
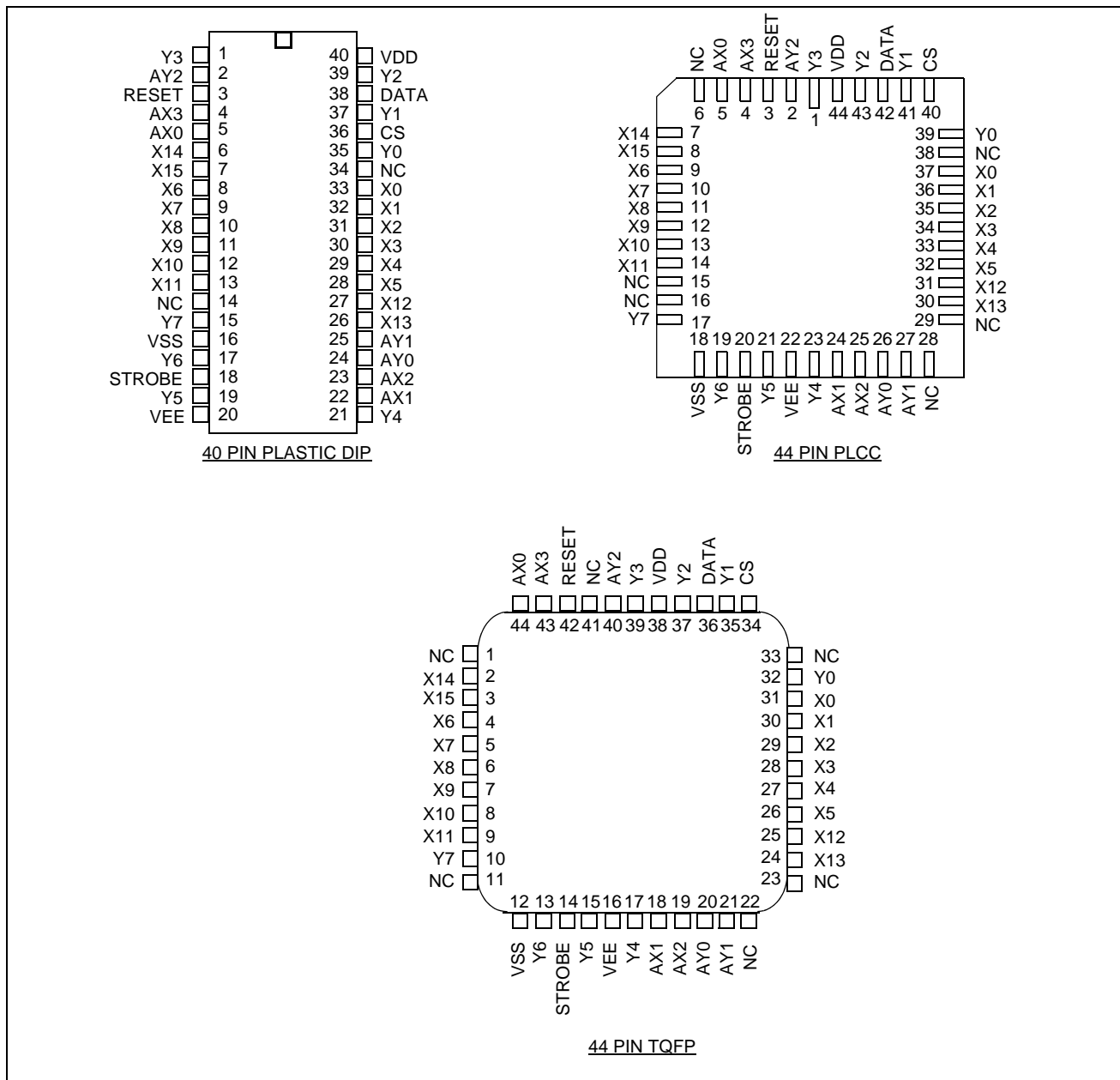


Figure 1 - Functional Block Diagram

**Change Summary**

Changes from the January 2010 issue to the September 2011 issue.

Page	Item	Change
1	Ordering Information	Removed leaded packages as per PCN notice.



**Figure 2 - Pin Connections**

## Pin Description

Pin #			Name	Description
TQFP	PDIP	PLCC		
39	1	1	Y3	<b>Y3 Analog (Input/Output):</b> this is connected to the Y3 column of the switch array.
40	2	2	AY2	<b>Y2 Address Line (Input).</b>
42	3	3	RESET	<b>Master RESET (Input):</b> this is used to turn off all switches regardless of the condition of CS. Active High.
43,44	4,5	4,5	AX3,AX0	<b>X3 and X0 Address Lines (Inputs).</b>
2, 3	6,7	7,8	X14, X15	<b>X14 and X15 Analog (Inputs/Outputs):</b> these are connected to the X14 and X15 rows of the switch array.
4-9	8-13	9-14	X6-X11	<b>X6-X11 Analog (Inputs/Outputs):</b> these are connected to the X6-X11 rows of the switch array.
41,1,11	14	6,15,16	NC	<b>No Connection</b>
10	15	17	Y7	<b>Y7 Analog (Input/Output):</b> this is connected to the Y7 column of the switch array.
12	16	18	V <sub>SS</sub>	<b>Digital Ground Reference.</b>
13	17	19	Y6	<b>Y6 Analog (Input/Output):</b> this is connected to the Y6 column of the switch array.
14	18	20	STROBE	<b>STROBE (Input):</b> enables function selected by address and data. Address must be stable before STROBE goes high and DATA must be stable on the falling edge of the STROBE. Active High.
15	19	21	Y5	<b>Y5 Analog (Input/Output):</b> this is connected to the Y5 column of the switch array.
16	20	22	V <sub>EE</sub>	<b>Negative Power Supply.</b>
17	21	23	Y4	<b>Y4 Analog (Input/Output):</b> this is connected to the Y4 column of the switch array.
18,19	22, 23	24,25	AX1,AX2	<b>X1 and X2 Address Lines (Inputs).</b>
20,21	24, 25	26,27	AY0,AY1	<b>Y0 and Y1 Address Lines (Inputs).</b>
24,25	26, 27	30,31	X13, X12	<b>X13 and X12 Analog (Inputs/Outputs):</b> these are connected to the X13 and X12 rows of the switch array.
26-31	28 - 33	32-37	X5-X0	<b>X5-X0 Analog (Inputs/Outputs):</b> these are connected to the X5-X0 rows of the switch array.
22,23,33	34	28,29, 38	NC	<b>No Connection.</b>
32	35	39	Y0	<b>Y0 Analog (Input/Output):</b> this is connected to the Y0 column of the switch array.
34	36	40	CS	<b>Chip Select (Input):</b> this is used to select the device. Active High.

## Pin Description (continued)

Pin #			Name	Description
TQFP	PDIP	PLCC		
35	37	41	Y1	<b>Y1 Analog (Input/Output):</b> this is connected to the Y1 column of the switch array.
36	38	42	DATA	<b>DATA (Input):</b> a logic high input will turn on the selected switch and a logic low will turn off the selected switch. Active High.
37	39	43	Y2	<b>Y2 Analog (Input/Output):</b> this is connected to the Y2 column of the switch array.
38	40	44	V <sub>DD</sub>	<b>Positive Power Supply.</b>

## Functional Description

The MT8816 is an analog switch matrix with an array size of 8 x 16. The switch array is arranged such that there are 8 columns by 16 rows. The columns are referred to as the Y inputs/outputs and the rows are the X inputs/outputs. The crosspoint analog switch array will interconnect any X I/O with any Y I/O when turned on and provide a high degree of isolation when turned off. The control memory consists of a 128 bit write only RAM in which the bits are selected by the address inputs (AY0-AY2, AX0-AX3). Data is presented to the memory on the DATA input. Data is asynchronously written into memory whenever both the CS (Chip Select) and STROBE inputs are high and are latched on the falling edge of STROBE. A logical "1" written into a memory cell turns the corresponding crosspoint switch on and a logical "0" turns the crosspoint off. Only the crosspoint switches corresponding to the addressed memory location are altered when data is written into memory. The remaining switches retain their previous states. Any combination of X and Y inputs/outputs can be interconnected by establishing appropriate patterns in the control memory. A logical "1" on the RESET input will asynchronously return all memory locations to logical "0" turning off all crosspoint switches regardless of whether CS is high or low. Two voltage reference pins ( $V_{SS}$  and  $V_{EE}$ ) are provided for the MT8816 to enable switching of negative analog signals. The range for digital signals is from  $V_{DD}$  to  $V_{SS}$  while the range for analog signals is from  $V_{DD}$  to  $V_{EE}$ .  $V_{SS}$  and  $V_{EE}$  pins can be tied together if a single voltage reference is needed.

## Address Decode

The seven address inputs along with the STROBE and CS (Chip Select) are logically ANDed to form an enable signal for the resettable transparent latches. The DATA input is buffered and is used as the input to all latches. To write to a location, RESET must be low and CS must go high while the address and data are set up. Then the STROBE input is set high and then low causing the data to be latched. The data can be changed while STROBE is high, however, the corresponding switch will turn on and off in accordance with the DATA input. DATA must be stable on the falling edge of STROBE in order for correct data to be written to the latch.

## Applications

Figure 3 shows a typical Operating Circuit of a video surveillance system using analog crosspoint switches which allow multiple video sources switched to multiple output devices, e.g., video monitor, video recorder etc.

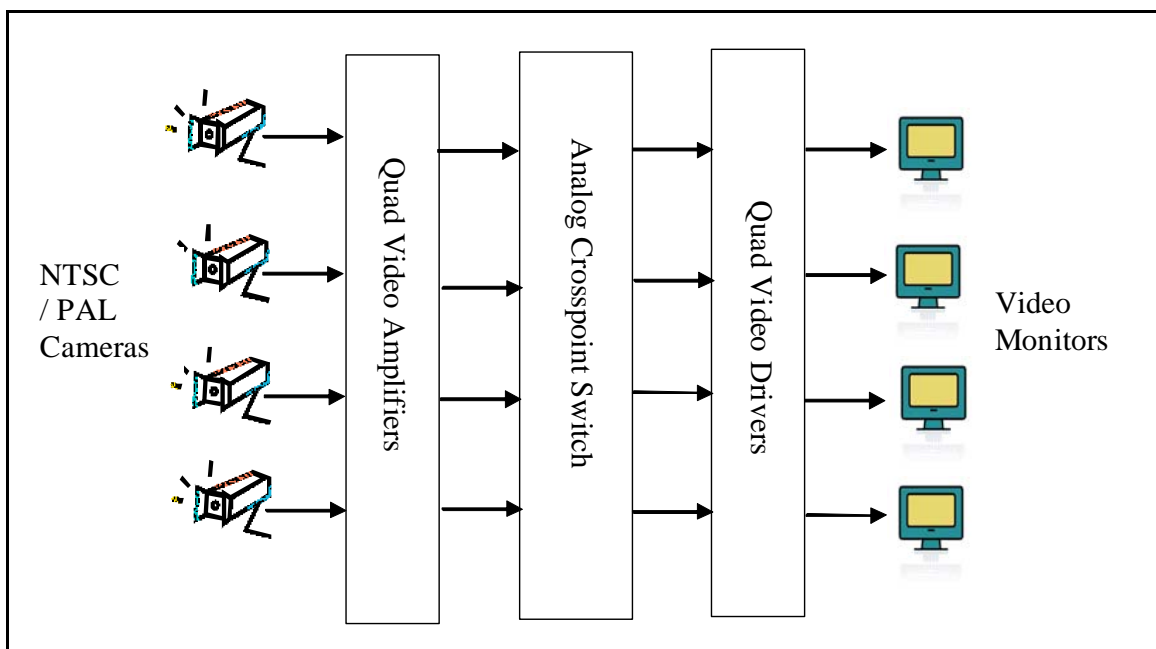


Figure 3 - Typical Video Surveillance System

Figure 4 illustrates the major components of a video surveillance system. In the center is the MT8816, a 16 x 8 analog cross-point IC. At the left are 16 video input buffers CLC2005 from Cadeka Microcircuits. At the right hand side are 8 video output buffers CLC2005 and each buffer is capable of driving a 75 ohm video load directly. BNC connectors are provided for all video inputs and video outputs.

A FT245R USB FIFO from Future Technology Devices International (FTDI) provides a standard USB interface for a PC. Through this USB connection the PC controls the switching of the video signals.

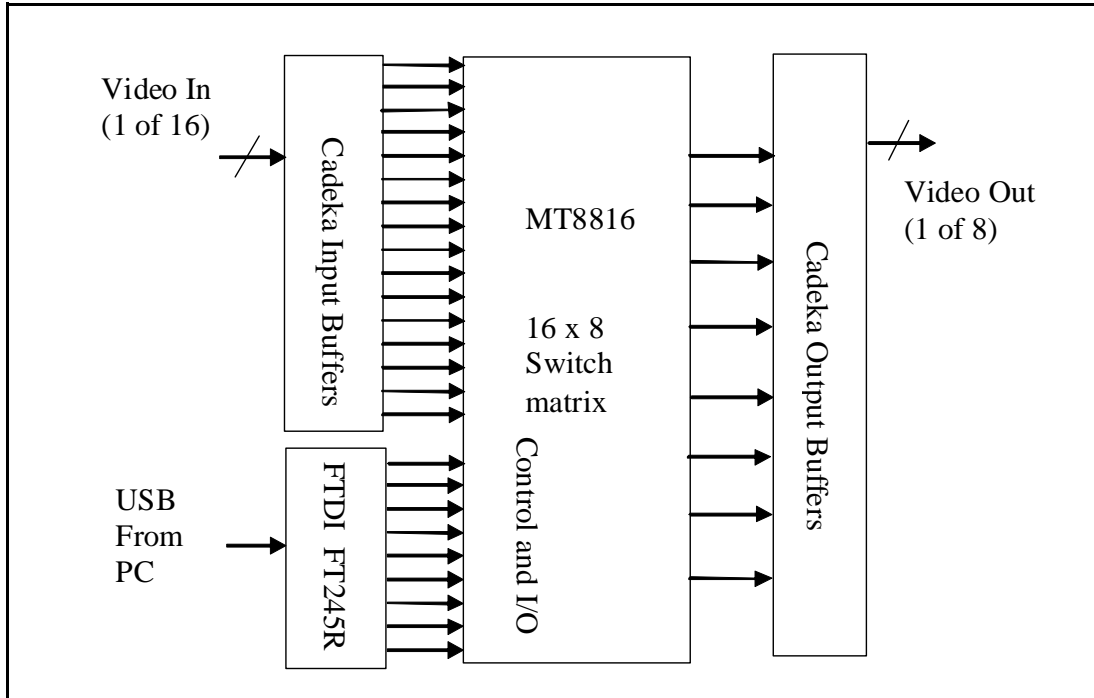


Figure 4 - Functional Block Diagram for a 16 x 8 Video Surveillance System using MT8816

**Absolute Maximum Ratings\*** - Voltages are with respect to  $V_{EE}$  unless otherwise stated.

	Parameter	Symbol	Min.	Max.	Units
1	Supply Voltage	$V_{DD}$	-0.3	16.0	V
		$V_{SS}$	-0.3	$V_{DD}+0.3$	V
2	Analog Input Voltage	$V_{INA}$	-0.3	$V_{DD}+0.3$	V
3	Digital Input Voltage	$V_{IN}$	$V_{SS}-0.3$	$V_{DD}+0.3$	V
4	Current on any I/O Pin	I		$\pm 15$	mA
5	Storage Temperature	$T_S$	-65	+150	$^{\circ}\text{C}$
6	Package Power Dissipation	$P_D$		0.6	W

\* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

**Recommended Operating Conditions** - Voltages are with respect to  $V_{EE}$  unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	Operating Temperature	$T_O$	-40	25	85	$^{\circ}\text{C}$	
2	Supply Voltage	$V_{DD}$	4.5		13.2	V	
		$V_{SS}$	$V_{EE}$		$V_{DD}-4.5$	V	
3	Analog Input Voltage	$V_{INA}$	$V_{EE}$		$V_{DD}$	V	
4	Digital Input Voltage	$V_{IN}$	$V_{SS}$		$V_{DD}$	V	

**DC Electrical Characteristics<sup>†</sup>** - Voltages are with respect to  $V_{EE} = V_{SS} = 0\text{ V}$ ,  $V_{DD} = 12\text{ V}$  unless otherwise stated.

	Characteristics	Sym.	Min.	Typ. <sup>‡</sup>	Max.	Units	Test Conditions
1	Quiescent Supply Current	$I_{DD}$		1	100	$\mu\text{A}$	All digital inputs at $V_{IN}=V_{SS}$ or $V_{DD}$
				0.4	1.5	mA	All digital inputs at $V_{IN}=2.4\text{ V} + V_{SS}$ ; $V_{SS}=7.0\text{ V}$
				5	15	mA	All digital inputs at $V_{IN}=3.4\text{ V}$
2	Off-state Leakage Current (See G.9 in Appendix)	$I_{OFF}$		$\pm 1$	$\pm 500$	nA	$ V_{X_i} - V_{Y_j}  = V_{DD} - V_{EE}$ See Appendix, Fig. A.1
3	Input Logic "0" level	$V_{IL}$			$0.8+V_s$	V	$V_{SS}=7.5\text{ V}$ ; $V_{EE}=0\text{ V}$
4	Input Logic "1" level	$V_{IH}$	$2.0+V_{SS}$			V	$V_{SS}=6.5\text{ V}$ ; $V_{EE}=0\text{ V}$
5	Input Logic "1" level	$V_{IH}$	3.3			V	
6	Input Leakage (digital pins)	$I_{LEAK}$		0.1	10	$\mu\text{A}$	All digital inputs at $V_{IN} = V_{SS}$ or $V_{DD}$

<sup>†</sup> DC Electrical Characteristics are over recommended temperature range.

<sup>‡</sup> Typical figures are at  $25^{\circ}\text{C}$  and are for design aid only; not guaranteed and not subject to production testing.

**DC Electrical Characteristics- Switch Resistance** -  $V_{DC}$  is the external DC offset applied at the analog I/O pins.

	Characteristics	Sym.	25°C		70°C		85°C		Units	Test Conditions
			Typ.	Max.	Typ.	Max.	Typ.	Max.		
1	On-state Resistance $V_{DD}=12V$ $V_{DD}=10V$ $V_{DD}=5V$ (See G.1, G.2, G.3 in Appendix)	$R_{ON}$	45 55 120	65 75 185		75 85 215		80 90 225	$\Omega$ $\Omega$ $\Omega$	$V_{SS}=V_{EE}=0V, V_{DC}=V_{DD}/2,$ $ V_{Xi}-V_{Yj}  = 0.4V$ See Appendix, Fig. A.2
2	Difference in on-state resistance between two switches (See G.4 in Appendix)	$\Delta R_{ON}$	5	10		10		10	$\Omega$	$V_{DD}=12V, V_{SS}=V_{EE}=0,$ $V_{DC}=V_{DD}/2,$ $ V_{Xi}-V_{Yj}  = 0.4V$ See Appendix, Fig. A.2

**AC Electrical Characteristics<sup>†</sup> - Crosspoint Performance**- Voltages are with respect to  $V_{DD}=5V, V_{SS}=0V, V_{EE}=-7V$ , unless otherwise stated.

	Characteristics	Sym.	Min.	Typ. <sup>‡</sup>	Max.	Units	Test Conditions
1	Switch I/O Capacitance	$C_S$		20		pF	f=1 MHz
2	Feedthrough Capacitance	$C_F$		0.2		pF	f=1 MHz
3	Frequency Response Channel "ON" $20\text{LOG}(V_{OUT}/V_{Xi})=-3\text{ dB}$	$F_{3dB}$		45		MHz	Switch is "ON"; $V_{INA} = 2V_{pp}$ sinewave; $R_L = 1\text{ k}\Omega$ See Appendix, Fig. A.3
4	Total Harmonic Distortion (See G.5, G.6 in Appendix)	THD		0.01		%	Switch is "ON"; $V_{INA} = 2V_{pp}$ sinewave f= 1 kHz; $R_L=1\text{ k}\Omega$
5	Feedthrough Channel "OFF" Feed.= $20\text{LOG}(V_{OUT}/V_{Xi})$ (See G.8 in Appendix)	FDT		-95		dB	All Switches "OFF"; $V_{INA}=2V_{pp}$ sinewave f= 1 kHz; $R_L=1\text{ k}\Omega$ . See Appendix, Fig. A.4
6	Crosstalk between any two channels for switches $X_i-Y_i$ and $X_j-Y_j$ . $X_{talk}=20\text{LOG}(V_{Yj}/V_{Xi})$ . (See G.7 in Appendix).	$X_{talk}$		-45		dB	$V_{INA}=2V_{pp}$ sinewave f= 10 MHz; $R_L = 75\ \Omega$
				-90		dB	$V_{INA}=2V_{pp}$ sinewave f= 10 kHz; $R_L = 600\ \Omega$ .
				-85		dB	$V_{INA}=2V_{pp}$ sinewave f= 10 kHz; $R_L = 1\text{ k}\Omega$ .
				-80		dB	$V_{INA}=2V_{pp}$ sinewave f= 1 kHz; $R_L = 10\text{ k}\Omega$ . Refer to Appendix, Fig. A.5 for test circuit.
7	Propagation delay through switch	$t_{PS}$			30	ns	$R_L=1\text{ k}\Omega; C_L=50\text{ pF}$

<sup>†</sup> Timing is over recommended temperature range. See Fig. 3 for control and I/O timing details.

<sup>‡</sup> Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Crosstalk measurements are for Plastic DIPS only, crosstalk values for PLCC packages are approximately 5 dB better.

**AC Electrical Characteristics<sup>†</sup> - Control and I/O Timings**- Voltages are with respect to  $V_{DD} = 5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $V_{EE} = -7\text{ V}$ , unless otherwise stated.

	Characteristics	Sym.	Min.	Typ. <sup>‡</sup>	Max.	Units	Test Conditions
1	Control Input crosstalk to switch (for CS, DATA, STROBE, Address)	$CX_{\text{talk}}$		30		mVpp	$V_{IN}=3\text{ V}$ squarewave; $R_{IN}=1\text{ k}\Omega$ , $R_L=10\text{ k}\Omega$ . See Appendix, Fig. A.6
2	Digital Input Capacitance	$C_{DI}$		10		pF	$f=1\text{ MHz}$
3	Switching Frequency	$F_O$			20	MHz	
4	Setup Time DATA to STROBE	$t_{DS}$	10			ns	$R_L=1\text{ k}\Omega$ , $C_L=50\text{ pF}$ <sup>¿</sup>
5	Hold Time DATA to STROBE	$t_{DH}$	10			ns	$R_L=1\text{ k}\Omega$ , $C_L=50\text{ pF}$ <sup>¿</sup>
6	Setup Time Address to STROBE	$t_{AS}$	10			ns	$R_L=1\text{ k}\Omega$ , $C_L=50\text{ pF}$ <sup>¿</sup>
7	Hold Time Address to STROBE	$t_{AH}$	10			ns	$R_L=1\text{ k}\Omega$ , $C_L=50\text{ pF}$ <sup>¿</sup>
8	Setup Time CS to STROBE	$t_{CSS}$	10			ns	$R_L=1\text{ k}\Omega$ , $C_L=50\text{ pF}$ <sup>¿</sup>
9	Hold Time CS to STROBE	$t_{CSH}$	10			ns	$R_L=1\text{ k}\Omega$ , $C_L=50\text{ pF}$ <sup>¿</sup>
10	STROBE Pulse Width	$t_{SPW}$	20			ns	$R_L=1\text{ k}\Omega$ , $C_L=50\text{ pF}$ <sup>¿</sup>
11	RESET Pulse Width	$t_{RPW}$	40			ns	$R_L=1\text{ k}\Omega$ , $C_L=50\text{ pF}$ <sup>¿</sup>
12	STROBE to Switch Status Delay	$t_S$		40	100	ns	$R_L=1\text{ k}\Omega$ , $C_L=50\text{ pF}$ <sup>¿</sup>
13	DATA to Switch Status Delay	$t_D$		50	100	ns	$R_L=1\text{ k}\Omega$ , $C_L=50\text{ pF}$ <sup>¿</sup>
14	RESET to Switch Status Delay	$t_R$		35	100	ns	$R_L=1\text{ k}\Omega$ , $C_L=50\text{ pF}$ <sup>¿</sup>

<sup>†</sup> Timing is over recommended temperature range. See Fig. 3 for control and I/O timing details.

Digital Input rise time ( $t_r$ ) and fall time ( $t_f$ ) = 5 ns.

<sup>‡</sup> Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

<sup>¿</sup> Refer to Appendix, Fig. A.7 for test circuit.

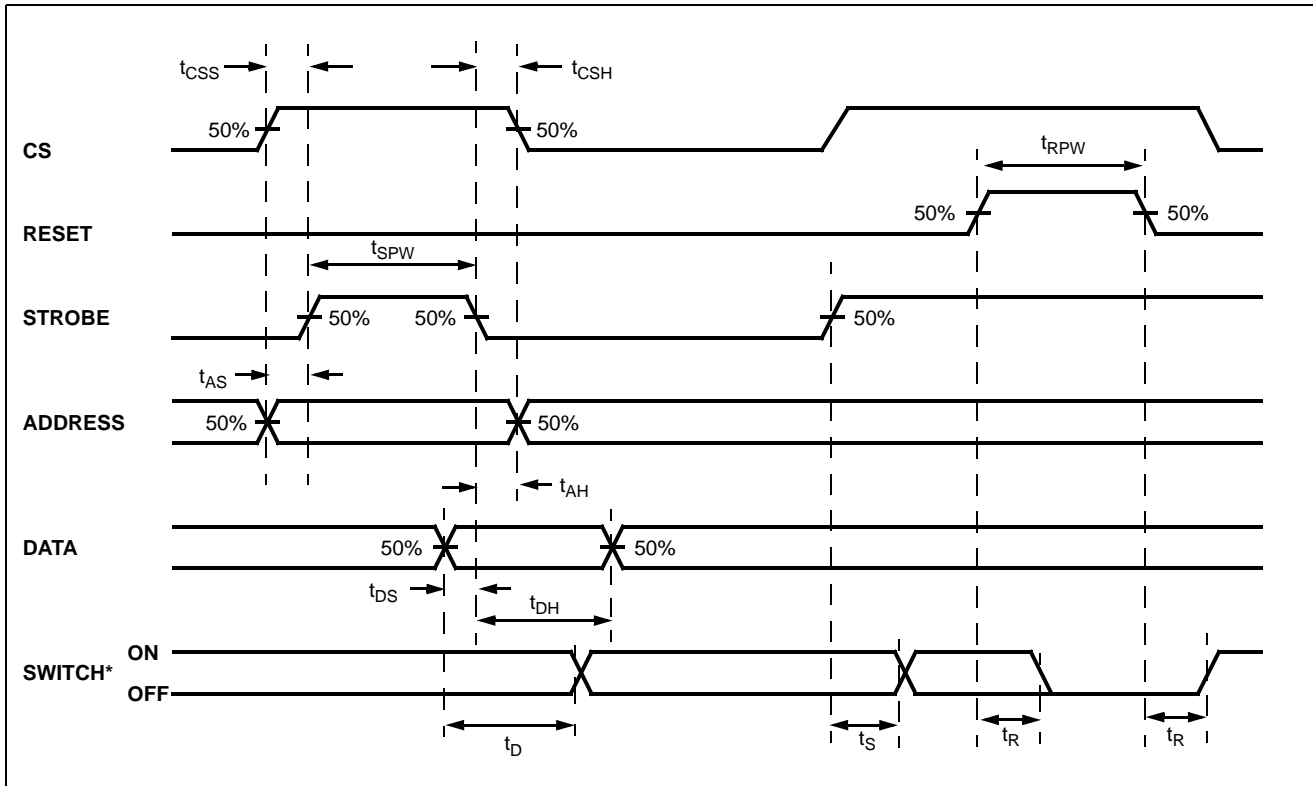


Figure 5 - Control Memory Timing Diagram

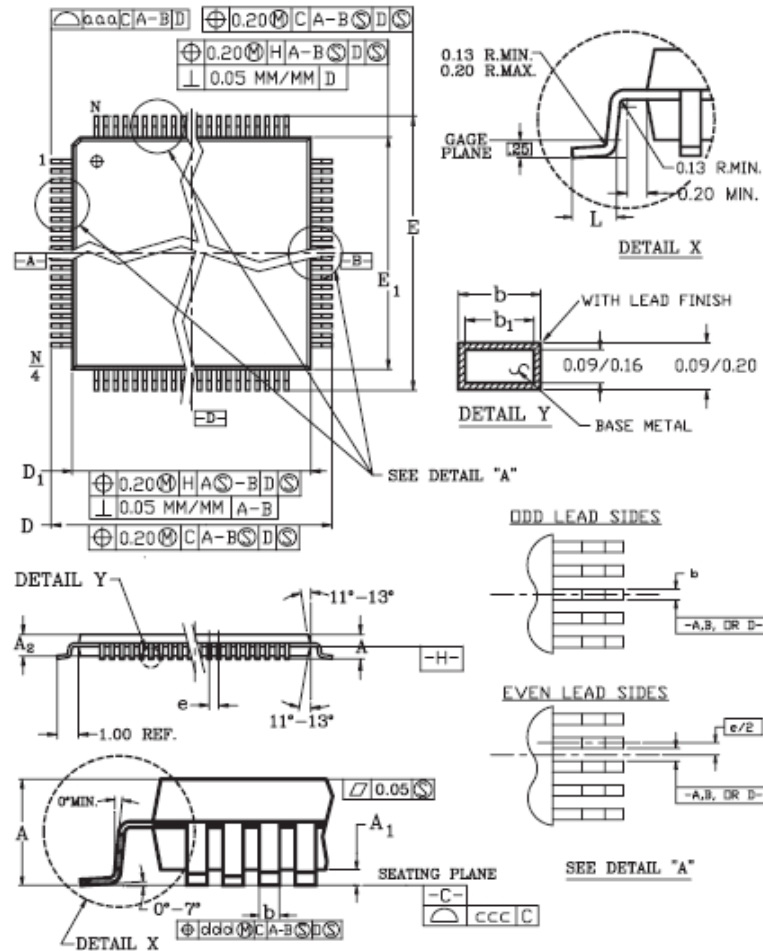
\* See Appendix, Fig. A.7 for switching waveform

AX0	AX1	AX2	AX3	AY0	AY1	AY2	Connection*
0	0	0	0	0	0	0	X0-Y0
1	0	0	0	0	0	0	X1-Y0
0	1	0	0	0	0	0	X2-Y0
1	1	0	0	0	0	0	X3-Y0
0	0	1	0	0	0	0	X4-Y0
1	0	1	0	0	0	0	X5-Y0
0	1	1	0	0	0	0	X12-Y0
1	1	1	0	0	0	0	X13-Y0
0	0	0	1	0	0	0	X6-Y0
1	0	0	1	0	0	0	X7-Y0
0	1	0	1	0	0	0	X8-Y0
1	1	0	1	0	0	0	X9-Y0
0	0	1	1	0	0	0	X10-Y0
1	0	1	1	0	0	0	X11-Y0
0	1	1	1	0	0	0	X14-Y0
1	1	1	1	0	0	0	X15-Y0
0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	1 ↓ 1	0 ↓ 0	0 ↓ 0	X0-Y1 ↓ X15-Y1
0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 0	1 ↓ 1	0 ↓ 0	X0-Y2 ↓ X15-Y2
0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	1 ↓ 1	1 ↓ 1	0 ↓ 0	X0-Y3 ↓ X15-Y3
0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 0	0 ↓ 0	1 ↓ 1	X0-Y4 ↓ X15-Y4
0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	1 ↓ 1	0 ↓ 0	1 ↓ 1	X0-Y5 ↓ X15-Y5
0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 0	1 ↓ 1	1 ↓ 1	X0-Y6 ↓ X15-Y6
0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	1 ↓ 1	1 ↓ 1	1 ↓ 1	X0-Y7 ↓ X15-Y7

**Table 1 - Address Decode Truth Table**

\* Switch connections are not in ascending order

44 Pin TQFP



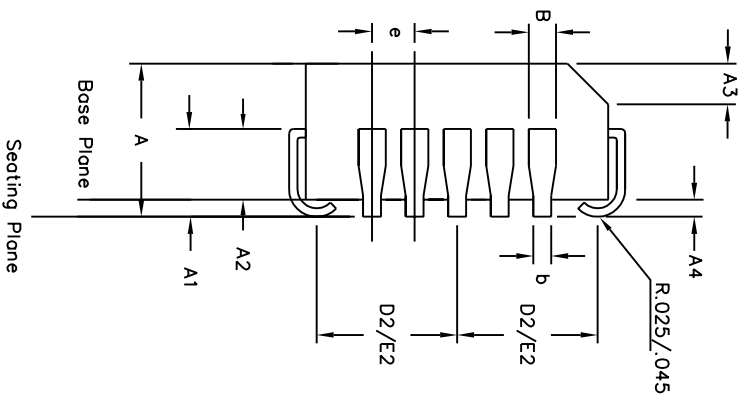
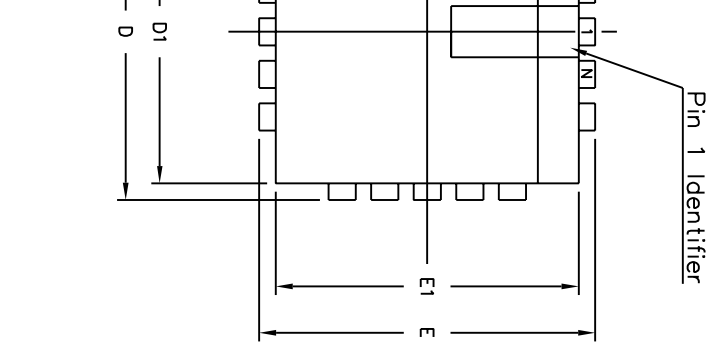
Symbol	Min	Nom	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
D		12 BSC	
D1		10 BSC	
E		12 BSC	
E1		10 BSC	
L	0.45	0.60	0.75
N		44	
e		0.80 BSC	
b	0.30	0.37	0.45
b1	0.30	0.35	0.40
occ		0.10	
ddd		0.20	
aaa		0.20	

JEDEC #: MS-026 (C) ACB

- Notes:
- All dimensions and tolerances conform to ANSI Y14.5-1982.
  - Datum plane  $\square$  is located at the mold parting line and is coincident with the bottom of the lead where the lead exits the plastic body.
  - Dimensions "D1" and "E1" do not include mold protrusion. Allowable protrusion is 0.254mm per side. Dimensions "D1" and "E1" include mold mismatch and are determined at Datum plane  $\square$ .
  - Dimension "B" does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the "b" dimension at maximum material condition. Dambar can not be located on the lower radius or the foot.
  - Controlling dimensions: Millimeter.
  - Dimensions "D" and "E" are measured from both innermost and outermost points.
  - Deviation from lead-tip true position shall be within  $\pm 0.076$ mm for pitch  $> 0.5$ mm and within  $\pm 0.04$  for pitch  $\leq 0.5$ mm.
  - Lead coplanarity shall be within: (Refer to 06-500)
    - 0.10mm for devices with lead pitch of 0.65-0.80mm.
    - 0.076mm for devices with lead pitch of 0.50mm.
 Coplanarity is measured per specification 06-500.
  - Half span (center of package to lead tip) shall be  $15.30 \pm 0.165$ mm ( $602 \pm 0.065^\circ$ ).
  - "N" is the total number of terminals.
  - The top of package is smaller than the bottom of the package by 0.15mm.
  - This outline conforms to JEDEC publication 95 registration MS-026
  - The 160 lead is a compliant depopulation of the 176 lead MS-026 variation BGA.

Note:

Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.



Symbol	Control Dimensions in. inches		Altern. Dimensions in. millimetres	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.062	0.083	1.57	2.11
A3	0.042	0.056	1.07	1.42
A4	0.020	—	0.51	—
D	0.685	0.695	17.40	17.65
D1	0.650	0.656	16.51	16.66
D2	0.291	0.319	7.39	8.10
E	0.685	0.695	17.40	17.65
E1	0.650	0.656	16.51	16.66
E2	0.291	0.319	7.39	8.10
B	0.026	0.032	0.66	0.81
b	0.013	0.021	0.33	0.53
e	0.050	BSC	1.27	BSC
Pin features				
ND	11			
NE	11			
N	44			
Note	Square			
Conforms to JEDEC MS-018AC Iss. A				

ances conform to ANSI Y14.5M-1982  
do not include mould protrusions.  
on is 0.010" per side. Dimensions D1 and E1  
mismatch and are determined at the  
and E1 are measured at the extreme material  
r lower parting line.  
inches.  
rminids.  
120° minimum bend.



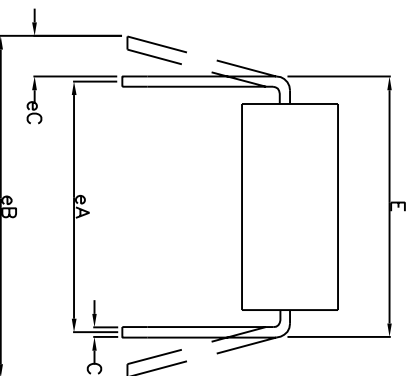
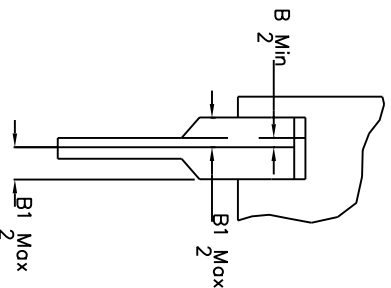
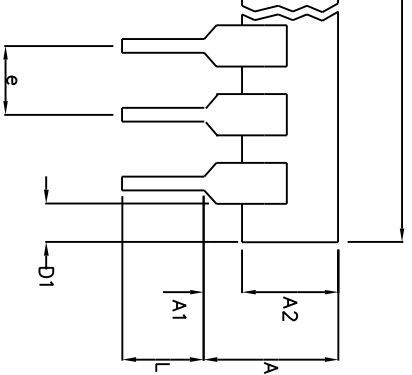
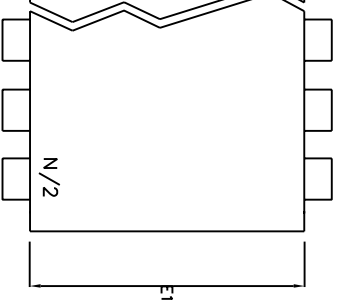
Previous package codes

HP / P

Package Code QA

Package Outline for  
44 lead PLCC

GPD000003



	Min mm	Max mm	Min Inches	Max Inches
A		6.35		0.250
A1	0.38		0.015	
A2	3.18	4.95	0.125	0.195
B	0.36	0.56	0.014	0.022
B1	0.76	1.78	0.030	0.070
C	0.20	0.38	0.008	0.015
D	50.29	53.21	1.980	2.095
D1	0.13		0.005	
E	15.24	15.88	0.600	0.625
E1	12.32	14.73	0.485	0.580
e	2.54	BSC	0.100	BSC
eA	15.24	BSC	0.600	BSC
eB		17.78		0.700
L	2.92	5.08	0.115	0.200
N		40		40

Conforms to Jeduc MS-011AC ISS.B

Dimensions are measured with the package seated in the Seating Plane. Dimensions shall include mold flash or protrusions. Mold flash or protrusion shall not exceed 0.010 inch. Dimensions are measured with leads constrained to be perpendicular to plane T. Dimensions are measured at the lead tips with the leads unconstrained; eC must be zero or greater.



**ZARLINK**  
SEMICONDUCTOR

Previous package codes

DP / E

Package Code

DA

Package Outline for  
40 lead PDIP

GPD000073



**For more information about all Zarlink products  
visit our Web Site at  
[www.zarlink.com](http://www.zarlink.com)**

Information relating to products and services furnished herein by Zarlink Semiconductor Inc. or its subsidiaries (collectively "Zarlink") is believed to be reliable. However, Zarlink assumes no liability for errors that may appear in this publication, or for liability otherwise arising from the application or use of any such information, product or service or for any infringement of patents or other intellectual property rights owned by third parties which may result from such application or use. Neither the supply of such information or purchase of product or service conveys any license, either express or implied, under patents or other intellectual property rights owned by Zarlink or licensed from third parties by Zarlink, whatsoever. Purchasers of products are also hereby notified that the use of product in certain ways or in combination with Zarlink, or non-Zarlink furnished goods or services may infringe patents or other intellectual property rights owned by Zarlink.

This publication is issued to provide information only and (unless agreed by Zarlink in writing) may not be used, applied or reproduced for any purpose nor form part of any order or contract nor to be regarded as a representation relating to the products or services concerned. The products, their specifications, services and other information appearing in this publication are subject to change by Zarlink without notice. No warranty or guarantee express or implied is made regarding the capability, performance or suitability of any product or service. Information concerning possible methods of use is provided as a guide only and does not constitute any guarantee that such methods of use will be satisfactory in a specific piece of equipment. It is the user's responsibility to fully determine the performance and suitability of any equipment using such information and to ensure that any publication or data used is up to date and has not been superseded. Manufacturing does not necessarily include testing of all functions or parameters. These products are not suitable for use in any medical products whose failure to perform may result in significant injury or death to the user. All products and materials are sold and services provided subject to Zarlink's conditions of sale which are available on request.

Purchase of Zarlink's I2C components conveys a license under the Philips I2C Patent rights to use these components in an I2C System, provided that the system conforms to the I2C Standard Specification as defined by Philips.



Zarlink, ZL, the Zarlink Semiconductor logo and the Legerity logo and combinations thereof, VoiceEdge, VoicePort, SLAC, ISLIC, ISLAC and VoicePath are trademarks of Zarlink Semiconductor Inc.

**TECHNICAL DOCUMENTATION - NOT FOR RESALE**

---

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

-  [View MT8816AP1 on WIN SOURCE](#)
-  [Microsemi Corporation](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management