THE DATASHEET OF

MT48H8M16LFB4-8:J TR

Mobile SDRAM

MT48H8M16LF - 2 Meg x 16 x 4 banks

Features

- VDD/VDDQ = 1.70–1.95V
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, or 8
- Auto precharge and concurrent auto precharge modes
- Auto refresh and self refresh mode
- 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Partial-array self refresh (PASR) power-saving mode
- Deep power-down mode
- Programmable output drive strength
- On-chip temperature sensor to control the self-refresh rate
- Operating temperature ranges
  - Commercial (0°C to +70°C)
  - Industrial (–40°C to +85°C)

Options — Marking

- VDD/VDDQ
  - 1.8V/1.8V — H
- Configurations
  - 8 Meg x 16 (2 Meg x 16 x 4 banks) — 8M16
- Package/Ball out
  - 54-ball VFBGA, 8mm x 8mm — B4
- Timing (cycle time)
  - 7.5ns @ CL = 3 (133 MHz) — -75
  - 8ns @ CL = 3 (125 MHz) — -8
- Operating temperature
  - Commercial (0°C to +70°C) — none
  - Industrial (–40°C to +85°C) — IT
- Die revision designator — :J

Figure 1: 54-Ball VFBGA Assignment (Top View)

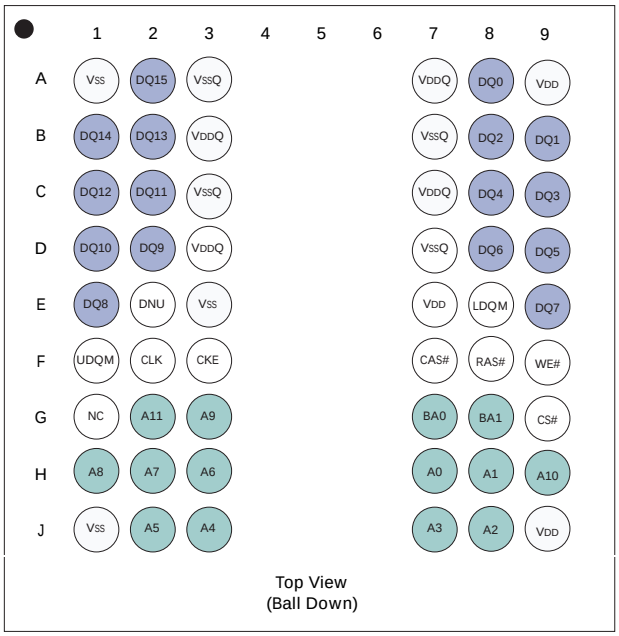

Table 1: Address Table

	8 Meg x 16
Configuration	2 Meg x 16 x 4 banks
Refresh count	4K
Row addressing	4K (A0–A11)
Bank addressing	4 (BA0, BA1)
Column addressing	512 (A0–A8)

Table 2: Key Timing Parameters
CL = CAS (READ) latency

Speed Grade	Clock Frequency		Access Time		Setup Time	Hold Time
	CL = 2	CL = 3	CL = 2	CL = 3		
-75	104 MHz	133 MHz	8ns	6ns	2.5ns	1ns
-8	83 MHz	125 MHz	8ns	7ns	2.5ns	1ns

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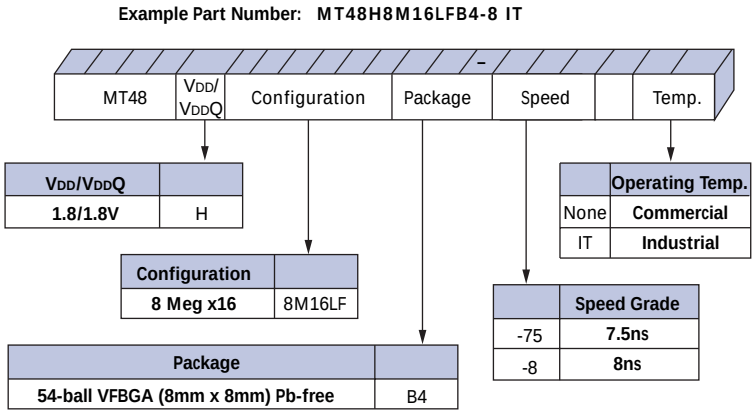
Figure 2: Part Numbering Diagram



General Description

The Micron® 128Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 134,217,728 bits. It is internally configured as a quad-bank DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the x16's 33,554,432-bit banks is organized as 4,096 rows by 512 columns by 16 bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0–A11select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The SDRAM provides for programmable read or write burst lengths (BL) of 1, 2, 4, or 8 locations with a burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The 128Mb SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless high-speed, random-access operation.

The 128Mb SDRAM is designed to operate in 1.8V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, deep power-down mode. All inputs and outputs are LVTTL-compatible.

Self refresh mode offers temperature compensation through an on-die temperature sensor and partial-array self refresh (PASR). PASR allows users to achieve additional power savings over normal usage. The temperature sensor is enabled by default and the PASR settings can be programmed through the extended mode register.

SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time and the capability to randomly change column addresses on each clock cycle during a burst access.

Figure 3: 8 Meg x 16 SDRAM Functional Block Diagram

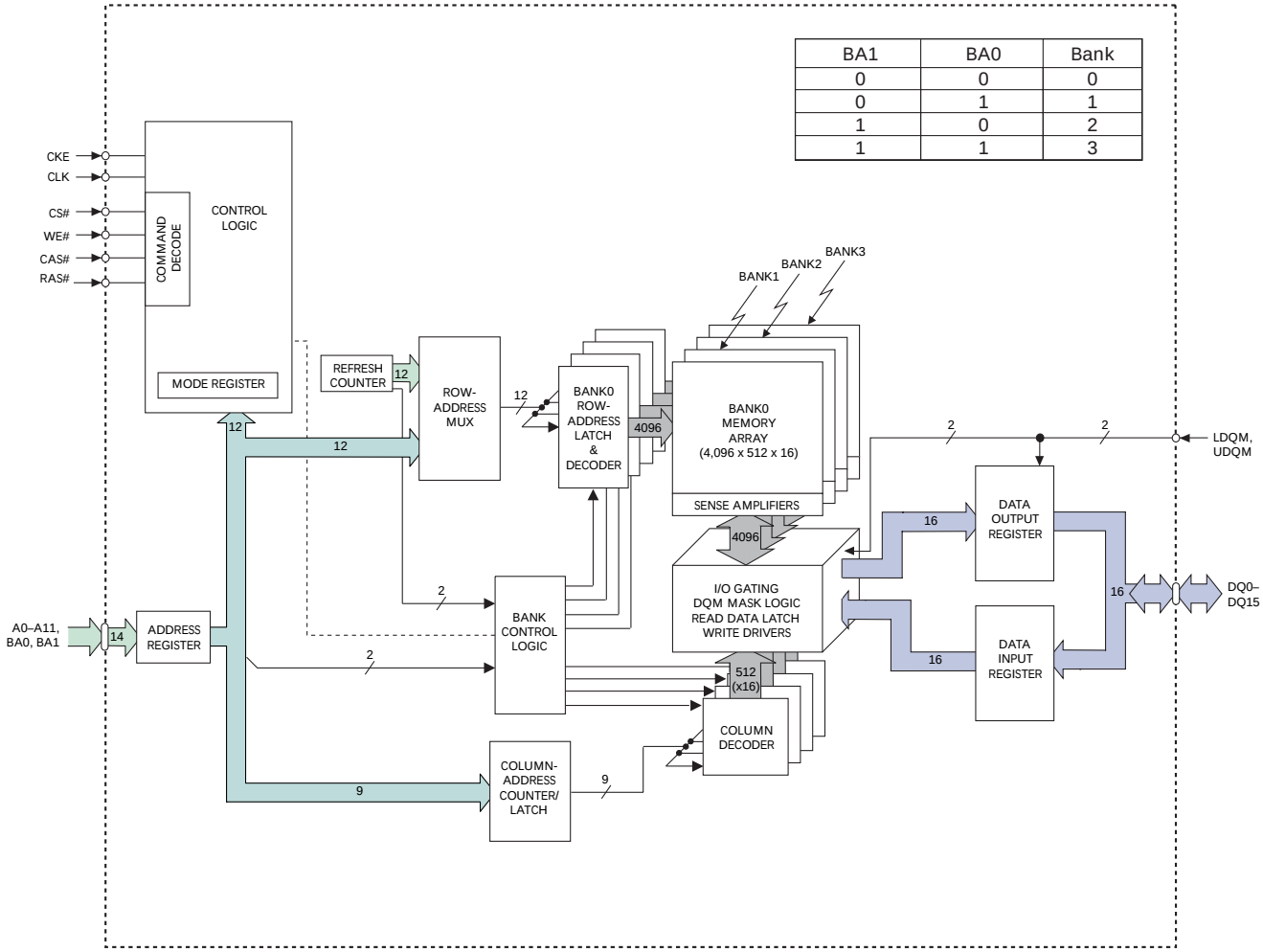


Table 3: Ball Descriptions

54-BALL FBGA	SYMBOL	TYPE	DESCRIPTION
F2	CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
F3	CKE	Input	Clock enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides PRECHARGE power-down and SELF REFRESH operation (all banks idle), ACTIVE power-down (row active in any bank), deep power-down (all banks idle), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
G9	CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
F7, F8, F9	CAS#, RAS#, WE#	Input	Command inputs: CAS#, RAS#, and WE# (along with CS#) define the command being entered.
E8, F1	LDQM, UDQM	Input	Input/Output mask: DQM is sampled HIGH and is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) during a READ cycle. LDQM corresponds to DQ0–DQ7, UDQM corresponds to DQ8–DQ15. LDQM and UDQM are considered same state when referenced as DQM. DQM loading is designed to match that of DQ balls.
G7, G8	BA0, BA1	Input	Bank address input(s): BA0 and BA1 define to which bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied. These balls also select between the mode register and the extended mode register.
H7, H8, J8, J7, J3, J2, H3, H2, H1, G3, H9, G2	A0–A11	Input	Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ or WRITE commands, to select one location out of the memory array in the respective bank. During a PRECHARGE command, A10 determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0, BA1) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
A8, B9, B8, C9, C8, D9, D8, E9, E1, D2, D1, C2, C1, B2, B1, A2	DQ0–DQ15	I/O	Data input/output: Data bus.
E2, G1	DNU/NC	–	DNU = do not use: Must be left unconnected. NC = no connect (internally unconnected): Can be left unconnected, but it is recommended that it is connected to V_{SS}.
A7, B3, C7, D3	$V_{DD}Q$	Supply	DQ power: Provide isolated power to DQs for improved noise immunity.
A3, B7, C3, D7	$V_{SS}Q$	Supply	DQ ground: Provide isolated ground to DQs for improved noise immunity.
A9, E7, J9	V_{DD}	Supply	Core power supply.
A1, E3, J1	V_{SS}	Supply	Ground.

Functional Description

In general, the 128Mb SDRAMs (2 Meg x 16 x 4 banks) are quad-bank DRAMs that operate at 1.8V and include a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the x16's 33,554,432-bit banks is organized as 4,096 rows by 512 columns by 16 bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0 and BA1 select the bank, A0–A11 select the row). The address bits (A0–A8) registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions, and device operation.

Initialization

SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Power should be applied to V_{DD} and $V_{DD}Q$ simultaneously. Once the power is applied to V_{DD} and $V_{DD}Q$, and the clock is stable (stable clock is defined as a signal cycling within timing constraints specified for the clock pin), the SDRAM requires a 100µs delay prior to issuing any command other than a COMMAND INHIBIT or NOP. Starting at some point during this 100µs period and continuing at least through the end of this period, COMMAND INHIBIT or NOP commands should be applied.

Once the 100µs delay has been satisfied with at least one COMMAND INHIBIT or NOP command having been applied, a PRECHARGE command should be applied. All banks must then be precharged, thereby placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SDRAM is ready for mode register programming. Because the mode register will power up in an unknown state, it should be loaded prior to applying any operational command.

Mode Register Definition

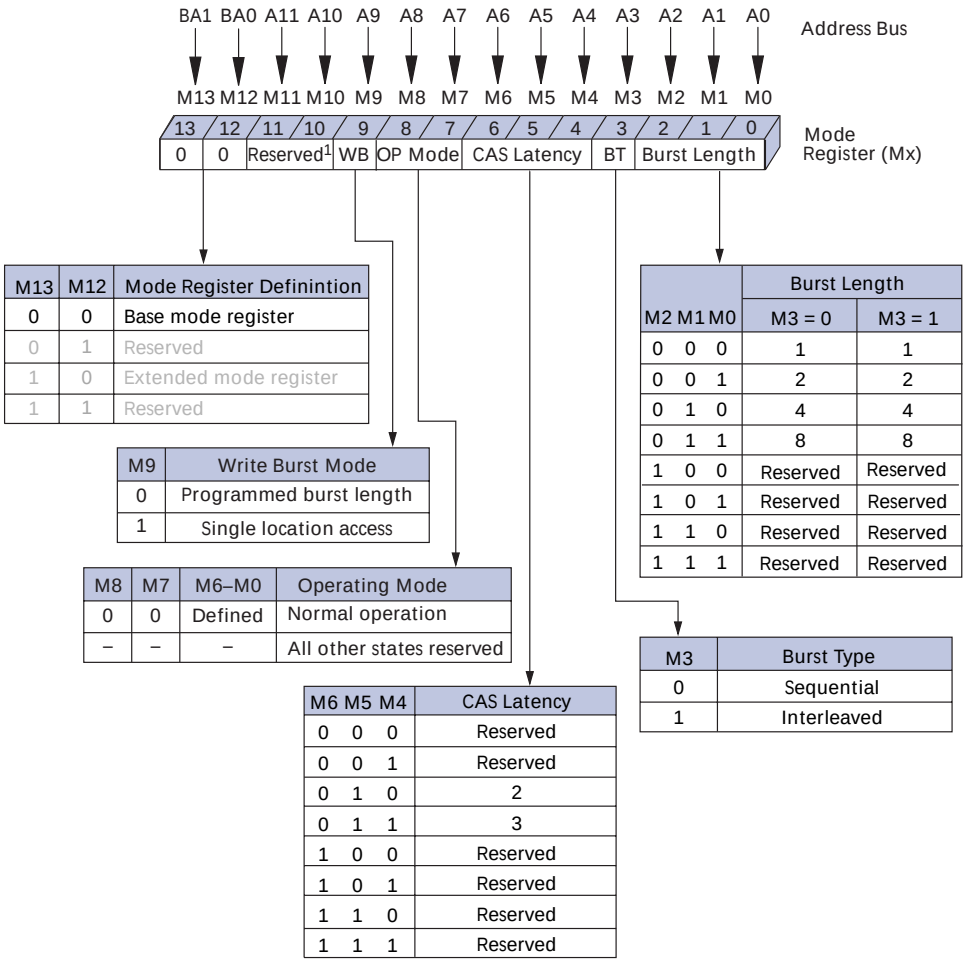
There are two mode registers in the mobile component, the mode register and the extended mode register. The mode register is illustrated in Figure 4 on page 9 and the extended mode register is illustrated in Figure 6 on page 12.

The mode register defines the specific mode of operation of the SDRAM, including BL, burst type, CAS latency (CL), operating mode, and write burst mode. The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.

Mode register bits M0–M2 specify BL, M3 specifies the type of burst (sequential or interleaved), M4–M6 specify the CL, M7 and M8 specify the operating mode, M9 specifies the write burst mode, and M10, and M11 should be set to zero. M12 and M13 should be set to zero to select the mode register.

The mode register must be loaded when all banks are idle, and the controller must wait ^{t}MRD before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Figure 4: Mode Register Definition



M13	M12	Mode Register Definintion
0	0	Base mode register
0	1	Reserved
1	0	Extended mode register
1	1	Reserved

M9	Write Burst Mode
0	Programmed burst length
1	Single location access

M8	M7	M6–M0	Operating Mode
0	0	Defined	Normal operation
–	–	–	All other states reserved

M6	M5	M4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

			Burst Length	
M2	M1	M0	M3 = 0	M3 = 1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Reserved	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

Notes: 1. Must be programmed “0,0” to ensure compatibility with future devices.

Burst Length (BL)

Read and write accesses to the SDRAM are burst oriented, with BL being programmable, as shown in Figure 4. BL determines the maximum number of column locations that can be accessed for a given READ or WRITE command. BLs of 1, 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to BL is selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1–A8 when BL = 2; by A2–A8 when BL = 4; and by A3–A8 when BL = 8. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by BL, the burst type, and the starting column address, as shown in Table 4 on page 10.

Table 4: Burst Definition
Note 1

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
2^2			**A0**		
			0	0-1	0-1
			1	1-0	1-0
4^3		**A1**	**A0**		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8^4	**A2**	**A1**	**A0**		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

Notes:
1. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
2. For BL = 2, A1–A8 select the block-of-two burst; A0 selects the starting column within the block.
3. For BL = 4, A2–A8 select the block-of-four burst; A0–A1 select the starting column within the block.
4. For BL = 8, A3–A8 select the block-of-eight burst; A0–A2 select the starting column within the block.

CAS Latency (CL)

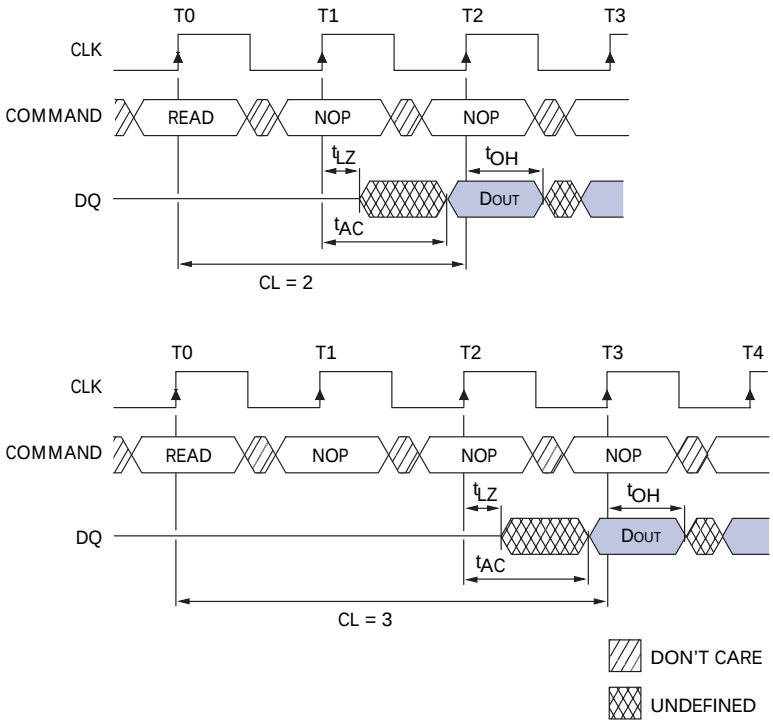
The CL is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to two or three clocks.

If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available by clock edge *n* + *m*. The DQs will start driving as a result of the clock edge one cycle earlier (*n* + *m* - 1), and provided that the relevant access times are met, the data will be valid by clock edge *n* + *m*. For example, assuming that the clock cycle time is such that all relevant access times are met, if a READ command is registered at T0

and the latency is programmed to two clocks, the DQs will start driving after T1 and the data will be valid by T2, as shown in Figure 5. Table 5 indicates the operating frequencies at which each CL setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Figure 5: CAS Latency



Operating Mode

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use. The programmed BL applies to both read and write bursts.

Reserved states should not be used because unknown operation or incompatibility with future versions may result.

Write Burst Mode

When M9 = 0, BL programmed via M0–M2 applies to both READ and WRITE bursts; when M9 = 1, the programmed BL applies to READ bursts, but write accesses are single-location accesses.

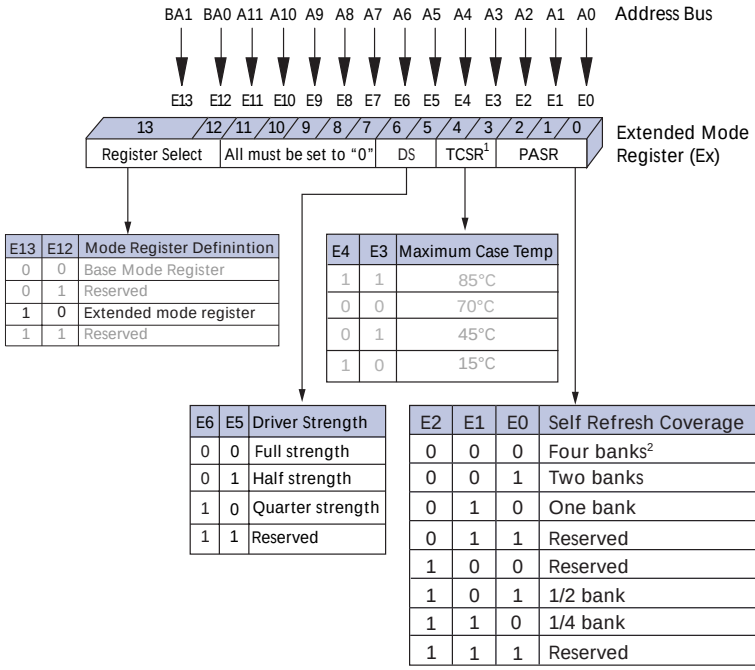
Extended Mode Register

The extended mode register controls the functions beyond those controlled by the mode register. These additional functions are special features of the mobile device. They include temperature-compensated self refresh (TCSR) control, PASR, and output drive strength.

The extended mode register is programmed via the MODE REGISTER SET command (with BA1 = 1 and BA0 = 0) and retains the stored information until it is programmed again or the device loses power.

The extended mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

Figure 6: Extended Mode Register Diagram



E13	E12	Mode Register Definintion
0	0	Base Mode Register
0	1	Reserved
1	0	Extended mode register
1	1	Reserved

E4	E3	Maximum Case Temp
1	1	85°C
0	0	70°C
0	1	45°C
1	0	15°C

E6	E5	Driver Strength
0	0	Full strength
0	1	Half strength
1	0	Quarter strength
1	1	Reserved

E2	E1	E0	Self Refresh Coverage
0	0	0	Four banks[2]
0	0	1	Two banks
0	1	0	One bank
0	1	1	Reserved
1	0	0	Reserved
1	0	1	1/2 bank
1	1	0	1/4 bank
1	1	1	Reserved

Notes: 1. On-die temperature sensor is used in place of the TCSR. Setting these bits has no effect.

Temperature-Compensated Self Refresh (TCSR)

On this version of the Mobile SDR SDRAM, a temperature sensor is implemented for automatic control of the self refresh oscillator on the device. Therefore, it is recommended not to program or use the temperature-compensated self refresh control bits in the extended mode register.

Programming of the TCSR bits has no effect on the device. The self refresh oscillator will continue refresh at the factory programmed optimal rate for the device temperature.

Partial-Array Self Refresh (PASR)

For further power savings during SELF REFRESH, the PASR feature allows the controller to select the amount of memory that will be refreshed during SELF REFRESH. The following refresh options are available:

1. All banks (banks 0, 1, 2, and 3).
2. Two banks (banks 0 and 1; BA1 = 0)
3. One bank (bank 0; BA1 = BA0 = 0)
4. Half bank (bank 0, BA1 = BA0 = row address MSB = 0)
5. Quarter bank (bank0, BA1 = BA0 = row address MSB = row address MSB - 1 = 0)

WRITE and READ commands occur to any bank selected during standard operation, but only the selected banks, or segments of banks, in PASR will be refreshed during SELF REFRESH. It is important to note that data in unused banks, or portions of banks, will be lost when PASR is used.

Driver Strength

Bits E5 and E6 of the extended mode register can be used to select the driver strength of the DQ outputs. This value should be set according to the application's requirements. Full drive strength is suitable to drive higher load systems. Half drive strength is intended for multi-drop systems with various loads. Quarter drive strength is intended for lighter loads or point-to-point systems.

Commands

Truth Table 1 provides a quick reference of available commands. This is followed by a written description of each command. Three additional Truth Tables appear following "Operation" on page 17; these tables provide current state/next state information.

Table 5: Truth Table 1 – Commands and DQM Operation
Note 1; notes appear below table

Name (Function)	CS#	RAS#	CAS#	WE#	DQM	ADDR	DQs	Notes
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/Row	X	2
READ (Select bank and column, and start READ burst)	L	H	L	H	L/H	Bank/Col	X	3
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	L/H	Bank/Col	Valid	3
BURST TERMINATE or deep power-down (Enter deep power-down mode)	L	H	H	L	X	X	X	4, 5
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Bank, A10	X	6
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	X	X	7, 8
LOAD MODE REGISTER/LOAD EXTENDED MODE REGISTER	L	L	L	L	X	Op-Code	X	9
Write enable/output enable	X	X	X	X	L	X	Active	10
Write inhibit/output High-Z	X	X	X	X	H	X	High-Z	10

Notes:
1. CKE is HIGH for all commands shown except SELF REFRESH and deep power-down.
2. A0–A11 provide row address, and BA0, BA1 determine which bank is made active.
3. A0–A8 provide column address; A10 HIGH enables the auto precharge feature (non persistent), while A10 LOW disables the auto precharge feature; BA0, BA1 determine which bank is being read from or written to.
4. This command is BURST TERMINATE when CKE is HIGH and deep power-down when CKE is LOW.
5. The purpose of the BURST TERMINATE command is to stop a data burst, thus the command could coincide with data on the bus. However, the DQs column reads a "Don't Care" state to illustrate that the BURST TERMINATE command can occur when there is no data present.
6. A10 LOW: BA0, BA1 determine the bank being precharged. A10 HIGH: All banks precharged and BA0, BA1 are "Don't Care."
7. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
8. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
9. A0-A11 define op-code written to mode register.
10. Activates or deactivates the DQs during WRITEs (zero-clock delay) and READs (two-clock delay). LDQM controls DQ0–7, UDQM controls DQ8–15.

COMMAND INHIBIT

The COMMAND INHIBIT function prevents new commands from being executed by the SDRAM, regardless of whether the CLK signal is enabled. The SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to perform a NOP to an SDRAM which is selected (CS# is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE REGISTER

The mode register is loaded via inputs A0–A11, BA0, BA1. See "Mode Register Definition" on page 8. The LOAD MODE REGISTER and LOAD EXTENDED MODE REGISTER commands can only be issued when all banks are idle, and a subsequent executable command cannot be issued until ^{t}MRD is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A11 selects the row. This row remains active (or open) for accesses until a precharge command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A8 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the read burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Read data appears on the DQ subject to the logic level on the DQM inputs 2 clocks earlier. If a given DQM signal was registered HIGH, the corresponding DQ will be High-Z two clocks later; if the DQM signal was registered LOW, the DQ will provide valid data.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A8 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the write burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQ is written to the memory array subject to the DQM input logic level appearing coincident with the data. If a given DQM signal is registered LOW, the corresponding data will be written to memory; if the DQM signal is registered HIGH, the corresponding data inputs will be ignored, and a write will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (^{t}RP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only 1 bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

Auto Precharge

Auto precharge is a feature which performs the same individual-bank precharge function described above, without requiring an explicit command. This is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. Auto precharge is non persistent because it is either enabled or disabled for each individual READ or WRITE command.

Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge time (^{t}RP) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type in "Operation" on page 17.

BURST TERMINATE

The BURST TERMINATE command is used to truncate fixed-length bursts. The most recently registered READ or WRITE command prior to the BURST TERMINATE command will be truncated, as shown in "Operation" on page 17.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the SDRAM and is analogous to CAS#-BEFORE-RAS# (CBR) refresh in conventional DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required. All active banks must be PRECHARGED prior to issuing an AUTO REFRESH command. The AUTO REFRESH command should not be issued until the minimum ^{t}RP has been met after the PRECHARGE command as shown in "Operation" on page 17.

The addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an AUTO REFRESH command. The 128Mb SDRAM requires 4,096 AUTO REFRESH cycles every 64ms (^{t}REF). Providing a distributed AUTO REFRESH command every 15.625µs will meet the refresh requirement and ensure that each row is refreshed. Alternatively, 4,096 AUTO REFRESH commands can be issued in a burst at the minimum cycle rate (^{t}RFC), once every 64ms.

SELF REFRESH

The SELF REFRESH command can be used to retain data in the SDRAM, even if the rest of the system is powered down, as long as power is not completely removed from the SDRAM. When in the self refresh mode, the SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command

except CKE is disabled (LOW). Once the SELF REFRESH command is registered, all the inputs to the SDRAM become "Don't Care" with the exception of CKE, which must remain LOW.

During self refresh, the device is refreshed as identified in the extended mode register (see PASR setting). The SDRAM must remain in self refresh mode for a minimum period equal to ^{t}RAS and may remain in self refresh mode for an indefinite period beyond that.

The procedure for exiting self refresh requires a sequence of commands. First, CLK must be stable (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) prior to CKE going back HIGH. Once CKE is HIGH, the SDRAM must have NOP commands issued (a minimum of two clocks) for ^{t}XSR because time is required for the completion of any internal refresh in progress.

Upon exiting the self refresh mode, AUTO REFRESH commands should be issued at once and then every 15.625µs or less, as both SELF REFRESH and AUTO REFRESH utilize the row refresh counter.

Deep Power-Down

Deep power-down is an operating mode used to achieve maximum power reduction by eliminating the power to the memory array. Data will not be retained once the device enters deep power-down mode.

This mode is entered by having all banks idle then CS# and WE# held LOW with RAS# and CAS# held HIGH at the rising edge of the clock, while CKE is LOW. This mode is exited by asserting CKE HIGH.

Operation

Bank/Row Activation

Before any READ or WRITE commands can be issued to a bank within the SDRAM, a row in that bank must be "opened." This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated (see Figure 7 on page 18).

After opening a row (issuing an ACTIVE command), a READ or WRITE command may be issued to that row, subject to the ^{t}RCD specification. ^{t}RCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a ^{t}RCD specification of 20ns with a 125 MHz clock (8ns period) results in 2.5 clocks, rounded to 3. This is reflected in Figure 8 on page 18, which covers any case where $2 < {}^{t}\text{RCD (MIN)}/{}^{t}\text{CK} \leq 3$. (The same procedure is used to convert other specification limits from time units to clock cycles.)

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been "closed" (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by ^{t}RC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by ^{t}RRD.

Figure 7: Activating a Specific Row in a Specific Bank Register

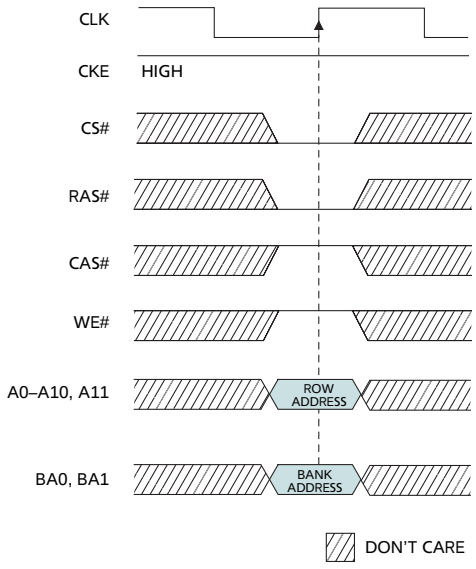
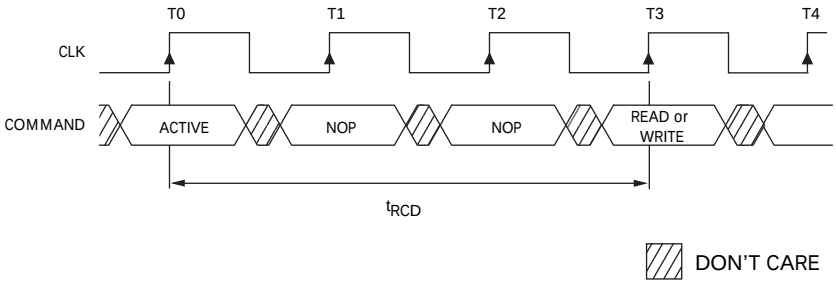


Figure 8: Meeting ^{t}RCD (MIN) When 2 < ^{t}RCD (MIN)/^{t}CK≤ 3



READs

READ bursts are initiated with a READ command, as shown in Figure 9 on page 19.

The starting column and bank addresses are provided with the READ command, and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic READ commands used in the following illustrations, auto precharge is disabled.

During READ bursts, the valid data-out element from the starting column address will be available following the CL after the READ command. Each subsequent data-out element will be valid by the next positive clock edge. Figure 5 on page 11, shows general timing for each possible CL setting.

Upon completion of a burst, assuming no other commands have been initiated, the DQ will go High-Z.

Data from any READ burst may be truncated with a subsequent READ command, and data from a fixed-length READ burst may be immediately followed by data from a READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the

last desired data element of a longer burst that is being truncated. The new READ command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* = CL - 1.

This is shown in Figure 10 on page 20 for CAS latencies of two and three; data element *n* + 3 is either the last of a burst of four or the last desired of a longer burst. The 128Mb SDRAM uses a pipelined architecture and therefore does not require the 2*n* rule associated with a prefetch architecture. A READ command can be initiated on any clock cycle following a previous READ command. Full-speed random read accesses can be performed to the same bank, as shown in Figure 11 on page 21, or each subsequent READ may be performed to a different bank.

Data from any READ burst may be truncated with a subsequent WRITE command, and data from a fixed-length READ burst may be immediately followed by data from a WRITE command (subject to bus turnaround limitations). The WRITE burst may be initiated on the clock edge immediately following the last (or last desired) data element from the READ burst, provided that I/O contention can be avoided. In a given system design, there may be a possibility that the device driving the input data will go Low-Z before the SDRAM DQ go High-Z. In this case, at least a single-cycle delay should occur between the last read data and the WRITE command.

Figure 9: READ Command

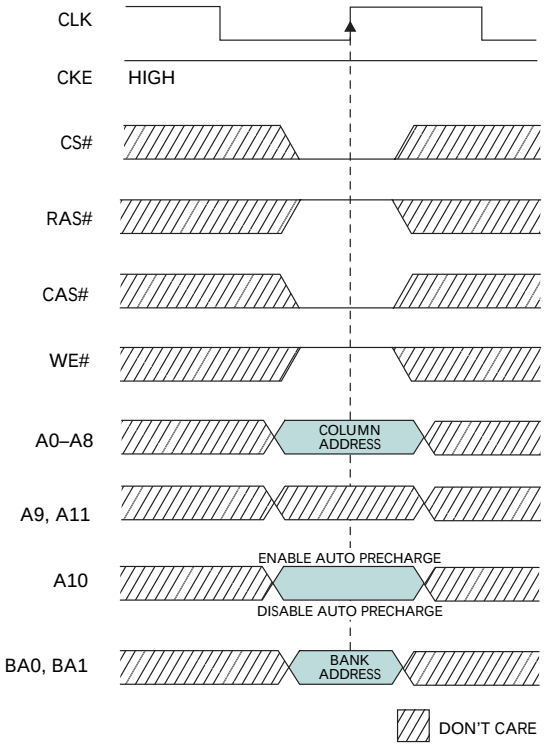
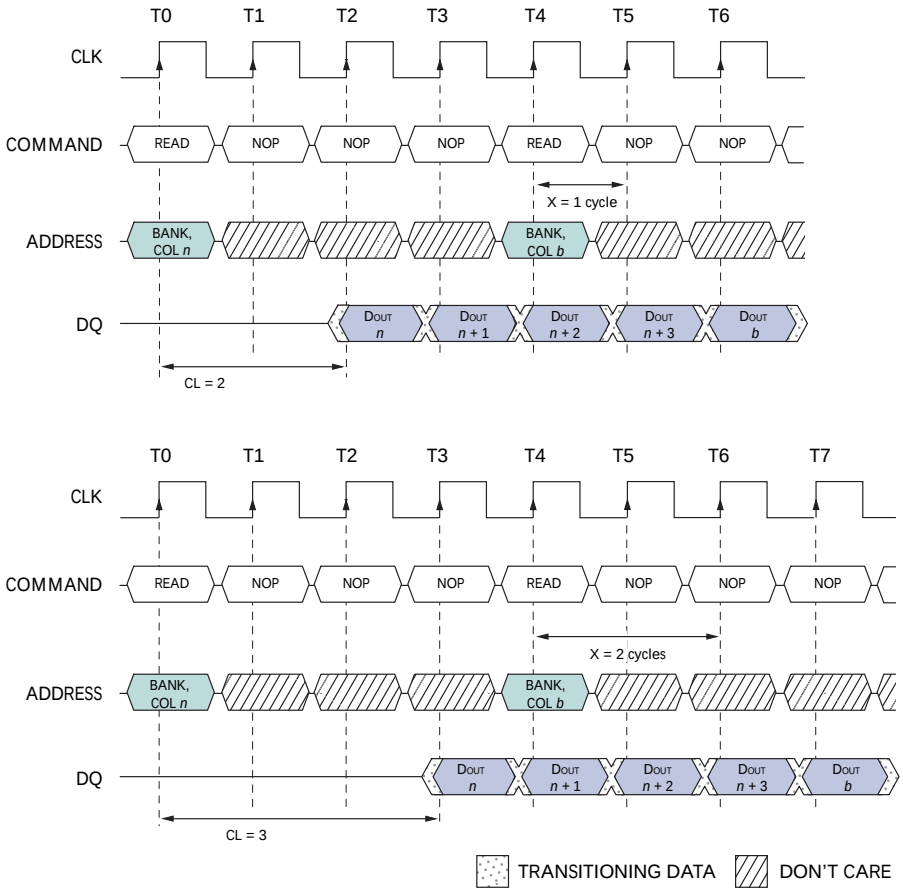
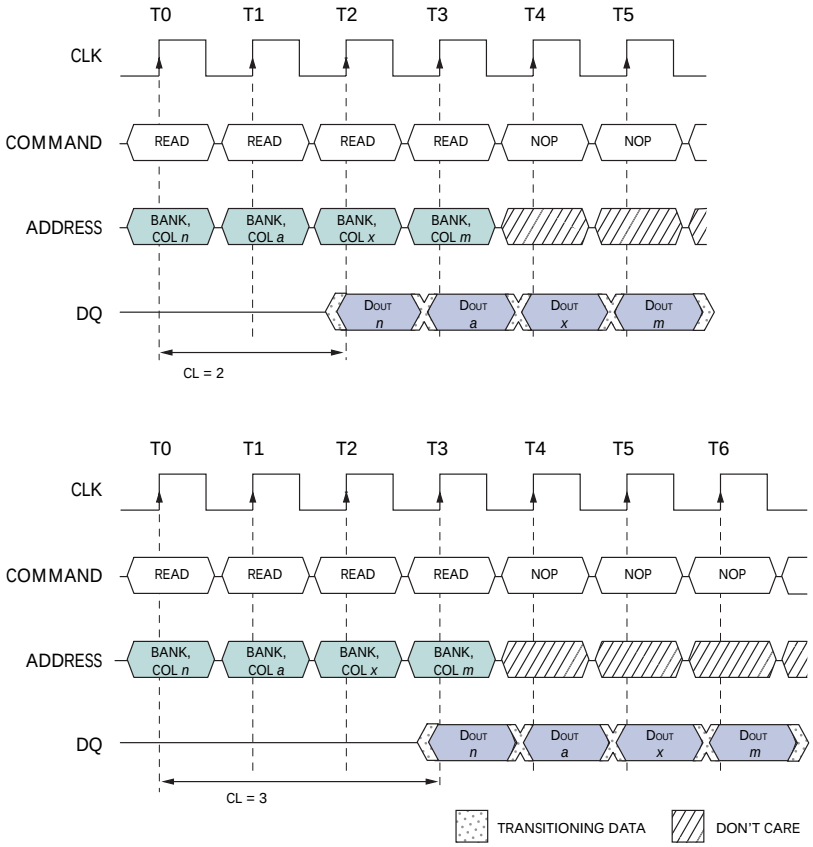


Figure 10: Consecutive READ Bursts



Notes: 1. Each READ command may be to any bank. DQM is LOW.

Figure 11: Random READ Accesses



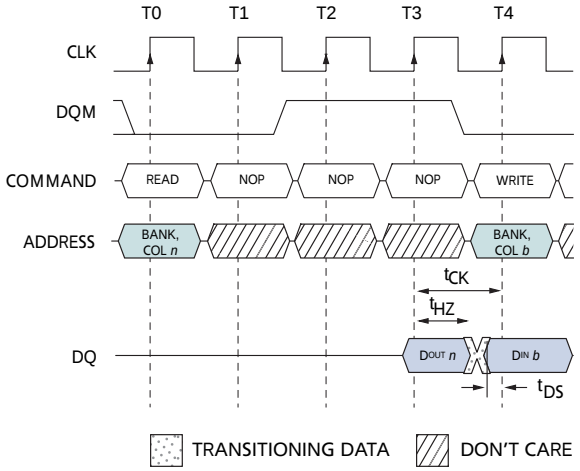
Notes: 1. Each READ command may be to any bank. DQM is LOW.

The DQM input is used to avoid I/O contention, as shown in Figure 12 and Figure 13 on page 22. The DQM signal must be asserted (HIGH) at least 2 clocks prior to the WRITE command (DQM latency is 2 clocks for output buffers) to suppress data-out from the READ. Once the WRITE command is registered, the DQ will go High-Z (or remain High-Z), regardless of the state of the DQM signal, provided the DQM was active on the clock just prior to the WRITE command that truncated the READ command. If not, the second WRITE will be an invalid WRITE. For example, if DQM was LOW during T4 in Figure 14 on page 23, then the WRITEs at T5 and T7 would be valid, while the WRITE at T6 would be invalid.

The DQM signal must be de-asserted prior to the WRITE command (DQM latency is zero clocks for input buffers) to ensure that the written data is not masked. Figure 13 shows the case where the clock frequency allows for bus contention to be avoided without adding a NOP cycle, and Figure 13 shows the case where the additional NOP is needed. A fixed-length READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that auto precharge was not activated). The PRECHARGE command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* = CL - 1. This is shown in Figure 14 for each possible CL; data element *n* + 3 is either the last of a burst of four or the last desired of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^{t}RP is met. Note that part of the row precharge time is hidden during the access of the last data element(s).

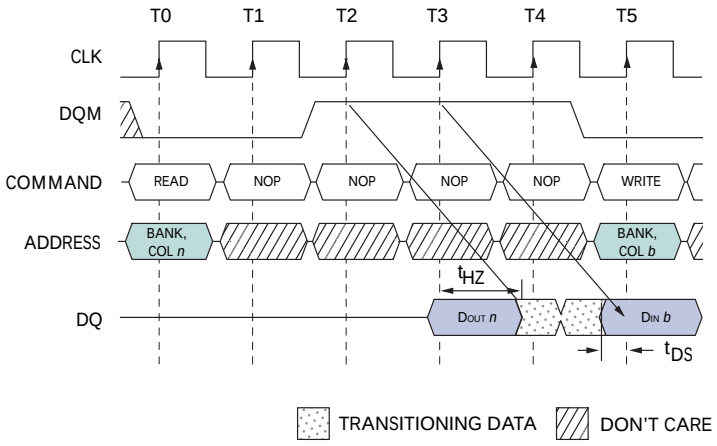
In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst with auto precharge. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command; the advantage of the PRECHARGE command is that it can be used to truncate fixed-length bursts.

Figure 12: READ-to-WRITE



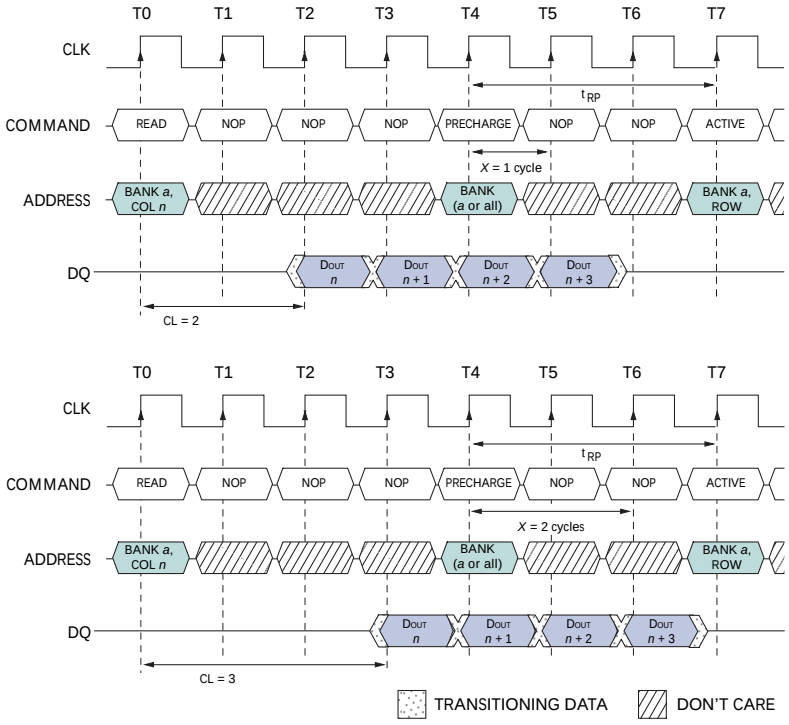
Notes: 1. CL = 3 is used for illustration; the READ command may be to any bank, and the WRITE command may be to any bank. If a burst of one is used, then DQM is not required.

Figure 13: READ-to-WRITE with Extra Clock Cycle



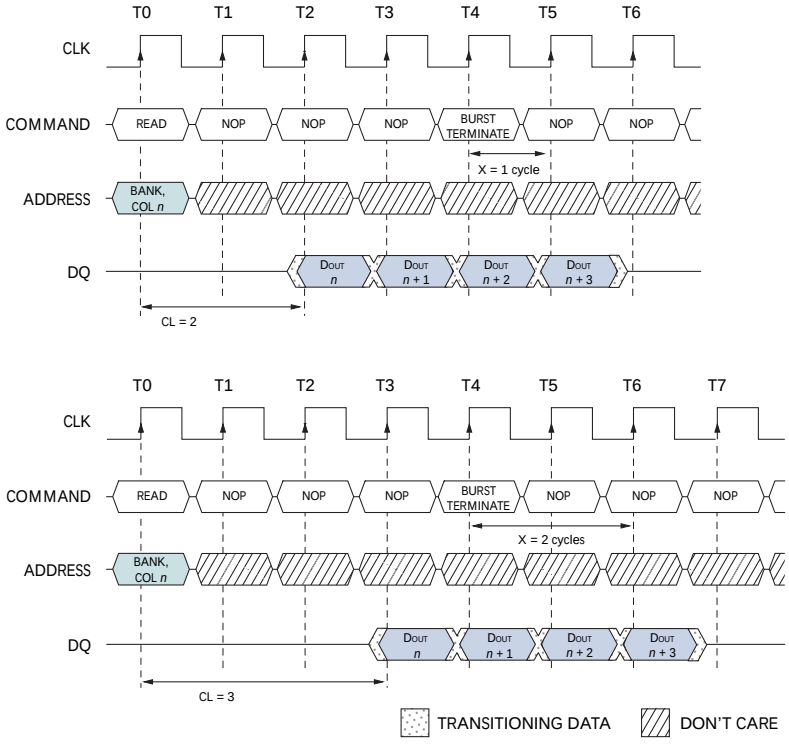
Notes: 1. CL = 3 is used for illustration; the READ command may be to any bank, and the WRITE command may be to any bank.

Figure 14: READ-to-PRECHARGE



Notes: 1. DQM is LOW.

Figure 15: Terminating a READ Burst



Notes: 1. DQM is LOW.

Fixed-length READ bursts may be truncated with a BURST TERMINATE command, provided that auto precharge was not activated. The BURST TERMINATE command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* = CL - 1. This is shown in Figure 15 for each possible CL; data element *n* + 3 is the last desired data element of a longer burst.

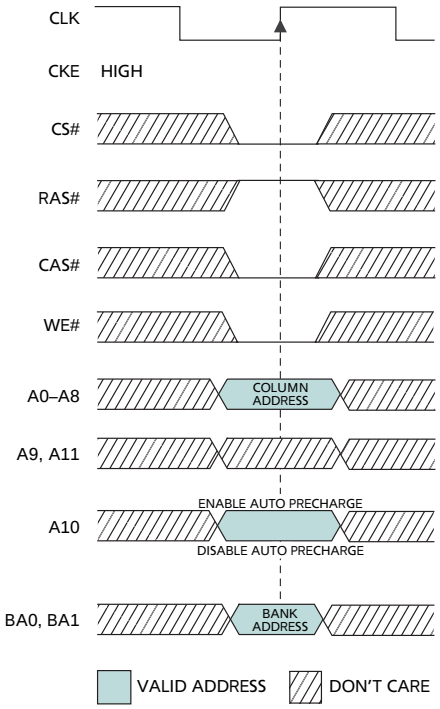
WRITEs

WRITE bursts are initiated with a WRITE command, as shown in Figure 16.

The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic WRITE commands used in the following illustrations, auto precharge is disabled.

During WRITE bursts, the first valid data-in element will be registered coincident with the WRITE command. Subsequent data elements will be registered on each successive positive clock edge. Upon completion of a fixed-length burst, assuming no other commands have been initiated, the DQ will remain High-Z and any additional input data will be ignored (see Figure 17 on page 25).

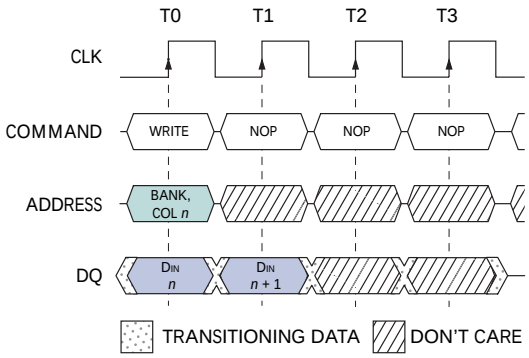
Figure 16: WRITE Command



Data for any WRITE burst may be truncated with a subsequent WRITE command, and data for a fixed-length WRITE burst may be immediately followed by data for a WRITE command. The new WRITE command can be issued on any clock following the previous WRITE command, and the data provided coincident with the new command applies to the new command. An example is shown in Figure 18 on page 25. Data *n* + 1 is either the last of a burst of two or the last desired of a longer burst. The Mobile SDRAM uses a pipelined architecture and therefore does not require the 2*n* rule associated with a prefetch architecture. A WRITE command can be initiated on any clock cycle following a previous

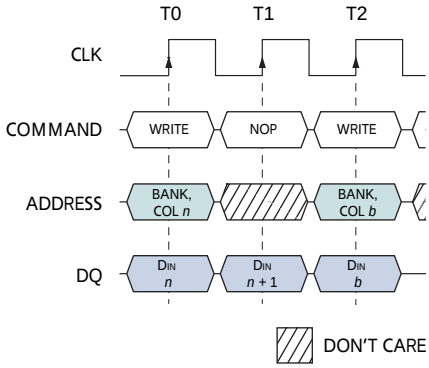
WRITE command. Full-speed random write accesses within a page can be performed to the same bank, as shown in Figure 19, or each subsequent WRITE may be performed to a different bank.

Figure 17: WRITE Burst



Notes: 1. BL = 2. DQM is LOW.

Figure 18: WRITE-to-WRITE



Notes: 1. DQM is LOW. Each WRITE command may be to any bank.

Data for any WRITE burst may be truncated with a subsequent READ command, and data for a fixed-length WRITE burst may be immediately followed by a READ command. Once the READ command is registered, the data inputs will be ignored, and WRITEs will not be executed. An example is shown in Figure 20 on page 26. Data *n* + 1 is either the last of a burst of two or the last desired of a longer burst.

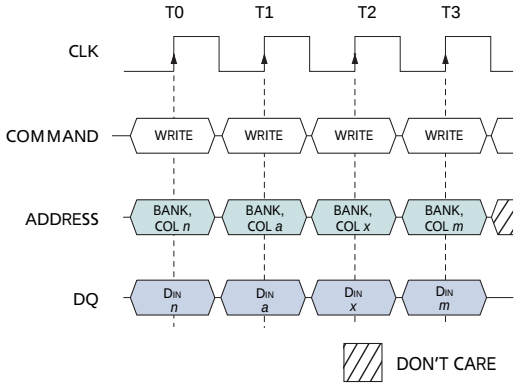
Data for a fixed-length WRITE burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that auto precharge was not activated). The PRECHARGE command should be issued ^{t}WR after the clock edge at which the last desired input data element is registered. The auto precharge mode requires a ^{t}WR of at least one clock plus time, regardless of frequency.

In addition, when truncating a WRITE burst, the DQM signal must be used to mask input data for the clock edge prior to, and the clock edge coincident with, the PRECHARGE command. An example is shown in Figure 21 on page 27. Data *n* + 1 is either the last of a burst of two or the last desired of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^{t}RP is met.

In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst with auto precharge. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command; the advantage of the PRECHARGE command is that it can be used to truncate fixed-length bursts.

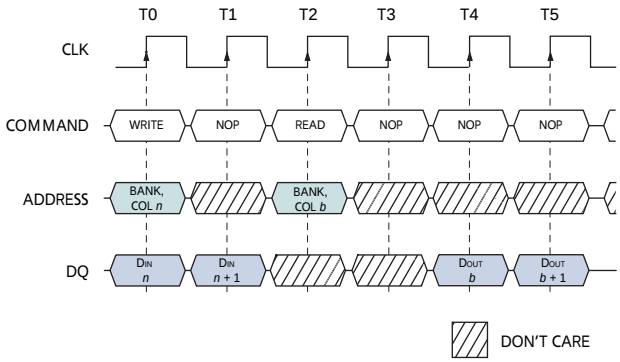
Fixed-length WRITE bursts can be truncated with the BURST TERMINATE command. When truncating a WRITE burst, the input data applied coincident with the BURST TERMINATE command will be ignored. The last data written (provided that DQM is LOW at that time) will be the input data applied one clock previous to the BURST TERMINATE command. This is shown in Figure 22 on page 27, where data *n* is the last desired data element of a longer burst.

Figure 19: Random WRITE Cycles



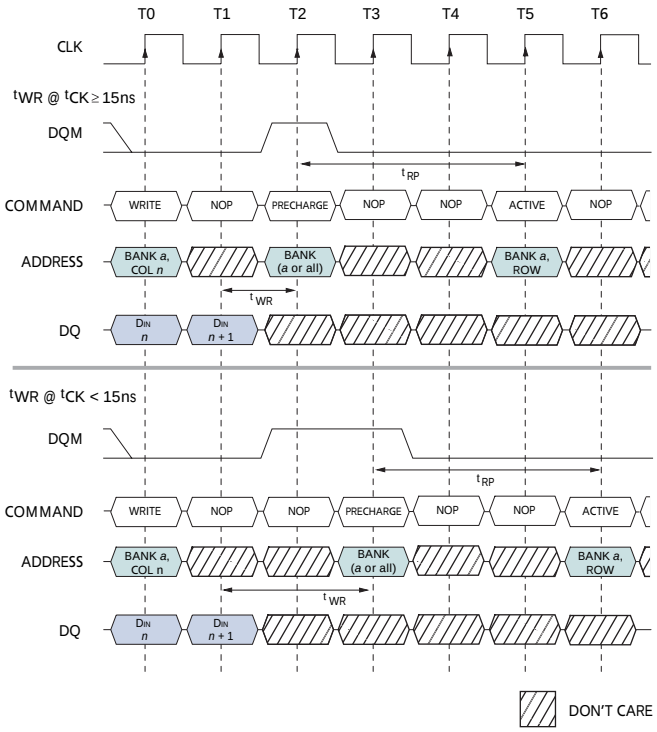
Notes: 1. Each WRITE command may be to any bank. DQM is LOW.

Figure 20: WRITE-to-READ



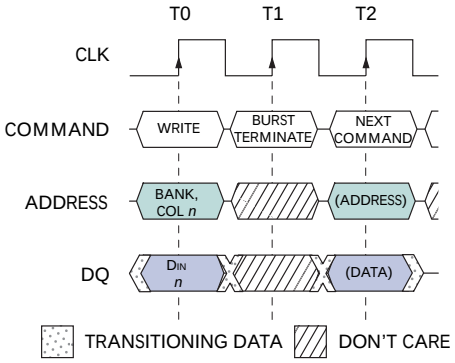
Notes: 1. CL = 2 is used for illustration; the WRITE command may be to any bank, and the READ command may be to any bank. DQM is LOW.

Figure 21: WRITE-to-PRECHARGE



Notes: 1. DQM could remain LOW in this example if the WRITE burst is a fixed length of two.

Figure 22: Terminating a WRITE Burst

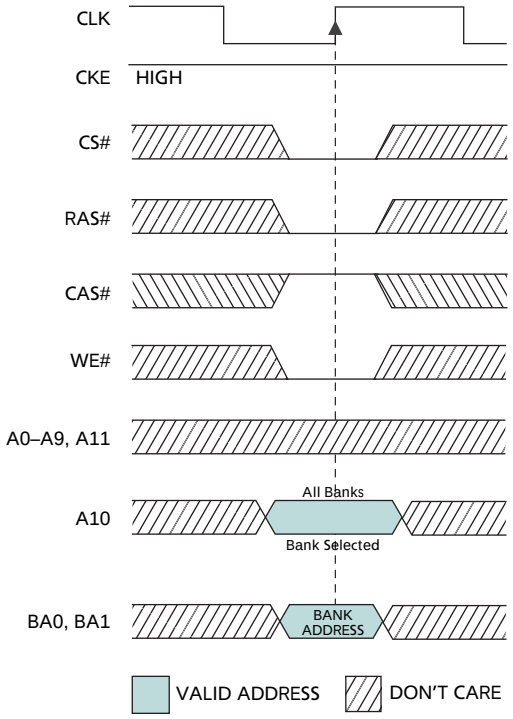


Notes: 1. DQMs are LOW.

PRECHARGE

The PRECHARGE command (see Figure 23 on page 28) is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (^{t}RP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

Figure 23: PRECHARGE Command

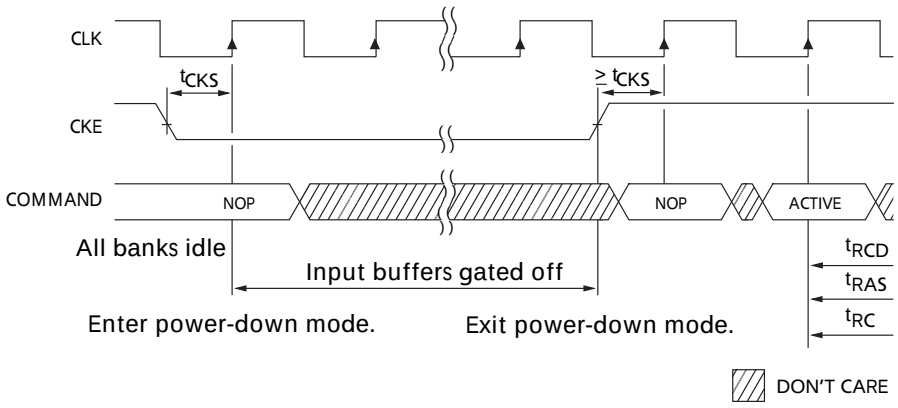


Power-Down

Power-down occurs if CKE is registered LOW coincident with a NOP or COMMAND INHIBIT when no accesses are in progress. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CKE, for maximum power savings while in standby. The device must not remain in the power-down state longer than the refresh period (64ms) since no refresh operations are performed in this mode.

The power-down state is exited by registering a NOP or COMMAND INHIBIT and CKE HIGH at the desired clock edge (meeting ^{t}CKS). See Figure 24 on page 28.

Figure 24: Power-Down



Deep Power-Down

Deep power-down mode is a maximum power savings feature achieved by shutting off the power to the entire memory array of the device. Data in the memory array will not be retained once deep power-down mode is executed. Deep power-down mode is entered by having all banks idle then CS# and WE# held LOW with RAS# and CAS# HIGH at the rising edge of the clock, while CKE is LOW. CKE must be held LOW during deep power-down.

In order to exit deep power-down mode, CKE must be asserted HIGH. Upon exit of deep power-down mode a full Mobile SDRAM initialization sequence, is required.

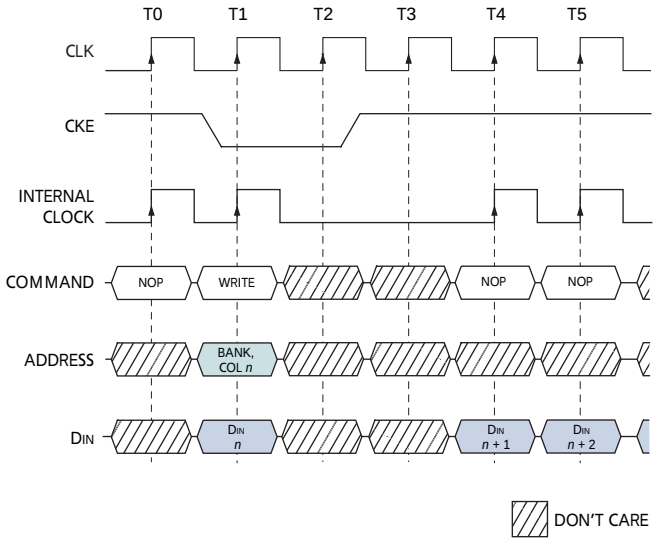
Clock Suspend

The clock suspend mode is entered when a column access/burst is in progress and CKE is registered LOW. In the clock suspend mode, the internal clock is deactivated, "freezing" the synchronous logic.

For each positive clock edge on which CKE is sampled LOW, the next internal positive clock edge is suspended. Any command or data present on the input balls at the time of a suspended internal clock edge is ignored; any data present on the DQ balls remains driven; and burst counters are not incremented, as long as the clock is suspended. (See examples in Figure 25 and Figure 26 on page 30.)

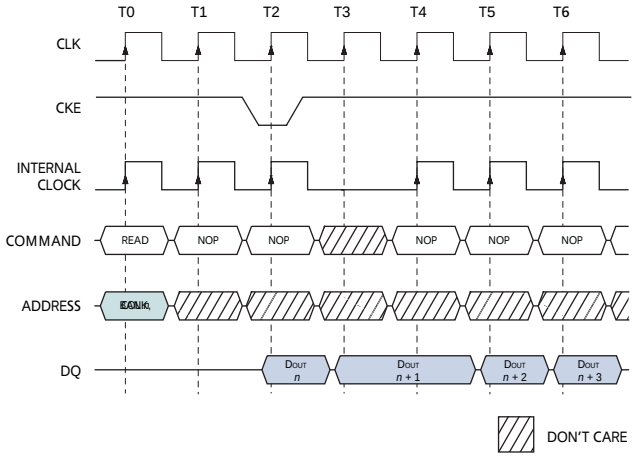
Clock suspend mode is exited by registering CKE HIGH; the internal clock and related operation will resume on the subsequent positive clock edge.

Figure 25: Clock Suspend During WRITE Burst



Notes: 1. BL = 4 or greater, and DM is LOW.

Figure 26: Clock Suspend During READ Burst



Notes: 1. CL = 2, BL = 4 or greater, and DQM is LOW.

Burst Read/Single Write

The burst read/single write mode is entered by programming the write burst mode bit (M9) in the mode register to a logic 1. In this mode, all WRITE commands result in the access of a single column location (burst of one), regardless of the programmed BL. READ commands access columns according to the programmed BL and sequence, just as in the normal mode of operation (M9 = 0).

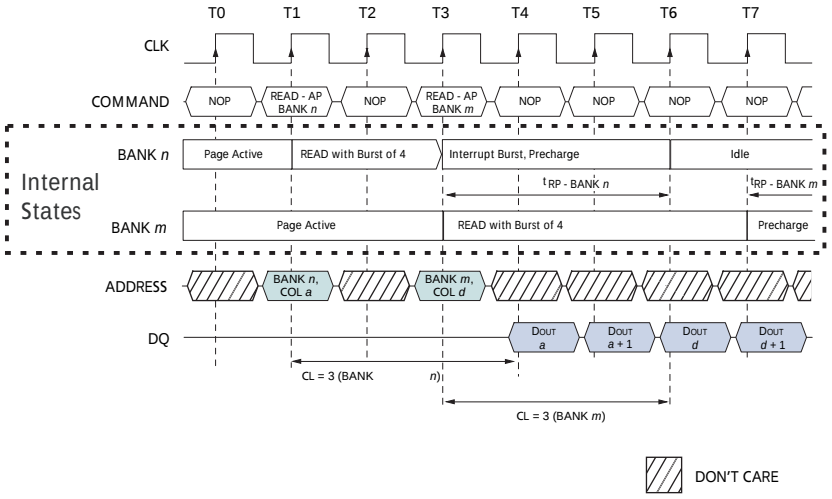
Concurrent Auto Precharge

Micron SDRAM devices support concurrent auto precharge, which allows an access command (READ or WRITE) to another bank while an access command with auto precharge enabled is executing. Four cases where concurrent auto precharge occurs are defined below.

READ with Auto Precharge

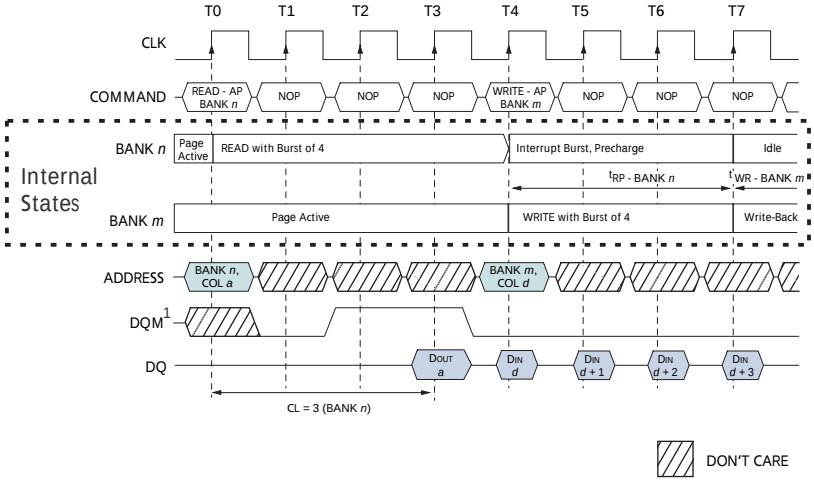
1. Interrupted by a READ (with or without auto precharge): A READ to bank *m* will interrupt a READ on bank *n*, 2 or 3 clocks later, depending on CL. The precharge to bank *n* will begin when the READ to bank *m* is registered (see Figure 27 on page 31).
2. Interrupted by a WRITE (with or without auto precharge): When a WRITE to bank *m* registers, a READ on bank *n* will be interrupted. DQM should be used 2 clocks prior to the WRITE command to prevent bus contention. The precharge to bank *n* will begin when the WRITE to bank *m* is registered (see Figure 28 on page 31).

Figure 27: READ With Auto Precharge Interrupted by a READ



Notes: 1. DQM is LOW.

Figure 28: READ With Auto Precharge Interrupted by a WRITE

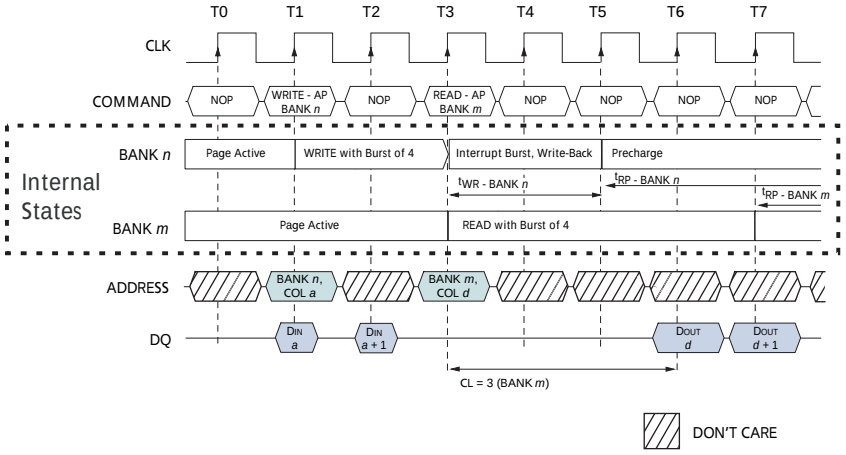


Notes: 1. DQM is HIGH at T2 to prevent DOUT *a* + 1 from contending with DIN *d* at T4.

WRITE with Auto Precharge

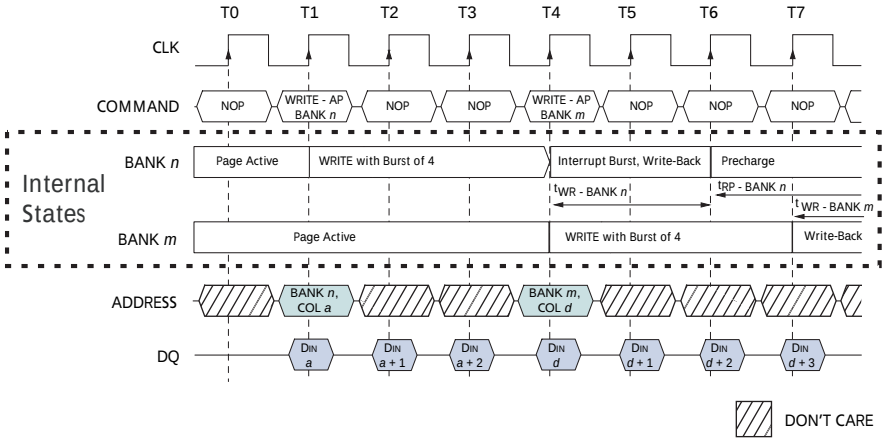
1. Interrupted by a READ (with or without auto precharge): When a READ to bank *m* registers, it will interrupt a WRITE on bank *n*, with the data-out appearing 2 or 3 clocks later, depending on CL. The precharge to bank *n* will begin after ^{t}WR is met, where ^{t}WR begins when the READ to bank *m* is registered. The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m* (see Figure 29).
2. Interrupted by a WRITE (with or without auto precharge): When a WRITE to bank *m* registers, it will interrupt a WRITE on bank *n*. The precharge to bank *n* will begin after ^{t}WR is met, where ^{t}WR begins when the WRITE to bank *m* is registered. The last valid data WRITE to bank *n* will be data registered one clock prior to a WRITE to bank *m* (see Figure 30 on page 32).

Figure 29: WRITE With Auto Precharge Interrupted by a READ



Notes: 1. DQM is LOW.

Figure 30: WRITE With Auto Precharge Interrupted by a WRITE



Notes: 1. DQM is LOW.

Truth Tables

Table 6: Truth Table 2 – CKE

Notes: 1–4; notes appear below table

CKE_{n-1}	CKE_n	Current State	$Command_n$	$Action_n$	Notes
L	L	Power-Down	X	Maintain power-down	
		Self refresh	X	Maintain self refresh	
		Clock suspend	X	Maintain clock suspend	
		Deep power-down	X	Maintain deep power-down	5
L	H	Power-Down	COMMAND INHIBIT or NOP	Exit power-down	6
		Deep power-down	X	Exit deep power-down	5
		Self refresh	COMMAND INHIBIT or NOP	Exit self refresh	7
		Clock suspend	X	Exit clock suspend	8
H	L	All banks idle	COMMAND INHIBIT or NOP	Power-Down entry	
		All banks idle	BURST TERMINATE	Deep power-down entry	5
		All banks idle	AUTO REFRESH	Self refresh entry	
		Reading or Writing	VALID	Clock suspend entry	
H	H		See Truth Table 3		

Notes:
1. CKE_n is the logic state of CKE at clock edge *n*; CKE_{n-1} was the state of CKE at the previous clock edge.
2. Current state is the state of the SDRAM immediately prior to clock edge *n*.
3. $COMMAND_n$ is the command registered at clock edge *n*, and $ACTION_n$ is a result of $COMMAND_n$.
4. All states and sequences not shown are illegal or reserved.
5. Deep power-down is a power-saving feature of this Mobile SDRAM device. This command is BURST TERMINATE when CKE is HIGH and deep power-down when CKE is LOW.
6. Exiting power-down at clock edge *n* will put the device in the all banks idle state in time for clock edge *n* + 1 (provided that ^tCKS is met).
7. Exiting self refresh at clock edge *n* will put the device in the all banks idle state once ^tXSR is met. COMMAND INHIBIT or NOP commands should be issued on any clock edges occurring during the ^tXSR period. A minimum of two NOP commands must be provided during ^tXSR period.
8. After exiting clock suspend at clock edge *n*, the device will resume operation and recognize the next command at clock edge *n* + 1.

Table 7: Truth Table 3 – Current State Bank *n*, Command to Bank *n*
Notes: 1–6; notes appear below table

Current State	CS#	RAS#	CAS#	WE#	Command (Action)	Notes
Any	H	X	X	X	COMMAND INHIBIT (NOP/Continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/Continue previous operation)	
Idle	L	L	H	H	ACTIVE (Select and activate row)	
	L	L	L	H	AUTO REFRESH	7
	L	L	L	L	LOAD MODE REGISTER	7
	L	L	H	L	PRECHARGE	8
Row active	L	H	L	H	READ (Select column and start READ burst)	9
	L	H	L	L	WRITE (Select column and start WRITE burst)	9
	L	L	H	L	PRECHARGE (Deactivate row in bank or banks)	10
Read (auto precharge disabled)	L	H	L	H	READ (Select column and start new READ burst)	9
	L	H	L	L	WRITE (Select column and start WRITE burst)	9
	L	L	H	L	PRECHARGE (Truncate READ burst, start PRECHARGE)	10
	L	H	H	L	BURST TERMINATE	11
Write (auto precharge disabled)	L	H	L	H	READ (Select column and start READ burst)	9
	L	H	L	L	WRITE (Select column and start new WRITE burst)	9
	L	L	H	L	PRECHARGE (Truncate WRITE burst, start PRECHARGE)	10
	L	H	H	L	BURST TERMINATE	11

Notes:

1. This table applies when CKE_{n-1} was HIGH and CKE_n is HIGH (see Truth Table 2) and after ^tXSR has been met (if the previous state was self refresh).
2. This table is bank-specific, except where noted; i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state. Exceptions are covered in the notes below.
3. Current state definitions:

   Idle: The bank has been precharged, and ^tRP has been met.

   Row active: A row in the bank has been activated, and ^tRCD has been met. No data bursts/accesses and no register accesses are in progress.

   Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

   Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

4. The following states must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Truth Table 3, and according to Truth Table 4.

   Precharging: Starts with registration of a PRECHARGE command and ends when ^tRP is met. Once ^tRP is met, the bank will be in the idle state.

   Row activating: Starts with registration of an ACTIVE command and ends when ^tRCD is met. Once ^tRCD is met, the bank will be in the row active state.

   Read w/auto precharge enabled: Starts with registration of a READ command with auto precharge enabled and ends when ^tRP has been met. Once ^tRP is met, the bank will be in the idle state.

   Write w/auto precharge enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when ^tRP has been met. Once ^tRP is met, the bank will be in the idle state.

5. The following states must not be interrupted by any executable command; COMMAND INHIBIT or NOP commands must be applied on each positive clock edge during these states.

Refreshing:	Starts with registration of an AUTO REFRESH command and ends when ^{t}RFC is met. Once ^{t}RFC is met, the SDRAM will be in the all banks idle state.
Accessing mode register:	Starts with registration of a LOAD MODE REGISTER command and ends when ^{t}MRD has been met. Once ^{t}MRD is met, the SDRAM will be in the all banks idle state.
Precharging all:	Starts with registration of a PRECHARGE ALL command and ends when ^{t}RP is met. Once ^{t}RP is met, all banks will be in the idle state.

6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle.
8. Does not affect the state of the bank and acts as a NOP to that bank.
9. READs or WRITEs listed in the Command (Action) column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
10. May or may not be bank-specific; if all banks are to be precharged, all must be in a valid state for precharging.
11. Not bank-specific; BURST TERMINATE affects the most recent READ or WRITE burst, regardless of bank.

Table 8: Truth Table 4 – Current State Bank *n*, Command to Bank *m*

Notes: 1–6; notes appear below and on next page

Current State	CS#	RAS#	CAS#	WE#	Command (Action)	Notes
Any	H	X	X	X	COMMAND INHIBIT (NOP/Continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/Continue previous operation)	
Idle	X	X	X	X	Any command allowed to bank m	
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start READ burst)	7
	L	H	L	L	WRITE (Select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (Auto Precharge Disabled)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start new READ burst)	7, 8
	L	H	L	L	WRITE (Select column and start WRITE burst)	7, 9
	L	L	H	L	PRECHARGE	10
Write (Auto Precharge Disabled)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start READ burst)	7, 11
	L	H	L	L	WRITE (Select column and start new WRITE burst)	7, 12
	L	L	H	L	PRECHARGE	10
Read (With Auto Precharge)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start new READ burst)	7, 13, 14
	L	H	L	L	WRITE (Select column and start WRITE burst)	7, 13, 15
	L	L	H	L	PRECHARGE	10
Write (With Auto Precharge)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start READ burst)	7, 13, 16
	L	H	L	L	WRITE (Select column and start new WRITE burst)	7, 13, 17
	L	L	H	L	PRECHARGE	10

Notes:

1. This table applies when CKE_{n-1} was HIGH and CKE_n is HIGH (see Truth Table 2) and after ^tXSR has been met (if the previous state was self refresh).
2. This table describes alternate bank operation, except where noted; i.e., the current state is for bank *n* and the commands shown are those allowed to be issued to bank *m* (assuming that bank *m* is in such a state that the given command is allowable). Exceptions are covered in the notes below.
3. Current state definitions:

Idle:	The bank has been precharged, and ^tRP has been met.
Row active:	A row in the bank has been activated, and ^tRCD has been met. No data bursts/accesses and no register accesses are in progress.
Read:	A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
Write:	A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
Read w/auto precharge enabled:	Starts with registration of a READ command with auto precharge enabled, and ends when ^tRP has been met. Once ^tRP is met, the bank will be in the idle state.
Write w/auto precharge enabled:	Starts with registration of a WRITE command with auto precharge enabled, and ends when ^tRP has been met. Once ^tRP is met, the bank will be in the idle state.

4. AUTO REFRESH, SELF REFRESH, and LOAD MODE REGISTER commands may only be issued when all banks are idle.

5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs to bank *m* listed in the Command (Action) column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
8. For a READ without auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the READ on bank *n*, CL later (see Figure 10 on page 20).
9. For a READ without auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the READ on bank *n* when registered (see Figure 12 and Figure 13 on page 22). DQM should be used one clock prior to the WRITE command to prevent bus contention.
10. Burst in bank *n* continues as initiated.
11. For a WRITE without auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the WRITE on bank *n* when registered (see Figure 20 on page 26), with the data-out appearing CL later. The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m*.
12. For a WRITE without auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the WRITE on bank *n* when registered (see Figure 18 on page 25). The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m*.
13. Concurrent auto precharge: Bank *n* will initiate the auto precharge command when its burst has been interrupted by bank *m*'s burst.
14. For a READ with auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the READ on bank *n*, CL later (see Figure 27 on page 31). The PRECHARGE to bank *n* will begin when the READ to bank *m* is registered.
15. For a READ with auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the READ on bank *n* when registered (see Figure 28 on page 31). DQM should be used two clocks prior to the WRITE command to prevent bus contention. The PRECHARGE to bank *n* will begin when the WRITE to bank *m* is registered.
16. For a WRITE with auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the WRITE on bank *n* when registered, with the data-out appearing CL later (see Figure 29 on page 32). The PRECHARGE to bank *n* will begin after ^{t}WR is met, where ^{t}WR begins when the READ to bank *m* is registered. The last valid WRITE bank *n* will be data-in registered one clock prior to the READ to bank *m*.
17. For a WRITE with auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the WRITE on bank *n* when registered. The PRECHARGE to bank *n* will begin after ^{t}WR is met, where ^{t}WR begins when the WRITE to bank *m* is registered (see Figure 30 on page 32). The last valid WRITE to bank *n* will be data registered one clock to the WRITE to bank *m*.

Electrical Specifications

Stresses greater than those listed in Table 9 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 9: Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Voltage on V_{DD}/$V_{DD}Q$ supply relative to V_{SS}	V_{DD}/$V_{DD}Q$	–0.35	+2.8	V
Voltage on inputs, NC or I/O pins relative to V_{SS}	V_{IN}	–0.35	+2.8	V
Storage temperature (plastic)	T_{STG}	–55	+150	°C

Table 10: DC Electrical Characteristics and Operating Conditions

Notes: 1, 5, 6; notes appear on page 42; V_{DD} = $V_{DD}Q$ = 1.7–1.95V

Parameter/Condition	Symbol	Min	Max	Units	Notes
Supply voltage	V_{DD}	1.7	1.95	V	
I/O supply voltage	$V_{DD}Q$	1.7	1.95	V	
Input high voltage: Logic 1; All inputs	V_{IH}	0.8 × $V_{DD}Q$	V_{DD} + 0.3	V	22
Input low voltage: Logic 0; All inputs	V_{IL}	–0.3	+0.3	V	22
Output high voltage: All inputs	V_{OH}	0.9 x $V_{DD}Q$	–	V	
Output low voltage: All inputs	V_{OL}	–	0.2	V	
Operating temperature: Commercial Industrial	T_A	 0 –40	 +70 +85	°C	
Input leakage current: Any input 0V ≤ V_{IN} ≤ V_{DD} (All other pins not under test = 0V)	I_I	–1.0	1.0	µA	
Output leakage current: DQ disabled; 0V ≤ V_{OUT} ≤ $V_{DD}Q$	I_{OZ}	–1.5	1.5	µA	

Table 11: Electrical Characteristics and Recommended AC Operating Conditions
Notes: 5, 6, 8, 9, 11; notes appear on page 42

AC Characteristics			-75		-8			
Parameter		**Symbol**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Access time from CLK (pos. edge)	CL = 3	^{t}AC (3)	–	6	–	7	ns	
	CL = 2	^{t}AC (2)	–	8	–	8	ns	
Address hold time		^{t}AH	1	–	1	–	ns	
Address setup time		^{t}AS	2.5	–	2.5	–	ns	
CLK high-level width		^{t}CH	3	–	3	–	ns	
CLK low-level width		^{t}CL	3	–	3	–	ns	
Clock cycle time	CL = 3	^{t}CK (3)	7.5	100	8	100	ns	23
	CL = 2	^{t}CK (2)	9.6	100	12	100	ns	23
CKE hold time		^{t}CKH	1	–	1	–	ns	
CKE setup time		^{t}CKS	2.5	–	2.5	–	ns	
CS#, RAS#, CAS#, WE#, DQM hold time		^{t}CMH	1	–	1	–	ns	
CS#, RAS#, CAS#, WE#, DQM setup time		^{t}CMS	2.5	–	2.5	–	ns	
Data-in hold time		^{t}DH	1	–	1	–	ns	
Data-in setup time		^{t}DS	2.5	–	2.5	–	ns	
Data-out High-Z time	CL = 3	^{t}HZ (3)	–	6	–	7	ns	10
	CL = 2	^{t}HZ (2)	–	8	–	8	ns	10
Data-out Low-Z time		^{t}LZ	1	–	1	–	ns	
Data-out hold time (load)		^{t}OH	2.5	–	2.5	–	ns	
Data-out hold time (no load)		^{t}OH$_{N}$	1.8	–	1.8	–	ns	
ACTIVE-to-PRECHARGE command		^{t}RAS	45	120,000	48	120,000	ns	
ACTIVE-to-ACTIVE command period		^{t}RC	67.5	–	72	–	ns	
ACTIVE-to-READ or WRITE delay		^{t}RCD	19.2	–	24	–	ns	
Refresh period (4,096 rows)		^{t}REF	–	64		64	ms	
AUTO REFRESH period		^{t}RFC	75	–	80	–	ns	
PRECHARGE command period		^{t}RP	19.2	–	24	–	ns	
ACTIVE bank *a* to ACTIVE bank *b* command		^{t}RRD	15	–	16	–	ns	
Transition time		^{t}T	0.5	1.2	0.5	1.2	ns	7
WRITE recovery time		^{t}WR	15	–	15	–	ns	24
Exit SELF REFRESH-to-ACTIVE command		^{t}XSR	75	–	80	–	ns	20

Table 12: AC Functional Characteristics
Notes: 5, 6, 8, 9, 11; notes appear on page 42

Parameter		Symbol	-75	-8	Units	Notes
READ/WRITE command to READ/WRITE command		tCCD	1	1	tCK	17
CKE to clock disable or power-down entry mode		tCKED	1	1	tCK	14
CKE to clock enable or power-down exit setup mode		tPED	1	1	tCK	14
DQM to input data delay		tDQD	0	0	tCK	17
DQM to data mask during WRITEs		tDQM	0	0	tCK	17
DQM to data High-Z during READs		tDQZ	2	2	tCK	17
WRITE command to input data delay		tDWD	0	0	tCK	17
Data-in to ACTIVE command		tDAL	5	5	tCK	15, 21
Data-in to PRECHARGE command		tDPL	2	2	tCK	16, 21
Last data-in to burst STOP command		tBDL	1	1	tCK	17
Last data-in to new READ/WRITE command		tCDL	1	1	tCK	17
Last data-in to PRECHARGE command		tRDL	2	2	tCK	16, 21
LOAD MODE REGISTER command to ACTIVE or REFRESH command		tMRD	2	2	tCK	
Data-out to High-Z from PRECHARGE command	CL = 3	tROH(3)	3	3	tCK	17
	CL = 2	tROH(2)	2	2	tCK	17

Table 13: IDD Specifications and Conditions
Notes: 5, 6, 11, 13; notes appear on page 42; VDD = VDDQ = 1.7–1.95V

Parameter/Condition		Symbol	Max		Units	Notes
			-75	-8		
Operating current: Active mode; BL = 1; READ or WRITE; tRC = tRC (MIN)		IDD1	50	50	mA	3, 18, 19
Standby current: Power-down mode; All banks idle; CKE = LOW		IDD2P	150	150	µA	26
Standby current: Non-power-down mode; All banks idle; CKE = HIGH		IDD2N	10	10	mA	
Standby current: Power-down mode; CKE = LOW; CS# = HIGH; All banks active; No accesses in progress		IDD3P	5	5	mA	3, 12, 19
Standby current: Non-power-down mode; CKE = HIGH; CS# = HIGH; All banks active after tRCD met; No accesses in progress		IDD3N	40	35	mA	3, 12, 19
Operating current: Burst mode; READ or WRITE; All banks active, half DQs toggling every cycle		IDD4	50	50	mA	3, 18, 19
Auto refresh current: CKE = HIGH; CS# = HIGH	tRFC = tRFC (MIN)	IDD5	100	80	mA	3, 12, 18, 19, 25
	tRFC = 15.625µs	IDD6	2	2	mA	
Deep power-down		IZZ	10	10	µA	26, 28

Table 14: IDD7 – Self Refresh Current Options

Notes: 4, 27; notes appear on page 42; VDD = VDDQ = 1.70–1.95

Temperature-Compensated Self Refresh Parameter/Condition	Maximum Temperature	-75/-8	Units
Self refresh current: CKE < 0.2V – 4 banks open	85ºC	300	µA
	70ºC	220	µA
	45ºC	180	µA
	15ºC	160	µA
Self refresh current: CKE < 0.2V – 2 banks open	85ºC	220	µA
	70ºC	180	µA
	45ºC	160	µA
	15ºC	150	µA
Self refresh current: CKE < 0.2V – 1 bank open	85ºC	180	µA
	70ºC	160	µA
	45ºC	150	µA
	15ºC	145	µA
Self refresh current: CKE < 0.2V – 1/2 bank open	85ºC	120	µA
	70ºC	110	µA
	45ºC	100	µA
	15ºC	90	µA
Self refresh current: CKE < 0.2V – 1/4 bank open	85ºC	115	µA
	70ºC	105	µA
	45ºC	95	µA
	15ºC	90	µA

Figure 31: Typical Self Refresh Current vs. Temperature

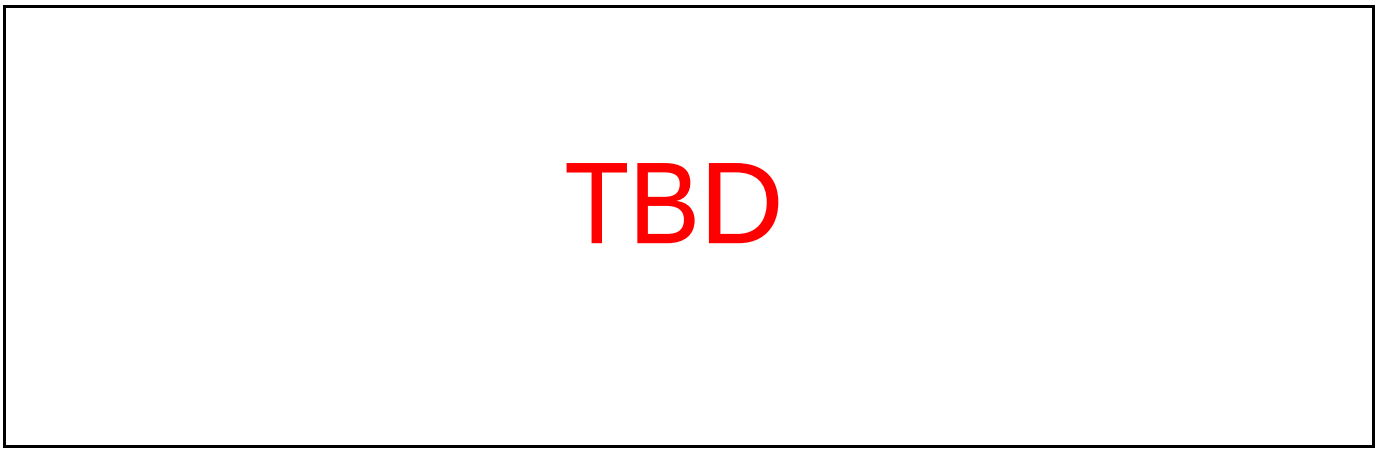


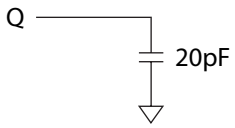
Table 15: Capacitance

Note: 2; notes appear on page 42

Parameter	Symbol	Min	Max	Units
Input capacitance: CLK	CI1	1.5	4.0	pF
Input capacitance: All other input-only balls	CI2	1.5	4.0	pF
Input/Output capacitance: DQ, LDQM, UDQM	CIO	3.0	6.0	pF

Notes

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{DD}, $V_{DD}Q$ = +1.8V; T_A = 25°C; ball under test biased at 1.4V. f = 1 MHz.
3. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. When the device is in self refresh mode, the on-chip refresh oscillator and address counters are enabled.
5. The minimum specifications are used only to indicate cycle time at which proper operation is ensured over the full temperature range (0°C –70°C standard, –40°C– 85°C for IT).
6. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (V_{DD} and $V_{DD}Q$ must be powered up simultaneously. V_{SS} and $V_{SS}Q$ must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
7. AC characteristics assume ^{t}T = 1ns.
8. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
9. Outputs measured for 1.8V at 0.9V with equivalent load:



10. ^{t}HZ defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The last valid data element will meet ^{t}OH before going High-Z.
11. AC timing and I_{DD} tests have V_{IL} and V_{IH}, with timing referenced to $V_{IH}/2$ = crossover point. If the input transition time is longer than ^{t}T (MAX), then the timing is referenced at V_{IL} (MAX) and V_{IH} (MIN) and no longer at the $V_{IH}/2$ crossover point.
12. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid V_{IH} or V_{IL} levels.
13. I_{DD} specifications are tested after the device is properly initialized.
14. Timing actually specified by ^{t}CKS; clock(s) specified as a reference only at minimum cycle rate.
15. Timing actually specified by ^{t}WR plus ^{t}RP; clock(s) specified as a reference only at minimum cycle rate.
16. Timing actually specified by ^{t}WR.
17. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
18. The I_{DD} current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
19. Address transitions average one transition every 2 clocks.
20. CLK must be toggled a minimum of two times during this period.
21. Based on ^{t}CK = 7.5ns for -75 and ^{t}CK = 8ns for -8.
22. V_{IH} overshoot: V_{IH} (MAX) = $V_{DD}Q$ + 2V for a pulse width ≤ 3ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = –2V for a pulse width ≤ 3ns.

23. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including ^{t}WR, and PRECHARGE commands). CKE may be used to reduce the data rate.
24. Auto precharge mode only. The precharge timing budget (^{t}RP) begins at 7.5ns for -75 and 7ns for -8 after the first clock delay, after the last WRITE is executed. For auto precharge mode, at least one clock cycle is required during ^{t}WR.
25. CKE is HIGH during REFRESH command period ^{t}RFC (MIN) else CKE is LOW.
26. Measurement is taken 500ms after entering into this operating mode to allow tester measurement settling time.
27. Values for IDD7 85°C 4 bank, 2 bank, and 1 bank are guaranteed for the entire temperature range. All other IDD7 values are estimated.
28. Deep power-down current is a nominal value at 25°C. This parameter is not tested.

Table 16: Target Normal Output Drive Characteristics (Full-Drive Strength)
The above characteristics are specified under best and worst process variation/conditions

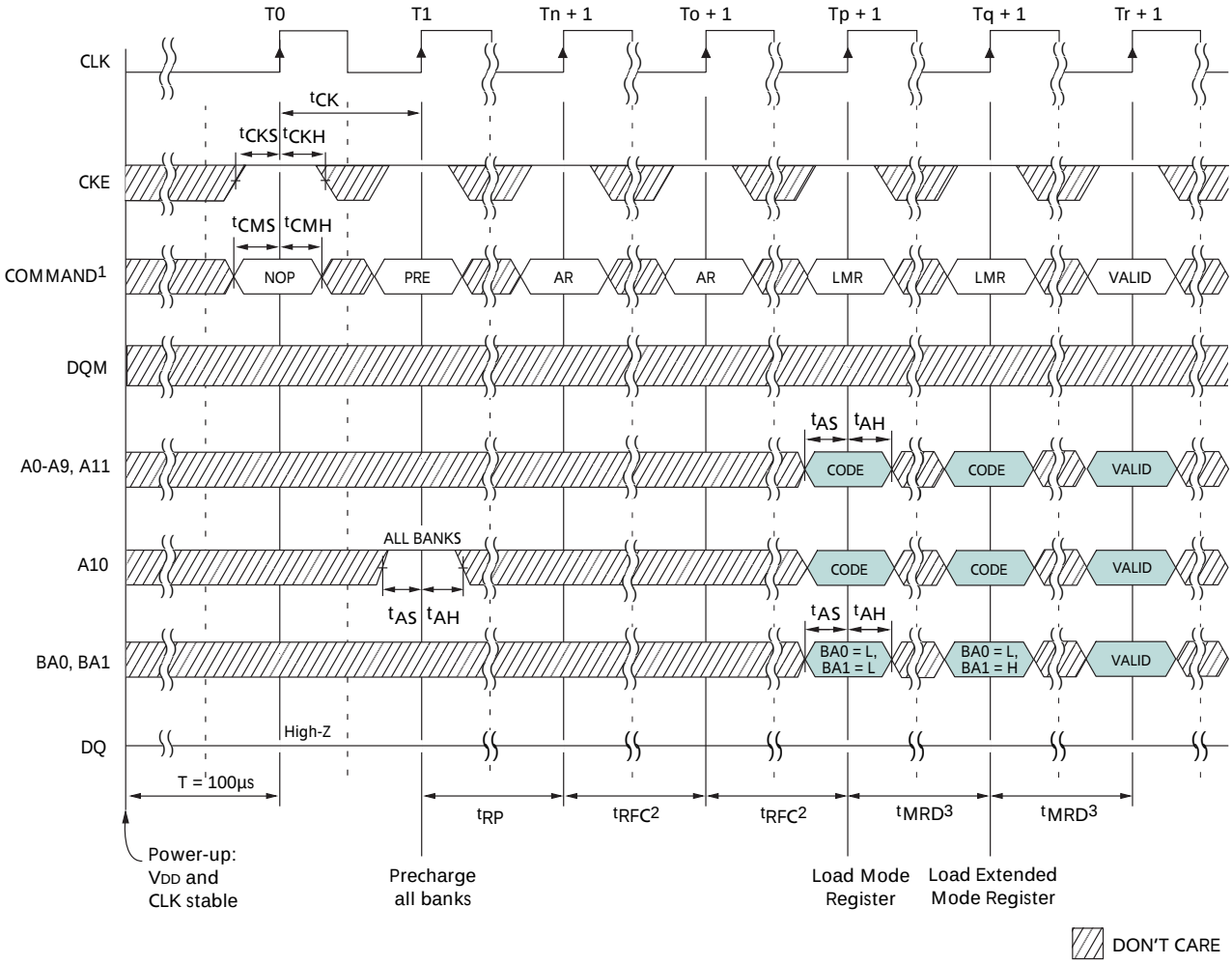
Voltage (V)	Pull-Down Current (mA)		Pull-Up Current (mA)	
	Min	Max	Min	Max
0.00	0.00	0.00	0.00	0.00
0.10	2.80	18.53	–2.80	–18.53
0.20	5.60	26.80	–5.60	–26.80
0.30	8.40	32.80	–8.40	–32.80
0.40	11.20	37.05	–11.20	–37.05
0.50	14.00	40.00	–14.00	–40.00
0.60	16.80	42.50	–16.80	–42.50
0.70	19.60	44.57	–19.60	–44.57
0.80	22.40	46.50	–22.40	–46.50
0.85	23.80	47.48	–23.80	–47.48
0.90	23.80	48.50	–23.80	–48.50
0.95	23.80	49.40	–23.80	–49.40
1.00	23.80	50.05	–23.80	–50.05
1.10	23.80	51.35	–23.80	–51.35
1.20	23.80	52.65	–23.80	–52.65
1.30	23.80	53.95	–23.80	–53.95
1.40	23.80	55.25	–23.80	–55.25
1.50	23.80	56.55	–23.80	–56.55
1.60	23.80	57.85	–23.80	–57.85
1.70	23.80	59.15	–23.80	–59.15
1.80	–	60.45	–	–60.45
1.90	–	61.75	–	–61.75

Table 17: Target Reduced Output Drive Characteristics (One-Half Drive Strength)
The above characteristics are specified under best and worst process variation/conditions

Voltage (V)	Pull-Down Current (mA)		Pull-Up Current (mA)	
	Min	Max	Min	Max
0.00	0.00	0.00	0.00	0.00
0.10	1.27	8.42	–1.27	–8.42
0.20	2.55	12.30	–2.55	–12.30
0.30	3.82	14.95	–3.82	–14.95
0.40	5.09	16.84	–5.09	–16.84
0.50	6.36	18.20	–6.36	–18.20
0.60	7.64	19.30	–7.64	–19.30
0.70	8.91	20.30	–8.91	–20.30
0.80	10.16	21.20	–10.16	–21.20
0.85	10.80	21.60	–10.80	–21.60
0.90	10.80	22.00	–10.80	–22.00
0.95	10.80	22.45	–10.80	–22.45
1.00	10.80	22.73	–10.80	–22.73
1.10	10.80	23.21	–10.80	–23.21
1.20	10.80	23.67	–10.80	–23.67
1.30	10.80	24.14	–10.80	–24.14
1.40	10.80	24.61	–10.80	–24.61
1.50	10.80	25.08	–10.80	–25.08
1.60	10.80	25.54	–10.80	–25.54
1.70	10.80	26.01	–10.80	–26.01
1.80	–	26.48	–	–26.48
1.90	–	26.95	–	–26.95

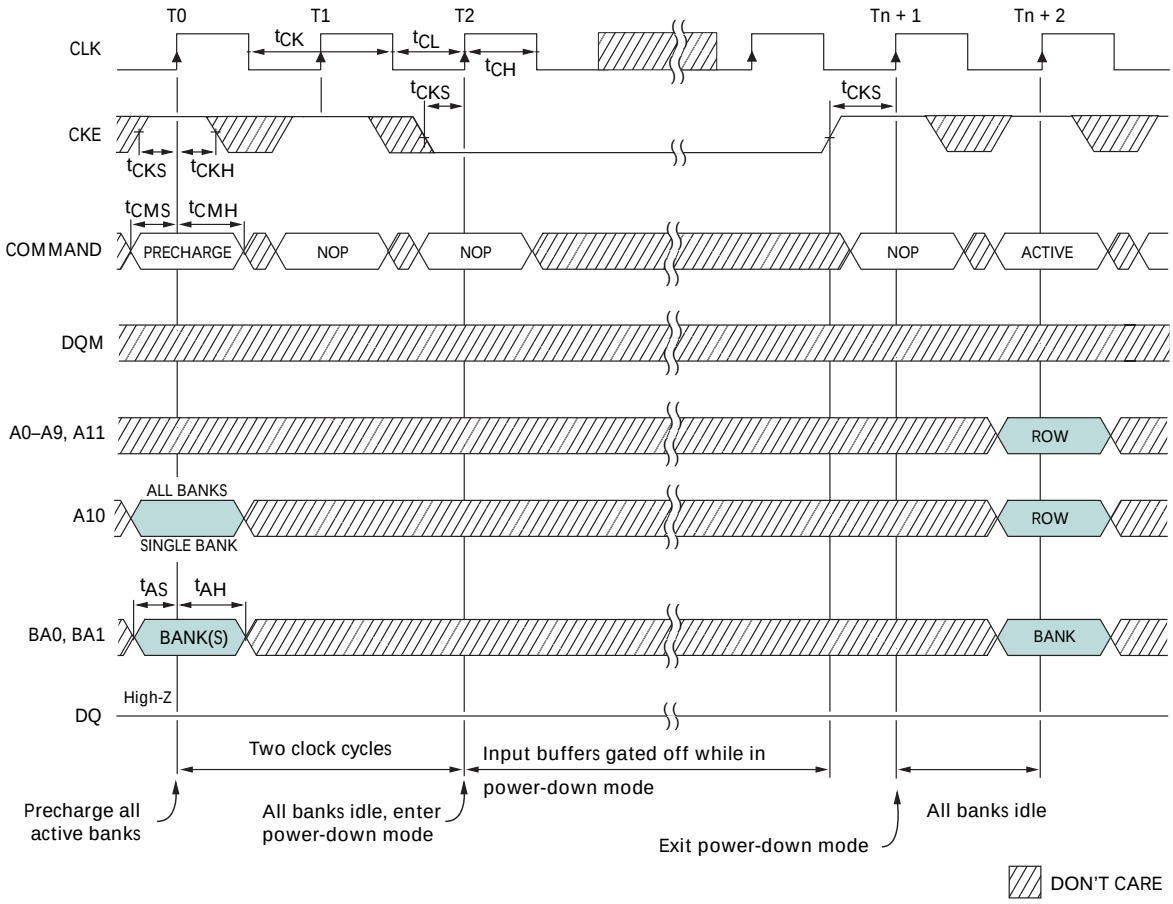
Timing Diagrams

Figure 32: Initialize and Load Mode Registers



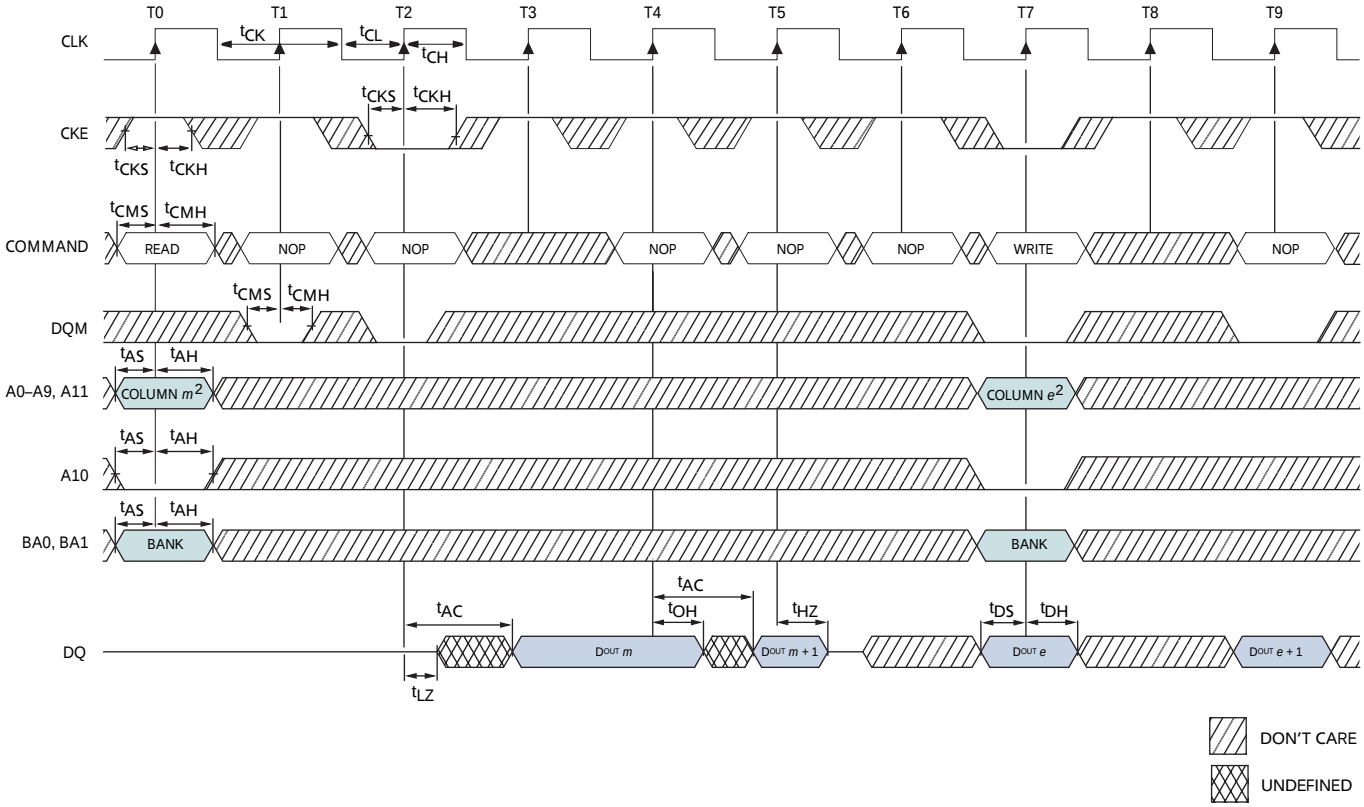
Notes:
1. PRE = PRECHARGE command, AR = AUTO REFRESH command, LMR = LOAD MODE REGISTER command.
2. Only NOPs or COMMAND INHIBITs may be issued during ^{t}RFC time.
3. At least one NOP or COMMAND INHIBIT is required during ^{t}MRD time.

Figure 33: Power-Down Mode



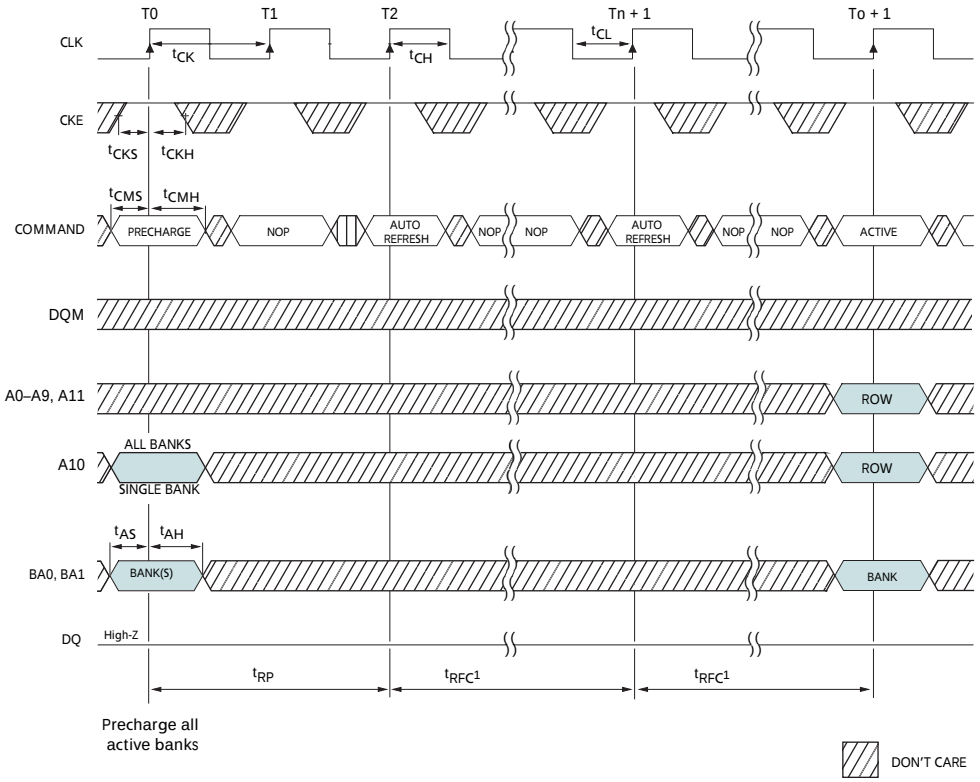
Notes: 1. Violating refresh requirements during power-down may result in a loss of data.

Figure 34: Clock Suspend Mode



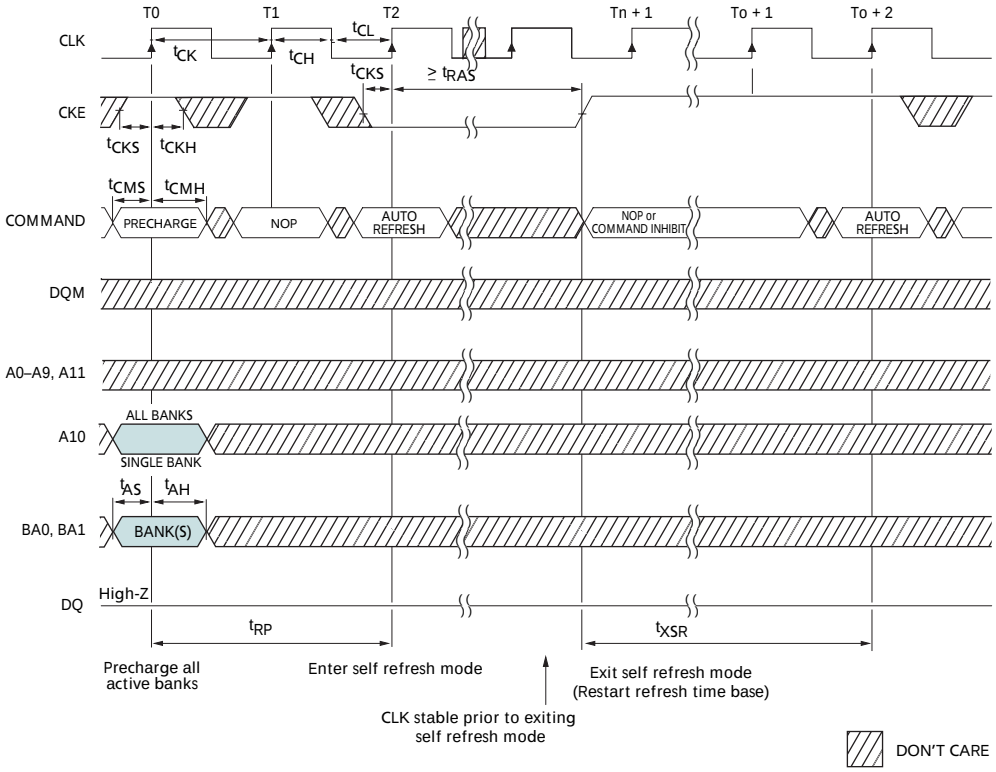
Notes: 1. For this example, BL = 2, CL = 3, and auto precharge is disabled.
2. A9 and A11 are "Don't Care."

Figure 35: Auto Refresh Mode



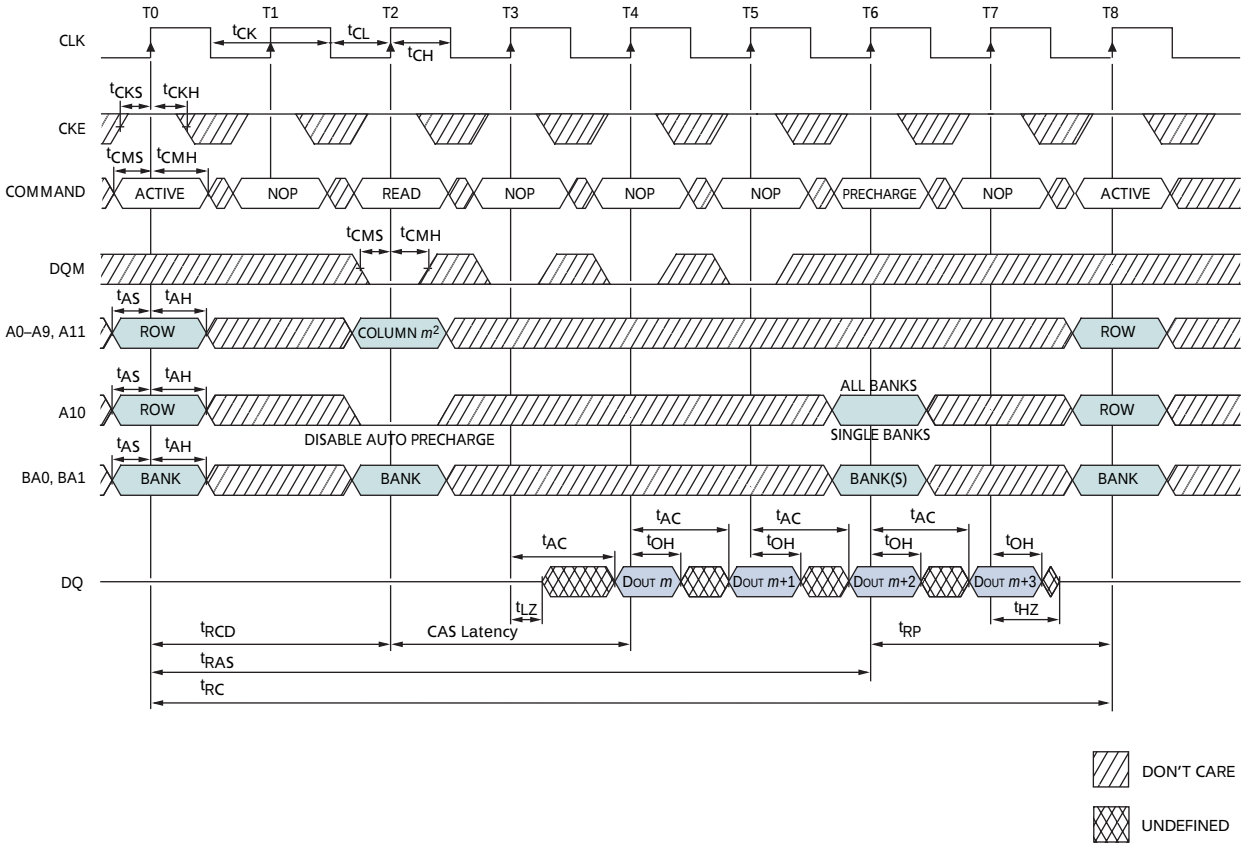
Notes: 1. Each AUTO REFRESH command performs a REFRESH cycle. Back-to-back commands are not required. ^{t}RFC must not be interrupted by any executable command; COMMAND INHIBIT or NOP must be applied on each positive edge during ^{t}RFC.

Figure 36: Self Refresh Mode



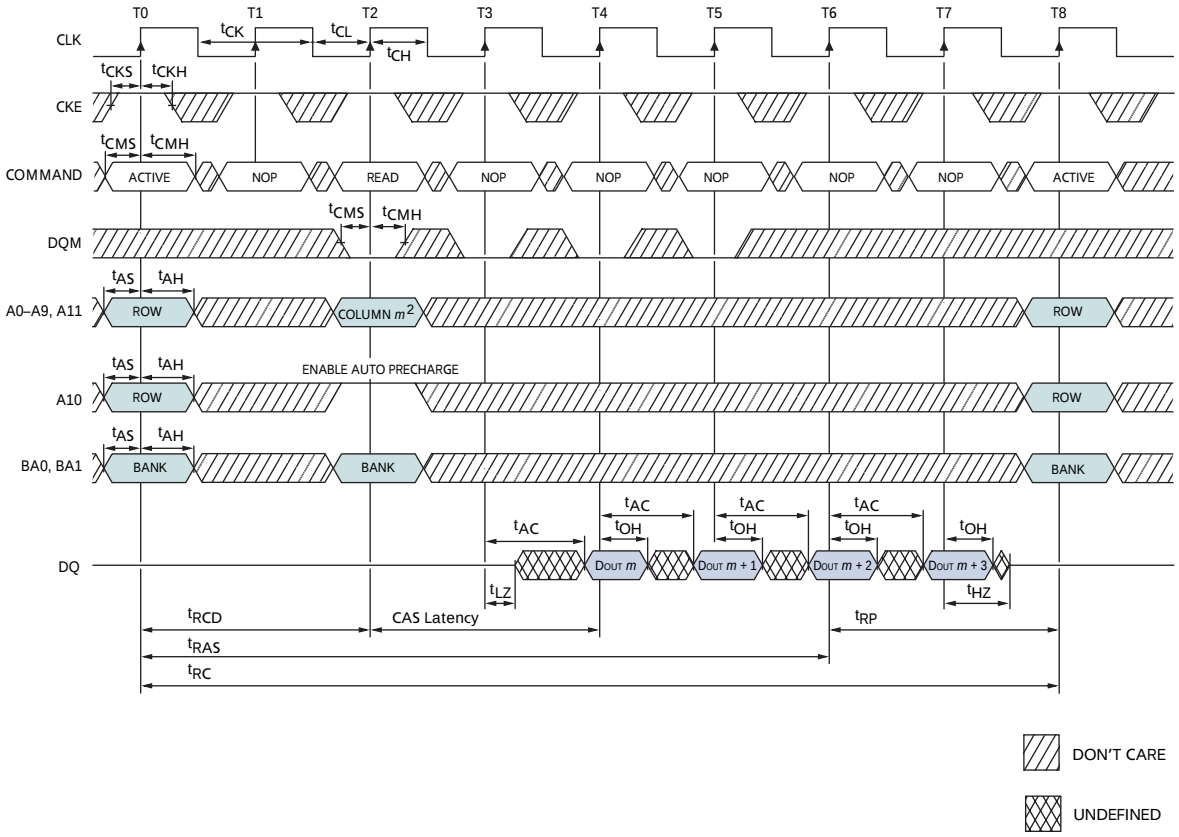
Notes: 1. ^{t}XSR requires a minimum of two clocks regardless of frequency or timing.

Figure 37: READ – Without Auto Precharge



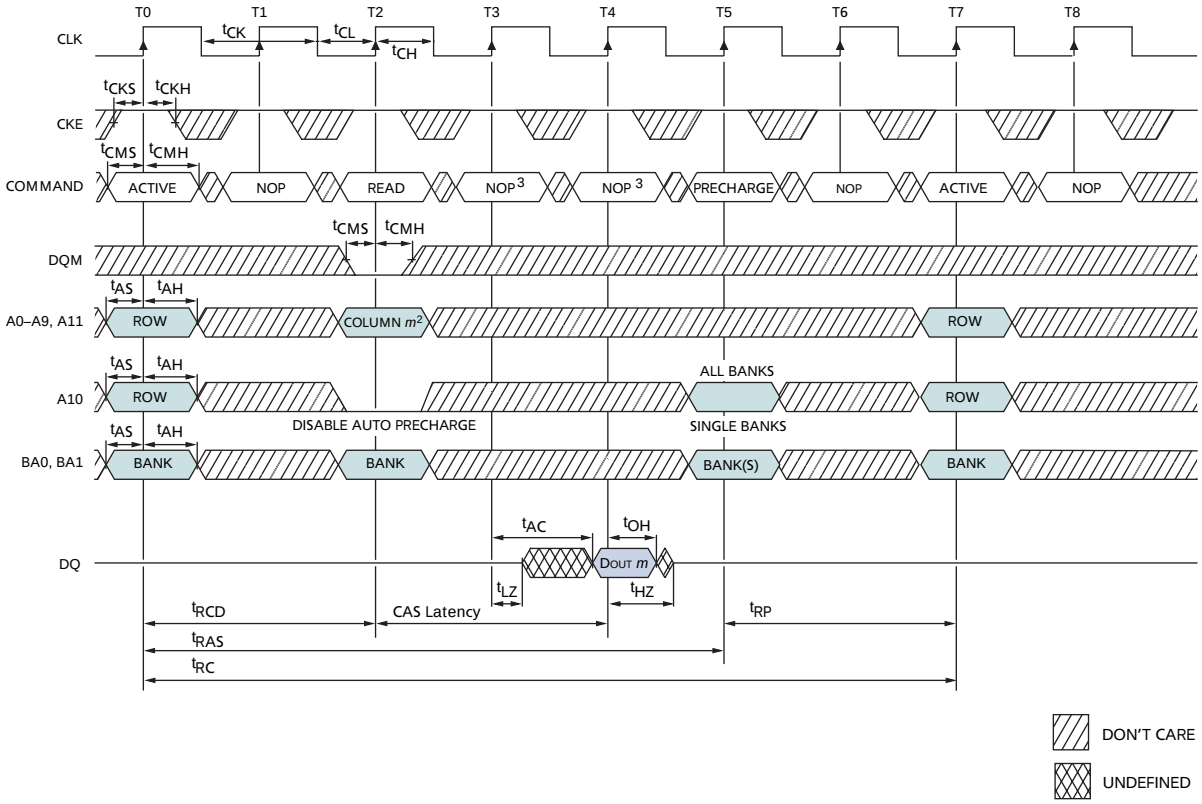
Notes: 1. For this example, BL = 4, CL = 2, and the READ burst is followed by a "manual" PRECHARGE.
2. A9 and A11 are "Don't Care."

Figure 38: READ – With Auto Precharge



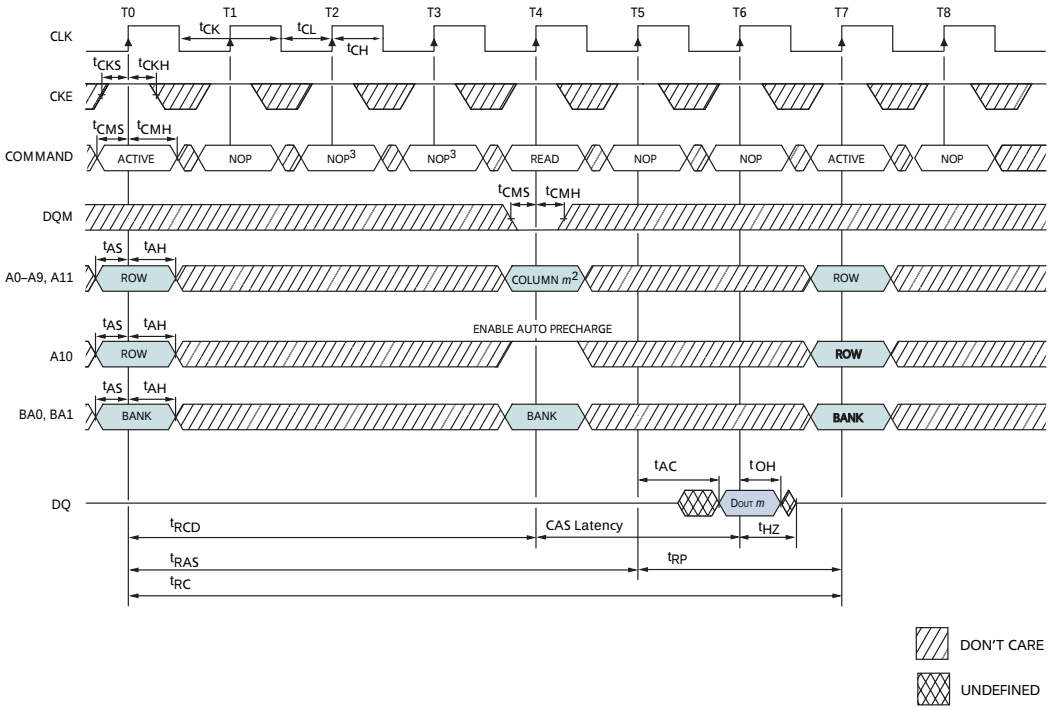
Notes: 1. For this example, BL = 4 and CL = 2.
2. A9 and A11 are "Don't Care."

Figure 39: Single READ – Without Auto Precharge



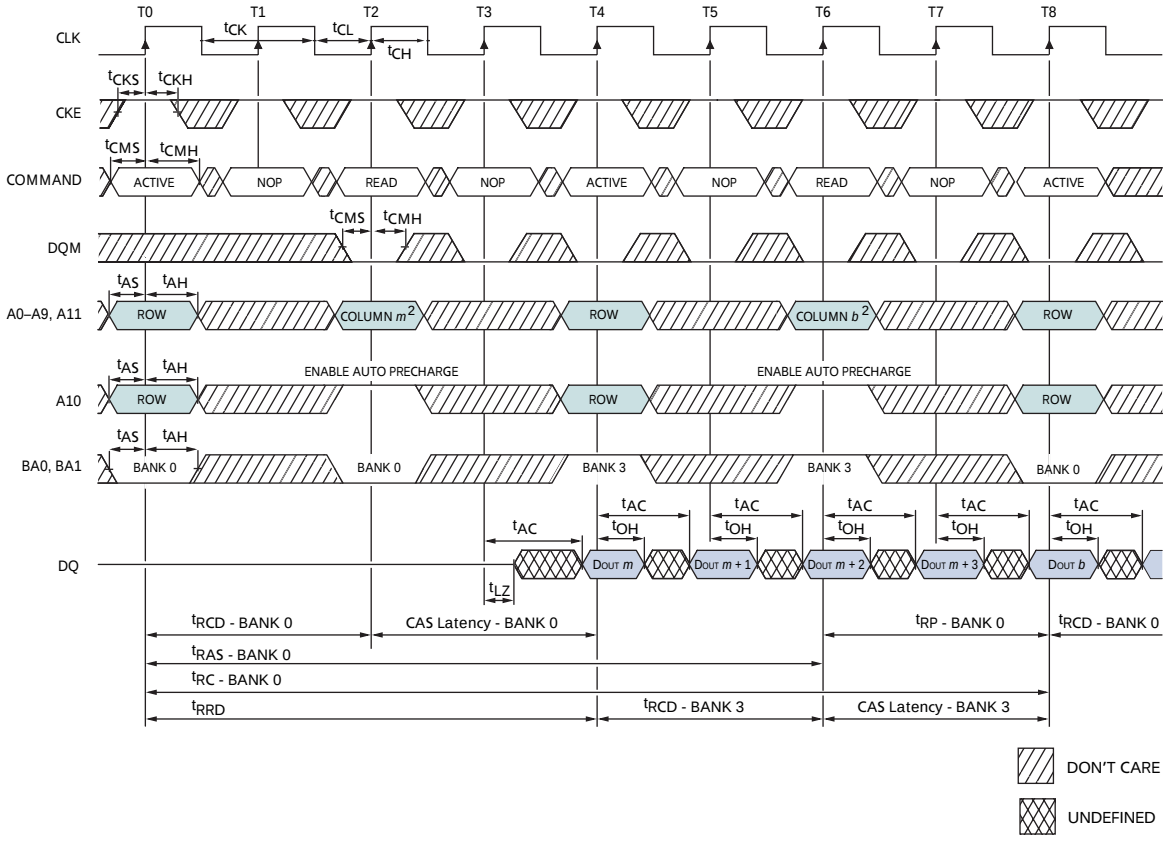
Notes:
1. For this example, BL = 4, CL = 2, and the READ burst is followed by a "manual" PRECHARGE.
2. A9 and A11 are "Don't Care."
3. PRECHARGE command not allowed or ^{t}RAS would be violated.

Figure 40: Single READ – With Auto Precharge



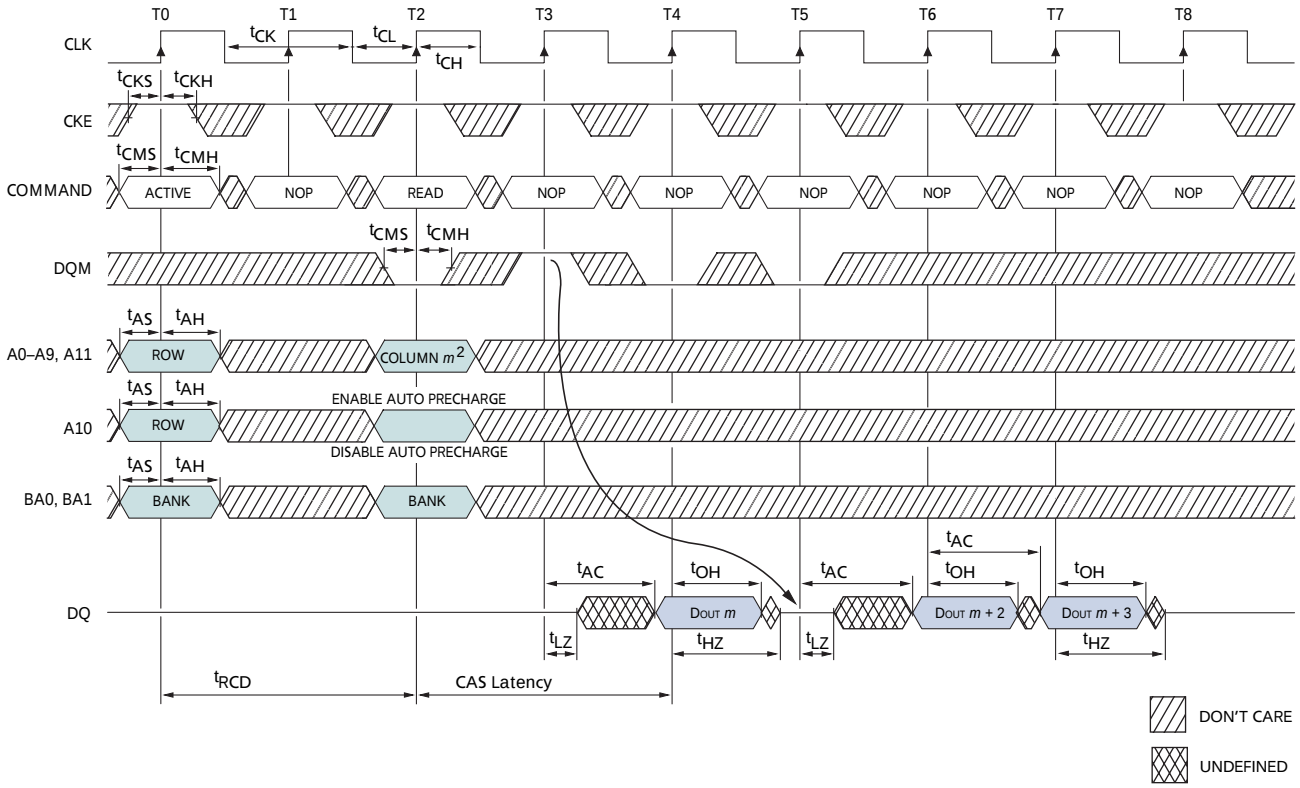
Notes:
1. For this example, BL = 4, CL = 2, and the READ burst is followed by a "manual" PRECHARGE.
2. A9 and A11 are "Don't Care."
3. PRECHARGE command not allowed or ^{t}RAS would be violated.

Figure 41: Alternating Bank Read Accesses



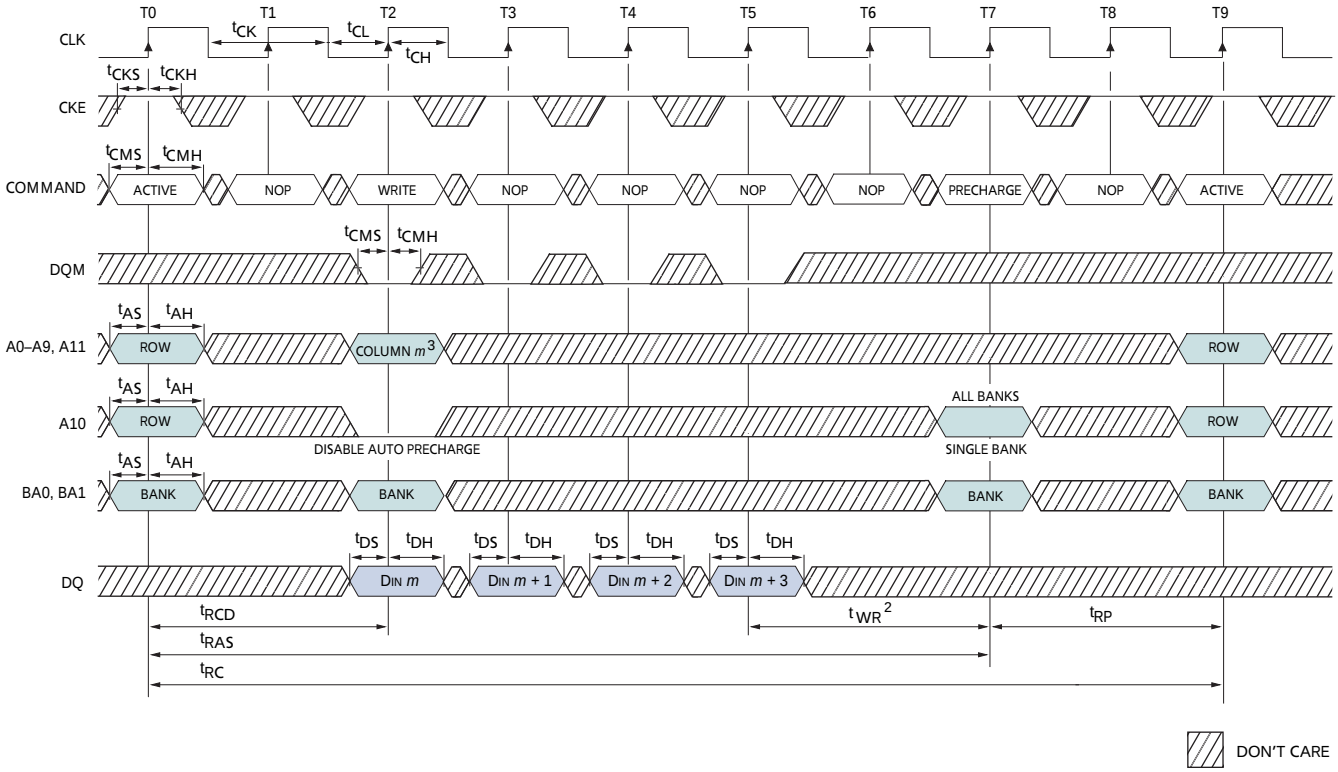
Notes: 1. For this example, BL = 4 and CL = 2.
2. A9 and A11 are "Don't Care."

Figure 42: READ – DQM Operation



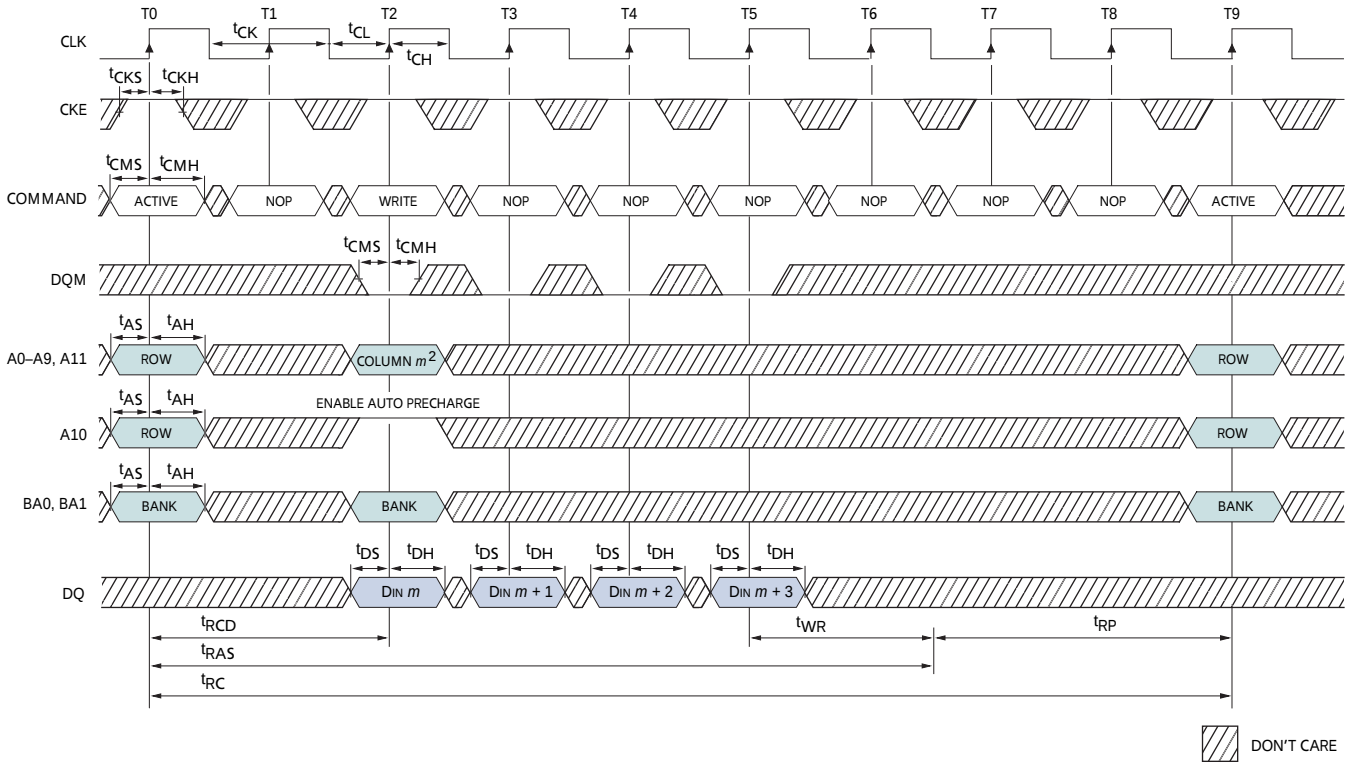
Notes: 1. For this example, CL = 2.
2. A9 and A11 are "Don't Care."

Figure 43: WRITE – Without Auto Precharge



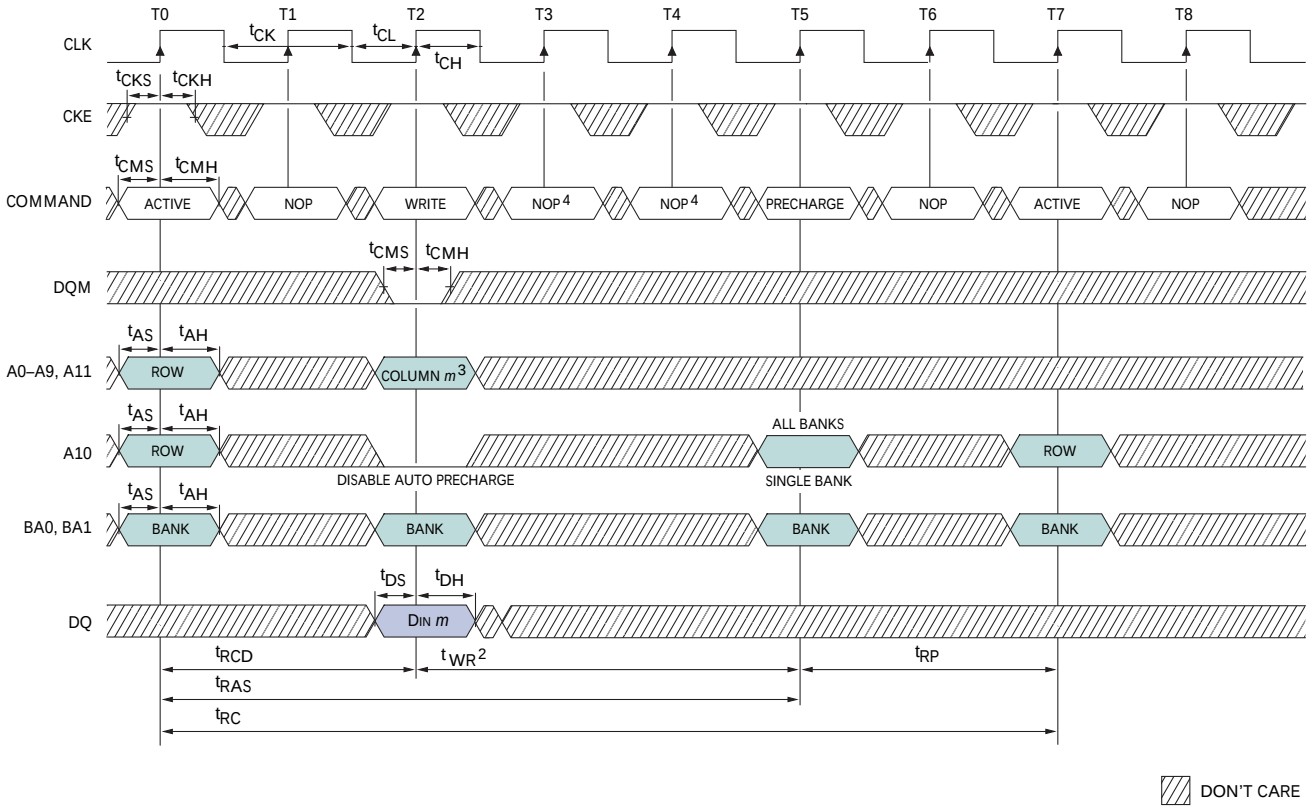
Notes:
1. For this example, BL = 4, and the WRITE burst is followed by a "manual" PRECHARGE.
2. 15ns is required between <DIN *m* + 3> and the PRECHARGE command, regardless of frequency.
3. A9 and A11 are "Don't Care."

Figure 44: WRITE – With Auto Precharge



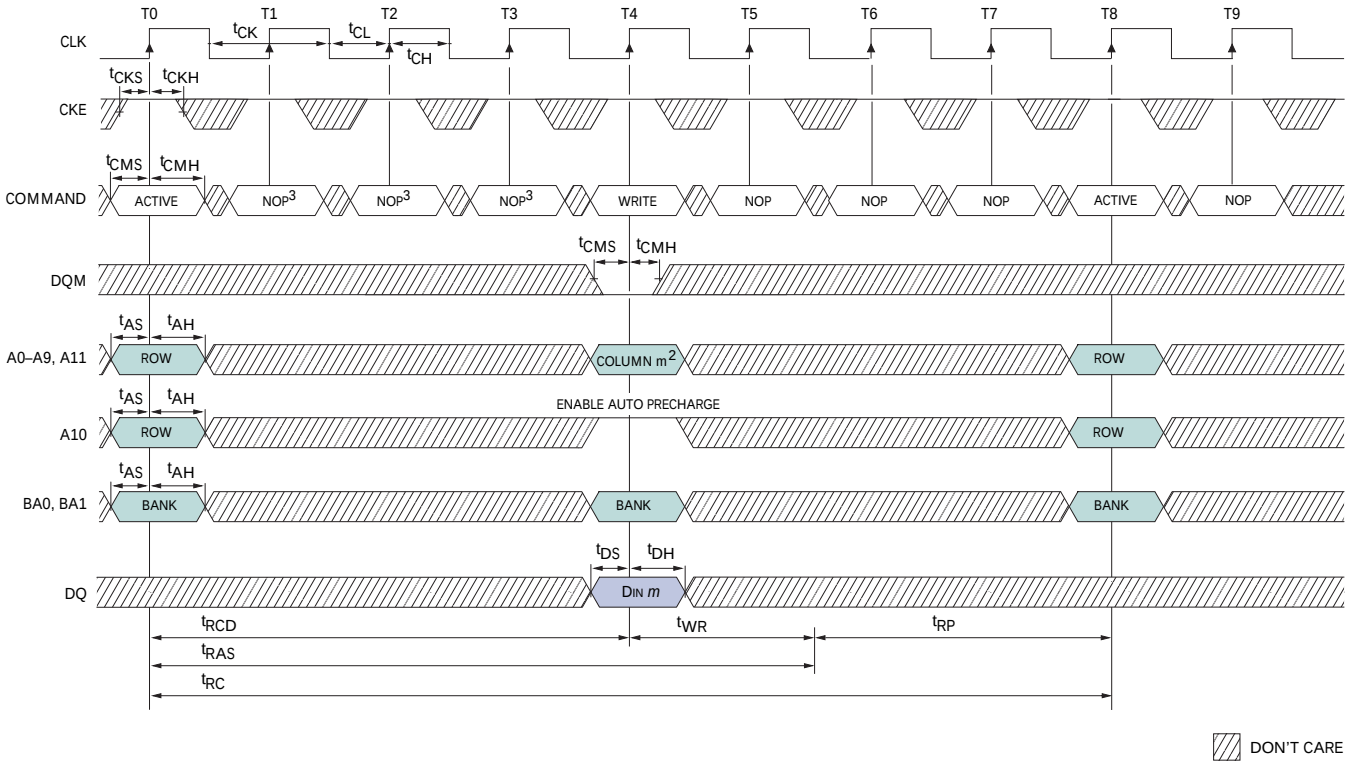
Notes: 1. For this example, BL = 4.
2. A9 and A11 are "Don't Care."

Figure 45: Single WRITE – Without Auto Precharge



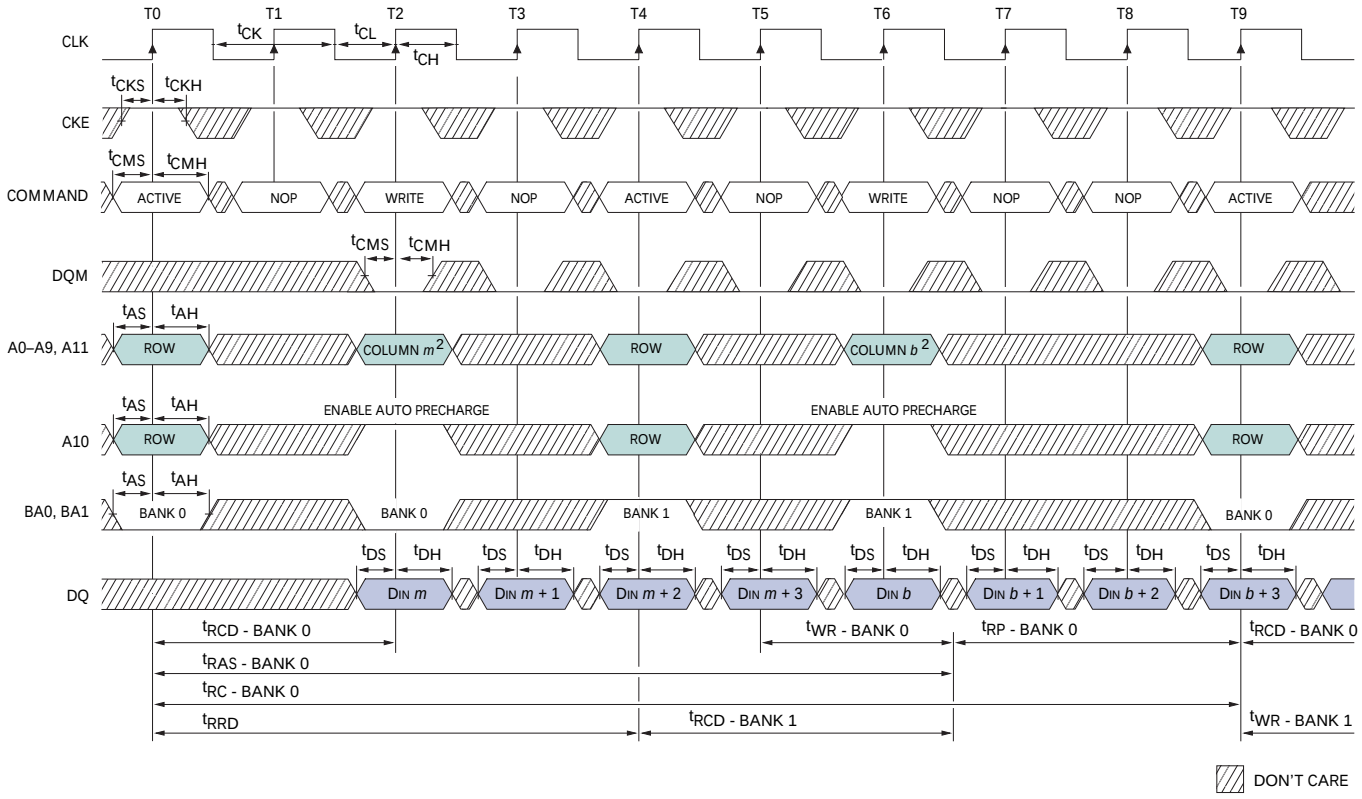
Notes:
1. For this example, BL = 1, and the WRITE burst is followed by a "manual" PRECHARGE.
2. 15ns is required between <DIN *m*> and the PRECHARGE command, regardless of frequency.
3. A9 and A11 are "Don't Care."
4. PRECHARGE command not allowed or ^{t}RAS would be violated.

Figure 46: Single WRITE – With Auto Precharge



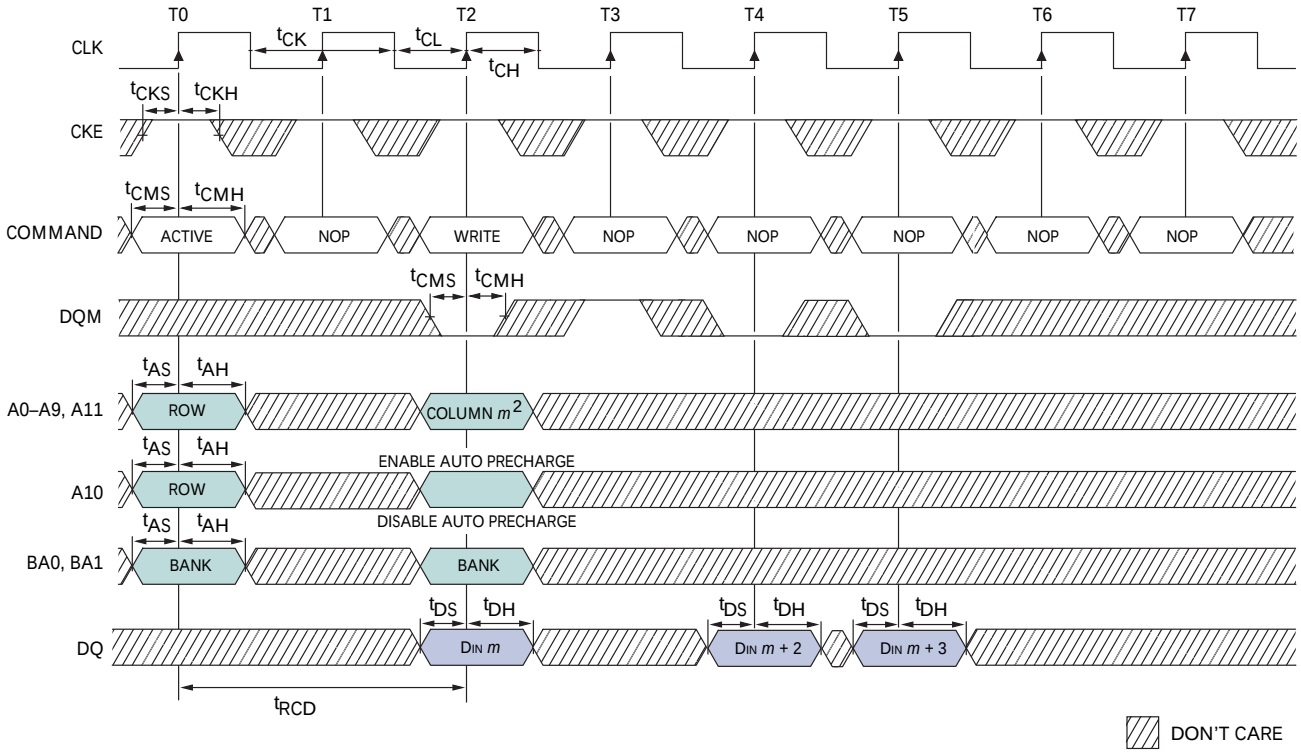
Notes:
1. For this example, BL = 1, and the WRITE burst is followed by a "manual" PRECHARGE.
2. 15ns is required between <DIN *m*> and the PRECHARGE command, regardless of frequency.
3. A9 and A11 are "Don't Care."
4. WRITE command not allowed or ^{t}RAS would be violated.

Figure 47: Alternating Bank Write Accesses



Notes: 1. For this example, BL = 4.
2. A9 and A11 are "Don't Care."

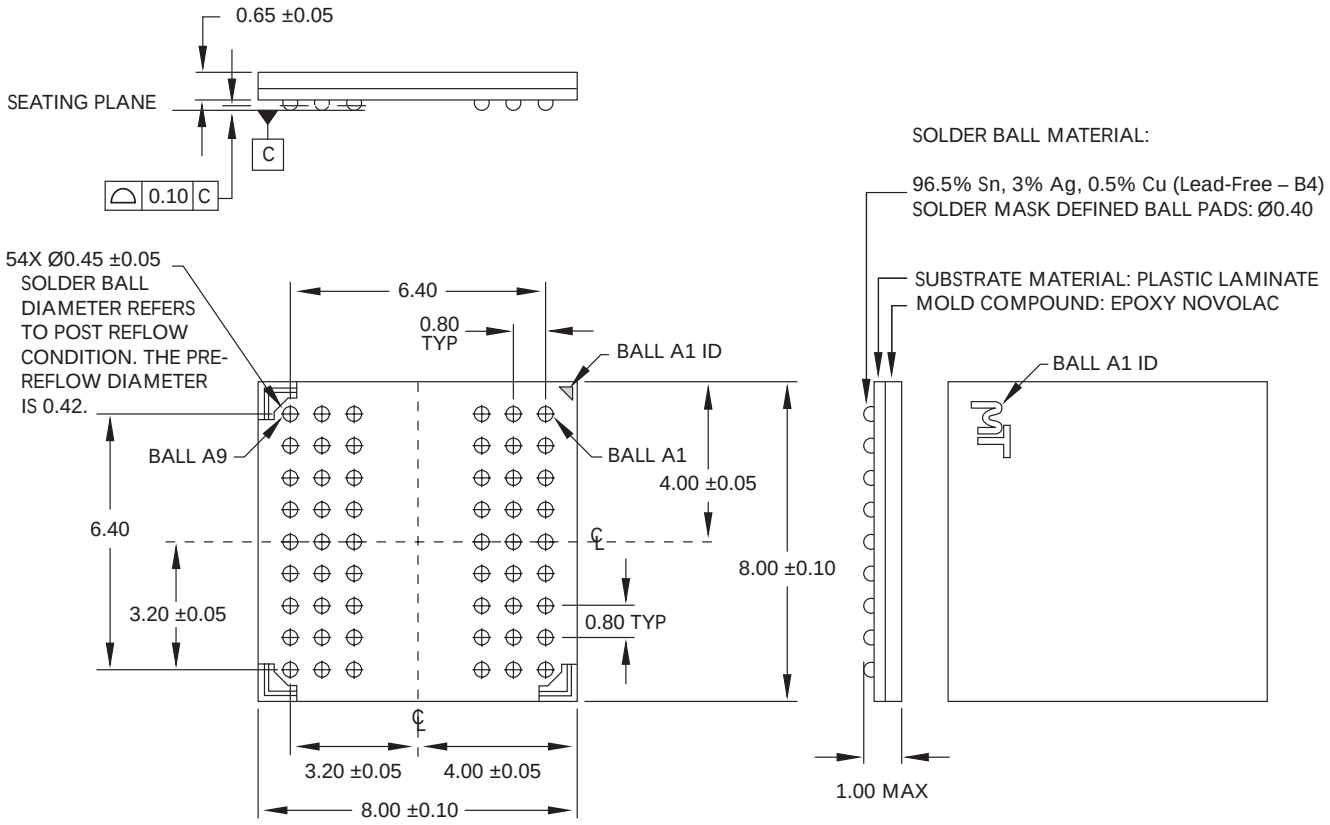
Figure 48: Write – DQM Operation



Notes: 1. For this example, BL = 4.
2. A9 and A11 are "Don't Care."

Package Dimensions

Figure 49: 54-Ball VFBGA (8mm x 8mm)



Notes: 1. All dimensions are in millimeters.

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