

Mobile SDRAM

MT48LC16M32L2 – 4 Meg x 32 x 4 Banks

MT48V16M32L2 – 4 Meg x 32 x 4 Banks

MT48H16M32L2 – 4 Meg x 32 x 4 Banks

Features

- Low voltage power supply
- Partial array self refresh power-saving mode
- Temperature compensated self refresh (TCSR)
- Deep power-down mode
- Programmable output drive strength
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto precharge, includes concurrent auto precharge, and auto refresh modes
- Self refresh mode; standard and low power
- 64ms, 8,192-cycle refresh
- LVTTTL-compatible inputs and outputs
- Operating temperature range
- Industrial (-40°C to +85°C)
- Supports CAS latency of 1, 2, 3

Options

- VDD/VDDQ
3.3V/3.3V LC
- 2.5V/2.5V V
- 1.8V/1.8V H
- Configuration
16M32 stacked die L2
- Package/ballout
Plastic package 90-ball FBGA F5
(8mm x 13mm) (standard)
- Plastic package 90-ball FBGA B5
(8mm x 13mm) (lead-free)
- Timing (cycle time)
8ns at CL3 (125 MHz) -8
10ns at CL3 (100 MHz) -10
- Temperature
Commercial (0°C to +70°C) No Marking
Industrial (-40°C to +85°C) IT

Marking

Addendum Changes

The standard 256Mb SDRAM Mobile x32 data sheets should be referenced for a complete description of SDRAM functionality and operating modes. This addendum data sheet will concentrate on the key differences required to support the enhanced options of the TwinDie configuration.

The Micron 256Mb Mobile X32 data sheet provides full specifications and functionality unless specified herein.

Table 1: Key Timing Parameters

Speed Grade	Clock Frequency	Access Time at CL = 3	Access Time at CL = 2
-8	125 MHz	7.5ns	8.5ns
-10	100 MHz	7.5ns	8.5ns

Table 2: Configuration

Architecture	16 Meg x 32
Configuration	4 Meg x 32 x 4 banks
Refresh Count	8K
Row Addressing	8K (A0–A12)
Bank Addressing	4 (BA0, BA1)
Column Addressing	512 (A0–A8)

General Description

The 512Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured by stacking two 256Mb, 8 Meg x 32 devices. Each of these 256Mb devices is configured as a quad bank DRAM with a synchronous interface. They are organized with 32 DQs with 4 banks of 67,108,864 bits, comprising of 8,192 rows by 512 columns by 32 bits wide.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A12 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access. The SDRAM provides for programmable READ or WRITE burst lengths of 1, 2, 4, or 8 locations, or the full page, with a burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The 512Mb SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2n rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless, high-speed, random-access operation.

The 512Mb SDRAM is designed to operate in 3.3V, 2.5V, and 1.8V memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTTL-compatible.

SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

Prior to normal operation, the SDRAM must be initialized. The following sections provide detailed information covering die initialization, register definition, command descriptions, and device operation on a per die basis unless otherwise noted.

This addendum documents any variances for the 512Mb: x32 Mobile SDRAM from the 256Mb: x32 Mobile SDRAM specification. Please refer to the 256Mb: x32 Mobile SDRAM data sheet on Micron's Web site for additional details on the part functionality.

Commands

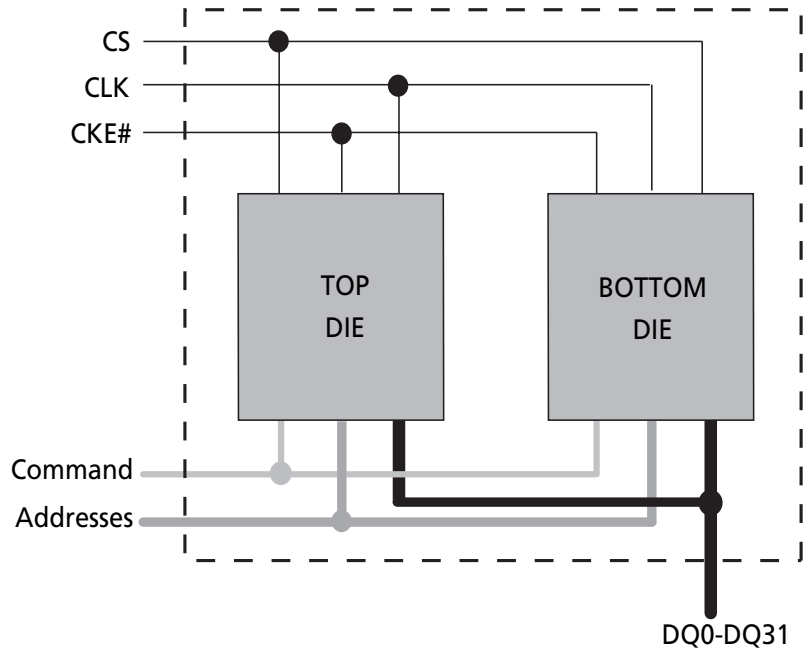
AUTO REFRESH

AUTO REFRESH is used during normal operation of the SDRAM and is analogous to CAS#-BEFORE-RAS# (CBR) REFRESH in conventional DRAMs. This command is non-persistent, so it must be issued each time a refresh is required. All active banks must be PRECHARGED prior to issuing a AUTO REFRESH command. The AUTO REFRESH command should not be issued until the minimum ^tRP has been met after the PRECHARGE command as shown in the operations section.

The addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an AUTO REFRESH command. The 512Mb TwinDie™ Mobile SDRAM requires 8,192 AUTO REFRESH cycles every 64ms (^tREF). Providing a distributed

AUTO REFRESH command every $7.81\mu\text{s}$ will meet the refresh requirement and ensure that each row is refreshed. Alternatively, 8,192 AUTO REFRESH commands can be issued in a burst at the minimum cycle rate (t^{RC}), once every 64ms.

Figure 1: Functional Block Diagram



Ball Assignment

Figure 2: 90-Ball FBGA Assignment

	1	2	3	4	5	6	7	8	9
A	DQ26	DQ24	Vss				VDD	DQ23	DQ21
B	DQ28	VDDQ	VssQ				VDDQ	VssQ	DQ19
C	VssQ	DQ27	DQ25				DQ22	DQ20	VDDQ
D	VssQ	DQ29	DQ30				DQ17	DQ18	VDDQ
E	VDDQ	DQ31	NC				NC	DQ16	VssQ
F	Vss	DQM3	A3				A2	DQM2	VDD
G	A4	A5	A6				A10	A0	A1
H	A7	A8	A12				NC	BA1	A11
J	CLK	CKE	A9				BA0	CS#	RAS#
K	DQM1	NC	NC				CAS#	WE#	DQM0
L	VDDQ	DQ8	Vss				VDD	DQ7	VssQ
M	VssQ	DQ10	DQ9				DQ6	DQ5	VDDQ
N	VssQ	DQ12	DQ14				DQ1	DQ3	VDDQ
P	DQ11	VDDQ	VssQ				VDDQ	VssQ	DQ4
R	DQ13	DQ15	Vss				VDD	DQ0	DQ2

Ball and Array

Electrical Specifications

Table 3: DC Electrical Characteristics and Operating Conditions (LC version)
 $V_{DD}/V_{DDQ} = +3.3V \pm 0.3V$

Notes: 1, 5, 6; please refer to the 256Mb: x32 Mobile SDRAM data sheet for all notes.

Parameter/Condition	Symbol	MIN	MAX	Units	Notes
Supply Voltage	V_{DD}/V_{DDQ}	3	3.6	V	
Input High Voltage: Logic 1; All inputs	V_{IH}	$0.8 \times V_{DDQ}$	$V_{DD} + 0.3$	V	22
Input Low Voltage: Logic 0; All inputs	V_{IL}	-0.3	0.3	V	22
Input Leakage Current: Any input $0V \leq V_{IN} \leq V_{DD}$ (All other balls not under test = 0V)	I_{II}	-5	5	μA	
Output Leakage Current: DQs are disabled; $0V \leq V_{OUT} \leq V_{DDQ}$	I_{OZ}	-5	5	μA	
Output Levels: Output High Voltage ($I_{OUT} = -4mA$)	V_{OH}	$V_{DDQ} - 0.2$	-	V	
Output Low Voltage ($I_{OUT} = 4mA$)	V_{OL}	-	0.2	V	

Table 4: DC Electrical Characteristics and Operating Conditions (V version)
 $V_{DD} = +2.5V \pm 0.2V$ $V_{DDQ} = +2.5V \pm 0.2V$ or $V_{DDQ} = +1.8V \pm 0.15V$

Notes: 1, 5, 6; please refer to the 256Mb: x32 Mobile SDRAM data sheet for all notes.

Parameter/Condition	Symbol	MIN	MAX	Units	Notes
Supply Voltage	V_{DD}/V_{DDQ}	2.3	2.7	V	
Input High Voltage: Logic 1; All inputs	V_{IH}	$0.8 \times V_{DDQ}$	$V_{DDQ} + 0.3$	V	22
Input Low Voltage: Logic 0; All inputs	V_{IL}	-0.3	0.3	V	22
Input Leakage Current: Any input $0V \leq V_{IN} \leq V_{DD}$ (All other balls not under test = 0V)	I_{II}	-3.0	3.0	μA	
Output Leakage Current: DQs are disabled; $0V \leq V_{OUT} \leq V_{DDQ}$	I_{OZ}	-3.0	3.0	μA	
Output Levels: Output High Voltage ($I_{OUT} = -4mA$)	V_{OH}	$0.9 \times V_{DDQ}$	-	V	
Output Low Voltage ($I_{OUT} = 4mA$)	V_{OL}	-	0.2	V	

Table 5: DC Electrical Characteristics and Operating Conditions (H version)

VDD = +1.8V ±0.1V VDDQ = +1.8V ±0.1V

Notes: 1, 5, 6; please refer to the 256Mb: x32 Mobile SDRAM data sheet for all notes.

Parameter/Condition	Symbol	MIN	MAX	Units	Notes
Supply Voltage	VDD/VDDQ	1.7	1.9	V	
Input High Voltage: Logic 1; All inputs	V _{IH}	0.8 x VDDQ	VDDQ + 0.3	V	22
Input Low Voltage: Logic 0; All inputs	V _{IL}	-0.3	0.3	V	22
Input Leakage Current: Any input 0V ≤ V _{IN} ≤ VDD (All other balls not under test = 0V)	I _I	-1.0	1.0	μA	
Output Leakage Current: DQs are disabled; 0V ≤ V _{OUT} ≤ VDDQ	I _{oz}	-1.5	1.55	μA	
Output Levels: Output High Voltage (I _{OUT} = -4mA)	V _{OH}	0.9 x VDDQ	–	V	
Output Low Voltage (I _{OUT} = 4mA)	V _{OL}	–	0.2	V	

Table 6: IDD Specifications and Conditions (LC version)

VDD = +3.3V ±0.3V, VDDQ = +3.3V ±0.3V

Notes: 1, 5, 6, 11, 13; please refer to the 256Mb: x32 Mobile SDRAM data sheet for all notes.

Parameter/Condition	Symbol	MAX		Units	Notes	
		-8	-10			
Operating Current: Active Mode; Burst = 2; READ or WRITE; t _{RC} = t _{RC} (MIN)	I _{DD1}	210	185	mA	3, 18, 19, 28	
Standby Current: Power-Down Mode; All banks idle; CKE = LOW	I _{DD2N}	800	800	μA	32	
Standby Current: Power-Down Mode; All banks idle; CKE = HIGH	I _{DD2NS}	60	60	mA		
Standby Current: Active Mode; CKE = HIGH; CS# = HIGH; All banks active after t _{RCD} met; No accesses in progress	I _{DD3NS}	80	80	mA	3, 12, 19, 28	
Standby Current: Active Mode; CKE = LOW; CS# = HIGH; All banks active; No accesses in progress	I _{DD3N}	60	60	mA		
Operating Current: Burst Mode; Continuous burst; READ or WRITE; All banks active, half DQs toggling every cycle.	I _{DD4}	165	140	mA	3, 18, 19, 28	
Auto Refresh Current CKE = HIGH; CS# = HIGH	t _{RFC} = t _{RFC} (MIN)	I _{DD5}	300	250	mA	3, 12, 18, 19, 28, 29
	t _{RFC} = 7.8μs	I _{DD6}	5.0	5.0	mA	
Deep power down	I _{ZZ}	20	20	μA		



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Table 7: IDD Specifications and Conditions (V version)

VDD = +2.5 ±0.2V, VDDQ = +2.5 ±0.2V

Notes: 1, 5, 6, 11, 13; please refer to the 256Mb: x32 Mobile SDRAM data sheet for all notes.

Parameter/Condition	Symbol	MAX		Units	Notes	
		-8	-10			
Operating Current: Active Mode; Burst = 2; READ or WRITE; t _{RC} = t _{RC} (MIN)	IDD1	210	185	mA	3, 18, 19, 28	
Standby Current: Power-Down Mode; All banks idle; CKE = LOW	IDD2N	800	800	μA	32	
Standby Current: Power-Down Mode; All banks idle; CKE = HIGH	IDD2NS	60	60	mA		
Standby Current: Active Mode; CKE = HIGH; CS# = HIGH; All banks active after t _{RCD} met; No accesses in progress	IDD3NS	80	80	mA	3, 12, 19, 28	
Standby Current: Active Mode; CKE = LOW; CS# = HIGH; All banks active; No accesses in progress	IDD3N	60	60	mA		
Operating Current: Burst Mode; Continuous burst; READ or WRITE; All banks active, half DQs toggling every cycle.	IDD4	165	140	mA	3, 18, 19, 28	
Auto Refresh Current CKE = HIGH; CS# = HIGH	t _{RFC} = t _{RFC} (MIN)	IDD5	300	250	mA	3, 12, 18, 19, 28, 29
	t _{RFC} = 7.8μs	IDD6	5.0	5.0	mA	
Deep power down	I _{ZZ}	20	20	μA		

Table 8: IDD Specifications and Conditions (H version)

VDD = 1.8 ±0.1V, VDDQ = 1.8V ±0.1V

Notes: 1, 5, 6, 11, 13; please refer to the 256Mb: x32 Mobile SDRAM data sheet for all notes.

Parameter/Condition	Symbol	MAX		Units	Notes	
		-8	-10			
Operating Current: Active Mode; Burst = 2; READ or WRITE; t _{RC} = t _{RC} (MIN)	IDD1	155	130	mA	3, 18, 19, 28	
Standby Current: Power-Down Mode; All banks idle; CKE = LOW	IDD2N	600	600	μA	32	
Standby Current: Power-Down Mode; All banks idle; CKE = HIGH	IDD2NS	40	40	mA		
Standby Current: Active Mode; CKE = HIGH; CS# = HIGH; All banks active after t _{RCD} met; No accesses in progress	IDD3NS	60	60	mA	3, 12, 19, 28	
Standby Current: Active Mode; CKE = LOW; CS# = HIGH; All banks active; No accesses in progress	IDD3N	40	40	mA		
Operating Current: Burst Mode; Continuous burst; READ or WRITE; All banks active, half DQs toggling every cycle.	IDD4	115	95	mA	3, 18, 19, 28	
Auto Refresh Current CKE = HIGH; CS# = HIGH	t _{RFC} = t _{RFC} (MIN)	IDD5	245	205	mA	3, 12, 18, 19, 28, 29
	t _{RFC} = 7.8μs	IDD6	5.0	5.0	mA	
Deep power down	I _{ZZ}	20	20	μA		

Table 9: IDD7 - Self Refresh Current Options

Note: 4; please refer to the 256Mb: x32 Mobile SDRAM data sheet for all notes. Values for IDD7 for 85°C are 100 percent tested. Values for 70°C, 45°C, and 15°C are sampled only.

Temperature Compensated Self Refresh Parameter/Condition	MAX Temperature	VDD = 3.3	VDD = 2.5	VDD = 1.8	Units	Notes
Self Refresh Current: CKE = LOW – 4 Bank Refresh	85°C	1600	1600	1200	μA	4
	70°C	1300	1300	960	μA	4
	45°C	1000	1000	740	μA	4
	15°C	864	864	630	μA	4
Self Refresh Current: CKE = LOW – 2 Bank Refresh	85°C	1200	1200	900	μA	4
	70°C	1025	1025	760	μA	4
	45°C	875	875	640	μA	4
	15°C	800	800	580	μA	4
Self Refresh Current: CKE = LOW – 1 Bank Refresh	85°C	1000	1000	750	μA	4
	70°C	900	900	660	μA	4
	45°C	800	800	590	μA	4
	15°C	760	760	560	μA	4
Self Refresh Current: CKE = LOW – Half Bank Refresh	85°C	900	900	680	μA	4
	70°C	825	825	610	μA	4
	45°C	780	780	566	μA	4
	15°C	750	750	540	μA	4
Self Refresh Current: CKE = LOW – Quarter Bank Refresh	85°C	850	850	640	μA	4
	70°C	800	800	590	μA	4
	45°C	760	760	550	μA	4
	15°C	740	740	536	μA	4

IDD7 Curves

Figure 3: Typical Self Refresh Current vs. Temperature – 3.3V Part

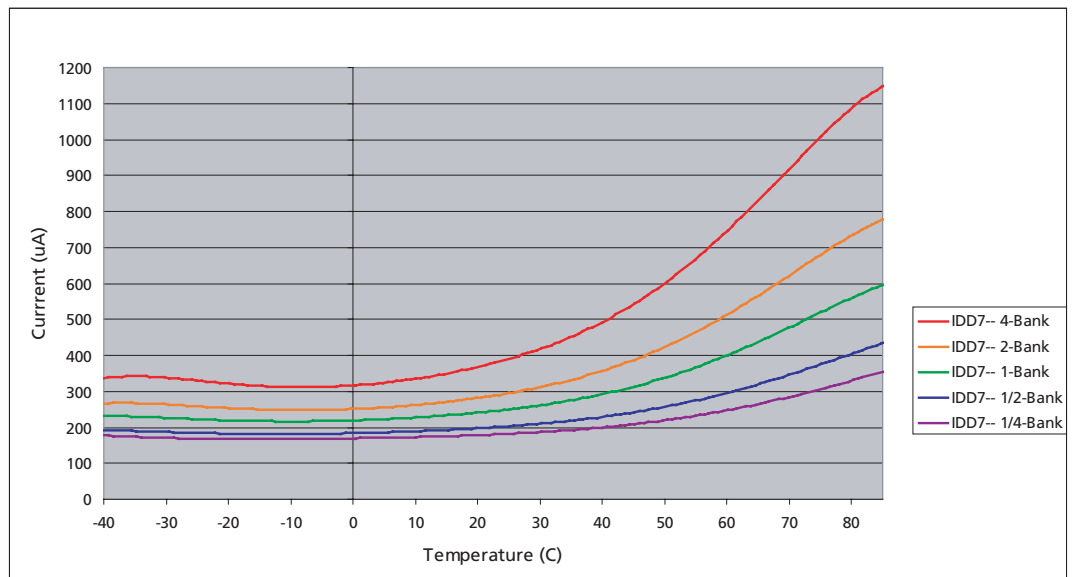


Figure 4: Typical Self Refresh Current vs. Temperature – 2.5V Part

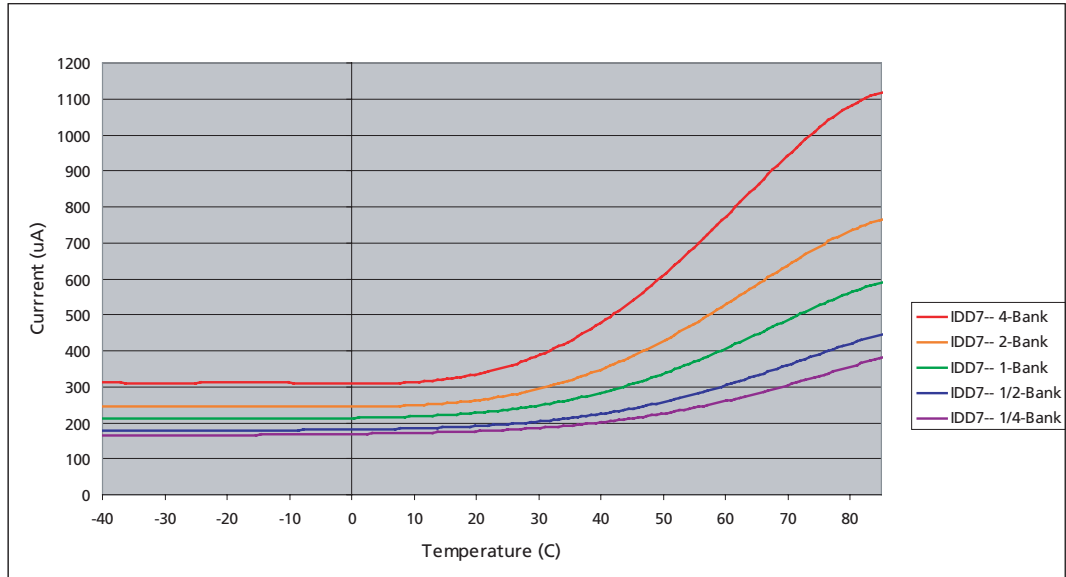


Figure 5: Typical Self Refresh Current vs. Temperature – 1.8V Part

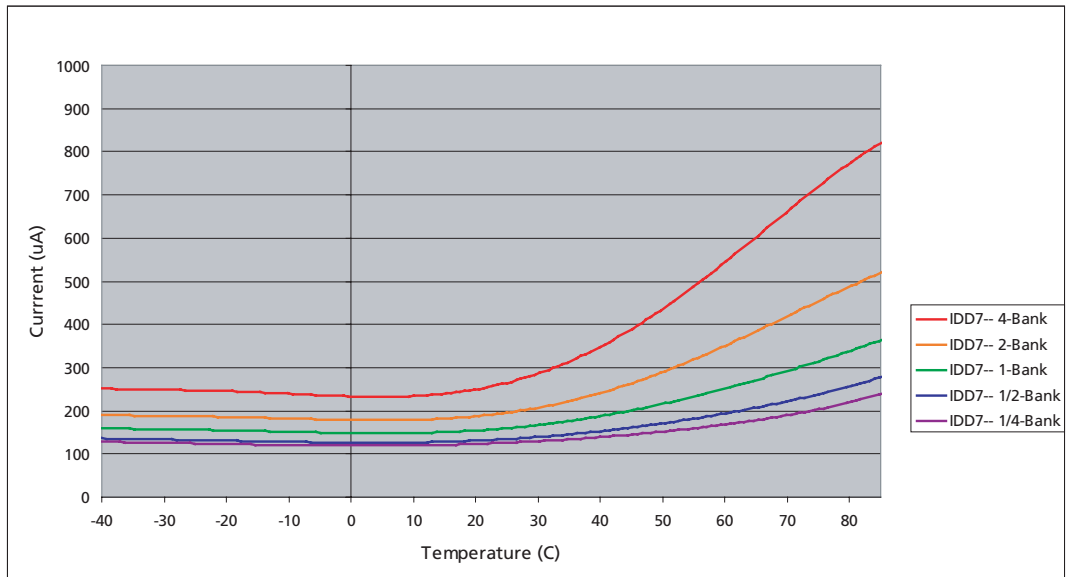
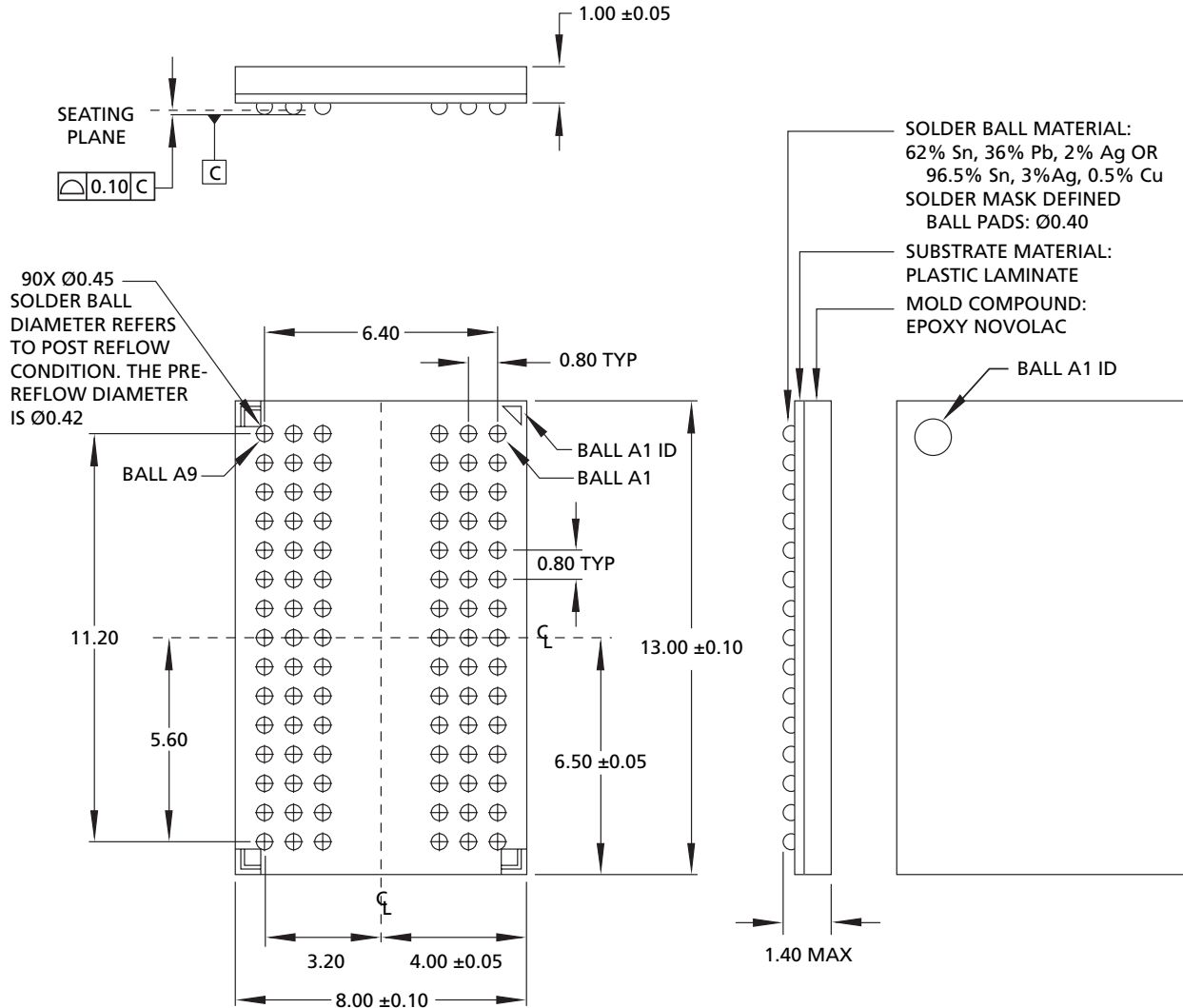


Table 10: Capacitance

Parameter – FBGA "S2" Package	Symbol	MIN	MAX	Units
Input Capacitance: CLK	C1	5	8	pF
Input Capacitance: All other input-only balls	C12	5	8	pF
Input/Output Capacitance: DQs	C10	8	12	pF

Package Dimensions

Figure 6: 90-Ball FBGA (8mm x 13mm)



- Notes: 1. All dimensions in millimeters.
2. Recommended pad size for PCB is 0.4mm ±0.025mm.



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This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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