THE DATASHEET OF

MT46V128M8P-6T:A

www.win-source.net 0086-755-83957316

DDR SDRAM

MT46V256M4 – 64 Meg x 4 x 4 Banks
MT46V128M8 – 32 Meg x 8 x 4 Banks
MT46V64M16 – 16 Meg x 16 x 4 Banks

Features

- VDD = 2.5V ±0.2V, VDDQ = 2.5V ±0.2V
  VDD = 2.6V ±0.1V, VDDQ = 2.6V ±0.1V (DDR400)
- Bidirectional data strobe (DQS) transmitted/ received with data, that is, source-synchronous data capture (x16 has two – one per byte)
- Internal, pipelined double-data-rate (DDR) architecture; two data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- DLL to align DQ and DQS transitions with CK
- Four internal banks for concurrent operation
- Data mask (DM) for masking write data (x16 has two – one per byte)
- Programmable burst lengths (BL): 2, 4, or 8
- Auto refresh and self refresh modes
- Longer-lead TSOP for improved reliability (OCPL)
- 2.5V I/O (SSTL_2 compatible)
- Concurrent auto precharge option is supported
- ^{t}RAS lockout supported (^{t}RAP = ^{t}RCD)

Options — Marking

- Configuration
  - 256 Meg x 4 (64 Meg x 4 x 4 banks) — 256M4
  - 128 Meg x 8 (32 Meg x 8 x 4 banks) — 128M8
  - 64 Meg x 16 (16 Meg x 16 x 4 banks) — 64M16
- Plastic package – OCPL
  - 66-pin TSOP (400-mil width, 0.65mm pin pitch) — TG
  - 66-pin TSOP (Pb-free) (400-mil width, 0.65mm pin pitch) — P
- Timing – cycle time
  - 5.0ns @ CL = 3 (DDR400B) — -5B[1]
  - 6.0ns @ CL = 2.5 (DDR333B)[2] — -6T
  - 7.5ns @ CL = 2.5 (DDR266B)[2] — -75
- Temperature rating
  - Commercial (0°C to +70°C) — None
  - Industrial (–40°C to +85°C) — IT
- Revision — :A

Notes: 1. Not recommended for new designs.
2. See Table 3 on page 2 for module compatibility.

Table 1: Key Timing Parameters
CL = CAS (READ) latency; data-out window is MIN clock rate with 50 percent duty cycle at CL = 2.5

Speed Grade	Clock Rate (MHz)			Data-Out Window	Access Window	DQS–DQ Skew
	CL = 2	CL = 2.5	CL = 3			
-5B	133	167	200	1.6ns	±0.70ns	0.40ns
-6T	133	167	n/a	2.0ns	±0.70ns	0.45ns
-75	100	133	n/a	2.5ns	±0.75ns	0.50ns

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Table 2: Addressing

Parameter	256 Meg x 4	128 Meg x 8	64 Meg x 16
Configuration	64 Meg x 4 x 4 banks	32 Meg x 8 x 4 banks	16 Meg x 16 x 4 banks
Refresh count	8K	8K	8K
Row address	16K (A0–A13)	16K (A0–A13)	16K (A0–A13)
Bank address	4 (BA0, BA1)	4 (BA0, BA1)	4 (BA0, BA1)
Column address	4K (A0–A9, A11, A12)	2K (A0–A9, A11)	1K (A0–A9)

Table 3: Speed Grade Compatibility

Marking	PC3200 (3-3-3)	PC2700 (2.5-3-3)	PC2100 (2-2-2)	PC2100 (2-3-3)	PC2100 (2.5-3-3)	PC1600 (2-2-2)
-5B	Yes	Yes	Yes	Yes	Yes	Yes
-6T	–	Yes	Yes	Yes	Yes	Yes
-75	–	–	–	–	Yes	Yes
	-5B	**-6T**	**-75**	**-75**	**-75**	**-75**

Figure 1: 1Gb DDR SDRAM Part Numbers

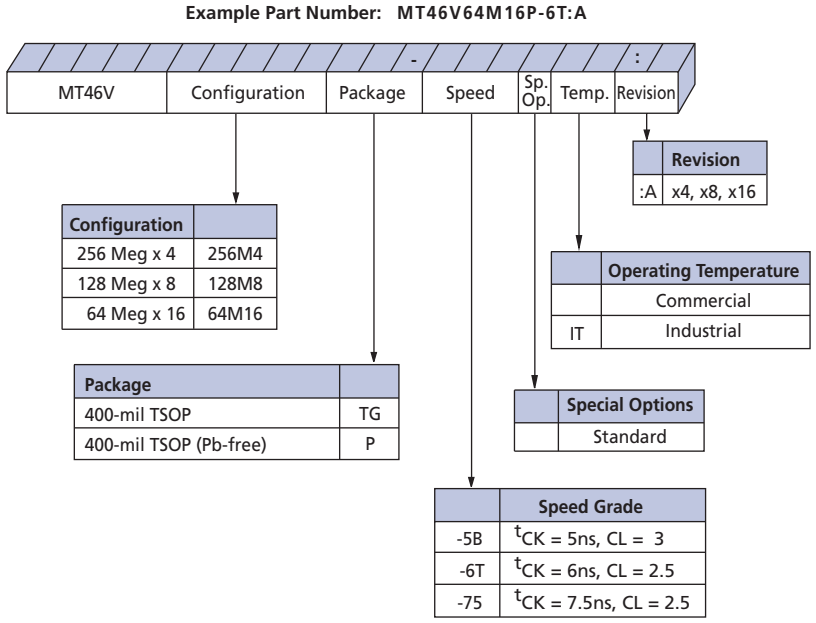

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Table of Contents

State Diagram 4
Functional Description 5
General Notes 5
Functional Block Diagrams 6
Pin Assignments and Descriptions 8
Package Dimensions 11
Electrical Specifications – I_{DD} 12
Electrical Specifications – DC and AC 15
Notes 26
Commands 34
DESELECT 38
NO OPERATION (NOP) 38
LOAD MODE REGISTER (LMR) 38
ACTIVE (ACT) 39
READ 40
WRITE 41
PRECHARGE (PRE) 42
BURST TERMINATE (BST) 42
AUTO REFRESH (AR) 42
SELF REFRESH 42
Operations 43
INITIALIZATION 43
REGISTER DEFINITION 46
ACTIVE 50
READ 51
WRITE 63
PRECHARGE 76
AUTO REFRESH 78
SELF REFRESH 79
Power-down (CKE Not Active) 81

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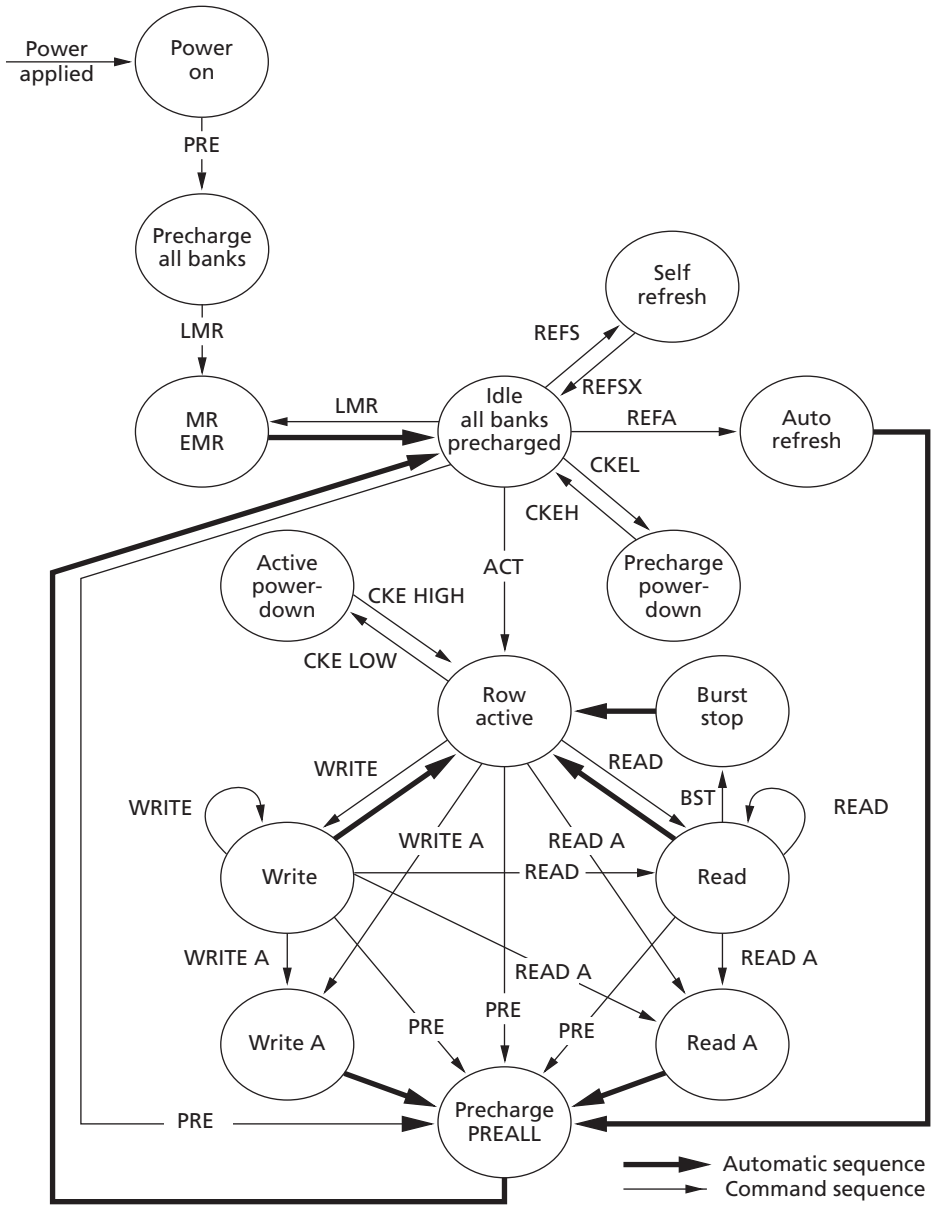
State Diagram

Figure 2: Simplified State Diagram



ACT = ACTIVE
BST = BURST TERMINATE
CKEH = Exit power-down
CKEL = Enter power-down
EMR = Extended mode register
LMR = LOAD MODE REGISTER
MR = Mode register
PRE = PRECHARGE
PREALL = PRECHARGE all banks
READ A = READ with auto precharge
REFA = AUTO REFRESH
REFS = Enter self refresh
REFSX = Exit self refresh
WRITE A = WRITE with auto precharge

Note: This diagram represents operations within a single bank only and does not capture concurrent operations in other banks.

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Functional Description

The DDR SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM effectively consists of a single 2*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. The x16 offering has two data strobes, one for the lower byte and one for the upper byte.

The DDR SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which may then be followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR SDRAM provides for programmable READ or WRITE burst lengths of 2, 4, or 8 locations. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDR SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving power-down mode. All inputs are compatible with the JEDEC standard for SSTL_2. All full-drive option outputs are SSTL_2, Class II compatible.

General Notes

- The functionality and the timing specifications discussed in this data sheet are for the DLL-enabled mode of operation.
- Throughout the data sheet, the various figures and text refer to DQs as “DQ.” The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise. Additionally, the x16 is divided into two bytes, the lower byte and upper byte. For the lower byte (DQ[7:0]) DM refers to LDM and DQS refers to LDQS. For the upper byte (DQ[15:8]) DM refers to UDM and DQS refers to UDQS.
- Complete functionality is described throughout the document and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
- Any specific requirement takes precedence over a general statement.

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Functional Block Diagrams

The 1Gb DDR SDRAM is a high-speed CMOS, dynamic random access memory containing 1,073,741,824 bits. It is internally configured as a 4-bank DRAM.

Figure 3: 256 Meg x 4 Functional Block Diagram

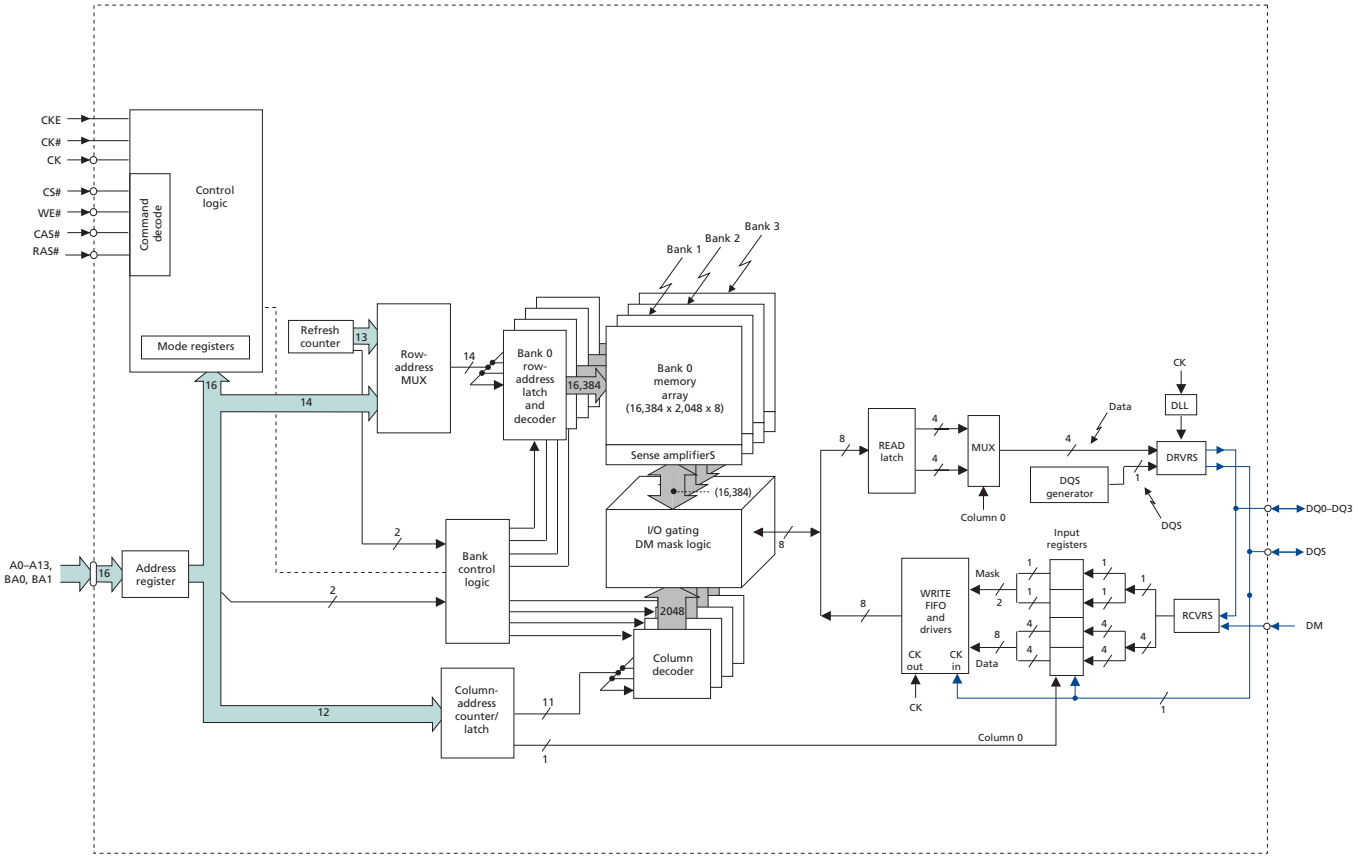

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Figure 4: 128 Meg x 8 Functional Block Diagram

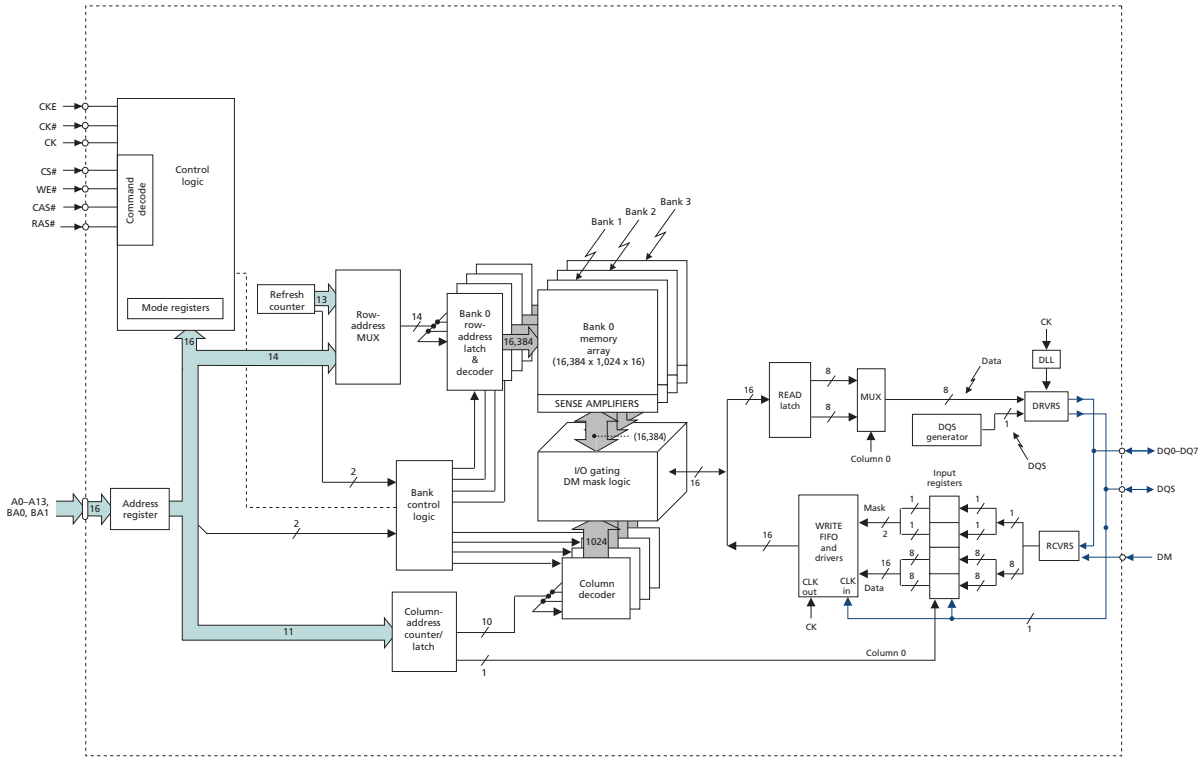
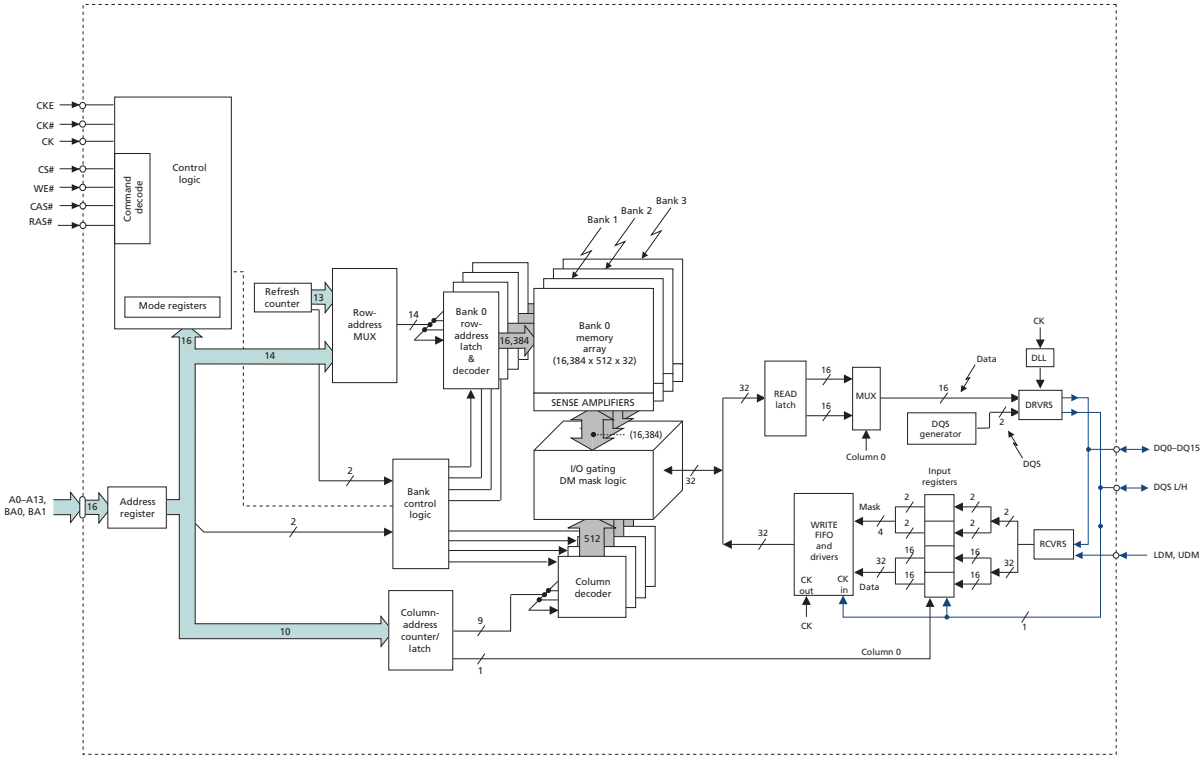


Figure 5: 64 Meg x 16 Functional Block Diagram



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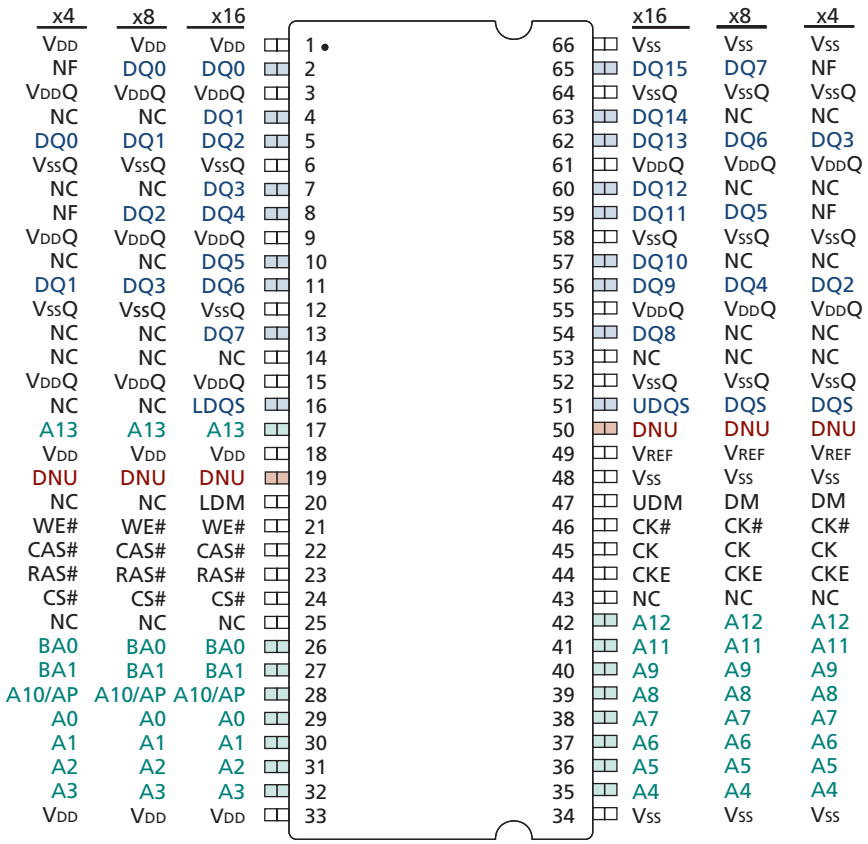
Pin Assignments and Descriptions

Figure 6: 66-pin TSOP Pin Assignments (Top View)



x4	x8	x16			x16	x8	x4
VDD	VDD	VDD	1 •	66	VSS	VSS	VSS
NF	DQ0	DQ0	2	65	DQ15	DQ7	NF
VDDQ	VDDQ	VDDQ	3	64	VSSQ	VSSQ	VSSQ
NC	NC	DQ1	4	63	DQ14	NC	NC
DQ0	DQ1	DQ2	5	62	DQ13	DQ6	DQ3
VSSQ	VSSQ	VSSQ	6	61	VDDQ	VDDQ	VDDQ
NC	NC	DQ3	7	60	DQ12	NC	NC
NF	DQ2	DQ4	8	59	DQ11	DQ5	NF
VDDQ	VDDQ	VDDQ	9	58	VSSQ	VSSQ	VSSQ
NC	NC	DQ5	10	57	DQ10	NC	NC
DQ1	DQ3	DQ6	11	56	DQ9	DQ4	DQ2
VSSQ	VSSQ	VSSQ	12	55	VDDQ	VDDQ	VDDQ
NC	NC	DQ7	13	54	DQ8	NC	NC
NC	NC	NC	14	53	NC	NC	NC
VDDQ	VDDQ	VDDQ	15	52	VSSQ	VSSQ	VSSQ
NC	NC	LDQS	16	51	UDQS	DQS	DQS
A13	A13	A13	17	50	DNU	DNU	DNU
VDD	VDD	VDD	18	49	VREF	VREF	VREF
DNU	DNU	DNU	19	48	VSS	VSS	VSS
NC	NC	LDM	20	47	UDM	DM	DM
WE#	WE#	WE#	21	46	CK#	CK#	CK#
CAS#	CAS#	CAS#	22	45	CK	CK	CK
RAS#	RAS#	RAS#	23	44	CKE	CKE	CKE
CS#	CS#	CS#	24	43	NC	NC	NC
NC	NC	NC	25	42	A12	A12	A12
BA0	BA0	BA0	26	41	A11	A11	A11
BA1	BA1	BA1	27	40	A9	A9	A9
A10/AP	A10/AP	A10/AP	28	39	A8	A8	A8
A0	A0	A0	29	38	A7	A7	A7
A1	A1	A1	30	37	A6	A6	A6
A2	A2	A2	31	36	A5	A5	A5
A3	A3	A3	32	35	A4	A4	A4
VDD	VDD	VDD	33	34	VSS	VSS	VSS

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Table 4: Pin Descriptions

TSOP Numbers	Symbol	Type	Description
29, 30, 31, 32, 35, 36, 37, 38, 39, 40, 28, 41, 42, 17	A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, A12, A13	Input	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0, BA1) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER (LMR) command.
26, 27	BA0, BA1	Input	**Bank address inputs:** BA0 and BA1 define the bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0 and BA1 also define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command.
45, 46	CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data (DQ and DQS) is referenced to the crossings of CK and CK#.
44	CKE	Input	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers, and output drivers. Taking CKE LOW provides PRECHARGE power-down and SELF REFRESH operations (all banks idle) or ACTIVE power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, CK#, and CKE) are disabled during power-down. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_2 input but will detect an LVCMOS LOW level after V_{DD} is applied and until CKE is first brought HIGH, after which it becomes a SSTL_2 input only.
24	CS#	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
47 20, 47	DM LDM, UDM	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins. For the x16, LDM is DM for DQ[7;0] and UDM is DM for DQ[15:8]. Pin 20 is a NC on x4 and x8.
23, 22, 21	RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with CS#) define the command being entered.
2, 4, 5, 7, 8, 10, 11, 13, 54, 56, 57, 59, 60, 62, 63, 65	DQ[3:0] DQ[7:4] DQ[11:8] DQ[15:12]	I/O	**Data input/output:** Data bus for x16.
2, 5, 8, 11, 56, 59, 62, 65	DQ[3:0] DQ[7:4]	I/O	**Data input/output:** Data bus for x8.
5, 11, 56, 62	DQ[3:0]	I/O	**Data input/output:** Data bus for x4.
51 16 51	DQS LDQS UDQS	I/O	**Data strobe:** Output with read data, input with write data. DQS is edge-aligned with read data, center-aligned with write data. It is used to capture data. For the x16, LDQS is DQS for DQ[7:0] and UDQS is DQS for DQ[15:8]. Pin 16 is NC on x4 and x8.
1, 18, 33	V_{DD}	Supply	Power supply.
3, 9, 15, 55, 61	V_{DDQ}	Supply	**DQ power supply:** Isolated on the die for improved noise immunity.

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Table 4: Pin Descriptions (continued)

TSOP Numbers	Symbol	Type	Description
34, 48, 66	V_{SS}	Supply	Ground.
6, 12, 52, 58, 64	V_{SSQ}	Supply	**DQ ground:** Isolated on the die for improved noise immunity.
49	V_{REF}	Supply	SSTL_2 reference voltage.
14, 25, 43, 53	NC	–	**No connect for x16:** These pins should be left unconnected.
4, 7, 10, 13, 14, 16, 20, 25, 43, 53, 54, 57, 60, 63	NC	–	**No connect for x8:** These pins should be left unconnected.
4, 7, 10, 13, 14, 16, 20, 25, 43, 53, 54, 57, 60, 63	NC	–	**No connect for x4:** These pins should be left unconnected.
2, 8, 59, 65	NF	–	**No function for x4:** These pins should be left unconnected.
19, 50	DNU	–	**Do not use:** Must float to minimize noise on V_{REF}.

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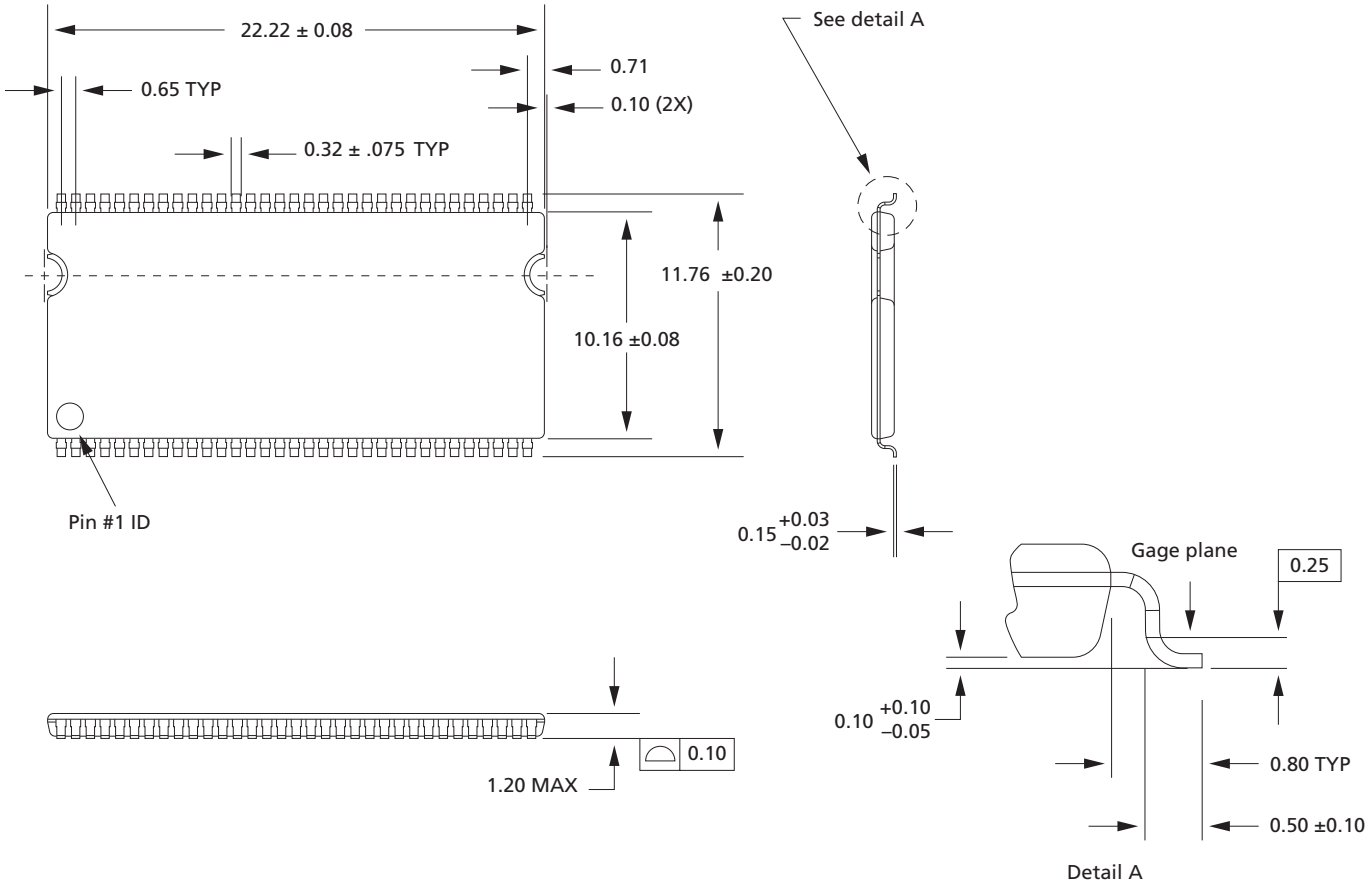
Package Dimensions

Figure 7: 66-Pin Plastic TSOP (400 mil)



Notes:
1. All dimensions in millimeters.
2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.

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Electrical Specifications – I_{DD}

Table 5: I_{DD} Specifications and Conditions (x4, x8)

Notes 1–5, 11, 13, 15, and 47 apply to the entire table; Notes appear on page 26; See also Table 7 on page 14; V_{DDQ} = 2.6V ±0.1V, V_{DD} = 2.6V ±0.1V (-5B); V_{DDQ} = 2.5V ±0.2V, V_{DD} = 2.5V ±0.2V (-6T, -75); 0°C ≤ T_A ≤ 70°C

Parameter/Condition		Symbol	-5B	-6T	-75	Units	Notes
Operating one-bank active-precharge current: ^tRC = ^tRC (MIN); ^tCK = ^tCK (MIN); DQ, DM, and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		I_{DD0}	165	160	145	mA	23, 48
Operating one-bank active-read-precharge current: BL = 4; ^tRC = ^tRC (MIN); ^tCK = ^tCK (MIN); I_{OUT} = 0mA; Address and control inputs changing once per clock cycle		I_{DD1}	200	195	180	mA	23, 48
Precharge power-down standby current: All banks idle; Power-down mode; ^tCK = ^tCK (MIN); CKE = LOW		I_{DD2P}	13	10	10	mA	24, 33
Idle standby current: CS# = HIGH; All banks are idle; ^tCK = ^tCK (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle. V_{IN} = V_{REF} for DQ, DQS, and DM		I_{DD2F}	70	65	60	mA	51
Active power-down standby current: One bank active; Power-down mode; ^tCK = ^tCK (MIN); CKE = LOW		I_{DD3P}	40	35	30	mA	24, 33
Active standby current: CS# = HIGH; CKE = HIGH; One bank active; ^tRC = ^tRAS (MAX); ^tCK = ^tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		I_{DD3N}	55	50	45	mA	23
Operating burst read current: BL = 2; Continuous burst reads; One bank active; Address and control inputs changing once per clock cycle; ^tCK = ^tCK (MIN); I_{OUT} = 0mA		I_{DD4R}	225	220	200	mA	23, 48
Operating burst write current: BL = 2; Continuous burst writes; One bank active; Address and control inputs changing once per clock cycle; ^tCK = ^tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		I_{DD4W}	235	230	210	mA	23
Auto refresh burst current:	^tREFC = ^tRFC (MIN)	I_{DD5}	345	340	330	mA	50
	^tREFC = 7.8µs	I_{DD5A}	13	10	10	mA	28, 50
Self refresh current: CKE ≤ 0.2V	Standard	I_{DD6}	10	9	9	mA	12
Operating bank interleave read current: Four bank interleaving READs (BL = 4) with auto precharge; ^tRC = MIN; ^tCK = ^tCK (MIN); Address and control inputs change only during ACTIVE, READ, or WRITE commands		I_{DD7}	530	525	485	mA	23, 49

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Table 6: I_{DD} Specifications and Conditions (x16)

Notes 1–5, 11, 13, 15, and 47 apply to the entire table; Notes appear on page 26; See also Table 7 on page 14; V_{DDQ} = 2.6V ±0.1V, V_{DD} = 2.6V ±0.1V (-5B); V_{DDQ} = 2.5V ±0.2V, V_{DD} = 2.5V ±0.2V (-6T, -75); 0°C ≤ T_A ≤ 70°C

Parameter/Condition		Symbol	-5B	-6T	-75	Units	Notes
Operating one-bank active-precharge current: ^tRC = ^tRC (MIN); ^tCK = ^tCK (MIN); DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles		I_{DD0}	170	165	145	mA	23, 48
Operating one-bank active-read-precharge current: BL = 4; ^tRC = ^tRC (MIN); ^tCK = ^tCK (MIN); I_{OUT} = 0mA; Address and control inputs changing once per clock cycle		I_{DD1}	215	210	195	mA	23, 48
Precharge power-down standby current: All banks idle; Power-down mode; ^tCK = ^tCK (MIN); CKE = LOW		I_{DD2P}	15	10	10	mA	24, 33
Idle standby current: CS# = HIGH; All banks are idle; ^tCK = ^tCK (MIN); CKE = HIGH; Address and other control inputs changing once per clock cycle. V_{IN} = V_{REF} for DQ, DQS, and DM		I_{DD2F}	70	65	60	mA	51
Active power-down standby current: One bank active; Power-down mode; ^tCK = ^tCK (MIN); CKE = LOW		I_{DD3P}	40	35	30	mA	24, 33
Active standby current: CS# = HIGH; CKE = HIGH; One bank active; ^tRC = ^tRAS (MAX); ^tCK = ^tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		I_{DD3N}	55	50	45	mA	23
Operating burst read current: BL = 2; Continuous burst reads; One bank active; Address and control inputs changing once per clock cycle; ^tCK = ^tCK (MIN); I_{OUT} = 0mA		I_{DD4R}	280	270	245	mA	23, 48
Operating burst write current: BL = 2; Continuous burst writes; One bank active; Address and control inputs changing once per clock cycle; ^tCK = ^tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle		I_{DD4W}	285	275	250	mA	23
Auto refresh burst current:	^tREFC = ^tRFC (MIN)	I_{DD5}	345	340	330	mA	50
	^tREFC = 7.8µs	I_{DD5A}	15	10	10	mA	28, 50
Self refresh current: CKE ≤ 0.2V	Standard	I_{DD6}	10	9	9	mA	12
Operating bank interleave read current: Four bank interleaving READs (BL = 4) with auto precharge; ^tRC = MIN; ^tCK = ^tCK (MIN); Address and control inputs change only during ACTIVE, READ, or WRITE commands		I_{DD7}	545	535	495	mA	23, 49

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Table 7: I_{DD} Test Cycle Times

Values reflect number of clock cycles for each test

I_{DD} Test	Speed Grade	Clock Cycle Time	^{t}RRD	^{t}RCD	^{t}RAS	^{t}RP	^{t}RC	^{t}RFC	^{t}REFI	CL
I_{DD0}	-75	7.5ns	n/a	n/a	6	3	9	n/a	n/a	n/a
	-6T	6.0ns	n/a	n/a	7	3	10	n/a	n/a	n/a
	-5B	5.0ns	n/a	n/a	8	3	11	n/a	n/a	n/a
I_{DD1}	-75	7.5ns	n/a	n/a	6	3	9	n/a	n/a	2.5
	-6T	6.0ns	n/a	n/a	7	3	10	n/a	n/a	2.5
	-5B	5.0ns	n/a	n/a	8	3	11	n/a	n/a	3
I_{DD4R}	-75	7.5ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	2.5
	-6T	6.0ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	2.5
	-5B	5.0ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	3
I_{DD4W}	-75	7.5ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
	-6T	6.0ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
	-5B	5.0ns	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
I_{DD5}	-75	7.5ns	n/a	n/a	n/a	n/a	n/a	16	16	n/a
	-6T	6.0ns	n/a	n/a	n/a	n/a	n/a	20	20	n/a
	-5B	5.0ns	n/a	n/a	n/a	n/a	n/a	24	24	n/a
I_{DD5A}	-75	7.5ns	n/a	n/a	n/a	n/a	n/a	16	1,026	n/a
	-6T	6.0ns	n/a	n/a	n/a	n/a	n/a	20	1,182	n/a
	-5B	5.0ns	n/a	n/a	n/a	n/a	n/a	24	1,414	n/a
I_{DD7}	-75	7.5ns	2	3	n/a	3	10	n/a	n/a	2.5
	-6T	6.0ns	2	3	n/a	3	10	n/a	n/a	2.5
	-5B	5.0ns	2	3	n/a	3	11	n/a	n/a	3

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Electrical Specifications – DC and AC

Stresses greater than those listed in Table 8 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 8: Absolute Maximum Ratings

Parameter	Min	Max	Units
V_{DD} supply voltage relative to V_{SS}	–1V	3.6V	V
V_{DDQ} supply voltage relative to V_{SS}	–1V	3.6V	V
V_{REF} and inputs voltage relative to V_{SS}	–1V	3.6V	V
I/O pins voltage relative to V_{SS}	–0.5V	V_{DDQ} + 0.5V	V
Storage temperature (plastic)	–55	150	°C
Short circuit output current	–	50	mA

Table 9: DC Electrical Characteristics and Operating Conditions (-5B)

Notes: 1–5 and 17 apply to the entire table; Notes appear on page 26; V_{DDQ} = 2.6V ±0.1V, V_{DD} = 2.6V ±0.1V

Parameter/Condition		Symbol	Min	Max	Units	Notes
Supply voltage		V_{DD}	2.5	2.7	V	37, 42
I/O supply voltage		V_{DDQ}	2.5	2.7	V	37, 42, 45
I/O reference voltage		V_{REF}	0.49 × V_{DDQ}	0.51 × V_{DDQ}	V	7, 45
I/O termination voltage (system)		V_{TT}	V_{REF} - 0.04	V_{REF} + 0.04	V	8, 45
Input high (logic 1) voltage		$V_{IH(DC)}$	V_{REF} + 0.15	V_{DD} + 0.3	V	29
Input low (logic 0) voltage		$V_{IL(DC)}$	–0.3	V_{REF} - 0.15	V	29
Input leakage current: Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} pin 0V ≤ V_{IN} ≤ 1.35V (All other pins not under test = 0V)		I_I	–2	2	µA	
Output leakage current: (DQ are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ})		I_{OZ}	–5	5	µA	
Full-drive option output levels (x4, x8, x16):	High current (V_{OUT} = V_{DDQ} - 0.373V, minimum V_{REF}, minimum V_{TT})	I_{OH}	–16.8	–	mA	38, 40
	Low current (V_{OUT} = 0.373V, maximum V_{REF}, maximum V_{TT})	I_{OL}	16.8	–	mA	
Reduced-drive option output levels:	High current (V_{OUT} = V_{DDQ} - 0.373V, minimum V_{REF}, minimum V_{TT})	I_{OHR}	–9	–	mA	39, 40
	Low current (V_{OUT} = 0.373V, maximum V_{REF}, maximum V_{TT})	I_{OLR}	9	–	mA	
Ambient operating temperatures	Commercial	T_A	0	70	°C	
	Industrial	T_A	–40	85	°C	

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Table 10: DC Electrical Characteristics and Operating Conditions (-6, -6T, -75E, -75Z, -75)

Notes: 1–5 and 17 apply to the entire table; Notes appear on page 26; V_{DDQ} = 2.5V ±0.2V, V_{DD} = 2.5V ±0.2V

Parameter/Condition		Symbol	Min	Max	Units	Notes
Supply voltage		V_{DD}	2.3	2.7	V	37, 42
I/O supply voltage		V_{DDQ}	2.3	2.7	V	37, 42, 45
I/O reference voltage		V_{REF}	0.49 × V_{DDQ}	0.51 × V_{DDQ}	V	7, 45
I/O termination voltage (system)		V_{TT}	V_{REF} - 0.04	V_{REF} + 0.04	V	8, 45
Input high (logic 1) voltage		$V_{IH(DC)}$	V_{REF} + 0.15	V_{DD} + 0.3	V	29
Input low (logic 0) voltage		$V_{IL(DC)}$	–0.3	V_{REF} - 0.15	V	29
Input leakage current: Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} pin 0V ≤ V_{IN} ≤ 1.35V (All other pins not under test = 0V)		I_I	–2	2	µA	
Output leakage current: (DQ are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ})		I_{OZ}	–5	5	µA	
Full-drive option output levels (x4, x8, x16):	High current (V_{OUT} = V_{DDQ} - 0.373V, minimum V_{REF}, minimum V_{TT})	I_{OH}	–16.8	–	mA	38, 40
	Low current (V_{OUT} = 0.373V, maximum V_{REF}, maximum V_{TT})	I_{OL}	16.8	–	mA	
Reduced-drive option output levels:	High current (V_{OUT} = V_{DDQ} - 0.373V, minimum V_{REF}, minimum V_{TT})	I_{OHR}	–9	–	mA	39, 40
	Low current (V_{OUT} = 0.373V, maximum V_{REF}, maximum V_{TT})	I_{OLR}	9	–	mA	
Ambient operating temperatures	Commercial	T_A	0	70	°C	
	Industrial	T_A	–40	85	°C	

Table 11: AC Input Operating Conditions

Notes: 1–5 and 17 apply to the entire table; Notes appear on page 26;
0°C ≤ T_A ≤ 70°C; V_{DDQ} = 2.5V ±0.2V, V_{DD} = 2.5V ±0.2V (V_{DDQ} = 2.6V ±0.1V, V_{DD} = 2.6V ±0.1V for -5B)

Parameter/Condition	Symbol	Min	Max	Units	Notes
Input high (logic 1) voltage	$V_{IH(AC)}$	V_{REF} + 0.310	–	V	15, 29, 41
Input low (logic 0) voltage	$V_{IL(AC)}$	–	V_{REF} - 0.310	V	15, 29, 41
I/O reference voltage	$V_{REF(AC)}$	0.49 × V_{DDQ}	0.51 × V_{DDQ}	V	7

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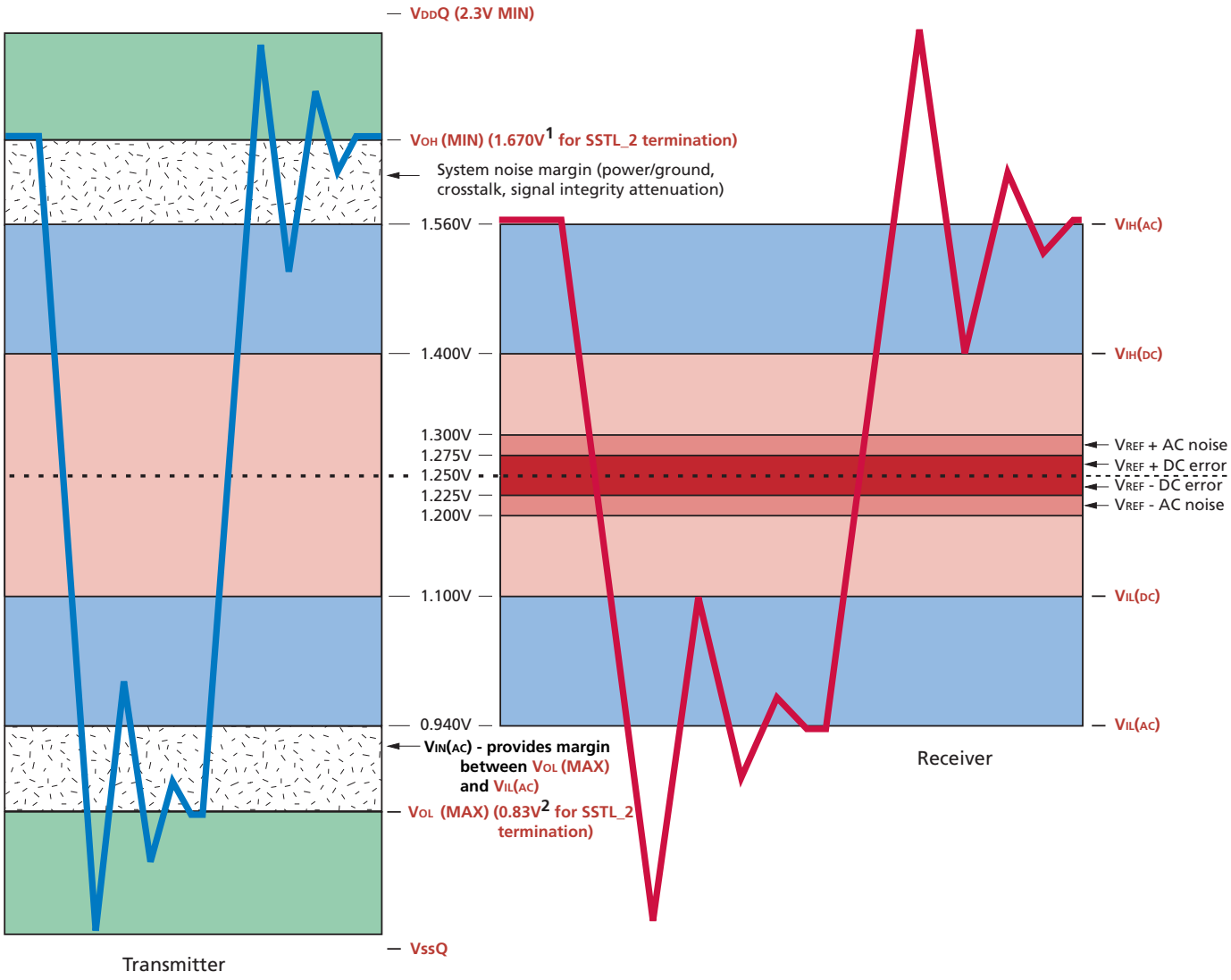
Figure 8: Input Voltage Waveform



Notes:
1. $V_{OH,min}$ with test load is 1.927V.
2. $V_{OL,max}$ with test load is 0.373V.
3. Numbers in diagram reflect nominal values utilizing circuit below for all devices other than -5B.

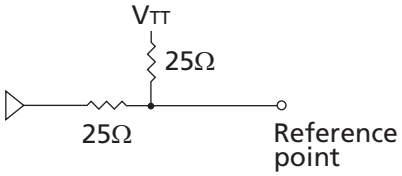


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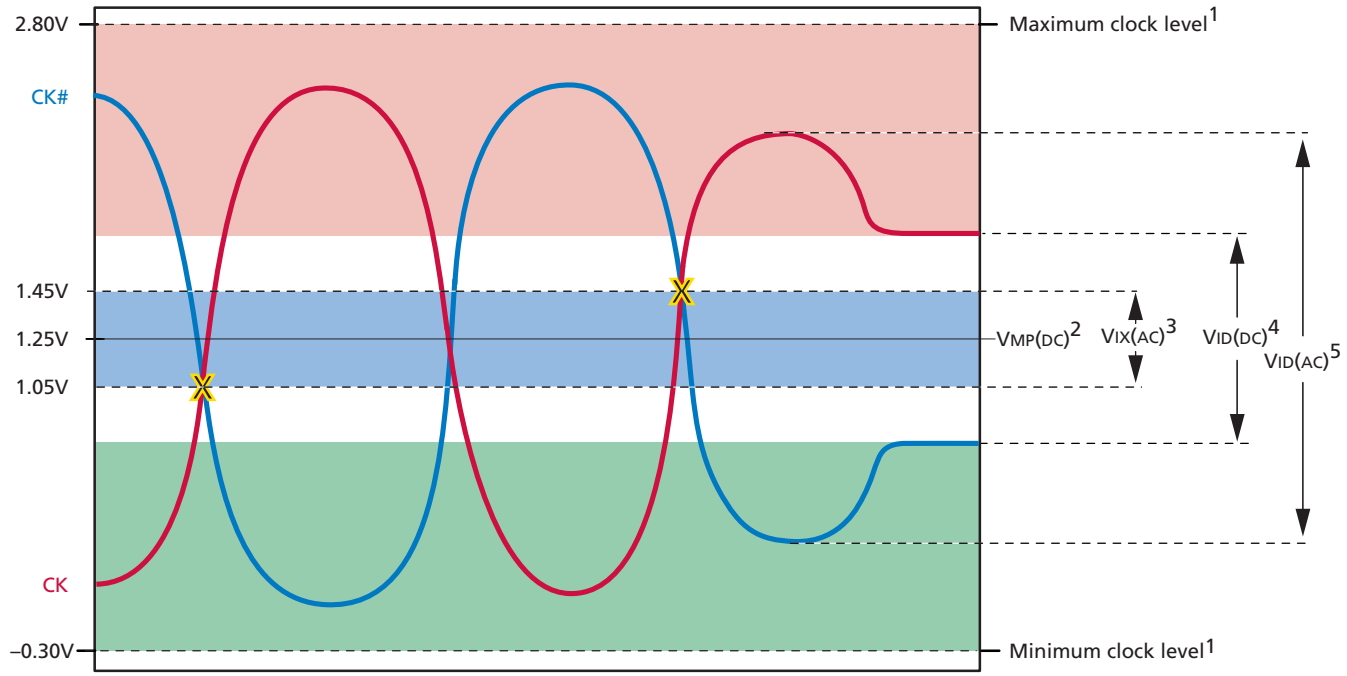
Table 12: Clock Input Operating Conditions

Notes: 1–5, 16, 17, and 31 apply to the entire table; Notes appear on page 26;
0°C ≤ T_A ≤ 70°C; V_{DDQ} = 2.5V ±0.2V, V_{DD} = 2.5V ±0.2V (V_{DDQ} = 2.6V ±0.1V, V_{DD} = 2.6V ±0.1V for -5B)

Parameter/Condition	Symbol	Min	Max	Units	Notes
Clock input mid-point voltage: CK and CK#	$V_{MP(DC)}$	1.15	1.35	V	7, 10
Clock input voltage level: CK and CK#	$V_{IN(DC)}$	–0.3	V_{DDQ} + 0.3	V	7
Clock input differential voltage: CK and CK#	$V_{ID(DC)}$	0.36	V_{DDQ} + 0.6	V	7, 9
Clock input differential voltage: CK and CK#	$V_{ID(AC)}$	0.7	V_{DDQ} + 0.6	V	9
Clock input crossing point voltage: CK and CK#	$V_{IX(AC)}$	0.5 × V_{DDQ} - 0.2	0.5 × V_{DDQ} + 0.2	V	10

Figure 9: SSTL_2 Clock Input



Notes:
1. CK or CK# may not be more positive than V_{DDQ} + 0.3V or more negative than V_{SS} - 0.3V.
2. This provides a minimum of 1.15V to a maximum of 1.35V and is always half of V_{DDQ}.
3. CK and CK# must cross in this region.
4. CK and CK# must meet at least $V_{ID(DC),min}$ when static and is centered around $V_{MP(DC)}$.
5. CK and CK# must have a minimum 700mV peak-to-peak swing.
6. For AC operation, all DC clock requirements must also be satisfied.
7. Numbers in diagram reflect nominal values for all devices other than -5B.

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Table 13: Capacitance (x4, x8 TSOP)
Note: 14 applies to the entire table; Notes appear on page 26

Parameter	Symbol	Min	Max	Units	Notes
Delta input/output capacitance: DQ[3:0] (x4), DQ[7:0] (x8)	DC_{IO}	–	0.50	pF	25
Delta input capacitance: Command and address	DC_{I1}	–	0.50	pF	30
Delta input capacitance: CK, CK#	DC_{I2}	–	0.25	pF	30
Input/output capacitance: DQ, DQS, DM	C_{IO}	4.0	5.0	pF	
Input capacitance: Command and address	C_{I1}	2.0	3.0	pF	
Input capacitance: CK, CK#	C_{I2}	2.0	3.0	pF	
Input capacitance: CKE	C_{I3}	2.0	3.0	pF	

Table 14: Capacitance (x16 TSOP)
Note: 14 applies to the entire table; Notes appear on page 26

Parameter	Symbol	Min	Max	Units	Notes
Delta input/output capacitance: DQ[7:0], LDQS, LDM	DC_{IOL}	–	0.50	pF	25
Delta input/output capacitance: DQ[15:8], UDQS, UDM	DC_{IOU}	–	0.50	pF	25
Delta input capacitance: Command and address	DC_{I1}	–	0.50	pF	30
Delta input capacitance: CK, CK#	DC_{I2}	–	0.25	pF	30
Input/output capacitance: DQ, LDQS, UDQS, LDM, UDM	C_{IO}	4.0	5.0	pF	
Input capacitance: Command and address	C_{I1}	2.0	3.0	pF	
Input capacitance: CK, CK#	C_{I2}	2.0	3.0	pF	
Input capacitance: CKE	C_{I3}	2.0	3.0	pF	

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Table 15: Electrical Characteristics and Recommended AC Operating Conditions (-5B)

Notes 1–6, 16–18, and 34 apply to the entire table; Notes appear on page 26;
$0°C \le T_A \le 70°C$; V_{DDQ} = 2.6V ±0.1V, V_{DD} = 2.6V ±0.1V

AC Characteristics			-5B			
Parameter		**Symbol**	**Min**	**Max**	**Units**	**Notes**
Access window of DQ from CK/CK#		^tAC	–0.70	0.70	ns	
CK high-level width		^tCH	0.45	0.55	^tCK	31
Clock cycle time	CL = 3	^tCK (3)	5	7.5	ns	52
	CL = 2.5	^tCK (2.5)	6	13	ns	46, 52
	CL = 2	^tCK (2)	7.5	13	ns	46, 52
CK low-level width		^tCL	0.45	0.55	^tCK	31
DQ and DM input hold time relative to DQS		^tDH	0.40	–	ns	27, 32
DQ and DM input pulse width (for each input)		^tDIPW	1.75	–	ns	32
Access window of DQS from CK/CK#		^tDQSCK	–0.60	0.60	ns	
DQS input high pulse width		^tDQSH	0.35	–	^tCK	
DQS input low pulse width		^tDQSL	0.35	–	^tCK	
DQS–DQ skew, DQS to last DQ valid, per group, per access		^tDQSQ	–	0.40	ns	26, 27
WRITE command to first DQS latching transition		^tDQSS	0.72	1.28	^tCK	
DQ and DM input setup time relative to DQS		^tDS	0.40	–	ns	27, 32
DQS falling edge from CK rising – hold time		^tDSH	0.2	–	^tCK	
DQS falling edge to CK rising – setup time		^tDSS	0.2	–	^tCK	
Half-clock period		^tHP	^tCH,^tCL	–	ns	35
Data-out High-Z window from CK/CK#		^tHZ	–	0.70	ns	19, 43
Address and control input hold time (slew rate ≥0.5 V/ns)		^tIH_F	0.60	–	ns	15
Address and control input pulse width (for each input)		^tIPW	2.2	–	ns	
Address and control input setup time (slew rate ≥0.5 V/ns)		^tIS_F	0.60	–	ns	15
Data-out Low-Z window from CK/CK#		^tLZ	–0.70	–	ns	19, 43
LOAD MODE REGISTER command cycle time		^tMRD	10	–	ns	
DQ–DQS hold, DQS to first DQ to go non-valid, per access		^tQH	^tHP -^tQHS	–	ns	26, 27
Data hold skew factor		^tQHS	–	0.50	ns	
ACTIVE-to-READ with auto precharge command		^tRAP	15	–	ns	
ACTIVE-to-PRECHARGE command		^tRAS	40	70,000	ns	36
ACTIVE-to-ACTIVE/AUTO REFRESH command period		^tRC	55	–	ns	55
ACTIVE-to-READ or WRITE delay		^tRCD	15	–	ns	
REFRESH-to-REFRESH command interval1Gb		^tREFC	–	70.3	µs	24
AUTO REFRESH command period	1Gb	^tRFC	120	–	ns	50
Average periodic refresh interval		^tREFI	–	7.8	µs	24
AUTO REFRESH command period		^tRFC	70	–	ns	50
PRECHARGE command period		^tRP	15	–	ns	
DQS read preamble		^tRPRE	0.9	1.1	^tCK	44
DQS read postamble		^tRPST	0.4	0.6	^tCK	44
ACTIVE bank *a* to ACTIVE bank *b* command		^tRRD	10	–	ns	
Terminating voltage delay to V_{DD}		^tVTD	0	–	ns	
DQS write preamble		^tWPRE	0.25	–	^tCK	
DQS write preamble setup time		^tWPRES	0	–	ns	21, 22
DQS write postamble		^tWPST	0.4	0.6	^tCK	20
Write recovery time		^tWR	15	–	ns	

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Table 15: Electrical Characteristics and Recommended AC Operating Conditions (-5B) (continued)
Notes 1–6, 16–18, and 34 apply to the entire table; Notes appear on page 26;
0°C ≤ T_A ≤ 70°C; V_{DDQ} = 2.6V ±0.1V, V_{DD} = 2.6V ±0.1V

AC Characteristics			-5B			
Parameter		**Symbol**	**Min**	**Max**	**Units**	**Notes**
Internal WRITE-to-READ command delay		^{t}WTR	2	–	^{t}CK	
Exit SELF REFRESH-to-non-READ command	1Gb	^{t}XSNR	126	–	ns	
Exit SELF REFRESH-to-READ command		^{t}XSRD	200	–	^{t}CK	
Data valid output window		n/a	^{t}QH - ^{t}DQSQ		ns	26

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Table 16: Electrical Characteristics and Recommended AC Operating Conditions (-6T)

Notes: 1–6, 16–18, and 34 apply to the entire table; Notes appear on page 26;
$0°C \le T_A \le 70°C$; V_{DDQ} = 2.5V ±0.2V, V_{DD} = 2.5V ±0.2V

AC Characteristics			-6T (TSOP)			
Parameter		**Symbol**	**Min**	**Max**	**Units**	**Notes**
Access window of DQ from CK/CK#		^tAC	–0.70	0.70	ns	
CK high-level width		^tCH	0.45	0.55	^tCK	31
Clock cycle time	CL = 2.5	^tCK (2.5)	6	13	ns	46, 52
	CL = 2	^tCK (2)	7.5	13	ns	46, 52
CK low-level width		^tCL	0.45	0.55	^tCK	31
DQ and DM input hold time relative to DQS		^tDH	0.45	–	ns	27, 32
DQ and DM input pulse width (for each input)		^tDIPW	1.75	–	ns	32
Access window of DQS from CK/CK#		^tDQSCK	–0.6	0.6	ns	
DQS input high pulse width		^tDQSH	0.35	–	^tCK	
DQS input low pulse width		^tDQSL	0.35	–	^tCK	
DQS–DQ skew, DQS to last DQ valid, per group, per access		^tDQSQ	–	0.45	ns	26, 27
WRITE command to first DQS latching transition		^tDQSS	0.75	1.25	^tCK	
DQ and DM input setup time relative to DQS		^tDS	0.45	–	ns	27, 32
DQS falling edge from CK rising - hold time		^tDSH	0.2	–	^tCK	
DQS falling edge to CK rising - setup time		^tDSS	0.2	–	^tCK	
Half-clock period		^tHP	^tCH, ^tCL	–	ns	35
Data-out High-Z window from CK/CK#		^tHZ	–	0.7	ns	19, 43
Address and control input hold time (fast slew rate)		^tIH_F	0.75	–	ns	
Address and control input hold time (slow slew rate)		^tIH_S	0.8	–	ns	15
Address and control input pulse width (for each input)		^tIPW	2.2	–	ns	
Address and control input setup time (fast slew rate)		^tIS_F	0.75	–	ns	
Address and control input setup time (slow slew rate)		^tIS_S	0.8	–	ns	15
Data-out Low-Z window from CK/CK#		^tLZ	–0.7	–	ns	19, 43
LOAD MODE REGISTER command cycle time		^tMRD	12	–	ns	
DQ-DQS hold, DQS to first DQ to go non-valid, per access		^tQH	^tHP - ^tQHS	–	ns	26, 27
Data hold skew factor		^tQHS	–	0.55	ns	
ACTIVE-to-READ with auto precharge command		^tRAP	15	–	ns	
ACTIVE-to-PRECHARGE command		^tRAS	42	70,000	ns	36, 54
ACTIVE-to-ACTIVE/AUTO REFRESH command period		^tRC	60	–	ns	55
ACTIVE-to-READ or WRITE delay		^tRCD	15	–	ns	
REFRESH-to-REFRESH command interval		^tREFC	–	70.3	µs	24
Average periodic refresh interval		^tREFI	–	7.8	µs	24
AUTO REFRESH command period	1Gb	^tRFC	120	–	ns	50
PRECHARGE command period		^tRP	15	–	ns	
DQS read preamble		^tRPRE	0.9	1.1	^tCK	44
DQS read postamble		^tRPST	0.4	0.6	^tCK	44
ACTIVE bank *a* to ACTIVE bank *b* command		^tRRD	12	–	ns	
Terminating voltage delay to V_{SS}		^tVTD	0	–	ns	
DQS write preamble		^tWPRE	0.25	–	^tCK	
DQS write preamble setup time		^tWPRES	0	–	ns	21, 22
DQS write postamble		^tWPST	0.4	0.6	^tCK	20

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Table 16: Electrical Characteristics and Recommended AC Operating Conditions (-6T) (continued)
Notes: 1–6, 16–18, and 34 apply to the entire table; Notes appear on page 26;
$0°C \le T_A \le 70°C$; V_{DDQ} = 2.5V ±0.2V, V_{DD} = 2.5V ±0.2V

AC Characteristics		-6T (TSOP)			
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Notes**
Write recovery time	^{t}WR	15	–	ns	
Internal WRITE-to-READ command delay	^{t}WTR	1	–	^{t}CK	
Exit SELF REFRESH-to-non-READ command 1Gb	^{t}XSNR	126	–	ns	
Exit SELF REFRESH-to-READ command	^{t}XSRD	200	–	^{t}CK	
Data valid output window	n/a	^{t}QH - ^{t}DQSQ		ns	26

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Table 17: Electrical Characteristics and Recommended AC Operating Conditions (-75)

Notes: 1–6, 16–18, and 34 apply to the entire table; Notes appear on page 26;
$0°C \le T_A \le 70°C$; V_{DDQ} = 2.5V ±0.2V, V_{DD} = 2.5V ±0.2V

AC Characteristics			-75			
Parameter		**Symbol**	**Min**	**Max**	**Units**	**Notes**
Access window of DQ from CK/CK#		^tAC	–0.75	0.75	ns	
CK high-level width		^tCH	0.45	0.55	^tCK	31
Clock cycle time	CL = 2.5	^tCK (2.5)	7.5	13	ns	46
	CL = 2	^tCK (2)	10	13	ns	46
CK low-level width		^tCL	0.45	0.55	^tCK	31
DQ and DM input hold time relative to DQS		^tDH	0.5	–	ns	27, 32
DQ and DM input pulse width (for each input)		^tDIPW	1.75	–	ns	32
Access window of DQS from CK/CK#		^tDQSCK	–0.75	0.75	ns	
DQS input high pulse width		^tDQSH	0.35	–	^tCK	
DQS input low pulse width		^tDQSL	0.35	–	^tCK	
DQS–DQ skew, DQS to last DQ valid, per group, per access		^tDQSQ	–	0.5	ns	26, 27
WRITE command-to-first DQS latching transition		^tDQSS	0.75	1.25	^tCK	
DQ and DM input setup time relative to DQS		^tDS	0.5	–	ns	27, 32
DQS falling edge from CK rising – hold time		^tDSH	0.2	–	^tCK	
DQS falling edge to CK rising – setup time		^tDSS	0.2	–	^tCK	
Half-clock period		^tHP	^tCH,^tCL	–	ns	35
Data-out High-Z window from CK/CK#		^tHZ	–	0.75	ns	19, 43
Address and control input hold time (fast slew rate)		^tIH_F	0.90	–	ns	
Address and control input hold time (slow slew rate)		^tIH_S	1	–	ns	15
Address and control input pulse width (for each input)		^tIPW	2.2	–	ns	
Address and control input setup time (fast slew rate)		^tIS_F	0.90	–	ns	
Address and control input setup time (slow slew rate)		^tIS_S	1	–	ns	15
Data-out Low-Z window from CK/CK#		^tLZ	–0.75	–	ns	19, 43
LOAD MODE REGISTER command cycle time		^tMRD	15	–	ns	
DQ–DQS hold, DQS to first DQ to go non-valid, per access		^tQH	^tHP -^tQHS	–	ns	26, 27
Data hold skew factor		^tQHS	–	0.75	ns	
ACTIVE-to-READ with auto precharge command		^tRAP	20	–	ns	
ACTIVE-to-PRECHARGE command		^tRAS	40	120,000	ns	36
ACTIVE-to-ACTIVE/AUTO REFRESH command period		^tRC	65	–	ns	55
ACTIVE-to-READ or WRITE delay		^tRCD	20	–	ns	
REFRESH-to-REFRESH command interval		^tREFC	–	70.3	µs	24
Average periodic refresh interval		^tREFI	–	7.8	µs	24
AUTO REFRESH command period	1Gb	^tRFC	120	–	ns	50
PRECHARGE command period		^tRP	20	–	ns	
DQS read preamble		^tRPRE	0.9	1.1	tCK	44
DQS read postamble		^tRPST	0.4	0.6	tCK	44
ACTIVE bank a to ACTIVE bank b command		^tRRD	15	–	ns	
Terminating voltage delay to V_{DD}		^tVTD	0	–	ns	
DQS write preamble		^tWPRE	0.25	–	tCK	
DQS write preamble setup time		^tWPRES	0	–	ns	21, 22
DQS write postamble		tWPST	0.4	0.6	tCK	20
Write recovery time		tWR	15	–	ns	

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Table 17: Electrical Characteristics and Recommended AC Operating Conditions (-75) (continued)
Notes: 1–6, 16–18, and 34 apply to the entire table; Notes appear on page 26;
0°C ≤ T_A ≤ 70°C; V_{DDQ} = 2.5V ±0.2V, V_{DD} = 2.5V ±0.2V

AC Characteristics			-75			
Parameter		Symbol	Min	Max	Units	Notes
Internal WRITE-to-READ command delay		^tWTR	1	–	^tCK	
Exit SELF REFRESH-to-non-READ command	1Gb	^tXSNR	127.5	–	ns	
Exit SELF REFRESH-to-READ command		^tXSRD	200	–	^tCK	
Data valid output window		n/a	^tQH - ^tDQSQ		ns	26

Table 18: Input Slew Rate Derating Values for Addresses and Commands
Note: 15 applies to the entire table; Notes appear on page 26;
0°C ≤ T_A ≤ 70°C; V_{DDQ} = 2.5V ±0.2V, V_{DD} = 2.5V ±0.2V

Speed	Slew Rate	^tIS	^tIH	Units
-75	0.500 V/ns	1.00	1	ns
-75	0.400 V/ns	1.05	1	ns
-75	0.300 V/ns	1.10	1	ns

Table 19: Input Slew Rate Derating Values for DQ, DQS, and DM
Note: 32 applies to the entire table; Notes appear on page 26;
0°C ≤ T_A ≤ 70°C; V_{DDQ} = 2.5V ±0.2V, V_{DD} = 2.5V ±0.2V

Speed	Slew Rate	^tDS	^tDH	Units
-75	0.500 V/ns	0.50	0.50	ns
-75	0.400 V/ns	0.55	0.55	ns
-75	0.300 V/ns	0.60	0.60	ns

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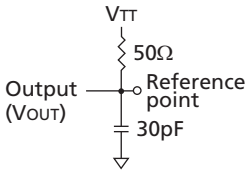
Notes

1. All voltages referenced to V_{SS}.
2. Tests for AC timing, I_{DD}, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and the device operation are guaranteed for the full voltage range specified.
3. Outputs (except for I_{DD} measurements) measured with equivalent load:



4. AC timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF}(or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1 V/ns in the range between $V_{IL(AC)}$ and $V_{IH(AC)}$.
5. The AC and DC input level specifications are as defined in the SSTL_2 standard (that is, the receiver will effectively switch as a result of the signal crossing the AC input level and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. All speed grades are not offered on all densities. Refer to page 1 for availability.
7. V_{REF} is expected to equal $V_{DDQ}/2$ of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (noncommon mode) on V_{REF} may not exceed ±2% of the DC value. Thus, from $V_{DDQ}/2$, V_{REF} is allowed ±25mV for DC error and an additional ±25mV for AC noise. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
8. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, it is expected to be set equal to V_{REF}, and it must track variations in the DC level of V_{REF}.
9. V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK#.
10. The value of V_{IX} and V_{MP} is expected to equal $V_{DDQ}/2$ of the transmitting device and must track variations in the DC level of the same.
11. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle times at CL = 3 for -5B; CL = 2.5, -6T/-75 speeds with the outputs open.
12. Enables on-chip refresh and address counters.
13. I_{DD} specifications are tested after the device is properly initialized and is averaged at the defined cycle rate.
14. This parameter is sampled. V_{DD} = 2.5V ±0.2V, V_{DDQ} = 2.5V ±0.2V, $V_{REF} = V_{SS}$, f = 100 MHz, T_A = 25°C, $V_{OUT(DC)} = V_{DDQ}/2$, V_{OUT} (peak-to-peak) = 0.2V. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
15. For slew rates less than 1 V/ns and greater than or equal to 0.5 V/ns. If the slew rate is less than 0.5 V/ns, timing must be derated: ^{t}IS has an additional 50ps per each 100 mV/ns reduction in slew rate from the 500 mV/ns. ^{t}IH has 0ps added, that is, it remains constant. If the slew rate exceeds 4.5 V/ns, functionality is uncertain. For -5B and -6T, slew rates must be greater than or equal to 0.5 V/ns.

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16. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross; the input reference level for signals other than CK/CK# is V_{REF}.
17. Inputs are not recognized as valid until V_{REF} stabilizes. Once initialized, including self refresh mode, V_{REF} must be powered within specified range. Exception: during the period before V_{REF} stabilizes, CKE < 0.3 × V_{DD} is recognized as LOW.
18. The output timing reference level, as measured at the timing reference point (indicated in Note 3), is V_{TT}.
19. ^{t}HZ and ^{t}LZ transitions occur in the same access time windows as data valid transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (High-Z) or begins driving (Low-Z).
20. The intent of the "Don't Care" state after completion of the postamble is the DQS-driven signal should either be HIGH, LOW, or High-Z, and that any signal transition within the input switching region must follow valid input requirements. That is, if DQS transitions HIGH (above $V_{IH(DC)min}$) then it must not transition LOW (below $V_{IH(DC)}$ prior to ^{t}DQSH [MIN]).
21. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
22. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on ^{t}DQSS.
23. MIN (^{t}RC or ^{t}RFC) for I_{DD} measurements is the smallest multiple of ^{t}CK that meets the minimum absolute value for the respective parameter. ^{t}RAS (MAX) for I_{DD} measurements is the largest multiple of ^{t}CK that meets the maximum absolute value for ^{t}RAS.
24. The refresh period is 64ms. This equates to an average refresh rate of 7.8125µs. However, an AUTO REFRESH command must be asserted at least once every 70.3µs; burst refreshing or posting by the DRAM controller greater than 8 REFRESH cycles is not allowed.
25. The I/O capacitance per DQS and DQ byte/group will not differ by more than this maximum amount for any given device.
26. The data valid window is derived by achieving other specifications: ^{t}HP (^{t}CK/2), ^{t}DQSQ, and ^{t}QH (^{t}QH = ^{t}HP - ^{t}QHS). The data valid window derates in direct proportion to the clock duty cycle and a practical data valid window can be derived. The clock is allowed a maximum duty cycle variation of 45/55, because functionality is uncertain when operating beyond a 45/55 ratio. The data valid window derating curves are provided in Figure 10 on page 28 for duty cycles ranging between 50/50 and 45/55.
27. Referenced to each output group: x4 = DQS with DQ[3:0]; x8 = DQS with DQ[7:0]; x16 = LDQS with DQ[7:0] and UDQS with DQ[15:8].
28. This limit is actually a nominal value and does not result in a fail value. CKE is HIGH during the REFRESH command period (^{t}RFC [MIN]), else CKE is LOW (that is, during standby).
29. To maintain a valid level, the transitioning edge of the input must:
    - 29a. Sustain a constant slew rate from the current AC level through to the target AC level, $V_{IL(AC)}$ or $V_{IH(AC)}$.
    - 29b. Reach at least the target AC level.
    - 29c. After the AC target level is reached, continue to maintain at least the target DC level, $V_{IL(DC)}$ or $V_{IH(DC)}$.

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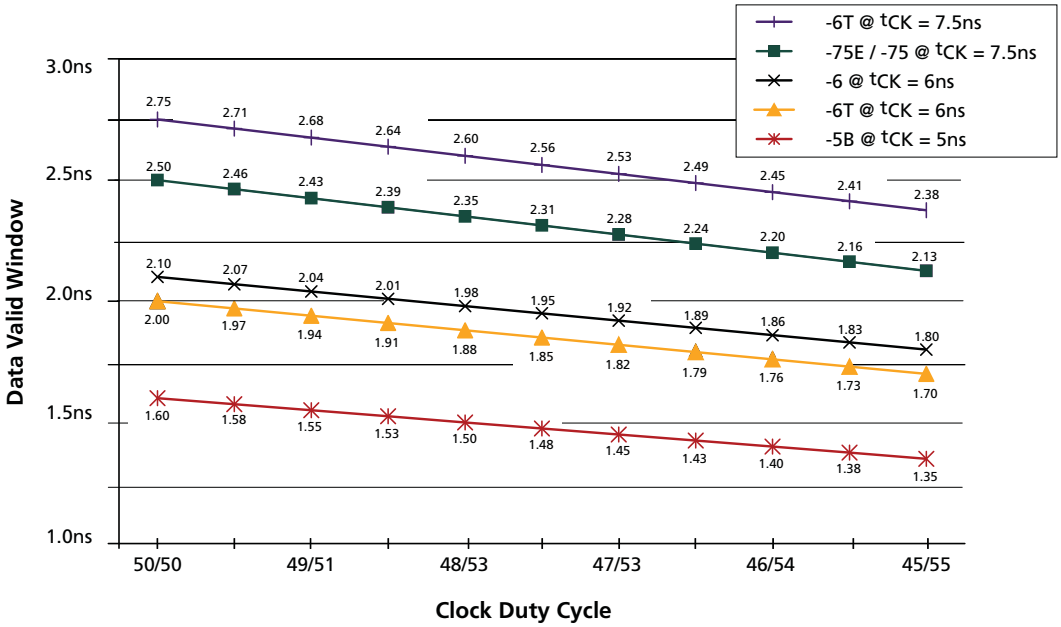
30. The input capacitance per pin group will not differ by more than this maximum amount for any given device.
31. CK and CK# input slew rate must be ≥1 V/ns (≥2 V/ns if measured differentially).

Figure 10: Derating Data Valid Window (^{t}QH – ^{t}DQSQ)



32. DQ and DM input slew rates must not deviate from DQS by more than 10%. If the DQ/DM/DQS slew rate is less than 0.5 V/ns, timing must be derated: 50ps must be added to ^{t}DS and ^{t}DH for each 100 mV/ns reduction in slew rate. For -5B and -6T speed grades, the slew rate must be ≥0.5 V/ns. If the slew rate exceeds 4 V/ns, functionality is uncertain.
33. V_{DD} must not vary more than 4% if CKE is not active while any bank is active.
34. The clock is allowed up to ±150ps of jitter. Each timing parameter is allowed to vary by the same amount.
35. ^{t}HP (MIN) is the lesser of ^{t}CL (MIN) and ^{t}CH (MIN) actually applied to the device CK and CK# inputs, collectively, during bank active.
36. READs and WRITEs with auto precharge are not allowed to be issued until ^{t}RAS (MIN) can be satisfied prior to the internal PRECHARGE command being issued.
37. Any positive glitch must be less than 1/3 of the clock cycle and not more than 400mV or 2.9V (300mV or 2.9V maximum for -5B), whichever is less. Any negative glitch must be less than 1/3 of the clock cycle and not exceed either –300mV or 2.2V (2.4V for -5B), whichever is more positive. The average cannot be below the 2.5V (2.6V for -5B) minimum.
38. Normal output drive curves:
    38a. The full driver pull-down current variation from MIN to MAX process; temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 11 on page 29.
    38b. The driver pull-down current variation, within nominal voltage and temperature limits, is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 11 on page 29.

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38c. The full driver pull-up current variation from MIN to MAX process; temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 12 on page 29.

38d. The driver pull-up current variation within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 12 on page 29.

38e. The full ratio variation of MAX to MIN pull-up and pull-down current should be between 0.71 and 1.4 for drain-to-source voltages from 0.1V to 1.0V at the same voltage and temperature.

38f. The full ratio variation of the nominal pull-up to pull-down current should be unity ±10% for device drain-to-source voltages from 0.1V to 1.0V.

Figure 11: Full Drive Pull-Down Characteristics

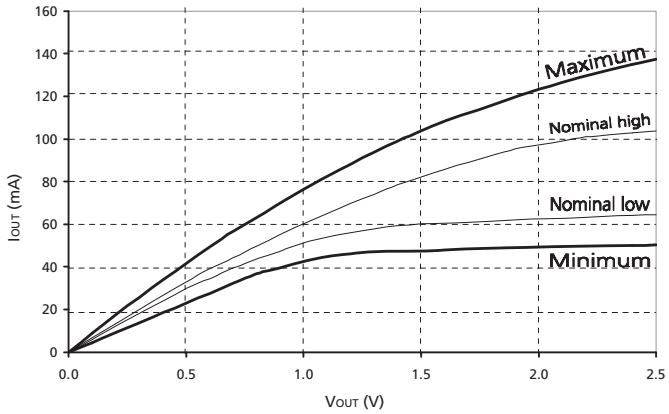
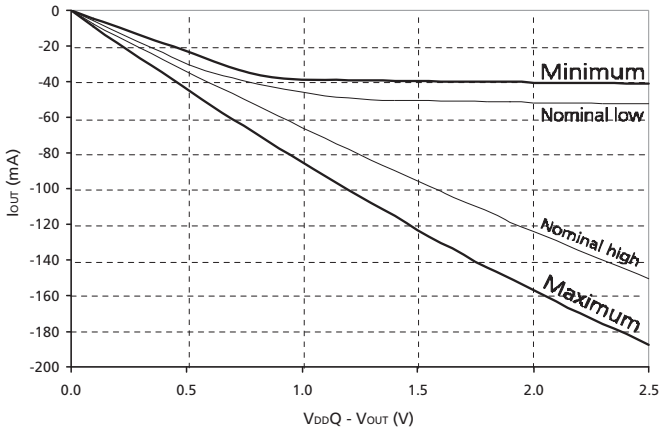


Figure 12: Full Drive Pull-Up Characteristics



39. Reduced output drive curves:

39a. The full driver pull-down current variation from MIN to MAX process; temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 13 on page 30.

39b. The driver pull-down current variation, within nominal voltage and temperature limits, is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 13 on page 30.

39c. The full driver pull-up current variation from MIN to MAX process; temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 14.

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39d. The driver pull-up current variation, within nominal voltage and temperature limits, is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 14 on page 30.

39e. The full ratio variation of the MAX-to-MIN pull-up and pull-down current should be between 0.71 and 1.4 for device drain-to-source voltages from 0.1V to 1.0V at the same voltage and temperature.

39f. The full ratio variation of the nominal pull-up to pull-down current should be unity ±10%, for device drain-to-source voltages from 0.1V to 1.0V.

Figure 13: Reduced Drive Pull-Down Characteristics

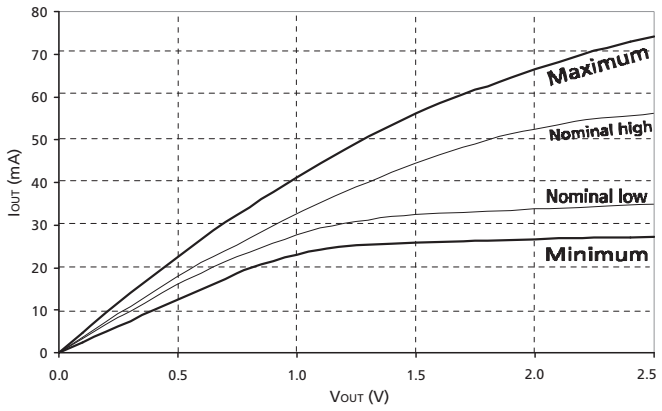
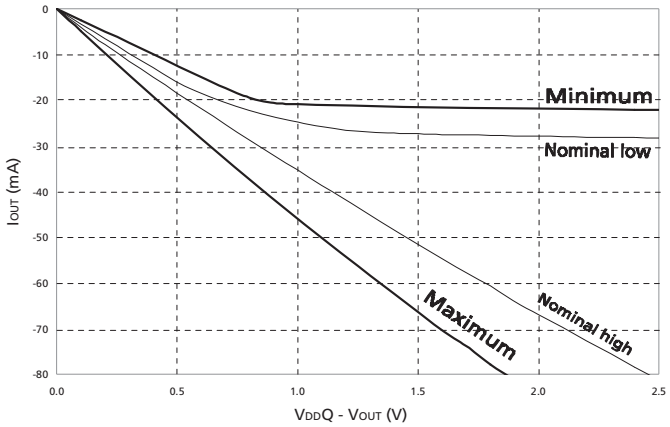


Figure 14: Reduced Drive Pull-Up Characteristics



40. The voltage levels used are derived from a minimum V_{DD} level and the referenced test load. In practice, the voltage levels obtained from a properly terminated bus will provide significantly different voltage values.

41. V_{IH} overshoot: $V_{IH,max} = V_{DDQ} + 1.5V$ for a pulse width ≤ 3ns, and the pulse width can not be greater than 1/3 of the cycle rate. V_{IL} undershoot: $V_{IL,min} = –1.5V$ for a pulse width ≤ 3ns, and the pulse width can not be greater than 1/3 of the cycle rate.

42. V_{DD} and V_{DDQ} must track each other.

43. ^{t}HZ (MAX) will prevail over $^{t}DQSCK$ (MAX) + $^{t}RPST$ (MAX) condition. ^{t}LZ (MIN) will prevail over $^{t}DQSCK$ (MIN) + $^{t}RPRE$ (MAX) condition.

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44. ^{t}RPST end point and ^{t}RPRE begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (^{t}RPST) or begins driving (^{t}RPRE).
45. During initialization, V_{DDQ}, V_{TT}, and V_{REF} must be equal to or less than V_{DD} + 0.3V. Alternatively, V_{TT} may be 1.35V maximum during power-up, even if V_{DD}/V_{DDQ} are 0V, provided a minimum of 42Ω of series resistance is used between the V_{TT} supply and the input pin.
46. The current Micron part operates below 83 MHz (slowest specified JEDEC operating frequency). As such, future die may not reflect this option.
47. When an input signal is HIGH or LOW, it is defined as a steady state logic HIGH or LOW.
48. Random address is changing; 50% of data is changing at every transfer.
49. Random address is changing; 100% of data is changing at every transfer.
50. CKE must be active (HIGH) during the entire time a REFRESH command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge, until ^{t}RFC has been satisfied.
51. I_{DD2N} specifies the DQ, DQS, and DM to be driven to a valid HIGH or LOW logic level. I_{DD2Q} is similar to I_{DD2F} except I_{DD2Q} specifies the address and control inputs to remain stable. Although I_{DD2F}, I_{DD2N}, and I_{DD2Q} are similar, I_{DD2F} is "worst case."
52. Whenever the operating frequency is altered, not including jitter, the DLL is required to be reset followed by 200 clock cycles before any READ command.
53. This is the DC voltage supplied at the DRAM and is inclusive of all noise up to 20 MHz. Any noise above 20 MHz at the DRAM generated from any source other than that of the DRAM itself may not exceed the DC voltage range of 2.6V ±100mV.
54. The -6T speed grade will operate with ^{t}RAS (MIN) = 40ns and ^{t}RAS (MAX) = 120,000ns at any slower frequency.
55. DRAM devices should be evenly addressed when being accessed. Disproportionate accesses to a particular row address may result in reduction of the product lifetime.

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Table 20: Normal Output Drive Characteristics

Characteristics are specified under best, worst, and nominal process variation/conditions

Voltage (V)	Pull-Down Current (mA)				Pull-Up Current (mA)			
	Nominal Low	Nominal High	Min	Max	Nominal Low	Nominal High	Min	Max
0.1	6.0	6.8	4.6	9.6	–6.1	–7.6	–4.6	–10.0
0.2	12.2	13.5	9.2	18.2	–12.2	–14.5	–9.2	–20.0
0.3	18.1	20.1	13.8	26.0	–18.1	–21.2	–13.8	–29.8
0.4	24.1	26.6	18.4	33.9	–24.0	–27.7	–18.4	–38.8
0.5	29.8	33.0	23.0	41.8	–29.8	–34.1	–23.0	–46.8
0.6	34.6	39.1	27.7	49.4	–34.3	–40.5	–27.7	–54.4
0.7	39.4	44.2	32.2	56.8	–38.1	–46.9	–32.2	–61.8
0.8	43.7	49.8	36.8	63.2	–41.1	–53.1	–36.0	–69.5
0.9	47.5	55.2	39.6	69.9	–43.8	–59.4	–38.2	–77.3
1.0	51.3	60.3	42.6	76.3	–46.0	–65.5	–38.7	–85.2
1.1	54.1	65.2	44.8	82.5	–47.8	–71.6	–39.0	–93.0
1.2	56.2	69.9	46.2	88.3	–49.2	–77.6	–39.2	–100.6
1.3	57.9	74.2	47.1	93.8	–50.0	–83.6	–39.4	–108.1
1.4	59.3	78.4	47.4	99.1	–50.5	–89.7	–39.6	–115.5
1.5	60.1	82.3	47.7	103.8	–50.7	–95.5	–39.9	–123.0
1.6	60.5	85.9	48.0	108.4	–51.0	–101.3	–40.1	–130.4
1.7	61.0	89.1	48.4	112.1	–51.1	–107.1	–40.2	–136.7
1.8	61.5	92.2	48.9	115.9	–51.3	–112.4	–40.3	–144.2
1.9	62.0	95.3	49.1	119.6	–51.5	–118.7	–40.4	–150.5
2.0	62.5	97.2	49.4	123.3	–51.6	–124.0	–40.5	–156.9
2.1	62.8	99.1	49.6	126.5	–51.8	–129.3	–40.6	–163.2
2.2	63.3	100.9	49.8	129.5	–52.0	–134.6	–40.7	–169.6
2.3	63.8	101.9	49.9	132.4	–52.2	–139.9	–40.8	–176.0
2.4	64.1	102.8	50.0	135.0	–52.3	–145.2	–40.9	–181.3
2.5	64.6	103.8	50.2	137.3	–52.5	–150.5	–41.0	–187.6
2.6	64.8	104.6	50.4	139.2	–52.7	–155.3	–41.1	–192.9
2.7	65.0	105.4	50.5	140.8	–52.8	–160.1	–41.2	–198.2

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Table 21: Reduced Output Drive Characteristics

Characteristics are specified under best, worst, and nominal process variation/conditions

Voltage (V)	Pull-Down Current (mA)				Pull-Up Current (mA)			
	Nominal Low	Nominal High	Min	Max	Nominal Low	Nominal High	Min	Max
0.1	3.4	3.8	2.6	5.0	–3.5	–4.3	–2.6	–5.0
0.2	6.9	7.6	5.2	9.9	–6.9	–7.8	–5.2	–9.9
0.3	10.3	11.4	7.8	14.6	–10.3	–12.0	–7.8	–14.6
0.4	13.6	15.1	10.4	19.2	–13.6	–15.7	–10.4	–19.2
0.5	16.9	18.7	13.0	23.6	–16.9	–19.3	–13.0	–23.6
0.6	19.9	22.1	15.7	28.0	–19.4	–22.9	–15.7	–28.0
0.7	22.3	25.0	18.2	32.2	–21.5	–26.5	–18.2	–32.2
0.8	24.7	28.2	20.8	35.8	–23.3	–30.1	–20.4	–35.8
0.9	26.9	31.3	22.4	39.5	–24.8	–33.6	–21.6	–39.5
1.0	29.0	34.1	24.1	43.2	–26.0	–37.1	–21.9	–43.2
1.1	30.6	36.9	25.4	46.7	–27.1	–40.3	–22.1	–46.7
1.2	31.8	39.5	26.2	50.0	–27.8	–43.1	–22.2	–50.0
1.3	32.8	42.0	26.6	53.1	–28.3	–45.8	–22.3	–53.1
1.4	33.5	44.4	26.8	56.1	–28.6	–48.4	–22.4	–56.1
1.5	34.0	46.6	27.0	58.7	–28.7	–50.7	–22.6	–58.7
1.6	34.3	48.6	27.2	61.4	–28.9	–52.9	–22.7	–61.4
1.7	34.5	50.5	27.4	63.5	–28.9	–55.0	–22.7	–63.5
1.8	34.8	52.2	27.7	65.6	–29.0	–56.8	–22.8	–65.6
1.9	35.1	53.9	27.8	67.7	–29.2	–58.7	–22.9	–67.7
2.0	35.4	55.0	28.0	69.8	–29.2	–60.0	–22.9	–69.8
2.1	35.6	56.1	28.1	71.6	–29.3	–61.2	–23.0	–71.6
2.2	35.8	57.1	28.2	73.3	–29.5	–62.4	–23.0	–73.3
2.3	36.1	57.7	28.3	74.9	–29.5	–63.1	–23.1	–74.9
2.4	36.3	58.2	28.3	76.4	–29.6	–63.8	–23.2	–76.4
2.5	36.5	58.7	28.4	77.7	–29.7	–64.4	–23.2	–77.7
2.6	36.7	59.2	28.5	78.8	–29.8	–65.1	–23.3	–78.8
2.7	36.8	59.6	28.6	79.7	–29.9	–65.8	–23.3	–79.7

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Commands

Tables 22 and 23 provide a quick reference of available commands. Two additional Truth Tables—Table 24 on page 35 and Table 25 on page 36—provide current state/next state information.

Table 22: Truth Table 1 – Commands

CKE is HIGH for all commands shown except SELF REFRESH; All states and sequences not shown are illegal or reserved

Function	CS#	RAS#	CAS#	WE#	Address	Notes
DESELECT	H	X	X	X	X	1
NO OPERATION (NOP)	L	H	H	H	X	1
ACTIVE (select bank and activate row)	L	L	H	H	Bank/row	2
READ (select bank and column and start READ burst)	L	H	L	H	Bank/col	3
WRITE (select bank and column and start WRITE burst)	L	H	L	L	Bank/col	3
BURST TERMINATE	L	H	H	L	X	4
PRECHARGE (deactivate row in bank or banks)	L	L	H	L	Code	5
AUTO REFRESH or SELF REFRESH (enter self refresh mode)	L	L	L	H	X	6, 7
LOAD MODE REGISTER	L	L	L	L	Op-code	8

Notes:
1. DESELECT and NOP are functionally interchangeable.
2. BA[1:0] provide bank address and A[*n*:0] (128Mb: *n* = 11; 256Mb and 512Mb: *n* = 12; 1Gb: *n* = 13) provide row address.
3. BA[1:0] provide bank address; A[*i*:0] provide column address, (where A*i* is the most significant column address bit for a given density and configuration, see Table 2 on page 2) A10 HIGH enables the auto precharge feature (non persistent), and A10 LOW disables the auto precharge feature.
4. Applies only to READ bursts with auto precharge disabled; this command is undefined (and should not be used) for READ bursts with auto precharge enabled and for WRITE bursts.
5. A10 LOW: BA[1:0] determine which bank is precharged. A10 HIGH: all banks are precharged and BA[1:0] are "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH; SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing while in self refresh mode, all inputs and I/Os are "Don't Care" except for CKE.
8. BA[1:0] select either the mode register or the extended mode register (BA0 = 0, BA1 = 0 select the mode register; BA0 = 1, BA1 = 0 select extended mode register; other combinations of BA[1:0] are reserved). A[*n*:0] provide the op-code to be written to the selected mode register.

Table 23: Truth Table 2 – DM Operation

Used to mask write data, provided coincident with the corresponding data

Name (Function)	DM	DQ
Write enable	L	Valid
Write inhibit	H	X

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Table 24: Truth Table 3 – Current State Bank *n* – Command to Bank *n*

Notes: 1–6 apply to the entire table; Notes appear below

Current State	CS#	RAS#	CAS#	WE#	Command/Action	Notes
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVE (select and activate row)	
	L	L	L	H	AUTO REFRESH	7
	L	L	L	L	LOAD MODE REGISTER	7
Row active	L	H	L	H	READ (select column and start READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	8
Read (auto precharge disabled)	L	H	L	H	READ (select column and start new READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst)	10, 12
	L	L	H	L	PRECHARGE (truncate READ burst, start PRECHARGE)	8
	L	H	H	L	BURST TERMINATE	9
Write (auto precharge disabled)	L	H	L	H	READ (select column and start READ burst)	10, 11
	L	H	L	L	WRITE (select column and start new WRITE burst)	10
	L	L	H	L	PRECHARGE (truncate WRITE burst, start PRECHARGE)	8, 11

Notes:
1. This table applies when CKE_{n-1} was HIGH and CKE_n is HIGH (see Table 27 on page 38) and after ^{t}XSNR has been met (if the previous state was self refresh).
2. This table is bank-specific, except where noted (that is, the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state). Exceptions are covered in the notes below.
3. Current state definitions:
   - Idle: The bank has been precharged, and ^{t}RP has been met.
   - Row active: A row in the bank has been activated, and ^{t}RCD has been met. No data bursts/accesses and no register accesses are in progress.
   - Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
   - Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
4. The following states must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Table 24 and according to Table 25 on page 36.
   - Precharging: Starts with registration of a PRECHARGE command and ends when ^{t}RP is met. Once ^{t}RP is met, the bank will be in the idle state.
   - Row activating: Starts with registration of an ACTIVE command and ends when ^{t}RCD is met. Once ^{t}RCD is met, the bank will be in the "row active" state.
   - Read with auto precharge enabled: Starts with registration of a READ command with auto precharge enabled and ends when ^{t}RP has been met. Once ^{t}RP is met, the bank will be in the idle state.
   - Write with auto precharge enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when ^{t}RP has been met. Once ^{t}RP is met, the bank will be in the idle state.
5. The following states must not be interrupted by any executable command; COMMAND INHIBIT or NOP commands must be applied on each positive clock edge during these states.

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- Refreshing: Starts with registration of an AUTO REFRESH command and ends when ^{t}RFC is met. After ^{t}RFC is met, the DDR SDRAM will be in the all banks idle state.
- Accessing mode register: Starts with registration of an LMR command and ends when ^{t}MRD has been met. After ^{t}MRD is met, the DDR SDRAM will be in the all banks idle state.
- Precharging all: Starts with registration of a PRECHARGE ALL command and ends when ^{t}RP is met. After ^{t}RP is met, all banks will be in the idle state.

6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle, and bursts are not in progress.
8. May or may not be bank-specific; if multiple banks are to be precharged, each must be in a valid state for precharging.
9. Not bank-specific; BURST TERMINATE affects the most recent READ burst, regardless of bank.
10. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
11. Requires appropriate DM masking.
12. A WRITE command may be applied after the completion of the READ burst; otherwise, a BURST TERMINATE must be used to end the READ burst prior to asserting a WRITE command.

Table 25: Truth Table 4 – Current State Bank *n* – Command to Bank *m*
Notes: 1–6 apply to the entire table; Notes appear on page 36

Current State	CS#	RAS#	CAS#	WE#	Command/Action	Notes
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any command otherwise allowed to bank *m*	
Row activating, active, or precharging	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (auto precharge disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7, 9
	L	L	H	L	PRECHARGE	
Write (auto precharge disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 8
	L	H	L	L	WRITE (select column and start new WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (with auto-precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7, 9
	L	L	H	L	PRECHARGE	
Write (with auto-precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7
	L	H	L	L	WRITE (select column and start new WRITE burst)	7
	L	L	H	L	PRECHARGE	

Notes: 1. This table applies when CKE_{n-1} was HIGH and CKE_n is HIGH (see Table 27 on page 38) and after ^{t}XSNR has been met (if the previous state was self refresh).

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2. This table describes alternate bank operation, except where noted (that is, the current state is for bank *n*, and the commands shown are those allowed to be issued to bank *m*, assuming that bank *m* is in such a state that the given command is allowable). Exceptions are covered in the notes below.
3. Current state definitions:
   - Idle: The bank has been precharged, and ^{t}RP has been met.
   - Row active: A row in the bank has been activated, and ^{t}RCD has been met. No data bursts/accesses and no register accesses are in progress.
   - Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
   - Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
   - Read with auto precharge enabled: See note 3a below.
   - Write with auto precharge enabled: See note 3a below.
     a. The read with auto precharge enabled or write with auto precharge enabled states can each be broken into two parts: the access period and the precharge period. For read with auto precharge, the precharge period is defined as if the same burst was executed with auto precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For write with auto precharge, the precharge period begins when ^{t}WR ends, with ^{t}WR measured as if auto precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or ^{t}RP) begins. This device supports concurrent auto precharge such that when a read with auto precharge is enabled or a write with auto precharge is enabled, any command to other banks is allowed, as long as that command does not interrupt the read or write data transfer already in process. In either case, all other related limitations apply (for example, contention between read data and write data must be avoided).
     b. The minimum delay from a READ or WRITE command with auto precharge enabled, to a command to a different bank is summarized in Table 26.

Table 26: Command Delays

CL_{RU} = CL rounded up to the next integer

From Command	To Command	Minimum Delay with Concurrent Auto Precharge
WRITE with auto precharge	READ or READ with auto precharge	[1 + (BL/2)] × ^{t}CK + ^{t}WTR
	WRITE or WRITE with auto precharge	(BL/2) × ^{t}CK
	PRECHARGE	1 ^{t}CK
	ACTIVE	1 ^{t}CK
READ with auto precharge	READ or READ with auto precharge	(BL/2) × ^{t}CK
	WRITE or WRITE with auto precharge	[CL_{RU} + (BL/2)] × ^{t}CK
	PRECHARGE	1 ^{t}CK
	ACTIVE	1 ^{t}CK

4. AUTO REFRESH and LMR commands may only be issued when all banks are idle.
5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs listed in the "Command/Action" column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
8. Requires appropriate DM masking.
9. A WRITE command may be applied after the completion of the READ burst; otherwise, a BURST TERMINATE must be used to end the READ burst prior to asserting a WRITE command.

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Table 27: Truth Table 5 – CKE

Notes 1–6 apply to the entire table; Notes appear below

CKE_{n-1}	CKE_n	Current State	$Command_n$	$Action_n$	Notes
L	L	Power-down	X	Maintain power-down	
		Self refresh	X	Maintain self refresh	
L	H	Power-down	DESELECT or NOP	Exit power-down	
		Self refresh	DESELECT or NOP	Exit self refresh	7
H	L	All banks idle	DESELECT or NOP	Precharge power-down entry	
		Bank(s) active	DESELECT or NOP	Active power-down entry	
		All banks idle	AUTO REFRESH	Self refresh entry	
H	H		See Table 22 on page 34		

Notes:
1. CKE_n is the logic state of CKE at clock edge *n*; CKE_{n-1} was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR SDRAM immediately prior to clock edge *n*.
3. $COMMAND_n$ is the command registered at clock edge *n*, and $ACTION_n$ is a result of $COMMAND_n$.
4. All states and sequences not shown are illegal or reserved.
5. CKE must not drop LOW during a column access. For a READ, this means CKE must stay HIGH until after the read postamble time (^tRPST); for a WRITE, CKE must stay HIGH until the write recovery time (^tWR) has been met.
6. Once initialized, including during self refresh mode, V_{REF} must be powered within the specified range.
7. Upon exit of the self refresh mode, the DLL is automatically enabled. A minimum of 200 clock cycles is needed before applying a READ command for the DLL to lock. DESELECT or NOP commands should be issued on any clock edges occurring during the ^tXSNR period.

DESELECT

The DESELECT function (CS# HIGH) prevents new commands from being executed by the DDR SDRAM. The DDR SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct the selected DDR SDRAM to perform a NOP (CS# is LOW with RAS#, CAS#, and WE# are HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE REGISTER (LMR)

The mode registers are loaded via inputs A0–A*n* (see "REGISTER DEFINITION" on page 46). The LMR command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until ^tMRD is met.

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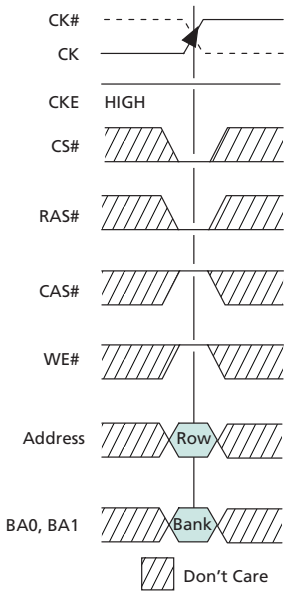
ACTIVE (ACT)

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access, like a read or a write, as shown in Figure 15. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A[*n*:0] selects the row.

Figure 15: Activating a Specific Row in a Specific Bank



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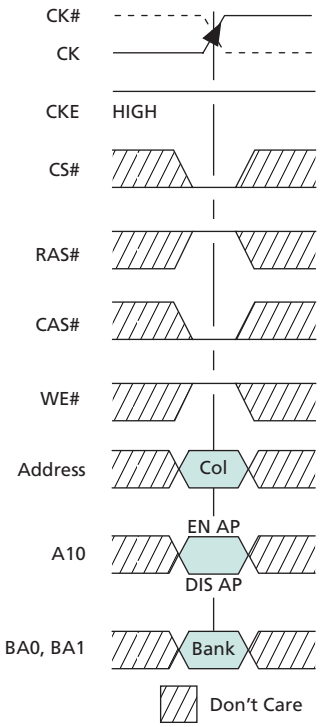
READ

The READ command is used to initiate a burst read access to an active row, as shown in Figure 16 on page 40. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A[*i*:0] (where A*i* is the most significant column address bit for a given density and configuration, see Table 2 on page 2) selects the starting column location.

Figure 16: READ Command



Note: EN AP = enable auto precharge; DIS AP = disable auto precharge.

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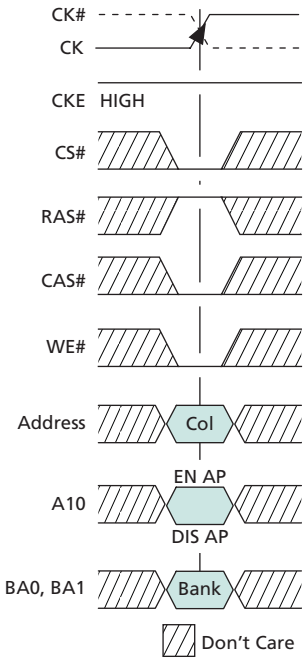
WRITE

The WRITE command is used to initiate a burst write access to an active row as shown in Figure 17. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A[*i*:0] (where A*i* is the most significant column address bit for a given density and configuration, see Table 2 on page 2) selects the starting column location.

Figure 17: WRITE Command



Note: EN AP = enable auto precharge; and DIS AP = disable auto precharge.

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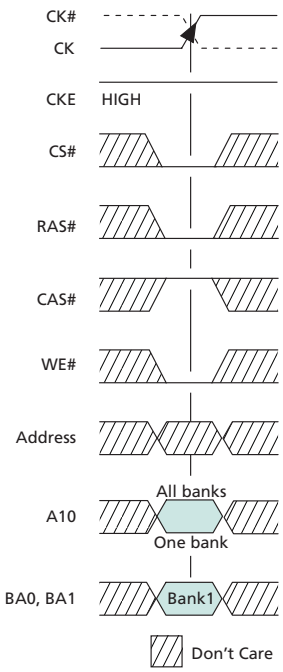
PRECHARGE (PRE)

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks as shown in Figure 18. The value on the BA0, BA1 inputs selects the bank, and the A10 input selects whether a single bank is precharged or whether all banks are precharged.

Figure 18: PRECHARGE Command



Notes: 1. If A10 is HIGH, bank address becomes "Don't Care."

BURST TERMINATE (BST)

The BURST TERMINATE command is used to truncate READ bursts (with auto precharge disabled). The most recently registered READ command prior to the BURST TERMINATE command will be truncated, as shown in "Operations" on page 43. The open page from which the READ burst was terminated remains open.

AUTO REFRESH (AR)

AUTO REFRESH is used during normal operation of the DDR SDRAM and is analogous to CAS#-before-RAS# (CBR) refresh in FPM/EDO DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required. All banks must be idle before an AUTO REFRESH command is issued.

SELF REFRESH

The SELF REFRESH command can be used to retain data in the DDR SDRAM, even if the rest of the system is powered down. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW).

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Operations

INITIALIZATION

Prior to normal operation, DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures, other than those specified, may result in undefined operation.

To ensure device operation, the DRAM must be initialized as described in the following steps:

1. Simultaneously apply power to V_{DD} and V_{DDQ}.
2. Apply V_{REF} and then V_{TT} power. V_{TT} must be applied after V_{DDQ} to avoid device latch-up, which may cause permanent damage to the device. Except for CKE, inputs are not recognized as valid until after V_{REF} is applied.
3. Assert and hold CKE at a LVCMOS logic LOW. Maintaining an LVCMOS LOW level on CKE during power-up is required to ensure that the DQ and DQS outputs will be in the High-Z state, where they will remain until driven in normal operation (by a read access).
4. Provide stable clock signals.
5. Wait at least 200µs.
6. Bring CKE HIGH, and provide at least one NOP or DESELECT command. At this point, the CKE input changes from a LVCMOS input to a SSTL_2 input only and will remain a SSTL_2 input unless a power cycle occurs.
7. Perform a PRECHARGE ALL command.
8. Wait at least ^{t}RP time; during this time NOPs or DESELECT commands must be given.
9. Using the LMR command, program the extended mode register (E0 = 0 to enable the DLL and E1 = 0 for normal drive; or E1 = 1 for reduced drive and E2–E*n* must be set to 0 [where *n* = most significant bit]).
10. Wait at least ^{t}MRD time; only NOPs or DESELECT commands are allowed.
11. Using the LMR command, program the mode register to set operating parameters and to reset the DLL. At least 200 clock cycles are required between a DLL reset and any READ command.
12. Wait at least ^{t}MRD time; only NOPs or DESELECT commands are allowed.
13. Issue a PRECHARGE ALL command.
14. Wait at least ^{t}RP time; only NOPs or DESELECT commands are allowed.
15. Issue an AUTO REFRESH command. This may be moved prior to step 13.
16. Wait at least ^{t}RFC time; only NOPs or DESELECT commands are allowed.
17. Issue an AUTO REFRESH command. This may be moved prior to step 13.
18. Wait at least ^{t}RFC time; only NOPs or DESELECT commands are allowed.
19. Although not required by the Micron device, JEDEC requires an LMR command to clear the DLL bit (set M8 = 0). If an LMR command is issued, the same operating parameters should be utilized as in step 11.
20. Wait at least ^{t}MRD time; only NOPs or DESELECT commands are supported.
21. At this point the DRAM is ready for any valid command. At least 200 clock cycles with CKE HIGH are required between step 11 (DLL RESET) and any READ command.

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Figure 19: INITIALIZATION Flow Diagram

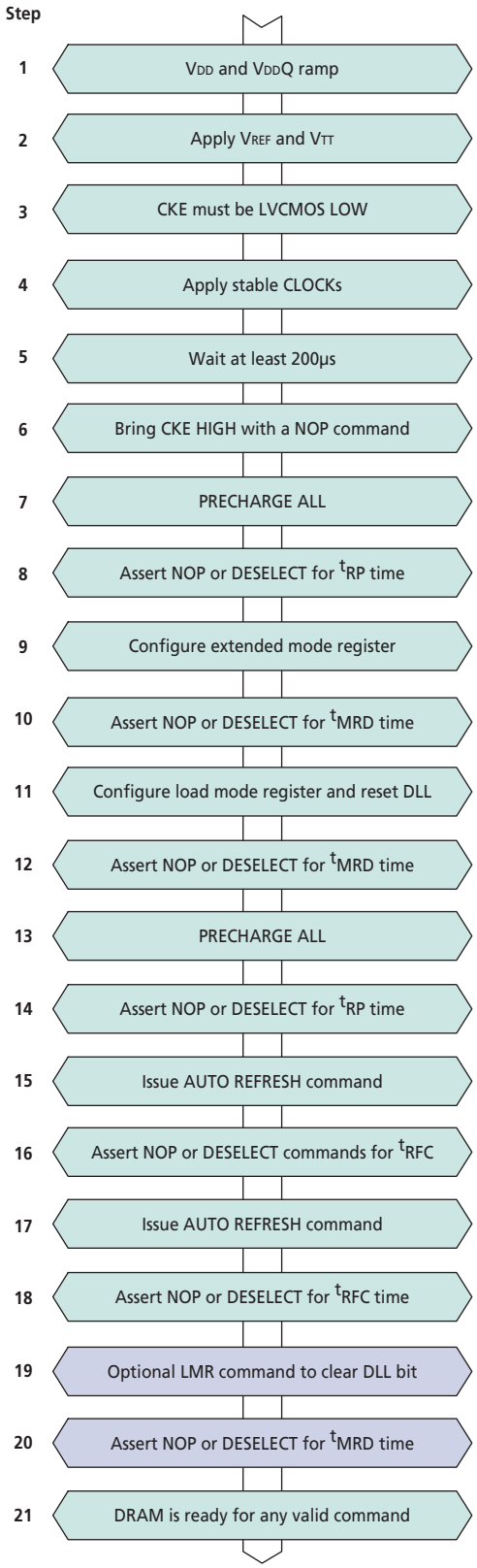

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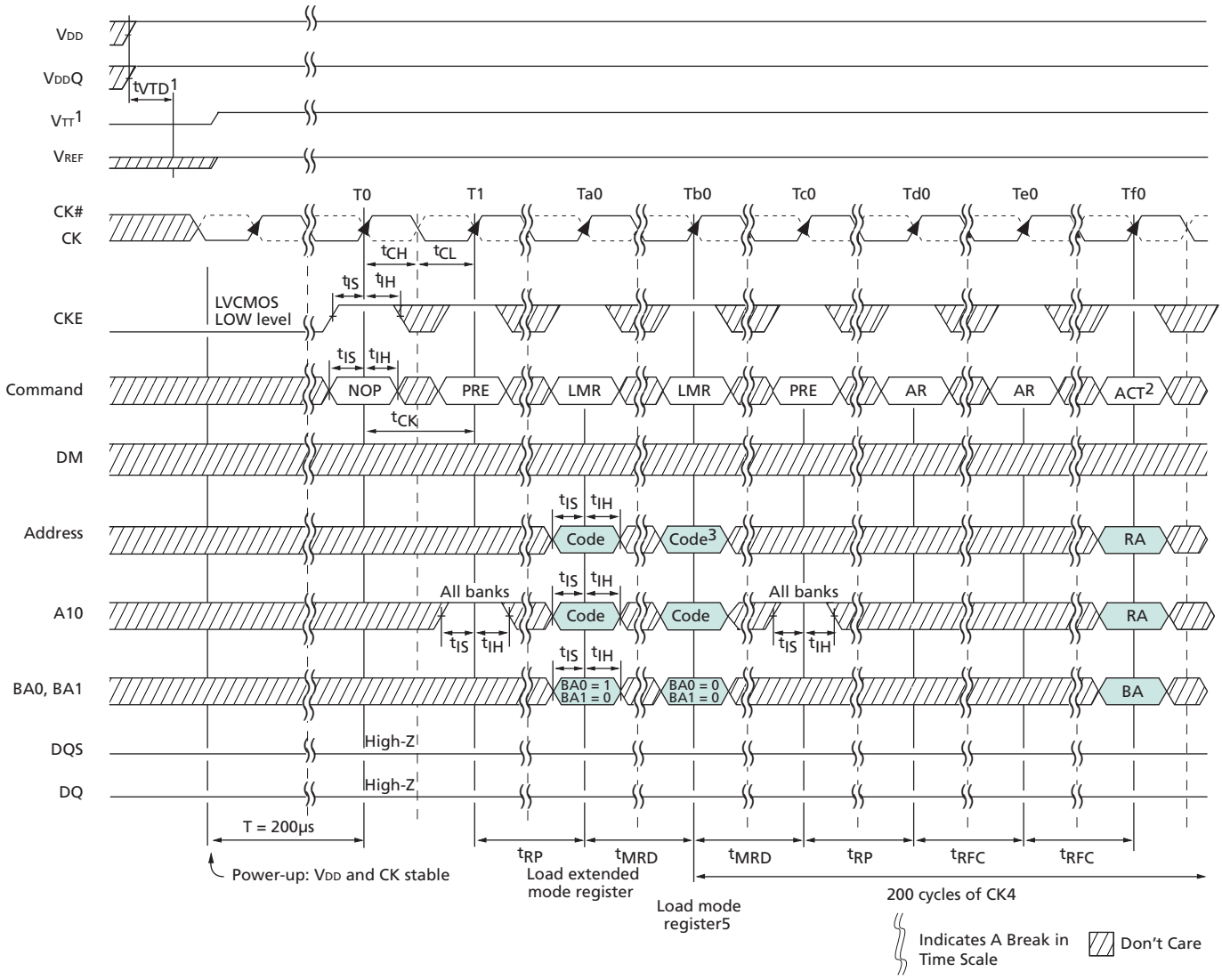
Figure 20: INITIALIZATION Timing Diagram



Notes:
1. V_{TT} is not applied directly to the device; however, $^{t}VTD \geq 0$ to avoid device latch-up. V_{DDQ}, V_{TT}, and $V_{REF} \leq V_{DD}$ + 0.3V. Alternatively, V_{TT} may be 1.35V maximum during power-up, even if V_{DD}/V_{DDQ} are 0V, provided a minimum of 42Ω of series resistance is used between the V_{TT} supply and the input pin. Once initialized, V_{REF} must always be powered within the specified range.
2. Although not required by the Micron device, JEDEC specifies issuing another LMR command (A8 = 0) prior to activating any bank. If another LMR command is issued, the same, previously issued operating parameters must be used.
3. The two AUTO REFRESH commands at Td0 and Te0 may be applied following the LMR command at Ta0.
4. ^{t}MRD is required before any command can be applied (during MRD time only NOPs or DESELECTs are allowed), and 200 cycles of CK are required before a READ command can be issued.
5. While programming the operating parameters, reset the DLL with A8 = 1.

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REGISTER DEFINITION

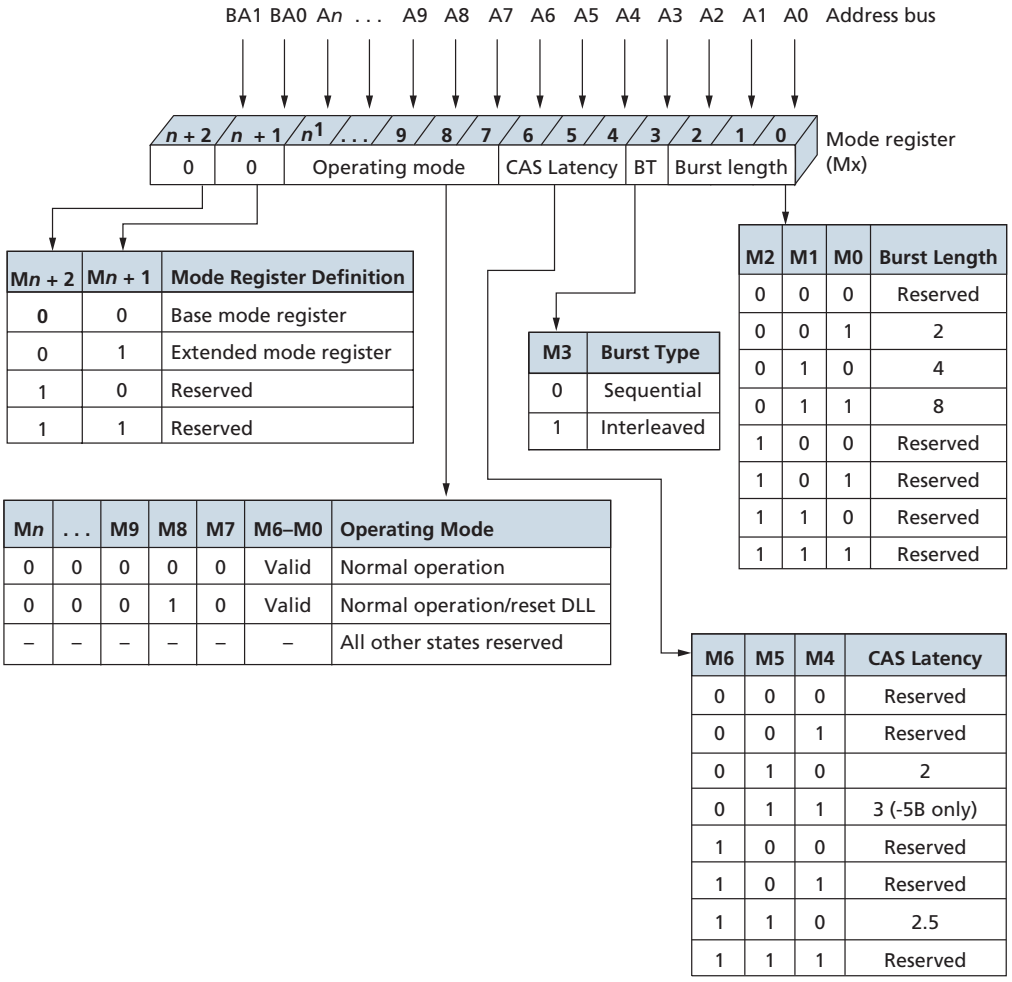
Mode Register

The mode register is used to define the specific DDR SDRAM mode of operation. This definition includes the selection of a burst length, a burst type, a CAS latency, and an operating mode, as shown in Figure 21. The mode register is programmed via the LMR command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again or until the device loses power (except for bit A8, which is self-clearing).

Reprogramming the mode register will not alter the contents of the memory, provided it is performed correctly. The mode register must be loaded (reloaded) when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Mode register bits A[2:0] specify the burst length, A3 specifies the type of burst (sequential or interleaved), A[6:4] specify the CAS latency, and A[*n*:7] specify the operating mode.

Figure 21: Mode Register Definition



Mn + 2	Mn + 1	Mode Register Definition
0	0	Base mode register
0	1	Extended mode register
1	0	Reserved
1	1	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

M2	M1	M0	Burst Length
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Mn	. . .	M9	M8	M7	M6–M0	Operating Mode
0	0	0	0	0	Valid	Normal operation
0	0	0	1	0	Valid	Normal operation/reset DLL
–	–	–	–	–	–	All other states reserved

M6	M5	M4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3 (-5B only)
1	0	0	Reserved
1	0	1	Reserved
1	1	0	2.5
1	1	1	Reserved

Notes: 1. *n* is the most significant row address bit from Table 2 on page 2.

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Burst Length (BL)

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable for both READ and WRITE bursts, as shown in Figure 21 on page 46. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. BL = 2, BL = 4, or BL = 8 locations are available for both the sequential and the interleaved burst types. Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block—meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A[*i*:1] when BL = 2, by A[*i*:2] when BL = 4, and by A[*i*:3] when BL = 8 (where A*i* is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. For example: for BL = 8, A[*i*:3]select the eight-data-element block; A[2:0] select the first access within the block.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address, as shown in Table 28.

Table 28: Burst Definition

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
2	–	–	**A0**	–	–
	–	–	0	0-1	0-1
	–	–	1	1-0	1-0
4	–	**A1**	**A0**	–	–
	–	0	0	0-1-2-3	0-1-2-3
	–	0	1	1-2-3-0	1-0-3-2
	–	1	0	2-3-0-1	2-3-0-1
	–	1	1	3-0-1-2	3-2-1-0
8	**A2**	**A1**	**A0**	–	–
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

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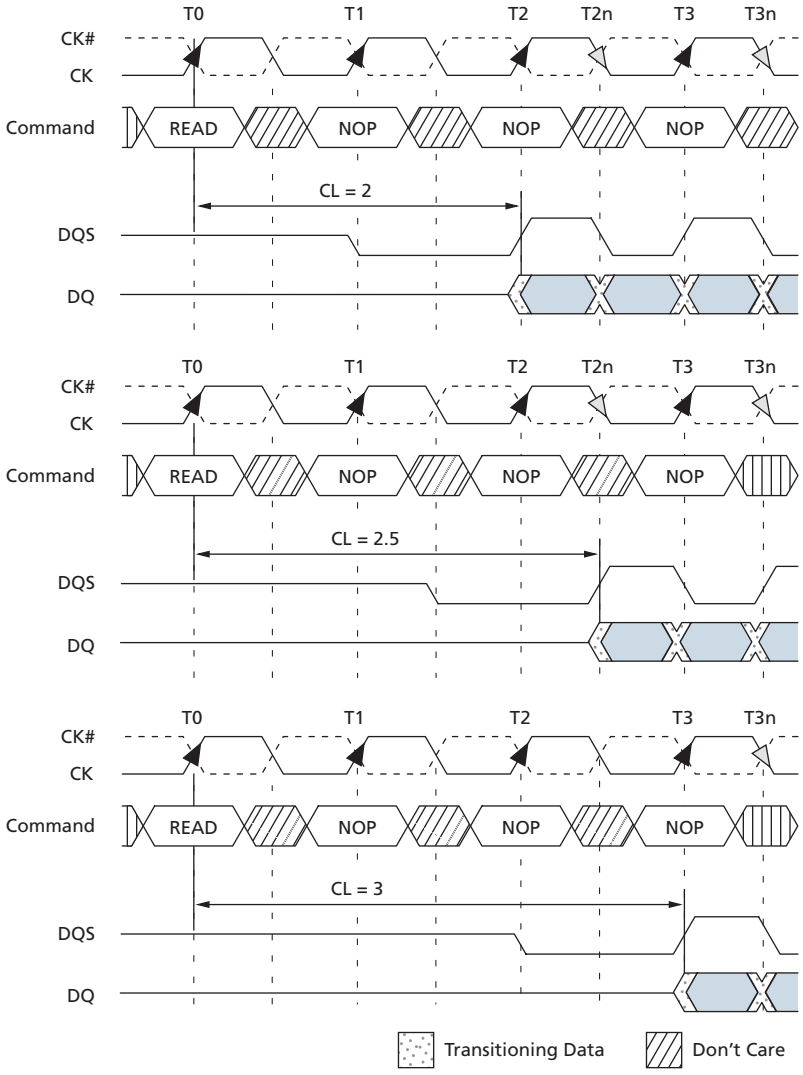
CAS Latency (CL)

The CL is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency can be set to 2, 2.5, or 3 (-5B only) clocks, as shown in Figure 22. Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available nominally coincident with clock edge *n* + *m*. Table 29 on page 49 indicates the operating frequencies at which each CL setting can be used.

Figure 22: CAS Latency



Note: BL = 4 in the cases shown; shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

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Table 29: CAS Latency

Speed	Allowable Operating Clock Frequency (MHz)		
	CL = 2	CL = 2.5	CL = 3
-5B	75 ≤ *f* ≤ 133	75 ≤ *f* ≤ 167	133 ≤ *f* ≤ 200
-6/-6T	75 ≤ *f* ≤ 133	75 ≤ *f* ≤ 167	–
-75E	75 ≤ *f* ≤ 133	75 ≤ *f* ≤ 133	–
-75Z	75 ≤ *f* ≤ 133	75 ≤ *f* ≤ 133	–
-75	75 ≤ *f* ≤ 100	75 ≤ *f* ≤ 133	–

Operating Mode

The normal operating mode is selected by issuing an LMR command with bits A7–A*n* each set to zero and bits A[6:0] set to the desired values. A DLL reset is initiated by issuing an LMR command with bits A7 and A[*n*:9] each set to zero, bit A8 set to one, and bits A[6:0] set to the desired values. Although not required by the Micron device, JEDEC specifications recommend that an LMR command resetting the DLL should always be followed by an LMR command selecting normal operating mode.

All other combinations of values for A[*n*:7] are reserved for future use and/or test modes. Test modes and reserved states should not be used, as unknown operation or incompatibility with future versions may result.

Extended Mode Register

The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable and output drive strength. These functions are controlled via the bits shown in Figure 23 on page 50. The extended mode register is programmed via the LMR command to the mode register (with BA0 = 1 and BA1 = 0) and will retain the stored information until it is programmed again or until the device loses power. The enabling of the DLL should always be followed by an LMR command to the mode register (BA0/BA1 = 0) to reset the DLL. The extended mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either requirement could result in an unspecified operation.

Output Drive Strength

The normal drive strength for all outputs is specified to be SSTL_2, Class II. This option is intended for the support of the lighter load and/or point-to-point environments. The selection of the reduced drive strength will alter the DQ and DQS pins from SSTL_2, Class II drive strength to a reduced drive strength, which is approximately 54% of the SSTL_2, Class II drive strength.

DLL Enable/Disable

When the part is running without the DLL enabled, device functionality may be altered. The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation (when the device exits self refresh mode, the DLL is enabled automatically). Anytime the DLL is enabled, 200 clock cycles with CKE HIGH must occur before a READ command can be issued.

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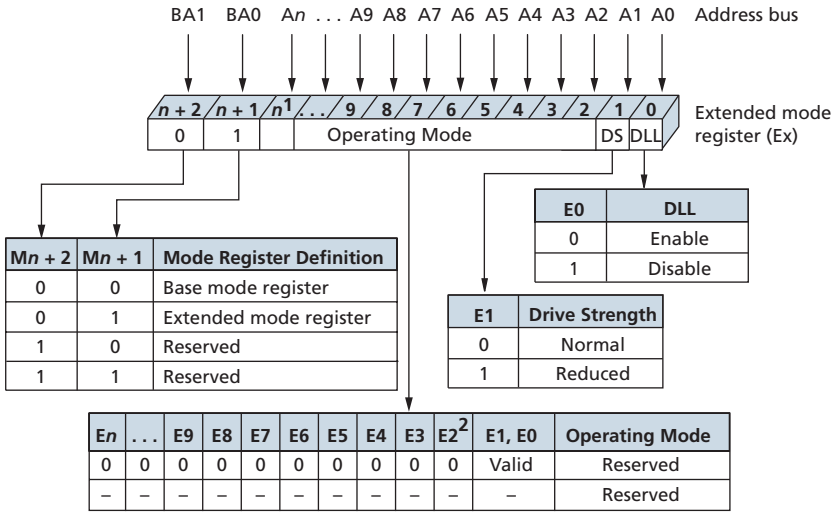
Figure 23: Extended Mode Register Definition



Notes: 1. *n* is the most significant row address bit from Table 2 on page 2.
2. The QFC# option is not supported.

ACTIVE

After a row is opened with an ACTIVE command, a READ or WRITE command may be issued to that row, subject to the ^{t}RCD specification. ^{t}RCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a ^{t}RCD specification of 20ns with a 133 MHz clock (7.5ns period) results in 2.7 clocks rounded to 3. This is reflected in Figure 24 on page 51, which covers any case where $2 < {}^{t}\text{RCD (MIN)} / {}^{t}\text{CK} \leq 3$ (Figure 24 also shows the same case for ^{t}RRD; the same procedure is used to convert other specification limits from time units to clock cycles).

A row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been "closed" (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by ^{t}RC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by ^{t}RRD.

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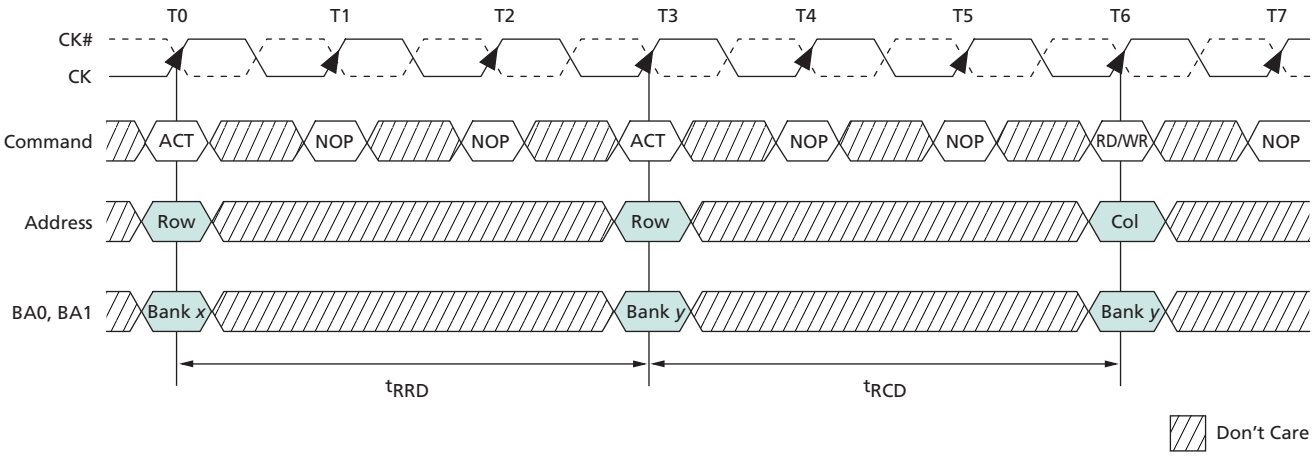
Figure 24: Example: Meeting ^{t}RCD (^{t}RRD) MIN When 2 < ^{t}RCD (^{t}RRD) MIN/^{t}CK ≤ 3



READ

During the READ command, the value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

Note: For the READ commands used in the following illustrations, auto precharge is disabled.

During READ bursts, the valid data-out element from the starting column address will be available following the CL after the READ command. Each subsequent data-out element will be valid nominally at the next positive or negative clock edge (that is, at the next crossing of CK and CK#). Figure 25 on page 53 shows the general timing for each possible CL setting. DQS is driven by the DDR SDRAM along with output data. The initial LOW state on DQS is known as the read preamble; the LOW state coincident with the last data-out element is known as the read postamble.

Upon completion of a burst, assuming no other commands have been initiated, the DQ will go High-Z. Detailed explanations of ^{t}DQSQ (valid data-out skew), ^{t}QH (data-out window hold), and the valid data window are depicted in Figure 33 on page 61 and Figure 34 on page 62. Detailed explanations of ^{t}DQSCK (DQS transition skew to CK) and ^{t}AC (data-out transition skew to CK) are depicted in Figure 35 on page 63.

Data from any READ burst may be concatenated or truncated with data from a subsequent READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new READ command should be issued *x* cycles after the first READ command, where *x* equals the number of desired data element pairs (pairs are required by the 2*n*-prefetch architecture). This is shown in Figure 26 on page 54. A READ command can be initiated on any clock cycle following a previous READ command. Nonconsecutive read data is illustrated in Figure 27 on page 55. Full-speed random read accesses within a page (or pages) can be performed, as shown in Figure 28 on page 56.

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Data from any READ burst may be truncated with a BURST TERMINATE command, as shown in Figure 29 on page 57. The BURST TERMINATE latency is equal to the CL, that is, the BURST TERMINATE command should be issued *x* cycles after the READ command where *x* equals the number of desired data element pairs (pairs are required by the 2*n*-prefetch architecture).

Data from any READ burst must be completed or truncated before a subsequent WRITE command can be issued. If truncation is necessary, the BURST TERMINATE command must be used, as shown in Figure 30 on page 58. The ^{t}DQSS (NOM) case is shown; the ^{t}DQSS (MAX) case has a longer bus idle time. (^{t}DQSS [MIN] and ^{t}DQSS [MAX] are defined in the section on WRITEs.) A READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank provided that auto precharge was not activated.

The PRECHARGE command should be issued *x* cycles after the READ command, where *x* equals the number of desired data element pairs (pairs are required by the 2*n*-prefetch architecture). This is shown in Figure 31 on page 59. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until both ^{t}RAS and ^{t}RP have been met. Part of the row precharge time is hidden during the access of the last data elements.

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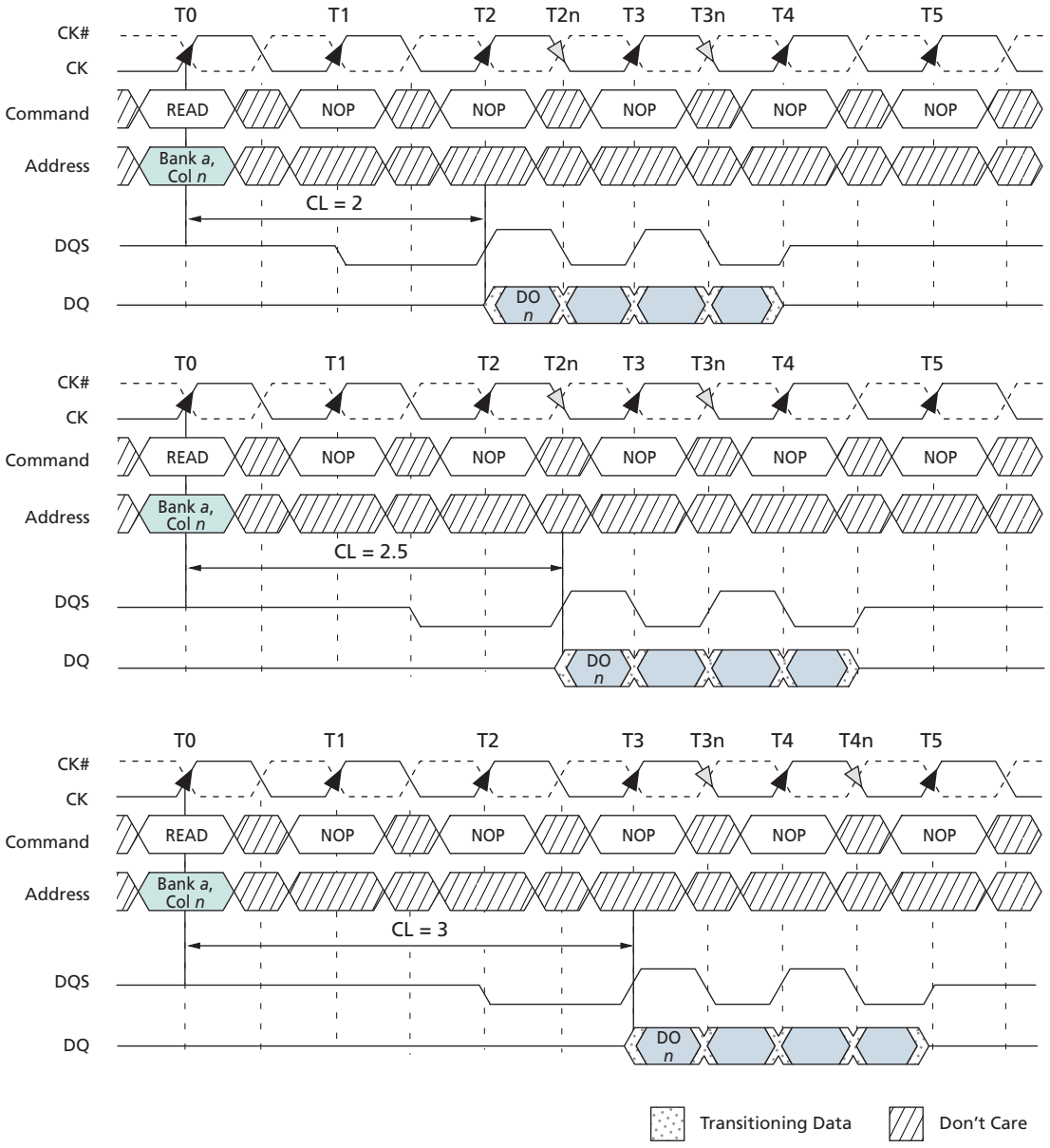
Figure 25: READ Burst



Notes:
1. DO *n* = data-out from column *n*.
2. BL = 4.
3. Three subsequent elements of data-out appear in the programmed order following DO *n*.
4. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

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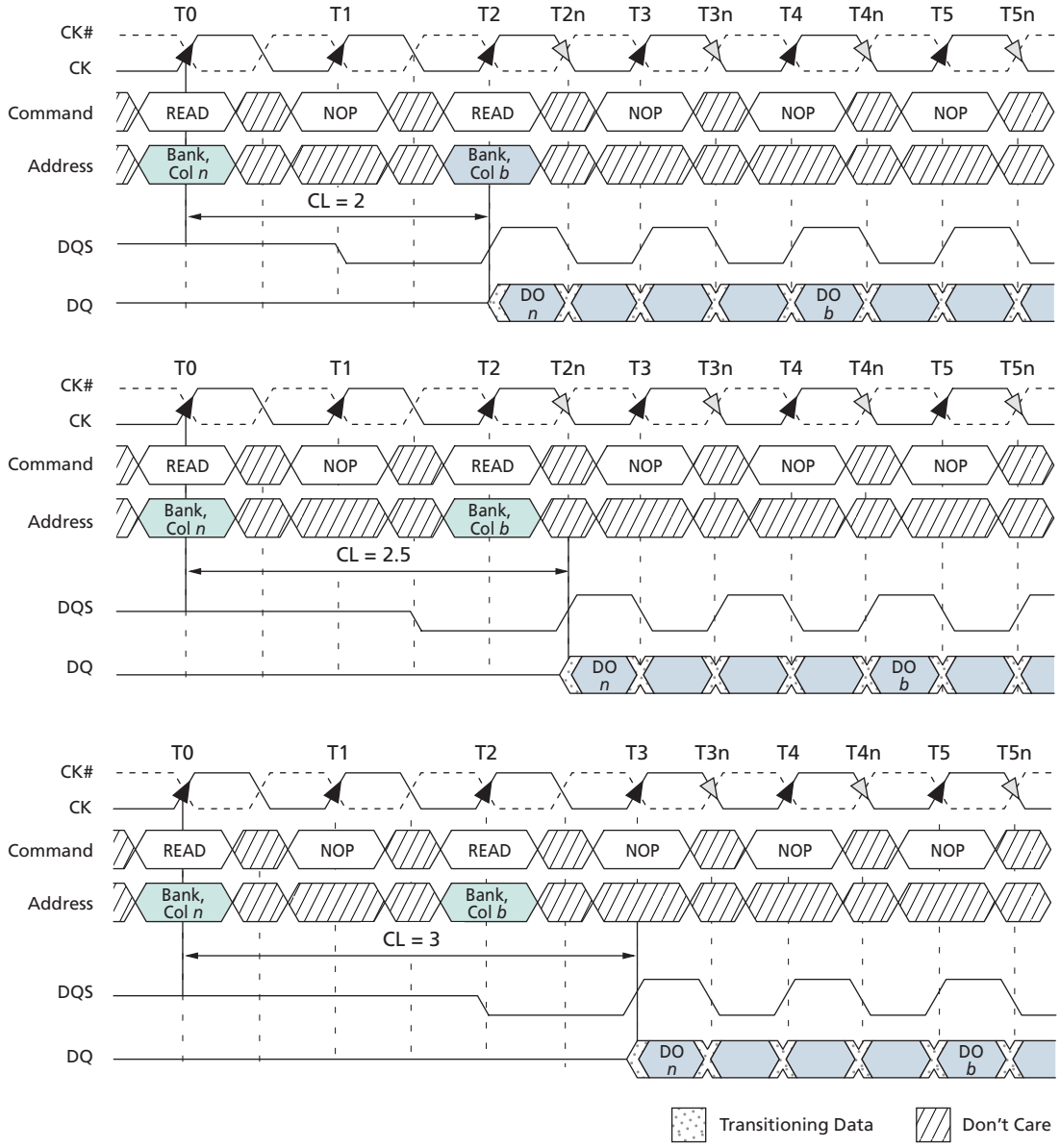
Figure 26: Consecutive READ Bursts



Notes:
1. DO *n* (or *b*) = data-out from column *n* (or column *b*).
2. BL = 4 or BL = 8 (if BL = 4, the bursts are concatenated; if BL = 8, the second burst interrupts the first).
3. Three subsequent elements of data-out appear in the programmed order following DO *n*.
4. Three (or seven) subsequent elements of data-out appear in the programmed order following DO *b*.
5. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.
6. Example applies only when READ commands are issued to same device.

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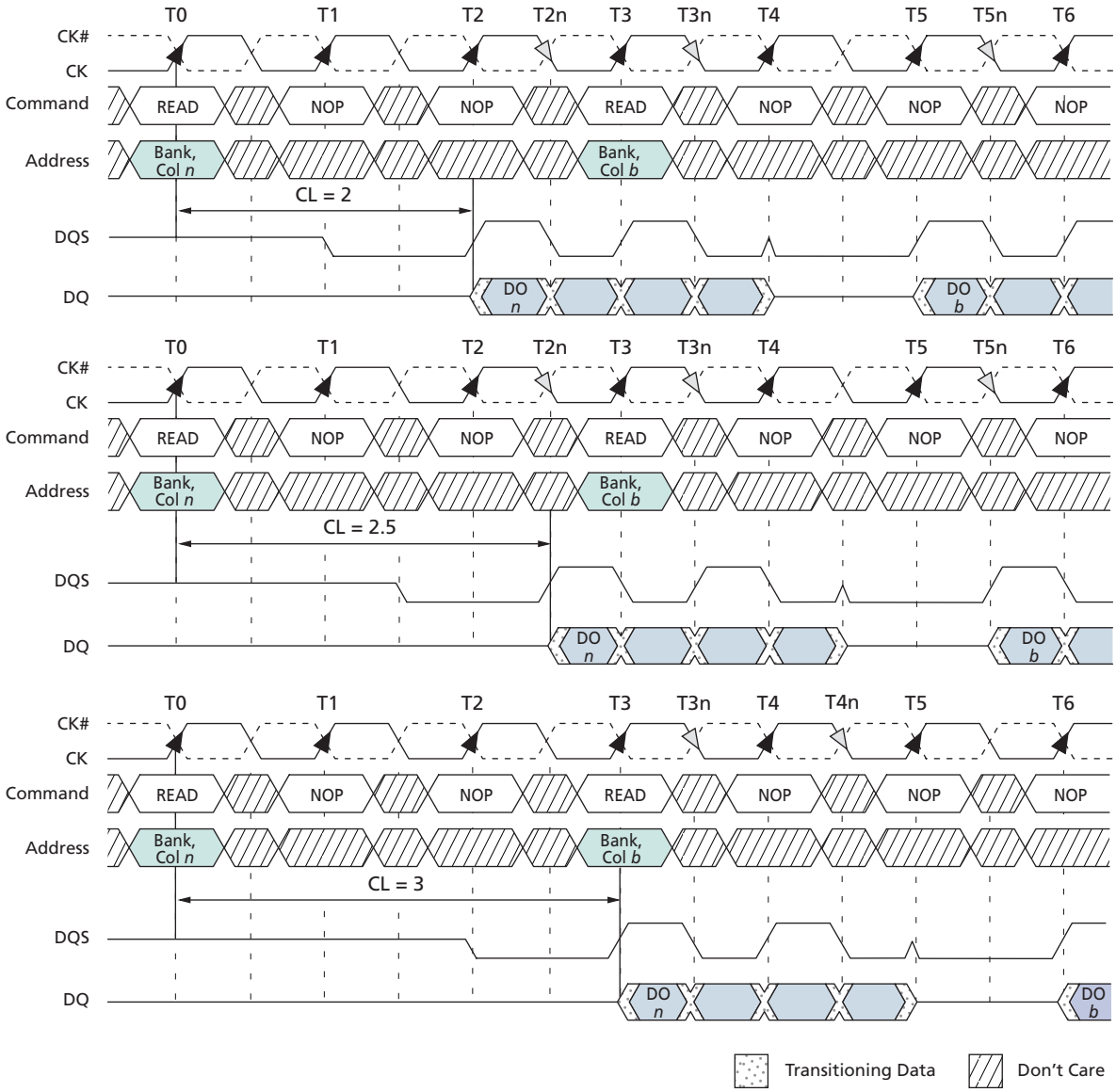
Figure 27: Nonconsecutive READ Bursts



Notes:
1. DO *n* (or *b*) = data-out from column *n* (or column *b*).
2. BL = 4 or BL = 8 (if BL = 4, the bursts are concatenated; if BL = 8, the second burst interrupts the first).
3. Three subsequent elements of data-out appear in the programmed order following DO *n*.
4. Three (or seven) subsequent elements of data-out appear in the programmed order following DO *b*.
5. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

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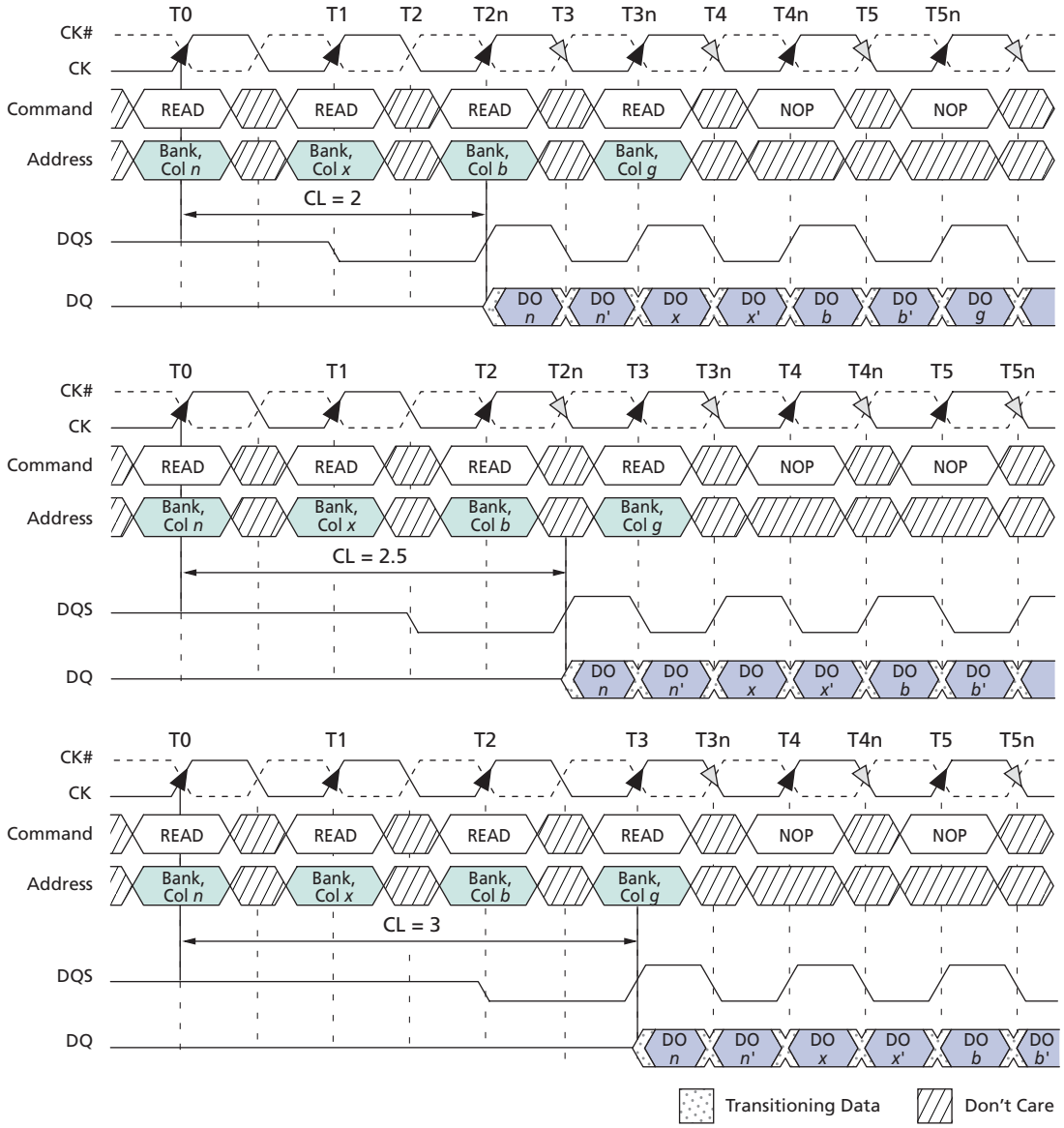
Figure 28: Random READ Accesses



Notes:
1. DO *n* (or *x* or *b* or *g*) = data-out from column *n* (or column *x* or column *b* or column *g*).
2. BL = 2, BL = 4, or BL = 8 (if BL = 4 or BL = 8, the following burst interrupts the previous).
3. *n*', *x*', *b*', or *g*' indicate the next data-out following DO *n*, DO *x*, DO *b*, or DO *g*, respectively.
4. READs are to an active row in any bank.
5. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

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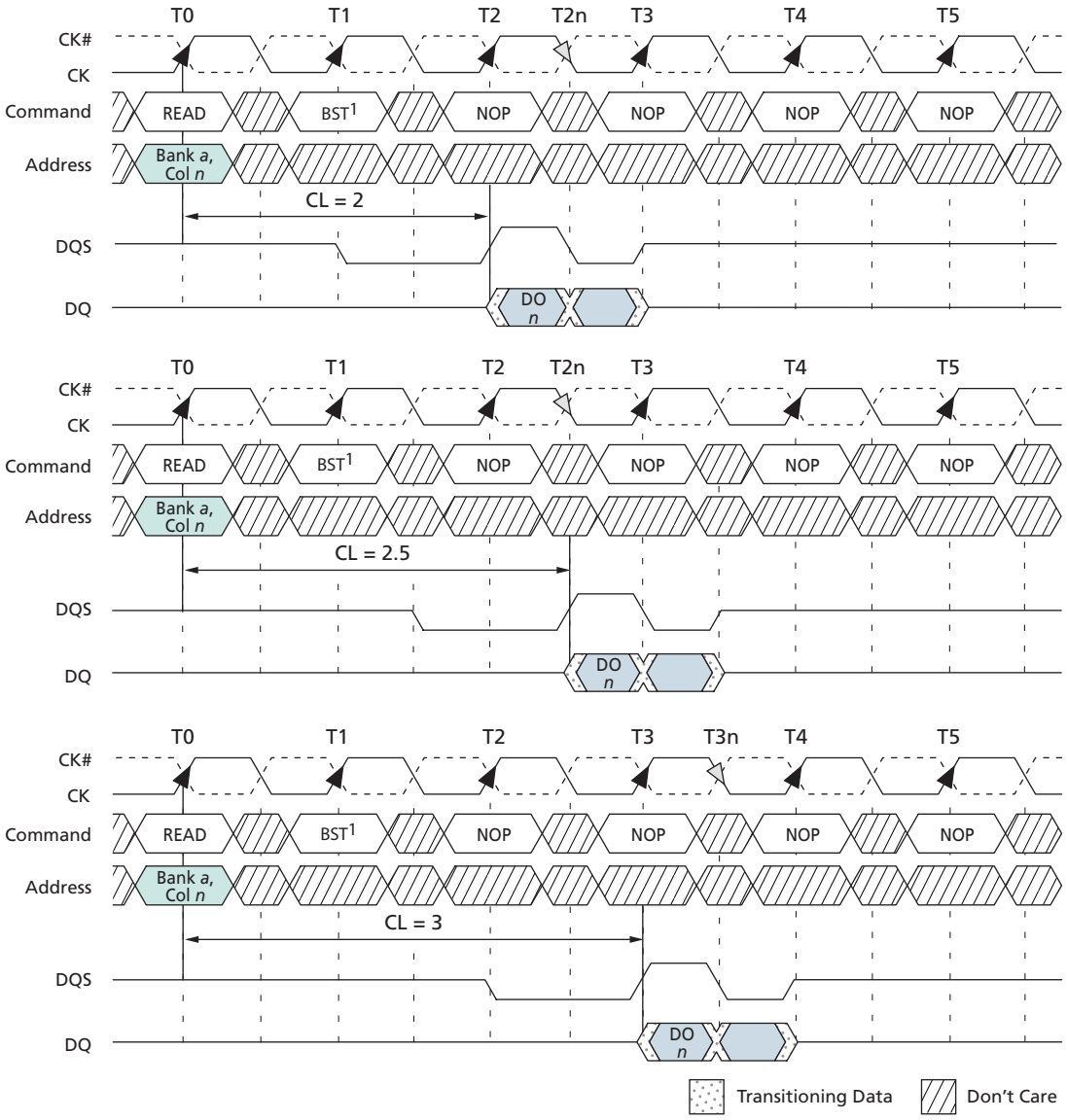
Figure 29: Terminating a READ Burst



Notes:
1. Page remains open.
2. DO *n* = data-out from column *n*.
3. BL = 4.
4. Subsequent element of data-out appears in the programmed order following DO *n*.
5. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

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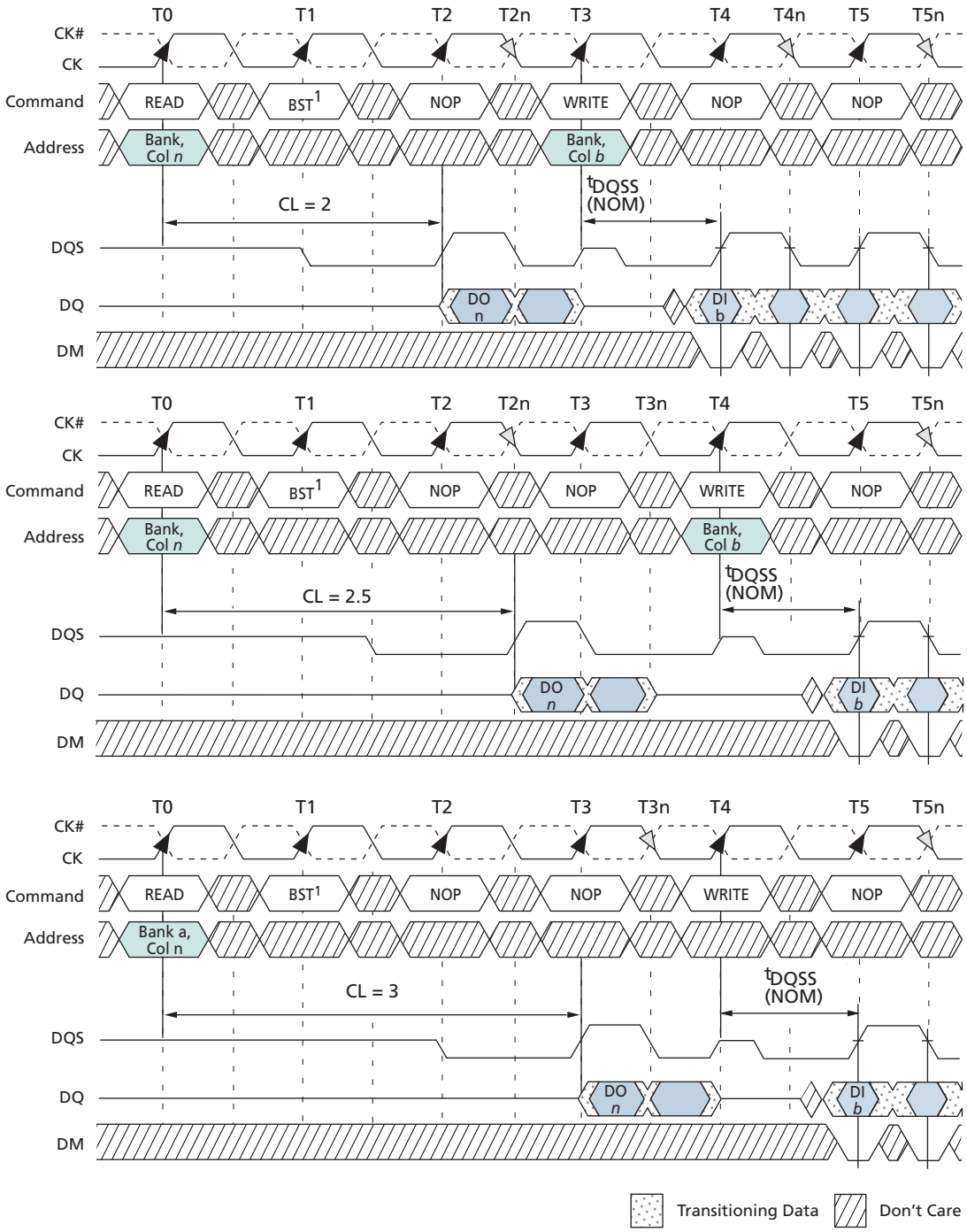
Figure 30: READ-to-WRITE



Notes:
1. Page remains open.
2. DO *n* = data-out from column *n*; DI *b* = data-in from column *b*.
3. BL = 4 (applies for bursts of 8 as well; if BL = 2, the BURST command shown can be NOP).
4. One subsequent element of data-out appears in the programmed order following DO *n*.
5. Data-in elements are applied following DI *b* in the programmed order.
6. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.

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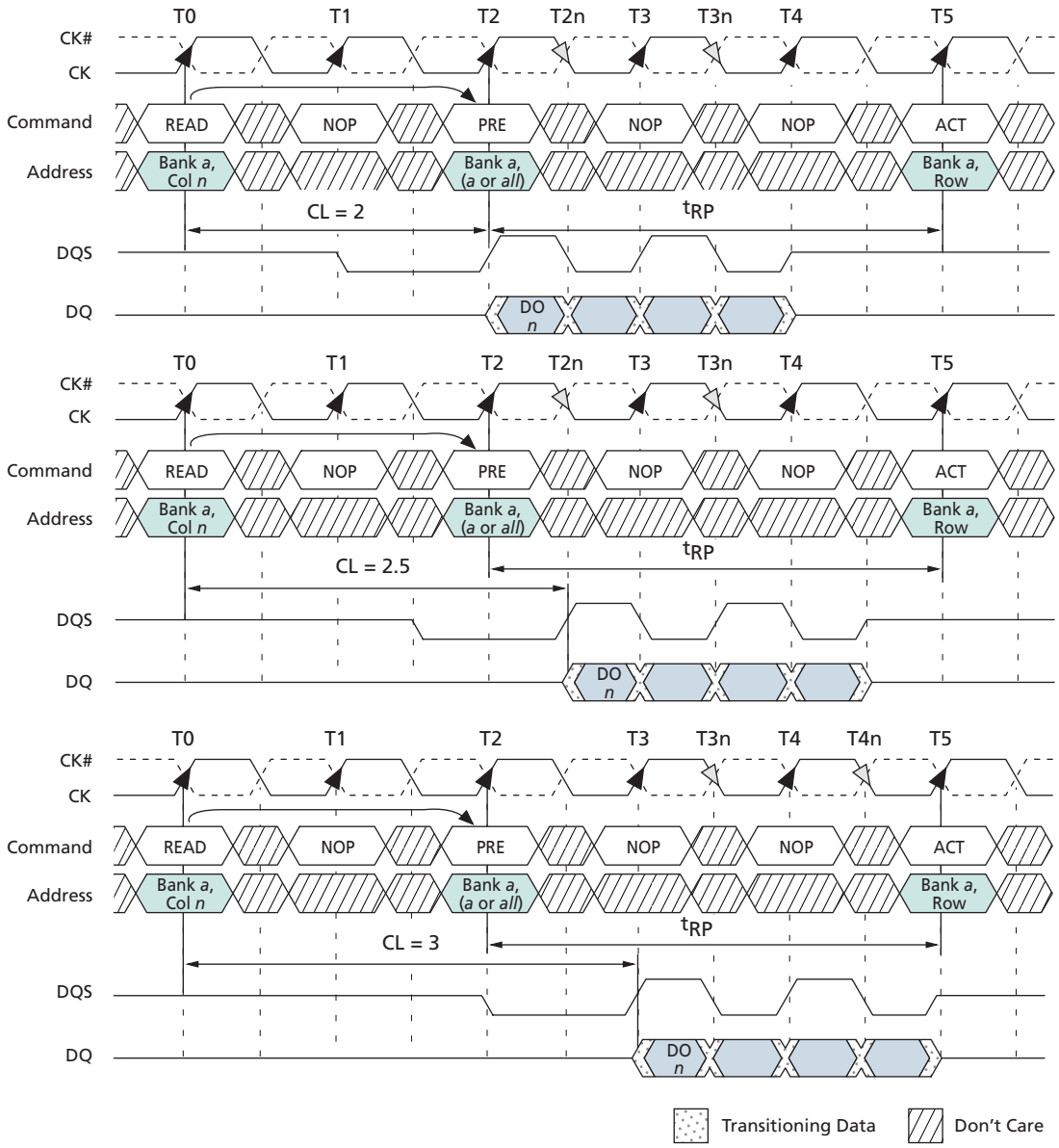
Figure 31: READ-to-PRECHARGE



Notes:
1. Provided ^{t}RAS (MIN) is met, a READ command with auto precharge enabled would cause a precharge to be performed at *x* number of clock cycles after the READ command, where *x* = BL/2.
2. DO *n* = data-out from column *n*.
3. BL = 4 or an interrupted burst of 8.
4. Three subsequent elements of data-out appear in the programmed order following DO *n*.
5. Shown with nominal ^{t}AC, ^{t}DQSCK, and ^{t}DQSQ.
6. READ-to-PRECHARGE equals two clocks, which allows two data pairs of data-out; it is also assumed that ^{t}RAS (MIN) is met.
7. An ACTIVE command to the same bank is only allowed if ^{t}RC (MIN) is met.

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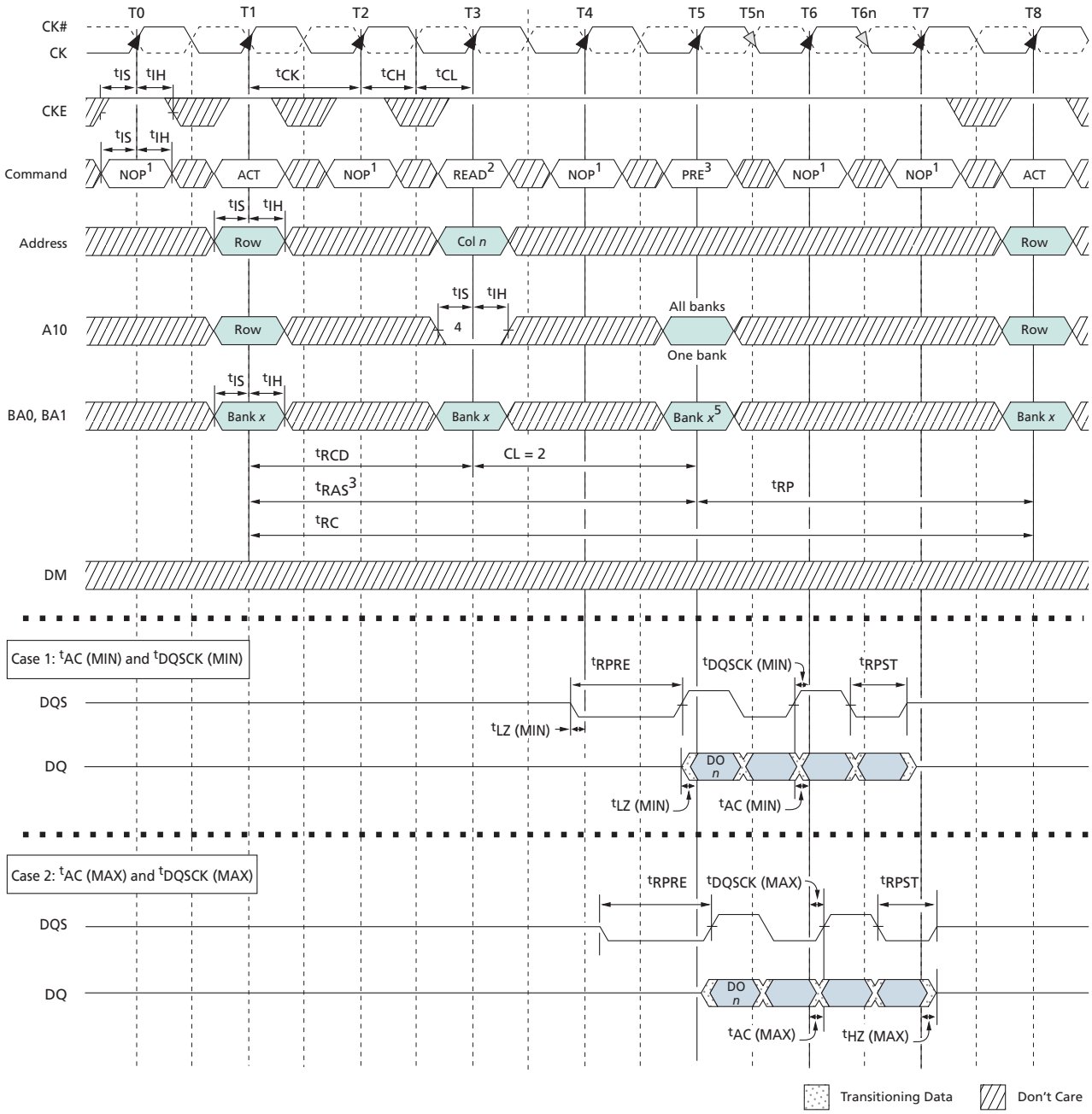
Figure 32: Bank READ – Without Auto Precharge



Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. BL = 4.
3. The PRECHARGE command can only be applied at T5 if ^{t}RAS (MIN) is met.
4. Disable auto precharge.
5. "Don't Care" if A10 is HIGH at T5.
6. DO *n* (or *b*) = data-out from column *n* (or column *b*); subsequent elements are provided in the programmed order.
7. Refer to Figure 33 on page 61, Figure 34 on page 62, and Figure 35 on page 63 for detailed DQS and DQ timing.

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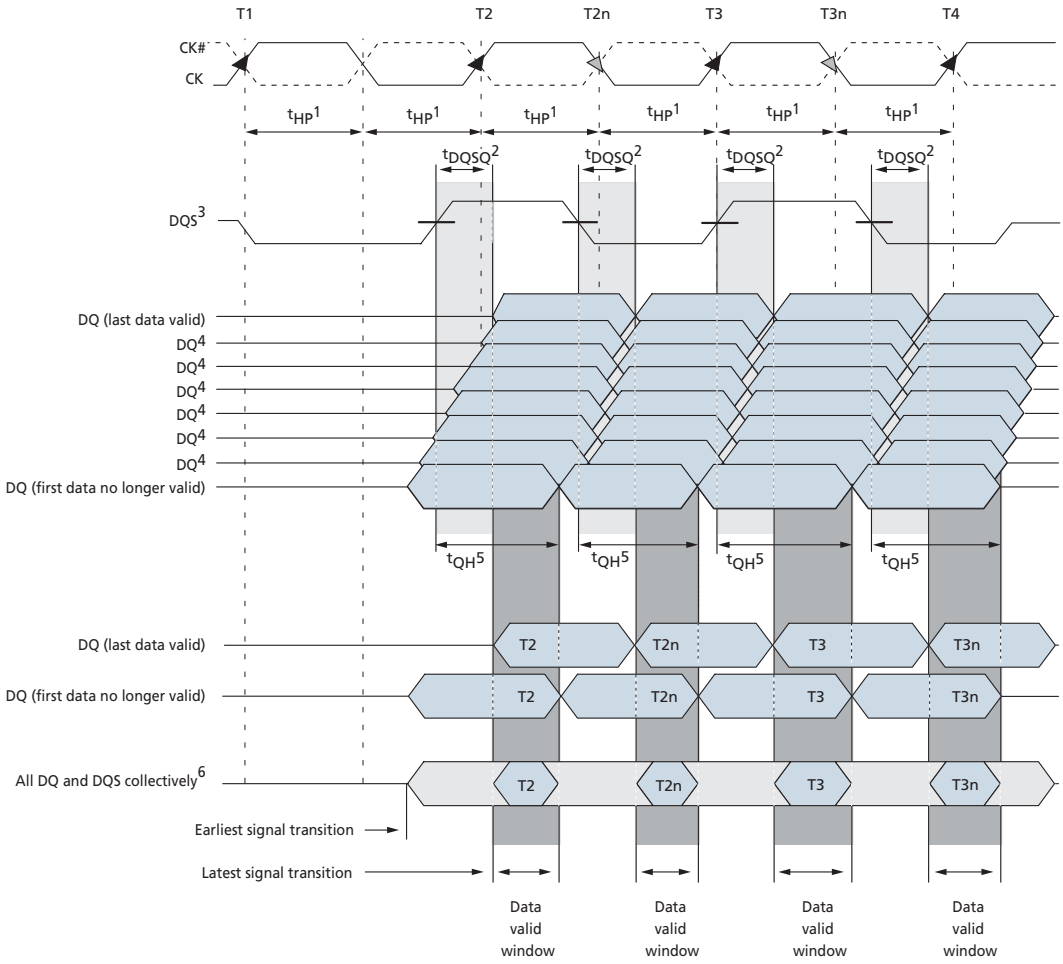
Figure 33: x4, x8 Data Output Timing – ^{t}DQSQ, ^{t}QH, and Data Valid Window



Notes:
1. ^{t}HP is the lesser of ^{t}CL or ^{t}CH clock transition collectively when a bank is active.
2. ^{t}DQSQ is derived at each DQS clock edge, is not cumulative over time, begins with DQS transition, and ends with the last valid DQ transition.
3. DQ transitioning after DQS transition define the ^{t}DQSQ window. DQS transitions at T2 and T2n are an "early DQS"; at T3, a "nominal DQS"; and at T3n, a "late DQS".
4. For a x4, only two DQ apply.
5. ^{t}QH is derived from ^{t}HP: ^{t}QH = ^{t}HP - ^{t}QHS.
6. The data valid window is derived for each DQS transitions and is defined as ^{t}QH - ^{t}DQSQ.

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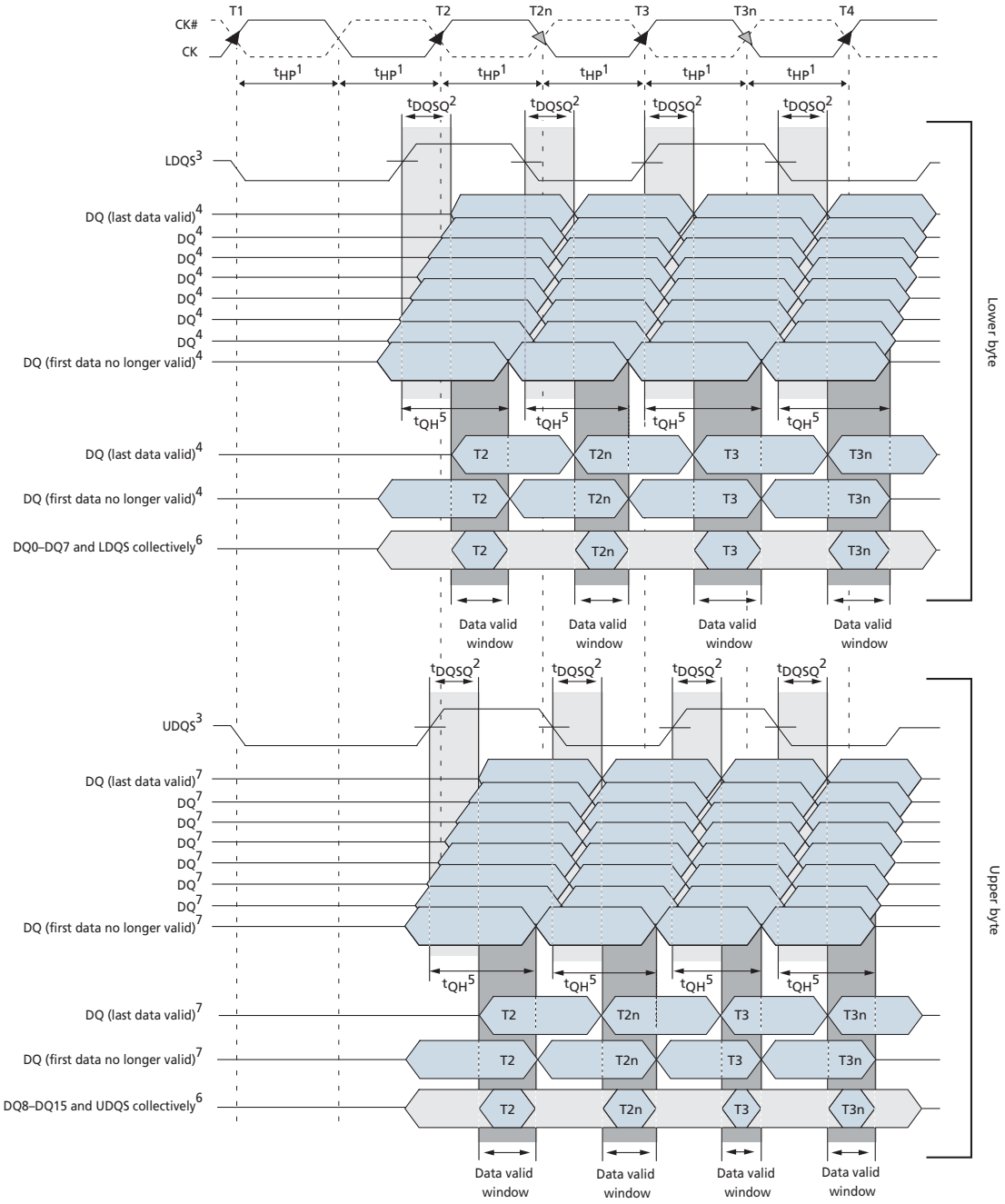
Figure 34: x16 Data Output Timing – ^{t}DQSQ, ^{t}QH, and Data Valid Window



Notes:
1. ^{t}HP is the lesser of ^{t}CL or ^{t}CH clock transition collectively when a bank is active.
2. ^{t}DQSQ is derived at each DQS clock edge, is not cumulative over time, begins with DQS transition, and ends with the last valid DQ transition.
3. DQ transitioning after DQS transition define the ^{t}DQSQ window. LDQS defines the lower byte, and UDQS defines the upper byte.
4. DQ0, DQ1, DQ2, DQ3, DQ4, DQ5, DQ6, or DQ7.
5. ^{t}QH is derived from ^{t}HP: ^{t}QH = ^{t}HP - ^{t}QHS.
6. The data valid window is derived for each DQS transition and is ^{t}QH - ^{t}DQSQ.
7. DQ8, DQ9, DQ10, D11, DQ12, DQ13, DQ14, or DQ15.

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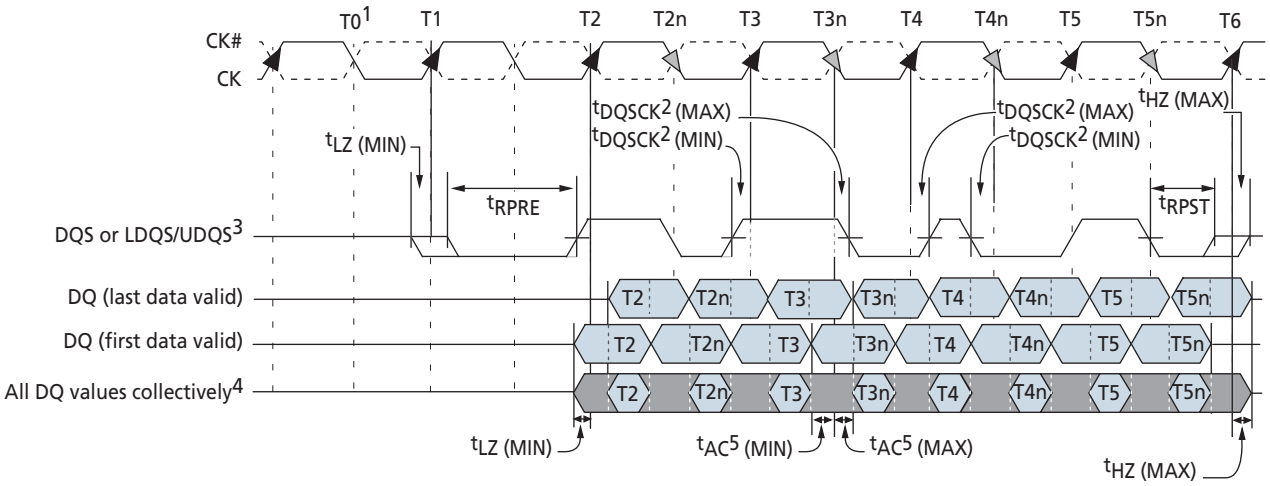
Figure 35: Data Output Timing – ^{t}AC and ^{t}DQSCK



Notes:
1. READ command with CL = 2 issued at T0.
2. ^{t}DQSCK is the DQS output window relative to CK and is the "long term" component of the DQS skew.
3. DQ transitioning after DQS transition define the ^{t}DQSQ window.
4. All DQ must transition by ^{t}DQSQ after DQS transitions, regardless of ^{t}AC.
5. ^{t}AC is the DQ output window relative to CK and is the "long term" component of DQ skew.
6. ^{t}LZ (MIN) and ^{t}AC (MIN) are the first valid signal transitions.
7. ^{t}HZ (MAX) and ^{t}AC (MAX) are the latest valid signal transitions.

WRITE

During a WRITE command, the value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst (after ^{t}WR time); if auto precharge is not selected, the row will remain open for subsequent accesses.

Input data appearing on the DQ is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory. If the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

Note: For the WRITE commands used in the following illustrations, auto precharge is disabled.

During WRITE bursts, the first valid data-in element will be registered on the first rising edge of DQS following the WRITE command, and subsequent data elements will be registered on successive edges of DQS. The LOW state on DQS between the WRITE command and the first rising edge is known as the write preamble; the LOW state on DQS following the last data-in element is known as the write postamble.

The time between the WRITE command and the first corresponding rising edge of DQS (^{t}DQSS) is specified with a relatively wide range (from 75% to 125% of one clock cycle). All of the WRITE diagrams show the nominal case, and where the two extreme cases (that is, ^{t}DQSS [MIN] and ^{t}DQSS [MAX]) might not be intuitive; they have also been included. Figure 36 on page 65 shows the nominal case and the extremes of ^{t}DQSS for BL = 4. Upon completion of a burst, assuming no other commands have been initiated, the DQ will remain High-Z and any additional input data will be ignored.

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Data for any WRITE burst may be concatenated with or truncated with a subsequent WRITE command. In either case, a continuous flow of input data can be maintained. The new WRITE command can be issued on any positive edge of clock following the previous WRITE command. The first data element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new WRITE command should be issued *x* cycles after the first WRITE command, where *x* equals the number of desired data element pairs (pairs are required by the 2*n*-prefetch architecture).

Figure 37 on page 66 shows concatenated bursts of 4. An example of nonconsecutive WRITEs is shown in Figure 38 on page 67. Full-speed random write accesses within a page or pages can be performed as shown in Figure 39 on page 67.

Data for any WRITE burst may be followed by a subsequent READ command. To follow a WRITE without truncating the WRITE burst, ^{t}WTR should be met, as shown in Figure 40 on page 68.

Data for any WRITE burst may be truncated by a subsequent READ command, as shown in Figure 41 on page 69.

Note that only the data-in pairs that are registered prior to the ^{t}WTR period are written to the internal array, and any subsequent data-in should be masked with DM, as shown in Figure 42 on page 70.

Data for any WRITE burst may be followed by a subsequent PRECHARGE command. To follow a WRITE without truncating the WRITE burst, ^{t}WR should be met, as shown in Figure 43 on page 71.

Data for any WRITE burst may be truncated by a subsequent PRECHARGE command, as shown in Figure 44 on page 72 and Figure 45 on page 73. Only the data-in pairs registered prior to the ^{t}WR period are written to the internal array; any subsequent data-in should be masked with DM, as shown in Figures 44 and 45. After the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^{t}RP is met.

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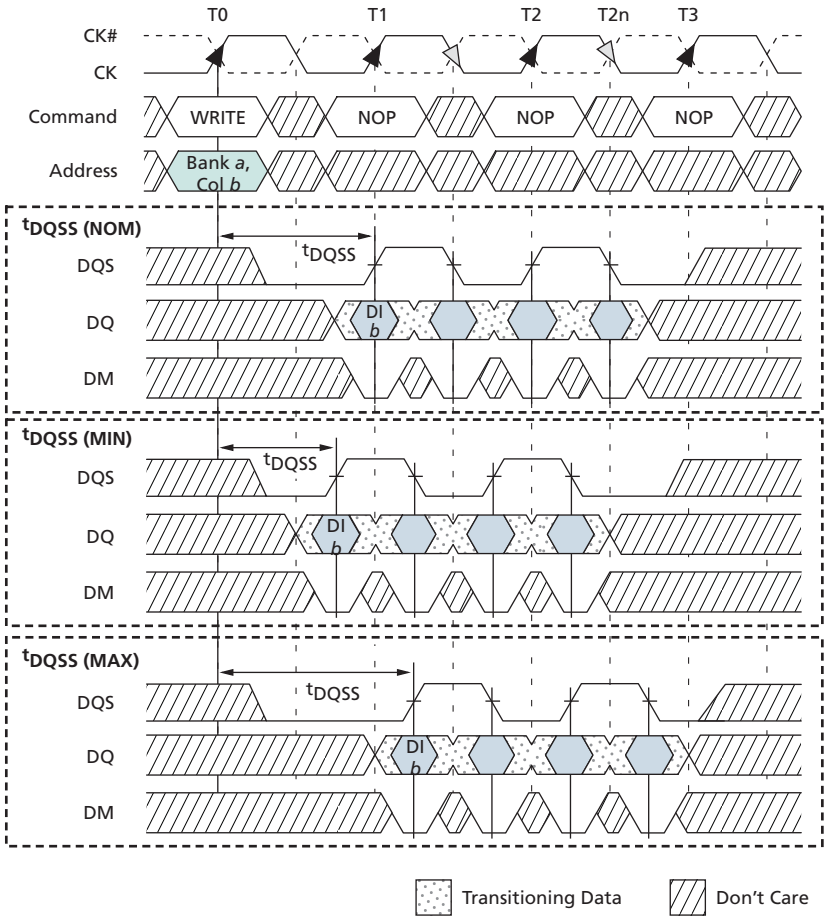
Figure 36: WRITE Burst



Notes:
1. DI *b* = data-in for column *b*.
2. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
3. An uninterrupted burst of 4 is shown.
4. A10 is LOW with the WRITE command (auto precharge is disabled).

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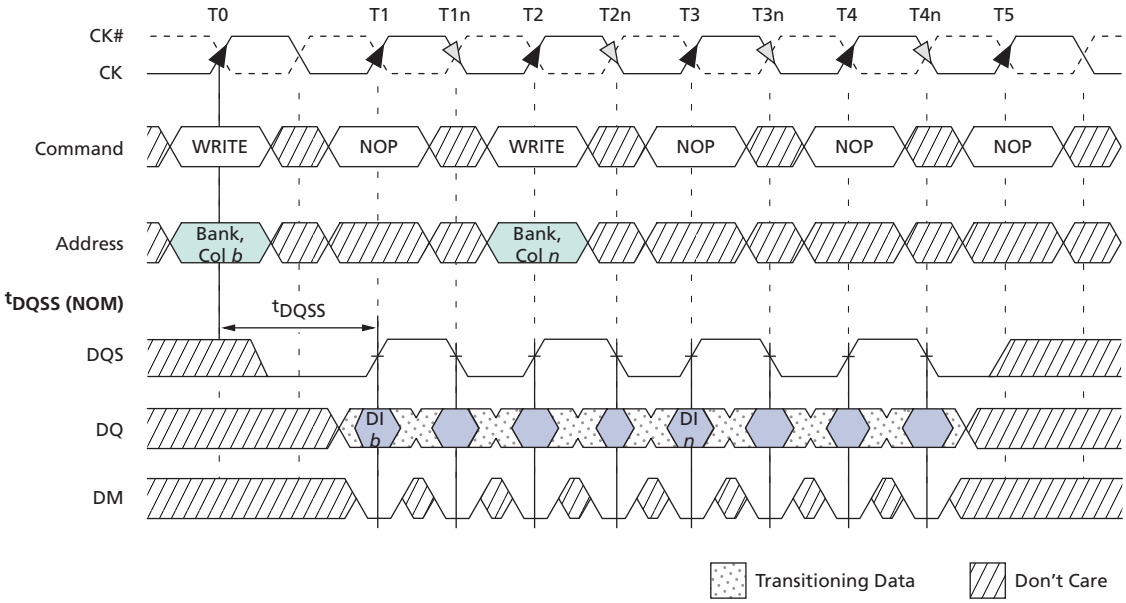
Figure 37: Consecutive WRITE-to-WRITE



Notes:
1. DI *b* (or *n*) = data-in from column *b* (or column *n*).
2. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
3. Three subsequent elements of data-in are applied in the programmed order following DI *n*.
4. An uninterrupted burst of 4 is shown.
5. Each WRITE command may be to any bank.

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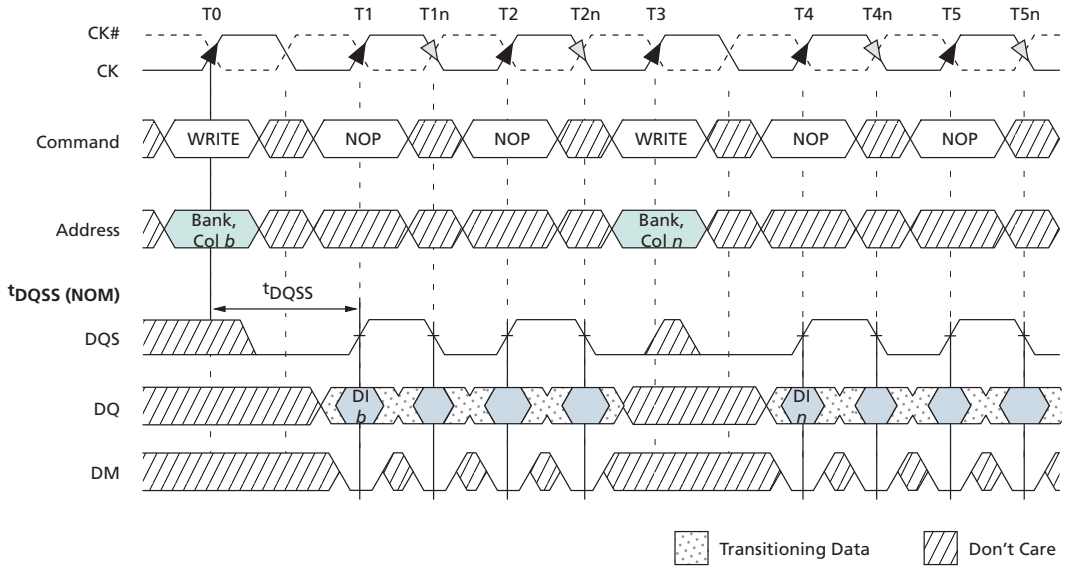
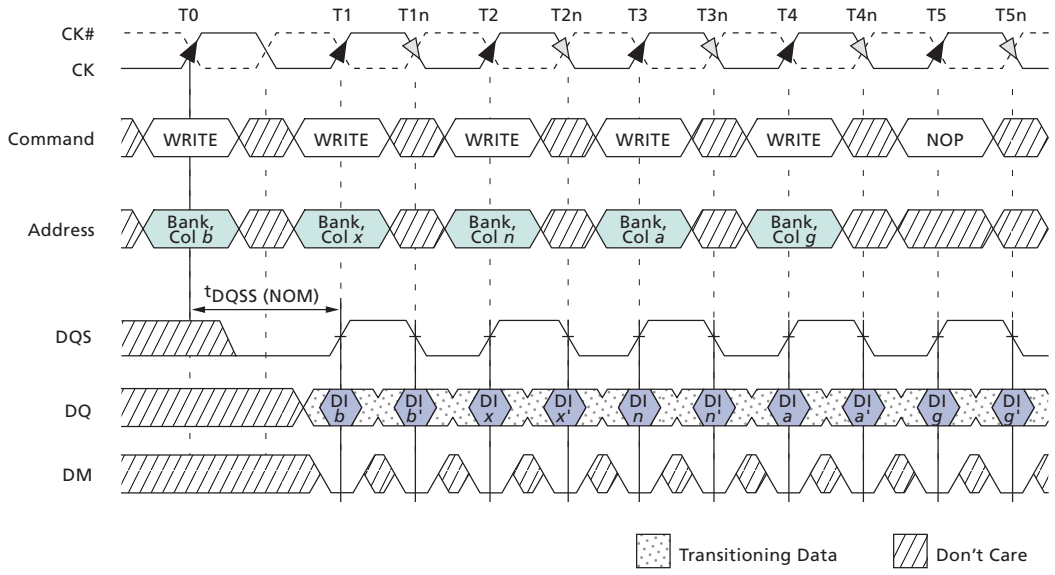
Figure 38: Nonconsecutive WRITE-to-WRITE



Notes:
1. DI *b* (or *n*) = data-in from column *b* (or column *n*).
2. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
3. Three subsequent elements of data-in are applied in the programmed order following DI *n*.
4. An uninterrupted burst of 4 is shown.
5. Each WRITE command may be to any bank.

Figure 39: Random WRITE Cycles



Notes:
1. DI *b* (or *x* or *n* or *a* or *g*) = data-in from column *b* (or column *x*, or column *n*, or column *a*, or column *g*).
2. *b*', x', *n*', *a*' or *g*' indicate the next data-in following DO *b*, DO *x*, DO *n*, DO *a*, or DO *g*, respectively.
3. Programmed BL = 2, BL = 4, or BL = 8 in cases shown.
4. Each WRITE command may be to any bank.

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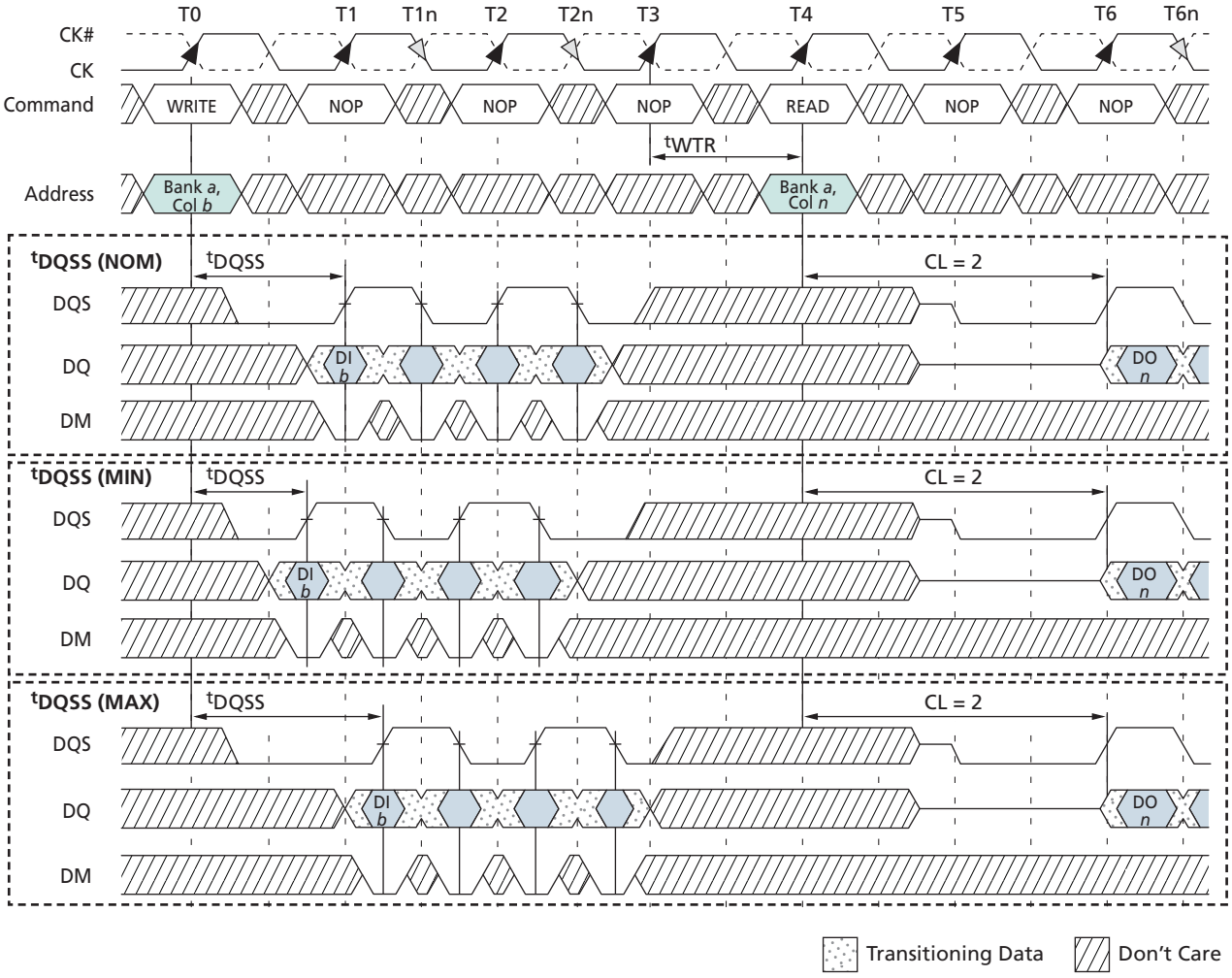
Figure 40: WRITE-to-READ – Uninterrupting



Notes:
1. DI *b* = data-in for column *b*; DO *n* = data-out for column *n*.
2. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
3. An uninterrupted burst of 4 is shown.
4. ^{t}WTR is referenced from the first positive CK edge after the last data-in pair.
5. The READ and WRITE commands are to the same device. However, the READ and WRITE commands may be to different devices, in which case ^{t}WTR is not required, and the READ command could be applied earlier.
6. A10 is LOW with the WRITE command (auto precharge is disabled).

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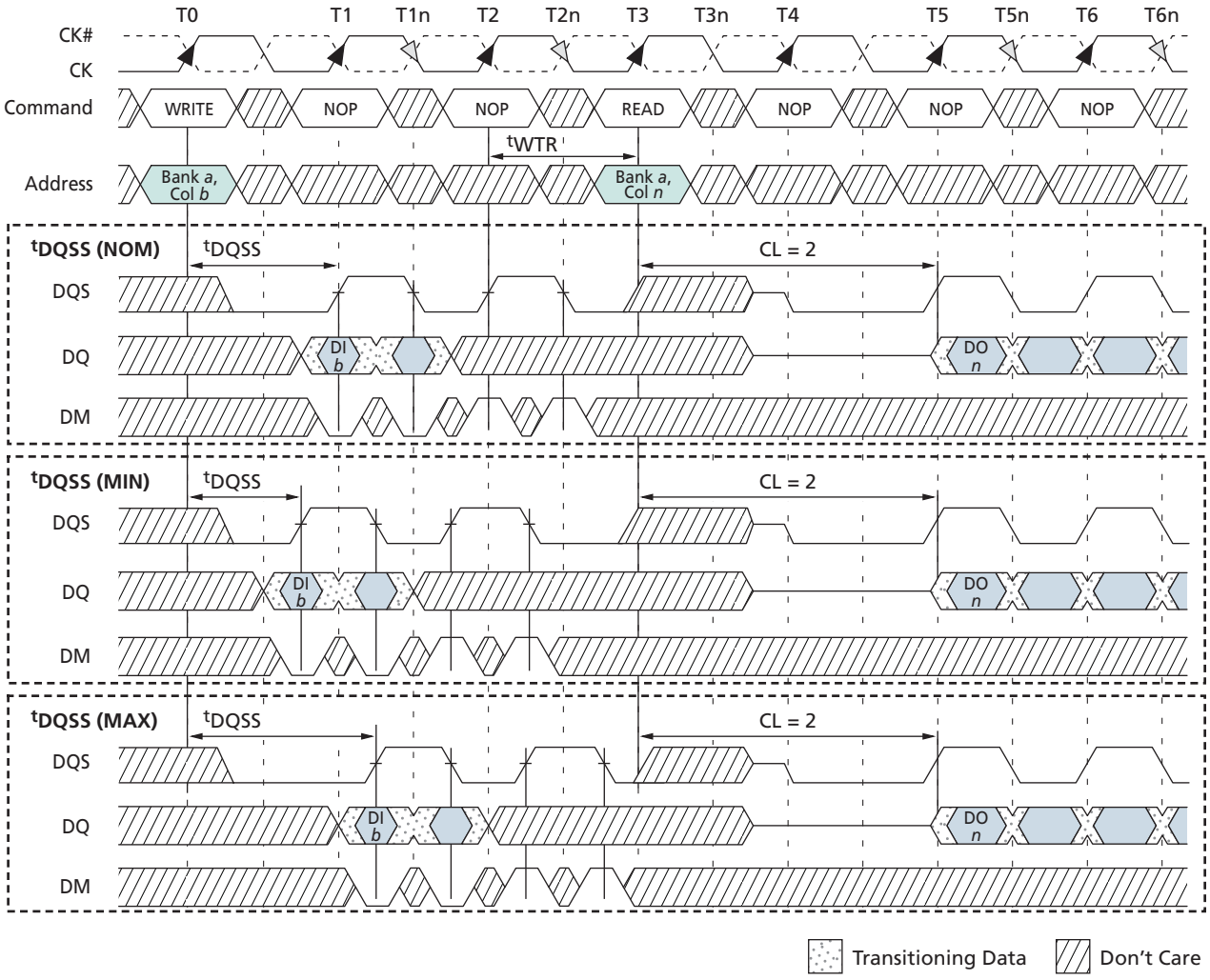
Figure 41: WRITE-to-READ – Interrupting



Notes:
1. DI *b* = data-in for column *b*; DO *n* = data-out for column *n*.
2. An interrupted burst of 4 is shown; two data elements are written.
3. One subsequent element of data-in is applied in the programmed order following DI *b*.
4. ^{t}WTR is referenced from the first positive CK edge after the last data-in pair.
5. A10 is LOW with the WRITE command (auto precharge is disabled).
6. DQS is required at T2 and T2n (nominal case) to register DM.
7. If the burst of 8 is used, DM and DQS are required at T3 and T3n because the READ command will not mask these two data elements.

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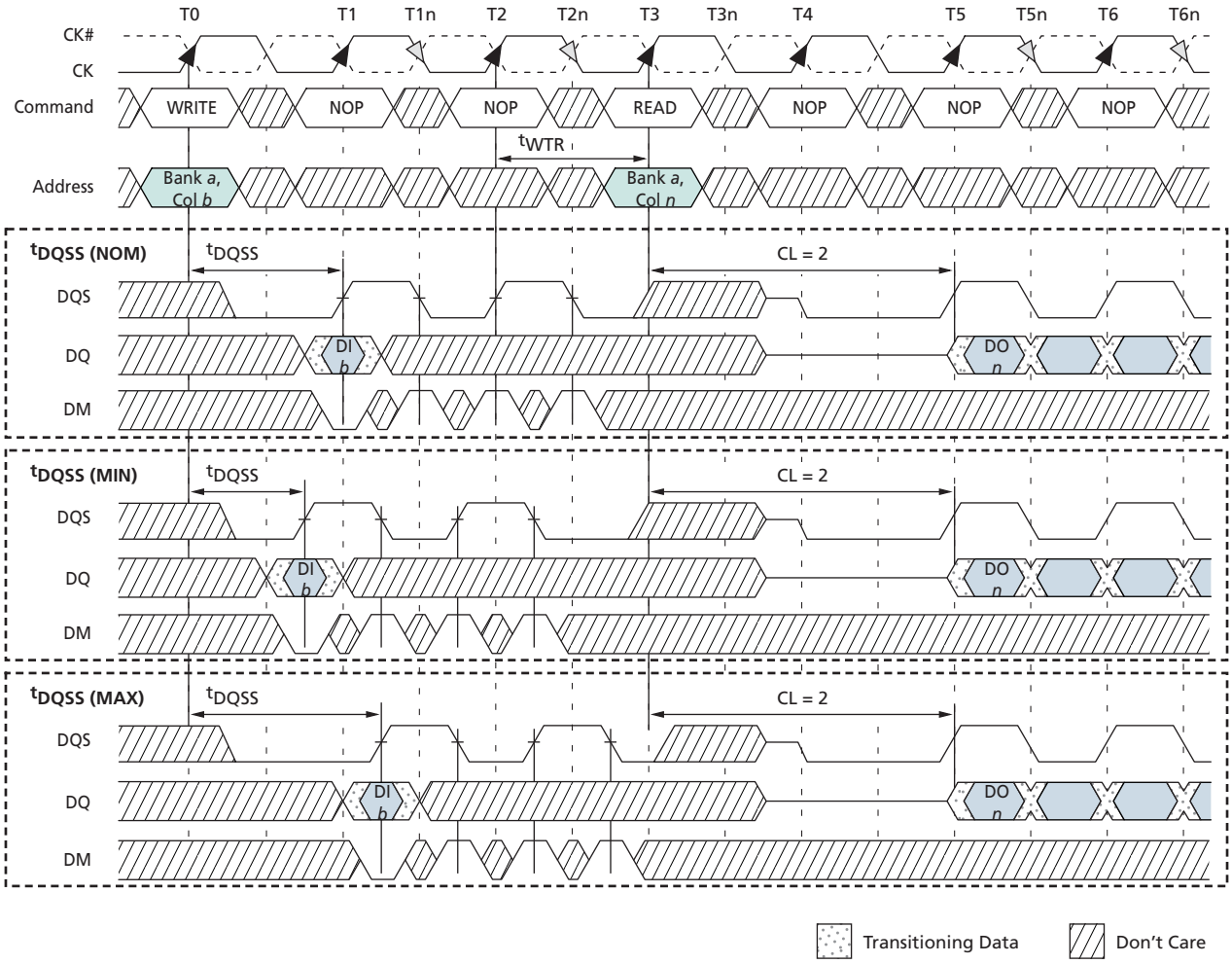
Figure 42: WRITE-to-READ – Odd Number of Data, Interrupting



Notes:
1. DI *b* = data-in for column *b*; DO *n* = data-out for column *n*.
2. An interrupted burst of 4 is shown; one data element is written.
3. ^{t}WTR is referenced from the first positive CK edge after the last desired data-in pair (not the last two data elements).
4. A10 is LOW with the WRITE command (auto precharge is disabled).
5. DQS is required at T1n, T2, and T2n (nominal case) to register DM.
6. If the burst of 8 is used, DM and DQS are required at T3–T3n because the READ command will not mask these data elements.

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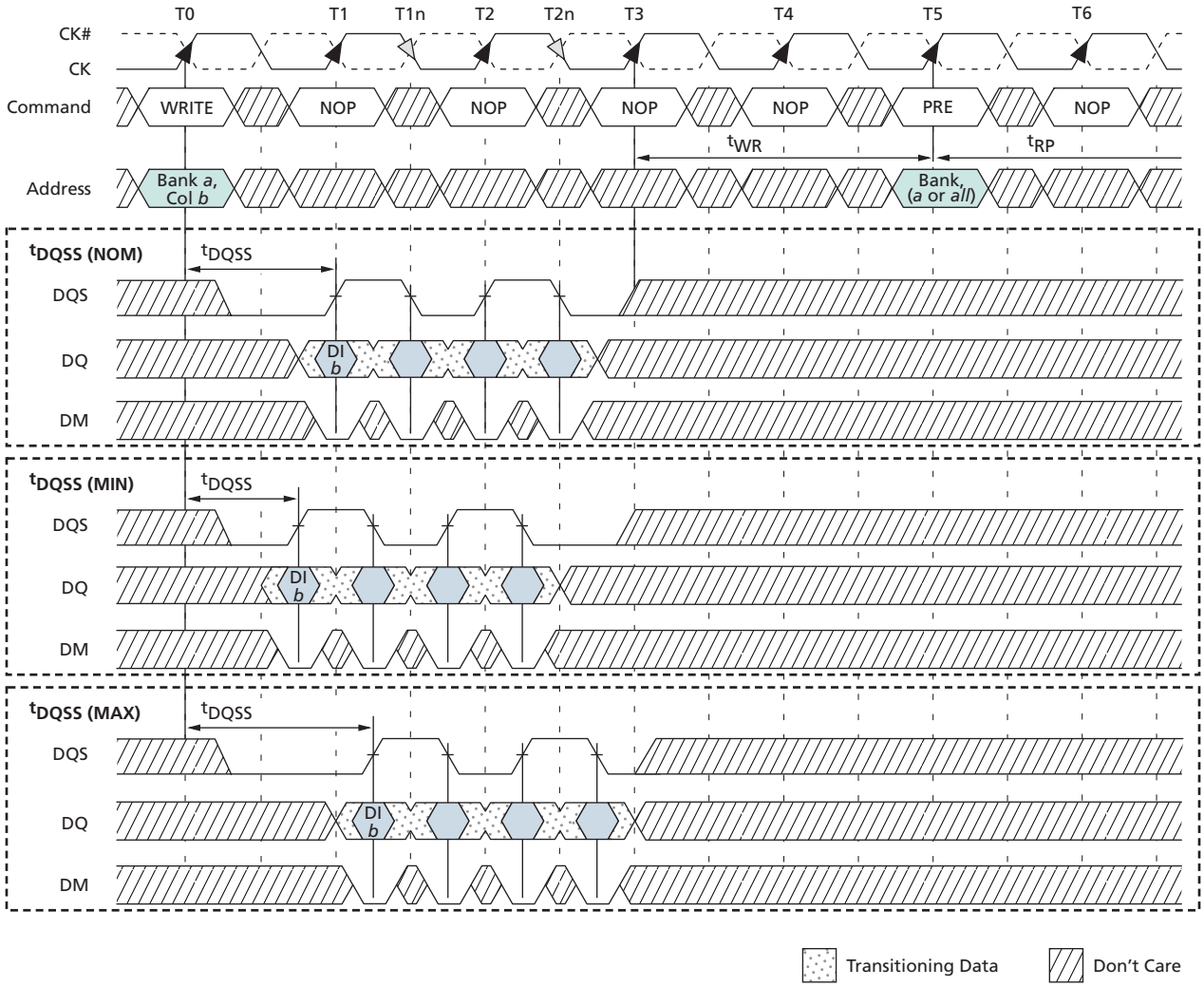
Figure 43: WRITE-to-PRECHARGE – Uninterrupting



Notes:
1. DI *b* = data-in for column *b*.
2. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
3. An uninterrupted burst of 4 is shown.
4. ^{t}WR is referenced from the first positive CK edge after the last data-in pair.
5. The PRECHARGE and WRITE commands are to the same device. However, the PRECHARGE and WRITE commands may be to different devices, in which case ^{t}WR is not required, and the PRECHARGE command could be applied earlier.
6. A10 is LOW with the WRITE command (auto precharge is disabled).

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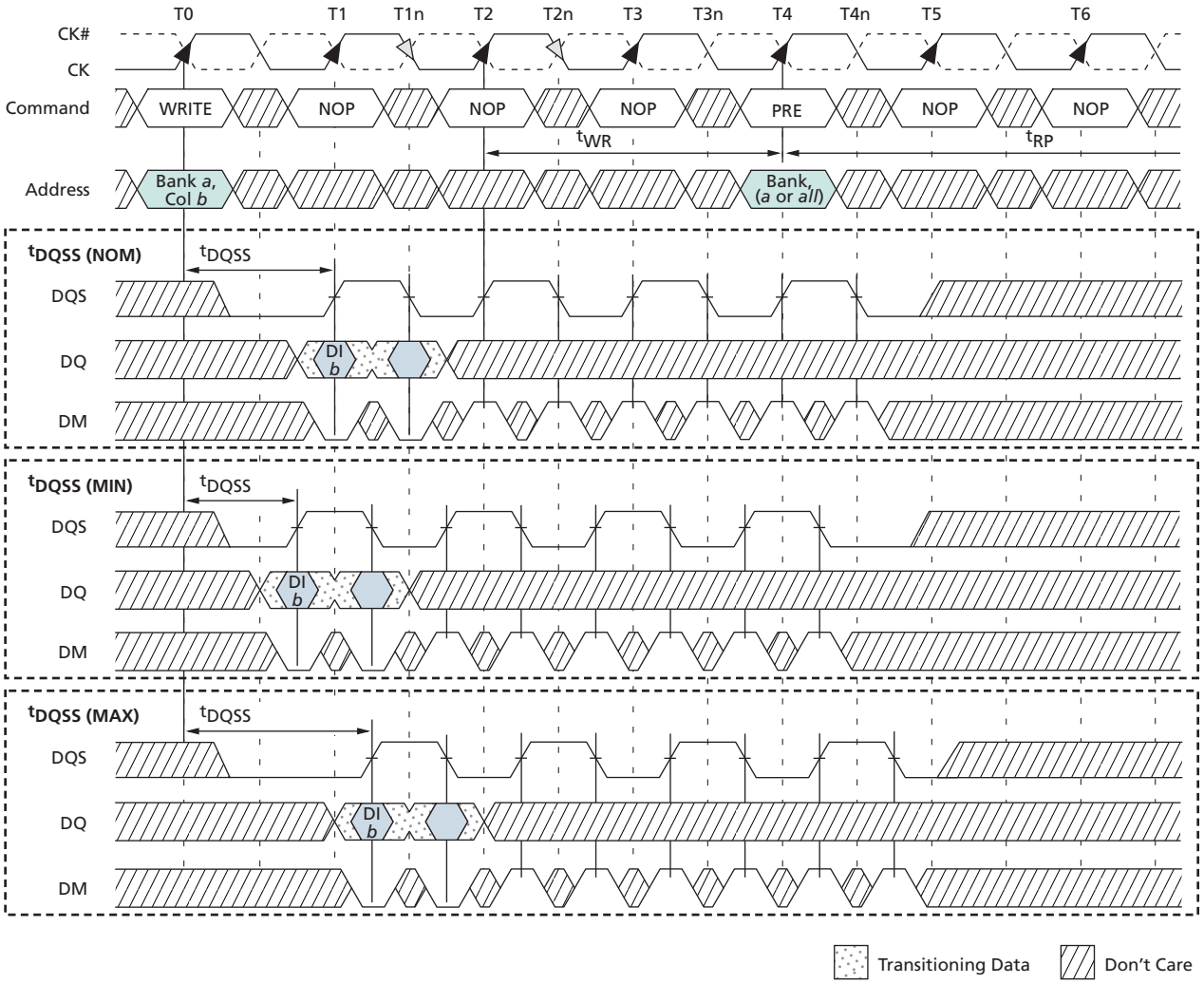
Figure 44: WRITE-to-PRECHARGE – Interrupting



Notes:
1. DI *b* = data-in for column *b*.
2. Subsequent element of data-in is applied in the programmed order following DI *b*.
3. An interrupted burst of 8 is shown; two data elements are written.
4. ^{t}WR is referenced from the first positive CK edge after the last data-in pair.
5. A10 is LOW with the WRITE command (auto precharge is disabled).
6. DQS is required at T4 and T4n (nominal case) to register DM.
7. If the burst of 4 is used, DQS and DM are not required at T3, T3n, T4, and T4n.

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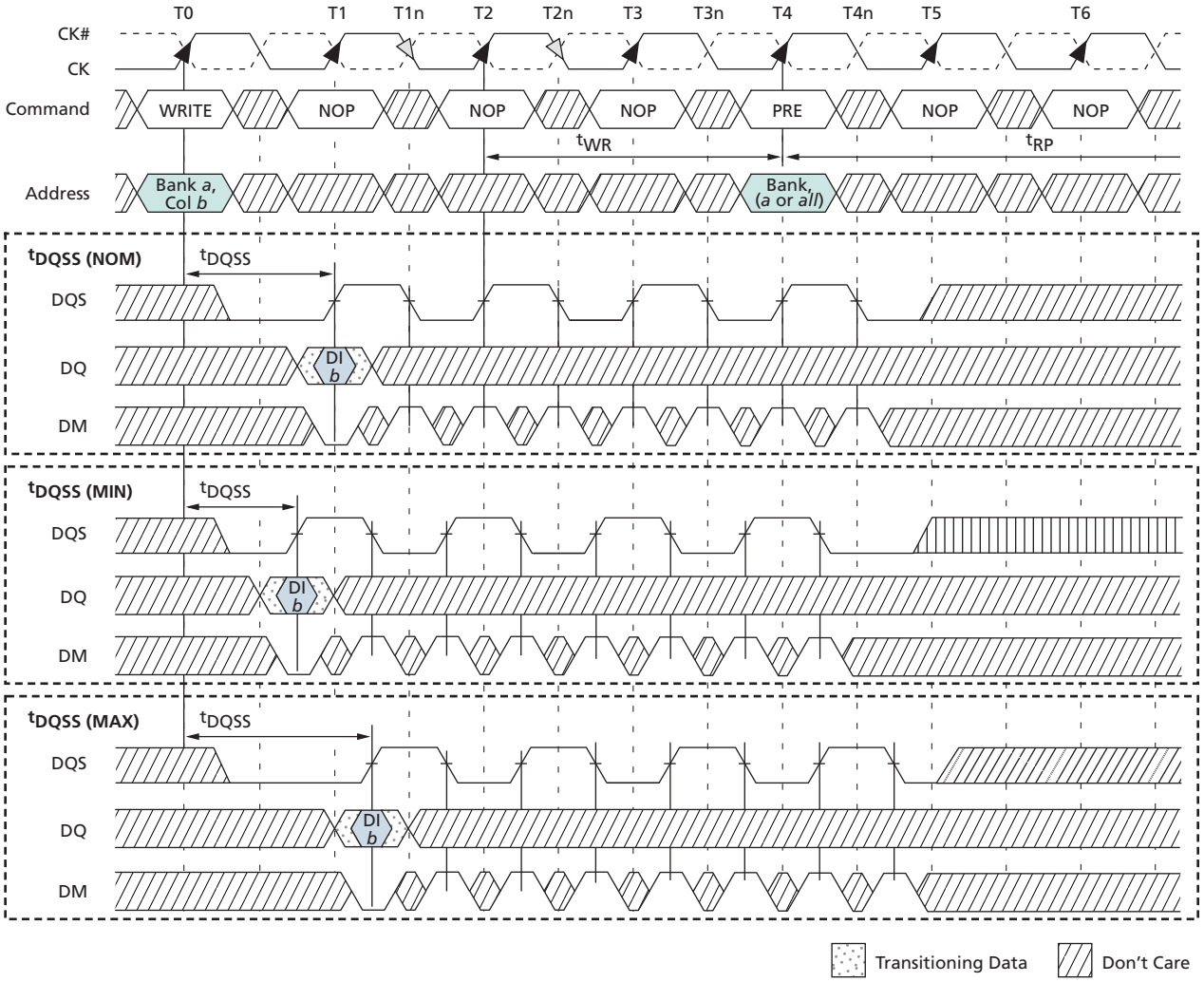
Figure 45: WRITE-to-PRECHARGE – Odd Number of Data, Interrupting



Notes:
1. DI *b* = data-in for column *b*.
2. An interrupted burst of 8 is shown; one data element is written.
3. ^{t}WR is referenced from the first positive CK edge after the last data-in pair.
4. A10 is LOW with the WRITE command (auto precharge is disabled).
5. DQS is required at T4 and T4n (nominal case) to register DM.
6. If the burst of 4 is used, DQS and DM are not required at T3, T3n, T4, and T4n.

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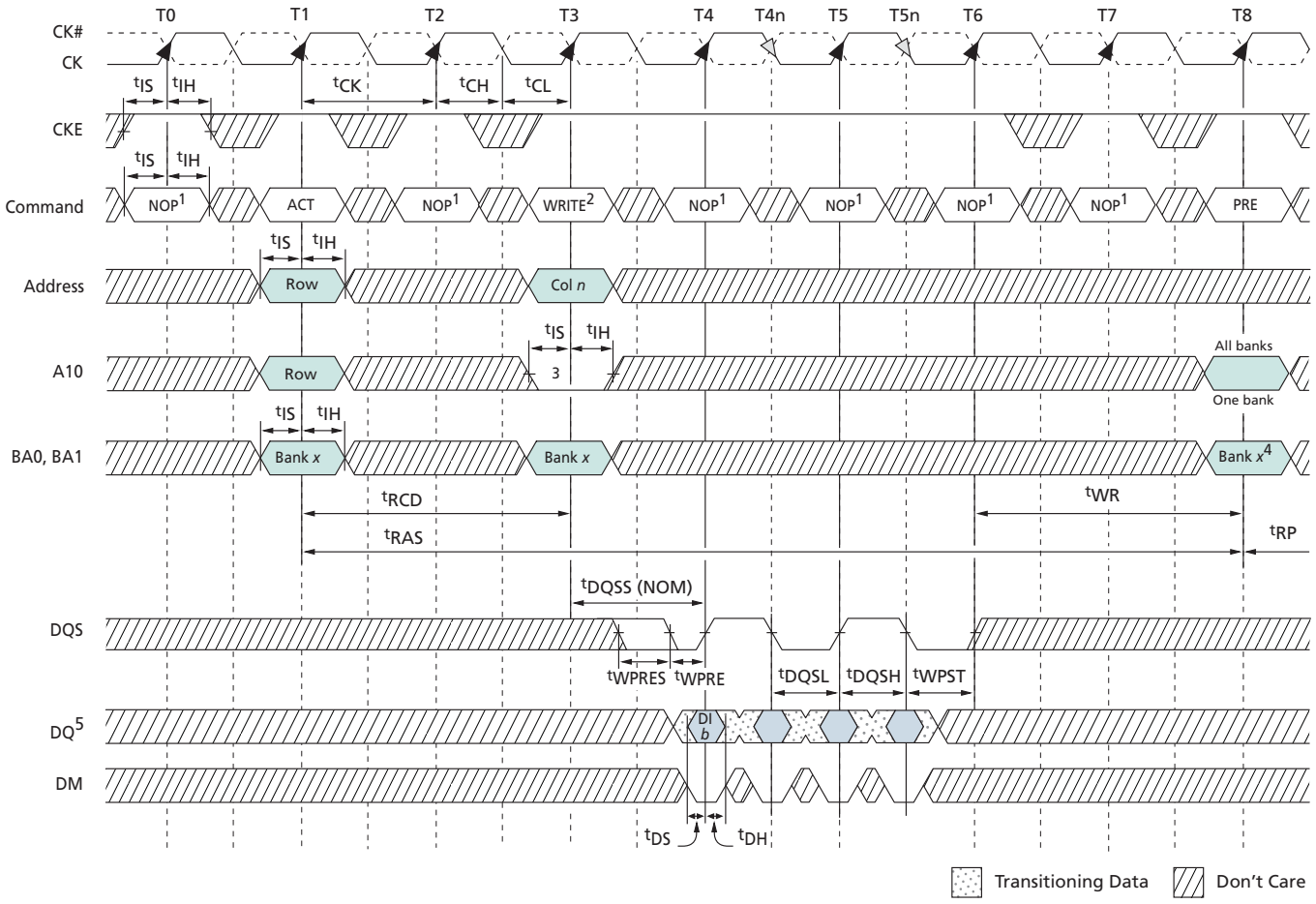
Figure 46: Bank WRITE – Without Auto Precharge



Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. BL = 4.
3. Disable auto precharge.
4. "Don't Care" if A10 is HIGH at T8.
5. DI *b* = data-in from column *b*; subsequent elements are provided in the programmed order.
6. See Figure 48 on page 76 for detailed DQ timing.

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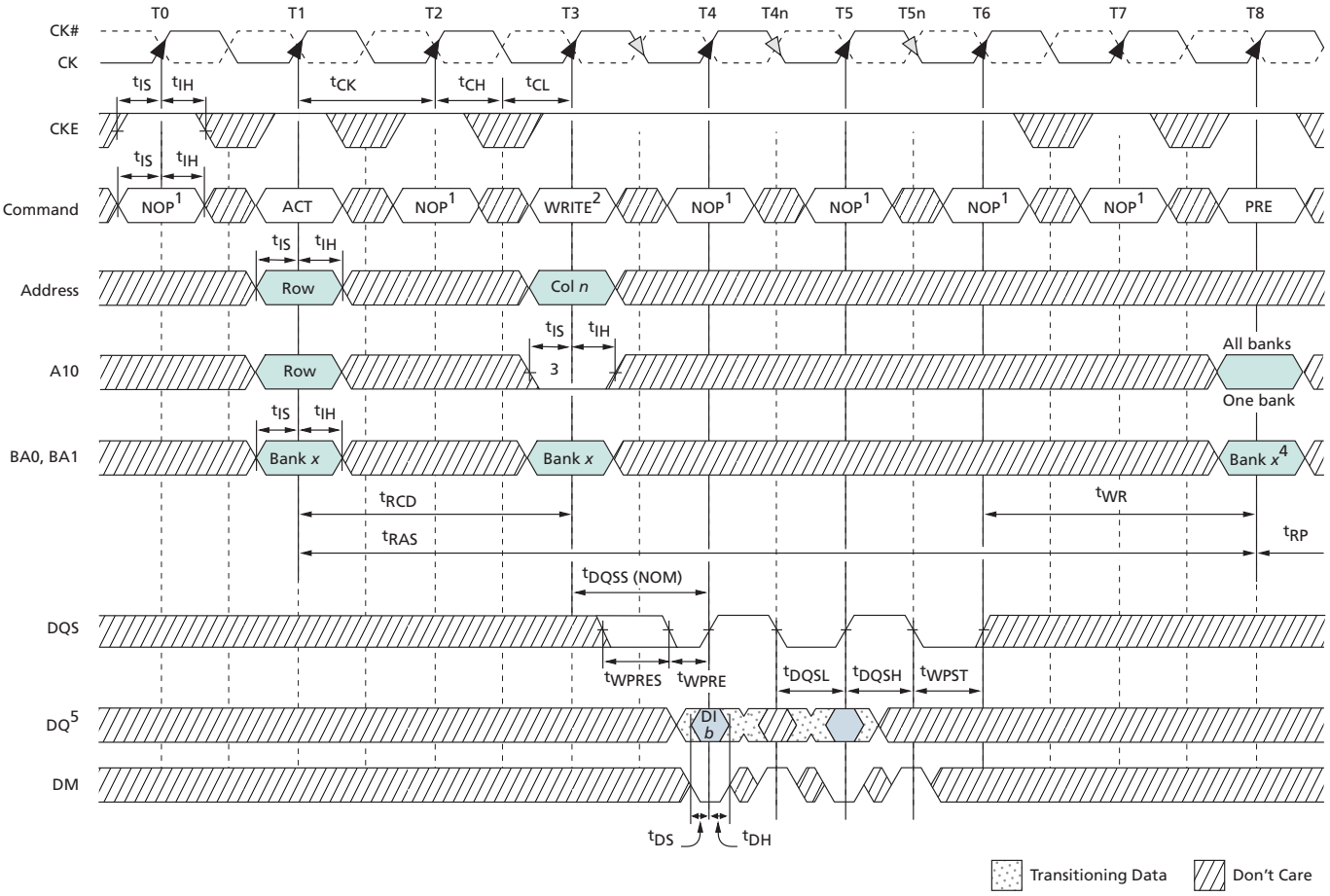
Figure 47: WRITE – DM Operation



Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. BL = 4.
3. Disable auto precharge.
4. "Don't Care" if A10 is HIGH at T8.
5. DI *b* = data-in from column *b*; subsequent elements are provided in the programmed order.
6. See Figure 48 on page 76 for detailed DQ timing.

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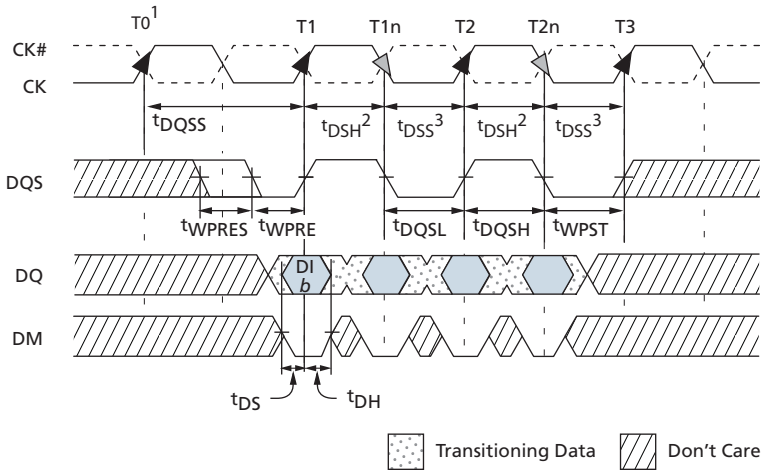
Figure 48: Data Input Timing



Notes:
1. WRITE command issued at T0.
2. ^{t}DSH (MIN) generally occurs during ^{t}DQSS (MIN).
3. ^{t}DSS (MIN) generally occurs during ^{t}DQSS (MAX).
4. For x16, LDQS controls the lower byte and UDQS controls the upper byte.
5. DI *b* = data-in from column *b*.

PRECHARGE

The bank(s) will be available for a subsequent row access a specified time (^{t}RP) after the PRECHARGE command is issued, except in the case of concurrent auto precharge. With concurrent auto precharge, a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank (idle state), or if the previously open row is already in the process of precharging.

Auto Precharge

Auto precharge is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit command. This is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. Auto precharge is either enabled or disabled for each individual READ or WRITE command. This device supports concurrent auto precharge if the command to the other bank does not interrupt the data transfer to the current bank.

Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. This "earliest valid stage" is determined as if an explicit PRECHARGE command was issued at the earliest possible time, without violating ^{t}RAS (MIN), as described for each burst type in "Operations" on page 43. The user must not issue another command to the same bank until the precharge time (^{t}RP) is completed.

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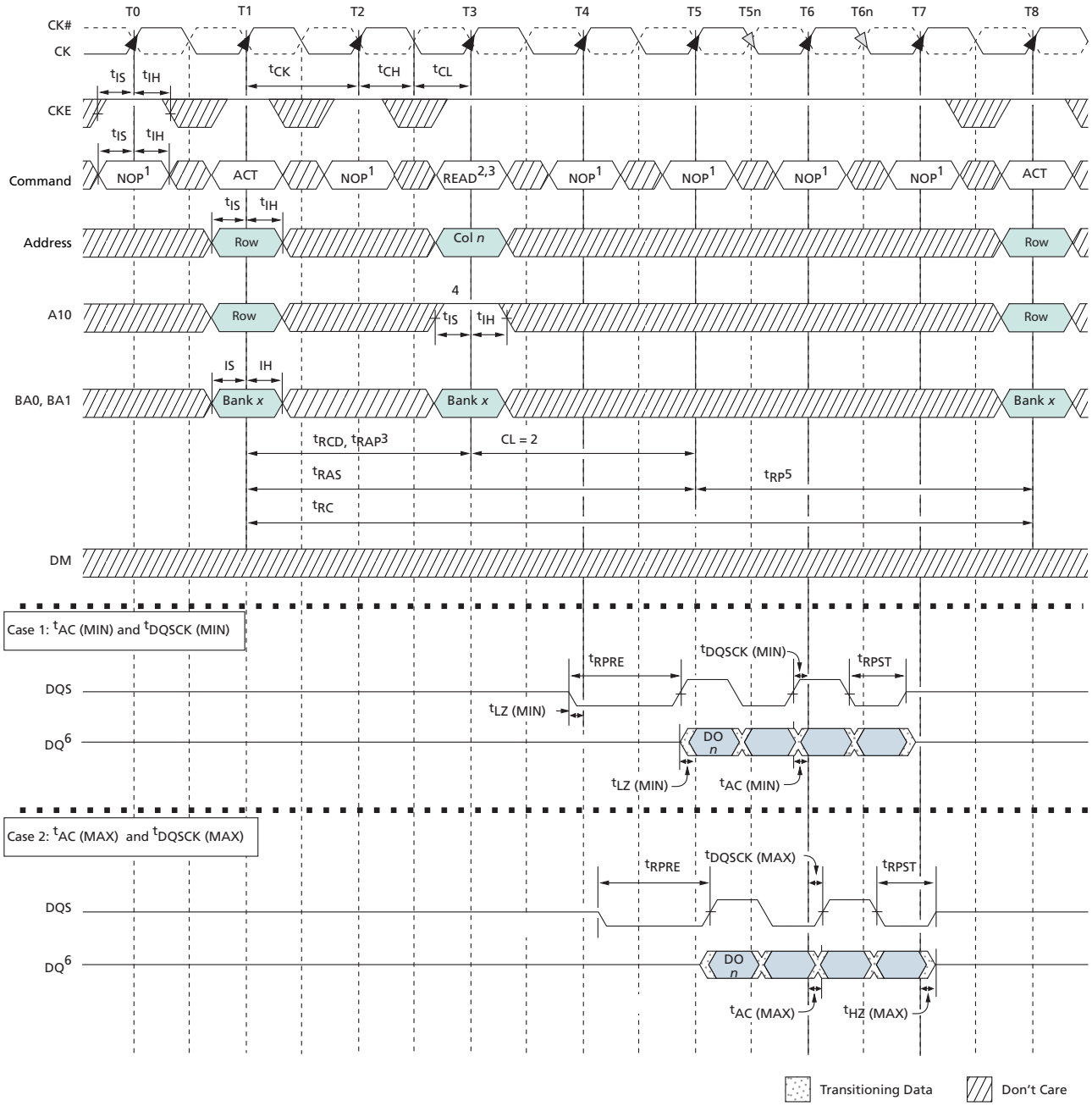
Figure 49: Bank READ – with Auto Precharge



Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. BL = 4.
3. The READ command can only be applied at T3 if ^{t}RAP is satisfied at T3.
4. Enable auto precharge.
5. ^{t}RP starts only after ^{t}RAS has been satisfied.
6. DO *n* = data-out from column *n;* subsequent elements are provided in the programmed order.
7. Refer to Figure 33 on page 61, Figure 34 on page 62, and Figure 35 on page 63 for detailed DQS and DQ timing.

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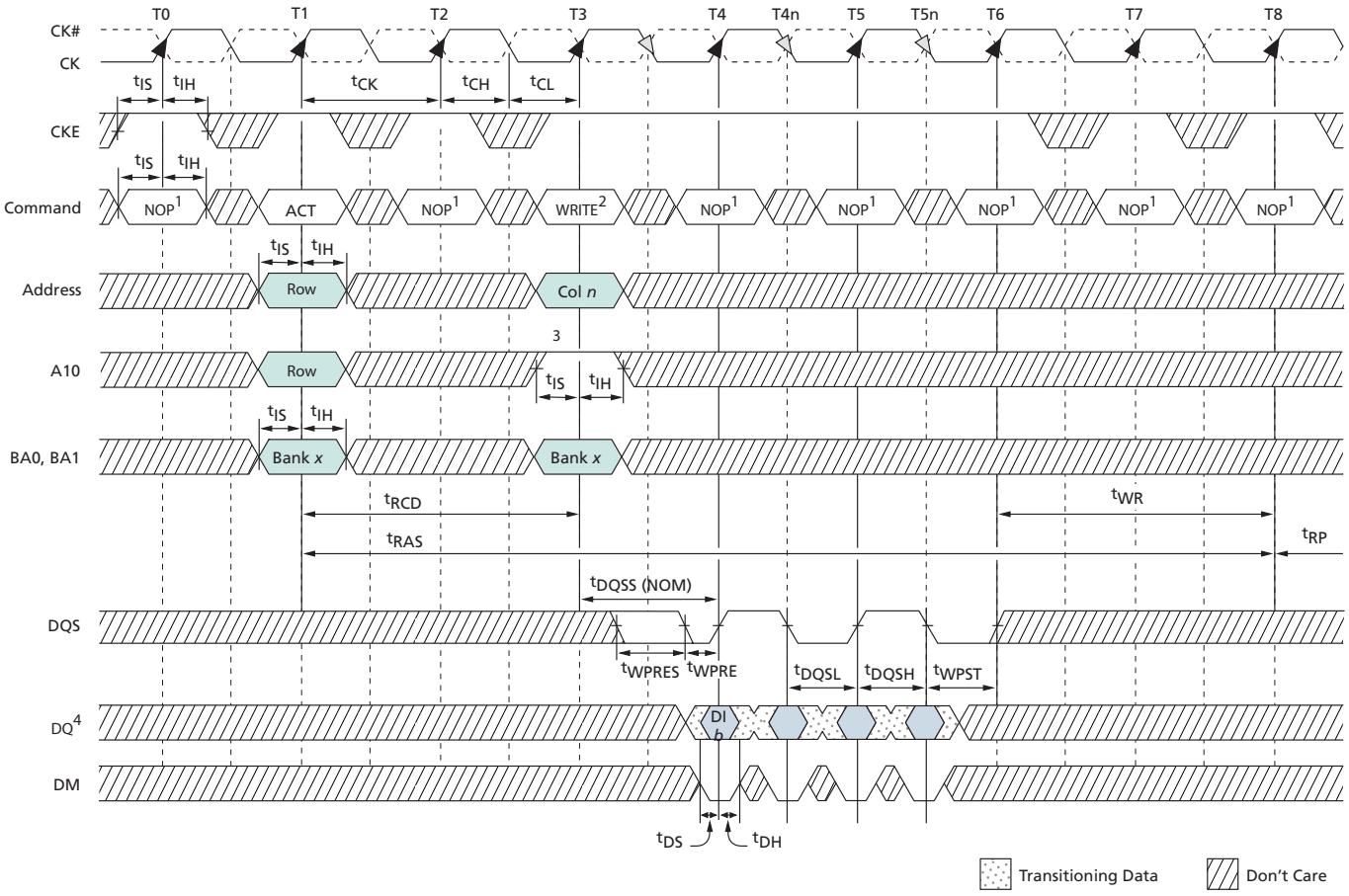
Figure 50: Bank WRITE – with Auto Precharge



Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. BL = 4.
3. Enable auto precharge.
4. DI *n* = data-out from column *n*; subsequent elements are provided in the programmed order.
5. See Figure 48 on page 76 for detailed DQ timing.

AUTO REFRESH

During auto refresh, the addressing is generated by the internal refresh controller. This makes the address bits a "Don't Care" during an AUTO REFRESH command. The DDR SDRAM requires AUTO REFRESH cycles at an average interval of ^{t}REFI (MAX).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM, meaning that the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 9 × ^{t}REFI(= ^{t}REFC). JEDEC specifications only support 8 × ^{t}REFI; Micron specifications exceed the JEDEC requirement by one clock. This maximum absolute interval is to allow future support for DLL updates, internal to the DDR SDRAM, to be restricted to AUTO REFRESH cycles, without allowing excessive drift in ^{t}AC between updates.

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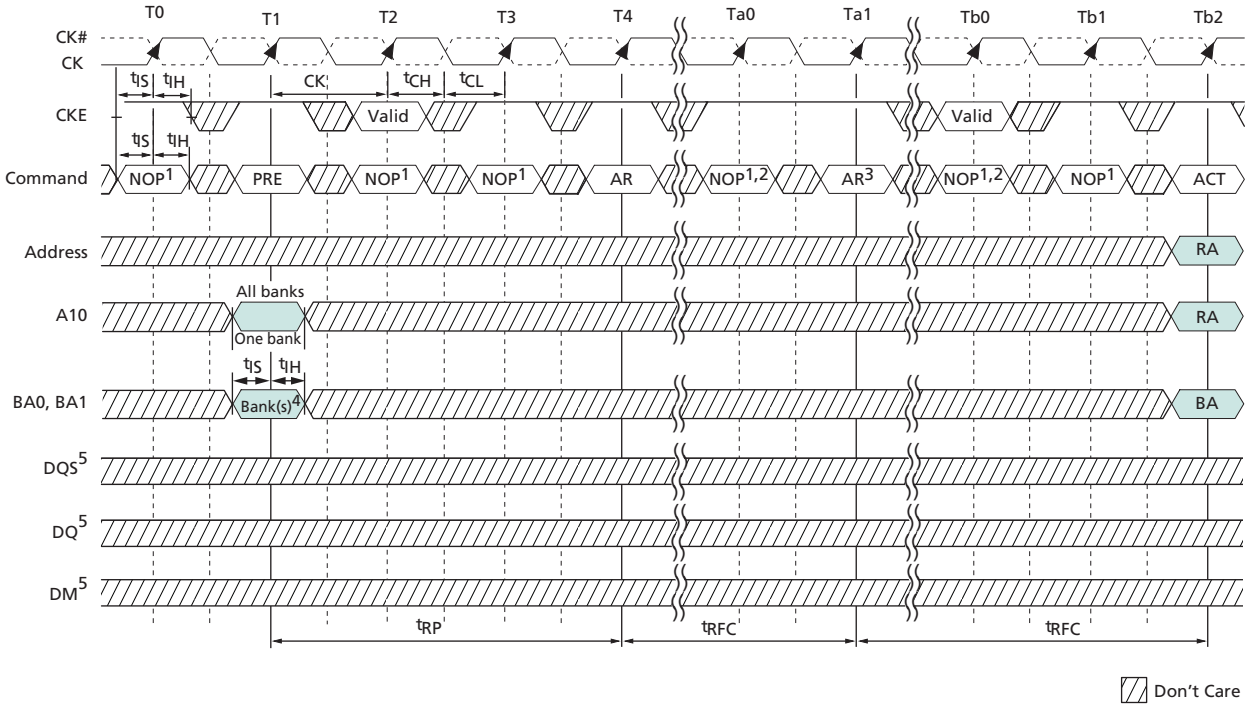
Although not a JEDEC requirement, to provide for future functionality features, CKE must be active (HIGH) during the AUTO REFRESH period. The AUTO REFRESH period begins when the AUTO REFRESH command is registered and ends ^{t}RFC later.

Figure 51: Auto Refresh Mode



Notes:
1. NOP commands are shown for ease of illustration; other valid commands may be possible at these times. CKE must be active during clock-positive transitions.
2. NOP or COMMAND INHIBIT are the only commands allowed until after ^{t}RFC time; CKE must be active during clock-positive transitions.
3. The second AUTO REFRESH is not required and is only shown as an example of two back-to-back AUTO REFRESH commands.
4. "Don't Care" if A10 is HIGH at this point; A10 must be HIGH if more than one bank is active (that is, must precharge all active banks).
5. DM, DQ, and DQS signals are all "Don't Care"/High-Z for the operations shown.

SELF REFRESH

When in the self refresh mode, the DDR SDRAM retains data without external clocking. The DLL is automatically disabled upon entering SELF REFRESH and is automatically enabled upon exiting SELF REFRESH (a DLL reset and 200 clock cycles must then occur before a READ command can be issued). Input signals except CKE are "Don't Care" during SELF REFRESH. V_{REF} voltage is also required for the full duration of SELF REFRESH.

The procedure for exiting SELF REFRESH requires a sequence of commands. First, CK and CK# must be stable prior to CKE going back HIGH. Once CKE is HIGH, the DDR SDRAM must have NOP commands issued for ^{t}XSNR because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements is to apply NOPs for ^{t}XSRD time, then a DLL RESET (via

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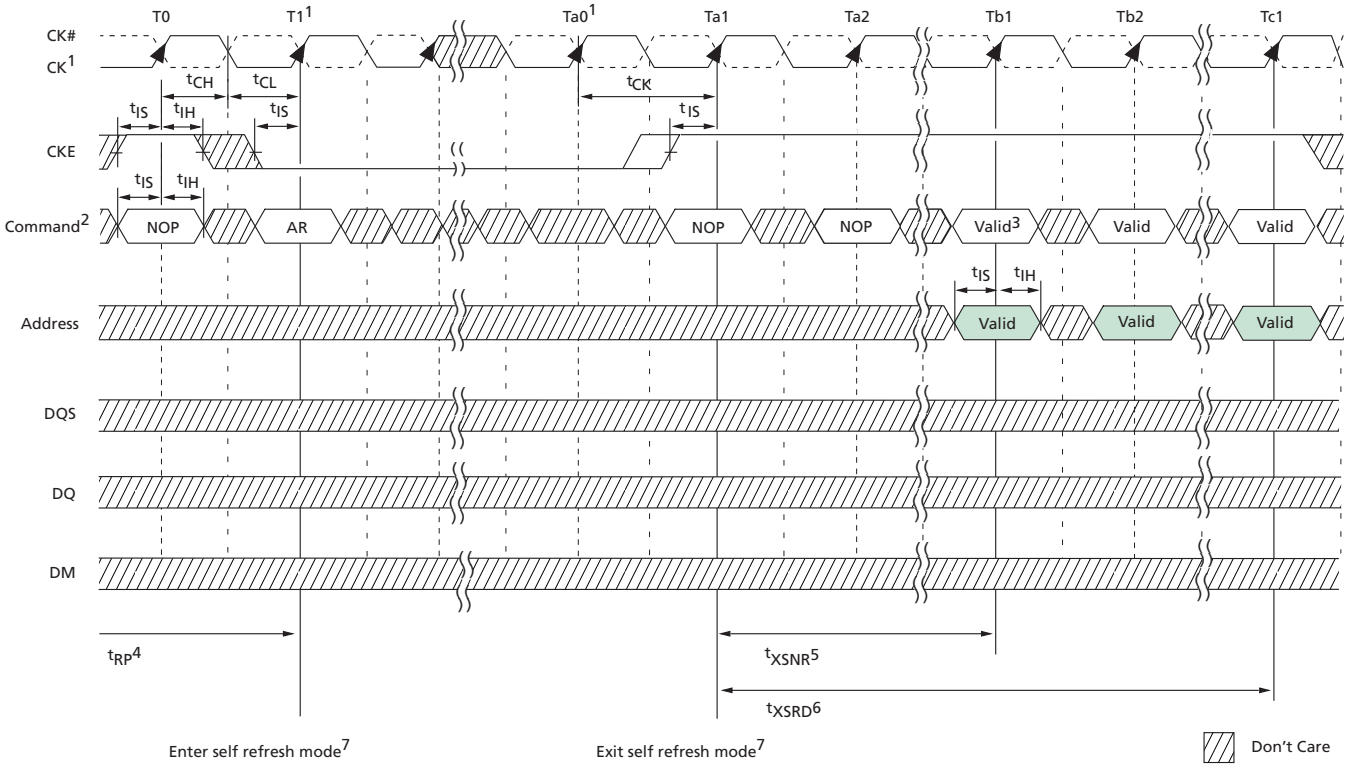
the extended mode register) and NOPs for 200 additional clock cycles before applying a READ. Any command other than a READ can be performed ^{t}XSNR (MIN) after the DLL reset. NOP or DESELECT commands must be issued during the ^{t}XSNR (MIN) time.

Figure 52: Self Refresh Mode



Notes:
1. Clock must be stable until after the SELF REFRESH command has been registered. A change in clock frequency is allowed before Ta0, provided it is within the specified ^{t}CK limits. Regardless, the clock must be stable before exiting self refresh mode—that is, the clock must be cycling within specifications by Ta0.
2. NOPs are interchangeable with DESELECT commands.
3. AUTO REFRESH is not required at this point but is highly recommended.
4. Device must be in the all banks idle state prior to entering self refresh mode.
5. ^{t}XSNR is required before any non-READ command can be applied; that is only NOP or DESELECT commands are allowed until Tb1.
6. ^{t}XSRD (200 cycles of a valid clock with CKE = HIGH) is required before any READ command can be applied.
7. As a general rule, any time self refresh mode is exited, the DRAM may not re-enter the self refresh mode until all rows have been refreshed via the AUTO REFRESH command at the distributed refresh rate, ^{t}REFI, or faster. However, the self refresh mode may be re-entered anytime after exiting if each of the following conditions is met:
   - 7a. The DRAM had been in the self refresh mode for a minimum of 200ms prior to exiting.
   - 7b. ^{t}XSNR and ^{t}XSRD are not violated.
   - 7c. At least two AUTO REFRESH commands are performed during each ^{t}REFI interval while the DRAM remains out of self refresh mode.
8. If the clock frequency is changed during self refresh mode, a DLL reset is required upon exit.
9. Once the device is initialized, V_{REF} must always be powered within specified range.

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Power-down (CKE Not Active)

Unlike SDR SDRAMs, DDR SDRAMs require CKE to be active at all times an access is in progress, from the issuing of a READ or WRITE command, until completion of the access. Thus a clock suspend is not supported. For READs, an access completion is defined when the read postamble is satisfied; for WRITEs, when the write recovery time (^{t}WR) is satisfied.

Power-down, as shown in Figure 53 on page 82, is entered when CKE is registered LOW and all criteria in Table 27 on page 38 are met. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when a row is active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK, CK#, and CKE. For maximum power savings, the DLL is frozen during precharge power-down mode. Exiting power-down requires the device to be at the same voltage and frequency as when it entered power-down. However, power-down duration is limited by the refresh requirements of the device (^{t}REFC).

While in power-down, CKE LOW and a stable clock signal must be maintained at the inputs of the DDR SDRAM, while all other input signals are “Don’t Care.” The power-down state is synchronously exited when CKE is registered HIGH (in conjunction with a NOP or DESELECT command). A valid executable command may be applied one clock cycle later.

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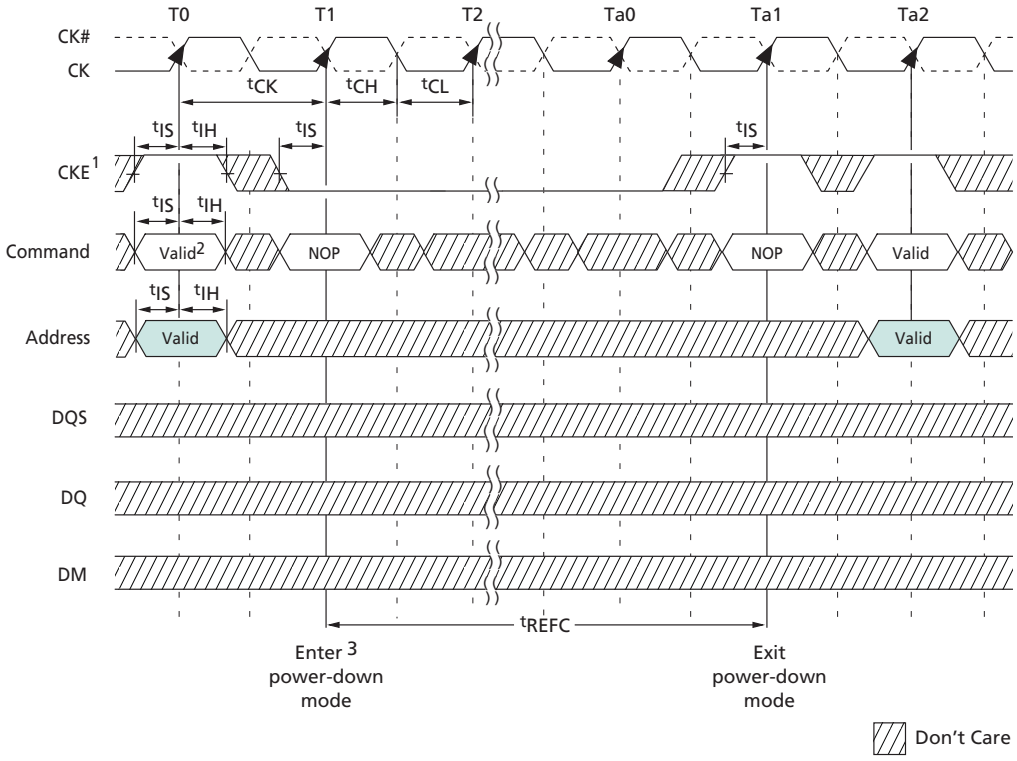
Figure 53: Power-Down Mode



Notes:
1. Once initialized, V_{REF} must always be powered within the specified range.
2. If this command is a PRECHARGE (or if the device is already in the idle state), then the power-down mode shown is precharge power-down. If this command is an ACTIVE (or if at least one row is already active), then the power-down mode shown is active power-down.
3. No column accesses are allowed to be in progress at the time power-down is entered.

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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