# THE DATASHEET OF

# MT46H16M16LFBF-75IT

www.win-source.net 0086-755-83957316

# Mobile DDR SDRAM

## MT46H16M16LF – 4 Meg x 16 x 4 banks
## MT46H8M32LF/LG – 2 Meg x 32 x 4 banks

For the latest data sheet, refer to Micron's Web site: www.micron.com

## Features

- VDD/VDDQ = 1.70–1.95V
- Bidirectional data strobe per byte of data (DQS)
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Four internal banks for concurrent operation
- Data masks (DM) for masking write data—one mask per byte
- Programmable burst lengths: 2, 4, or 8
- Concurrent auto precharge option supported
- Auto refresh and self refresh modes
- 1.8V LVCMOS compatible inputs
- On-chip temperature sensor to control self refresh rate
- Partial-array self refresh (PASR)
- Deep power-down (DPD)
- Selectable output drive (DS)
- Clock stop capability
- 64ms refresh period

**Table 1: Configuration Addressing**

| DQ Bus Width | Architecture | JEDEC-Standard Option | Reduced Page-Size Option |
|---|---|---|---|
| | Number of banks | 4 | 4 |
| | Bank address balls | BA0, BA1 | BA0, BA1 |
| x16 | Row address balls | A0–A12 | – |
| | Column address balls | A0–A8 | – |
| x32 | Row address balls | A0–A11 | A0–A12 |
| | Column address balls | A0–A8 | A0–A7 |

**Table 2: Key Timing Parameters**

| Speed Grade | Clock Rate (MHz) | | Access Time | |
|---|---|---|---|---|
| | CL = 2 | CL = 3 | CL = 2 | CL = 3 |
| -6 | 83.3 | 166 | 6.5ns | 5.0ns |
| -75 | 83.3 | 133 | 6.5ns | 6.0ns |

## Options — Marking

- VDD/VDDQ
  - 1.8V/1.8V — H
- Configuration
  - 16 Meg x 16 (4 Meg x 16 x 4 banks) — 16M16
  - 8 Meg x 32 (2 Meg x 32 x 4 banks) — 8M32
- Row size option
  - JEDEC-standard option — LF
  - Reduced page-size option[2] — LG
- Plastic "green" packages
  - 60-ball VFBGA 8mm x 9mm[1] — BF
  - 90-ball VFBGA 8mm x 13mm[2] — B5
- Timing – cycle time
  - 6ns at CL = 3 — -6
  - 7.5ns at CL = 3 — -75
- Power
  - Standard — None
  - Low IDD2P/IDD6 — L
- Operating temperature range
  - Commercial (0°C to +70°C) — None
  - Industrial (–40°C to +85°C) — IT
- Design revision — :A

Notes: 1. Only available for x16 configuration.
2. Only available for x32 configuration.


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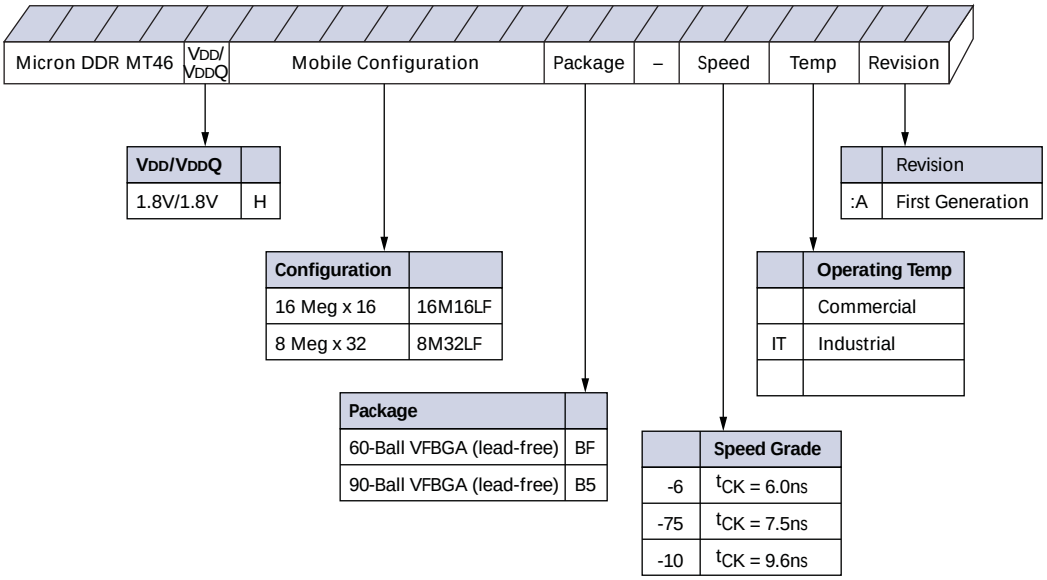
**Figure 1: 256Mb Mobile DDR Part Numbering**

Example Part Number: MT46H16M16LFXX-75IT :A




## FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. For a quick conversion of an FBGA code, see the FBGA part marking decoder at www.micron.com/decoder.

## General Description

The 256Mb Mobile DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 268,435,456 bits. It is internally configured as a quad-bank DRAM. On the x16 device, each of the 67,108,864-bit banks is organized as 8,192 rows by 512 columns by 16 bits. On the x32 device, each of the 67,108,864-bit banks is organized as 4,096 rows by 512 columns by 32 bits.

The 256Mb Mobile DDR SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O balls. A single read or write access for the 256Mb Mobile DDR SDRAM effectively consists of a single 2*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O balls.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the Mobile DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. The x16 offering has two data strobes: one for the lower byte and one for the upper byte. The x32 offering has four data strobes, one per byte.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The 256Mb Mobile DDR SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the Mobile DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The Mobile DDR SDRAM provides for programmable READ or WRITE burst lengths of 2, 4, or 8. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDR SDRAM, the pipelined, multibank architecture of Mobile DDR SDRAM enables concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving power-down mode. Deep power-down mode is offered to achieve maximum power reduction by eliminating the power draw of the memory array. Data will not be retained when the device enters DPD mode.

Self refresh mode offers temperature compensation through an on-chip temperature sensor and partial-array self refresh, which enables users to achieve additional power savings. The temperature sensor is enabled by default, and the partial-array self refresh can be programmed through the extended mode register.

Notes:
1. Throughout the data sheet, various figures and text refer to DQs as “DQ.” The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise.
2. Complete functionality is described throughout the document, and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
3. Any specific requirement takes precedence over a general statement.


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# Functional Block Diagrams

## Figure 2: Functional Block Diagram (16 Meg x 16)

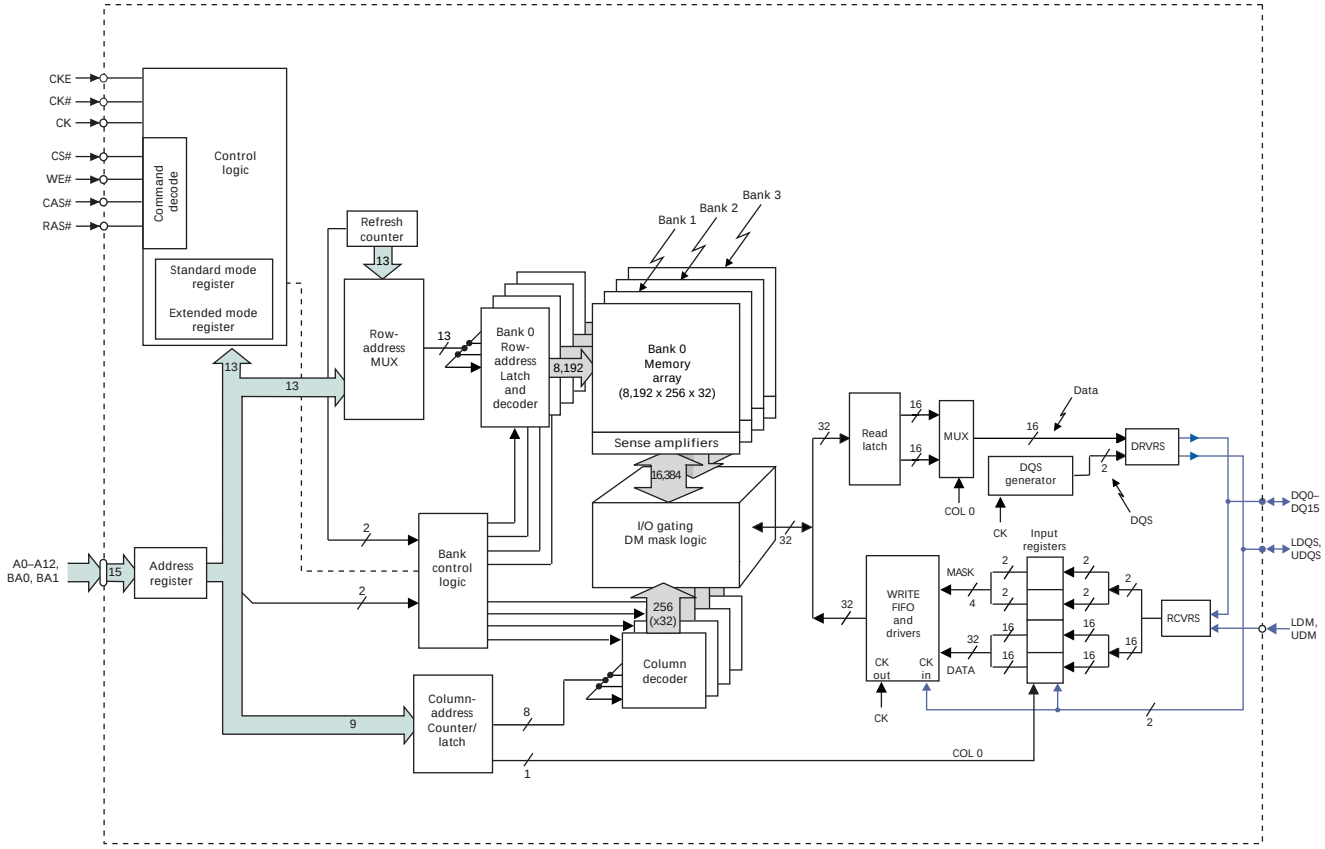



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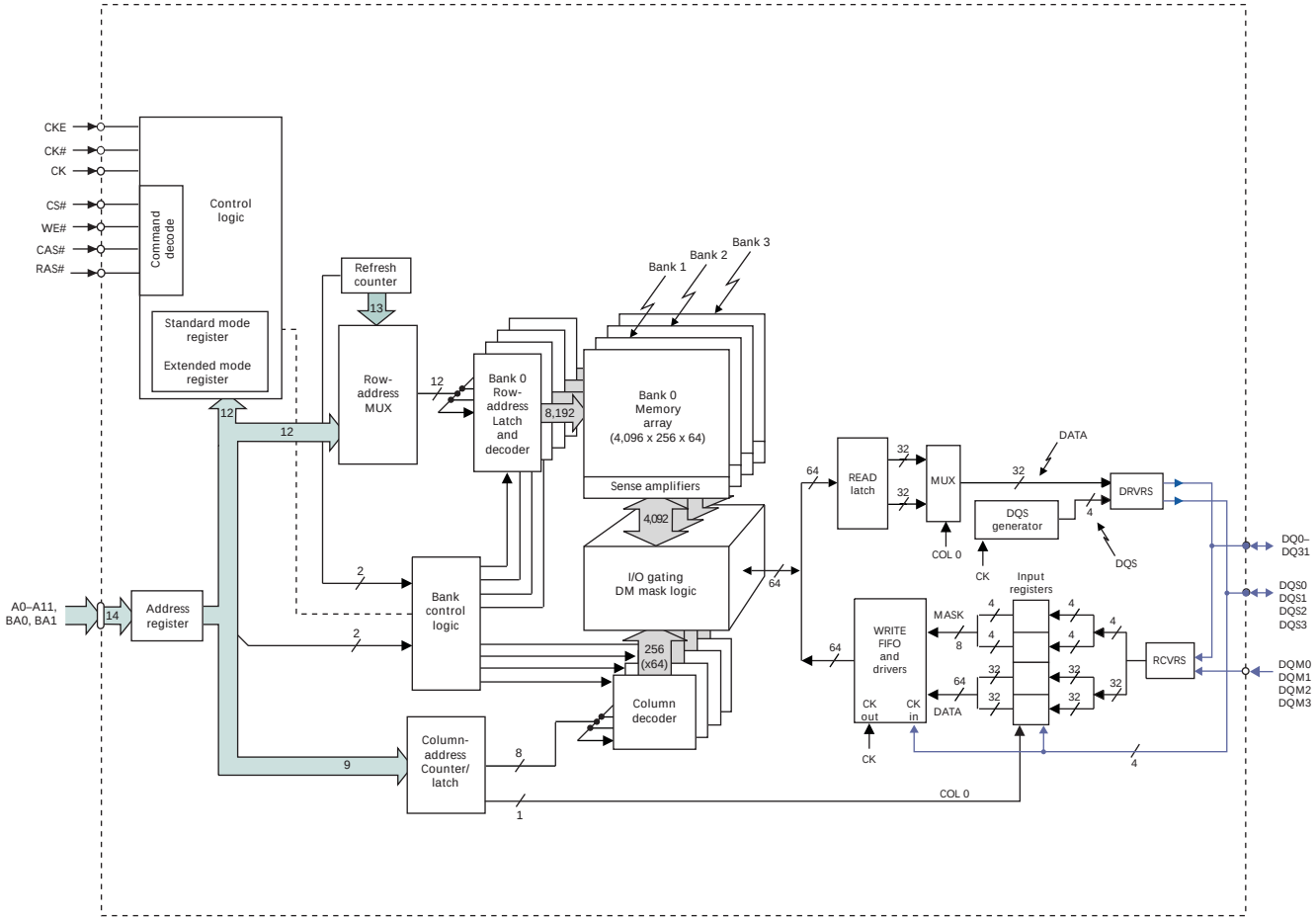
**Figure 3: Functional Block Diagram (8 Meg x 32)**




Notes: 1. JEDEC-standard x32 DQ configuration shown.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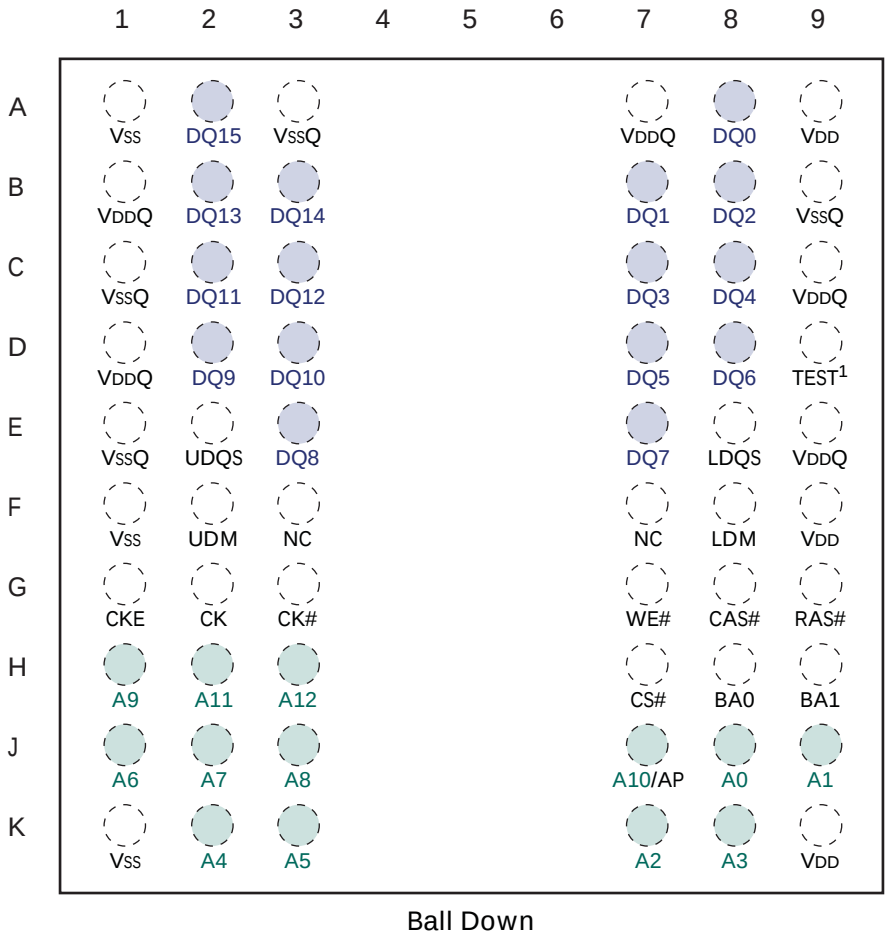
## Ballouts and Ball Descriptions

**Figure 4: 60-Ball VFBGA Ball Assignments – 8mm x 9mm (Top View)**




Notes: 1. D9 is a test pin that must be connected to VSS or VSSQ in normal operation.


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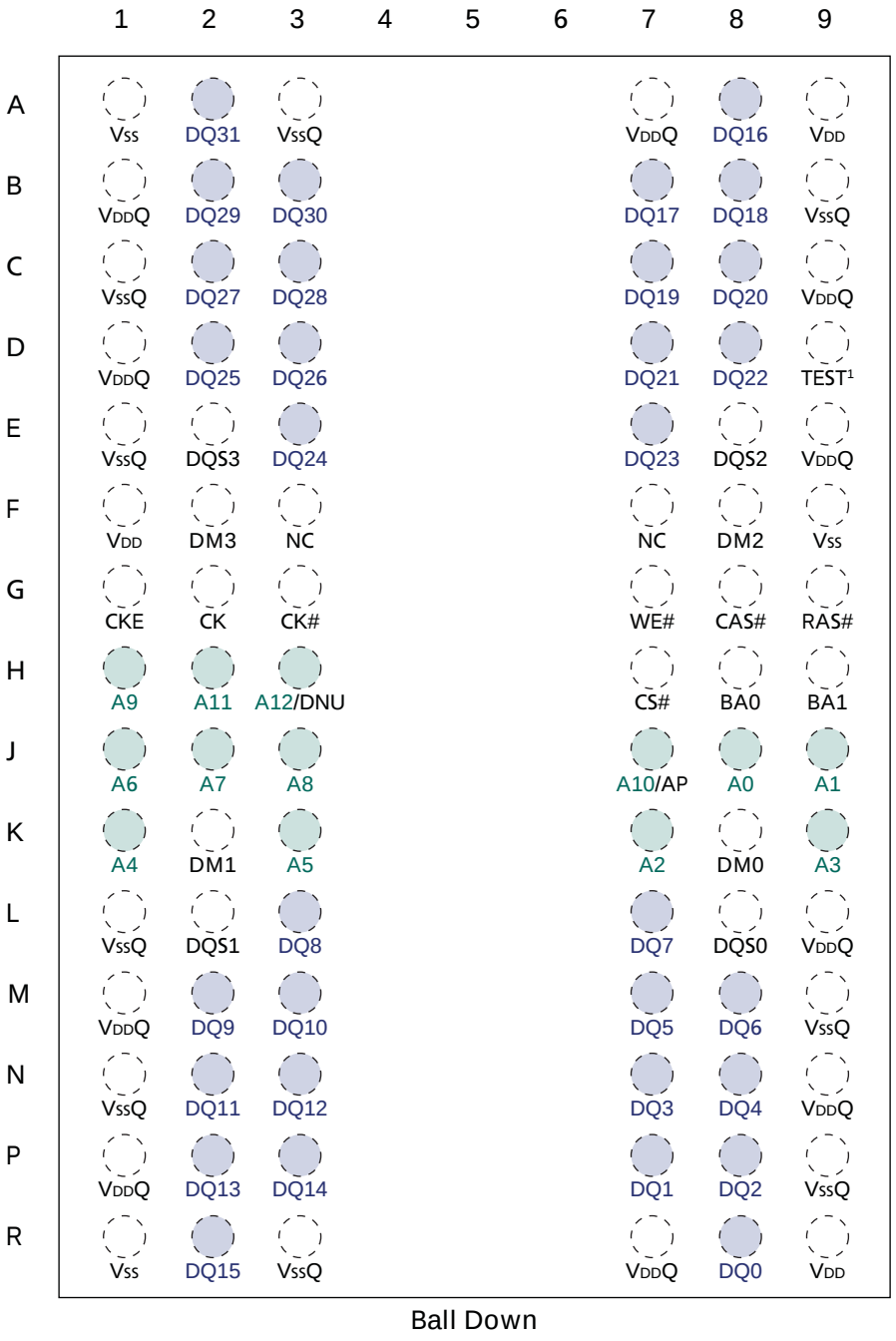
**Figure 5: 90-Ball VFBGA Ball Assignments – 8mm x 13mm (Top View)**




Notes: 1. D9 is a test pin that must be connected to VSS or VSSQ in normal operation.


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**Table 3: 60-Ball VFBGA Ball Descriptions**

| Ball Numbers | Symbol | Type | Description |
|---|---|---|---|
| G2, G3 | CK, CK# | Input | **Clock**: CK is the system clock input. CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Input and output data is referenced to the crossing of CK and CK# (both directions of the crossing). |
| G1 | CKE | Input | **Clock enable**: CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Taking CKE LOW enables PRECHARGE power-down and SELF REFRESH operations (all banks idle) or ACTIVE power-down (row active in any bank). CKE is synchronous for all functions except SELF REFRESH exit. All input buffers (except CKE) are disabled during power-down and self refresh modes. |
| H7 | CS# | Input | **Chip select**: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code. |
| G9, G8, G7 | RAS#, CAS#, WE# | Input | **Command inputs**: RAS#, CAS#, and WE# (along with CS#) define the command being entered. |
| F2, F8 | UDM, LDM | Input | **Input data mask**: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. For the x16, LDM is DM for DQ0–DQ7, and UDM is DM for DQ8–DQ15. |
| H8, H9 | BA0, BA1 | Input | **Bank address inputs**: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0 and BA1 also determine which mode register (standard mode register or extended mode register) is loaded during a LOAD MODE REGISTER command. |
| J8, J9, K7, K8, K2, K3, J1, J2, J3, H1, J7, H2, H3 | A0–A12 | Input | **Address inputs**: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. During a PRECHARGE command, A10 determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0, BA1) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command. |
| A8, B7, B8, C7, C8, D7, D8, E7, E3, D2, D3, C2, C3, B2, B3, A2 | DQ0–DQ15 | I/O | **Data input/output**: Data bus for x16. |
| E2, E8 | UDQS, LDQS | I/O | **Data strobe**: Output with read data, input with write data. DQS is edge-aligned with read data, center-aligned with write data. Data strobe is used to capture data. |
| A7, B1, C9, D1, E9 | $V_{DD}Q$ | Supply | DQ power supply. |
| A3, B9, C1, E1 | $V_{SS}Q$ | Supply | DQ ground. |
| A9, F9, K9 | $V_{DD}$ | Supply | Power supply. |
| A1, F1, K1 | $V_{SS}$ | Supply | Ground. |
| F3, F7 | NC | – | **No connect**: May be left unconnected. |
| D9 | TEST | – | Test pin that must be connected to $V_{SS}$ or $V_{SS}Q$ in normal operation. |


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**Table 4: 90-Ball VFBGA Ball Description**

| Ball Numbers | Symbol | Type | Description |
|---|---|---|---|
| G2, G3 | CK, CK# | Input | **Clock**: CK is the system clock input. CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Input and output data is referenced to the crossing of CK and CK# (both directions of the crossing). |
| G1 | CKE | Input | **Clock enable**: CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Taking CKE LOW enables PRECHARGE power-down and SELF REFRESH operations (all banks idle) or ACTIVE power-down (row active in any bank). CKE is synchronous for all functions except SELF REFRESH exit. All input buffers (except CKE) are disabled during power-down and self refresh modes. |
| H7 | CS# | Input | **Chip select**: CS# enables the command decoder (registered LOW) and disables the command decoder (registered HIGH). All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code. |
| G9, G8, G7 | RAS#, CAS#, WE# | Input | **Command inputs**: RAS#, CAS#, and WE# (along with CS#) define the command being entered. |
| K8, K2, F8, F2 | DM0–DM3 | Input | **Input data mask**: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM balls are input-only, the DM loading is designed to match that of DQ and DQS balls. For the x32, DM0 is DM for DQ0–DQ7; DM1 is DM for DQ8–DQ15; DM2 is DM for DQ16–DQ23; and DM3 is DM for DQ24–DQ31. |
| H8, H9 | BA0, BA1 | Input | **Bank address inputs**: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0 and BA1 also determine which mode register (standard mode register or extended mode register) is loaded during a LOAD MODE REGISTER command. |
| J8, J9, K7, K9, K1, K3, J1, J2, J3, H1, J7, H2 | A0–A11 | Input | **Address inputs**: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ or WRITE commands, to select one location out of the memory array in the respective bank. During a PRECHARGE command, A10 determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0, BA1) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command. |
| H3 | A12/DNU | Input | A12 is an address input for the LG reduced page-size option (see "Options" on page 1). Leave as DNU for JEDEC-standard option. |
| R8, P7, P8, N7, N8, M7, M8, L7, L3, M2, M3, N2, N3, P2, P3, R2, A8, B7, B8, C7, C8, D7, D8, E7, E3, D2, D3, C2, C3, B2, B3, A2 | DQ0–DQ31 | I/O | **Data input/output**: Data bus for x32. |
| L8, L2, E8, E2 | DQS0–DQS3 | I/O | **Data strobe**: Output with read data, input with write data. DQS is edge-aligned with read data, center-aligned with write data. Data strobe is used to capture data. |
| A7, B1, C9, D1, E9, L9, M1, N9, P1, R7 | $V_{DD}Q$ | Supply | DQ power supply. |


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**Table 4: 90-Ball VFBGA Ball Description (Continued)**

| Ball Numbers | Symbol | Type | Description |
|---|---|---|---|
| A3, B9, C1, E1, L1, M9, N1, P9, R3 | $V_{SS}Q$ | Supply | DQ ground. |
| A9, F1, R9 | $V_{DD}$ | Supply | Power supply |
| A1, F9, R1 | $V_{SS}$ | Supply | Ground. |
| F3, F7 | NC | – | **No connect**: May be left unconnected. |
| D9 | TEST | – | Test pin that must be connected to $V_{SS}$ or $V_{SS}Q$ in normal operation. |


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# Functional Description

The 256Mb Mobile DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 268,435,456 bits. It is internally configured as a quad-bank DRAM. Each of the 67,108,864-bit banks on the x16 is organized as 8,192 rows by 512 columns by 16 bits. Each of the 67,108,864-bit banks on the x32 is organized as 4,096 rows by 512 columns by 32 bits for the standard addressing configuration.

The 256Mb Mobile DDR SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n*-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O balls. Single read or write access for the 256Mb Mobile DDR SDRAM consists of a single 2*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O balls.

Read and write accesses to the Mobile DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The DLL circuit that is typically used on standard DDR devices is not necessary on the Mobile DDR SDRAM. It has been omitted to save power.

Prior to normal operation, the Mobile DDR SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions, and device operation.

## Initialization

Mobile DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

If there is an interruption to the device power, the initialization routine must be followed to ensure proper functionality of the Mobile DDR SDRAM. The clock stop feature is not available until the device has been properly initialized.

To properly initialize the Mobile DDR SDRAM, this sequence must be followed:

1. The core power ($V_{DD}$) and I/O power ($V_{DD}Q$) must be brought up simultaneously. It is recommended that $V_{DD}$ and $V_{DD}Q$ be from the same power source, or $V_{DD}Q$ must never exceed $V_{DD}$. Assert and hold CKE HIGH.
2. After power supply voltages are stable and the CKE has been driven HIGH, it is safe to apply the clock.
3. After the clock is stable, a 200µs (MIN) delay is required by the Mobile DDR SDRAM prior to applying an executable command. During this time, a NOP or DESELECT command must be issued on the command bus.
4. Issue a PRECHARGE ALL command.
5. Issue a NOP or DESELECT command for at least $^{t}$RP time.
6. Issue an AUTO REFRESH command followed by a NOP or DESELECT command for at least $^{t}$RFC time. Issue a second AUTO REFRESH command followed by a NOP or DESELECT command for at least $^{t}$RFC time. As part of the initialization sequence, two AUTO REFRESH commands must be issued.


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7. Using the LOAD MODE REGISTER command, load the standard mode register as desired.
8. Issue a NOP or DESELECT command for at least $^{t}$MRD time.
9. Using the LOAD MODE REGISTER command, load the extended mode register to the desired operating modes. Note that the sequence in which the standard and extended mode registers are programmed is not critical.
10. Issue NOP or DESELECT commands for at least $^{t}$MRD time.

The Mobile DDR SDRAM has been properly initialized and is ready to receive any valid command.

# Register Definition

## Mode Registers

The mode registers are used to define the specific mode of operation of the Mobile DDR SDRAM. Two mode registers are used to specify the operational characteristics of the device.

## Standard Mode Register

The standard mode register bit definition enables the selection of burst length, burst type, CAS latency, and operating mode, as shown in Figure 6 on page 16. Reserved states should not be used, as this may result in setting the device into an unknown state or cause incompatibility with future versions of Mobile DDR SDRAM. The standard mode register is programmed via the LOAD MODE REGISTER command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again, the device goes into deep power-down mode, or the device loses power.

Reprogramming the mode register will not alter the contents of the memory, provided it is performed correctly. The mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait before initiating the subsequent operation. Violating any of these requirements will result in unspecified operation.

### Burst Length

Read and write accesses to the Mobile DDR SDRAM are burst oriented; the burst length is programmable. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both sequential and interleaved burst types.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap when a boundary is reached. The block is uniquely selected by A1–A*i* when BL = 2, by A2–A*i* when BL = 4, and by A3–A*i* when BL = 8, where A*i* is the most significant column address bit for a given configuration. The remaining (least significant) address bits are used to specify the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

### Burst Type

Accesses within a given burst may be programmed either to be sequential or interleaved via the standard mode register.

The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address (see Table 5 on page 17).


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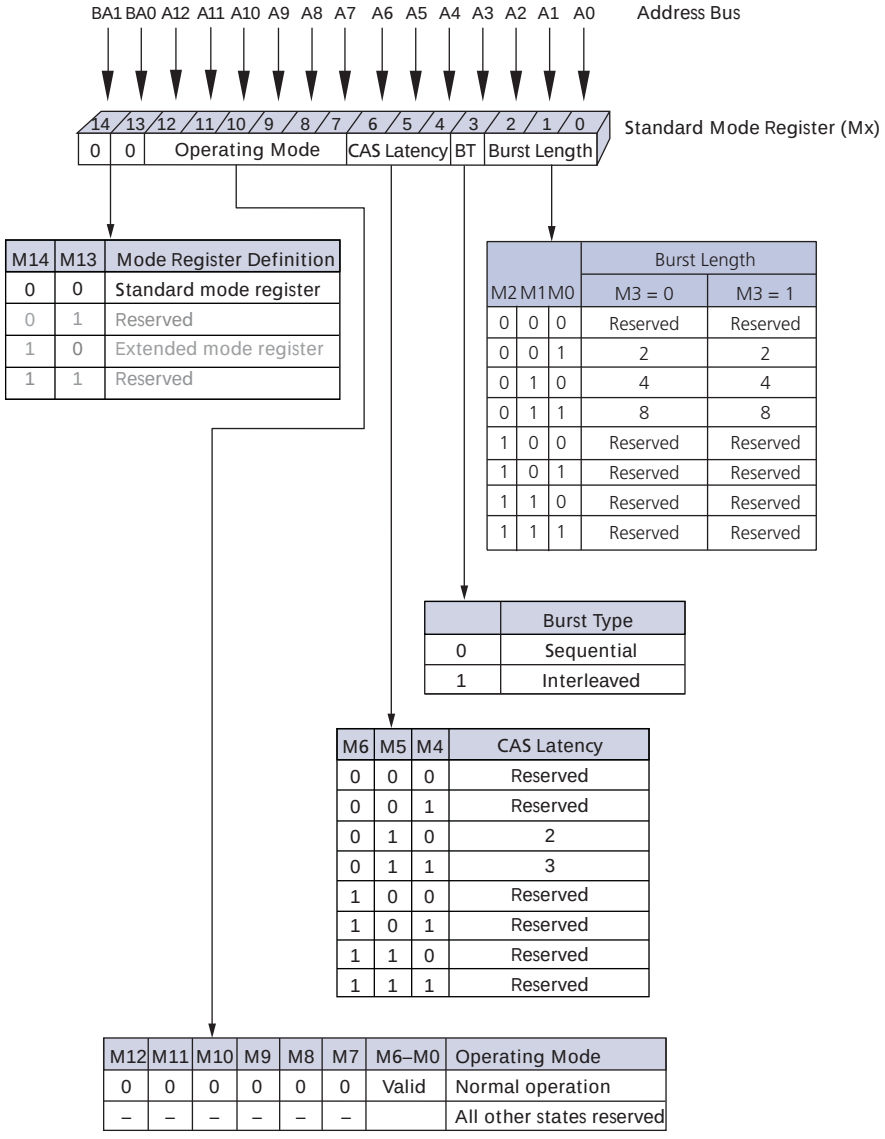
## CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first output data. The latency can be set to two or three clocks, as shown in Figure 7 on page 18.

For CAS latency three (CL = 3), if the READ command is registered at clock edge *n*, then the data will nominally be available at (*n* + 2 clocks + $^{t}$AC). For CL = 2, if the READ command is registered at clock edge *n*, then the data will be nominally be available at (*n* + 1 clock + $^{t}$AC).

**Figure 6: Standard Mode Register Definition**




| M14 | M13 | Mode Register Definition |
|---|---|---|
| 0 | 0 | Standard mode register |
| 0 | 1 | Reserved |
| 1 | 0 | Extended mode register |
| 1 | 1 | Reserved |

| | | | Burst Length | |
|---|---|---|---|---|
| M2 | M1 | M0 | M3 = 0 | M3 = 1 |
| 0 | 0 | 0 | Reserved | Reserved |
| 0 | 0 | 1 | 2 | 2 |
| 0 | 1 | 0 | 4 | 4 |
| 0 | 1 | 1 | 8 | 8 |
| 1 | 0 | 0 | Reserved | Reserved |
| 1 | 0 | 1 | Reserved | Reserved |
| 1 | 1 | 0 | Reserved | Reserved |
| 1 | 1 | 1 | Reserved | Reserved |

| | Burst Type |
|---|---|
| 0 | Sequential |
| 1 | Interleaved |

| M6 | M5 | M4 | CAS Latency |
|---|---|---|---|
| 0 | 0 | 0 | Reserved |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | Reserved |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

| M12 | M11 | M10 | M9 | M8 | M7 | M6–M0 | Operating Mode |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | Valid | Normal operation |
| – | – | – | – | – | – | | All other states reserved |


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**Table 5: Burst Definition Table**

| Burst Length | Starting Column Address | | | | Order of Accesses Within a Burst | |
|---|---|---|---|---|---|---|
| | | | | | Type = Sequential | Type = Interleaved |
| 2 | | | | **A0** | | |
| | | | | 0 | 0-1 | 0-1 |
| | | | | 1 | 1-0 | 1-0 |
| 4 | | | **A1** | **A0** | | |
| | | | 0 | 0 | 0-1-2-3 | 0-1-2-3 |
| | | | 0 | 1 | 1-2-3-0 | 1-0-3-2 |
| | | | 1 | 0 | 2-3-0-1 | 2-3-0-1 |
| | | | 1 | 1 | 3-0-1-2 | 3-2-1-0 |
| 8 | | **A2** | **A1** | **A0** | | |
| | | 0 | 0 | 0 | 0-1-2-3-4-5-6-7 | 0-1-2-3-4-5-6-7 |
| | | 0 | 0 | 1 | 1-2-3-4-5-6-7-0 | 1-0-3-2-5-4-7-6 |
| | | 0 | 1 | 0 | 2-3-4-5-6-7-0-1 | 2-3-0-1-6-7-4-5 |
| | | 0 | 1 | 1 | 3-4-5-6-7-0-1-2 | 3-2-1-0-7-6-5-4 |
| | | 1 | 0 | 0 | 4-5-6-7-0-1-2-3 | 4-5-6-7-0-1-2-3 |
| | | 1 | 0 | 1 | 5-6-7-0-1-2-3-4 | 5-4-7-6-1-0-3-2 |
| | | 1 | 1 | 0 | 6-7-0-1-2-3-4-5 | 6-7-4-5-2-3-0-1 |
| | | 1 | 1 | 1 | 7-0-1-2-3-4-5-6 | 7-6-5-4-3-2-1-0 |


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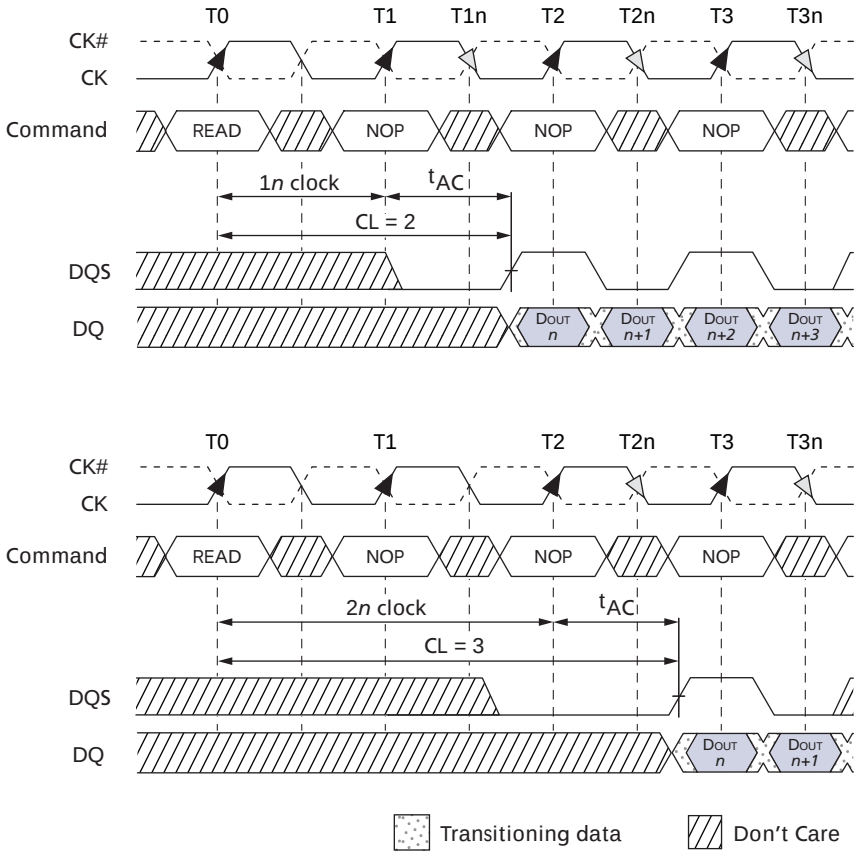
**Figure 7: CAS Latency**




Notes: 1. BL = 4 in the cases shown.
2. Shown with nominal $^{t}$AC and nominal $^{t}$DQSQ.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### Operating Mode

The normal operating mode is selected by issuing a LOAD MODE REGISTER command with bits A7–A11 (x32) or A7–A12 (x16) each set to zero and bits A0–A6 set to the desired values.

All other combinations of values for A7–A11/A12 are reserved for future use and/or test modes. Test modes and reserved states should not be used, because unknown operation or incompatibility with future versions may result.

## Extended Mode Register

The extended mode register controls functions specific to Mobile SDRAM operation. These additional functions include drive strength, temperature-compensated self refresh, and partial-array self refresh.

The extended mode register is programmed via the LOAD MODE REGISTER command (with BA0 = 0 and BA1 = 1) and will retain the stored information until it is programmed again, the device goes into deep power-down mode, or the device loses power.

### Temperature-Compensated Self Refresh

On this version of the Mobile DDR SDRAM, a temperature sensor is implemented for automatic control of the SELF REFRESH oscillator. Programming the TCSR bits will have no effect on the device. The SELF REFRESH oscillator will continue to refresh at the factory-programmed optimal rate for the device temperature.

### Partial-Array Self Refresh

For further power savings during SELF REFRESH, the partial-array self refresh (PASR) feature enables the controller to select the amount of memory that will be refreshed during SELF REFRESH.

**Table 6: Partial-Array Self Refresh Options**

| Memory | Bank |
|---|---|
| Full array | Banks 0, 1, 2, and 3 |
| Half array | Banks 0 and 1 |
| Quarter array | Bank 0 |
| Eighth array | Bank 0 with row address MSB = 0 |
| Sixteenth array | Bank 0 with row address MSB = 0 and MSB - 1 = 0 |

WRITE and READ commands can still occur during standard operation, but only the selected regions of the array will be refreshed during SELF REFRESH. Data in regions that are not selected will be lost.

### Output Driver Strength

Because the Mobile DDR SDRAM is designed for use in smaller systems that are typically point-to-point connections, an option to control the drive strength of the output buffers is provided. Drive strength should be selected based on expected loading of the memory bus. There are four allowable settings for the output drivers: 25Ω, 55Ω, 80Ω, and 100Ω internal impedance.


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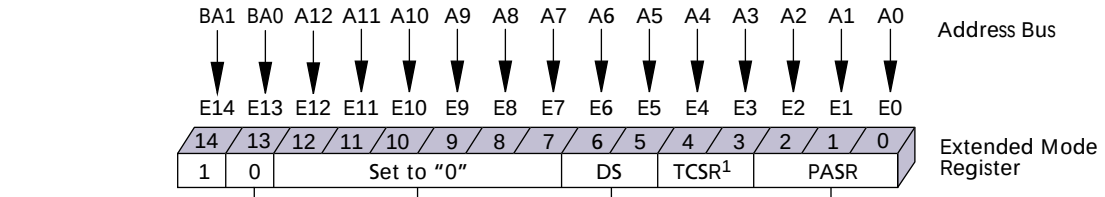
**Figure 8: Extended Mode Register**




| E14 | E13 | Mode Register Definition |
|---|---|---|
| 0 | 0 | Standard mode register |
| 0 | 1 | Reserved |
| 1 | 0 | Extended mode register |
| 1 | 1 | Reserved |

| E6 | E5 | Driver Strength |
|---|---|---|
| 0 | 0 | Full-strength driver |
| 0 | 1 | Half-strength driver |
| 1 | 0 | Quarter-strength driver |
| 1 | 1 | One-eighth-strength driver |

| E12 | E11 | E10 | E9 | E8 | E7 | E6–E0 | Operating Mode |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | Valid | Normal operation |
| – | – | – | – | – | – | – | All other states reserved |

| E2 | E1 | E0 | Partial-Array Self Refresh Coverage |
|---|---|---|---|
| 0 | 0 | 0 | Full array |
| 0 | 0 | 1 | Half array |
| 0 | 1 | 0 | Quarter array |
| 0 | 1 | 1 | Reserved |
| 1 | 0 | 0 | Reserved |
| 1 | 0 | 1 | One-eighth array |
| 1 | 1 | 0 | One-sixteenth array |
| 1 | 1 | 1 | Reserved |

Notes: 1. On-die temperature sensor is used in place of TCSR. Setting these bits will have no effect.

## Stopping the External Clock

One method of controlling the power efficiency in applications is to throttle the clock that controls the DDR SDRAM. Control the clock in two ways:

- Change the clock frequency.
- Stop the clock.

The Mobile DDR SDRAM enables the clock to change frequency during operation only if all the timing parameters are met and all refresh requirements are satisfied.

The clock can be stopped if no DRAM operations are in progress that would be affected by this change. Any DRAM operation already in process must be completed before entering clock stop mode; this includes the following timings: $^{t}$RCD, $^{t}$RP, $^{t}$RFC, $^{t}$MRD, $^{t}$WR, and all data-out for READ bursts.

For example, if a WRITE or a READ is in progress, the entire data burst must be complete prior to stopping the clock. For READs, a burst completion is defined when the read postamble is satisfied. For WRITEs, a burst completion is defined when the write postamble and $^{t}$WR or $^{t}$WTR are satisfied.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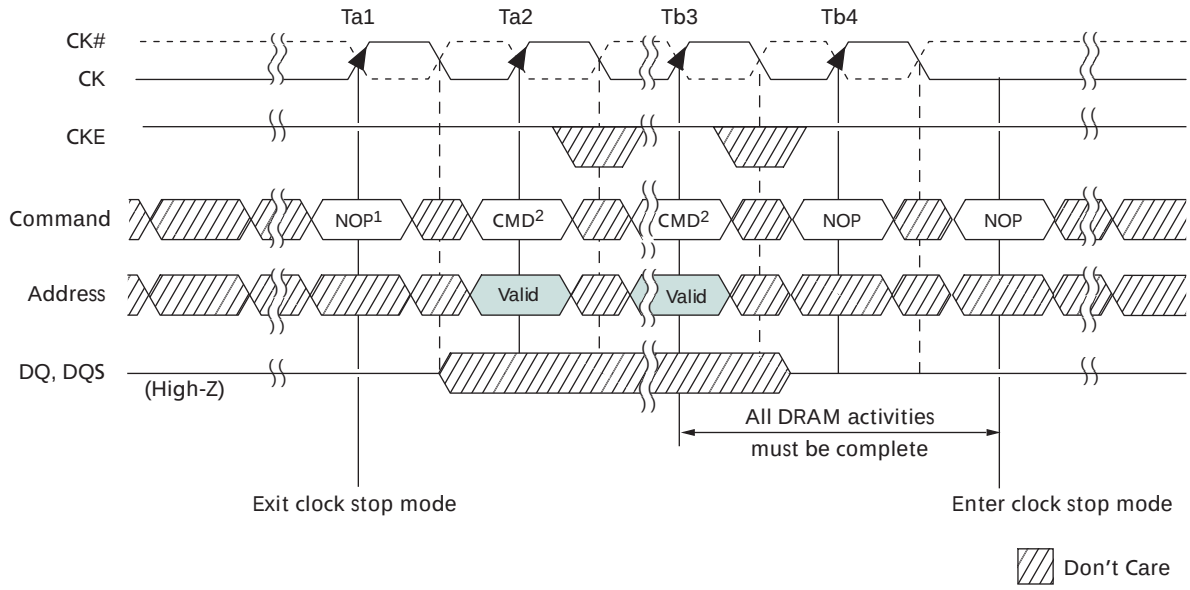
CKE must be held HIGH with CK = LOW and CK# = HIGH for the full duration of the clock stop mode. One clock cycle and at least one NOP or DESELECT is required after the clock is restarted before a valid command can be issued. Figure 9 on page 21 illustrates the clock stop mode.

**Figure 9: Clock Stop Mode**




Notes:
1. Prior to Ta1, the device is in clock stop mode. To exit, at least one NOP is required before any valid command is issued.
2. Any valid command is allowed; device is not in clock stop mode.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# Commands

Tables 7 and 8 provide a quick reference of available commands. This is followed by a description of each command. Three additional truth tables provide CKE commands and current/next state information (see Table 9 on page 51, Table 10 on page 52, and Table 11 on page 54).

**Table 7: Truth Table – Commands**
Notes 1 and 2 apply to all commands

| Name (Function) | CS# | RAS# | CAS# | WE# | Address | Notes |
|---|---|---|---|---|---|---|
| DESELECT (NOP) | H | X | X | X | X | 3 |
| NO OPERATION (NOP) | L | H | H | H | X | 3 |
| ACTIVE (select bank and activate row) | L | L | H | H | Bank/row | 4 |
| READ (select bank and column, and start READ burst) | L | H | L | H | Bank/column | 5 |
| WRITE (select bank and column, and start WRITE burst) | L | H | L | L | Bank/column | 5 |
| BURST TERMINATE or deep power-down (enter deep power-down mode) | L | H | H | L | X | 6, 7 |
| PRECHARGE (deactivate row in bank or banks) | L | L | H | L | Code | 8 |
| AUTO REFRESH (refresh all or single bank) or SELF REFRESH (enter self refresh mode) | L | L | L | H | X | 9, 10 |
| LOAD MODE REGISTER (standard or extended mode registers) | L | L | L | L | Op-code | 11 |

Notes:
1. CKE is HIGH for all commands shown except SELF REFRESH and deep power-down.
2. All states and sequences not shown are reserved and/or illegal.
3. DESELECT and NOP are functionally interchangeable.
4. BA0–BA1 provide bank address and A0–A12/A13 provide row address.
5. BA0–BA1 provide bank address; A0–A8 provide column address; A10 HIGH enables the auto precharge feature (nonpersistent); A10 LOW disables the auto precharge feature.
6. Applies only to read bursts with auto precharge disabled; this command is undefined (and should not be used) for READ bursts with auto precharge enabled and for WRITE bursts.
7. This command is a BURST TERMINATE if CKE is HIGH and deep power-down if CKE is LOW.
8. A10 LOW: BA0–BA1 determine which bank is precharged.
   A10 HIGH: all banks are precharged and BA0–BA1 are "Don't Care."
9. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
10. Internal refresh counter controls row addressing; all self refresh inputs and I/Os are "Don't Care" except for CKE.
11. BA0–BA1 either select the standard mode register or the extended mode register (BA0 = 0, BA1 = 0 select the standard mode register; BA0 = 0, BA1 = 1 select extended mode register; other combinations of BA0–BA1 are reserved). A0–A12/A13 provide the op-code to be written to the selected mode register.

**Table 8: Truth Table – DM Operation**

| Name (Function) | DM | DQ | Notes |
|---|---|---|---|
| Write enable | L | Valid | 1, 2 |
| Write inhibit | H | X | 1, 2 |

Notes:
1. Used to mask write data; provided coincident with the corresponding data.
2. All states and sequences not shown are reserved and illegal.


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## DESELECT

The DESELECT function (CS# HIGH) prevents new commands from being executed by the Mobile DDR SDRAM. Operations already in progress are not affected.

## NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct the selected Mobile DDR SDRAM to perform a NOP (CS# is LOW with RAS#, CAS#, and WE# HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

## LOAD MODE REGISTER

The mode registers are loaded via inputs BA0–BA1 and A0–A12. See mode register descriptions in "Register Definition" on page 15. The LOAD MODE REGISTER command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until $^{t}$MRD is met.

## ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0 and BA1 inputs selects the bank, and the address provided on inputs A0–A12 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

## READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A*i* (where *i* = the most significant column address bit for each configuration) selects the starting column location. The value on input A10 determines whether auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

## WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0–BA1 inputs selects the bank, and the address provided on inputs A0–A*i* (where *i* = the most significant column address bit for each configuration) selects the starting column location. The value on input A10 determines whether auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQ is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.


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## PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time ($^{t}$RP) after the PRECHARGE command is issued. The exception is the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as "Don't Care." After a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging.

## BURST TERMINATE

The BURST TERMINATE command is used to truncate READ bursts (with auto precharge disabled). The most recently registered READ command prior to the BURST TERMINATE command will be truncated, as described in "Operations" on page 26. The open page from which the READ burst was terminated remains open.

## AUTO REFRESH

The AUTO REFRESH command is nonpersistent and must be issued each time a refresh is required.

The addressing is generated by the internal refresh controller. This makes the address bits a "Don't Care" during an AUTO REFRESH command. The 256Mb Mobile DDR SDRAM requires AUTO REFRESH cycles at an average interval of 7.8125µs (MAX).

To enable improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided.

Although not a JEDEC requirement, CKE must be active (HIGH) during the auto refresh period to provide for future functionality features. The auto refresh period begins when the AUTO REFRESH command is registered, and it ends $^{t}$RFC later.

## SELF REFRESH

The SELF REFRESH command can be used to retain data in the Mobile DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the Mobile DDR SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command, except that CKE is disabled (LOW). All command and address input signals except CKE are "Don't Care" during SELF REFRESH. For details on entering and exiting self refresh mode, see Figure 44 on page 72. During SELF REFRESH, the device is refreshed as identified in the extended mode register (see PASR setting).

## Auto Precharge

Auto precharge is a feature that performs the same individual-bank PRECHARGE function described above, without requiring an explicit command. This is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst.


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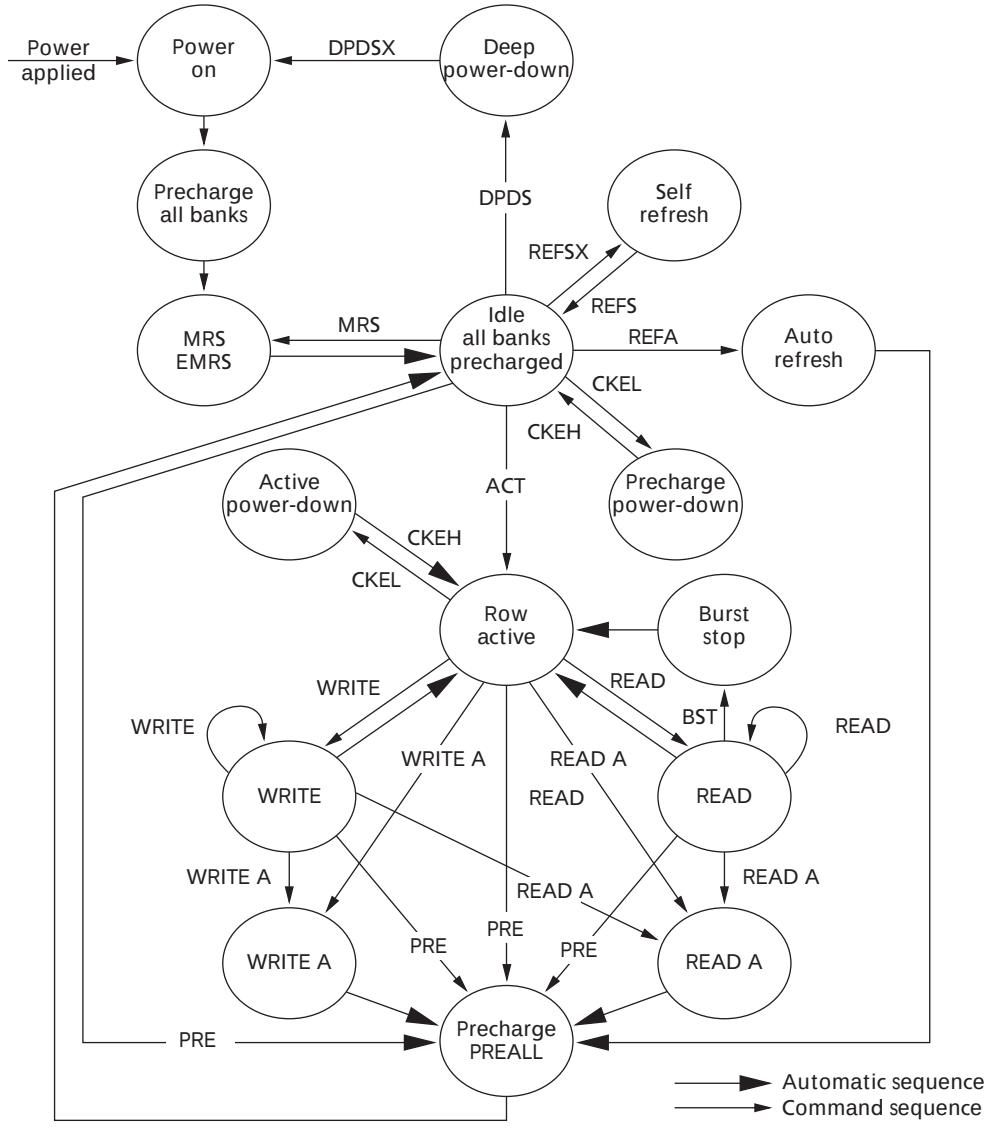
Auto precharge is nonpersistent in that it is either enabled or disabled for each individual READ or WRITE command. This device supports concurrent auto precharge if the command to the other bank does not interrupt the data transfer to the current bank.

Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. This earliest valid stage is determined as if an explicit PRECHARGE command were issued at the earliest possible time, without violating $^{t}$RAS (MIN), as described for each burst type in "Operations" on page 26. The user must not issue another command to the same bank until the precharge time ($^{t}$RP) is completed.

## Deep Power-Down

Deep power-down is an operating mode used to achieve maximum power reduction by eliminating the power draw of the memory array. Data will not be retained when the device enters deep power-down mode.

**Figure 10: Mobile DRAM State Diagram**





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# Operations

## Bank/Row Activation

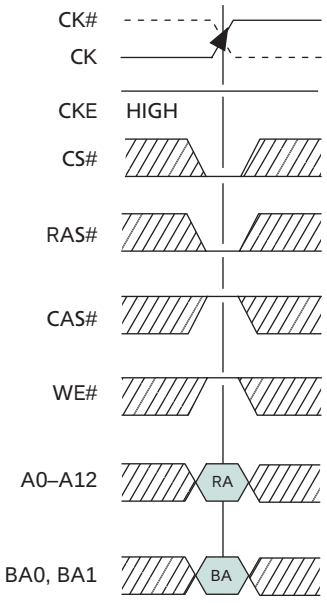
Before any READ or WRITE commands can be issued to a bank within the Mobile DDR SDRAM, a row in that bank must be "opened." This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated, as shown in Figure 11.

After a row is opened with an ACTIVE command, a READ or WRITE command may be issued to that row, subject to the $^{t}$RCD specification. $^{t}$RCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a $^{t}$RCD specification of 20ns with a 133 MHz clock (7.5ns period) results in 2.7 clocks rounded to 3. This is reflected in Figure 12 on page 27, which covers any case where $2 < {}^{t}\text{RCD (MIN)} / {}^{t}\text{CK} \leq 3$. (Figure 12 also shows the same case for $^{t}$RRD; the same procedure is used to convert other specification limits from time units to clock cycles.)

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been "closed" (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by $^{t}$RC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by $^{t}$RRD.

**Figure 11: Activating a Specific Row in a Specific Bank**




Notes: 1. RA = row address
2. BA = bank address


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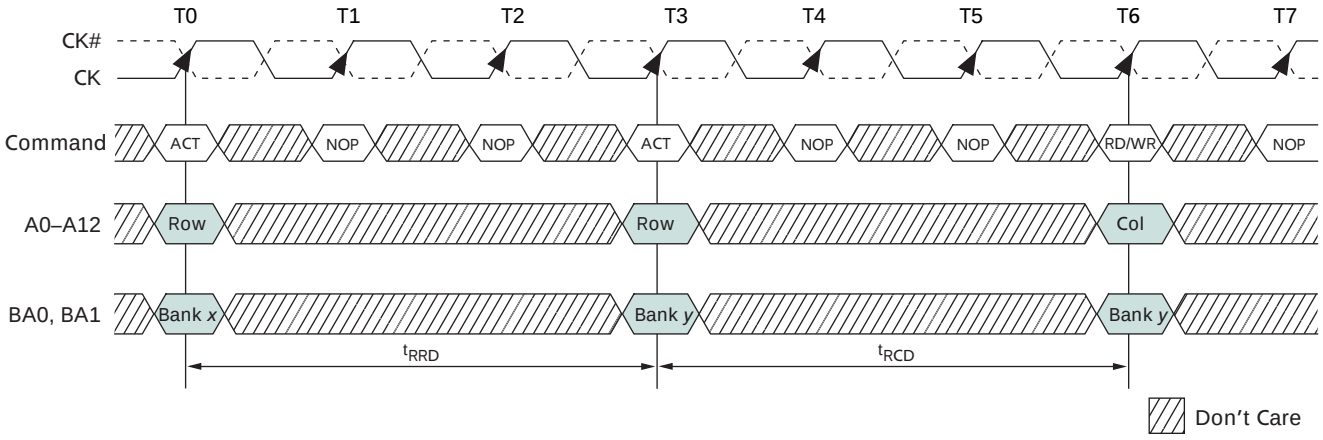
**Figure 12: Example: Meeting $^{t}$RCD ($^{t}$RRD) MIN When 2 < $^{t}$RCD ($^{t}$RRD) MIN**




## READs

READ burst operations are initiated with a READ command, as shown in Figure 13 on page 28.

The starting column and bank addresses are provided with the READ command, and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the READ commands used in the following illustrations, auto precharge is disabled.

During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data-out element will be valid nominally at the next positive or negative clock edge (for example, at the next crossing of CK and CK#). Figure 14 on page 29 shows general timing for different CAS latency settings. DQS is driven by the Mobile DDR SDRAM along with output data. The initial LOW state on DQS is known as the read preamble; the LOW state coincident with the last data-out element is known as the read postamble.

Upon completion of a burst, assuming no other commands have been initiated, the DQ will go High-Z. A detailed explanation of $^{t}$DQSQ (valid data-out skew), $^{t}$QH (data-out window hold), and the valid data window is depicted in Figure 37 on page 66. A detailed explanation of $^{t}$DQSCK (DQS transition skew to CK) and $^{t}$AC (data-out transition skew to CK) is depicted in Figure 39 on page 68.

Data from any READ burst may be concatenated with or truncated with data from a subsequent READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst either follows the last element of a completed burst or the last desired data element of a longer burst that is being truncated. The new READ command should be issued *x* cycles after the first READ command, where *x* equals the number of desired data element pairs (pairs are required by the 2*n*-prefetch architecture). This is shown in Figure 15 on page 30. A READ command can be initiated on any clock cycle following a previous READ command. Nonconsecutive read data is illustrated in Figure 16 on page 31. Full-speed random read accesses within a page (or pages) can be performed, as shown in Figure 17 on page 32.


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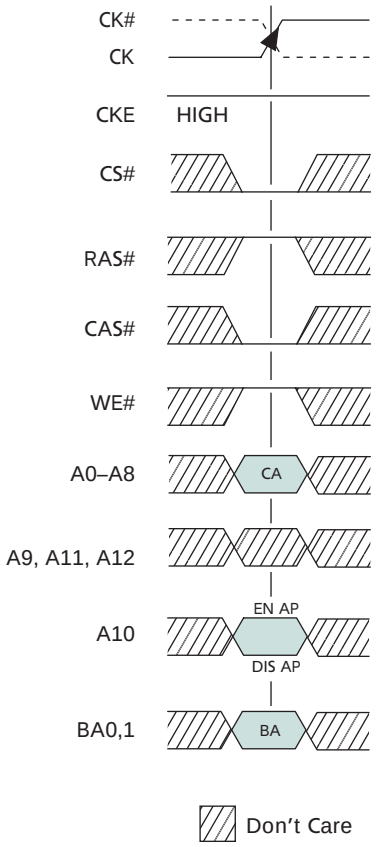
**Figure 13: READ Command**




Notes:
1. CA = column address
2. BA = bank address
3. EN AP = enable auto precharge
4. DIS AP = disable auto precharge
5. x16 DQ configuration example


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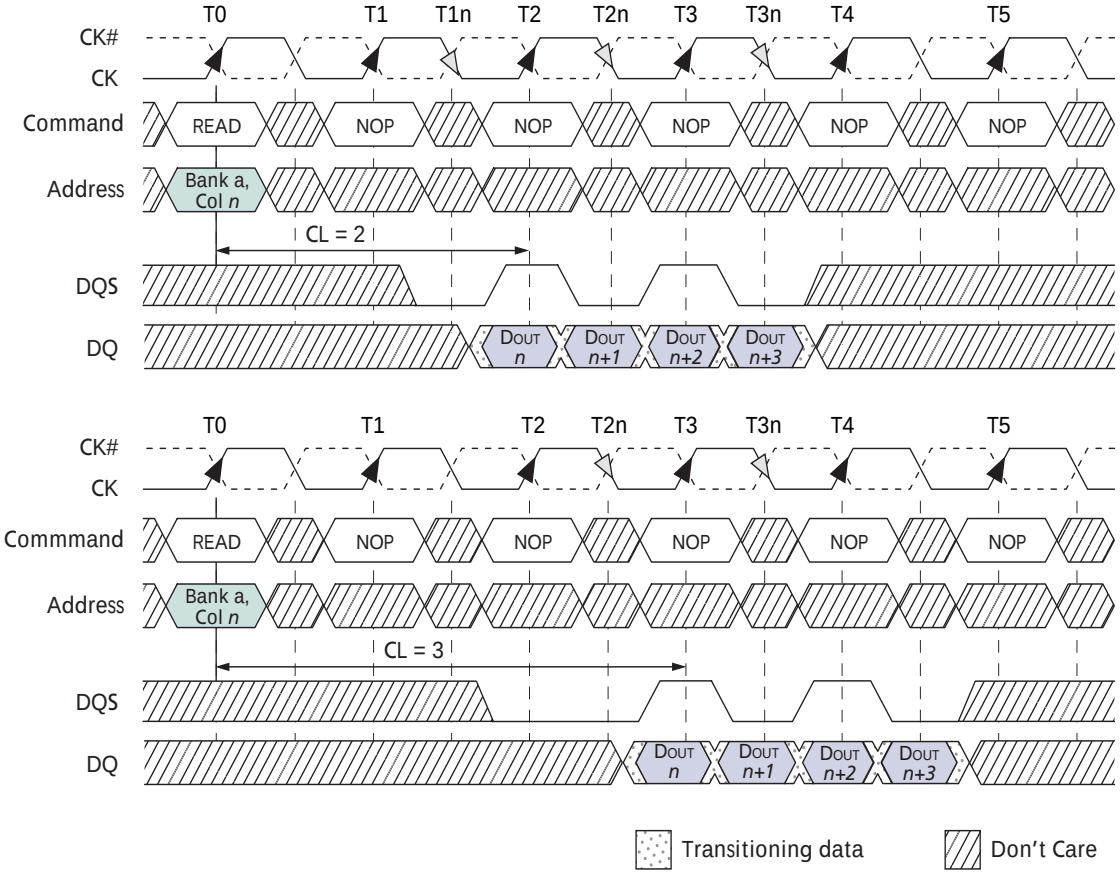
**Figure 14: READ Burst**




Notes:
1. DOUT *n* = data-out from column *n*.
2. BL = 4.
3. Shown with nominal $^{t}$AC, $^{t}$DQSCK, and $^{t}$DQSQ.


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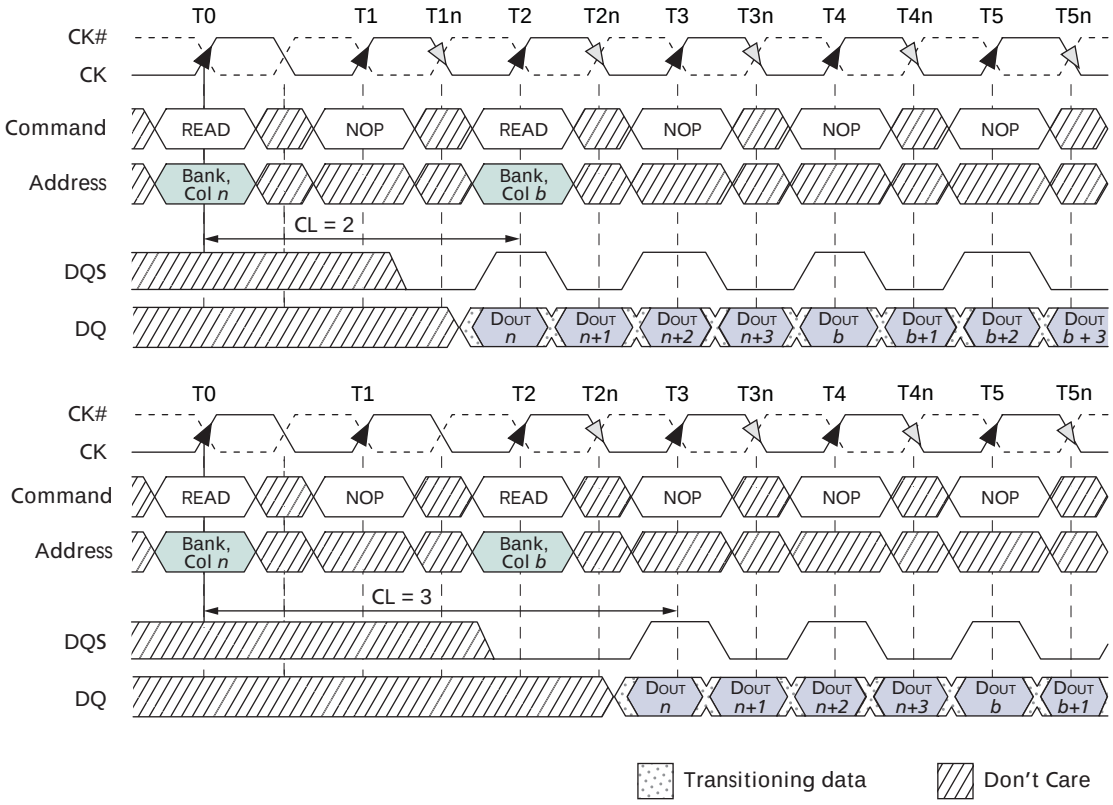
**Figure 15: Consecutive READ Bursts**




Notes:
1. DOUT *n* (or *b*) = data-out from column *n* (or column *b*).
2. BL = 4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first).
3. Shown with nominal $^{t}$AC, $^{t}$DQSCK, and $^{t}$DQSQ.
4. Example applies only when READ commands are issued to the same device.


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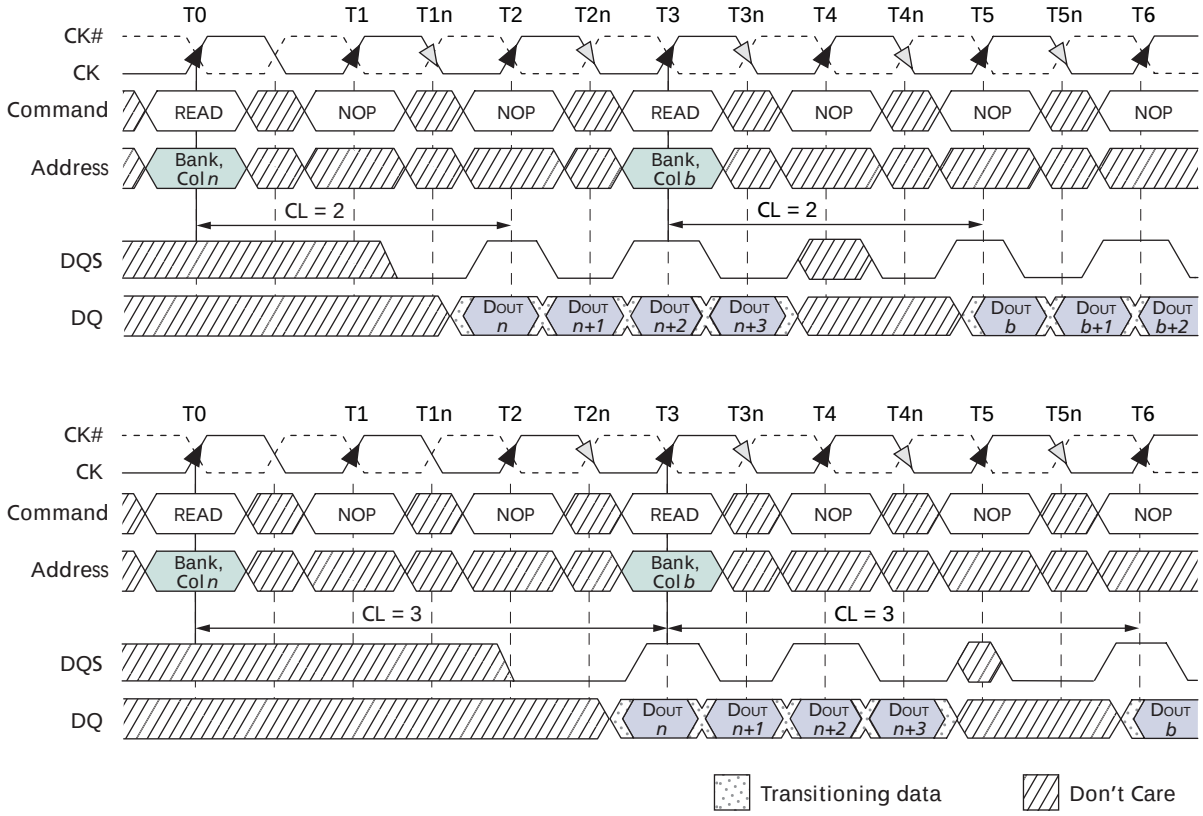
**Figure 16: Nonconsecutive READ Bursts**




Notes:
1. DOUT *n* (or *b*) = data-out from column *n* (or column *b*).
2. BL = 4 or 8 (if burst is 8, the second burst interrupts the first).
3. Shown with nominal $^{t}$AC, $^{t}$DQSCK, and $^{t}$DQSQ.
4. Example applies when READ commands are issued to different devices or nonconsecutive READs.


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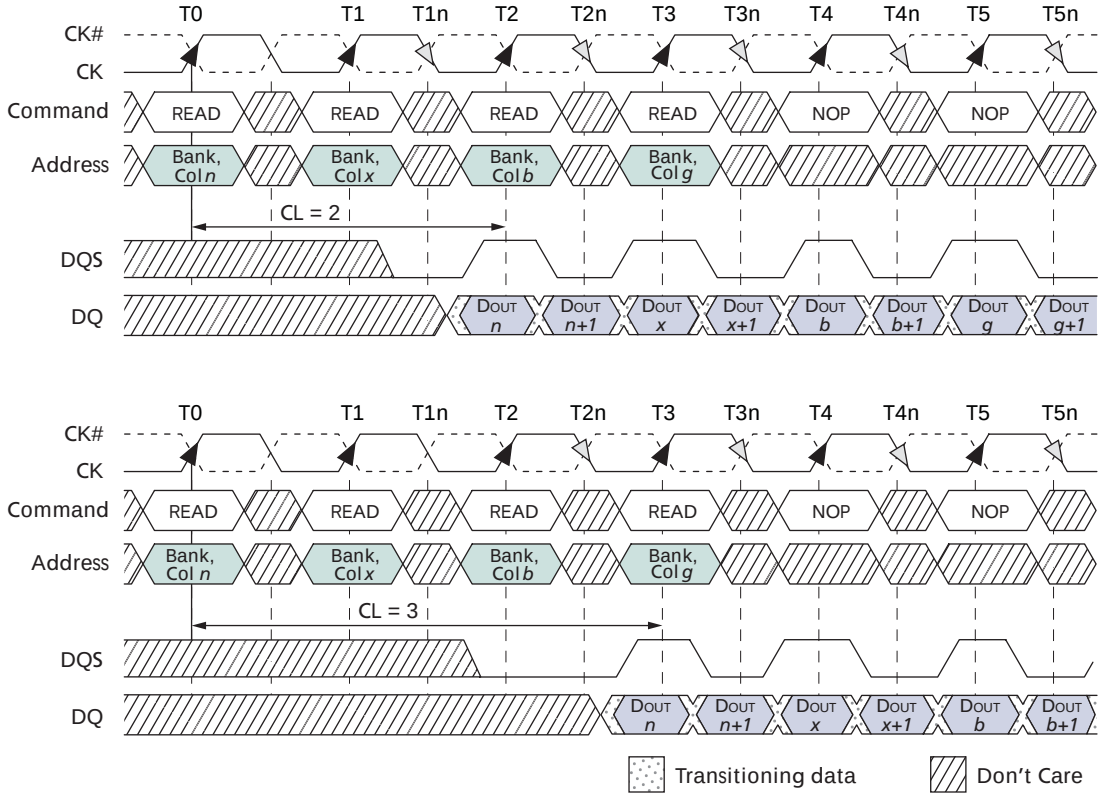
**Figure 17: Random READ Accesses**




Notes:
1. DOUT *n* (or *x*, *b*, *g*) = data-out from column *n* (column *x*, column *b,* column *g*).
2. BL = 2, 4, or 8 (if 4 or 8, the following burst interrupts the previous).
3. READs are to an active row in any bank.
4. Shown with nominal $^{t}$AC, $^{t}$DQSCK, and $^{t}$DQSQ.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## Truncated READs

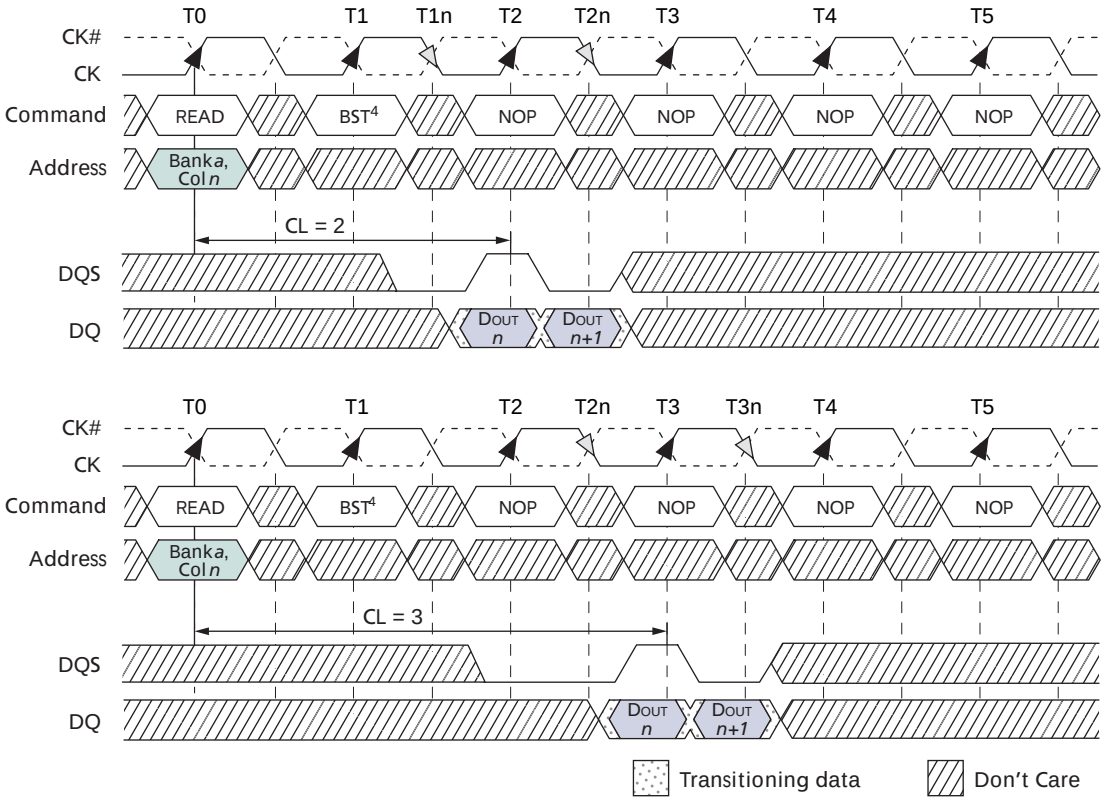
Data from any non-auto precharge READ burst may be truncated with a BURST TERMINATE command, as shown in Figure 18. The BURST TERMINATE latency is equal to the READ (CAS) latency; for example, the BURST TERMINATE command should be issued *x* cycles after the READ command, where *x* equals the number of desired data element pairs (pairs are required by the 2*n*-prefetch architecture).

Data from any non-auto precharge READ burst must be completed or truncated before a subsequent WRITE command can be issued. If truncation is necessary, the BURST TERMINATE command must be used, as shown in Figure 18. The $^{t}$DQSS (MIN) case is shown; the $^{t}$DQSS (MAX) case has a longer bus idle time. ($^{t}$DQSS [MIN] and $^{t}$DQSS [MAX] are defined in the section on WRITEs.)

A READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank provided that auto precharge was not activated. The PRECHARGE command should be issued *x* cycles after the READ command, where *x* equals the number of desired data element pairs (pairs are required by the *n*-prefetch architecture). This is shown in Figure 20 on page 35. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until $^{t}$RP is met.

**Note:** Part of the row precharge time is hidden during the access of the last data elements.

**Figure 18: Terminating a READ Burst**




Notes:
1. DOUT *n* = data-out from column *n*.
2. BL = 4 or 8.
3. Shown with nominal $^{t}$AC, $^{t}$DQSCK, and $^{t}$DQSQ.
4. BST = BURST TERMINATE command; page remains open.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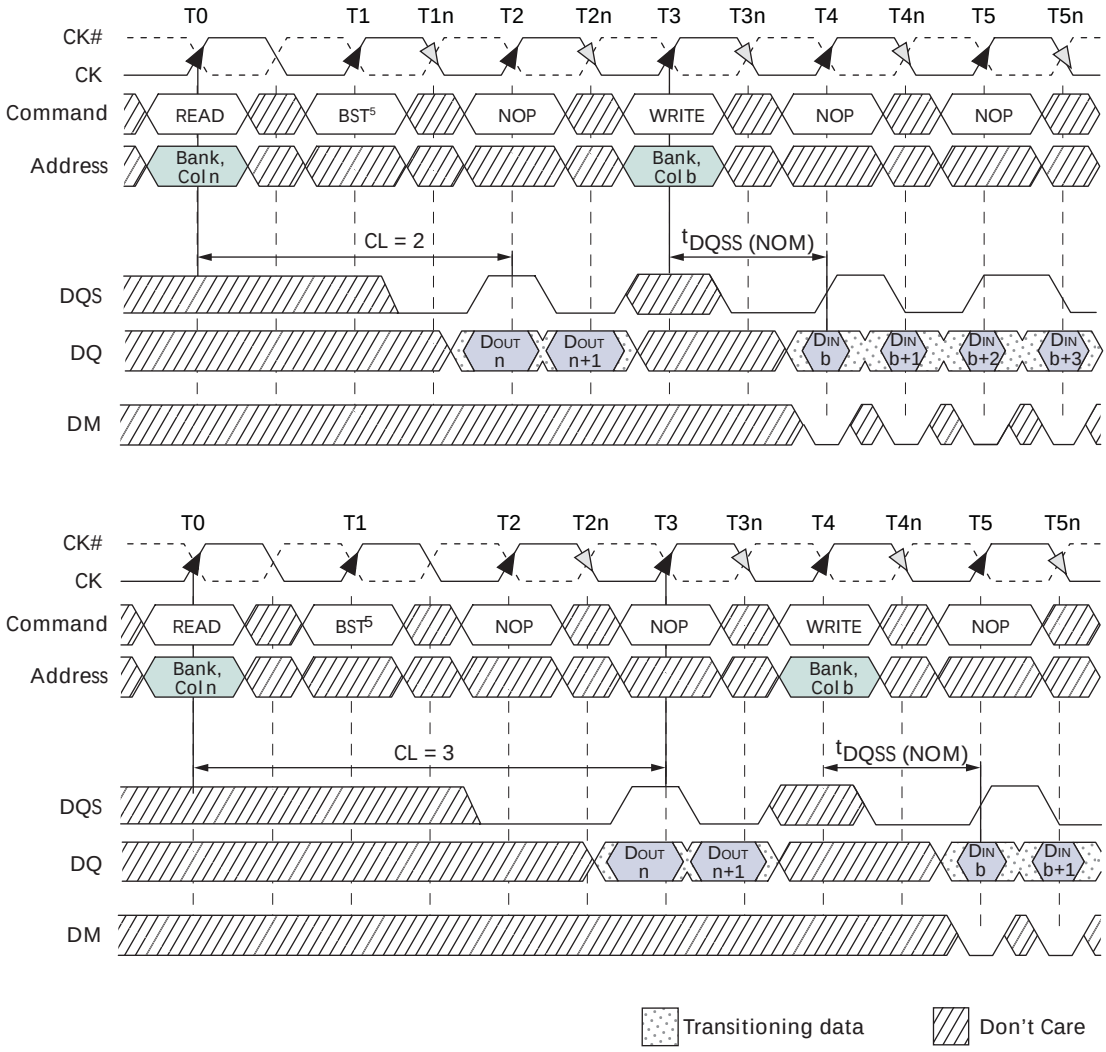
5. CKE = HIGH.

**Figure 19: READ-to-WRITE**




Notes:
1. DOUT *n* = data-out from column *n*.
2. DIN *b* = data-in from column *b*.
3. BL = 4 in the cases shown (applies for bursts of 8 as well; if BL = 2, the BST command shown can be a NOP).
4. Shown with nominal $^{t}$AC, $^{t}$DQSCK, and $^{t}$DQSQ.
5. BST = BURST TERMINATE command; page remains open.
6. CKE = HIGH.


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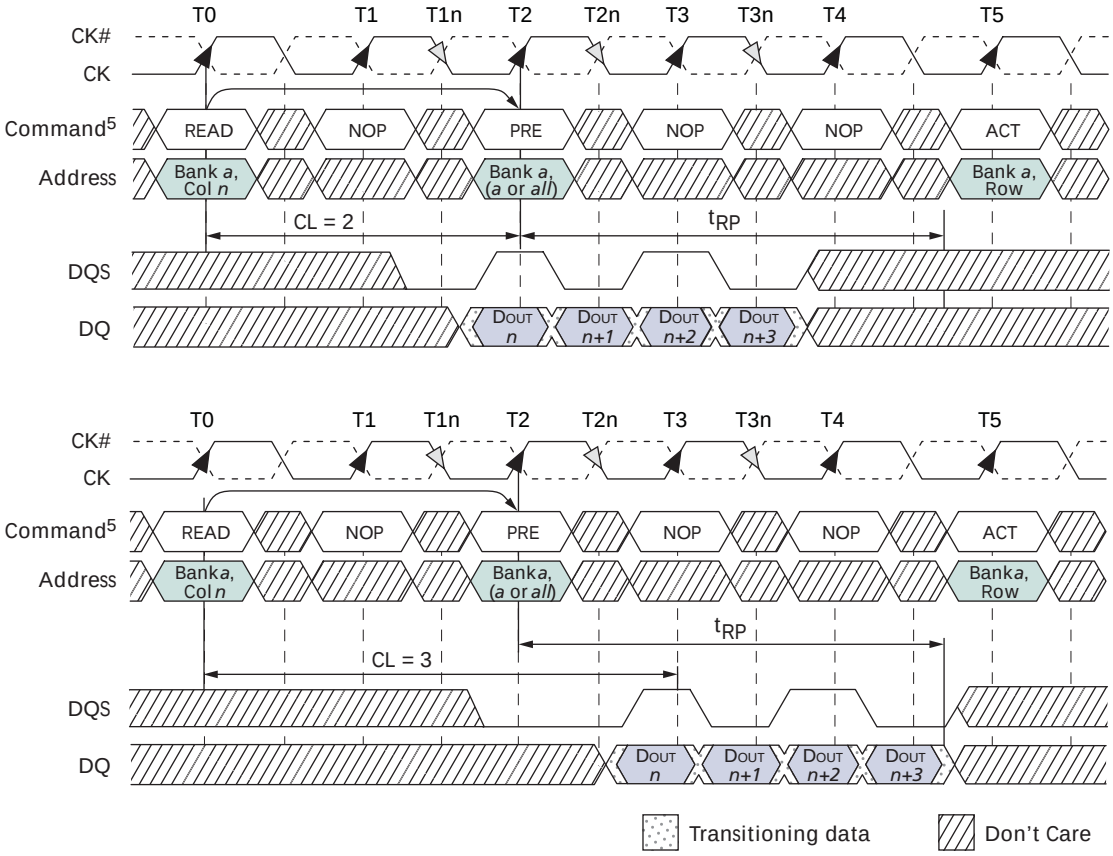
**Figure 20: READ-to-PRECHARGE**




Notes:
1. DOUT *n* = data-out from column *n*.
2. BL = 4 or an interrupted burst of 8.
3. Shown with nominal $^{t}$AC, $^{t}$DQSCK, and $^{t}$DQSQ.
4. READ-to-PRECHARGE equals 2 clock cycles, which allows 2 data pairs of data-out.
5. A READ command with auto precharge enabled, provided $^{t}$RAS (MIN) is met, would cause a precharge to be performed at *x* number of clock cycles after the READ command, where *x* = BL/2.
6. PRE = PRECHARGE command; ACT = ACTIVE command.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## WRITEs

WRITE bursts are initiated with a WRITE command, as shown in Figure 21 on page 37.

The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the WRITE commands used in the following illustrations, auto precharge is disabled.

During WRITE bursts, the first valid data-in element will be registered on the first rising edge of DQS following the WRITE command, and subsequent data elements will be registered on successive edges of DQS. The LOW state on DQS between the WRITE command and the first rising edge is known as the write preamble; the LOW state on DQS following the last data-in element is known as the write postamble.

The time between the WRITE command and the first corresponding rising edge of DQS ($^{t}$DQSS) is specified with a relatively wide range (from 75 percent to 125 percent of one clock cycle). All the WRITE diagrams show the nominal case, and where the two extreme cases (for example, $^{t}$DQSS [MIN] and $^{t}$DQSS [MAX]) might not be intuitive, they have also been included. Figure 22 on page 38 shows the nominal case and the extremes of $^{t}$DQSS for a burst of 4. Upon completion of a burst, assuming no other commands have been initiated, the DQ will remain High-Z, and any additional input data will be ignored.

Data for any WRITE burst may be concatenated with or truncated with a subsequent WRITE command. In either case, a continuous flow of input data can be maintained. The new WRITE command can be issued on any positive edge of clock following the previous WRITE command. The first data element from the new burst is applied either after the last element of a completed burst or the last desired data element of a longer burst that is being truncated. The new WRITE command should be issued *x* cycles after the first WRITE command, where *x* equals the number of desired data element pairs (pairs are required by the 2*n*-prefetch architecture).

Figure 23 on page 39 shows concatenated bursts of 4. An example of nonconsecutive WRITEs is shown in Figure 24 on page 39. Full-speed random write accesses within a page or pages can be performed, as shown in Figure 25 on page 40.

Data for any WRITE burst may be followed by a subsequent READ command. To follow a WRITE without truncating the WRITE burst, $^{t}$WTR should be met, as shown in Figure 26 on page 41.

Data for any WRITE burst may be truncated by a subsequent READ command, as shown in Figure 27 on page 42. Note that only the data-in pairs that are registered prior to the $^{t}$WTR period are written to the internal array, and any subsequent data-in should be masked with DM, as shown in Figure 28 on page 43.

Data for any WRITE burst may be followed by a subsequent PRECHARGE command. To follow a WRITE without truncating the WRITE burst, $^{t}$WR should be met, as shown in Figure 29 on page 44. At least one clock cycle is required during $^{t}$WR time when in auto-precharge mode.

Data for any WRITE burst may be truncated by a subsequent PRECHARGE command, as shown in Figure 30 on page 45 and Figure 31 on page 46. Note that only the data-in pairs that are registered prior to the $^{t}$WR period are written to the internal array, and any subsequent data-in should be masked with DM, as shown in Figures 30 and 31. After the PRECHARGE command, a subsequent command to the same bank cannot be issued until $^{t}$RP is met.


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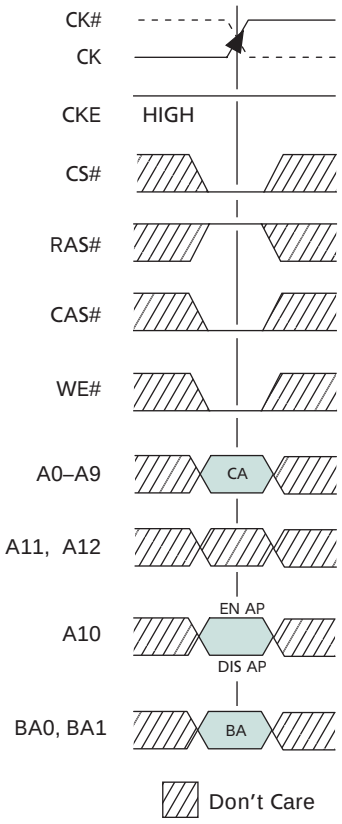
**Figure 21: WRITE Command**




Notes:
1. CA = column address.
2. BA = bank address.
3. EN AP = enable auto precharge.
4. DIS AP = disable auto precharge.


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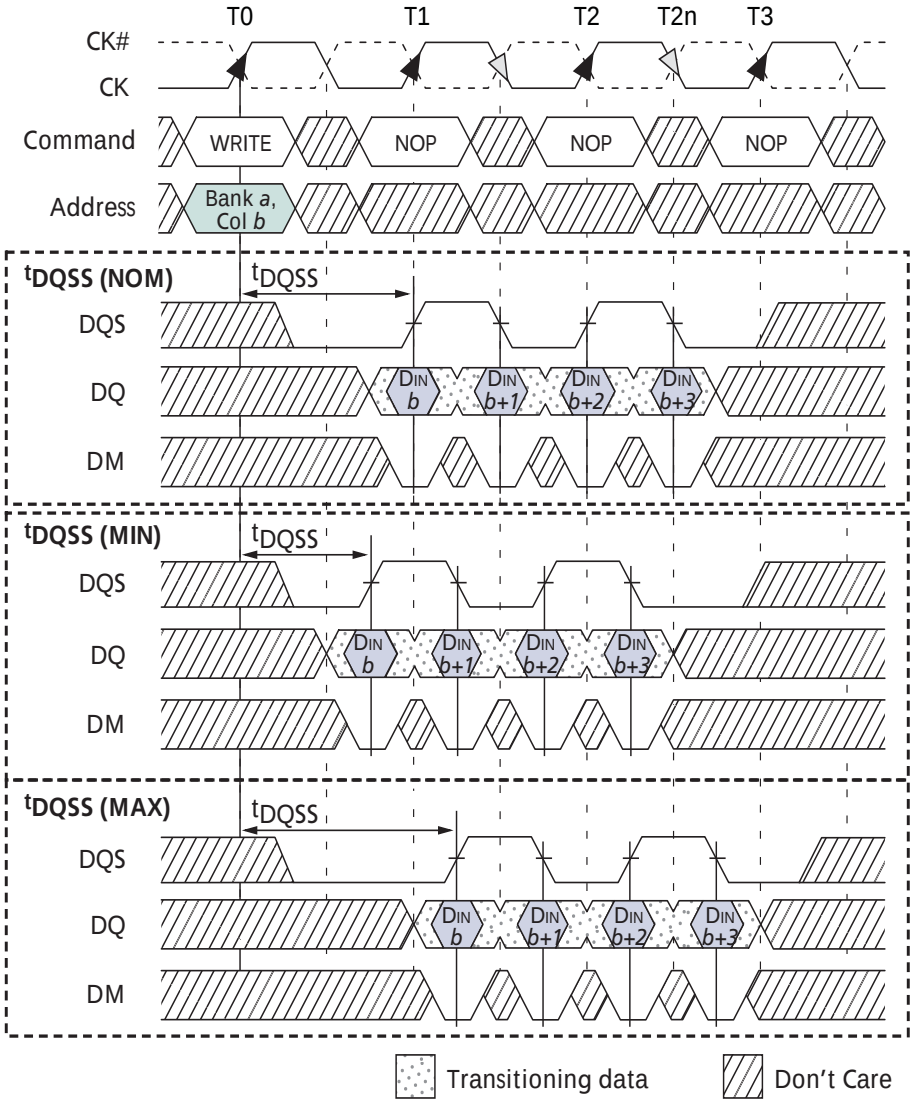
**Figure 22: WRITE Burst**




Notes:
1. DIN *b* = data-in for column *b*.
2. An uninterrupted burst of 4 is shown.
3. A10 is LOW with the WRITE command (auto precharge is disabled).


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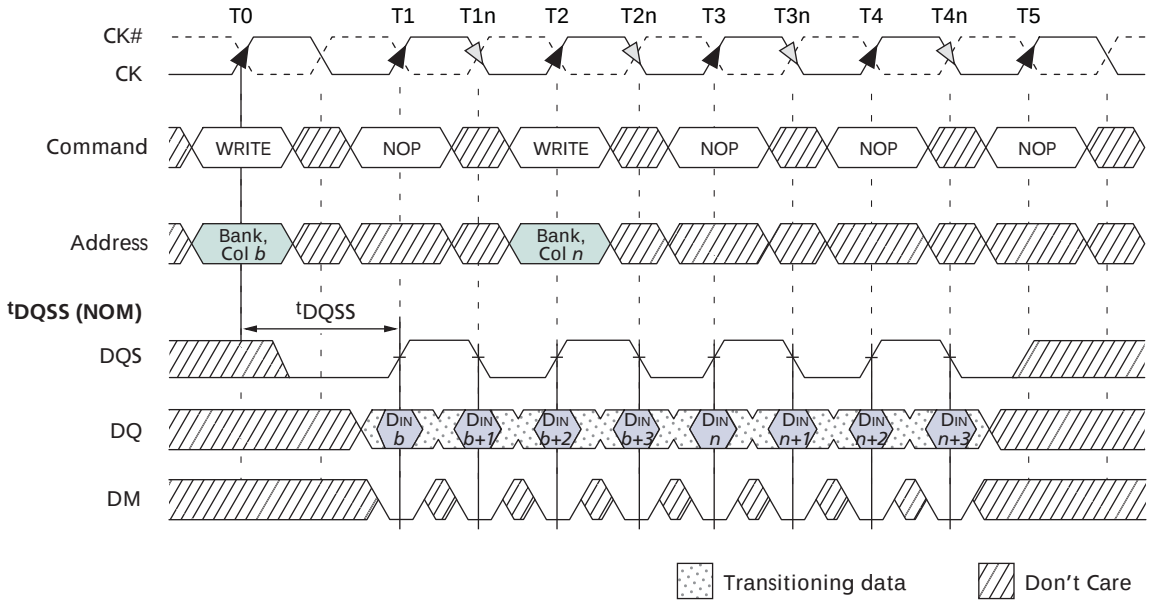
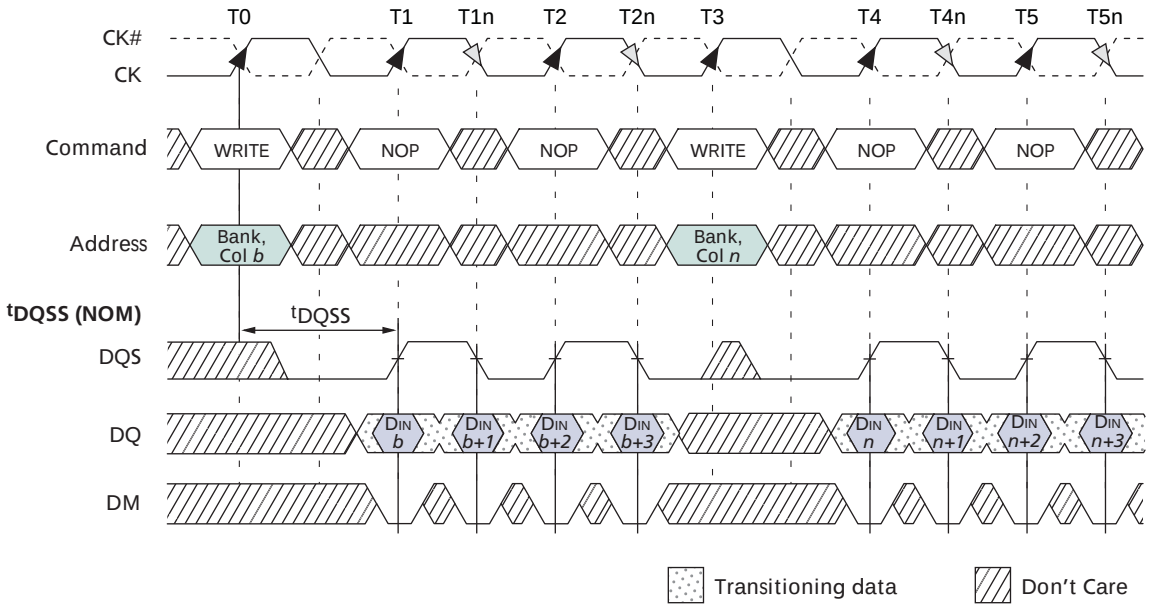
**Figure 23: Consecutive WRITE-to-WRITE**




Notes:
1. DIN *b* (*n*) = data-in for column *b* (*n*).
2. An uninterrupted burst of 4 is shown.
3. Each WRITE command may be to any bank.

**Figure 24: Nonconsecutive WRITE-to-WRITE**




Notes:
1. DIN *b (n)* = data-in for column *b (n).*
2. An uninterrupted burst of 4 is shown.
3. Each WRITE command may be to any bank.


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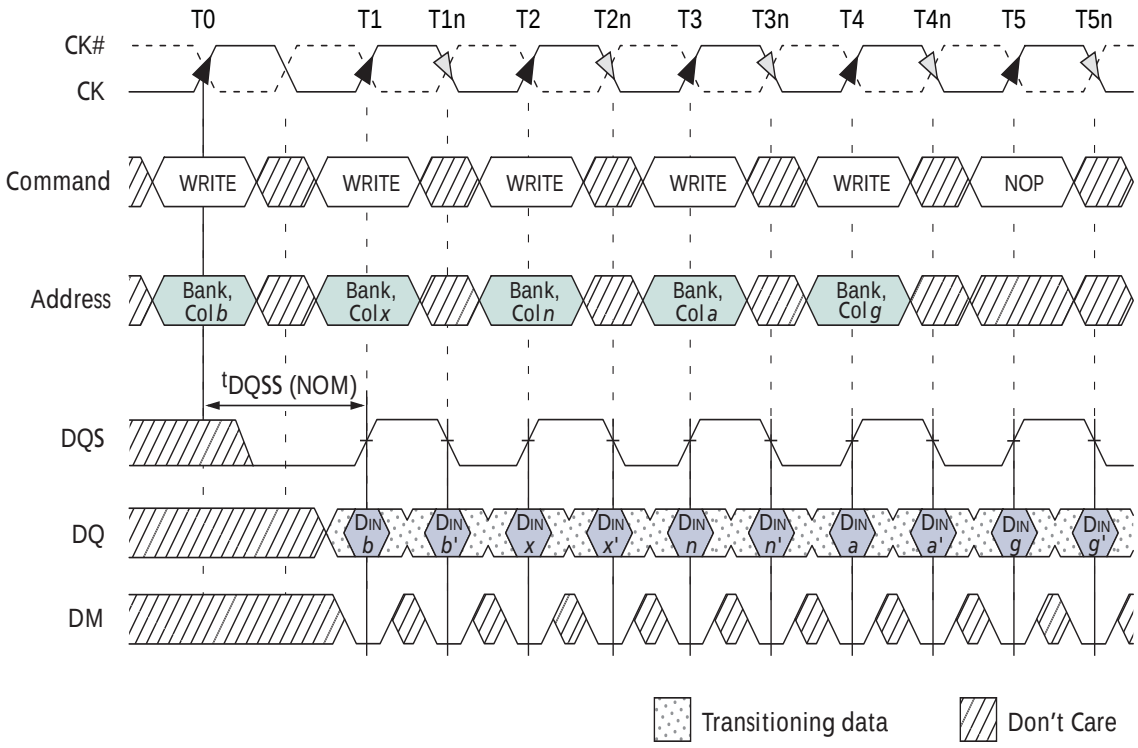
**Figure 25: Random WRITE Cycles**




Notes:
1. DIN *b* (or *x, n, a, g*) = data-in for column *b* (or *x, n, a, g*).
2. *b*' (or *x*', *n*', *a*', *g*') = the next data-in following DIN *b (x, n, a, g)*, according to the programmed burst order.
3. Programmed BL = 2, 4, or 8 in cases shown.
4. Each WRITE command may be to any bank.


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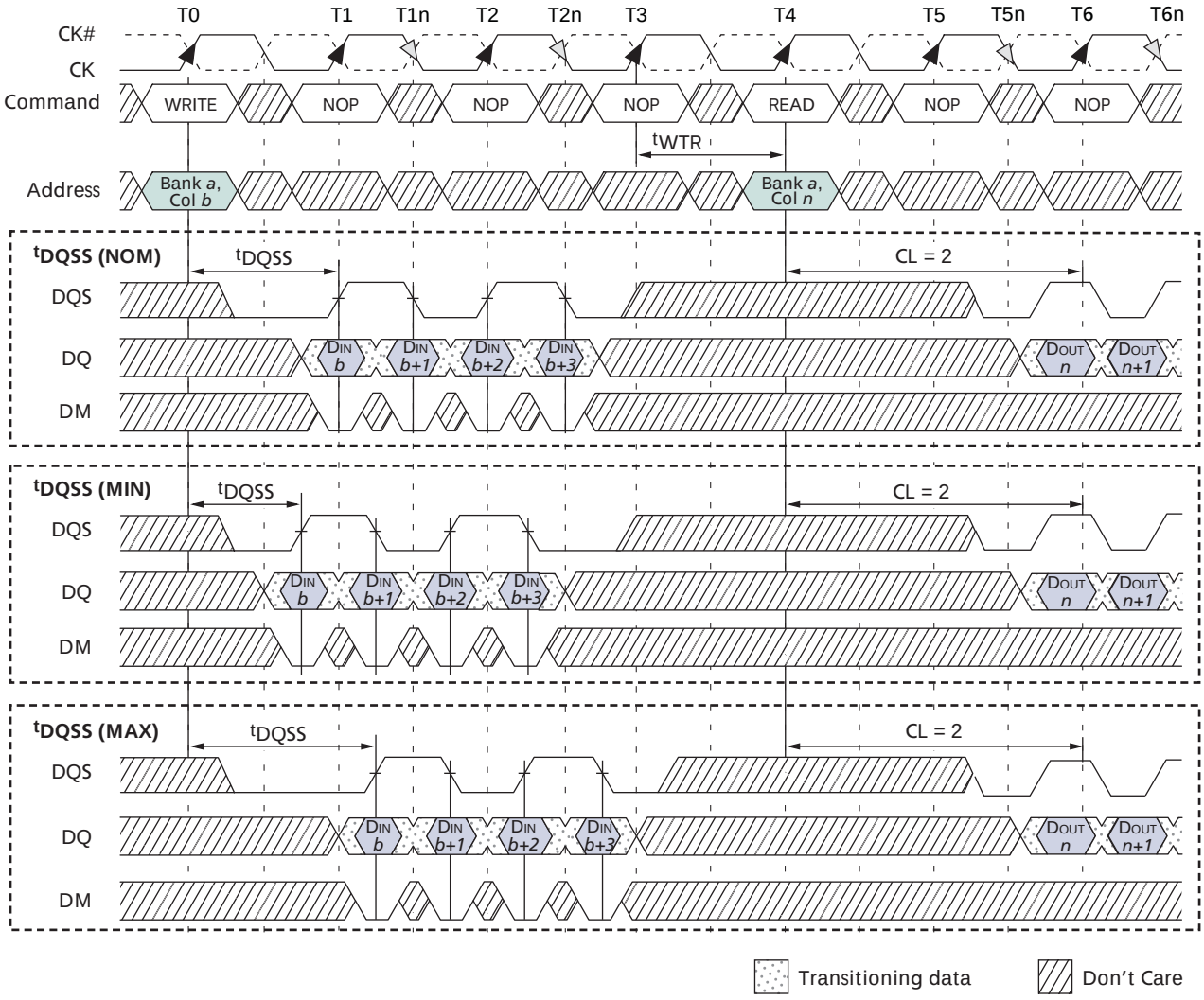
**Figure 26: WRITE-to-READ – Uninterrupting**




Notes:
1. DIN *b* = data-in for column *b*; DOUT *n* = data-out for column *n*.
2. An uninterrupted burst of 4 is shown.
3. tWTR is referenced from the first positive CK edge after the last data-in pair.
4. The READ and WRITE commands are to the same bank. However, the READ and WRITE commands can be directed to different banks in which case tWTR is not required, and the READ command could be applied earlier.
5. A10 is LOW with the WRITE command (auto precharge is disabled).


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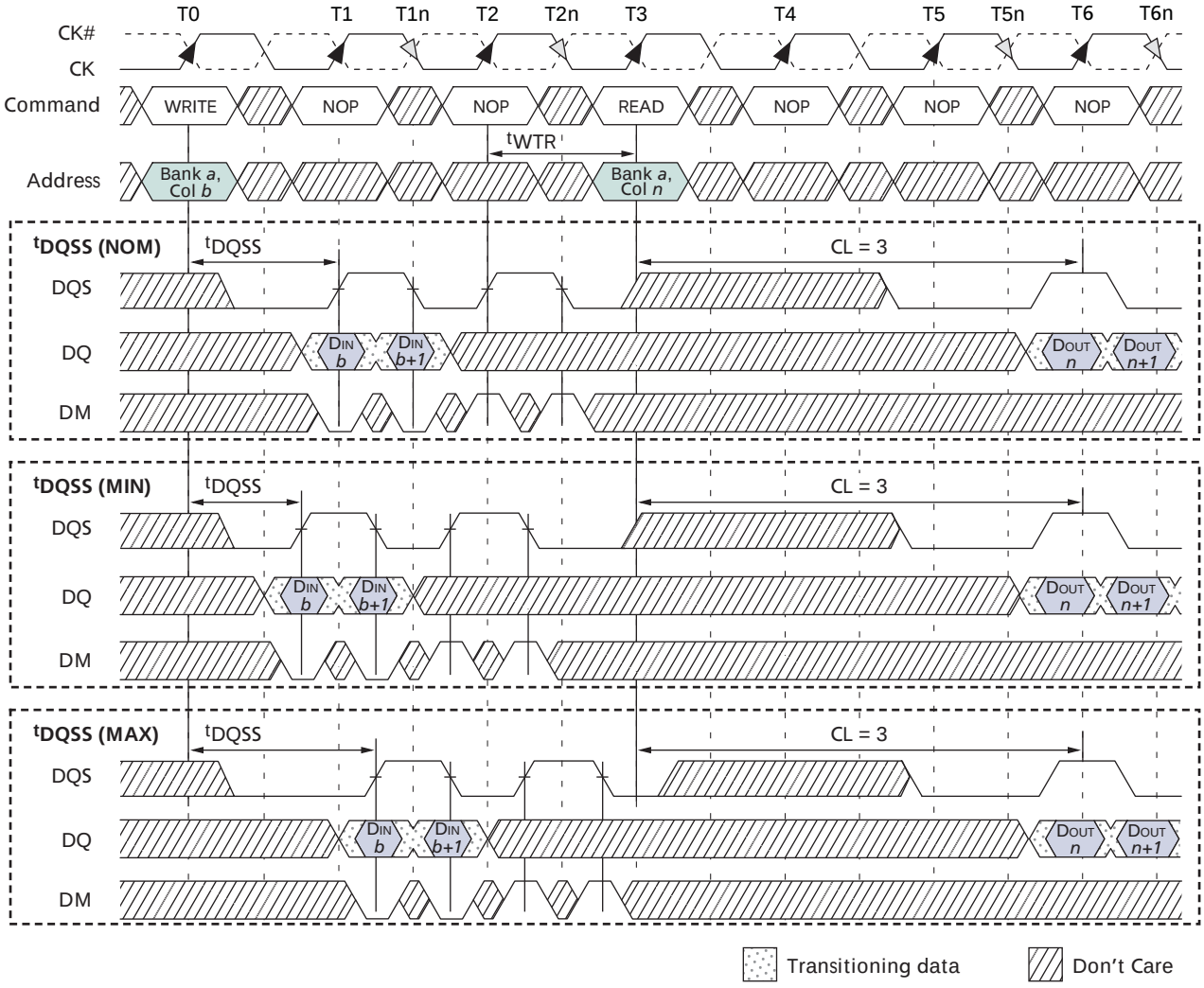
**Figure 27: WRITE-to-READ – Interrupting**




Notes:
1. DIN *b* = data-in for column *b;* DOUT *n* = data-out for column *n*.
2. An interrupted burst of 4 is shown; two data elements are written.
3. tWTR is referenced from the first positive CK edge after the last data-in pair.
4. A10 is LOW with the WRITE command (auto precharge is disabled).
5. DQS is required at T2 and T2n (nominal case) to register DM.
6. If the burst of 8 was used, DM and DQS would be required at T3 and T3n because the READ command would not mask these two data elements.


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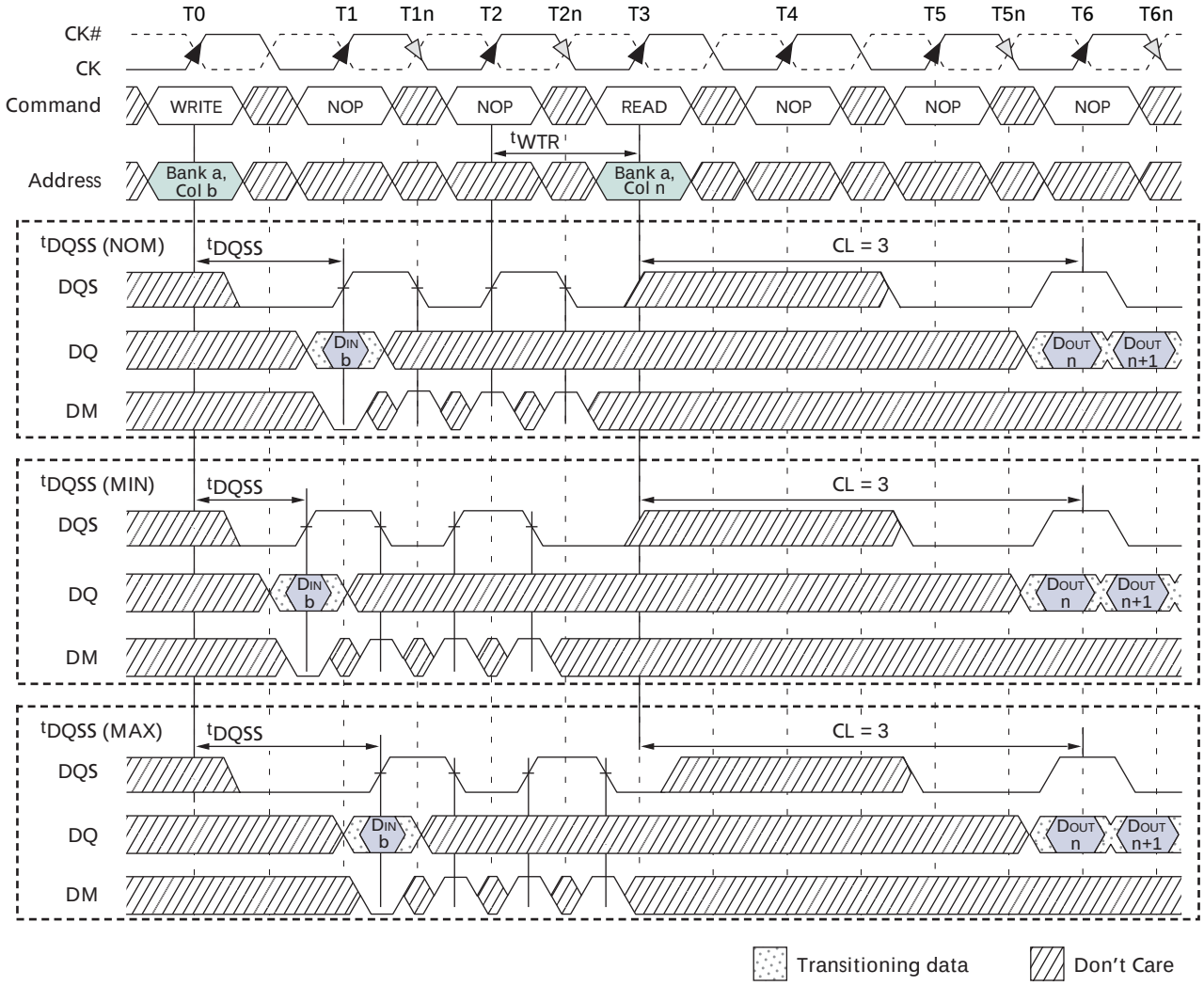
**Figure 28: WRITE-to-READ – Odd Number of Data, Interrupting**




Notes:
1. DIN *b* = data-in for column *b;* DOUT *n* = data-out for column *n*.
2. An interrupted burst of 4 is shown; one data element is written, and three are masked.
3. tWTR is referenced from the first positive CK edge after the last data-in.
4. A10 is LOW with the WRITE command (auto precharge is disabled).
5. DQS is required at T2 and T2n (nominal case) to register DM.
6. If the burst of 8 was used, DM and DQS would be required at T3 and T3n because the READ command would not mask these two data elements.


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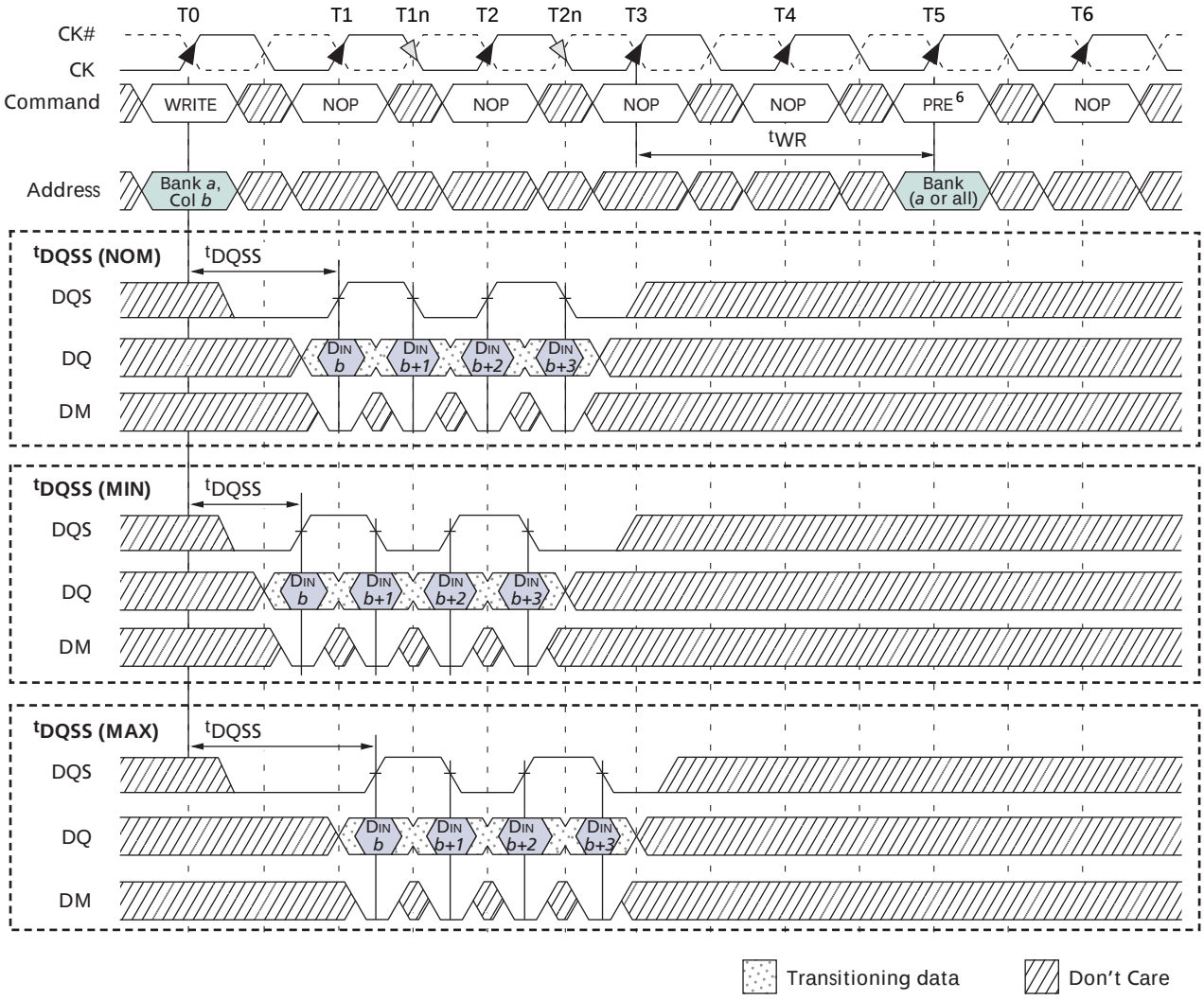
**Figure 29: WRITE-to-PRECHARGE – Uninterrupting**




Notes:
1. DIN *b* = data-in for column *b*.
2. An uninterrupted burst of 4 is shown.
3. $^{t}$WR is referenced from the first positive CK edge after the last data-in pair.
4. The PRECHARGE and WRITE commands are to the same bank. However, the PRECHARGE and WRITE commands may be to different banks in which case $^{t}$WR is not required, and the PRECHARGE command could be applied earlier.
5. A10 is LOW with the WRITE command (auto precharge is disabled).
6. PRE = PRECHARGE command.


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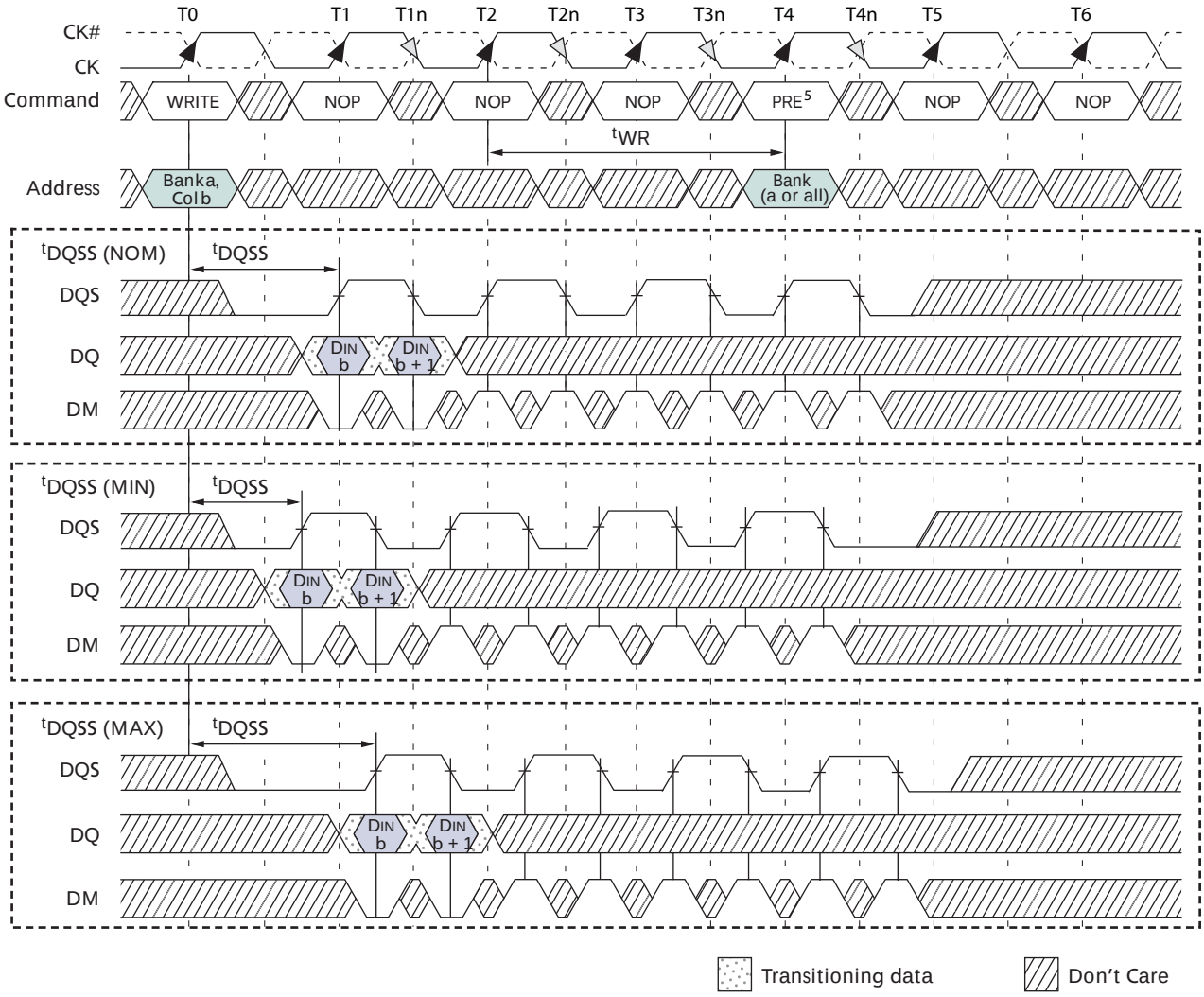
**Figure 30: WRITE-to-PRECHARGE – Interrupting**




Notes:
1. DIN *b* = data-in for column *b*.
2. An interrupted burst of 8 is shown; two data elements are written.
3. tWR is referenced from the first positive CK edge after the last data-in pair.
4. A10 is LOW with the WRITE command (auto precharge is disabled).
5. PRE = PRECHARGE command.
6. DQS is required at T4 and T4n (nominal case) to register DM.
7. If a burst of 4 is used, DQS and DM are not required at T3, T3n, T4, and T4n.


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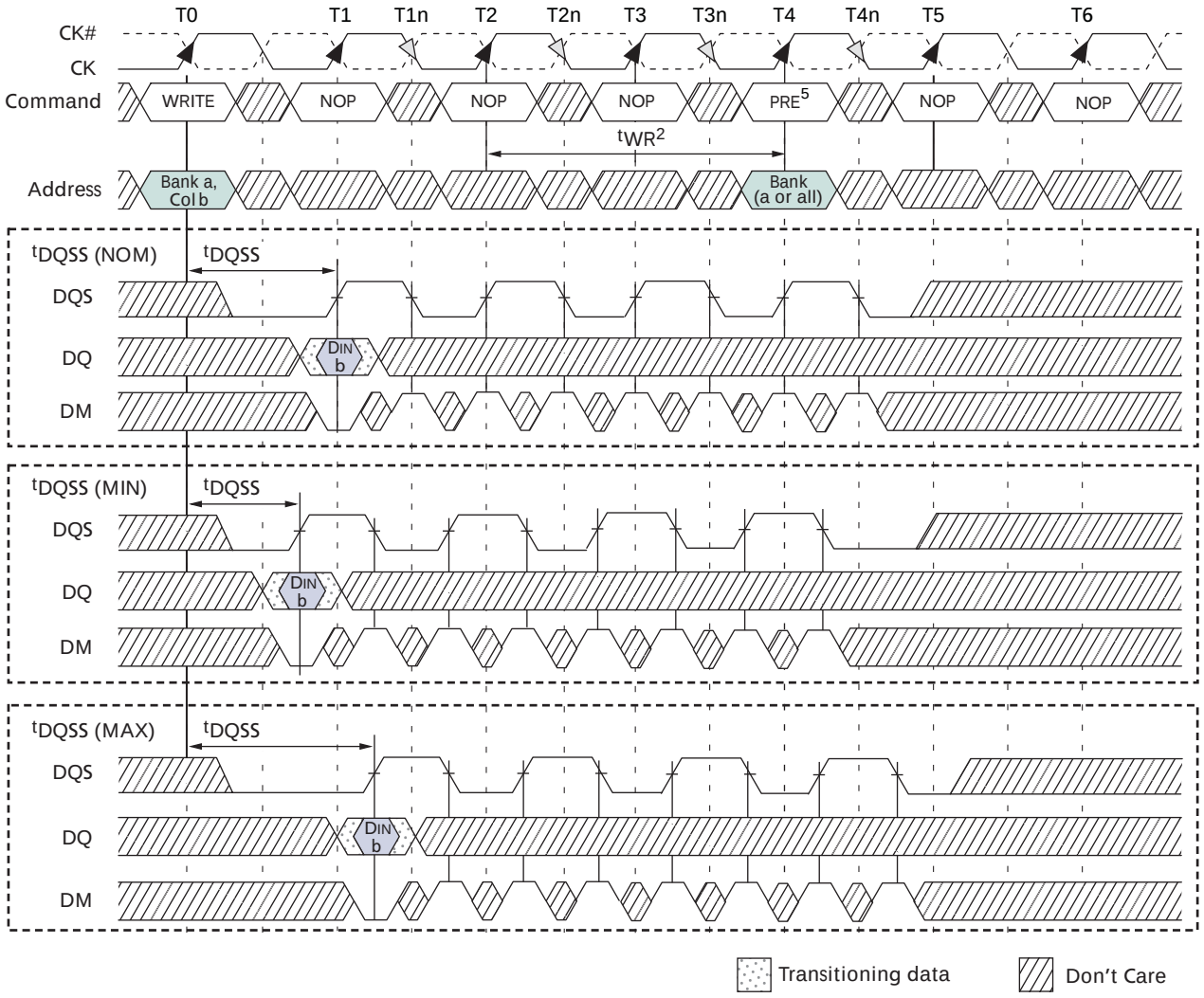
**Figure 31: WRITE-to-PRECHARGE – Odd Number of Data, Interrupting**




Notes:
1. DIN *b* = data-in for column *b*.
2. An interrupted burst of 8 is shown.
3. tWR is referenced from the first positive CK edge after the last data-in pair.
4. A10 is LOW with the WRITE command (auto precharge is disabled).
5. PRE = PRECHARGE command.
6. DQS is required at T4 and T4n to register DM.
7. If the burst of 4 is used, DQS and DM are not required at T3, T3n, T4, and T4n.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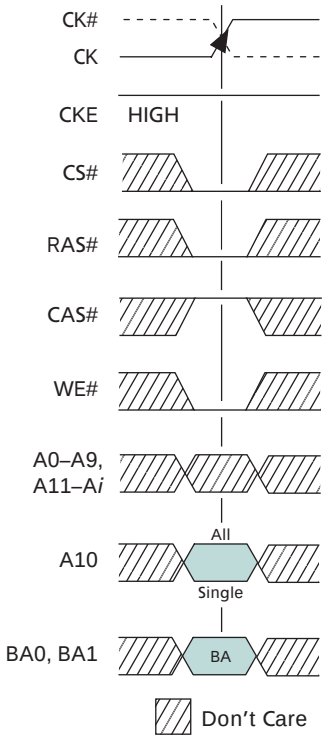
## PRECHARGE

The PRECHARGE command (Figure 32) is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time ($^{t}$RP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged. In the case where only one bank is to be precharged (A10 = LOW), inputs BA0–BA1 select the bank. When all banks are to be precharged (A10 = HIGH), inputs BA0–BA1 are treated as a "Don't Care." After a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

**Figure 32: PRECHARGE Command**




Notes:
1. BA = bank address.
2. A10 = 1 HIGH, all banks to be precharged, BA1, BA0 are "Don't Care."
3. A10 = 0 LOW, only bank selected by BA1 and BA0 will be precharged.
4. *i* = the most significant column address bit for each configuration.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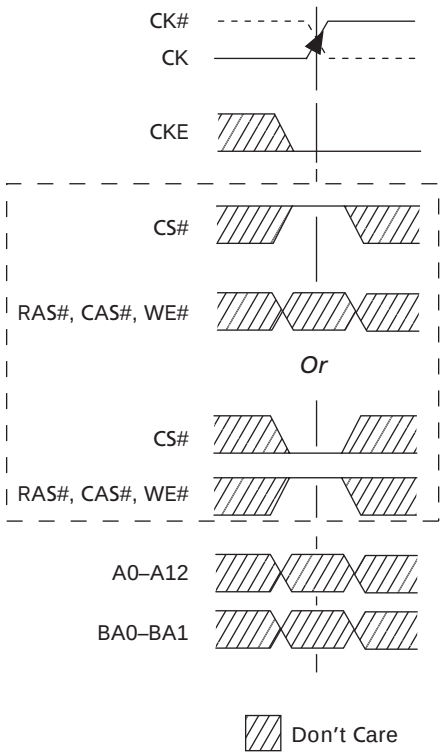
## Power-Down

Power-down (Figure 42 on page 70) is entered when CKE is registered LOW. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates all input and output buffers, including CK and CK# and excluding CKE. Exiting power-down requires the device to be at the same voltage as when it entered power-down and received a stable clock.

**Note:** The power-down duration is limited by the refresh requirements of the device.

While in power-down, CKE LOW must be maintained at the inputs of the Mobile DDR SDRAM, while all other input signals are “Don’t Care.” The power-down state is exited when CKE is registered HIGH (in conjunction with a NOP or DESELECT command). A NOP or DESELECT command must be maintained on the command bus until $^{t}$XP is satisfied.

**Figure 33: Power-Down Command (in Active or Precharge Modes)**





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## Deep Power-Down (DPD)

Deep power-down is an operating mode used to achieve maximum power reduction by eliminating the power of the memory array. Data will not be retained when the device enters deep power-down mode.

Before entering DPD mode, the DRAM must be in all banks idle state with no activity on the data bus ($^{t}$RP time must be met). This mode is entered by holding CS# and WE# LOW with RAS# and CAS# HIGH at the rising edge of the clock, while CKE is LOW. CKE must be held LOW to maintain DPD mode. The clock must be stable prior to exiting DPD mode. This mode is exited by asserting CKE HIGH with either a NOP or DESELECT command present on the command bus. Upon exit from DPD mode, 200µs of valid clocks either with a NOP or DESELECT command present on the command bus are required, and a PRECHARGE ALL command and a full DRAM initialization sequence are required.

**Figure 34: Deep Power-Down Command**

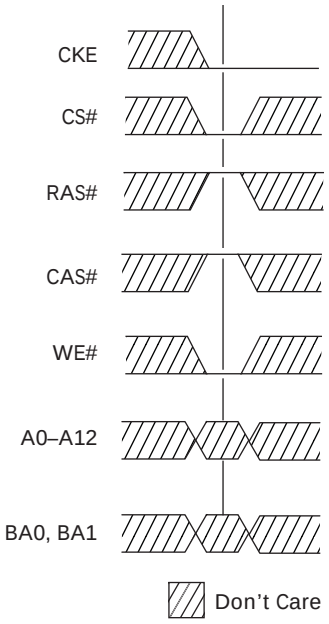



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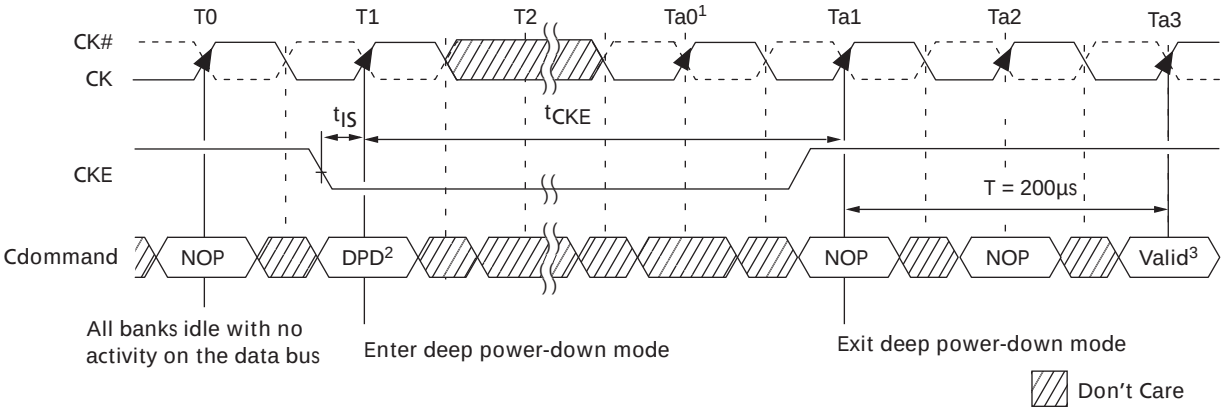
**Figure 35: Deep Power-Down**




Notes:
1. Clock must be stable prior to CKE going HIGH.
2. DPD = deep power-down command.
3. Upon exit from deep power-down mode, a PRECHARGE ALL command must be issued, followed by the initialization sequence (see page 14).


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**Table 9: Truth Table – CKE**

Notes 1–5 apply to all commands in this table

| $CKE_{n-1}$ | $CKE_n$ | Current State | $Command_n$ | $Action_n$ | Notes |
|---|---|---|---|---|---|
| L | L | Active power-down | X | Maintain active power-down | |
| L | L | Deep power-down | X | Maintain deep power-down | |
| L | L | (Precharge) power-down | X | Maintain (precharge) power-down | |
| L | L | SELF REFRESH | X | Maintain SELF REFRESH | |
| L | H | Active power-down | DESELECT or NOP | Exit active power-down | 6, 7 |
| L | H | Deep power-down | DESELECT or NOP | Exit deep power-down | 10, 11 |
| L | H | (Precharge) Power-down | DESELECT or NOP | Exit (precharge) power-down | 6, 7 |
| L | H | SELF REFRESH | DESELECT or NOP | Exit SELF REFRESH | 8, 9 |
| H | L | Bank(s) active | DESELECT or NOP | Active power-down entry | |
| H | L | All banks idle | BURST TERMINATE | Deep power-down entry | |
| H | L | All banks idle | DESELECT or NOP | (Precharge) Power-down entry | |
| H | L | All banks idle | AUTO REFRESH | SELF REFRESH entry | |
| H | H | | See Table 11 on page 54 | | |

Notes:
1. $CKE_n$ is the logic state of CKE at clock edge *n*; $CKE_{n-1}$ was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR SDRAM immediately prior to clock edge *n*.
3. $COMMAND_n$ is the command registered at clock edge *n*; and $ACTION_n$ is a result of $COMMAND_n$.
4. All states and sequences not shown are illegal or reserved.
5. $^tCKE$ pertains.
6. DESELECT or NOP commands should be issued on any clock edges occurring during the $^tXP$ period.
7. The clock must toggle at least one time during the $^tXP$ period.
8. DESELECT or NOP commands should be issued on any clock edges occurring during the $^tXSR$ period.
9. The clock must toggle at least one time during the $^tXSR$ period.
10. 200µs of valid clocks and NOP (or DESELECT) commands are required before any other valid command is allowed.
11. Upon exit from deep power-down mode and after the 200µs, a PRECHARGE ALL command is required, followed by the standard initialization sequence.


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**Table 10: Truth Table – Current State Bank *n* – Command to Bank *n***

Notes 1–6 apply to all states listed in this table; notes appear below and on next page

| Current State | CS# | RAS# | CAS# | WE# | Command (Action) | Notes |
|---|---|---|---|---|---|---|
| Any | H | X | X | X | DESELECT (NOP/continue previous operation) | |
| | L | H | H | H | NO OPERATION (NOP/continue previous operation) | |
| Idle | L | L | H | H | ACTIVE (select and activate row) | |
| | L | L | L | H | AUTO REFRESH | 7 |
| | L | L | L | L | LOAD MODE REGISTER | 7 |
| Row active | L | H | L | H | READ (select column and start READ burst) | 10 |
| | L | H | L | L | WRITE (select column and start WRITE burst) | 10 |
| | L | L | H | L | PRECHARGE (deactivate row in bank or banks) | 8 |
| Read (auto precharge disabled) | L | H | L | H | READ (select column and start new READ burst) | 10 |
| | L | H | L | L | WRITE (select column and start WRITE burst) | 10, 12 |
| | L | L | H | L | PRECHARGE (truncate READ burst, start PRECHARGE) | 8 |
| | L | H | H | L | BURST TERMINATE | 9 |
| Write (auto precharge disabled) | L | H | L | H | READ (select column and start READ burst) | 10, 11 |
| | L | H | L | L | WRITE (select column and start new WRITE burst) | 10 |
| | L | L | H | L | PRECHARGE (truncate WRITE burst, start PRECHARGE) | 8, 11 |

Notes:

1. This table applies when $CKE_{n-1}$ was HIGH and $CKE_n$ is HIGH and after $^tXSR$ has been met (if the previous state was SELF REFRESH), after $^tXP$ has been met (if the previous state was power-down), or 200µs if the previous state was DPD.
2. This table is bank-specific, except where noted (for example, the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state). Exceptions are discussed in the notes below.
3. Current state definitions:

   Idle: The bank has been precharged, and $^tRP$ has been met.
   Row active: A row in the bank has been activated, and $^tRCD$ has been met. No data bursts/accesses and no register accesses are in progress.
   Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
   Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

4. The following states must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to any other bank are determined by that bank's current state.

   Precharging: Starts with registration of a PRECHARGE command and ends when $^tRP$ is met. When $^tRP$ is met, the bank will be in the idle state.
   Row activating: Starts with registration of an ACTIVE command and ends when $^tRCD$ is met. When $^tRCD$ is met, the bank will be in the row active state.
   Read with auto precharge enabled: Starts with registration of a READ command with auto precharge enabled and ends when $^tRP$ has been met. When $^tRP$ is met, the bank will be in the idle state.
   Write with auto precharge enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when $^tRP$ has been met. When $^tRP$ is met, the bank will be in the idle state.


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5. : The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied on each positive clock edge during these states.

| | |
|---|---|
| Refreshing | Starts with registration of an AUTO REFRESH command and ends when $^{t}$RFC is met. When $^{t}$RFC is met, the Mobile DDR SDRAM will be in the all banks idle state. |
| Accessing mode register | Starts with registration of a LOAD MODE REGISTER command and ends when $^{t}$MRD has been met. When $^{t}$MRD is met, the Mobile DDR SDRAM will be in the all banks idle state. |
| Precharging all: | Starts with registration of a PRECHARGE ALL command and ends when $^{t}$RP is met. When $^{t}$RP is met, all banks will be in the idle state. |

6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks be idle, and bursts not be in progress.
8. May or may not be bank-specific; if multiple banks are to be precharged, each must have an open row.
9. Not bank-specific; BURST TERMINATE affects the most recent READ burst, regardless of bank.
10. READs or WRITEs listed in the Command (Action) column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
11. Requires appropriate DM masking.
12. A WRITE command may be applied after the completion of the READ burst; otherwise, a BURST TERMINATE must be used to end the READ burst prior to asserting a WRITE command.


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**Table 11: Truth Table – Current State Bank *n* – Command to Bank *m***

Notes 1–6 apply to all states listed in this table; the other referenced notes appear below and on next page

| Current State | CS# | RAS# | CAS# | WE# | Command (Action) | Notes |
|---|---|---|---|---|---|---|
| Any | H | X | X | X | DESELECT (NOP/continue previous operation) | |
| | L | H | H | H | NO OPERATION (NOP/continue previous operation) | |
| Idle | X | X | X | X | Any command otherwise allowed to bank *m* | |
| Row activating,active, or precharging | L | L | H | H | ACTIVE (select and activate row) | |
| | L | H | L | H | READ (select column and start READ burst) | 7 |
| | L | H | L | L | WRITE (select column and start WRITE burst) | 7 |
| | L | L | H | L | PRECHARGE | |
| Read (auto precharge disabled) | L | L | H | H | ACTIVE (select and activate row) | |
| | L | H | L | H | READ (select column and start new READ burst) | 7 |
| | L | H | L | L | WRITE (select column and start WRITE burst) | 7, 9 |
| | L | L | H | L | PRECHARGE | |
| Write (auto precharge disabled) | L | L | H | H | ACTIVE (select and activate row) | |
| | L | H | L | H | READ (select column and start READ burst) | 7, 10 |
| | L | H | L | L | WRITE (select column and start new WRITE burst) | 7 |
| | L | L | H | L | PRECHARGE | |
| Read (with auto precharge) | L | L | H | H | ACTIVE (select and activate row) | |
| | L | H | L | H | READ (select column and start new READ burst) | 3a, 7 |
| | L | H | L | L | WRITE (select column and start WRITE burst) | 3a, 7 |
| | L | L | H | L | PRECHARGE | |
| Write (with auto precharge) | L | L | H | H | ACTIVE (select and activate row) | |
| | L | H | L | H | READ (select column and start READ burst) | 3a,7 |
| | L | H | L | L | WRITE (select column and start new WRITE burst) | 3a,7 |
| | L | L | H | L | PRECHARGE | |

Notes:

1. This table applies when $CKE_{n-1}$ was HIGH and $CKE_n$ is HIGH and after $^tXSR$ has been met (if the previous state was SELF REFRESH) or after $^tXP$ has been met (if the previous state was power-down) or 200µs if the previous state was deep power-down).
2. This table describes alternate bank operation, except where noted (for example, the current state is for bank n and the commands shown are those allowed to be issued to bank *m,* assuming that bank *m* is in such a state that given command is allowable). Exceptions are covered in the notes below.
3. Current state definitions:

   Idle: The bank has been precharged, and $^tRP$ has been met.

   Row active: A row in the bank has been activated, and $^tRCD$ has been met. No data bursts/accesses and no register accesses are in progress.

   Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

   Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

   3a. The READ with auto precharge enabled or WRITE with auto precharge enabled states can each be broken into two parts: the access period and the precharge period. For read with auto precharge, the precharge period is defined as if the same burst were executed with auto precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For write with auto precharge, the precharge period begins when $^tWR$ ends, with $^tWR$ measured as if auto precharge were disabled. The access period starts with registration of the command and ends where the precharge period (or $^tRP$) begins.


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This device supports concurrent auto precharge such that when a read with auto precharge is enabled or a write with auto precharge is enabled, any command to other banks is supported, as long as that command does not interrupt the read or write data transfer already in process. In either case, all other related limitations apply (that is, contention between read data and write data must be avoided).

3b. The minimum delay from a READ or WRITE command with auto precharge enabled to a command to a different bank is summarized below.

| From Command | To Command | Minimum Delay (with Concurrent Auto Precharge) |
|---|---|---|
| WRITE (with auto precharge) | READ or READ (with auto precharge) | [1 + (BL/2)] $^{t}$CK + $^{t}$WTR |
| | WRITE or WRITE (with auto precharge) | (BL/2) $^{t}$CK |
| | PRECHARGE | 1 $^{t}$CK |
| | ACTIVE | 1 $^{t}$CK |
| READ (with auto precharge) | READ or READ (with auto precharge) | (BL/2) × $^{t}$CK |
| | WRITE or WRITE (with auto precharge) | [$CL_{RU}$ + (BL/2)] $^{t}$CK |
| | PRECHARGE | 1 $^{t}$CK |
| | ACTIVE | 1 $^{t}$CK |

$CL_{RU}$ = CAS latency (CL) rounded up to the next integer; BL = burst length

4. AUTO REFRESH and LOAD MODE REGISTER commands may only be issued when all banks are idle.
5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs listed in the Command (Action) column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
8. Requires appropriate DM masking.
9. A WRITE command may be applied after the completion of the READ burst; otherwise, a BURST TERMINATE must be used to end the READ burst prior to asserting a WRITE command.
10. A READ command may be applied after the completion of the WRITE burst; otherwise, a BURST TERMINATE must be used to end the WRITE burst prior to asserting a READ command.


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# Electrical Specifications

## Absolute Maximum Ratings

Stresses greater than those listed in Table 12 may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Table 12: Absolute Maximum Ratings**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$ | $V_{DD}$ supply voltage relative to $V_{SS}$ | –0.3 | 2.7 | V |
| $V_{DDQ}$ | $V_{DDQ}$ supply voltage relative to $V_{SS}$ | –0.3 | 2.7 | V |
| $V_{IN}$, $V_{OUT}$ | Voltage on any pin relative to $V_{SS}$ | –0.3 | 2.7 | V |
| $T_{STG}$ | Storage temperature | –55 | +150 | °C |

**Table 13: Electrical Characteristics and Operating Conditions**

Notes 1–5 on pages 52 and 53 apply to all parameters in this table; see other indicated notes on pages 63–65

$V_{DD}/V_{DDQ}$ = 1.70–1.95V

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | 1.70 | 1.95 | V | 26, 29 |
| I/O supply voltage | $V_{DDQ}$ | 1.70 | 1.95 | V | 26, 29 |
| **Address and command inputs** | | | | | |
| Input HIGH voltage | $V_{IH}$ | 0.8 × $V_{DDQ}$ | $V_{DDQ}$ + 0.3 | V | 21, 28 |
| Input LOW voltage | $V_{IL}$ | –0.3 | 0.2 × $V_{DDQ}$ | V | 21, 28 |
| **Clock inputs (CK, CK#)** | | | | | |
| DC input voltage | $V_{IN}$ | –0.3 | $V_{DDQ}$ + 0.3 | V | 22 |
| DC input differential voltage | $V_{ID(DC)}$ | 0.4 × $V_{DDQ}$ | $V_{DDQ}$ + 0.6 | V | 7,22 |
| AC input differential voltage | $V_{ID(AC)}$ | 0.6 × $V_{DDQ}$ | $V_{DDQ}$ + 0.6 | V | 7,22 |
| AC differential crossing voltage | $V_{IX}$ | 0.4 × $V_{DDQ}$ | 0.6 × $V_{DDQ}$ | V | 8, 22 |
| **Data inputs** | | | | | |
| DC input HIGH voltage | $V_{IH(DC)}$ | 0.7 × $V_{DDQ}$ | $V_{DDQ}$ + 0.3 | V | 21, 23, 28 |
| AC input HIGH voltage | $V_{IH(AC)}$ | 0.8 × $V_{DDQ}$ | $V_{DDQ}$ + 0.3 | V | 21, 23, 28 |
| DC input LOW voltage | $V_{IL(DC)}$ | –0.3 | 0.3 × $V_{DDQ}$ | V | 21, 23, 28 |
| AC input LOW voltage | $V_{IL(AC)}$ | –0.3 | 0.2 × $V_{DDQ}$ | V | 21, 23, 28 |
| **Data outputs** | | | | | |
| DC output HIGH voltage: Logic 1 ($I_{OH}$ = –0.1mA) | $V_{OH}$ | 0.9 × $V_{DDQ}$ | – | V | 27 |
| DC output LOW voltage: Logic 0 ($I_{OL}$ = 0.1mA) | $V_{OL}$ | – | 0.1 × $V_{DDQ}$ | V | 27 |
| **Leakage current** | | | | | |
| Input leakage current<br>Any input 0V ≤ $V_{IN}$ ≤ $V_{DD}$<br>(All other pins not under test = 0V) | $I_I$ | –1 | 1 | µA | |
| Output leakage current<br>(DQ are disabled; 0V ≤ $V_{OUT}$ ≤ $V_{DDQ}$) | $I_{OZ}$ | –5 | 5 | µA | |
| **Operating temperature** | | | | | |
| Commercial | $T_A$ | 0 | +70 | °C | |
| Industrial | $T_A$ | –40 | +85 | °C | |


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**Table 14: Capacitance (x16, x32)**

Note 41 on page 65 applies to all parameters in this table; notes appear on pages 63–65

| Parameter | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Delta input/output capacitance: DQ, DQS, DM | $DC_{IO}$ | – | 0.50 | pF | 17 |
| Delta input capacitance: command and address | $DC_{I1}$ | – | 0.50 | pF | |
| Delta input capacitance: CK, CK# | $DC_{I2}$ | – | 0.25 | pF | |
| Input/output capacitance: DQ, DQS, DM | $C_{IO}$ | 2.0 | 4.5 | pF | |
| Input capacitance: command and address | $C_{I1}$ | 1.5 | 3.0 | pF | |
| Input capacitance: CK, CK# | $C_{I2}$ | 1.5 | 3.5 | pF | |
| Input capacitance: CS#, CKE | $C_{I3}$ | 1.5 | 3.0 | pF | |


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**Table 15: IDD Specifications and Conditions (x16)**

Notes: 1–5, 9, 11 apply to all parameters in this table; notes appear on pages 63–65; VDD/VDDQ = 1.70–1.95V

| Parameter/Condition | | Symbol | Max -6 | Max -75 | Units | Notes |
|---|---|---|---|---|---|---|
| **Operating one bank active-precharge current**: tRFC = tRFC (MIN); tCK = tCK (MIN); CKE = HIGH; CS = HIGH between valid commands; Address inputs are switching every two clock cycles; Data bus inputs are stable | | IDD0 | 60 | 55 | mA | 16 |
| **Precharge power-down standby current**: All banks idle; CKE is LOW; CS is HIGH, tCK = tCK (MIN); Address and control inputs are switching; Data bus inputs are stable | | IDD2P Standard | 300 | 300 | µA | 36 |
| | | IDD2P Low power | 220 | 220 | | 36 |
| **Precharge power-down standby current with clock stopped**: All banks idle; CKE is LOW; CS is HIGH, CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable | | IDD2PS Standard | 300 | 300 | µA | 36 |
| | | IDD2PS Low power | 220 | 220 | | 36 |
| **Precharge non-power-down standby current**: All banks idle; CKE = HIGH; CS = HIGH; tCK = tCK (MIN); Address and control inputs are switching; Data bus inputs are stable | | IDD2N | 25 | 20 | mA | |
| **Precharge non-power-down standby current with clock stopped**: All banks idle; CKE = HIGH; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable | | IDD2NS | 5 | 5 | mA | |
| **Active power-down standby current**: One bank active; CKE = LOW; CS = HIGH; tCK = tCK (MIN); Address and control inputs are switching; Data bus inputs are stable | | IDD3P | 5 | 5 | mA | |
| **Active power-down standby current with clock stopped**: One bank active; CKE = LOW; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable | | IDD3PS | 3 | 3 | mA | |
| **Active non-power-down standby current**: One bank active; CKE = HIGH; CS = HIGH; tCK = tCK (MIN); Address and control inputs are switching; Data bus inputs are stable | | IDD3N | 25 | 20 | mA | 16 |
| **Active non-power-down standby current with clock stopped**: One bank active; CKE = HIGH; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable | | IDD3NS | 10 | 10 | mA | 16 |
| **Operating burst read**: One bank active; BL = 4; CL = 3; tCK = tCK (MIN); Continuous read bursts; IOUT = 0mA; Address inputs are switching every two clock cycles; 50 percent data changing each burst | | IDD4R | 100 | 95 | mA | 16 |
| **Operating burst write**: One bank active; BL = 4; tCK= tCK (MIN); Continuous write bursts; Address inputs are switching; 50 percent data changing each burst | | IDD4W | 100 | 100 | mA | 16 |
| **Auto refresh current**: Burst refresh; CKE = HIGH; Address and control inputs are switching; Data bus inputs are stable | tRFC = tRFC (MIN) | IDD5 | 65 | 60 | mA | |
| | tRFC = tREFI | IDD5a | 3 | 3 | mA | 20 |
| **Deep power-down current**: Address and control inputs are stable; Data bus inputs are stable | | IDD8 | 10 | 10 | µA | 36, 38 |


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**Table 16: IDD Specifications and Conditions (x32)**

Notes: 1–5, 9, 11 apply to all parameters in this table; notes appear on pages 63–65; VDD/VDDQ = 1.70–1.95V

| Parameter/Condition | | Symbol | Max | | Units | Notes |
|---|---|---|---|---|---|---|
| | | | -6 | -75 | | |
| **Operating one bank active-precharge current**: tRFC = tRFC (MIN); tCK = tCK (MIN); CKE = HIGH; CS = HIGH between valid commands; Address inputs are switching every two clock cycles; Data bus inputs are stable | JEDEC-standard option | IDD0 | 80 | 65 | mA | 16, 36 |
| | Reduced page-size option | IDD0 | 70 | 55 | mA | 16, 35 |
| **Precharge power-down standby current**: All banks idle; CKE is LOW; CS is HIGH, tCK = tCK (MIN); Address and control inputs are switching; Data bus inputs are stable | | IDD2P Standard | 300 | 300 | µA | 36 |
| | | IDD2P Low power | 220 | 220 | | 36 |
| **Precharge power-down standby current with clock stopped**: All banks idle; CKE is LOW; CS is HIGH, CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable | | IDD2PS Standard | 300 | 300 | µA | 36 |
| | | IDD2PS Low power | 220 | 220 | | 36 |
| **Precharge non-power-down standby current**: All banks idle; CKE = HIGH; CS = HIGH; tCK = tCK (MIN); Address and control inputs are switching; Data bus inputs are stable | | IDD2N | 25 | 20 | mA | |
| **Precharge non-power-down standby current with clock stopped**: All banks idle; CKE = HIGH; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable | | IDD2NS | 5 | 5 | mA | |
| **Active power-down standby current**: One bank active; CKE = LOW; CS = HIGH; tCK = tCK (MIN); Address and control inputs are switching; Data bus inputs are stable | | IDD3P | 5 | 5 | mA | |
| **Active power-down standby current with clock stopped**: One bank active; CKE = LOW; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable | | IDD3PS | 3 | 3 | mA | |
| **Active non-power-down standby current**: One bank active; CKE = HIGH; CS = HIGH; tCK = tCK (MIN); Address and control inputs are switching; Data bus inputs are stable | | IDD3N | 25 | 20 | mA | 16 |
| **Active non-power-down standby current with clock stopped**: One bank active; CKE = HIGH; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable | | IDD3NS | 10 | 10 | mA | 16 |
| **Operating burst read**: One bank active; BL = 4; CL = 3; tCK = tCK (MIN); IOUT = 0mA; Address inputs are switching every two clock cycles; 50 percent data changing each burst | | IDD4R | 135 | 115 | mA | 16 |
| **Operating burst WRITE**: One bank active; BL = 4; tCK = tCK (MIN); Address inputs are switching; 50 percent data changing each burst | JEDEC-standard option | IDD4W | 160 | 140 | mA | 16, 36 |
| | Reduced page-size option | IDD4W | 140 | 120 | mA | 16, 35 |
| **Auto refresh current**: Burst refresh; CKE = HIGH; Address and control inputs are switching; Data bus inputs are stable | tRC = tRFC (MIN) | IDD5 | 65 | 60 | mA | |
| | tRC = tREFI | IDD5a | 3 | 3 | mA | 20 |
| **Deep power-down current**: Address and control inputs are stable; Data bus inputs are stable | | IDD8 | 10 | 10 | µA | 36, 38 |


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**Table 17: IDD6 Specifications and Conditions (x16, x32)**

Notes: 1–5, 9, 10, 36, and 39 apply to all parameters in this table; notes appear on pages 63–65; VDD/VDDQ = 1.70–1.95V

| Parameter/Condition | | Symbol | Low IDD6 Option "L" | Standard IDD6 Option | Units |
|---|---|---|---|---|---|
| **Self refresh current**: CKE = LOW; tCK = tCK (MIN); Address and control inputs are stable; Data bus input are stable | Full array, 85°C | IDD6a | 220 | 300 | µA |
| | Full array, 70°C | IDD6b | 175 | 210 | µA |
| | Full array, 45°C | IDD6c | 140 | 190 | µA |
| | Full array 15°C | IDD6d | 125 | 180 | µA |
| | Half array, 85°C | IDD6a | 200 | 275 | µA |
| | Half array, 70°C | IDD6b | 150 | 180 | µA |
| | Half array, 45°C | IDD6c | 130 | 160 | µA |
| | Half array, 15°C | IDD6d | 115 | 150 | µA |
| | 1/4 array, 85°C | IDD6a | 185 | 265 | µA |
| | 1/4 array, 70°C | IDD6b | 140 | 160 | µA |
| | 1/4 array, 45°C | IDD6c | 120 | 140 | µA |
| | 1/4 array, 15°C | IDD6d | 115 | 140 | µA |
| | 1/8 array, 85°C | IDD6a | 175 | 255 | µA |
| | 1/8 array, 70°C | IDD6b | 125 | 150 | µA |
| | 1/8 array, 45°C | IDD6c | 115 | 130 | µA |
| | 1/8 array, 15°C | IDD6d | 110 | 125 | µA |
| | 1/16 array, 85°C | IDD6a | 170 | 250 | µA |
| | 1/16 array, 70°C | IDD6b | 120 | 140 | µA |
| | 1/16 array, 45°C | IDD6c | 110 | 120 | µA |
| | 1/16 array, 15°C | IDD6d | 105 | 115 | µA |

**Figure 36: Typical Self Refresh Current vs. Temperature (x16, x32)**

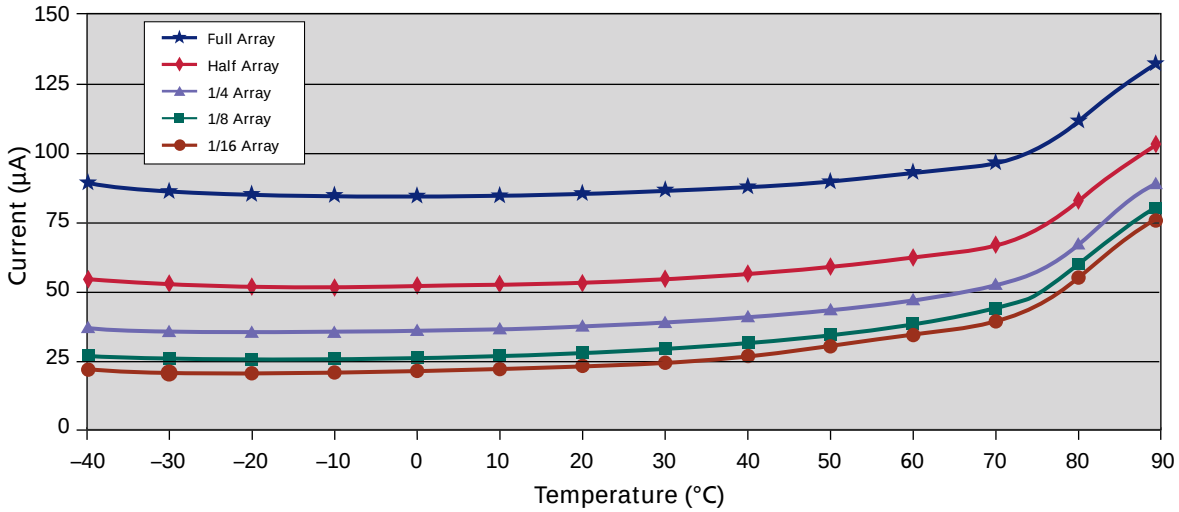



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**Table 18: Electrical Characteristics and Recommended AC Operating Conditions**

Notes: 1–6, 22 apply to all parameters in this table; notes appear on pages 63–65; VDD/VDDQ = 1.70–1.95V

| Parameter | | Symbol | -6 | | -75 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | | |
| Access window of DQ from CK/CK# | CL = 3 | tAC(3) | 2.0 | 5.0 | 2.0 | 6.0 | ns | |
| | CL = 2 | tAC(2) | 2.0 | 6.5 | 2.0 | 6.5 | | |
| CK high-level width | | tCH | 0.45 | 0.55 | 0.45 | 0.55 | tCK | |
| CK low-level width | | tCL | 0.45 | 0.55 | 0.45 | 0.55 | tCK | |
| Clock cycle time | CL = 3 | tCK(3) | 6 | – | 7.5 | – | ns | 24 |
| | CL = 2 | tCK(2) | 12 | – | 12 | – | | |
| Minimum tCKE HIGH/LOW time | | tCKE | 1 | – | 1 | – | tCK | |
| Auto precharge write recovery + precharge time | | tDAL | – | – | – | – | | 32 |
| DQ and DM input hold time relative to DQS | | tDH | 0.5 | – | 0.75 | – | ns | 19,23,31 |
| DQ and DM input setup time relative to DQS | | tDS | 0.5 | – | 0.75 | – | ns | 19,23,31 |
| DQ and DM input pulse width (for each input) | | tDIPW | 1.8 | – | 1.8 | – | ns | 33 |
| Access window of DQS from CK/CK# | CL = 3 | tDQSCK(3) | 2.0 | 5.0 | 2.0 | 6.0 | ns | |
| | CL = 2 | tDQSCK(2) | 2.0 | 6.5 | 2.0 | 6.5 | | |
| DQS input HIGH pulse width | | tDQSH | 0.35 | 0.6 | 0.4 | 0.6 | tCK | |
| DQS input LOW pulse width | | tDQSL | 0.35 | 0.6 | 0.4 | 0.6 | tCK | |
| DQS–DQ skew, DQS to last DQ valid, per group, per access | | tDQSQ | – | 0.5 | – | 0.6 | ns | 18, 19 |
| WRITE command to first DQS latching transition | | tDQSS | 0.75 | 1.25 | 0.75 | 1.25 | tCK | |
| DQS falling edge to CK rising - setup time | | tDSS | 0.2 | – | 0.2 | – | tCK | |
| DQS falling edge from CK rising - hold time | | tDSH | 0.2 | – | 0.2 | – | tCK | |
| Data valid output window (DVW) | | n/a | tQH - tDQSQ | | tQH - tDQSQ | | ns | 18 |
| Half clock period | | tHP | tCH, tCL | – | tCH, tCL | – | ns | 24 |
| Data-out High-Z window from CK/CK# | CL = 3 | tHZ(3) | – | 5.0 | – | 6.0 | ns | 12, 30 |
| | CL = 2 | tHZ(2) | – | 6.5 | – | 6.5 | ns | |
| Data-out Low-Z window from CK/CK# | | tLZ | 1.0 | – | 1.0 | – | ns | 12, 30 |
| Address and control input hold time (fast slew rate) | | tIHF | 1.1 | – | 1.3 | – | ns | 11 |
| Address and control input setup time (fast slew rate) | | tISF | 1.1 | – | 1.3 | – | ns | 11 |
| Address and control input hold time (slow slew rate) | | tIHS | 1.2 | – | 1.5 | – | ns | 11 |
| Address and control input setup time (slow slew rate) | | tISS | 1.2 | – | 1.5 | – | ns | 11 |
| Address and control input pulse width | | tIPW | 2.6 | – | 2.6 | – | ns | 33 |
| LOAD MODE REGISTER command cycle time | | tMRD | 2 | – | 2 | – | tCK | |
| DQ–DQS hold, DQS to first DQ to go non-valid, per access | | tQH | tHP - tQHS | – | tHP - tQHS | – | ns | 18, 19 |
| Data hold skew factor | | tQHS | | 0.65 | – | 0.75 | ns | |
| ACTIVE-to-PRECHARGE command | | tRAS | 42 | 70,000 | 45 | 70,000 | ns | 25 |
| ACTIVE-to-ACTIVE or ACTIVE-to-AUTO REFRESH command period | | tRC | 60 | – | 75 | – | ns | |
| ACTIVE-to-READ or WRITE delay | | tRCD | 18 | – | 22.5 | – | ns | |
| Refresh period | | tREF | – | 64 | – | 64 | ms | |
| Average periodic refresh interval (x16) | | tREFI | – | 7.8 | – | 7.8 | µs | 37 |
| Average periodic refresh interval (x32) | | tREFI | – | 15.6 | – | 15.6 | µs | 37 |
| AUTO REFRESH command period | | tRFC | 70 | – | 70 | – | ns | |
| PRECHARGE command period | | tRP | 18 | – | 22.5 | – | ns | |


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**Table 18: Electrical Characteristics and Recommended AC Operating Conditions (Continued)**

Notes: 1–6, 22 apply to all parameters in this table; notes appear on pages 63–65; VDD/VDDQ = 1.70–1.95V

| Parameter | | Symbol | -6 | | -75 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | | |
| DQS read preamble | CL = 2 | tRPRE(2) | 0.5 | 1.1 | 0.5 | 1.1 | tCK | |
| | CL = 3 | tRPRE(3) | 0.9 | 1.1 | 0.9 | 1.1 | | |
| DQS read postamble | | tRPST | 0.4 | 0.6 | 0.4 | 0.6 | tCK | |
| ACTIVE bank *a* to ACTIVE bank *b* command | | tRRD | 12 | – | 15 | – | ns | |
| DQS write preamble | | tWPRE | 0.25 | – | 0.25 | – | tCK | |
| DQS write preamble setup time | | tWPRES | 0 | – | 0 | – | ns | 14, 15 |
| DQS write postamble | | tWPST | 0.4 | 0.6 | 0.4 | 0.6 | tCK | 13 |
| WRITE recovery time | | tWR | 12 | – | 15 | – | ns | 40 |
| Internal WRITE to READ command delay | | tWTR | 1 | – | 1 | – | tCK | |
| Exit power-down to first valid command | | tXP | 1 | – | 1 | – | tCK | |
| Exit SELF REFRESH to first valid command | | tXSR | 120 | – | 120 | – | ns | |


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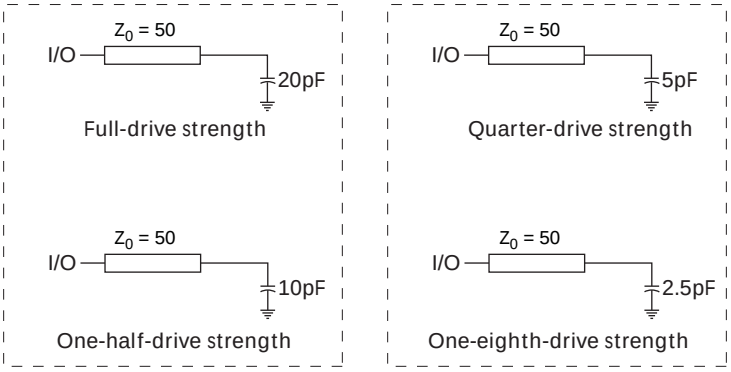
# Notes

1. All voltages referenced to $V_{SS}$.
2. All parameters assume proper device initialization.
3. Tests for AC timing, $I_{DD}$, and electrical AC and DC characteristics may be conducted at nominal supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
4. Outputs measured with equivalent load; transmission line delay is assumed to be very small:




5. Timing and $I_{DD}$ tests may use a $V_{IL}$-to-$V_{IH}$ swing of up to 1.5V in the test environment, but input timing is still referenced to $V_{DDQ}/2$ (or to the crossing point for CK/CK#). The output timing reference voltage level is $V_{DDQ}/2$.
6. All AC timings assume an input slew rate of 1V/ns.
7. $V_{ID}$ is the magnitude of the difference between the input level on CK and the input level on CK#.
8. The value of $V_{IX}$ is expected to equal $V_{DDQ}/2$ of the transmitting device and must track variations in the DC level of the same.
9. $I_{DD}$ is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time at CL = 3 for -6 and CL = 3 for -75 with the outputs open.
10. Enables on-chip refresh and address counters.
11. Fast command/address input slew rate ≥1 V/ns. Slow command/address input slew rate ≥0.5 V/ns. If the slew rate is less than 0.5 V/ns, timing must be derated: $^{t}IS$ has an additional 50ps per each 100 mV/ns reduction in slew rate from the 0.5 V/ns. $^{t}IH$ remains constant. If the slew rate exceeds 4.5 V/ns, functionality is uncertain.
12. $^{t}HZ$ and $^{t}LZ$ transitions occur in the same access time windows as data valid transitions. These parameters are not referenced to a specific voltage level but specify when the device output is no longer driving (HZ) or begins driving (LZ).
13. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
14. This is not a device limit. The device will operate with a negative value, but system performance (bus turnaround) will degrade accordingly.
15. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on $^{t}DQSS$.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16. MIN ($^{t}$RC or $^{t}$RFC) for IDD measurements is the smallest multiple of $^{t}$CK that meets the minimum absolute value for the respective parameter.
17. The I/O capacitance per DQS and DQ byte/group will not differ by more than this maximum amount for any given device.
18. The data valid window is derived by achieving other specifications: $^{t}$HP ($^{t}$CK/2), $^{t}$DQSQ, and $^{t}$QH ($^{t}$QH = $^{t}$HP - $^{t}$QHS). The data valid window derates in direct proportion to the clock duty cycle, and a practical data valid window can be derived. The clock is allowed a maximum duty cycle variation of 45/55. Functionality is uncertain when operating beyond a 45/55 ratio.
19. Referenced to each output group: for x16, LDQS with DQ0–DQ7; and UDQS with DQ8–DQ15. For x32, DQS0 with DQ0–DQ7; DQS1 with DQ8–DQ15; DQS2 with DQ16–DQ23; and DQS3 with DQ24–DQ31.
20. This limit is actually a nominal value and does not result in a fail value. CKE is HIGH during REFRESH command period ($^{t}$RFC [MIN]) else CKE is LOW (for example, during standby).
21. To maintain a valid level, the transitioning edge of the input must:
    a. Sustain a constant slew rate from the current AC level through to the target AC level, VIL(AC) or VIH(AC).
    b. Reach at least the target AC level.
    c. After the AC target level is reached, continue to maintain at least the target DC level, VIL(DC) or VIH(DC).
22. CK and CK# input slew rate must be ≥1 V/ns (2 V/ns if measured differentially).
23. DQ and DM input slew rates must not deviate from DQS by more than 10 percent. If the DQ/DM/DQS slew rate is less than 0.5 V/ns, timing must be derated: 50ps must be added to $^{t}$DS and $^{t}$DH for each 100 mV/ns reduction in slew rate. If slew rate exceeds 4 V/ns, functionality is uncertain.
24. $^{t}$HP (MIN) is the lesser of $^{t}$CL minimum and $^{t}$CH minimum actually applied to the device CK and CK# inputs, collectively.
25. READs and WRITEs with auto precharge are not allowed to be issued until $^{t}$RAS (MIN) can be satisfied prior to the internal PRECHARGE command being issued.
26. Any positive glitch must be less than 1/3 of the clock cycle and not more than +200mV or 2.0V, whichever is less. Any negative glitch must be less than 1/3 of the clock cycle and not exceed either –150mV or 1.6V, whichever is more positive.
27. The voltage levels used are derived from a minimum VDD level and the referenced test load. In practice, the voltage levels obtained from a properly terminated bus will provide significantly different voltage values.
28. VIH overshoot: VIH (MAX) = VDDQ + 1.0V for a pulse width ≤3ns, and the pulse width cannot be greater than 1/3 of the cycle rate. VIL undershoot: VIL (MIN) = –1.0V for a pulse width ≤3ns, and the pulse width cannot be greater than 1/3 of the cycle rate.
29. VDD and VDDQ must track each other, and VDDQ must be less than or equal to VDD.
30. $^{t}$HZ (MAX) will prevail over $^{t}$DQSCK (MAX) + $^{t}$RPST (MAX) condition.
31. The transition times for input signals (CAS#, CKE, CS#, DM, DQ, DQS, RAS#, WE#, and addresses) are measured between VIL(DC) and VIH(AC) for rising input signals and between VIH(DC) and VIL(AC) for falling input signals.
32. $^{t}$DAL = ($^{t}$WR/$^{t}$CK) + ($^{t}$RP/$^{t}$CK): for each term, if not already an integer, round to the next higher integer.
33. These parameters guarantee device timing, but are not tested on each device.
34. Clock must be toggled a minimum of two times during this period.


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35. Reduced page-size option (A12). See page 1.
36. Current may be slightly higher for up to 500ms when entering this operating mode.
37. The maximum $^{t}$REFI value applies to both A11 and A12 row size ordering options.
38. Deep power-down current is nominal value at 25°C. The parameter is not tested.
39. The values for IDD6 85°C are 100 percent tested. Values for 70°C, 45°C, and 15°C are sampled only.
40. At least one clock cycle is required during $^{t}$WR time when in auto-precharge mode.
41. This parameter is sampled. VDD/VDDQ = 1.70–1.95V, f = 100 MHz, $T_A$ = 25°C, VOUT (DC) = VDDQ/2, VOUT (peak-to-peak) = 0.2V.
DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.


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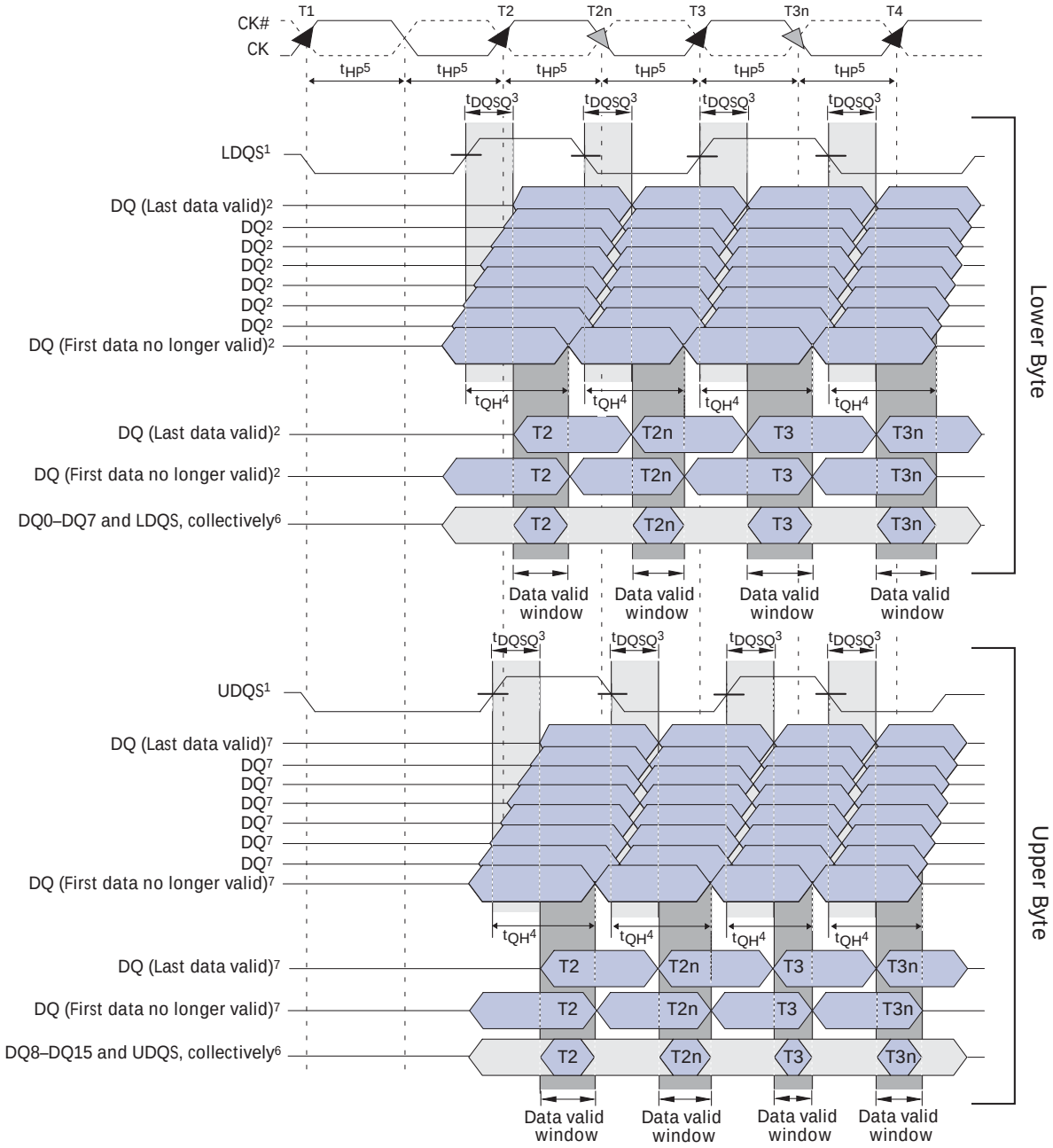
# Timing Diagrams

**Figure 37: Data Output Timing – $^{t}$DQSQ, $^{t}$QH, and Data Valid Window (x16)**




Notes:
1. DQ transitioning after DQS transitions defines the $^{t}$DQSQ window. LDQS defines the lower byte, and UDQS defines the upper byte.
2. DQ0, DQ1, DQ2, DQ3, DQ4, DQ5, DQ6, or DQ7.
3. $^{t}$DQSQ is derived at each DQS clock edge and is not cumulative over time and begins with DQS transition and ends with the last valid DQ transition.
4. $^{t}$QH is derived from $^{t}$HP: $^{t}$QH = $^{t}$HP - $^{t}$QHS.
5. $^{t}$HP is the lesser of $^{t}$CL or $^{t}$CH clock transition collectively when a bank is active.
6. The data valid window is derived for each DQS transition and is defined as $^{t}$QH - $^{t}$DQSQ.
7. DQ8, DQ9, DQ10, DQ11, DQ12, DQ13, DQ14, or DQ15.


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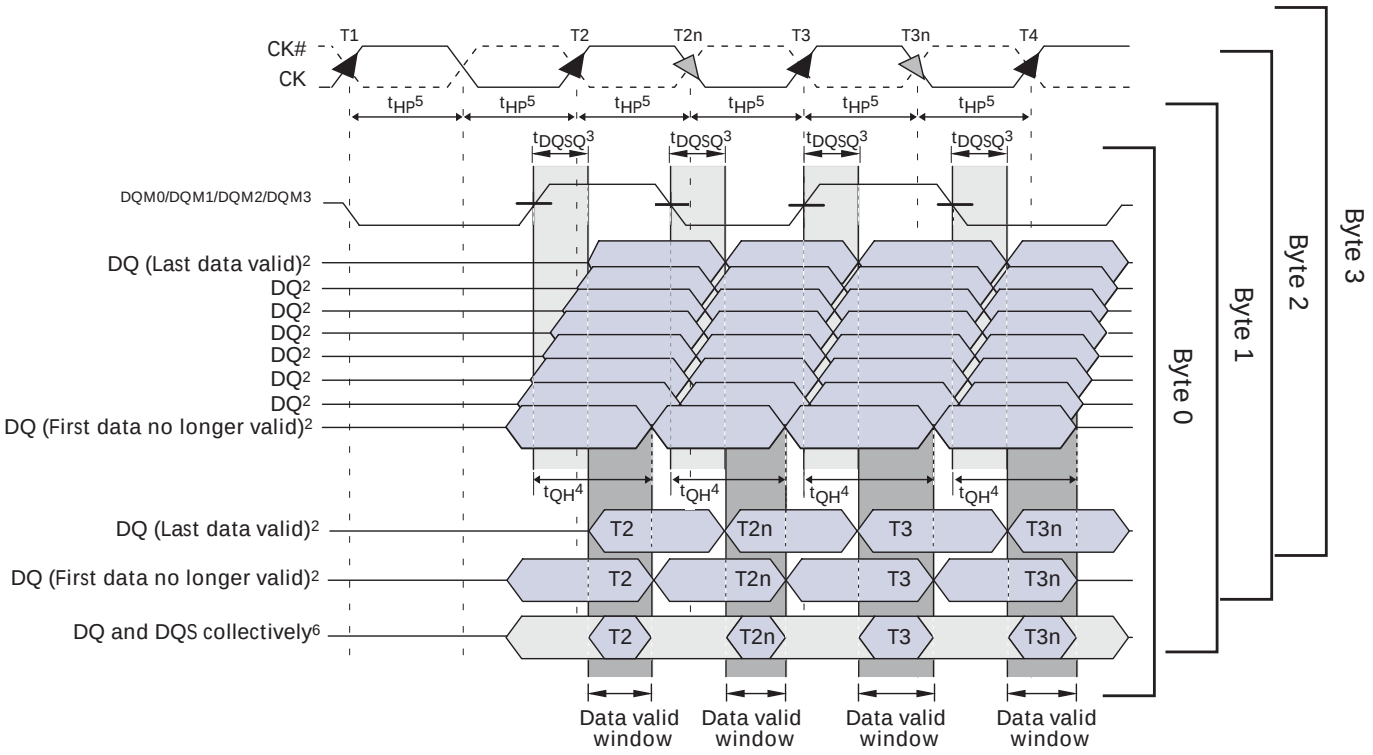
**Figure 38: Data Output Timing – $^{t}$DQSQ, $^{t}$QH, and Data Valid Window (x32)**




Notes:
1. DQ transitioning after DQS transitions defines the $^{t}$DQSQ window.
2. Byte 0 is DQ[7:0]; byte 1 is DQ[15:8]; byte 2 is DQ[23:16]; byte 3 is DQ[31:24].
3. $^{t}$DQSQ is derived at each DQS clock edge and is not cumulative over time and begins with DQS transition and ends with the last valid DQ transition.
4. $^{t}$QH is derived from $^{t}$HP: $^{t}$QH = $^{t}$HP - $^{t}$QHS.
5. $^{t}$HP is the lesser of $^{t}$CL or $^{t}$CH clock transition collectively when a bank is active.
6. The data valid window is derived for each DQS transition and is $^{t}$QH - $^{t}$DQSQ.


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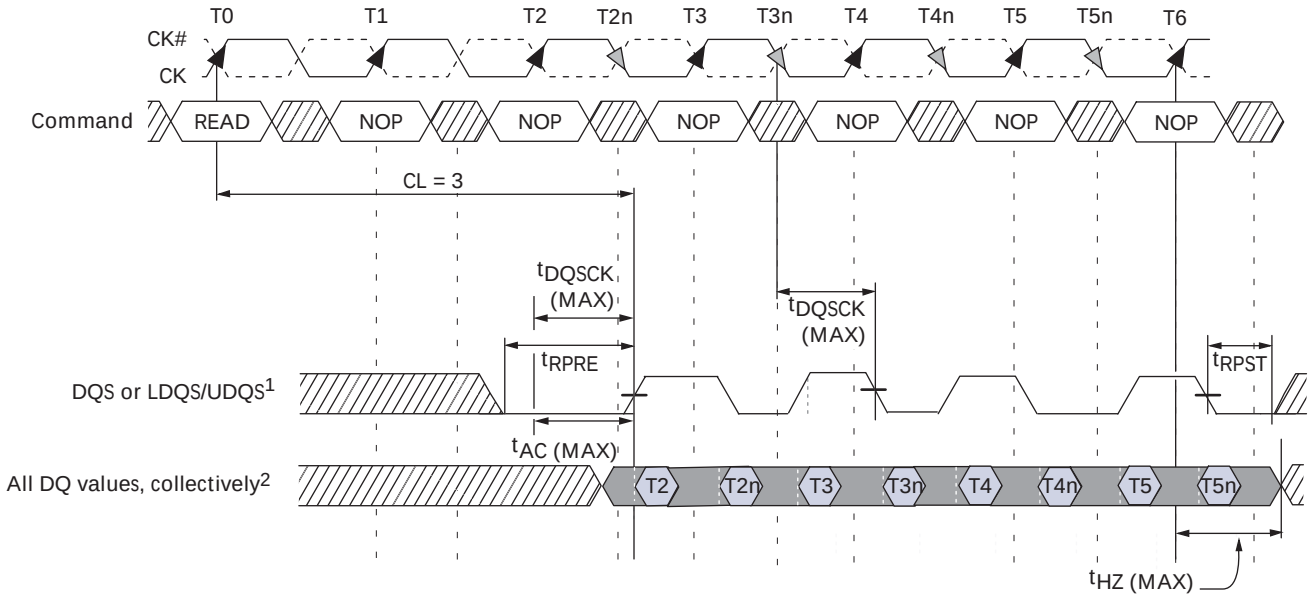
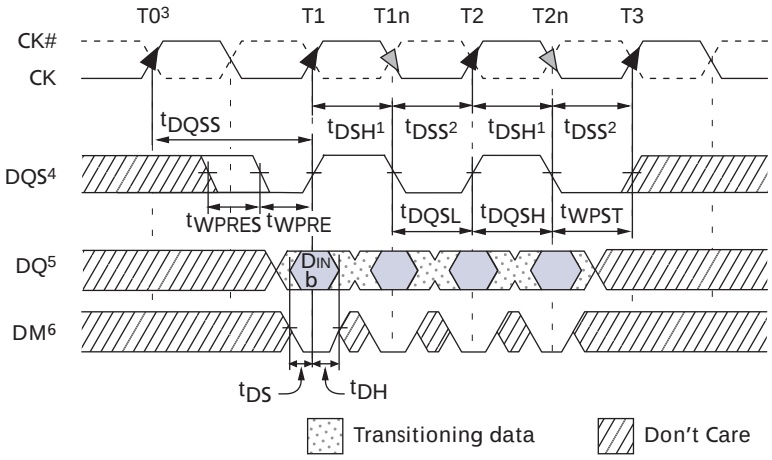
**Figure 39: Data Output Timing – $^{t}$AC and $^{t}$DQSCK**




Notes:
1. DQ transitioning after DQS transition define $^{t}$DQSQ window.
2. All DQ must transition by $^{t}$DQSQ after DQS transitions, regardless of $^{t}$AC.
3. $^{t}$AC is the DQ output window relative to CK and is the long-term component of DQ skew.
4. Shown with CL = 3.

**Figure 40: Data Input Timing**




Notes:
1. $^{t}$DSH (MIN) generally occurs during $^{t}$DQSS (MIN).
2. $^{t}$DSS (MIN) generally occurs during $^{t}$DQSS (MAX).
3. WRITE command issued at T0.
4. For x16, LDQS controls the lower byte, and UDQS controls the upper byte. For x32, DQS0 controls DQ[7:0], DQS1 controls DQ[15:8], DQS2 controls DQ[23:16], and DQS3 controls DQ[31:24].
5. For x16, LDM controls the lower byte, and UDM controls the upper byte. For x32, DM0 controls DQ[7:0], DM1 controls DQ[15:8]5, DM2 controls DQ[23:16], and DM3 controls DQ[31:24].


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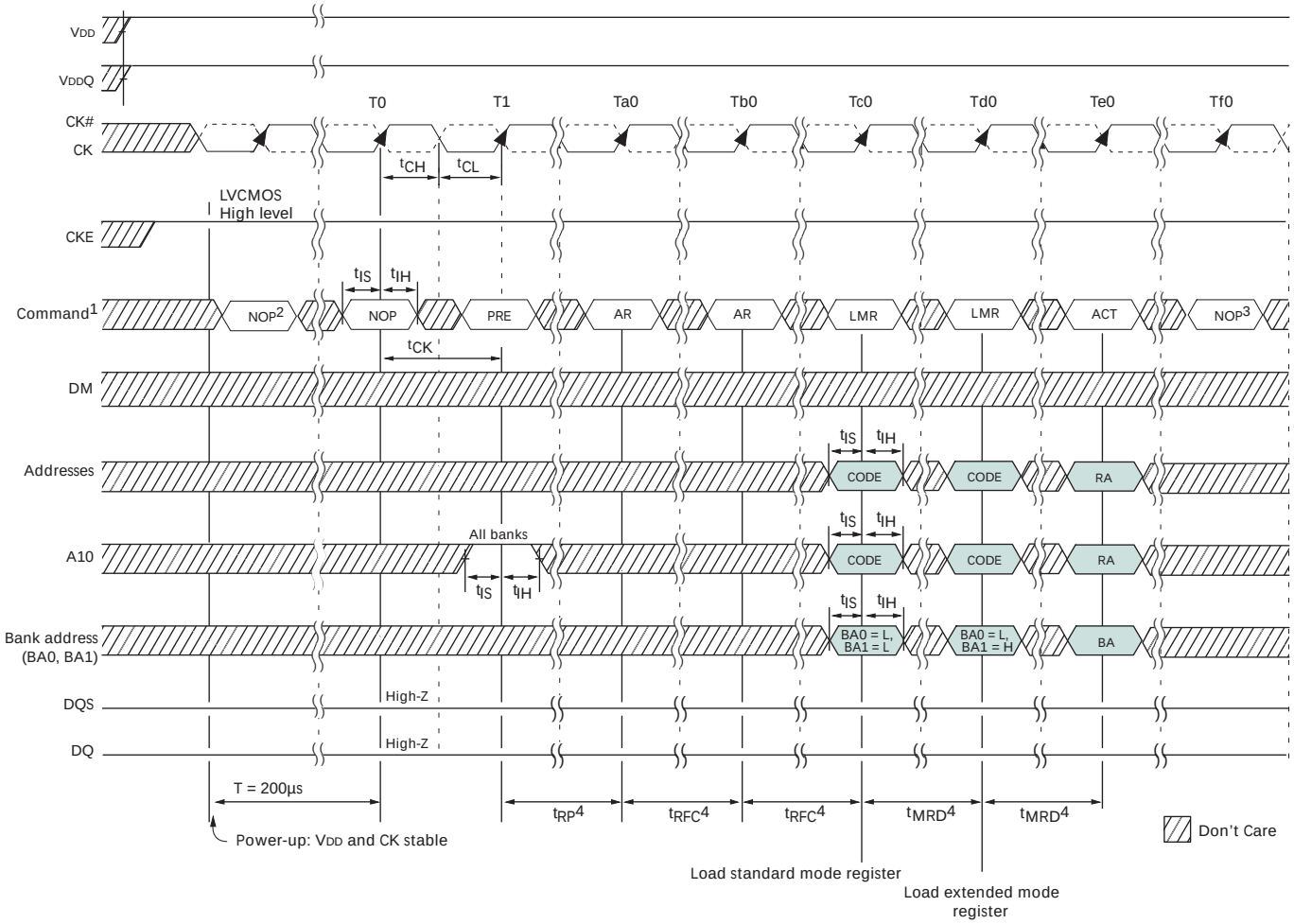
**Figure 41: Initialize and Load Mode Registers**




Notes:
1. PRE = PRECHARGE command; LMR = LOAD MODE REGISTER command; AR = AUTO REFRESH command; ACT = ACTIVE command; RA = row address; BA = bank address.
2. NOP or DESELECT commands are required for at least 200µs.
3. Other valid commands are possible.
4. NOP or DESELECT commands are required during this time.


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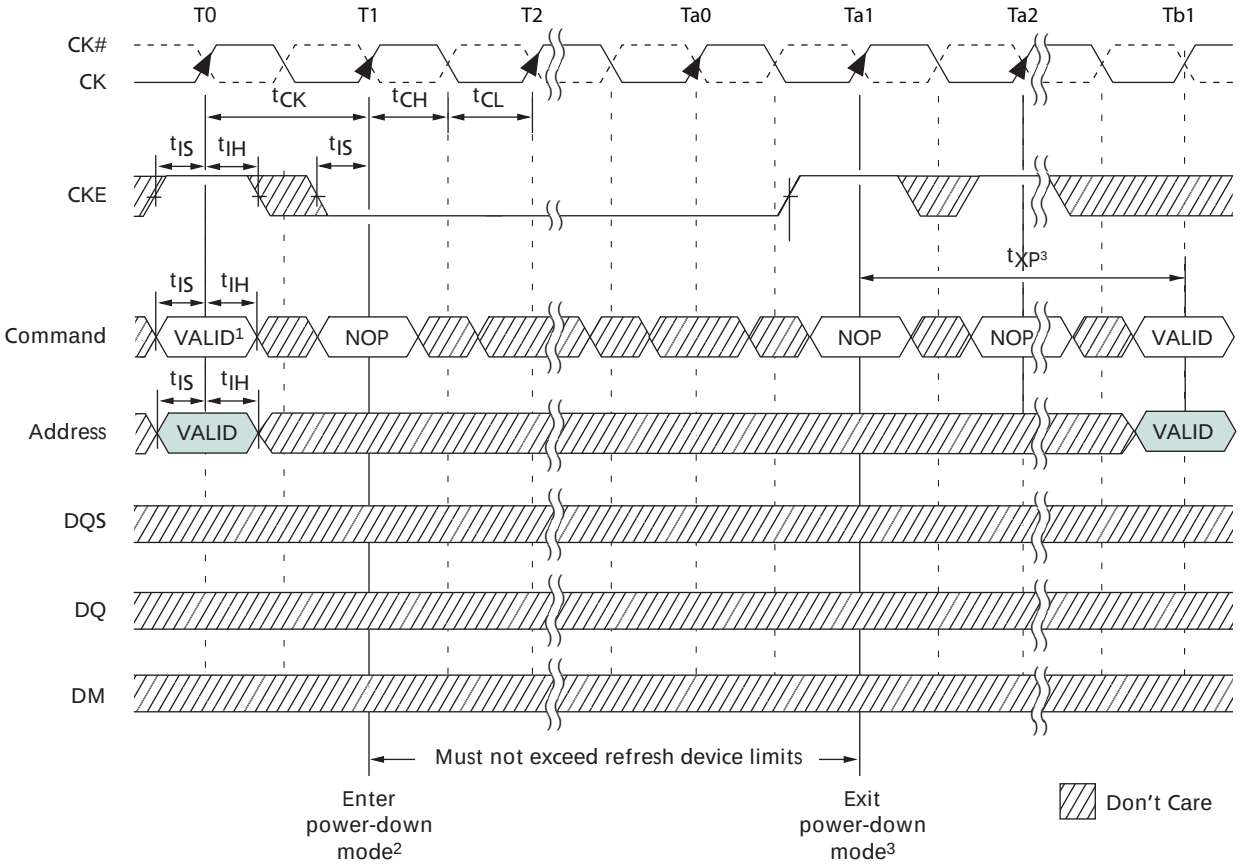
**Figure 42: Power-Down Mode (Active or Precharge)**




Notes:
1. If this command is a PRECHARGE (or if the device is already in the idle state), then the power-down mode shown is precharge power-down. If this command is an ACTIVE (or if at least one row is already active), then the power-down mode shown is active power-down.
2. No column accesses are allowed to be in progress at the time power-down is entered.
3. There must be at least one clock pulse during $^{t}$XP time.


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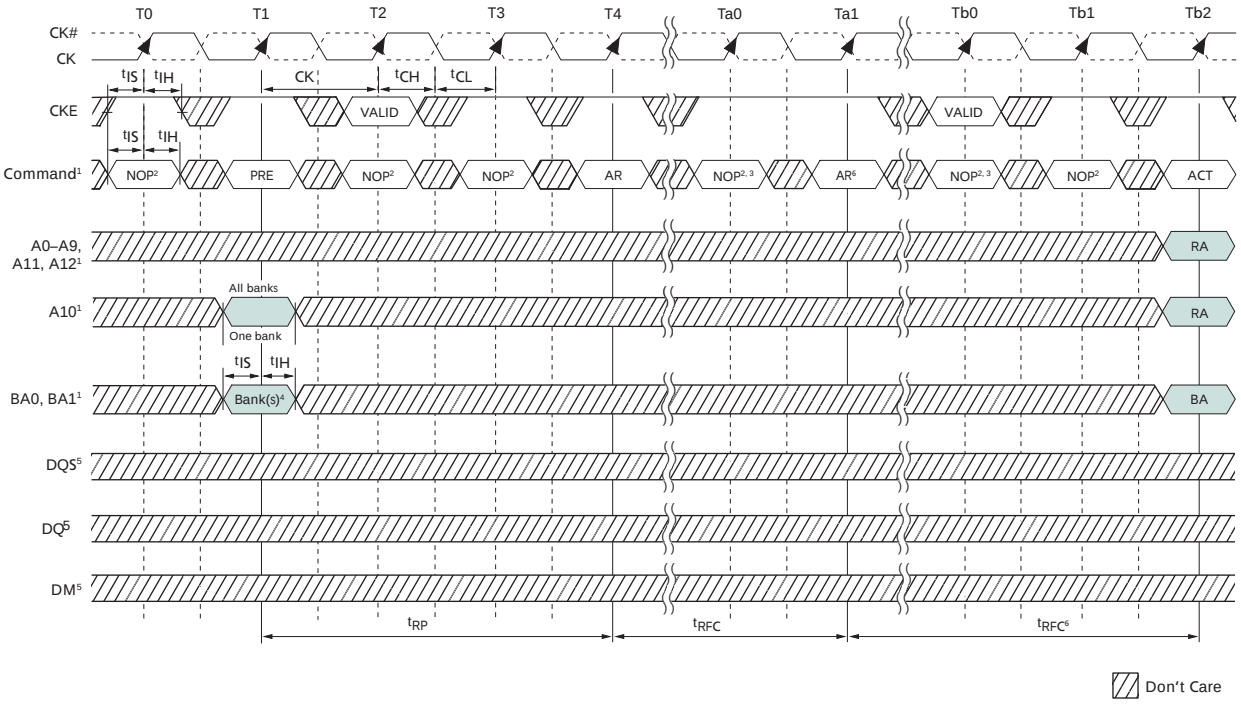
**Figure 43: Auto Refresh Mode**




Notes:
1. PRE = PRECHARGE; ACT = ACTIVE; AR = AUTO REFRESH; RA = row address; BA = bank address.
2. NOP commands are shown for ease of illustration; other valid commands may be possible at these times. CKE must be active during clock positive transitions.
3. NOP or COMMAND INHIBIT are the only commands allowed until after $^{t}$RFC time; CKE must be active during clock positive transitions.
4. "Don't Care" if A10 is HIGH at this point; A10 must be HIGH if more than one bank is active (for example, must precharge all active banks).
5. DM, DQ, and DQS signals are all "Don't Care"/High-Z for operations shown.
6. The second AUTO REFRESH is not required and is only shown as an example of two back-to-back AUTO REFRESH commands.


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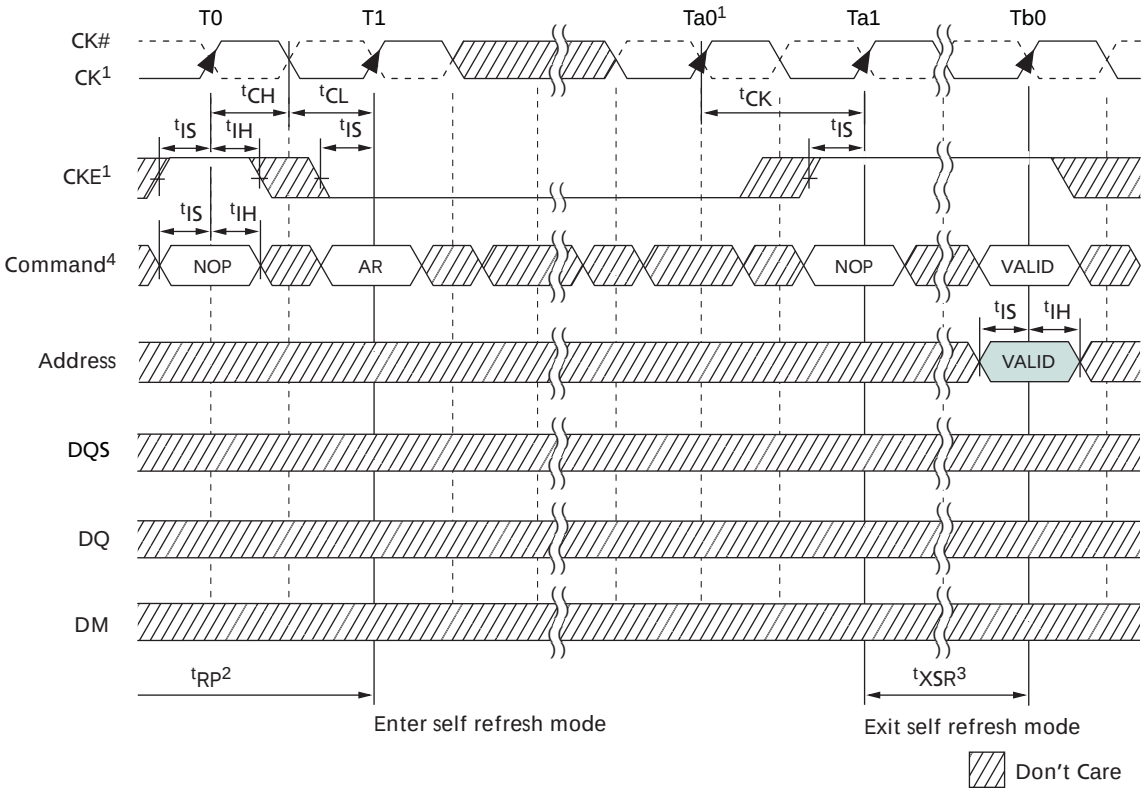
**Figure 44: Self Refresh Mode**




Notes:
1. Clock must be stable, cycling within specifications by Ta0, before exiting self refresh mode.
2. Device must be in the all banks idle state prior to entering self refresh mode.
3. NOPs or DESELECT is required for $^{t}$XSR time with at least two clock pulses.
4. AR = AUTO REFRESH command.
5. CKE must remain LOW to remain in self refresh mode.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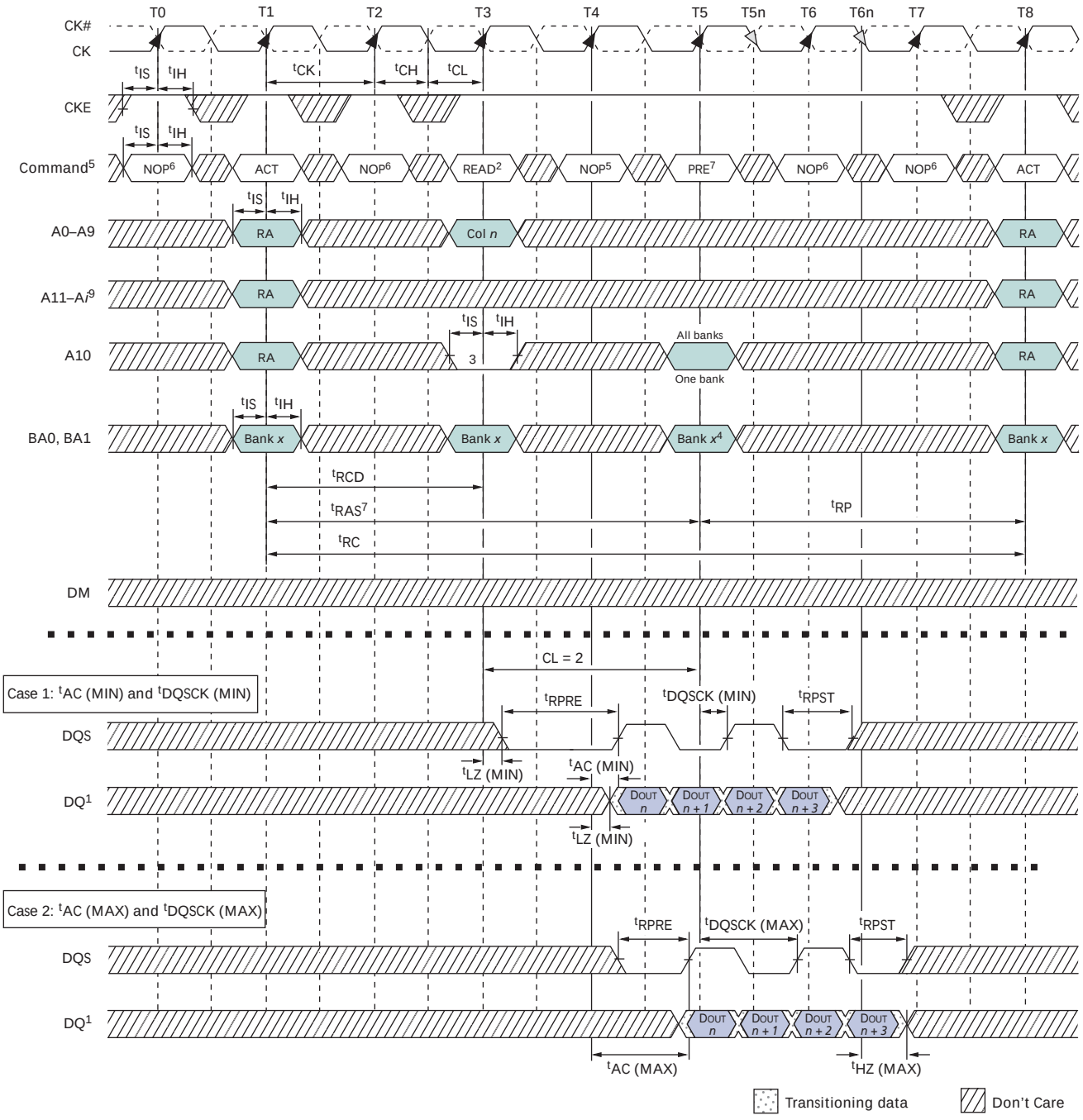
## Figure 45: Bank Read – Without Auto Precharge




Notes:
1. DOUT *n* = data-out from column *n*.
2. BL = 4 in the case shown.
3. Disable auto precharge.
4. "Don't Care" if A10 is HIGH at T5.
5. PRE = PRECHARGE, ACT = ACTIVE, RA = row address, and BA = bank address.
6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
7. The PRECHARGE command can only be applied at T5 if $^{t}$RAS minimum is met.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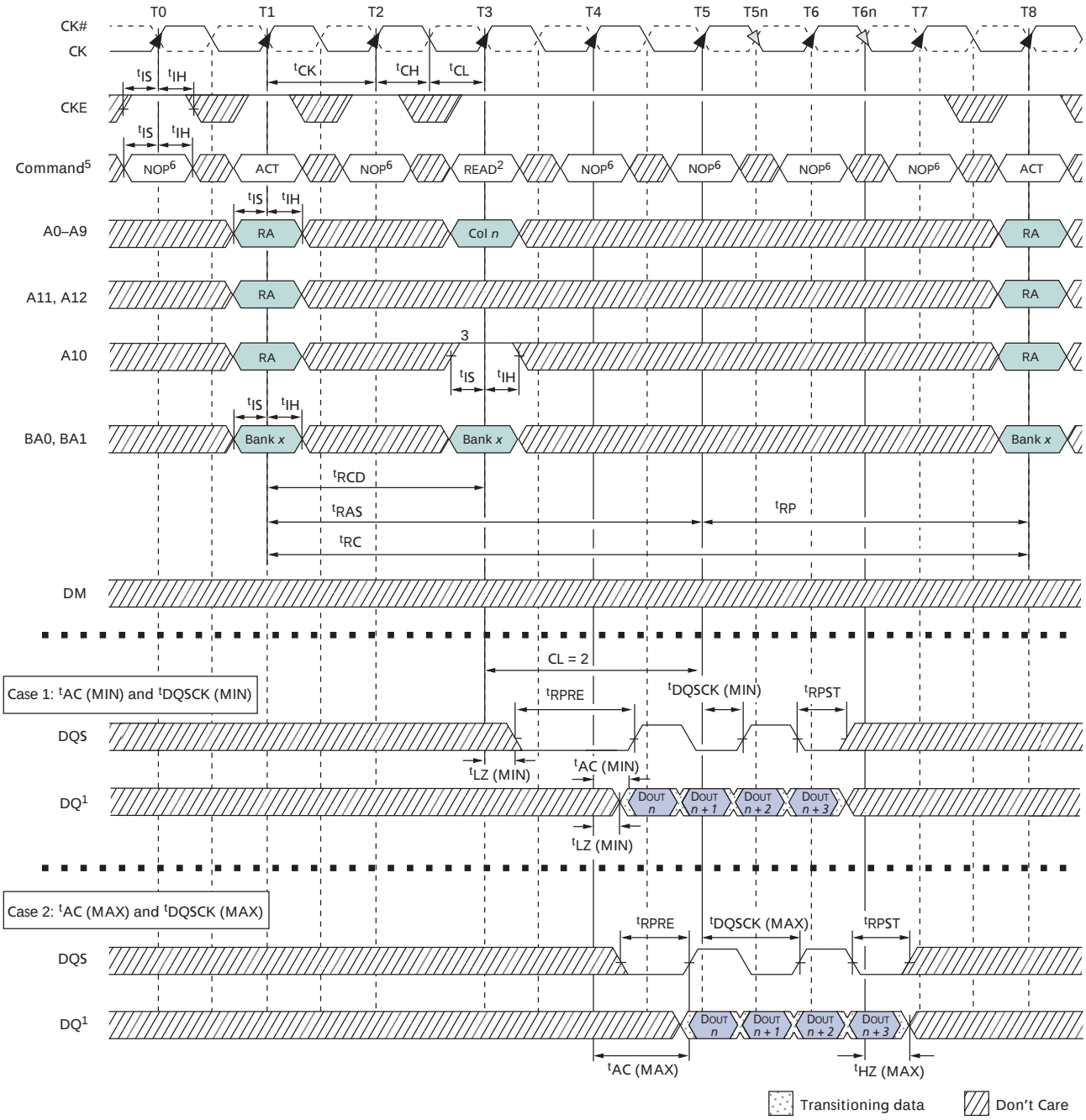
8. Refer to Figures 37 and 38 on pages 66–67 for DQS and DQ timing details.

**Figure 46: Bank Read – with Auto Precharge**




Notes:
1. DOUT *n* = data-out from column *n*.
2. BL = 4 in the case shown.
3. Enable auto precharge.
4. "Don't Care" if A10 is HIGH at T5.
5. PRE = PRECHARGE; ACT = ACTIVE; RA = row address; BA = bank address.
6. NOP commands are shown for ease of illustration; other commands may be valid at these times.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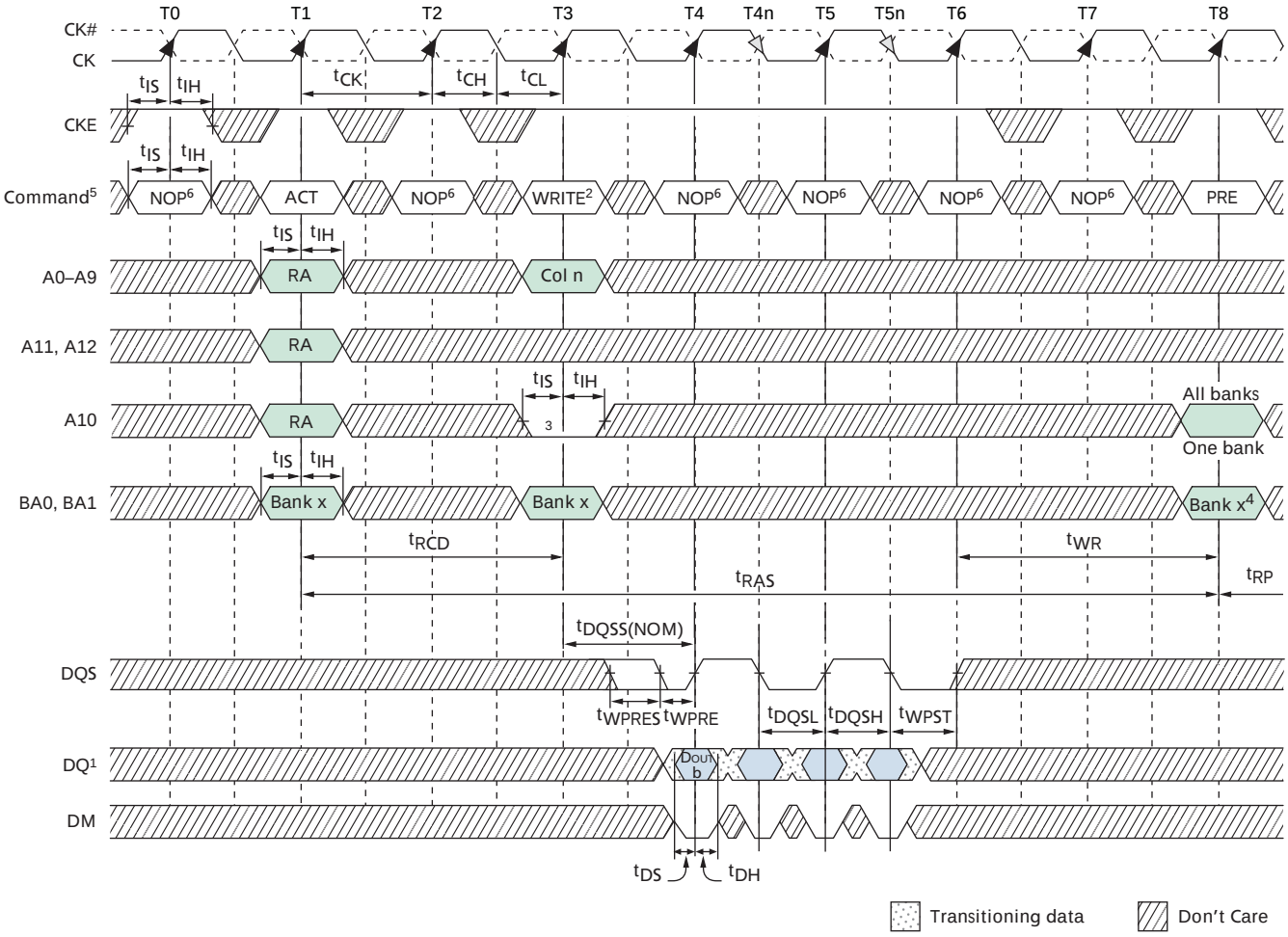
7. Refer to Figures 37 and 38 on pages 66–67 for DQS and DQ timing details.

**Figure 47: Bank Write – Without Auto Precharge**




Notes:
1. DIN *n* = data-in from column *n*; subsequent elements are provided in the programmed order.
2. BL = 4 in the case shown.
3. Disable auto precharge.
4. "Don't Care" if A10 is HIGH at T5.
5. PRE = PRECHARGE; ACT = ACTIVE; RA = row address; BA = bank address.
6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
7. $^{t}$DSH is applicable during $^{t}$DQSS (MIN) and is referenced from CK T4 or T5.
8. $^{t}$DSS is applicable during $^{t}$DQSS (MIN) and is referenced from CK T5 or T6.


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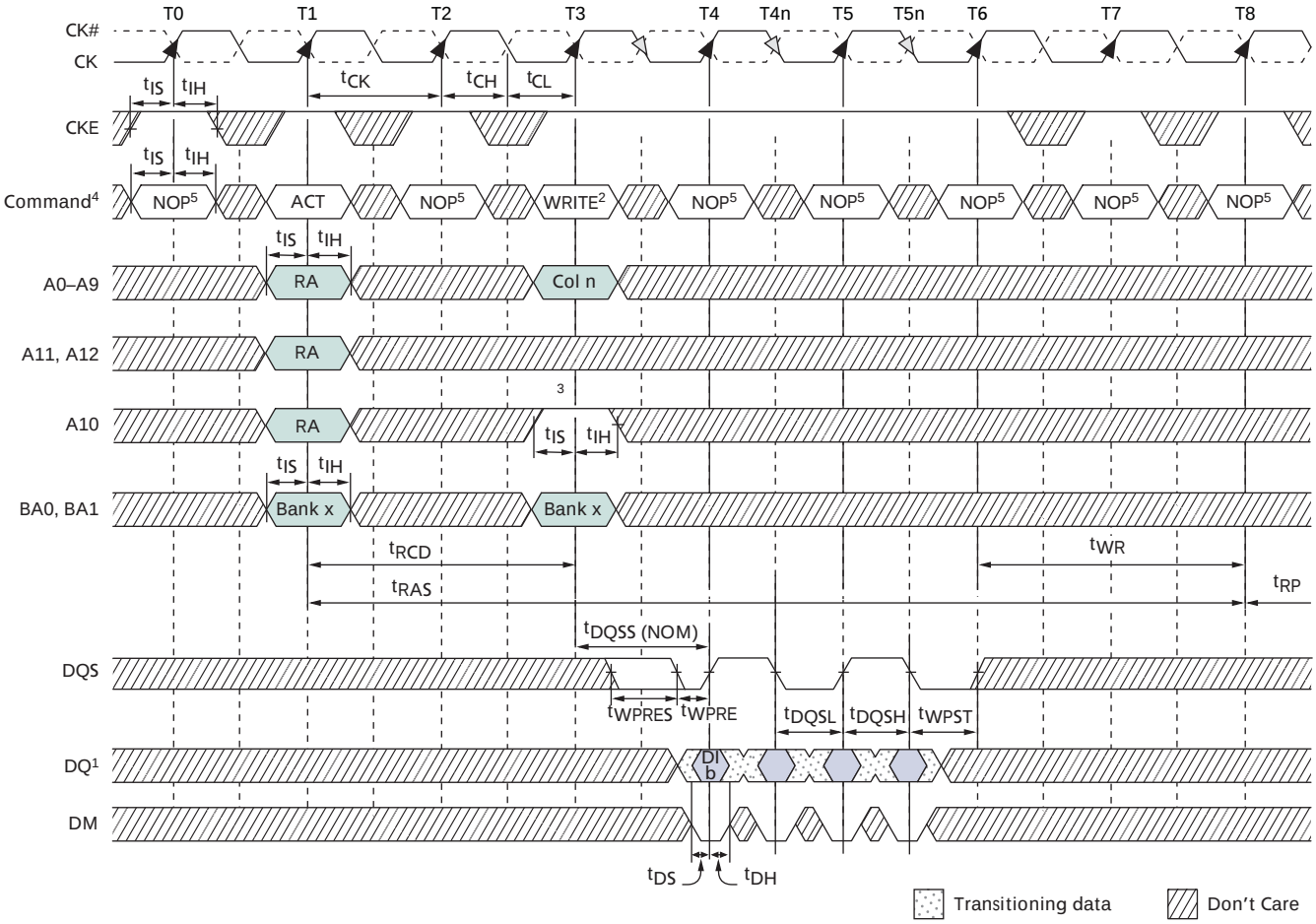
**Figure 48: Bank Write – with Auto Precharge**




Notes:
1. DIN *n* = data-in from column *n*; subsequent elements are provided in the programmed order.
2. BL = 4 in the case shown.
3. A10 = HIGH, enable auto precharge.
4. ACT = ACTIVE; RA = row address; BA = bank address.
5. NOP commands are shown for ease of illustration; other commands may be valid at these times.
6. $^{t}$DSH is applicable during $^{t}$DQSS (MIN) and is referenced from CK T4 or T5.
7. $^{t}$DSS is applicable during $^{t}$DQSS (MIN) and is referenced from CK T5 or T6.


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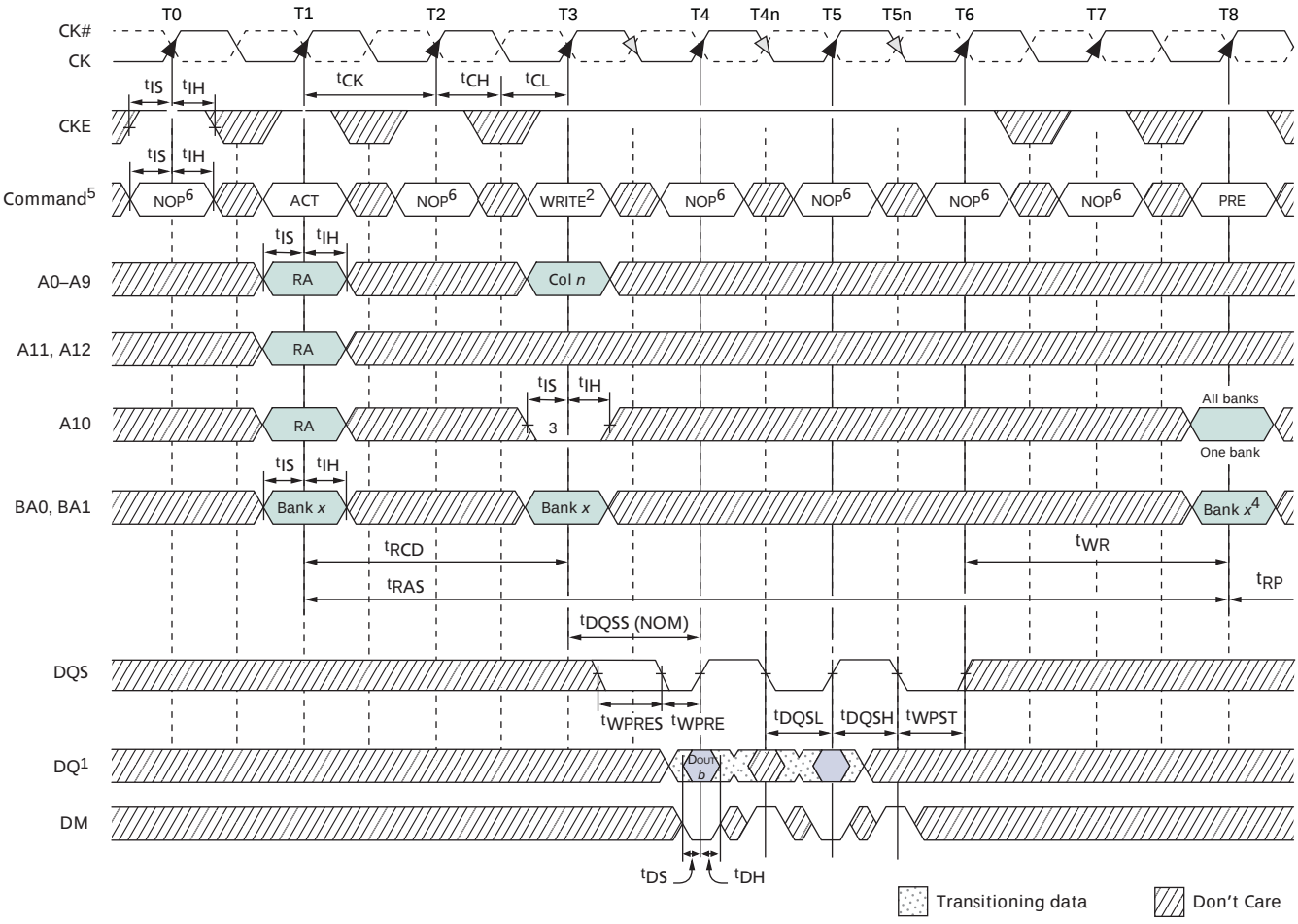
**Figure 49: Write – DM Operation**




Notes:
1. DIN *n* = data-in from column *n*; subsequent elements are provided in the programmed order.
2. BL = 4 in the case shown.
3. Disable auto precharge.
4. "Don't Care" if A10 is HIGH at T5.
5. PRE = PRECHARGE; ACT = ACTIVE; RA = row address; BA = bank address.
6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
7. $^{t}$DSH is applicable during $^{t}$DQSS (MIN) and is referenced from CK T4 or T5.
8. $^{t}$DSS is applicable during $^{t}$DQSS (MIN) and is referenced from CK T5 or T6.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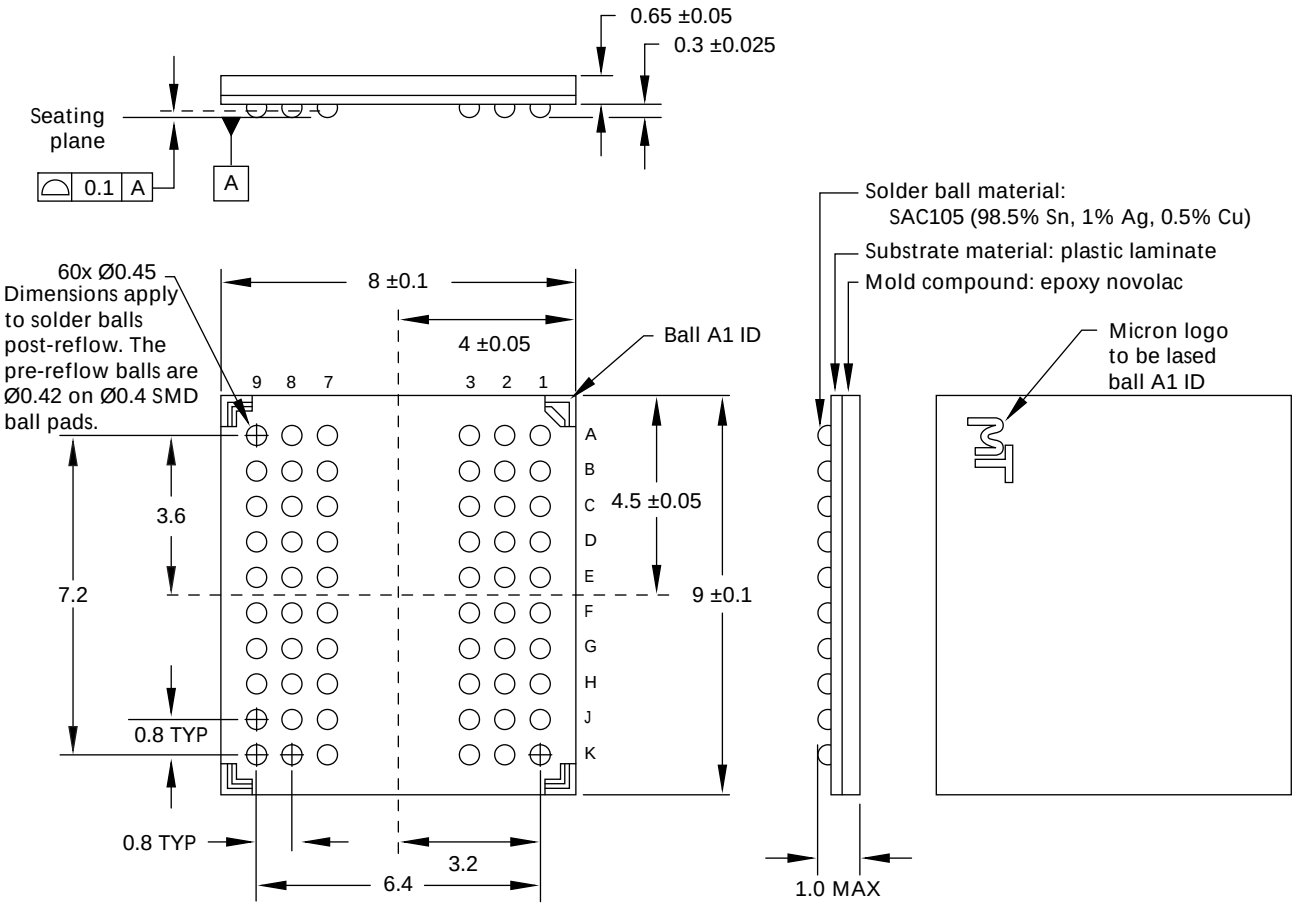
# Package Dimensions

**Figure 50: 60-Ball VFBGA Package**




Note: All dimensions are in millimeters.


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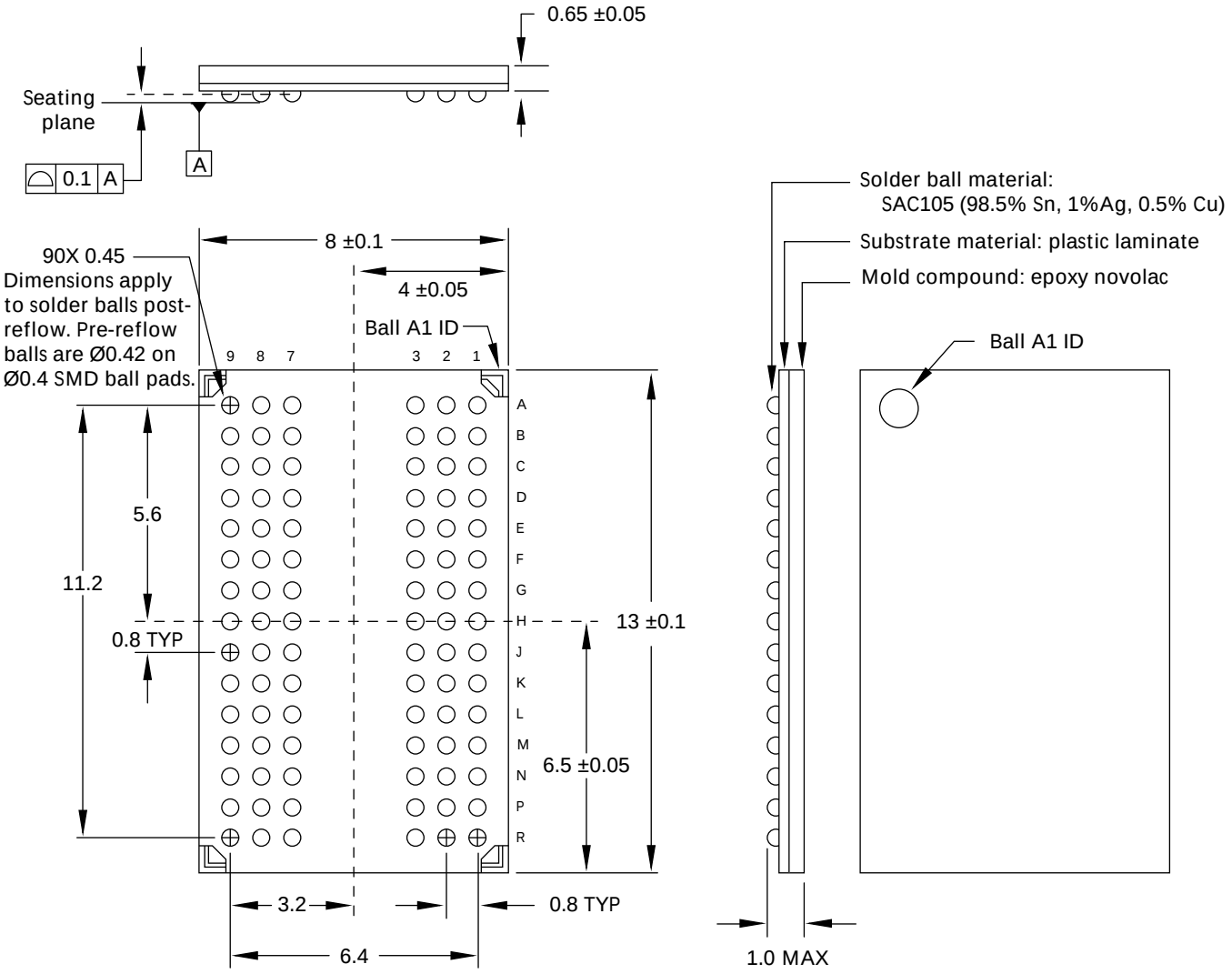
**Figure 51: 90-Ball VFBGA Package**




Note: All dimensions are in millimeters.

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.


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