



THE DATASHEET OF MSP430FE423IPM



MSP430FE42x Mixed-Signal Microcontrollers

1 Device Overview

1.1 Features

- Low Supply Voltage Range: 2.7 V to 3.6 V
- Ultra-Low Power Consumption:
 - Active Mode: 400 μ A at 1 MHz, 3 V
 - Standby Mode: 1.6 μ A
 - Off Mode (RAM Retention): 0.1 μ A
- Five Power-Saving Modes
- Wake up From Standby Mode in Less Than 6 μ s
- Frequency-Locked Loop, FLL+
- 16-Bit RISC Architecture, 125-ns Instruction Cycle Time
- Embedded Signal Processing for Single-Phase Energy Metering With Integrated Analog Front End and Temperature Sensor (ESP430CE1)
- 16-Bit Timer_A With Three Capture/Compare Registers
- Integrated LCD Driver for 128 Segments
- Serial Communication Interface (USART), Asynchronous UART or Synchronous SPI Selectable by Software
- Brownout Detector
- Supply Voltage Supervisor and Monitor With Programmable Level Detection
- Serial Onboard Programming, No External Programming Voltage Needed, Programmable Code Protection by Security Fuse
- Bootloader (BSL)
- Family Members Include:
 - MSP430FE423
8KB + 256 B of Flash Memory, 256 B of RAM
 - MSP430FE425
16KB + 256 B of Flash Memory, 512 B of RAM
 - MSP430FE427
32KB + 256 B of Flash Memory, 1KB of RAM
- Available in 64-Pin Quad Flat Pack (LQFP)
- For Complete Module Descriptions, See the [MSP430x4xx Family User's Guide](#)

1.2 Applications

- 2-Wire and 3-Wire Single-Phase Meters
- Tamper-Resistant Meters

1.3 Description

The TI MSP430™ family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows the device to wake up from low-power modes to active mode in less than 6 μ s.

The MSP430FE42x series are microcontroller configurations with three independent 16-bit sigma-delta ADCs and an embedded signal processor core used to measure and calculate single-phase energy in both 2-wire and 3-wire configurations. Also included are a built-in 16-bit timer, 128-segment LCD drive capability, and 14 I/O pins.

Typical applications include 2-wire and 3-wire single-phase metering including tamper-resistant meter implementations.



Device Information⁽¹⁾

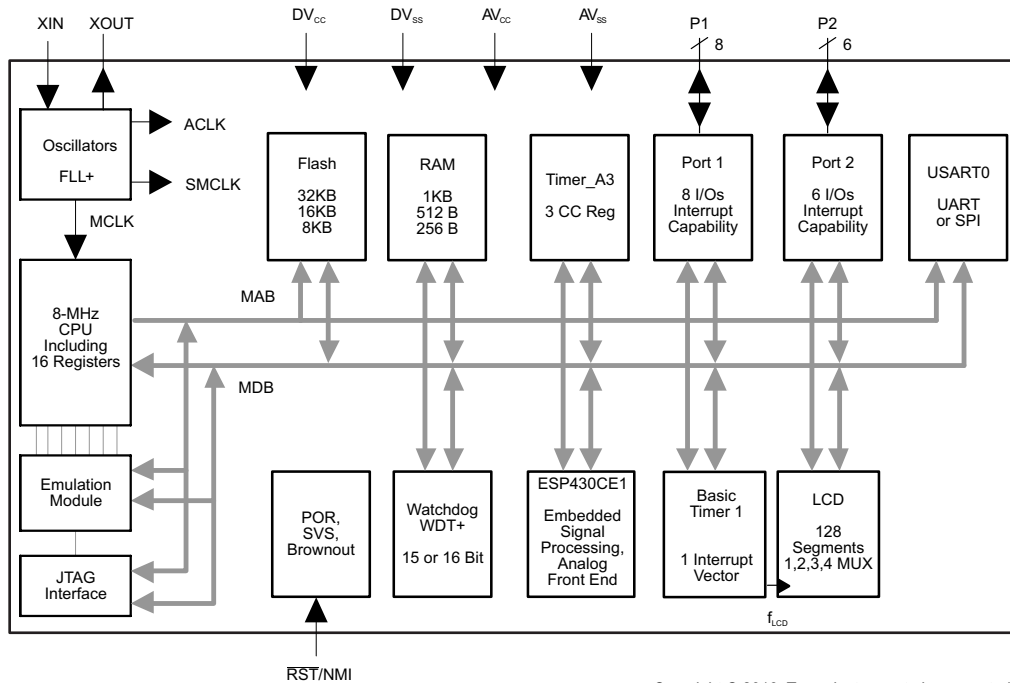
| PART NUMBER | PACKAGE | BODY SIZE ⁽²⁾ |
|----------------|-----------|--------------------------|
| MSP430FE427IPM | LQFP (64) | 10 mm x 10 mm |
| MSP430FE425IPM | LQFP (64) | 10 mm x 10 mm |
| MSP430FE423IPM | LQFP (64) | 10 mm x 10 mm |

(1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in [Section 8](#), or see the TI website at www.ti.com.

(2) The sizes shown here are approximations. For the package dimensions with tolerances, see the *Mechanical Data* in [Section 8](#).

1.4 Functional Block Diagram

Figure 1-1 shows the functional block diagram.



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Figure 1-1. MSP430FE42x Block Diagram

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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from October 16, 2008 to November 14, 2016 | | Page |
|--|--|-----------|
| • Format and organization changes throughout document, including addition of section numbering | | <u>1</u> |
| • Added Section 3 | | <u>5</u> |
| • Added Section 5 and moved all electrical and timing specifications to it | | <u>10</u> |
| • Added Section 5.2 , <i>ESD Ratings</i> | | <u>10</u> |
| • Changed the MAX value of the $I_{(LPM3)}$ parameter at 85°C from 2.6 to 3.5 μA in Section 5.4 , <i>Supply Current Into AV_{CC} and DV_{CC} Excluding External Current</i> | | <u>11</u> |
| • Added Section 5.5 , <i>Thermal Resistance Characteristics, PM Package (LQFP-64)</i> | | <u>12</u> |
| • Changed all cases of "bootstrap loader" to "bootloader" | | <u>38</u> |
| • Changed the value of the $\overline{\text{Port}}/\text{LCD}$ column in Table 6-14 , <i>Port P1 (P1.2 to P1.7) Pin Functions</i> | | <u>46</u> |
| • Changed the value of the $\overline{\text{Port}}/\text{LCD}$ column in Table 6-15 , <i>Port P2 (P2.0 and P2.1) Pin Functions</i> | | <u>47</u> |
| • Added Section 7 , <i>Device and Documentation Support</i> | | <u>52</u> |
| • Added Section 8 , <i>Mechanical, Packaging, and Orderable Information</i> | | <u>58</u> |

3 Device Comparison

Table 3-1 summarizes the available family members.

Table 3-1. Device Comparison⁽¹⁾⁽²⁾

| DEVICE | FLASH (KB) | RAM (B) | FREQUENCY (MHz) | BSL | ESP430 | I/O | PACKAGE |
|------------|------------|---------|-----------------|------|--------|-----|---------|
| MSP430F427 | 32 | 1K | 8 | UART | 1 | 14 | PM 64 |
| MSP430F425 | 16 | 512 | 8 | UART | 1 | 14 | PM 64 |
| MSP430F423 | 8 | 256 | 8 | UART | 1 | 14 | PM 64 |

(1) For the most current package and ordering information, see the *Package Option Addendum* in [Section 8](#), or see the TI website at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

TI Microcontrollers Product Selection TI's low-power and-high performance MCUs, with wired and wireless connectivity options, are optimized for a broad range of applications.

Products for MSP430 Ultra-Low-Power Microcontrollers One platform. One ecosystem. Endless possibilities. Enabling the connected world with innovations in ultra-low-power microcontrollers with advanced peripherals for precise sensing and measurement.

Products for MSP430F2x/4x Ultra-Low-Power Microcontrollers MSP430F2x/4x microcontrollers (MCUs) from the MSP ultra-low-power MCU series are general-purpose 16-bit microcontrollers used for a wide range of applications including consumer electronics, data logging applications, portable medical instruments, and low-power metering. MSP430F4x MCUs feature an integrated LCD controller, while select MSP430F2x devices feature extended temperature ranges.

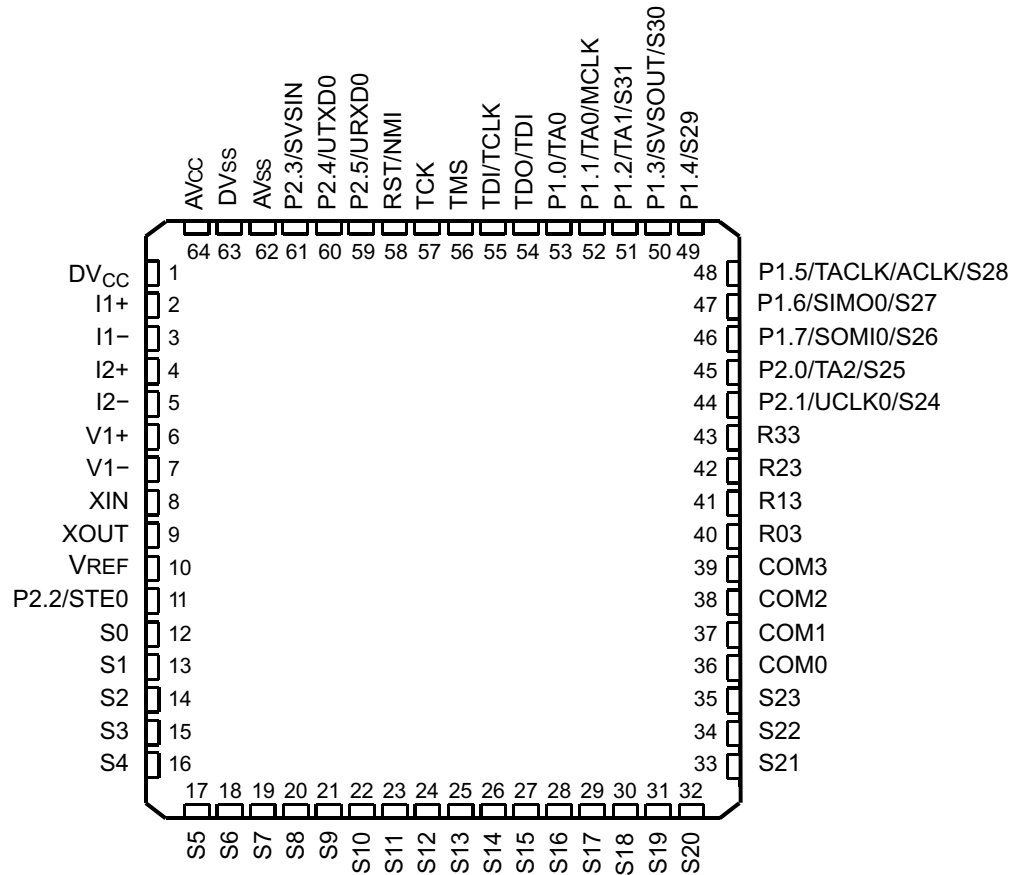
Companion Products for MSP430FE427 Review products that are frequently purchased or used with this product.

Reference Designs The TI Designs Reference Design Library is a robust reference design library that spans analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market.

4 Terminal Configuration and Functions

4.1 Pin Diagram

Figure 4-1 shows the pinout for the 64-pin PM package.



NOTE: TI recommends leaving all unused analog inputs open.

Figure 4-1. 64-Pin PM Package (Top View)

4.2 Signal Descriptions

Table 4-1 describes the signals for all device variants

Table 4-1. Terminal Functions

| SIGNAL NAME | PIN NO. | I/O | DESCRIPTION |
|------------------|---------|-----|---|
| DVCC | 1 | | Digital supply voltage, positive terminal |
| I1+ | 2 | I | Current 1 positive analog input, internal connection to SD16 channel 0 A0+ ⁽¹⁾ |
| I1- | 3 | I | Current 1 negative analog input, internal connection to SD16 channel 0 A0- ⁽¹⁾ |
| I2+ | 4 | I | Current 2 positive analog input, internal connection to SD16 channel 1 A0+ ⁽¹⁾ |
| I2- | 5 | I | Current 2 negative analog input, internal connection to SD16 channel 1 A0- ⁽¹⁾ |
| V1+ | 6 | I | Voltage 1 positive analog input, internal connection to SD16 channel 2 A0+ ⁽¹⁾ |
| V1- | 7 | I | Voltage 1 negative analog input, internal connection to SD16 channel 2 A0- ⁽¹⁾ |
| XIN | 8 | I | Input port for crystal oscillator XT1. Standard or watch crystals can be connected. |
| XOUT | 9 | O | Output terminal of crystal oscillator XT1 |
| V _{REF} | 10 | I/O | Input for an external reference voltage, internal reference voltage output (can be used as mid-voltage) |
| P2.2/STE0 | 11 | I/O | General-purpose digital I/O Slave transmit enable for USART0 in SPI mode |
| S0 | 12 | O | LCD segment output 0 |
| S1 | 13 | O | LCD segment output 1 |
| S2 | 14 | O | LCD segment output 2 |
| S3 | 15 | O | LCD segment output 3 |
| S4 | 16 | O | LCD segment output 4 |
| S5 | 17 | O | LCD segment output 5 |
| S6 | 18 | O | LCD segment output 6 |
| S7 | 19 | O | LCD segment output 7 |
| S8 | 20 | O | LCD segment output 8 |
| S9 | 21 | O | LCD segment output 9 |
| S10 | 22 | O | LCD segment output 10 |
| S11 | 23 | O | LCD segment output 11 |
| S12 | 24 | O | LCD segment output 12 |
| S13 | 25 | O | LCD segment output 13 |
| S14 | 26 | O | LCD segment output 14 |
| S15 | 27 | O | LCD segment output 15 |
| S16 | 28 | O | LCD segment output 16 |
| S17 | 29 | O | LCD segment output 17 |
| S18 | 30 | O | LCD segment output 18 |
| S19 | 31 | O | LCD segment output 19 |
| S20 | 32 | O | LCD segment output 20 |
| S21 | 33 | O | LCD segment output 21 |
| S22 | 34 | O | LCD segment output 22 |
| S23 | 35 | O | LCD segment output 23 |
| COM0 | 36 | O | Common output, COM0–COM3 are used for LCD backplanes. |
| COM1 | 37 | O | Common output, COM0–COM3 are used for LCD backplanes. |
| COM2 | 38 | O | Common output, COM0–COM3 are used for LCD backplanes. |
| COM3 | 39 | O | Common output, COM0–COM3 are used for LCD backplanes. |
| R03 | 40 | I | Input port of fourth positive (lowest) analog LCD level (V5) |
| R13 | 41 | I | Input port of third most positive analog LCD level (V4 or V3) |
| R23 | 42 | I | Input port of second most positive analog LCD level (V2) |

(1) TI recommends open connection for all unused analog inputs.

Table 4-1. Terminal Functions (continued)

| SIGNAL NAME | PIN NO. | I/O | DESCRIPTION |
|---------------------|---------|-----|--|
| R33 | 43 | O | Output port of most positive analog LCD level (V1) |
| P2.1/UCLK0/S24 | 44 | I/O | General-purpose digital I/O External clock input for USART0 in UART or SPI mode, or clock output for USART0 in SPI mode LCD segment output 24 ⁽²⁾ |
| P2.0/TA2/S25 | 45 | I/O | General-purpose digital I/O Timer_A Capture: CCI2A input, Compare: Out2 output LCD segment output 25 ⁽²⁾ |
| P1.7/SOMI0/S26 | 46 | I/O | General-purpose digital I/O Slave out/master in for USART0 in SPI mode LCD segment output 26 ⁽²⁾ |
| P1.6/SIMO0/S27 | 47 | I/O | General-purpose digital I/O Slave in/master out for USART0 in SPI mode LCD segment output 27 ⁽²⁾ |
| P1.5/TACLK/ACLK/S28 | 48 | I/O | General-purpose digital I/O Timer_A and SD16 clock signal TACLK input ACLK output (divided by 1, 2, 4, or 8) LCD segment output 28 ⁽²⁾ |
| P1.4/S29 | 49 | I/O | General-purpose digital I/O LCD segment output 29 ⁽²⁾ |
| P1.3/SVSOUT/S30 | 50 | I/O | General-purpose digital I/O SVS: output of SVS comparator LCD segment output 30 ⁽²⁾ |
| P1.2/TA1/S31 | 51 | I/O | General-purpose digital I/O Timer_A, Capture: CCI1A, CCI1B input, Compare: Out1 output LCD segment output 31 ⁽²⁾ |
| P1.1/TA0/MCLK | 52 | I/O | General-purpose digital I/O Timer_A, Capture: CCI0B input. Note: TA0 is only an input on this pin. MCLK output BSL receive |
| P1.0/TA0 | 53 | I/O | General-purpose digital I/O Timer_A, Capture: CCI0A input, Compare: Out0 output BSL transmit |
| TDO/TDI | 54 | I/O | Test data output port, TDO/TDI data output or programming data input terminal |
| TDI/TCLK | 55 | I | Test data input or test clock input. The device protection fuse is connected to TDI. |
| TMS | 56 | I | Test mode select. TMS is used as an input port for device programming and test. |
| TCK | 57 | I | Test clock. TCK is the clock input port for device programming and test. |
| RST/NMI | 58 | I | Reset input or nonmaskable interrupt input port |
| P2.5/URXD0 | 59 | I/O | General-purpose digital I/O Receive data in for USART0 in UART mode |
| P2.4/UTXD0 | 60 | I/O | General-purpose digital I/O Transmit data out for USART0 in UART mode |

(2) LCD function selected automatically when applicable LCD module control bits are set, not with PxSEL bits.

Table 4-1. Terminal Functions (continued)

| SIGNAL NAME | PIN NO. | I/O | DESCRIPTION |
|------------------|---------|-----|---|
| P2.3/SVSIN | 61 | I/O | General-purpose digital I/O Analog input to brownout, supply voltage supervisor |
| AV _{SS} | 62 | | Analog supply voltage, negative terminal. Supplies SD16, SVS, brownout, oscillator, and LCD resistive divider circuitry. |
| DV _{SS} | 63 | | Digital supply voltage, negative terminal |
| AV _{CC} | 64 | | Analog supply voltage, positive terminal. Supplies SD16, SVS, brownout, oscillator, and LCD resistive divider circuitry. Do not power up before DVCC. |

5 Specifications

5.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | MIN | MAX | UNIT | |
|---|---------------------|----------------|------|----|
| Voltage applied at V_{CC} to V_{SS} | -0.3 | 4.1 | V | |
| Voltage applied to any pin ⁽²⁾ | -0.3 | $V_{CC} + 0.3$ | V | |
| Diode current at any device terminal | | ± 2 | mA | |
| Storage temperature range, T_{stg} | Unprogrammed device | -55 | 150 | °C |
| | Programmed device | -40 | 85 | |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages referenced to V_{SS} . The JTAG fuse-blow voltage, V_{FB} , is allowed to exceed the absolute maximum rating. The voltage is applied to the TDI/TCLK pin when blowing the JTAG fuse.

5.2 ESD Ratings

| | | VALUE | UNIT |
|-------------------------------------|--|------------|------|
| $V_{(ESD)}$ Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ± 1000 | V |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ± 250 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ± 1000 V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ± 250 V may actually have higher performance.

5.3 Recommended Operating Conditions

Typical values are specified at $V_{CC} = 3.3$ V and $T_A = 25^\circ\text{C}$ (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|--|--|-----|--------|------|------|
| V_{CC} Supply voltage during program execution ⁽¹⁾ ($AV_{CC} = DV_{CC} = V_{CC}$) | ESP430 and SD16 disabled | 1.8 | | 3.6 | V |
| | SVS enabled, PORON = 1 ⁽²⁾ , ESP430 and SD16 disabled | 2.0 | | 3.6 | |
| | ESP430 or SD16 enabled or during programming of flash memory | 2.7 | | 3.6 | |
| V_{SS} Supply voltage ($AV_{SS} = DV_{SS} = V_{SS}$) | | 0 | | 0 | V |
| T_A Operating free-air temperature range | | -40 | | 85 | °C |
| $f_{(LFXT1)}$ LFXT1 crystal frequency ⁽³⁾ | LF selected, XTS_FLL = 0 | | 32.768 | | kHz |
| | XT1 selected, XTS_FLL = 1 | | | 8000 | |
| | XT1 selected, XTS_FLL = 1 | | 1000 | 8000 | |
| $f_{(System)}$ Processor frequency (signal MCLK) ⁽⁴⁾ (also see Figure 5-1) | $V_{CC} = 2.7$ V | | DC | 8.4 | MHz |
| | $V_{CC} = 3.6$ V | | DC | 8.4 | |

- (1) TI recommends powering AV_{CC} and DV_{CC} from the same source. A maximum difference of 0.3 V between AV_{CC} and DV_{CC} can be tolerated during power up and operation.
- (2) The minimum operating supply voltage is defined according to the trip point where POR is going active by decreasing the supply voltage. POR is going inactive when the supply voltage is raised above the minimum supply voltage plus the hysteresis of the SVS circuitry.
- (3) In LF mode, the LFXT1 oscillator requires a watch crystal.
- (4) For frequencies above 8 MHz, MCLK is sourced by the built-in oscillator (DCO and FLL+).

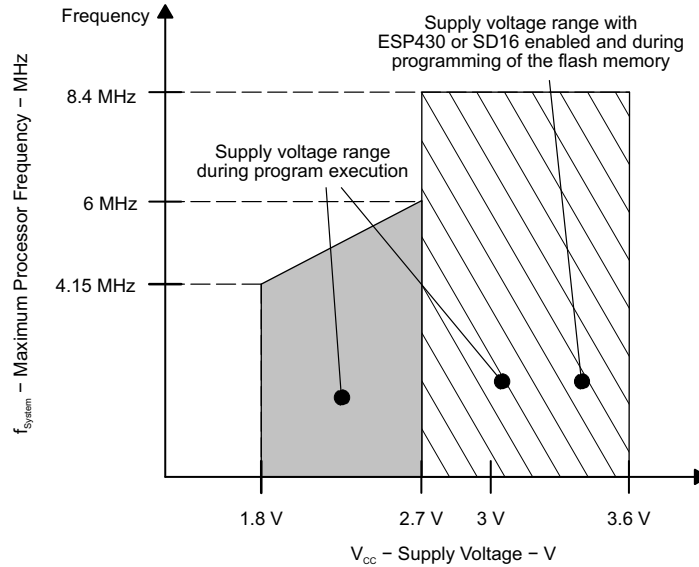


Figure 5-1. Frequency vs Supply Voltage

5.4 Supply Current Into AV_{CC} and DV_{CC} Excluding External Current⁽¹⁾

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | T _A | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------|--|----------------|-----------------|-----|-----|-----|------|
| I _(AM) | Active mode (AM) f _(MCLK) = f _(SMCLK) = f _(DCO) = 1 MHz, f _(ACLK) = 32768 Hz, XTS_FLL = 0, program executes in flash | -40°C to 85°C | 3 V | | 400 | 500 | μA |
| I _(LPM0) | Low-power mode 0 or 1 (LPM0 or LPM1) ⁽²⁾ f _(MCLK) = f _(SMCLK) = f _(DCO) = 1 MHz, f _(ACLK) = 32768 Hz, XTS_FLL = 0, FN_8 = FN_4 = FN_3 = FN_2 = 0 | -40°C to 85°C | 3 V | | 130 | 150 | μA |
| I _(LPM2) | Low-power mode 2 (LPM2) ⁽²⁾ | -40°C to 85°C | 3 V | | 10 | 22 | μA |
| I _(LPM3) | Low-power mode 3 (LPM3) ⁽²⁾ | -40°C | 3 V | | 1.5 | 2.0 | μA |
| | | 25°C | | | 1.6 | 2.1 | |
| | | 60°C | | | 1.7 | 2.2 | |
| | | 85°C | | | 2.0 | 3.5 | |
| I _(LPM4) | Low-power mode 4 (LPM4) ⁽²⁾ | -40°C | 3 V | | 0.1 | 0.5 | μA |
| | | 25°C | | | 0.1 | 0.5 | |
| | | 85°C | | | 0.8 | 2.5 | |

(1) All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current. The current consumption in LPM2, LPM3, and LPM4 are measured with active Basic Timer1 and LCD (ACLK selected). The current consumption of the ESP430CE1 and the SVS module are specified in their respective sections. LPMx currents measured with WDT+ disabled. The currents are characterized with a KDS Daishinku DT-38 (6 pF) crystal.

(2) Current consumption for brownout is included.

Current consumption of active mode versus system frequency:

$$I_{(AM)} = I_{(AM)} [1 \text{ MHz}] \times f_{(\text{System})} [\text{MHz}]$$

Current consumption of active mode versus supply voltage:

$$I_{(AM)} = I_{(AM)} [3 \text{ V}] + 170 \mu\text{A/V} \times (V_{\text{CC}} - 3 \text{ V})$$

5.5 Thermal Resistance Characteristics, PM Package (LQFP64)

| PARAMETER | | VALUE | UNIT |
|---------------------|--|-------|------|
| $R\theta_{JA}$ | Junction-to-ambient thermal resistance, still air ⁽¹⁾ | 55.7 | °C/W |
| $R\theta_{JC(TOP)}$ | Junction-to-case (top) thermal resistance ⁽²⁾ | 16.7 | °C/W |
| $R\theta_{JB}$ | Junction-to-board thermal resistance ⁽³⁾ | 27.1 | °C/W |
| Ψ_{JB} | Junction-to-board thermal characterization parameter | 26.8 | °C/W |
| Ψ_{JT} | Junction-to-top thermal characterization parameter | 0.8 | °C/W |

- (1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

5.6 Schmitt-Trigger Inputs – Ports (P1 and P2), \overline{RST}/NMI , JTAG (TCK, TMS, TDI/TCLK, TDO/TDI)

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | V_{CC} | MIN | MAX | UNIT |
|-----------|--|----------|------|------|------|
| V_{IT+} | Positive-going input threshold voltage | 3 V | 1.5 | 1.98 | V |
| V_{IT-} | Negative-going input threshold voltage | 3 V | 0.9 | 1.3 | V |
| V_{hys} | Input voltage hysteresis ($V_{IT+} - V_{IT-}$) | 3 V | 0.45 | 1 | V |

5.7 Inputs P1.x, P2.x, TAX

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V_{CC} | MIN | MAX | UNIT |
|---------------|---|--|----------|-----|-----|-------|
| $t_{(int)}$ | External interrupt timing | Port P1, P2: P1.x to P2.x, external trigger signal for the interrupt flag ⁽¹⁾ | 3 V | 1.5 | | cycle |
| | | | | 50 | | ns |
| $t_{(cap)}$ | Timer_A capture timing | TAx | 3 V | 50 | | ns |
| $f_{(TAext)}$ | Timer_A clock frequency externally applied to pin | TAxCLK, INCLK $t_{(H)} = t_{(L)}$ | 3 V | | 10 | MHz |
| $f_{(TAint)}$ | Timer_A clock frequency | SMCLK or ACLK signal selected | 3 V | | 10 | MHz |

- (1) The external signal sets the interrupt flag every time the minimum $t_{(int)}$ parameters are met. It may be set even with trigger signals shorter than $t_{(int)}$. Both the cycle and timing specifications must be met to ensure the flag is set. $t_{(int)}$ is measured in MCLK cycles.

5.8 Leakage Current – Ports (P1 and P2)⁽¹⁾

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V_{CC} | MIN | MAX | UNIT |
|-----------------|----------------------------|-------------------------------------|----------|-----|-----|------|
| $I_{lkg(P1.x)}$ | Leakage current, Port P1.x | Port 1: $V_{(P1.x)}$ ⁽²⁾ | 3 V | | ±50 | nA |
| $I_{lkg(P2.x)}$ | Leakage current, Port P2.x | Port 2: $V_{(P2.x)}$ ⁽²⁾ | 3 V | | ±50 | nA |

- (1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.
- (2) The port pin must be selected as input.

5.9 Outputs – Ports (P1 and P2)

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|-----------------|---------------------------|---|-----------------|------------------------|------------------------|------|
| V _{OH} | High-level output voltage | I _{OH(max)} = -1.5 mA ⁽¹⁾ | 3 V | V _{CC} - 0.25 | V _{CC} | V |
| | | I _{OH(max)} = -6 mA ⁽²⁾ | 3 V | V _{CC} - 0.6 | V _{CC} | |
| V _{OL} | Low-level output voltage | I _{OL(max)} = 1.5 mA ⁽¹⁾ | 3 V | V _{SS} | V _{SS} + 0.25 | V |
| | | I _{OL(max)} = 6 mA ⁽²⁾ | 3 V | V _{SS} | V _{SS} + 0.6 | |

- (1) The maximum total current, I_{OH(max)} and I_{OL(max)}, for all outputs combined, should not exceed ±12 mA to satisfy the maximum specified voltage drop.
- (2) The maximum total current, I_{OH(max)} and I_{OL(max)}, for all outputs combined, should not exceed ±48 mA to satisfy the maximum specified voltage drop.

5.10 Output Frequency

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|--|---|-----|----------------|------|
| f _(P_x.y) | Output frequency (1 ≤ x ≤ 2, 0 ≤ y ≤ 7) | C _L = 20 F, I _L = ±1.5 mA, V _{CC} = 3 V | DC | | 12 | MHz |
| f _(ACLK) , f _(MCLK) , f _(SMCLK) | P1.1/TA0/MCLK, P1.5/TACLK/ACLK/S28 | C _L = 20 pF, V _{CC} = 3 V | | | 12 | MHz |
| t _(Xdc) | Duty cycle of output frequency | P1.5/TACLK/ACLK/S28, C _L = 20 pF, V _{CC} = 3 V | f _{ACLK} = f _{LFXT1} = f _{XT1} | 40% | 60% | |
| | | | f _{ACLK} = f _{LFXT1} = f _{LF} | 30% | 70% | |
| | | f _{ACLK} = f _{LFXT1} | 50% | | | |
| | | P1.1/TA0/MCLK, C _L = 20 pF, V _{CC} = 3 V, f _{MCLK} = f _{DCOCLK} | 50% – 15 ns | 50% | 50% + 15 ns | |

5.11 Typical Characteristics – Ports P1 and P2

Figure 5-2 through Figure 5-5 show the typical output currents of Ports P1 and P2. One output loaded at a time.

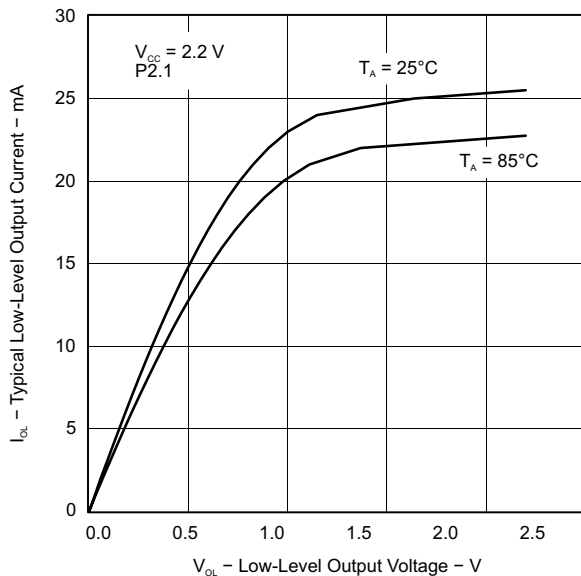


Figure 5-2. Typical Low-Level Output Current vs Low-Level Output Voltage

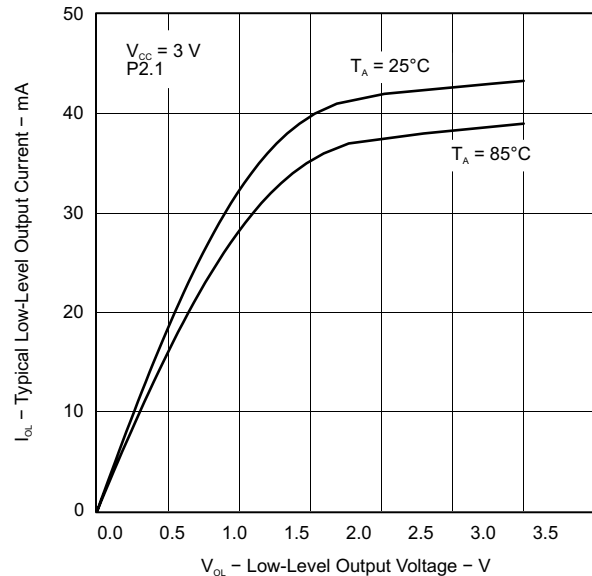


Figure 5-3. Typical Low-Level Output Current vs Low-Level Output Voltage

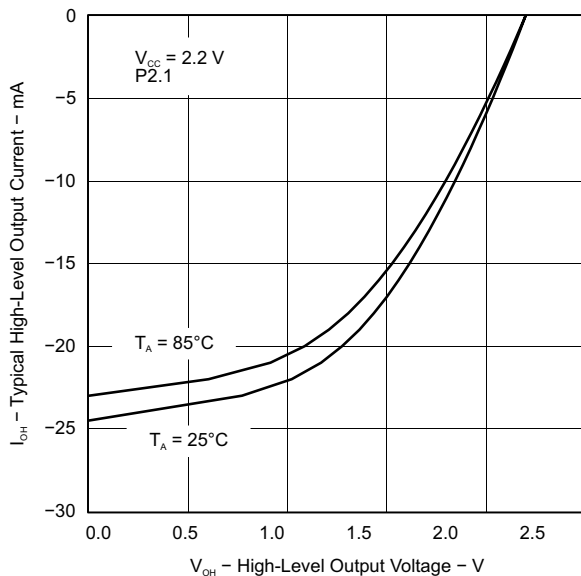


Figure 5-4. Typical High-Level Output Current vs High-Level Output Voltage

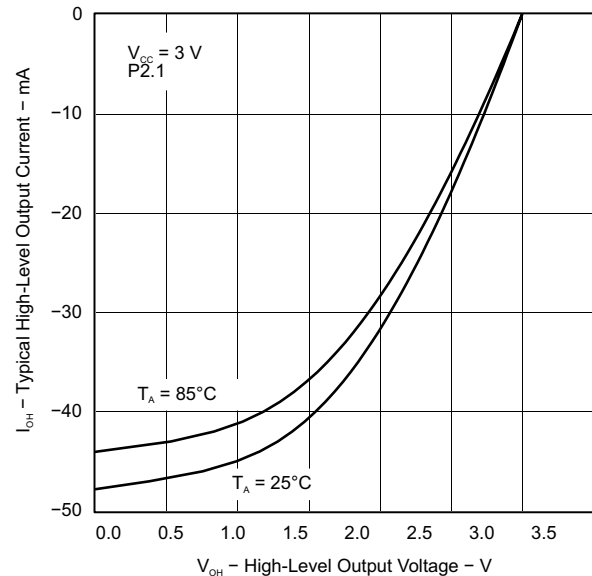


Figure 5-5. Typical High-Level Output Current vs High-Level Output Voltage

5.12 Wake-up Time From LPM3

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | MAX | UNIT |
|---------------|------------|-----------------|-----------------------|-----|-----|---------------|
| $t_{d(LPM3)}$ | Delay time | f = 1 MHz | $V_{CC} = 3\text{ V}$ | | 6 | μs |
| | | f = 2 MHz | | 6 | | |
| | | f = 3 MHz | | 6 | | |

5.13 RAM

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|------------|---------------------------|-----|-----|------|
| V_{RAMh} | CPU halted ⁽¹⁾ | 1.6 | | V |

- (1) This parameter defines the minimum supply voltage when the data in program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.

5.14 LCD

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|-----------------------|----------------------|--|---|---|-----|------------------|------|
| $V_{(33)}$ | Analog voltage | Voltage at R33 | $V_{CC} = 3\text{ V}$ | 2.5 | | $V_{CC} + 0.2$ | V |
| $V_{(23)}$ | | Voltage at R23 | | $\frac{[V_{(33)} - V_{(03)}] \times 2}{3 + V_{(03)}}$ | | | |
| $V_{(13)}$ | | Voltage at R13 | | $\frac{[V_{(33)} - V_{(03)}] \times 1}{3 + V_{(03)}}$ | | | |
| $V_{(33)} - V_{(03)}$ | | Voltage at R33 to R03 | | 2.5 | | $V_{CC} + 0.2$ | |
| $I_{(R03)}$ | Input leakage | $R03 = V_{SS}$ | No load at all segment and common lines, $V_{CC} = 3\text{ V}$ | | | ± 20 | nA |
| $I_{(R13)}$ | | $R13 = V_{CC} / 3$ | | | | ± 20 | |
| $I_{(R23)}$ | | $R23 = 2 \times V_{CC} / 3$ | | | | ± 20 | |
| $V_{(Sxx0)}$ | Segment line voltage | $I_{(Sxx)} = -3\ \mu\text{A}, V_{CC} = 3\text{ V}$ | | $V_{(03)}$ | | $V_{(03)} - 0.1$ | V |
| $V_{(Sxx1)}$ | | | | $V_{(13)}$ | | $V_{(13)} - 0.1$ | |
| $V_{(Sxx2)}$ | | | | $V_{(23)}$ | | $V_{(23)} - 0.1$ | |
| $V_{(Sxx3)}$ | | | | $V_{(33)}$ | | $V_{(33)} + 0.1$ | |

5.15 USART0⁽¹⁾

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|--------------|----------------------|--|-----|-----|------|----|
| $t_{(\tau)}$ | USART0 deglitch time | $V_{CC} = 3\text{ V}, \text{SYNC} = 0, \text{UART mode}$ | 150 | 280 | 500 | ns |

- (1) The signal applied to the USART0 receive signal/terminal (URXD0) should meet the timing requirements of $t_{(\tau)}$ to ensure that the URXS flip-flop is set. The URXS flip-flop is set with negative pulses meeting the minimum-timing condition of $t_{(\tau)}$. The operating conditions to set the flag must be met independently from this timing constraint. The deglitch circuitry is active only on negative transitions on the URXD0 line.

5.16 POR, BOR⁽¹⁾

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------|---|-----|---------------------------|------|---------------|
| $t_{d(BOR)}$ | | | | 2000 | μs |
| $V_{CC(start)}$ | $dV_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 5-6) | | $0.7 \times V_{(B_IT-)}$ | | V |
| $V_{(B_IT-)}$ | $dV_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 5-6 through Figure 5-8) | | 1.71 | | V |
| $V_{hys(B_IT-)}$ | $dV_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 5-6) | 70 | 130 | 180 | mV |
| $t_{(reset)}$ | Pulse duration needed at $\overline{\text{RST/NMI}}$ pin to accept reset internally, $V_{CC} = 3 \text{ V}$ | 2 | | | μs |

- (1) The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B_IT-)} + V_{hys(B_IT-)} \leq 1.8 \text{ V}$.
- (2) During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B_IT-)} + V_{hys(B_IT-)}$. The default FLL+ settings must not be changed until $V_{CC} \geq V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency. See the [MSP430x4xx Family User's Guide](#) for more information on the brownout and SVS circuit.

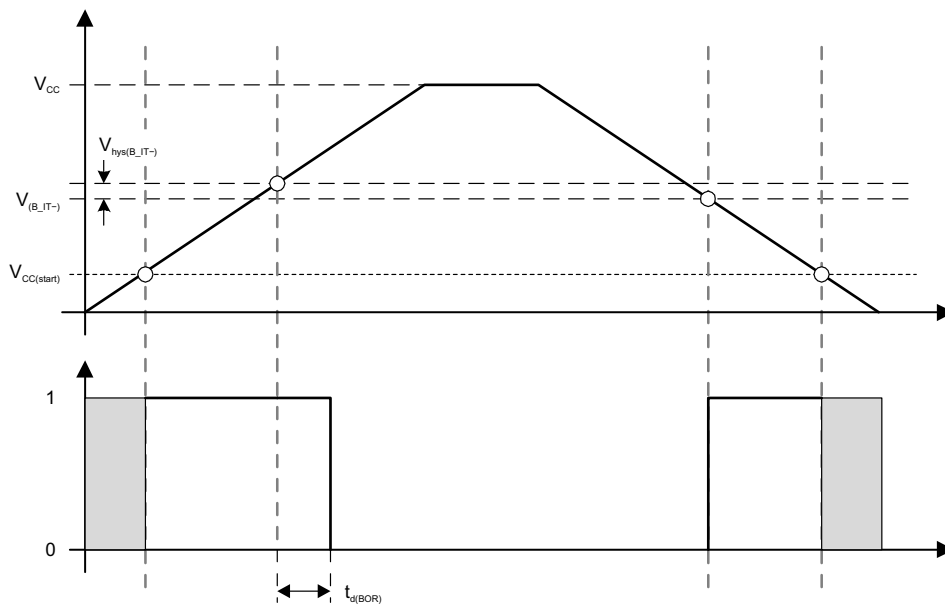


Figure 5-6. POR and BOR vs Supply Voltage

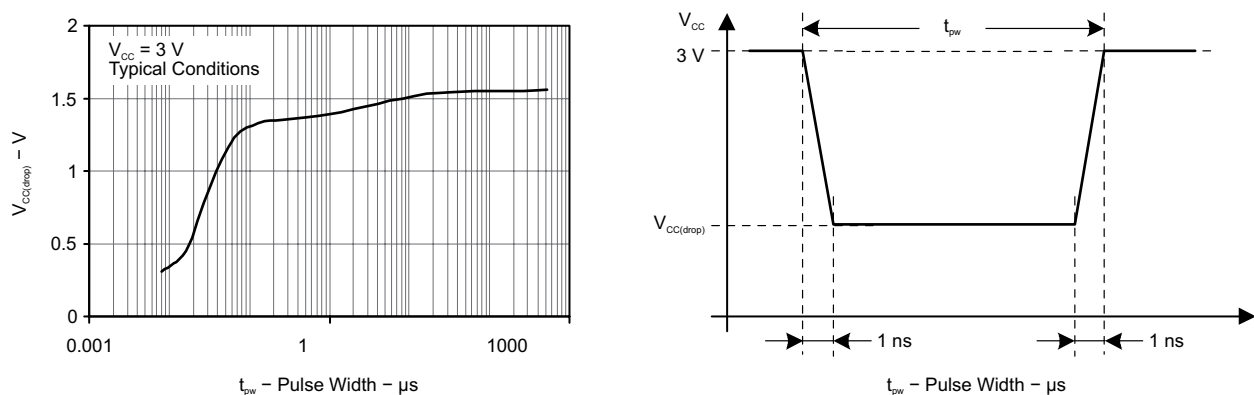


Figure 5-7. $V_{CC(drop)}$ Level With a Rectangular Voltage Drop to Generate a POR/Brownout Signal

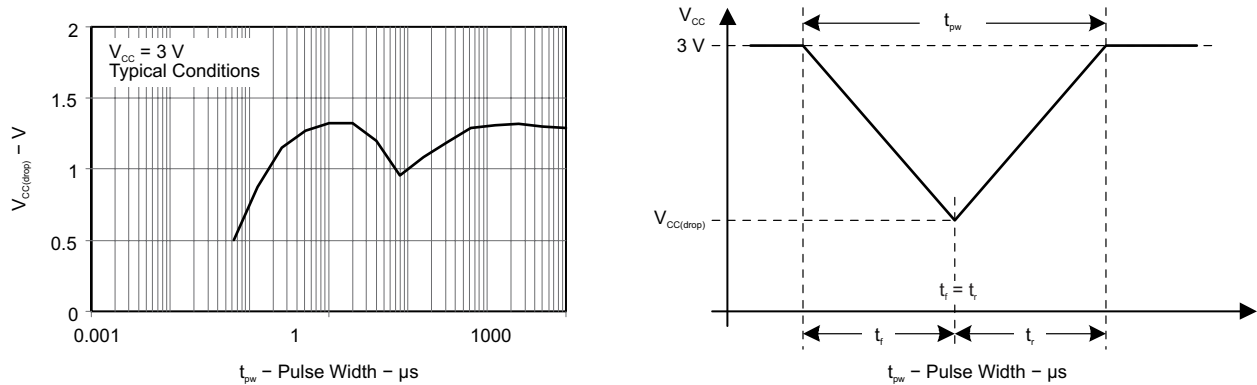


Figure 5-8. $V_{CC(drop)}$ Level With a Triangular Voltage Drop to Generate a POR or BOR Signal

5.17 SVS (Supply Voltage Supervisor and Monitor)⁽¹⁾

over recommended operating free-air temperature range (unless otherwise noted) (also see Figure 5-10)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|------------------------------|---|---------------|-------------------------------|--------------------|-------------------------------|----|
| $t_{(SVSR)}$ | $dV_{CC}/dt > 30 \text{ V/ms}$ (see Figure 5-9) | 5 | | 150 | μs | |
| | $dV_{CC}/dt \leq 30 \text{ V/ms}$ | | | 2000 | | |
| $t_{d(SV\text{Son})}$ | SVS on, switch from VLD = 0 to VLD \neq 0, $V_{CC} = 3 \text{ V}$ | 20 | | 150 | μs | |
| t_{settle} | VLD \neq 0 ⁽²⁾ | | | 12 | μs | |
| $V_{(SV\text{Sstart})}$ | VLD \neq 0, $V_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 5-9) | | 1.55 | 1.7 | V | |
| $V_{\text{hys}(SVS_IT-)}$ | $V_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 5-9) | VLD = 1 | 70 | 120 | 155 | mV |
| | | VLD = 2 to 14 | $V_{(SVS_IT-)} \times 0.004$ | | $V_{(SVS_IT-)} \times 0.008$ | |
| | $V_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 5-9), external voltage applied on P2.3 | VLD = 15 | 4.4 | | 10.4 | mV |
| $V_{(SVS_IT-)}$ | $V_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 5-9) | VLD = 1 | 1.8 | 1.9 | 2.05 | V |
| | | VLD = 2 | 1.94 | 2.1 | 2.25 | |
| | | VLD = 3 | 2.05 | 2.2 | 2.37 | |
| | | VLD = 4 | 2.14 | 2.3 | 2.48 | |
| | | VLD = 5 | 2.24 | 2.4 | 2.6 | |
| | | VLD = 6 | 2.33 | 2.5 | 2.71 | |
| | | VLD = 7 | 2.46 | 2.65 | 2.86 | |
| | | VLD = 8 | 2.58 | 2.8 | 3 | |
| | | VLD = 9 | 2.69 | 2.9 | 3.13 | |
| | | VLD = 10 | 2.83 | 3.05 | 3.29 | |
| | | VLD = 11 | 2.94 | 3.2 | 3.42 | |
| | | VLD = 12 | 3.11 | 3.35 | 3.61 ⁽³⁾ | |
| | | VLD = 13 | 3.24 | 3.5 | 3.76 ⁽³⁾ | |
| | | VLD = 14 | 3.43 | 3.7 ⁽³⁾ | 3.99 ⁽³⁾ | |
| | $V_{CC}/dt \leq 3 \text{ V/s}$ (see Figure 5-9), external voltage applied on P2.3 | VLD = 15 | 1.1 | 1.2 | 1.3 | |
| $I_{CC(SVS)}$ ⁽¹⁾ | VLD \neq 0, $V_{CC} = 2.2 \text{ V}$ or 3 V | | 10 | 15 | μA | |

(1) The current consumption of the SVS module is not included in the I_{CC} current consumption data.

(2) t_{settle} is the settling time that the comparator o/p must have a stable level after VLD is switched from VLD \neq 0 to a different VLD value between 2 and 15. The overdrive is assumed to be $> 50 \text{ mV}$.

(3) The recommended operating voltage range is limited to 3.6 V .

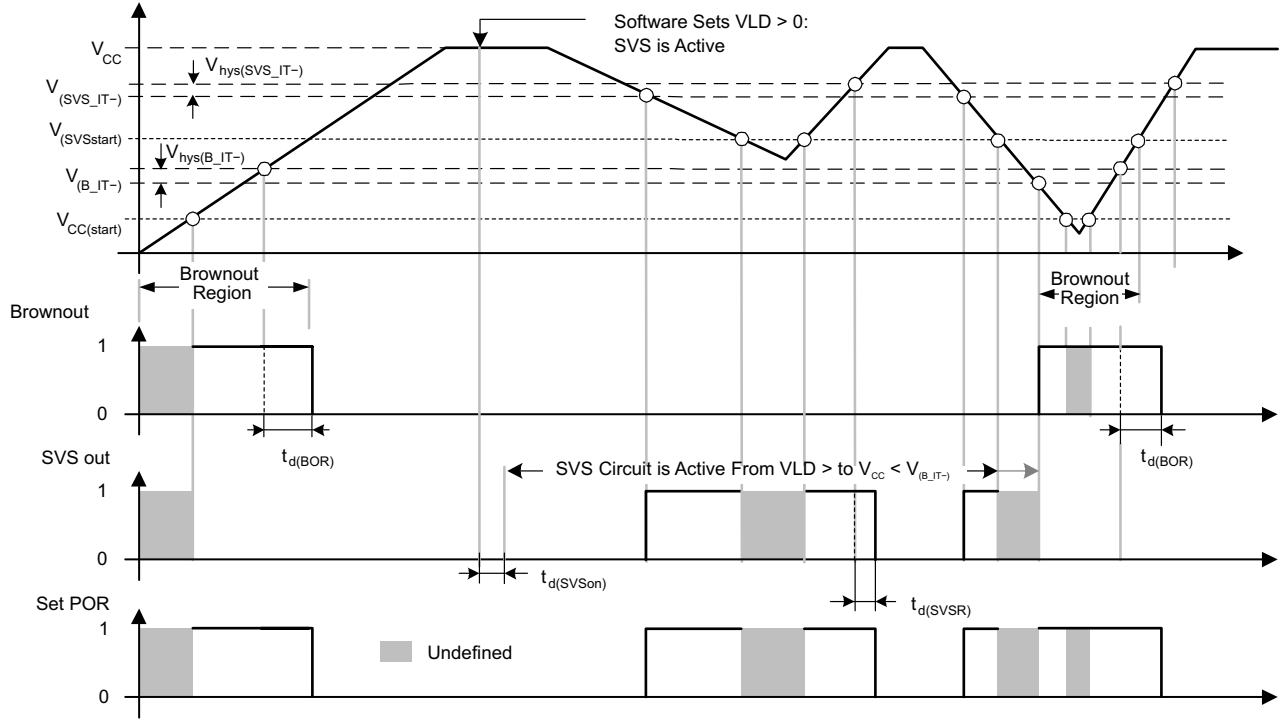


Figure 5-9. SVS Reset (SVSR) vs Supply Voltage

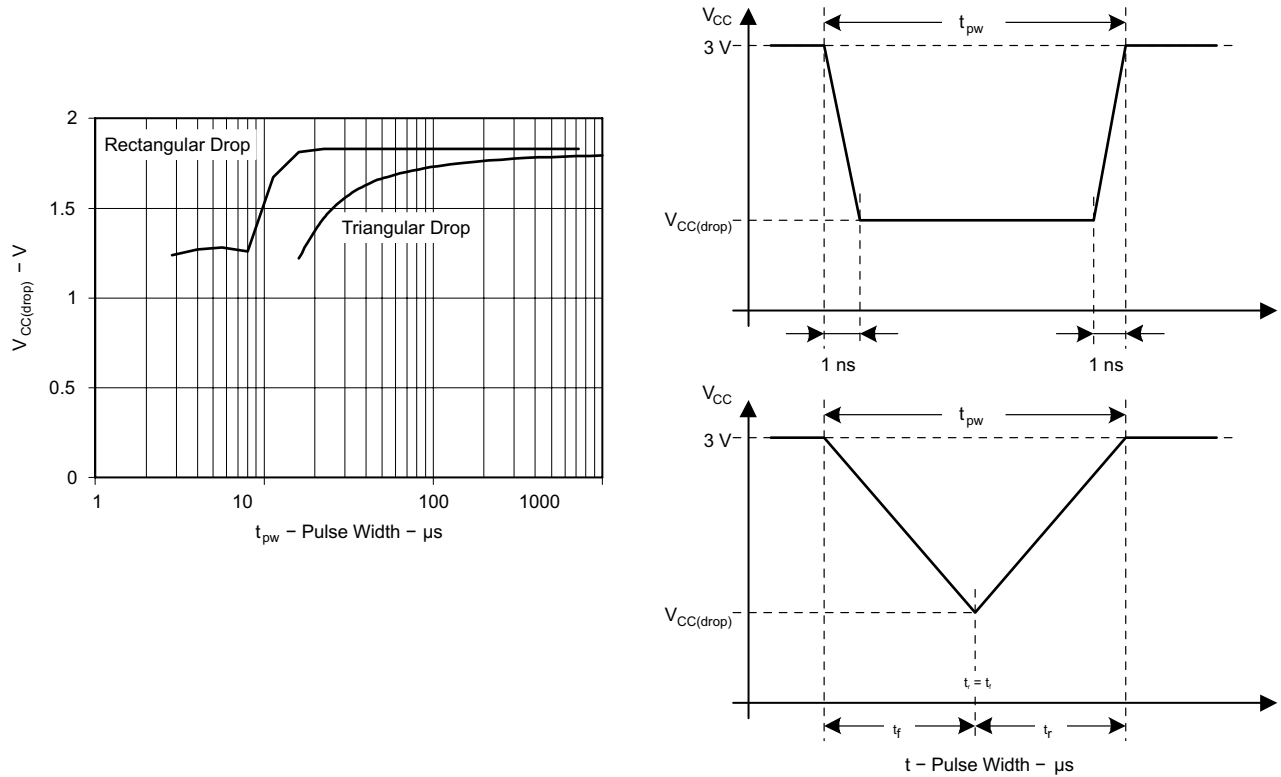


Figure 5-10. $V_{CC(drop)}$ With a Rectangular Voltage Drop and a Triangular Voltage Drop to Generate an SVS Signal

5.18 DCO

over recommended operating free-air temperature range (unless otherwise noted) (also see [Figure 5-11](#) through [Figure 5-13](#))

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------------|---|-----------------|------|------|------|------|
| f _(DCOCLK) | N _(DCO) = 01Eh, FN ₈ = FN ₄ = FN ₃ = FN ₂ = 0, D = 2, DCOPLUS = 0, f _{Crystal} = 32.768 kHz | 3 V | | 1 | | MHz |
| f _(DCO = 2) | FN ₈ = FN ₄ = FN ₃ = FN ₂ = 0, DCOPLUS = 1 | 3 V | 0.3 | 0.7 | 1.3 | MHz |
| f _(DCO = 27) | FN ₈ = FN ₄ = FN ₃ = FN ₂ = 0, DCOPLUS = 1 | 3 V | 2.7 | 6.1 | 11.3 | MHz |
| f _(DCO = 2) | FN ₈ = FN ₄ = FN ₃ = FN ₂ = 1, DCOPLUS = 1 | 3 V | 0.8 | 1.5 | 2.5 | MHz |
| f _(DCO = 27) | FN ₈ = FN ₄ = FN ₃ = FN ₂ = 1, DCOPLUS = 1 | 3 V | 6.5 | 12.1 | 20 | MHz |
| f _(DCO = 2) | FN ₈ = FN ₄ = 0, FN ₃ = 1, FN ₂ = x, DCOPLUS = 1 | 3 V | 1.3 | 2.2 | 3.5 | MHz |
| f _(DCO = 27) | FN ₈ = FN ₄ = 0, FN ₃ = 1, FN ₂ = x, DCOPLUS = 1 | 3 V | 10.3 | 17.9 | 28.5 | MHz |
| f _(DCO = 2) | FN ₈ = 0, FN ₄ = 1, FN ₃ = FN ₂ = x, DCOPLUS = 1 | 3 V | 2.1 | 3.4 | 5.2 | MHz |
| f _(DCO = 27) | FN ₈ = 0, FN ₄ = 1, FN ₃ = FN ₂ = x, DCOPLUS = 1 | 3 V | 16 | 26.6 | 41 | MHz |
| f _(DCO = 2) | FN ₈ = 1, FN ₄ = 1 = FN ₃ = FN ₂ = x, DCOPLUS = 1 | 3 V | 4.2 | 6.3 | 9.2 | MHz |
| f _(DCO = 27) | FN ₈ = 1, FN ₄ = 1 = FN ₃ = FN ₂ = x, DCOPLUS = 1 | 3 V | 30 | 46 | 70 | MHz |
| S _n | Step size (ratio) between adjacent DCO taps: S _n = f _{DCO(Tap n+1)} /f _{DCO(Tap n)} (see Figure 5-12 for taps 21 to 27) | 1 < TAP ≤ 20 | | | 1.11 | |
| | | TAP = 27 | | 1.06 | | 1.17 |
| D _t | Temperature drift, N _(DCO) = 01Eh, FN ₈ = FN ₄ = FN ₃ = FN ₂ = 0, D = 2, DCOPLUS = 0 | 3 V | -0.2 | -0.3 | -0.4 | %/°C |
| D _V | Drift with V _{CC} variation, N _(DCO) = 01Eh, FN ₈ = FN ₄ = FN ₃ = FN ₂ = 0, D = 2, DCOPLUS = 0 | | 0 | 5 | 15 | %/V |

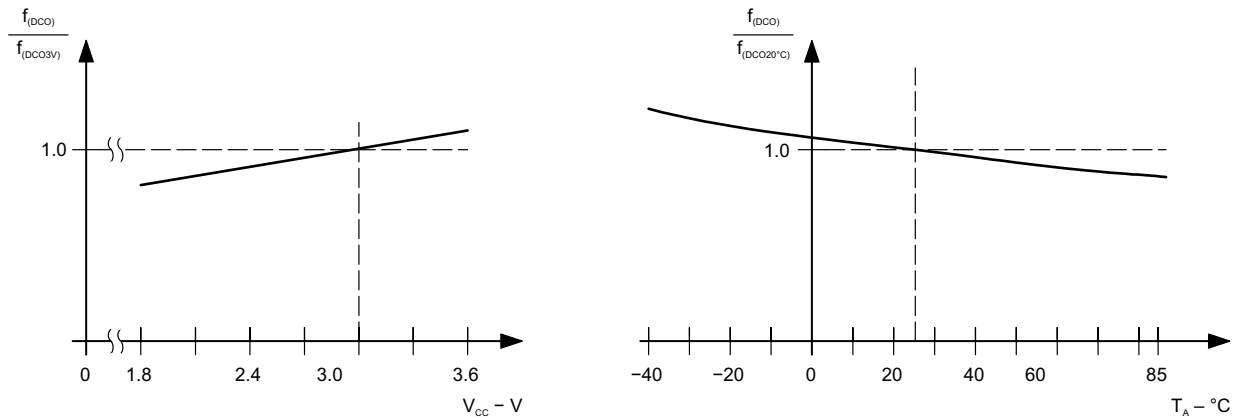


Figure 5-11. DCO Frequency vs Supply Voltage V_{CC} and vs Ambient Temperature

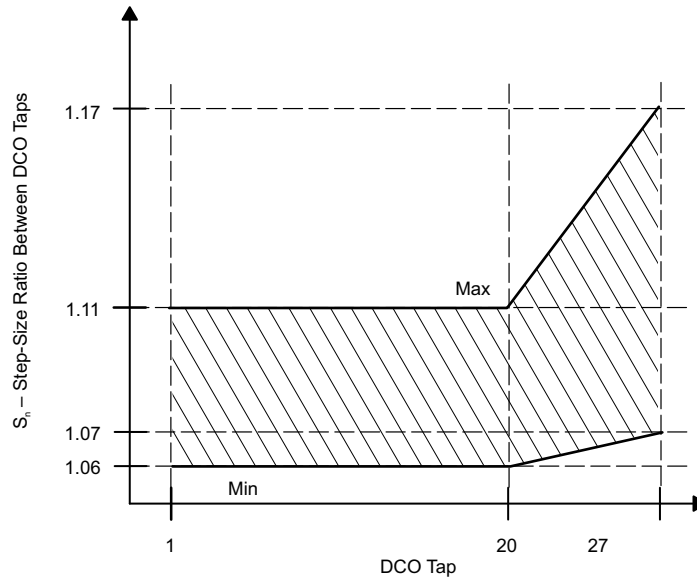


Figure 5-12. DCO Tap Step Size

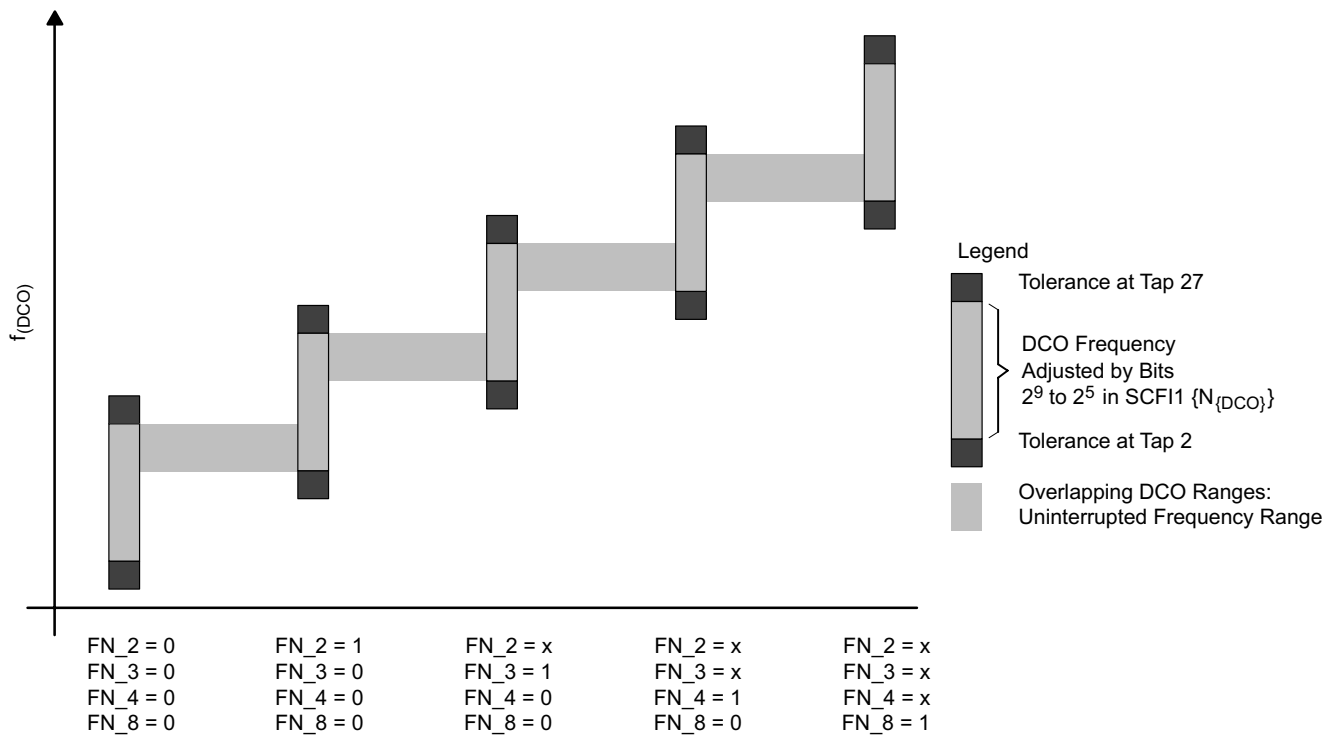


Figure 5-13. Five Overlapping DCO Ranges Controlled by FN_x Bits

5.19 Crystal Oscillator, LFXT1 Oscillator^{(1) (2)}

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------|--|-----------------|-----------------|-----------------------|-----|-----------------------|------|
| C _{XIN} | Integrated input capacitance ⁽³⁾ | OSCCAPx = 0h | 3 V | | 0 | | pF |
| | | OSCCAPx = 1h | | | 10 | | |
| | | OSCCAPx = 2h | | | 14 | | |
| | | OSCCAPx = 3h | | | 18 | | |
| C _{XOUT} | Integrated output capacitance ⁽³⁾ | OSCCAPx = 0h | 3 V | | 0 | | pF |
| | | OSCCAPx = 1h | | | 10 | | |
| | | OSCCAPx = 2h | | | 14 | | |
| | | OSCCAPx = 3h | | | 18 | | |
| V _{IL} | Input levels at XIN ⁽⁴⁾ | | 2.2 V, 3 V | V _{SS} | | 0.2 × V _{CC} | V |
| V _{IH} | | | | 0.8 × V _{CC} | | V _{CC} | |

- (1) The parasitic capacitance from the package and board may be estimated to be 2 pF. The effective load capacitor for the crystal is $(C_{XIN} \times C_{XOUT}) / (C_{XIN} + C_{XOUT})$. This is independent of XTS_FLL.
- (2) To improve EMI on the low-power LFXT1 oscillator, particularly in the LF mode (32 kHz), the following guidelines should be observed.
 - Keep the trace between the device and the crystal as short as possible.
 - Design a good ground plane around the oscillator pins.
 - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
 - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
 - Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
 - If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.
 - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.
- (3) TI recommends external capacitance for precision real-time clock applications; OSCCAPx = 0h.
- (4) Applies only when using an external logic-level clock source. XTS_FLL must be set. Not applicable when using a crystal or resonator.

5.20 ESP430CE1, SD16 and ESP430 Power Supply and Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | V _{CC} | MIN | TYP | MAX | UNIT |
|------------------------|--|---|--|-----------------|-----|------|------|------|
| AV _{CC} | Analog supply voltage | AV _{CC} = DV _{CC} , AV _{SS} = DV _{SS} = 0 V | | | 2.7 | | 3.6 | V |
| I _{ESP430CE1} | Total digital and analog supply current when ESP430 and SD16 active (I _{AVCC} + I _{DVCC}) | SD16LP = 0, f _{MCLK} = 4 MHz, f _{SD16} = f _{MCLK} / 4, SD16REFON = 1, SD16VMIDON = 0 | GAIN(V): 1, GAIN(I1): 1, I2: off | 3 V | | 2.0 | 2.6 | mA |
| | | | GAIN(V): 1, GAIN(I1): 32, I2: off | | | 2.4 | 3.3 | |
| | | | GAIN(V): 1, GAIN(I1): 1, GAIN(I2): 1 | | | 2.7 | 3.6 | |
| | | | GAIN(V): 1, GAIN(I1): 32, GAIN(I2): 32 | | | 3.4 | 4.9 | |
| | | SD16LP = 1, f _{MCLK} = 2 MHz, f _{SD16} = f _{MCLK} / 4, SD16REFON = 1, SD16VMIDON = 0 | GAIN(V): 1, GAIN(I1): 1, I2: off | | | 1.5 | 2.1 | |
| | | | GAIN(V): 1, GAIN(I1): 32, I2: off | | | 1.6 | 2.1 | |
| | | | GAIN(V): 1, GAIN(I1): 1, GAIN(I2): 1 | | | 2.1 | 2.8 | |
| | | | GAIN(V): 1, GAIN(I1): 32, GAIN(I2): 32 | | | 2.2 | 3.0 | |
| I _{SD16} | Analog supply current: 1 active SD16 channel including internal reference (ESP430 disabled) | SD16LP = 0, f _{SD16} = 1 MHz, SD16OSR = 256 | GAIN: 1, 2 | 3 V | | 650 | 950 | μA |
| | | | GAIN: 4, 8, 16 | | | 730 | 1100 | |
| | | | GAIN: 32 | | | 1050 | 1550 | |
| | | SD16LP = 1, f _{SD16} = 0.5 MHz, SD16OSR = 256 | GAIN: 1 | | | 620 | 930 | |
| | | | GAIN: 32 | | | 700 | 1060 | |
| | | | | | | | | |
| f _{MAINS} | Mains frequency range | | | 33 | | 80 | Hz | |
| f _{SD16} | Analog front-end input clock frequency | SD16LP = 0 (low-power mode disabled) | | | 1 | | MHz | |
| | | SD16LP = 1 (low-power mode enabled) | | | 0.5 | | | |

5.21 ESP430CE1, SD16 Input Range⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------|---|---|--|-----------------|----------------------|------|------------------|------|
| V _{ID} | Differential input voltage range for specified performance ⁽²⁾ | SD16GAIN _x = 1, SD16REFON = 1 | | | | ±500 | | mV |
| | | SD16GAIN _x = 2, SD16REFON = 1 | | | | ±250 | | |
| | | SD16GAIN _x = 4, SD16REFON = 1 | | | | ±125 | | |
| | | SD16GAIN _x = 8, SD16REFON = 1 | | | | ±62 | | |
| | | SD16GAIN _x = 16, SD16REFON = 1 | | | | ±31 | | |
| | | SD16GAIN _x = 32, SD16REFON = 1 | | | | ±15 | | |
| Z _I | Input impedance (one input pin to AV _{SS}) | f _{SD16} = 1 MHz, SD16GAIN _x = 1 | | 3 V | | 200 | | kΩ |
| | | f _{SD16} = 1 MHz, SD16GAIN _x = 32 | | | | 75 | | |
| Z _{ID} | Differential input impedance (IN+ to IN-) | f _{SD16} = 1 MHz, SD16GAIN _x = 1 | | 3 V | 300 | 400 | | kΩ |
| | | f _{SD16} = 1 MHz, SD16GAIN _x = 32 | | | | 100 | 150 | |
| V _I | Absolute input voltage range | | | | AV _{SS} - 1 | | AV _{CC} | V |
| V _{IC} | Common-mode input voltage range | | | | AV _{SS} - 1 | | AV _{CC} | V |

(1) All parameters pertain to each SD16 channel.

(2) The analog input range depends on the reference voltage applied to V_{REF}. If V_{REF} is sourced externally, the full-scale range is defined by V_{F_{SR+}} = +(V_{REF} / 2) / GAIN and V_{F_{SR-}} = -(V_{REF} / 2) / GAIN. The analog input range should not exceed 80% of V_{F_{SR+}} or V_{F_{SR-}}.

5.22 ESP430CE1, SD16 Performance

$f_{SD16} = 1$ MHz, SD16OSRx = 256, SD16REFON = 1, over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT | | | | | | | | | | | |
|----------------------|--------------------------------------|--|-----------------|------|------|------|-------|-----------------------------------|------|------|------|------|------|------|-------|-------|-------|-------|
| SINAD | Signal-to-noise + distortion ratio | SD16GAINx = 1, signal amplitude = 500 mV | 3 V | 83.5 | 85 | 76 | 79.5 | | | | | | | | | | | |
| | | SD16GAINx = 2, signal amplitude = 250 mV | | | | | | f _{IN} = 50 Hz or 100 Hz | 73 | 76.5 | | | | | | | | |
| | | SD16GAINx = 4, signal amplitude = 125 mV | | | | | | | | | 69 | 73 | | | | | | |
| | | SD16GAINx = 8, signal amplitude = 62 mV | | | | | | | | | | | 62 | 69 | | | | |
| | | SD16GAINx = 16, signal amplitude = 31 mV | | | | | | | | | | | | | 62 | 69 | | |
| | | SD16GAINx = 32, signal amplitude = 15 mV | | | | | | | | | | | | | | | 62 | 69 |
| G | Nominal gain | SD16GAINx = 1 | 3 V | 0.97 | 1.00 | 1.02 | | | | | | | | | | | | |
| | | SD16GAINx = 2 | | | | | 1.90 | 1.96 | 2.02 | | | | | | | | | |
| | | SD16GAINx = 4 | | | | | | | | 3.76 | 3.86 | 3.96 | | | | | | |
| | | SD16GAINx = 8 | | | | | | | | | | | 7.36 | 7.62 | | | | |
| | | SD16GAINx = 16 | | | | | | | | | | | | | 14.56 | 15.04 | | |
| | | SD16GAINx = 32 | | | | | | | | | | | | | | | 27.20 | 28.35 |
| E _{OS} | Offset error | SD16GAINx = 1 | 3 V | | | ±0.2 | | | | | | | | | | | | |
| | | SD16GAINx = 32 | | | | | | | ±1.5 | | | | | | | | | |
| dE _{OS} /dT | Offset error temperature coefficient | SD16GAINx = 1 | 3 V | | | ±4 | | | | ±20 | | | | | | | | |
| | | SD16GAINx = 32 | | | | | | | ±20 | | ±100 | | | | | | | |
| CMRR | Common-mode rejection ratio | SD16GAINx = 1, Common-mode input signal: V _{ID} = 500 mV, f _{IN} = 50 Hz or 100 Hz | 3 V | | | | | | | >90 | | | | | | | | |
| | | SD16GAINx = 32, Common-mode input signal: V _{ID} = 16 mV, f _{IN} = 50 Hz or 100 Hz | | | | | | | >75 | | | | | | | | | |
| AC PSRR | AC power-supply rejection ratio | SD16GAINx = 1, V _{CC} = 3 V ±100 mV, f _{VCC} = 50 Hz | 3 V | | | | | | | >80 | dB | | | | | | | |
| XT | Crosstalk | | 3 V | | | | <-100 | dB | | | | | | | | | | |

5.23 ESP430CE1, SD16 Temperature Sensor⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT | | | |
|----------------------------|--------------------------------------|---|-----------------|------|------|------|------|-----|-----|-----|
| TC _{Sensor} | Sensor temperature coefficient | | | 1.18 | 1.32 | 1.46 | mV/K | | | |
| V _{Offset,sensor} | Sensor offset voltage | | | -100 | | 100 | mV | | | |
| V _{Sensor} | Sensor output voltage ⁽²⁾ | Temperature sensor voltage at T _A = 85°C | 3 V | 435 | 475 | 515 | mV | | | |
| | | Temperature sensor voltage at T _A = 25°C | | | | | | 355 | 395 | 435 |
| | | Temperature sensor voltage at T _A = 0°C | | | | | | | | |

(1) The following formula can be used to calculate the temperature sensor output voltage:

$$V_{\text{Sensor,typ}} = TC_{\text{Sensor}} (273 + T [^{\circ}\text{C}]) + V_{\text{Offset,sensor}} [\text{mV}]$$

(2) Results based on characterization or production test, no TC_{Sensor} or V_{Offset,sensor}.

5.24 ESP430CE1, SD16 Built-in Voltage Reference

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------|---|--|-----------------|------|------|------|-------|
| V _{REF} | Internal reference voltage | SD16REFON = 1, SD16VMIDON = 0 | 3 V | 1.14 | 1.20 | 1.26 | V |
| I _{REF} | Reference supply current | SD16REFON = 1, SD16VMIDON = 0 | 3 V | | 175 | 260 | μA |
| TC | Temperature coefficient | SD16REFON = 1, SD16VMIDON = 0 ⁽¹⁾ | 3 V | | 20 | 50 | ppm/K |
| C _{REF} | V _{REF} load capacitance | SD16REFON = 1 SD16VMIDON = 0 ⁽²⁾ | | | 100 | | nF |
| I _{LOAD} | V _{REF(I)} maximum load current | SD16REFON = 0, SD16VMIDON = 0 | 3 V | | | ±200 | nA |
| t _{ON} | Turnon time | SD16REFON = 0 → 1, SD16VMIDON = 0, C _{REF} = 100 nF | 3 V | | 5 | | ms |
| DC PSR | DC power supply rejection, ΔV _{REF} /ΔV _{CC} | SD16REFON = 1, SD16VMIDON = 0, V _{CC} = 2.5 V to 3.6 V | | | 200 | | μV/V |

(1) Calculated using the box method: (MAX(−40°C to 85°C) – MIN(−40°C to 85°C)) / MIN(−40°C to 85°C) / (85°C – (−40°C)).

(2) There is no capacitance required on V_{REF}. However, TI recommends a capacitance of at least 100 nF to reduce any reference voltage noise.

5.25 ESP430CE1, SD16 Reference Output Buffer

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|--|---|-----------------|-----|-----|-----|------|
| V _{REF,BUF} | Reference buffer output voltage | SD16REFON = 1, SD16VMIDON = 1 | 3 V | | 1.2 | | V |
| I _{REF,BUF} | Reference supply and reference output buffer quiescent current | SD16REFON = 1, SD16VMIDON = 1 | 3 V | | 385 | 600 | A |
| C _{REF(O)} | Required load capacitance on V _{REF} | SD16REFON = 1, SD16VMIDON = 1 | | 470 | | | nF |
| I _{LOAD,Max} | Maximum load current on V _{REF} | SD16REFON = 1, SD16VMIDON = 1 | 3 V | | | ±1 | mA |
| | Maximum voltage variation versus load current | I _{LOAD} = 0 to 1 mA | 3 V | −15 | | +15 | mV |
| t _{ON} | Turnon time | SD16REFON = 0 → 1, SD16VMIDON = 0, C _{REF} = 100 nF | 3 V | | 100 | | μs |

5.26 ESP430CE1, SD16 External Reference Input

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------|---------------|-----------------|-----------------|-----|------|-----|------|
| V _{REF(I)} | Input voltage | SD16REFON = 0 | 3 V | 1.0 | 1.25 | 1.5 | V |
| I _{REF(I)} | Input current | SD16REFON = 0 | 3 V | | | 50 | nA |

5.27 ESP430CE1, Active Energy Measurement Test Conditions and Accuracy⁽¹⁾

 $T_A = 25^\circ\text{C}$, input conditions (unless otherwise noted): $I_B = 6\text{ A}$, $I_{MAX} = n \times I_B = 60\text{ A}$, $n = 10$, $V_N = 230\text{ V}$, $f_{MAINS} = 50\text{ Hz}$

| PARAMETER | TEST CONDITIONS | V_{CC} | TYP | UNIT |
|---------------------------------|---|----------|--------|------|
| Maximum error ⁽²⁾⁽³⁾ | $I = 0.05 \times I_B$, $V = V_N$, PF = 1.0 | 3 V | ±0.17% | |
| | $I = 0.1 \times I_B$ to I_{MAX} , $V = V_N$, PF = 1.0 | | ±0.18% | |
| | $I = 0.1 \times I_B$, $V = V_N$, PF = 0.5 lagging | | ±0.19% | |
| | $I = 0.2 \times I_B$ to I_{MAX} , $V = V_N$, PF = 0.5 lagging | | ±0.27% | |
| | $I = 0.1 \times I_B$, $V = V_N$, PF = 0.8 leading | | ±0.15% | |
| | $I = 0.2 \times I_B$ to I_{MAX} , $V = V_N$, PF = 0.8 leading | | ±0.24% | |
| | $I = 0.2 \times I_B$ to I_{MAX} , $V = V_N$, PF = 0.25 lagging | | ±0.38% | |

(1)

- $f_{ACLK} = 32768\text{ Hz}$ (watch crystal)
- $f_{MCLK} = 4.194\text{ MHz}$ (FLL+)
- $f_{SD16} = f_{MCLK} / 4 = 1.049\text{ MHz}$
- Single-point calibration at $I = 10\text{ A}$ and PF = 0.5 lagging
- Measurements according to IEC1036

(2) Measurements performed using complete hardware solution. Error shown contain temperature dependencies of all components including the MSP430FE42x, crystal, and discrete components.

- (3) I1 SD16GAIN x = 1 or 4: CT part number = T60404-E4624-X101 (Vacuumschmelze)
-
- I1 SD16GAINx = 8: shunt part number = A-H2-R005-F1-K2-0.1 (Isabellenhütte Heusler GmbH KG)
-
- I1 SD16GAINx = 32: shunt part number = BVO-M-R0002-5.0 (Isabellenhütte Heusler GmbH KG)

5.28 ESP430CE1, Active Energy Measurement Test Conditions and Accuracy⁽¹⁾

 $T_A = 25^\circ\text{C}$, input conditions (unless otherwise noted): $I_B = 10\text{ A}$, $I_{MAX} = n \times I_B = 60\text{ A}$, $n = 6$, $V_N = 230\text{ V}$, $f_{MAINS} = 50\text{ Hz}$

| PARAMETER | TEST CONDITIONS | V_{CC} | TYP | UNIT |
|---------------------------------|---|----------|--------|------|
| Maximum error ⁽²⁾⁽³⁾ | $I = 0.05 \times I_B$, $V = V_N$, PF = 1.0 | 3 V | ±0.11% | |
| | $I = 0.1 \times I_B$ to I_{MAX} , $V = V_N$, PF = 1.0 | | ±0.18% | |
| | $I = 0.1 \times I_B$, $V = V_N$, PF = 0.5 lagging | | ±0.45% | |
| | $I = 0.2 \times I_B$ to I_{MAX} , $V = V_N$, PF = 0.5 lagging | | ±0.33% | |
| | $I = 0.1 \times I_B$, $V = V_N$, PF = 0.8 leading | | ±0.10% | |
| | $I = 0.2 \times I_B$ to I_{MAX} , $V = V_N$, PF = 0.8 leading | | ±0.18% | |
| | $I = 0.2 \times I_B$ to I_{MAX} , $V = V_N$, PF = 0.25 lagging | | ±0.51% | |

(1)

- $f_{ACLK} = 32768\text{ Hz}$ (watch crystal)
- $f_{MCLK} = 4.194\text{ MHz}$ (FLL+)
- $f_{SD16} = f_{MCLK} / 4 = 1.049\text{ MHz}$
- Single-point calibration at $I = 10\text{ A}$ and PF = 0.5 lagging
- Measurements according to IEC1036

(2) Measurements performed using complete hardware solution. Error shown contain temperature dependencies of all components including the MSP430FE42x, crystal, and discrete components.

- (3) I1 SD16GAIN x = 1 or 4: CT part number = T60404-E4624-X101 (Vacuumschmelze)
-
- I1 SD16GAINx = 8: shunt part number = A-H2-R005-F1-K2-0.1 (Isabellenhütte Heusler GmbH KG)
-
- I1 SD16GAINx = 32: shunt part number = BVO-M-R0002-5.0 (Isabellenhütte Heusler GmbH KG)

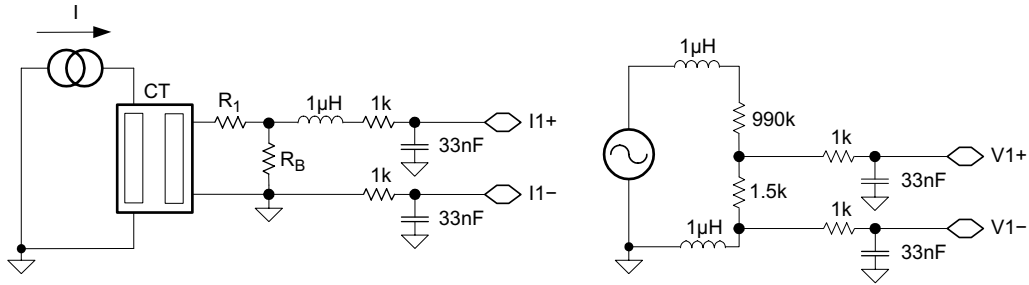


Figure 5-14. Energy Measurement Test Circuitry (SD16GAINx = 1 or 4)

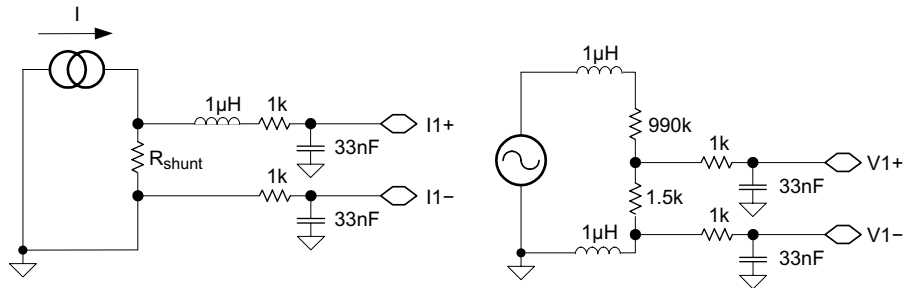
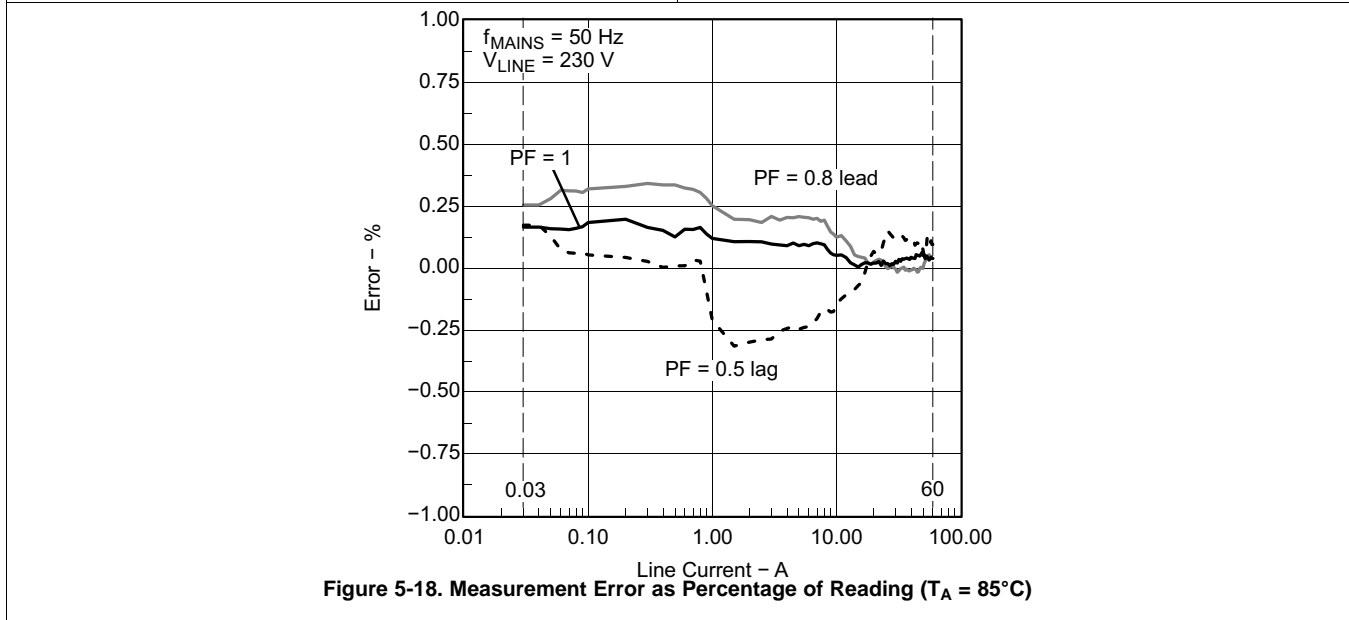
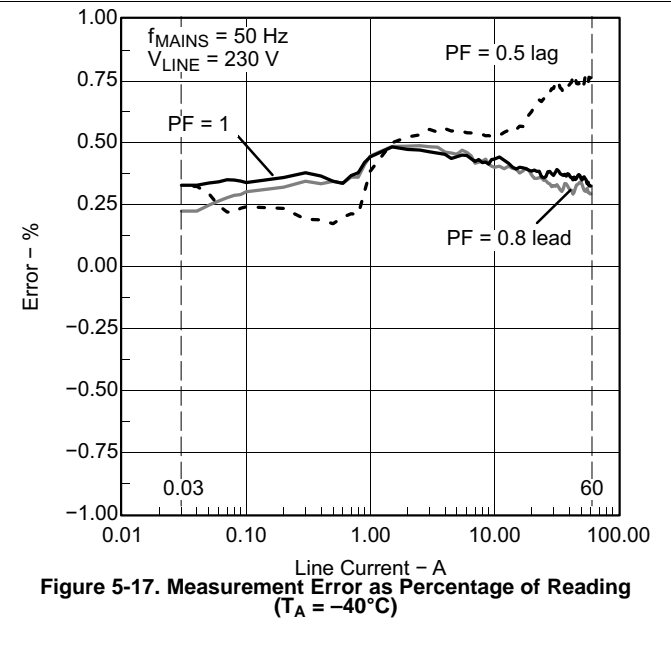
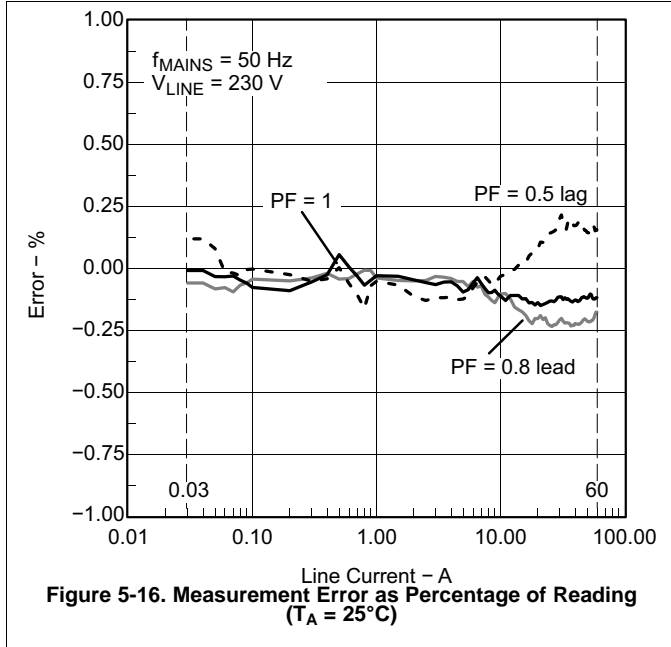


Figure 5-15. Energy Measurement Test Circuitry (SD16GAINx = 8 or 32)

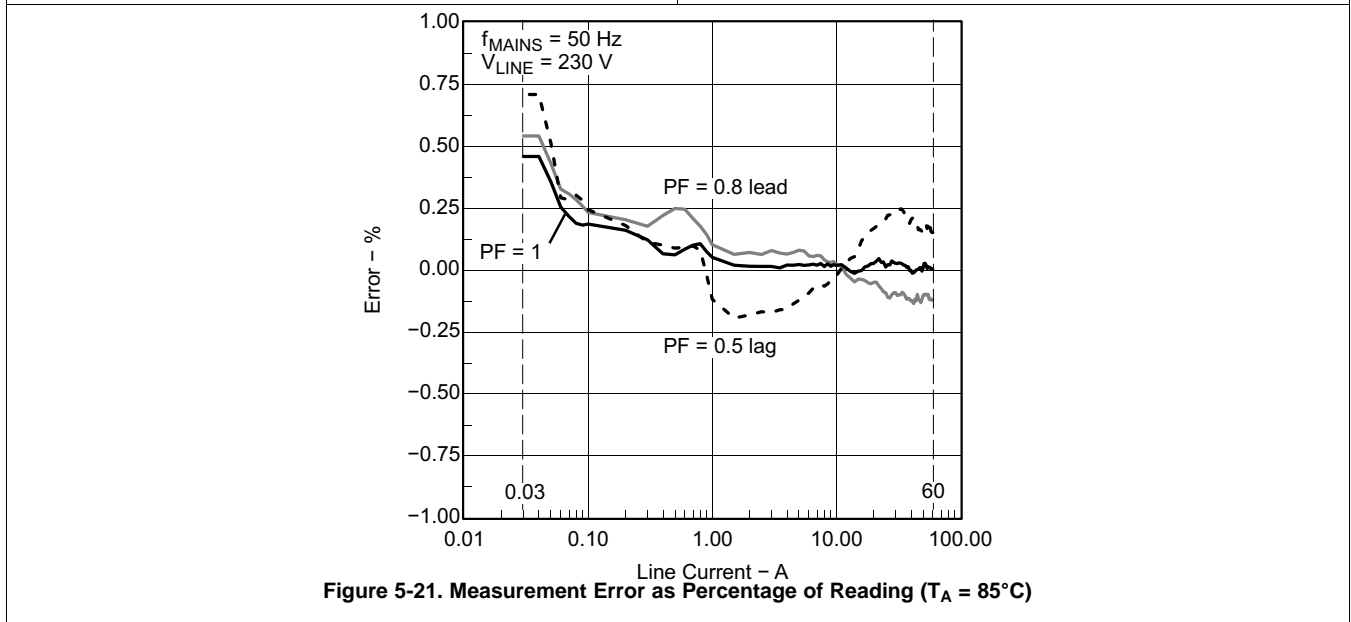
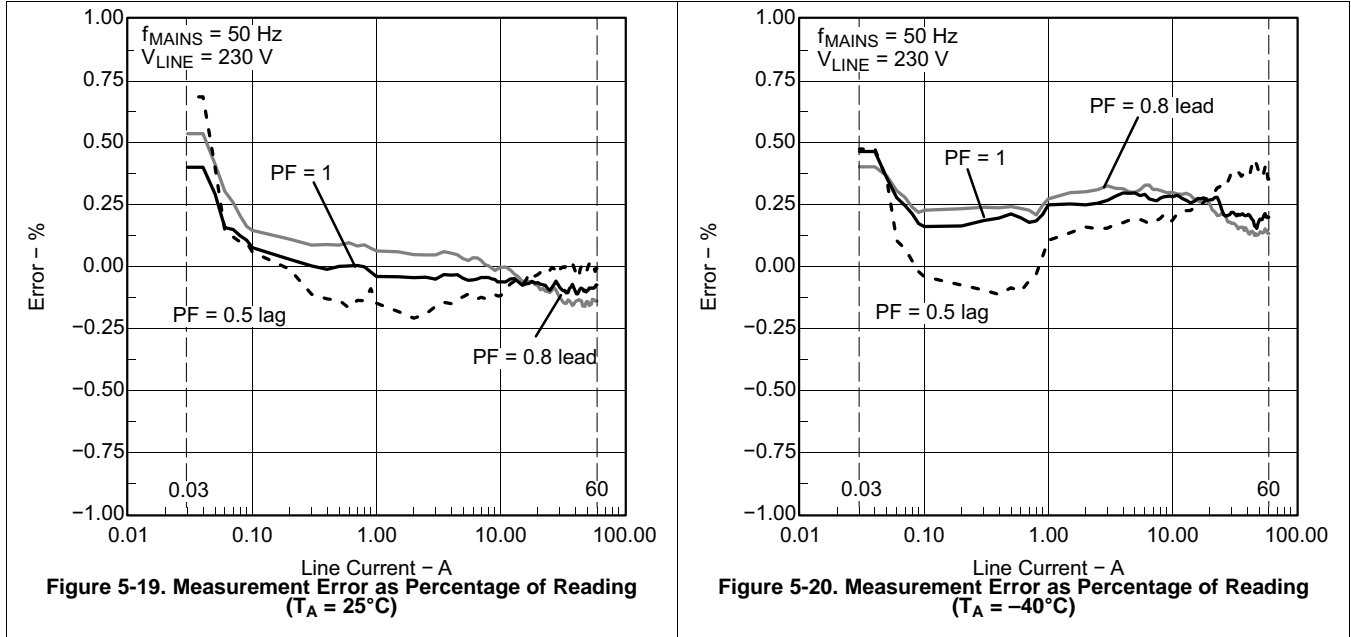
5.29 ESP430CE1 Typical Characteristics (I1 SD16GAINx = 1)

Results corrected for typical phase error of CT used (−40°C to 25°C: −0.7°; 25°C to 85°C: +0.5°). See Figure 5-14 for test circuitry: CT part number = T60404-E4624-X101 (Vacuumschmelze), $R_1 = 0 \Omega$, $R_B = 12.4 \Omega$



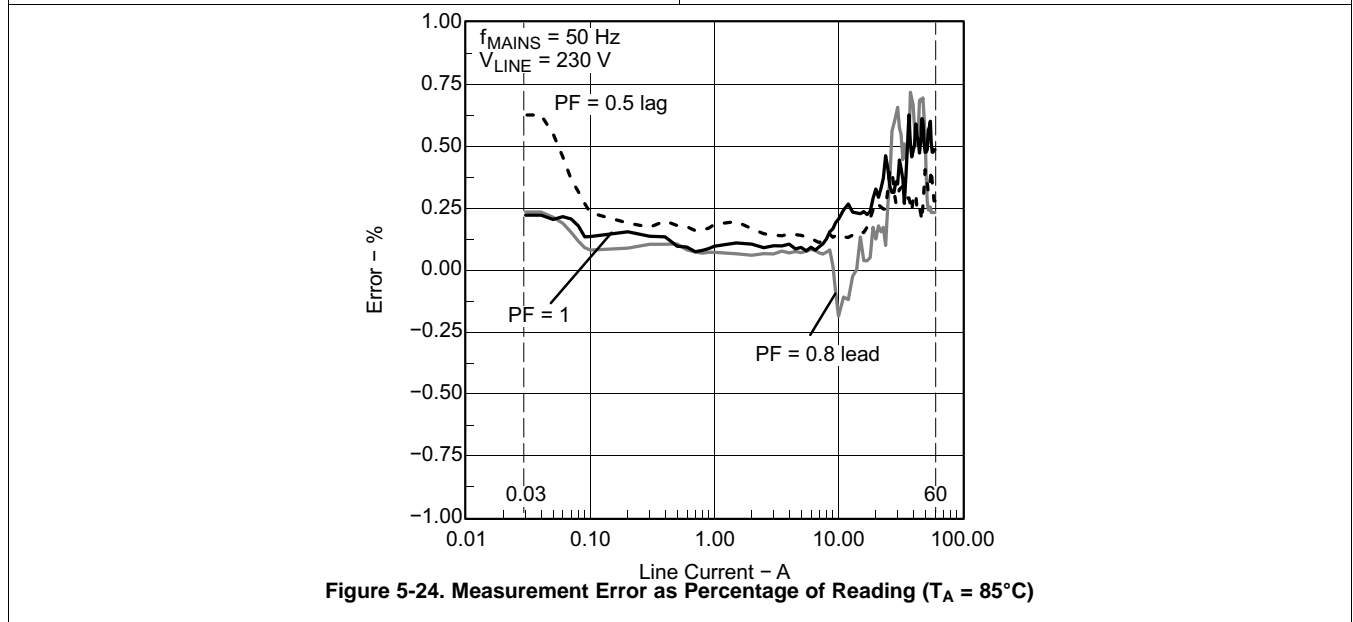
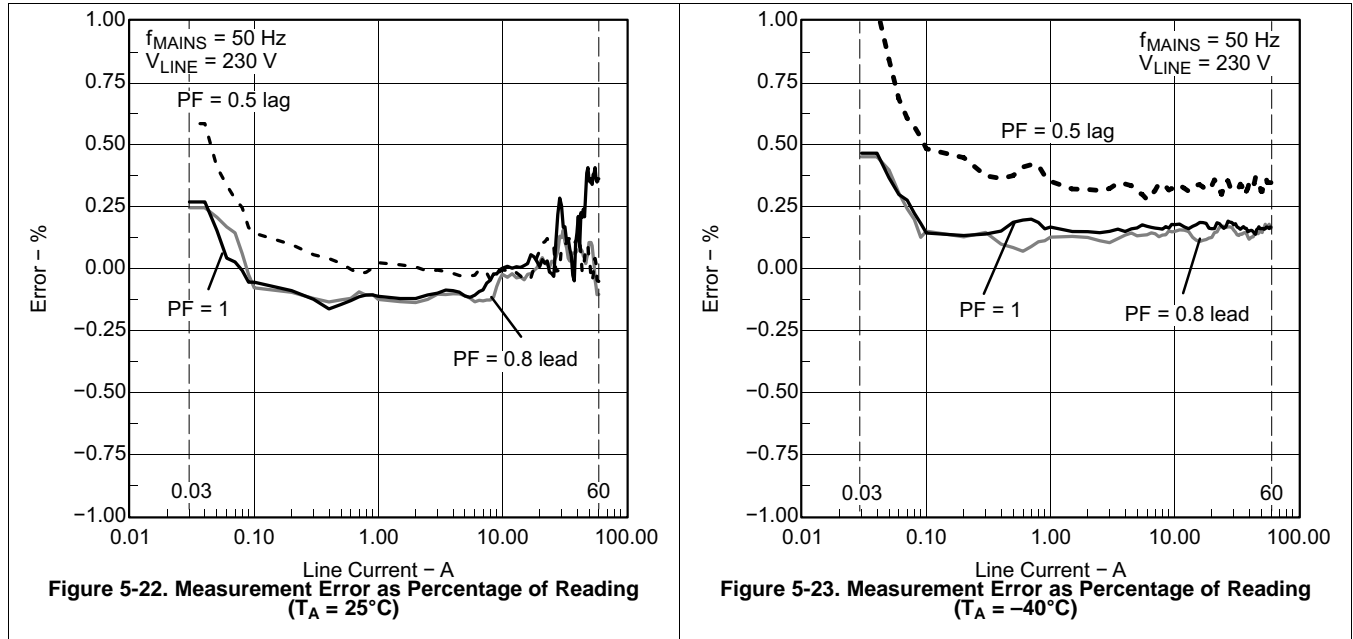
5.30 ESP430CE1 Typical Characteristics (I1 SD16GAINx = 4)

Results corrected for typical phase error of CT used (–40°C to 25°C: –0.7°; 25°C to 85°C: +0.5°). See [Figure 5-14](#) for test circuitry: CT part number = T60404-E4624-X101 (Vacuumschmelze), $R_1 = 9.36 \Omega$, $R_B = 3.16 \Omega$



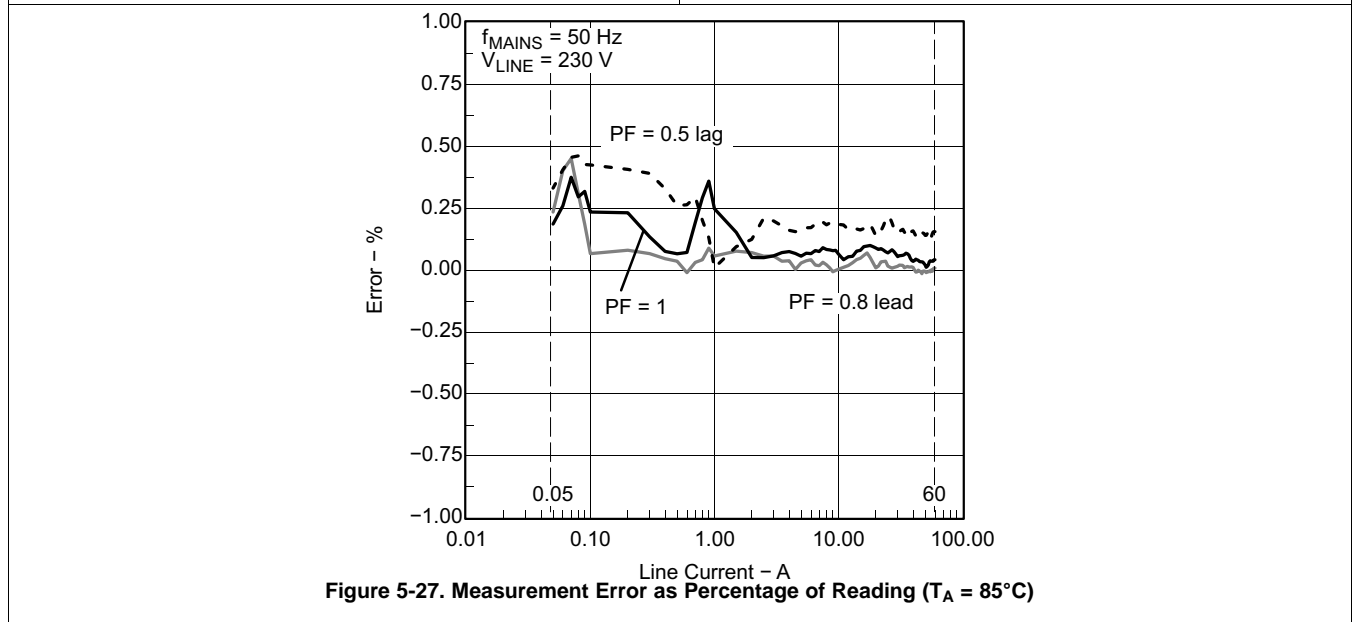
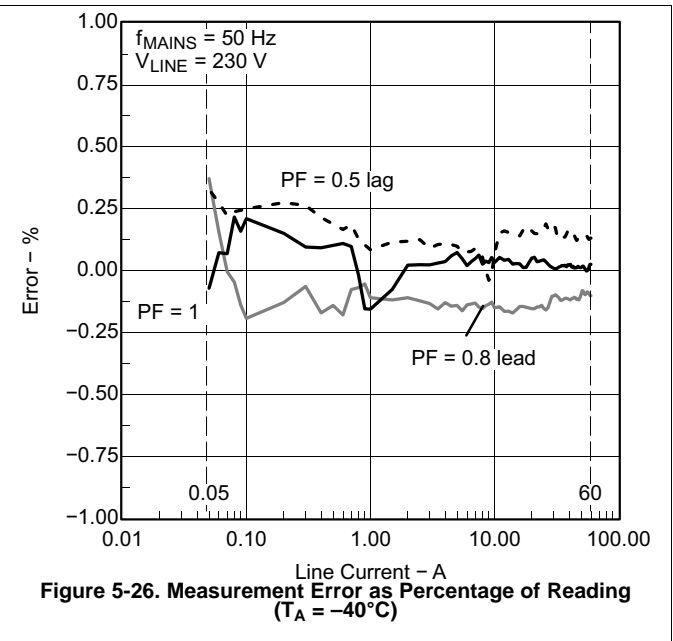
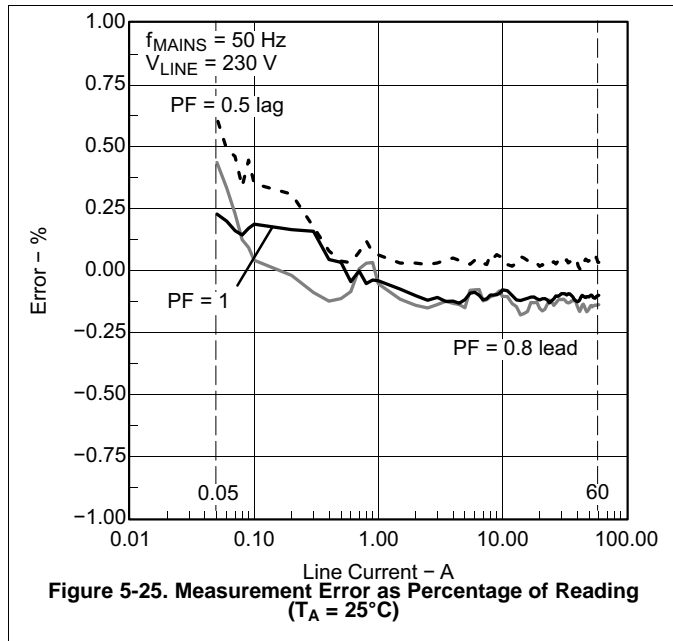
5.31 ESP430CE1 Typical Characteristics (I1 SD16GAINx = 8)

See [Figure 5-15](#) for test circuitry: shunt part number = A-H2-R005-F1-K2-0.1 (Isabellenhütte Heusler GmbH KG)



5.32 ESP430CE1 Typical Characteristics (I1 SD16GAINx = 32)

See [Figure 5-15](#) for test circuitry: shunt part number = BVO-M-R0002-5.0 (Isabellenhütte Heusler GmbH KG)



5.33 Flash Memory

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|----------------------------|---|-----------------------|-----------------|-----------------|-----------------|-----|------------------|
| V _{CC(PGM/ERASE)} | Program and erase supply voltage | | | 2.7 | | 3.6 | V |
| f _{FTG} | Flash timing generator frequency | | | 257 | | 476 | kHz |
| I _{PGM} | Supply current from DV _{CC} during program | | 2.7 V, 3.6 V | | 3 | 5 | mA |
| I _{ERASE} | Supply current from DV _{CC} during erase | | 2.7 V, 3.6 V | | 3 | 7 | mA |
| t _{CPT} | Cumulative program time | See ⁽¹⁾ | 2.7 V, 3.6 V | | | 10 | ms |
| t _{CMErase} | Cumulative mass erase time | See ⁽²⁾ | 2.7 V, 3.6 V | 200 | | | ms |
| | Program and erase endurance | | | 10 ⁴ | 10 ⁵ | | cycles |
| t _{Retention} | Data retention duration | T _J = 25°C | | 100 | | | years |
| t _{Word} | Word or byte program time | See ⁽³⁾ | | | 35 | | t _{FTG} |
| t _{Block, 0} | Block program time for first byte or word | | | | 30 | | |
| t _{Block, 1–63} | Block program time for each additional byte or word | | | | 21 | | |
| t _{Block, End} | Block program end-sequence wait time | | | | 6 | | |
| t _{Mass Erase} | Mass erase time | | | | 5297 | | |
| t _{Seg Erase} | Segment erase time | | | | 4819 | | |

- (1) The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word or byte write mode and block write mode.
- (2) The mass erase duration generated by the flash timing generator is at least 11.1 ms (= 5297 × (1 / f_{FTG,max}) = 5297 × (1 / 476 kHz)). To achieve the required cumulative mass erase time, the mass erase operation of the flash controller can be repeated until this time is met (a worst case minimum of 19 cycles is required).
- (3) These values are hardwired into the state machine of the flash controller (t_{FTG} = 1 / f_{FTG}).

5.34 JTAG Interface

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|--|--------------------|-----------------|-----|-----|-----|------|
| f _{TCK} | TCK input frequency | See ⁽¹⁾ | 2.2 V | 0 | | 5 | MHz |
| | | | 3V | 0 | | 10 | |
| R _{Internal} | Internal pullup resistance on TMS, TCK, TDI/TCLK | See ⁽²⁾ | 2.2 V, 3 V | 25 | 60 | 90 | kΩ |

- (1) f_{TCK} may be restricted to meet the timing requirements of the module selected.
- (2) TMS, TDI/TCLK, and TCK pullup resistors are implemented in all versions.

5.35 JTAG Fuse⁽¹⁾

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---------------------|---|-----------------------|-----|-----|------|
| V _{CC(FB)} | Supply voltage during fuse-blow condition | T _A = 25°C | 2.5 | | V |
| V _{FB} | Voltage level on TDI/TCLK for fuse-blow | | 6 | 7 | V |
| I _{FB} | Supply current into TDI/TCLK during fuse blow | | | 100 | mA |
| t _{FB} | Time to blow fuse | | | 1 | ms |

- (1) After the fuse is blown, no further access to the MSP430 JTAG/Test and emulation features is possible. The JTAG block is switched to bypass mode.

6 Detailed Description

6.1 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers (see [Figure 6-1](#)).

Peripherals are connected to the CPU using data, address, and control buses. Peripherals can be managed with all instructions.

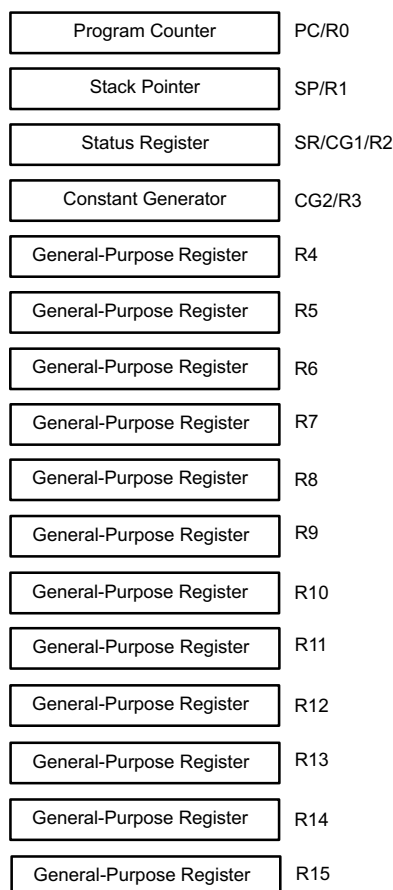


Figure 6-1. CPU Registers

6.2 Instruction Set

The instruction set consists of the original 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. [Table 6-1](#) lists examples of the three types of instruction formats; [Table 6-2](#) lists the address modes.

Table 6-1. Instruction Word Formats

| INSTRUCTION FORMAT | EXAMPLE | OPERATION |
|---|-----------|---|
| Dual operands, source and destination | ADD R4,R5 | $R4 + R5 \rightarrow R5$ |
| Single operand, destination only | CALL R8 | $PC \rightarrow (TOS), R8 \rightarrow PC$ |
| Relative jump, unconditional or conditional | JNE | Jump-on-equal bit = 0 |

Table 6-2. Address Mode Descriptions

| ADDRESS MODE | S ⁽¹⁾ | D ⁽¹⁾ | SYNTAX | EXAMPLE | OPERATION |
|------------------------|------------------|------------------|--------------------|-------------------|---|
| Register | • | • | MOV Rs, Rd | MOV R10, R11 | $R10 \rightarrow R11$ |
| Indexed | • | • | MOV X(Rn), Y(Rm) | MOV 2(R5), 6(R6) | $M(2+R5) \rightarrow M(6+R6)$ |
| Symbolic (PC relative) | • | • | MOV EDE, TONI | | $M(EDE) \rightarrow M(TONI)$ |
| Absolute | • | • | MOV & MEM, & TCDAT | | $M(MEM) \rightarrow M(TCDAT)$ |
| Indirect | • | | MOV @Rn, Y(Rm) | MOV @R10, Tab(R6) | $M(R10) \rightarrow M(Tab+R6)$ |
| Indirect autoincrement | • | | MOV @Rn+, Rm | MOV @R10+, R11 | $M(R10) \rightarrow R11$ $R10 + 2 \rightarrow R10$ |
| Immediate | • | | MOV #X, TONI | MOV #45, TONI | $\#45 \rightarrow M(TONI)$ |

(1) S = source, D = destination

6.3 Operating Modes

The MSP430FE42x has one active mode and five software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

Software can configure the following operating modes:

- Active mode (AM)
 - All clocks are active.
- Low-power mode 0 (LPM0)
 - CPU is disabled.
 - ACLK and SMCLK remain active, MCLK available to modules.
 - FLL+ loop control remains active.
- Low-power mode 1 (LPM1)
 - CPU is disabled.
 - ACLK and SMCLK remain active, MCLK available to modules.
 - FLL+ loop control is disabled.
- Low-power mode 2 (LPM2)
 - CPU is disabled.
 - MCLK, FLL+ loop control, and DCOCLK are disabled.
 - DC generator of the DCO remains enabled.
 - ACLK remains active.
- Low-power mode 3 (LPM3)
 - CPU is disabled.
 - MCLK, FLL+ loop control, and DCOCLK are disabled.
 - DC generator of the DCO is disabled.
 - ACLK remains active.
- Low-power mode 4 (LPM4)
 - CPU is disabled.
 - ACLK is disabled.
 - MCLK, FLL+ loop control, and DCOCLK are disabled.
 - DC generator of the DCO is disabled.
 - Crystal oscillator is stopped.

6.4 Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are in the address range 0FFFFh to 0FFE0h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence. [Table 6-3](#) lists the interrupt sources, flags, and vectors.

Table 6-3. Interrupt Sources, Flags, and Vectors

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|--|---|--|--------------|-------------|
| Power up External reset Watchdog Flash memory PC out of range ⁽¹⁾ | WDTIFG KEYV ⁽²⁾ | Reset | 0FFFEh | 15, highest |
| NMI oscillator fault Flash memory access violation | NMIIFG ⁽²⁾ OFIFG ⁽²⁾ ACCVIFG ⁽²⁾ | (Non)maskable ⁽³⁾ (Non)maskable (Non)maskable | 0FFFCh | 14 |
| ESP430 | MBCTL_OUTxIFG, MBCTL_INxIFG ⁽²⁾⁽⁴⁾ | Maskable | 0FFFAh | 13 |
| SD16 | SD16CCTLx SD16OVIFG, SD16CCTLx SD16IFG ⁽²⁾⁽⁴⁾ | Maskable | 0FFF8h | 12 |
| | | | 0FFF6h | 11 |
| Watchdog timer | WDTIFG | Maskable | 0FFF4h | 10 |
| USART0 receive | URXIFG0 | Maskable | 0FFF2h | 9 |
| USART0 transmit | UTXIFG0 | Maskable | 0FFF0h | 8 |
| | | | 0FFEEh | 7 |
| Timer_A3 | TACCR0 CCIFG ⁽⁴⁾ | Maskable | 0FFECCh | 6 |
| Timer_A3 | TACCR1 and TACCR2 CCIFGs, and TACTL TAIFG ⁽²⁾⁽⁴⁾ | Maskable | 0FFEAh | 5 |
| I/O port P1 (8 flags) | P1IFG.0 to P1IFG.7 ⁽²⁾⁽⁴⁾ | Maskable | 0FFE8h | 4 |
| | | | 0FFE6h | 3 |
| | | | 0FFE4h | 2 |
| I/O port P2 (8 flags) | P2IFG.0 to P2IFG.7 ⁽²⁾⁽⁴⁾ | Maskable | 0FFE2h | 1 |
| Basic Timer1 | BTIFG | Maskable | 0FFE0h | 0, lowest |

- (1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h–01FFh) or from within unused address ranges (0600h–0BFFh).
- (2) Multiple source flags
- (3) (Non)maskable: the individual interrupt enable bit can disable an interrupt event, but the general interrupt enable cannot.
- (4) Interrupt flags are in the module.

6.5 Special Function Registers

Most interrupt and module-enable bits are collected in the lowest address space. Special-function register bits not allocated to a functional purpose are not physically present in the device. This arrangement provides simple software access.

Legend


| | |
|---|---|
| rw | Bit can be read and written. |
| rw-0, rw-1 | Bit can be read and written. It is reset or set by PUC. |
| rw-(0), rw-(1) | Bit can be read and written. It is reset or set by POR. |
|  | SFR bit is not present in device. |

Figure 6-2 shows the Interrupt Enable Register 1, and Table 6-4 describes the bit fields.

Figure 6-2. Interrupt Enable Register 1 (Address = 00h)

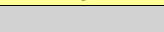
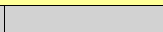
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|--------|--------|-------|---|--|------|-------|
| UTXIE0 | URXIE0 | ACCVIE | NMIIE |  |  | OFIE | WDTIE |
| rw-0 | rw-0 | rw-0 | rw-0 | | | rw-0 | rw-0 |

Table 6-4. Interrupt Enable Register 1 Description

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|-----|--------|------|-------|--|
| 7 | UTXIE0 | RW | 0h | USART0: UART and SPI transmit interrupt enable |
| 6 | URXIE0 | RW | 0h | USART0: UART and SPI receive interrupt enable |
| 5 | ACCVIE | RW | 0h | Flash access violation interrupt enable |
| 4 | NMIIE | RW | 0h | (Non)maskable interrupt enable |
| 1 | OFIE | RW | 0h | Oscillator fault interrupt enable |
| 0 | WDTIE | RW | 0h | Watchdog timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured in interval timer mode. |

Figure 6-3 shows the Interrupt Enable Register 2, and Table 6-5 describes the bit fields.

Figure 6-3. Interrupt Enable Register 2 (Address = 01h)

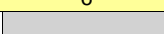
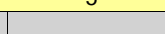
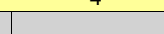
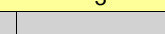



| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---|---|---|---|--|---|---|
| BTIE |  |  |  |  |  |  |  |
| rw-0 | | | | | | | |

Table 6-5. Interrupt Enable Register 2 Description

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|-----|-------|------|-------|-------------------------------|
| 7 | BTIE | RW | 0h | Basic Timer1 interrupt enable |

Figure 6-4 shows the Interrupt Flag Register 1, and Table 6-6 describes the bit fields.

Figure 6-4. Interrupt Flag Register 1 (Address = 02h)

| | | | | | | | |
|---------|---------|---|--------|---|---|-------|--------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UTXIFG0 | URXIFG0 | | NMIIFG | | | OFIFG | WDTIFG |
| rw-1 | rw-0 | | rw-0 | | | rw-1 | rw-(0) |

Table 6-6. Interrupt Flag Register 1 Description

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|-----|---------|------|-------|---|
| 7 | UTXIFG0 | RW | 1h | USART0: UART and SPI transmit flag |
| 6 | URXIFG0 | RW | 0h | USART0: UART and SPI receive flag |
| 4 | NMIIFG | RW | 0h | Set by the $\overline{\text{RST}}$ /NMI pin |
| 1 | OFIFG | RW | 1h | Flag set on oscillator fault. |
| 0 | WDTIFG | RW | 0h | Set on watchdog timer overflow (in watchdog mode) or security key violation. Reset on V_{CC} power on or a reset condition at the $\overline{\text{RST}}$ /NMI pin in reset mode. |

Figure 6-5 shows the Interrupt Flag Register 2, and Table 6-7 describes the bit fields.

Figure 6-5. Interrupt Flag Register 2 (Address = 03h)

| | | | | | | | |
|-------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BTIFG | | | | | | | |
| rw-0 | | | | | | | |

Table 6-7. Interrupt Flag Register 2 Description

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|-----|-------|------|-------|-----------------------------|
| 7 | BTIFG | RW | 0h | Basic Timer1 interrupt flag |

Figure 6-6 shows the Module Enable Register 1, and Table 6-8 describes the bit fields.

Figure 6-6. Module Enable Register 1 (Address = 04h)

| | | | | | | | |
|-------|-----------------|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UTXE0 | URXE0 USPIE0 | | | | | | |
| rw-0 | rw-0 | | | | | | |

Table 6-8. Module Enable Register 1 Description

| BIT | FIELD | TYPE | RESET | DESCRIPTION |
|-----|-----------------|------|-------|--|
| 7 | UTXE0 | RW | 0h | USART0: UART mode transmit enable |
| 6 | URXE0 USPIE0 | RW | 0h | USART0: UART mode receive enable USART0: SPI mode transmit and receive enable |

Module Enable Register 2 is not defined for the MSP430FE42x MCUs.

6.6 Memory Organization

Table 6-9 summarizes the memory map of the MSP430FE42x MCUs.

Table 6-9. Memory Organization

| | | MSP430FE423 | MSP430FE425 | MSP430FE427 |
|--------------------|-----------|---------------|---------------|---------------|
| Memory | Size | 8KB | 16KB | 32KB |
| Interrupt vector | Flash | 0FFFFh–0FFE0h | 0FFFFh–0FFE0h | 0FFFFh–0FFE0h |
| Code memory | Flash | 0FFFFh–0E000h | 0FFFFh–0C000h | 0FFFFh–08000h |
| Information memory | Size | 256 Byte | 256 Byte | 256 Byte |
| | | 010FFh–01000h | 010FFh–01000h | 010FFh–01000h |
| Boot memory | Size | 1KB | 1KB | 1KB |
| | | 0FFFh–0C00h | 0FFFh–0C00h | 0FFFh–0C00h |
| RAM | Size | 256 Byte | 512 Byte | 1KB |
| | | 02FFh–0200h | 03FFh–0200h | 05FFh–0200h |
| Peripherals | 16-bit | 01FFh–0100h | 01FFh–0100h | 01FFh–0100h |
| | 8-bit | 0FFh–010h | 0FFh–010h | 0FFh–010h |
| | 8-bit SFR | 0Fh–00h | 0Fh–00h | 0Fh–00h |

6.7 Bootloader (BSL)

The MSP430 bootloader (BSL) enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory through the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see [MSP430 Programming With the Bootloader \(BSL\)](#).

| BSL FUNCTION | PM PACKAGE PINS |
|---------------|-----------------|
| Data transmit | 53 - P1.0 |
| Data receiver | 52 - P1.1 |

6.8 Flash Memory

The flash memory (see [Figure 6-7](#)) can be programmed using the JTAG port, the bootloader, or in system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and two segments of information memory (A and B) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A and B can be erased individually, or as a group with segments 0 to n . Segments A and B are also called *information memory*.
- New devices may have some bytes programmed in the information memory (needed for test during manufacturing). The user should perform an erase of the information memory before the first use.

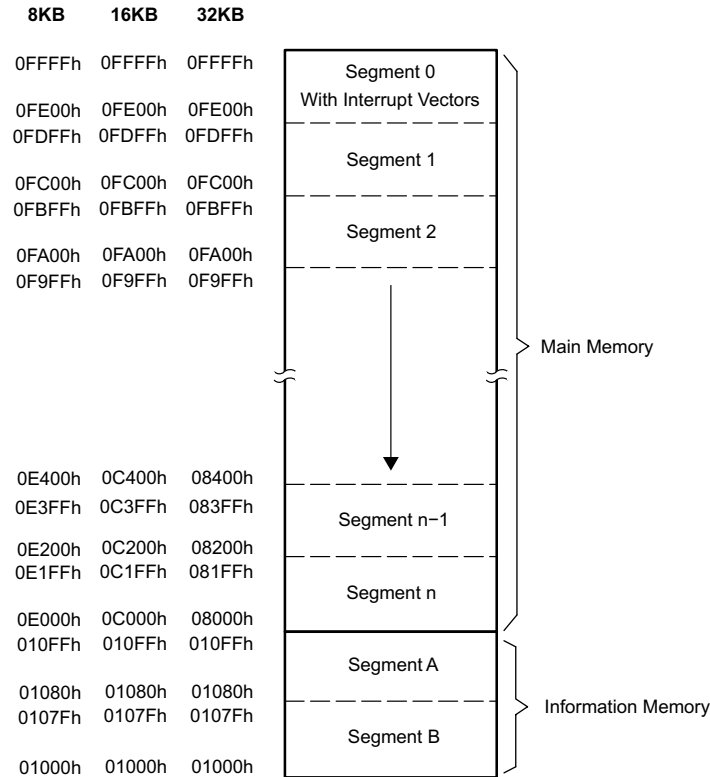


Figure 6-7. Flash Memory Map

6.9 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. Peripherals can be managed using all instructions. For complete module descriptions, see the [MSP430x4xx Family User's Guide](#).

6.9.1 Oscillator and System Clock

The clock system is supported by the FLL+ module that includes support for a 32768-Hz watch crystal oscillator, an internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator. The FLL+ clock module is designed to meet the requirements of both low system cost and low power consumption. The FLL+ features digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the watch crystal frequency. The internal DCO provides a fast turnon clock source and stabilizes in less than 6 μs. The FLL+ module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal or a high-frequency crystal
- Main clock (MCLK), the system clock used by the CPU
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, or ACLK/8

6.9.2 Brownout, Supply Voltage Supervisor (SVS)

The brownout circuit provides the proper internal reset signal to the device during power on and power off. The SVS circuitry detects if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (the device is not automatically reset).

The CPU begins code execution after the brownout circuit releases the device reset. However, V_{CC} may not have ramped to $V_{CC(min)}$ at that time. The user must ensure that the default FLL+ settings are not changed until V_{CC} reaches $V_{CC(min)}$. If desired, the SVS circuit can be used to determine when V_{CC} reaches $V_{CC(min)}$.

6.9.3 Digital I/O

Two I/O ports are implemented: ports P1 and P2 (only six P2 I/O signals are available on external pins).

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.

NOTE

Six bits of port P2 (P2.0 to P2.5) are available on external pins, but all control and data bits for port P2 are implemented.

6.9.4 Basic Timer1

The Basic Timer1 has two independent 8-bit timers that can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. The Basic Timer1 can be used to generate periodic interrupts and clock for the LCD module.

6.9.5 LCD Drive

The LCD driver generates the segment and common signals required to drive an LCD display. The LCD controller has dedicated data memory to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-mux, 3-mux, and 4-mux LCDs are supported by this peripheral.

6.9.6 Watchdog Timer (WDT+)

The primary function of the WDT+ module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

6.9.7 Timer_A3

Timer_A3 is a 16-bit timer and counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing (see [Table 6-10](#)). Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-10. Timer_A3 Signal Connections

| INPUT PIN NUMBER | DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | OUTPUT PIN NUMBER |
|------------------|---------------------------|-------------------|--------------|----------------------|-------------------|
| 48 - P1.5 | TACLK | TACLK | Timer | NA | |
| | ACLK | ACLK | | | |
| | SMCLK | SMCLK | | | |
| 48 - P1.5 | $\overline{\text{TACLK}}$ | INCLK | | | |
| 53 - P1.0 | TA0 | CCI0A | CCR0 | TA0 | 53 - P1.0 |
| 52 - P1.1 | TA0 | CCI0B | | | |
| | DV _{SS} | GND | | | |
| | DV _{CC} | V _{CC} | | | |
| 51 - P1.2 | TA1 | CCI1A | CCR1 | TA1 | 51 - P1.2 |
| 51 - P1.2 | TA1 | CCI1B | | | |
| | DV _{SS} | GND | | | |
| | DV _{CC} | V _{CC} | | | |
| 45 - P2.0 | TA2 | CCI2A | CCR2 | TA2 | 45 - P2.0 |
| | ACLK (internal) | CCI2B | | | |
| | DV _{SS} | GND | | | |
| | DV _{CC} | V _{CC} | | | |

6.9.8 USART0

The MSP430FE42x devices have one hardware universal synchronous/asynchronous receive transmit (USART0) peripheral module that is used for serial data communication. The USART supports synchronous SPI (3- or 4-pin) and asynchronous UART communication protocols, using double-buffered transmit and receive channels.

6.9.9 ESP430CE1

The ESP430CE1 module integrates a hardware multiplier, three independent 16-bit Sigma-Delta ADCs (SD16) and an embedded signal processor (ESP430). The ESP430CE1 module measures 2- or 3-wire single-phase energy and automatically calculates parameters which are made available to the MSP430 CPU. The module can be calibrated and initialized to accurately calculate energy, power factor, and other values for a wide range of metering sensor configurations.

6.9.10 Peripheral File Map

Table 6-11 and Table 6-12 list the peripheral registers with their addresses.

Table 6-11. Peripherals With Word Access

| MODULE | REGISTER NAME | ACRONYM | ADDRESS |
|------------------------------------|--|---------|---------|
| Watchdog | Watchdog timer control | WDTCTL | 0120h |
| Timer_A3 | Timer0_A interrupt vector | TA0IV | 012Eh |
| | Timer0_A control | TACTL0 | 0160h |
| | Capture/compare control 0 | TACCTL0 | 0162h |
| | Capture/compare control 1 | TACCTL1 | 0164h |
| | Capture/compare control 2 | TACCTL2 | 0166h |
| | Reserved | | 0168h |
| | Reserved | | 016Ah |
| | Reserved | | 016Ch |
| | Reserved | | 016Eh |
| | Timer_A counter | TA0R | 0170h |
| | Capture/compare 0 | TACCR0 | 0172h |
| | Capture/compare 1 | TACCR1 | 0174h |
| | Capture/compare 2 | TACCR2 | 0176h |
| | Reserved | | 0178h |
| | Reserved | | 017Ah |
| | Reserved | | 017Ch |
| Reserved | | 017Eh | |
| Hardware Multiplier ⁽¹⁾ | Sum extend | SUMEXT | 013Eh |
| | Result high word | RESHI | 013Ch |
| | Result low word | RESLO | 013Ah |
| | Second operand | OP2 | 0138h |
| | Multiply signed + accumulate/operand 1 | MACS | 0136h |
| | Multiply + accumulate/operand 1 | MAC | 0134h |
| | Multiply signed/operand 1 | MPYS | 0132h |
| | Multiply unsigned/operand 1 | MPY | 0130h |
| Flash | Flash control 3 | FCTL3 | 012Ch |
| | Flash control 2 | FCTL2 | 012Ah |
| | Flash control 1 | FCTL1 | 0128h |

(1) This module is contained within ESP430CE1. Registers are not accessible when ESP430 is active. ESP430 must be disabled or suspended to allow CPU access to these modules.

Table 6-11. Peripherals With Word Access (continued)

| MODULE | REGISTER NAME | ACRONYM | ADDRESS |
|---|-----------------------------|-----------|---------|
| SD16 ⁽¹⁾ (also see Table 6-12) | General control | SD16CTL | 0100h |
| | Channel 0 control | SD16CCTL0 | 0102h |
| | Channel 1 control | SD16CCTL1 | 0104h |
| | Channel 2 control | SD16CCTL2 | 0106h |
| | Reserved | | 0108h |
| | Reserved | | 010Ah |
| | Reserved | | 010Ch |
| | Reserved | | 010Eh |
| | Interrupt vector word | SD16IV | 0110h |
| | Channel 0 conversion memory | SD16MEM0 | 0112h |
| | Channel 1 conversion memory | SD16MEM1 | 0114h |
| | Channel 2 conversion memory | SD16MEM2 | 0116h |
| | Reserved | | 0118h |
| | Reserved | | 011Ah |
| | Reserved | | 011Ch |
| | Reserved | | 011Eh |
| ESP430 (ESP430CE1) | ESP430 control | ESPCTL | 0150h |
| | Mailbox control | MBCTL | 0152h |
| | Mailbox in 0 | MBIN0 | 0154h |
| | Mailbox in 1 | MBIN1 | 0156h |
| | Mailbox out 0 | MBOUT0 | 0158h |
| | Mailbox out 1 | MBOUT1 | 015Ah |
| | ESP430 return value 0 | RET0 | 01C0h |
| | ⋮ | ⋮ | ⋮ |
| | ESP430 return value 31 | RET31 | 01FEh |

Table 6-12. Peripherals With Byte Access

| MODULE | REGISTER NAME | ACRONYM | ADDRESS |
|---|-------------------------|------------|---------|
| SD16 ⁽¹⁾ (also see Table 6-11) | Channel 0 input control | SD16INCTL0 | 0B0h |
| | Channel 1 input control | SD16INCTL1 | 0B1h |
| | Channel 2 input control | SD16INCTL2 | 0B2h |
| | Reserved | | 0B3h |
| | Reserved | | 0B4h |
| | Reserved | | 0B5h |
| | Reserved | | 0B6h |
| | Reserved | | 0B7h |
| | Channel 0 preload | SD16PRE0 | 0B8h |
| | Channel 1 preload | SD16PRE1 | 0B9h |
| | Channel 2 preload | SD16PRE2 | 0BAh |
| | Reserved | | 0BBh |
| | Reserved | | 0BCh |
| | Reserved | | 0BDh |
| | Reserved | | 0BEh |
| | Reserved | | 0BFh |

(1) This module is contained within ESP430CE1. Registers are not accessible when ESP430 is active. ESP430 must be disabled or suspended to allow CPU access to these modules.

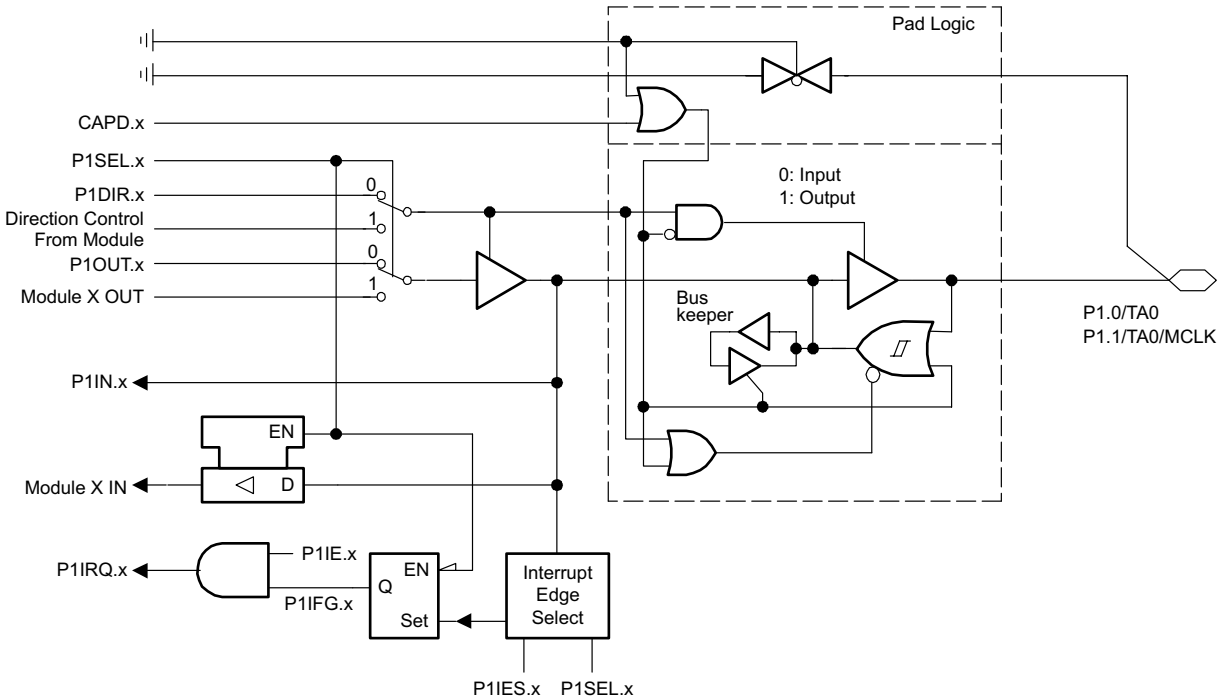
Table 6-12. Peripherals With Byte Access (continued)

| MODULE | REGISTER NAME | ACRONYM | ADDRESS |
|-------------------|-----------------------------------|----------|---------|
| LCD | LCD memory 20 | LCDM20 | 0A4h |
| | ⋮ | ⋮ | ⋮ |
| | LCD memory 16 | LCDM16 | 0A0h |
| | LCD memory 15 | LCDM15 | 09Fh |
| | ⋮ | ⋮ | ⋮ |
| | LCD memory 1 | LCDM1 | 091h |
| | LCD control and mode | LCDCTL | 090h |
| USART0 | Transmit buffer | U0TXBUF | 077h |
| | Receive buffer | U0RXBUF | 076h |
| | Baud rate 1 | U0BR1 | 075h |
| | Baud rate 0 | U0BR0 | 074h |
| | Modulation control | U0MCTL | 073h |
| | Receive control | U0RCTL | 072h |
| | Transmit control | U0TCTL | 071h |
| | USART control | U0CTL | 070h |
| Brownout, SVS | SVS control register | SVSCTL | 056h |
| FLL+ Clock | FLL+ control 1 | FLL_CTL1 | 054h |
| | FLL+ control 0 | FLL_CTL0 | 053h |
| | System clock frequency control | SCFQCTL | 052h |
| | System clock frequency integrator | SCFI1 | 051h |
| | System clock frequency integrator | SCFI0 | 050h |
| Basic Timer1 | BT counter 2 | BTCNT2 | 047h |
| | BT counter 1 | BTCNT1 | 046h |
| | BT control | BTCTL | 040h |
| Port P2 | Port P2 selection | P2SEL | 02Eh |
| | Port P2 interrupt enable | P2IE | 02Dh |
| | Port P2 interrupt-edge select | P2IES | 02Ch |
| | Port P2 interrupt flag | P2IFG | 02Bh |
| | Port P2 direction | P2DIR | 02Ah |
| | Port P2 output | P2OUT | 029h |
| | Port P2 input | P2IN | 028h |
| Port P1 | Port P1 selection | P1SEL | 026h |
| | Port P1 interrupt enable | P1IE | 025h |
| | Port P1 interrupt-edge select | P1IES | 024h |
| | Port P1 interrupt flag | P1IFG | 023h |
| | Port P1 direction | P1DIR | 022h |
| | Port P1 output | P1OUT | 021h |
| | Port P1 input | P1IN | 020h |
| Special Functions | SFR module enable 2 | ME2 | 005h |
| | SFR module enable 1 | ME1 | 004h |
| | SFR interrupt flag 2 | IFG2 | 003h |
| | SFR interrupt flag 1 | IFG1 | 002h |
| | SFR interrupt enable 2 | IE2 | 001h |
| | SFR interrupt enable 1 | IE1 | 000h |

6.10 Input/Output Diagrams

6.10.1 Port P1 (P1.0 and P1.1) Input/Output With Schmitt Trigger

Figure 6-8 shows the port diagram. Table 6-13 summarizes the selection of the port function.



NOTE: $0 \leq x \leq 1$. Port function is active if CAPD.x = 0.

Figure 6-8. Port P1 (P1.0 and P1.1) Diagram

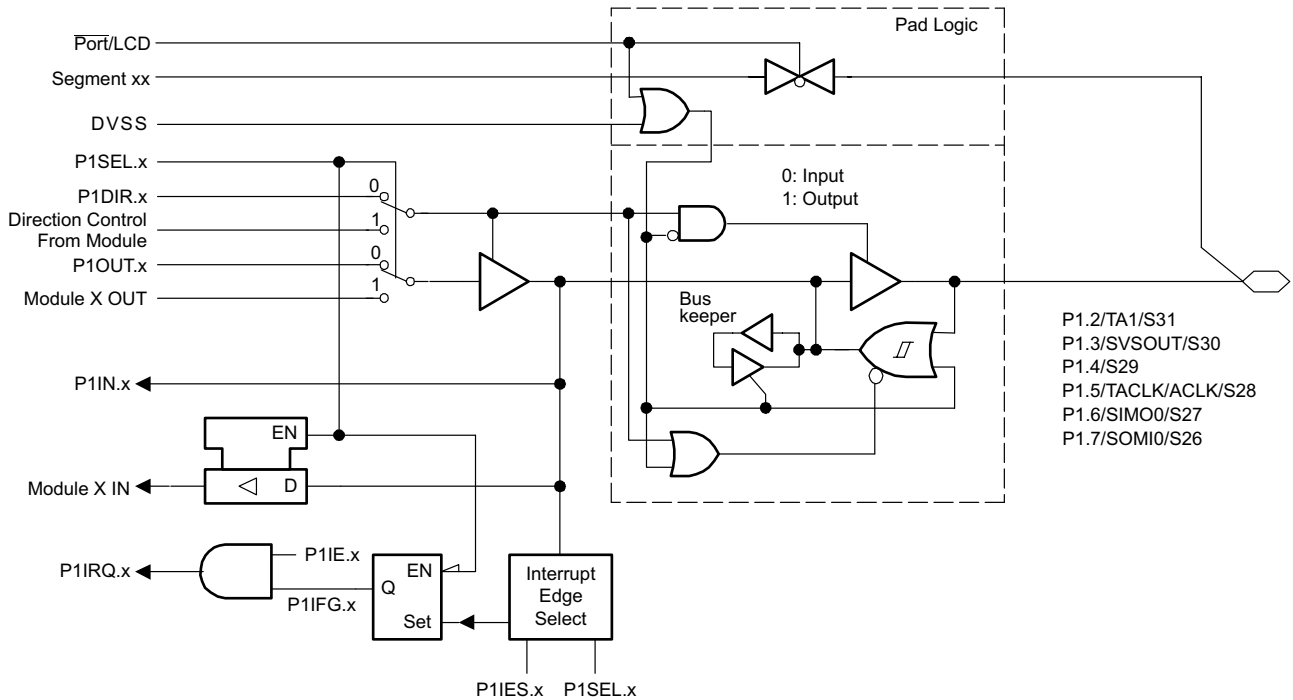
Table 6-13. Port P1 (P1.0 and P1.1) Pin Function

| P1SEL.x | PnDIR.x | DIRECTION CONTROL FROM MODULE | P1OUT.x | MODULE X OUT | P1IN.x | MODULE X IN | P1IE.x | P1IFG.x | P1IES.x | CAPD.x |
|---------|---------|-------------------------------|---------|--------------------------|--------|----------------------|--------|---------|---------|--------|
| P1SEL.0 | P1DIR.0 | P1DIR.0 | P1OUT.0 | Out0 Sig. ⁽¹⁾ | P1IN.0 | CCI0A ⁽¹⁾ | P1IE.0 | P1IFG.0 | P1IES.0 | DVSS |
| P1SEL.1 | P1DIR.1 | P1DIR.1 | P1OUT.1 | MCLK | P1IN.1 | CCI0B ⁽¹⁾ | P1IE.1 | P1IFG.1 | P1IES.1 | DVSS |

(1) Timer_A3

6.10.2 Port P1 (P1.2 to P1.7) Input/Output With Schmitt Trigger

Figure 6-9 shows the port diagram. Table 6-14 summarizes the selection of the port function.



NOTE: $2 \leq x \leq 7$. Port function is active if $\overline{\text{Port/LCD}} = 0$.

Figure 6-9. Port P1 (P1.2 to P1.7) Diagram

Table 6-14. Port P1 (P1.2 to P1.7) Pin Functions

| P1SEL.x | P1DIR.x | DIRECTION CONTROL FROM MODULE | P1OUT.x | MODULE X OUT | P1IN.x | MODULE X IN | P1IE.x | P1IFG.x | P1IES.x | $\overline{\text{Port/LCD}}$ | SEGMENT |
|---------|---------|-------------------------------|---------|--------------------------|--------|-------------------------|--------|---------|---------|-----------------------------------|---------|
| P1SEL.2 | P1DIR.2 | P1DIR.2 | P1OUT.2 | Out1 Sig. ⁽¹⁾ | P1IN.2 | CC1A† | P1IE.2 | P1IFG.2 | P1IES.2 | 0: LCDPx < 05h, 1: LCDPx ≥ 05h | S31 |
| P1SEL.3 | P1DIR.3 | P1DIR.3 | P1OUT.3 | SVSOUT | P1IN.3 | unused | P1IE.3 | P1IFG.3 | P1IES.3 | | S30 |
| P1SEL.4 | P1DIR.4 | P1DIR.4 | P1OUT.4 | DVSS | P1IN.4 | unused | P1IE.4 | P1IFG.4 | P1IES.4 | | S29 |
| P1SEL.5 | P1DIR.5 | P1DIR.5 | P1OUT.5 | ACLK | P1IN.5 | TACLK ⁽¹⁾ | P1IE.5 | P1IFG.5 | P1IES.5 | 0: LCDPx < 04h, 1: LCDPx ≥ 04h | S28 |
| P1SEL.6 | P1DIR.6 | DCM_SIMO | P1OUT.6 | SIMO0(o) ⁽²⁾ | P1IN.6 | SIMO0(i) ⁽²⁾ | P1IE.6 | P1IFG.6 | P1IES.6 | | S27 |
| P1SEL.7 | P1DIR.7 | DCM_SOMI | P1OUT.7 | SOMI0(o) ⁽²⁾ | P1IN.7 | SOMI0(i) ⁽²⁾ | P1IE.7 | P1IFG.7 | P1IES.7 | 0: LCDPx < 04h, 1: LCDPx ≥ 04h | S26 |

(1) Timer_A3

(2) USART0 (also see Figure 6-10)

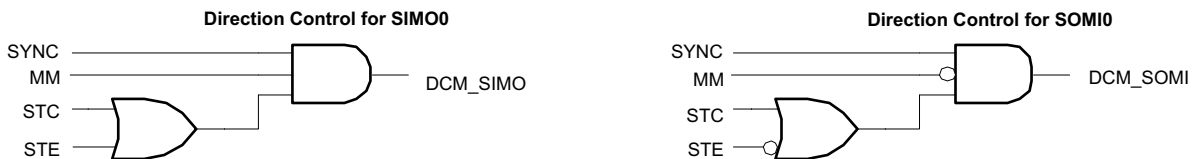
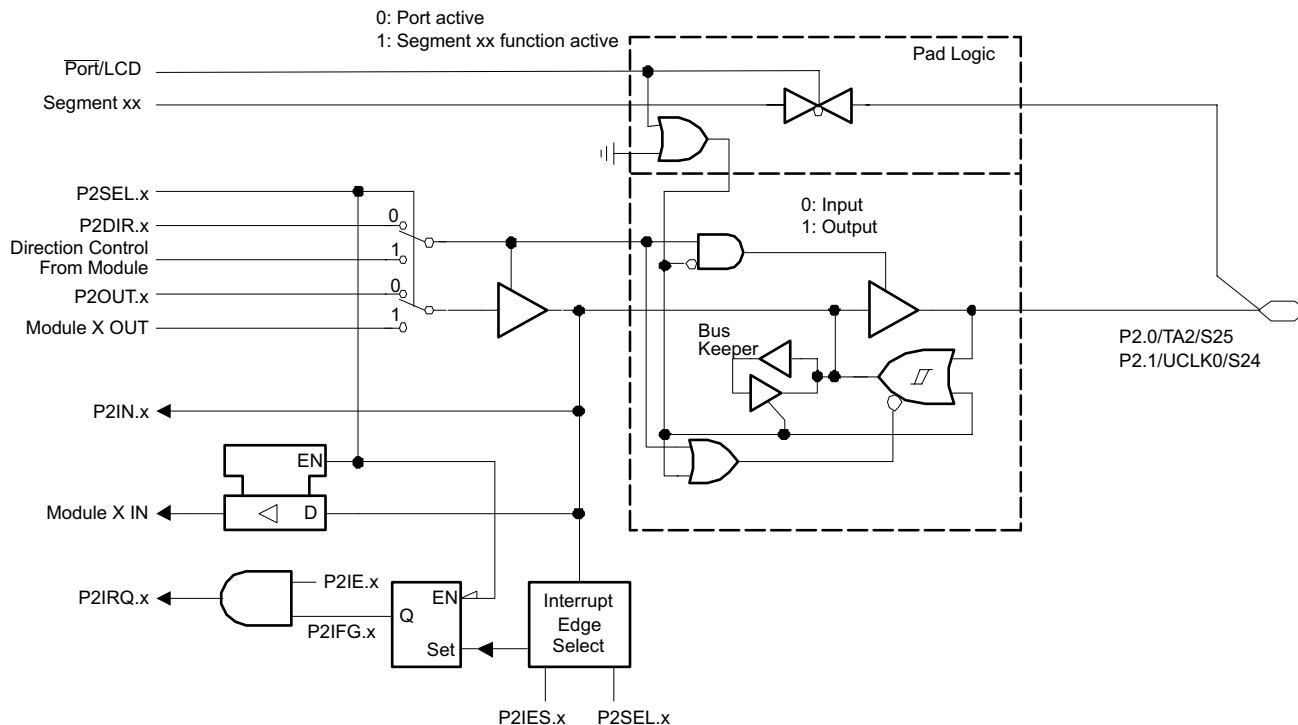


Figure 6-10. Direction Control for SIMO0 and SOMI0

6.10.3 Port P2 (P2.0 and P2.1) Input/Output With Schmitt Trigger

Figure 6-11 shows the port diagram. Table 6-15 summarizes the selection of the port function.



NOTE: $0 \leq x \leq 1$. Port function is active if $\overline{\text{Port/LCD}} = 0$.

Figure 6-11. Port P2 (P2.0 and P2.1) Diagram

Table 6-15. Port P2 (P2.0 and P2.1) Pin Functions

| P2SEL.x | P2DIR.x | DIRECTION CONTROL FROM MODULE | P2OUT.x | MODULE X OUT | P2IN.x | MODULE X IN | P2IE.x | P2IFG.x | P2IES.x | $\overline{\text{Port/LCD}}$ | SEGMENT |
|---------|---------|-------------------------------|---------|--------------------------|--------|-------------------------|--------|---------|---------|-----------------------------------|---------|
| P2SEL.0 | P2DIR.0 | P2DIR.0 | P2OUT.0 | Out2 Sig. ⁽¹⁾ | P2IN.0 | CCI2A ⁽¹⁾ | P2IE.0 | P2IFG.0 | P2IES.0 | 0: LCDPx < 04h, 1: LCDPx ≥ 04h | S25 |
| P2SEL.1 | P2DIR.1 | DCM_UCLK | P2OUT.1 | UCLK0(o) ⁽²⁾ | P2IN.1 | UCLK0(i) ⁽²⁾ | P2IE.1 | P2IFG.1 | P2IES.1 | | S24 |

(1) Timer_A3

(2) USART0 (also see Figure 6-12)

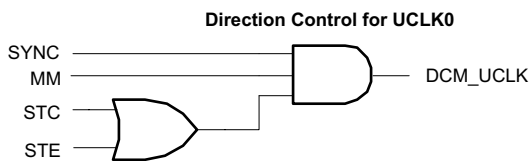


Figure 6-12. Direction Control for UCLK0

6.10.4 Port P2 (P2.2 to P2.5) Input/Output With Schmitt Trigger

Figure 6-13 shows the port diagram. Table 6-16 summarizes the selection of the port function.

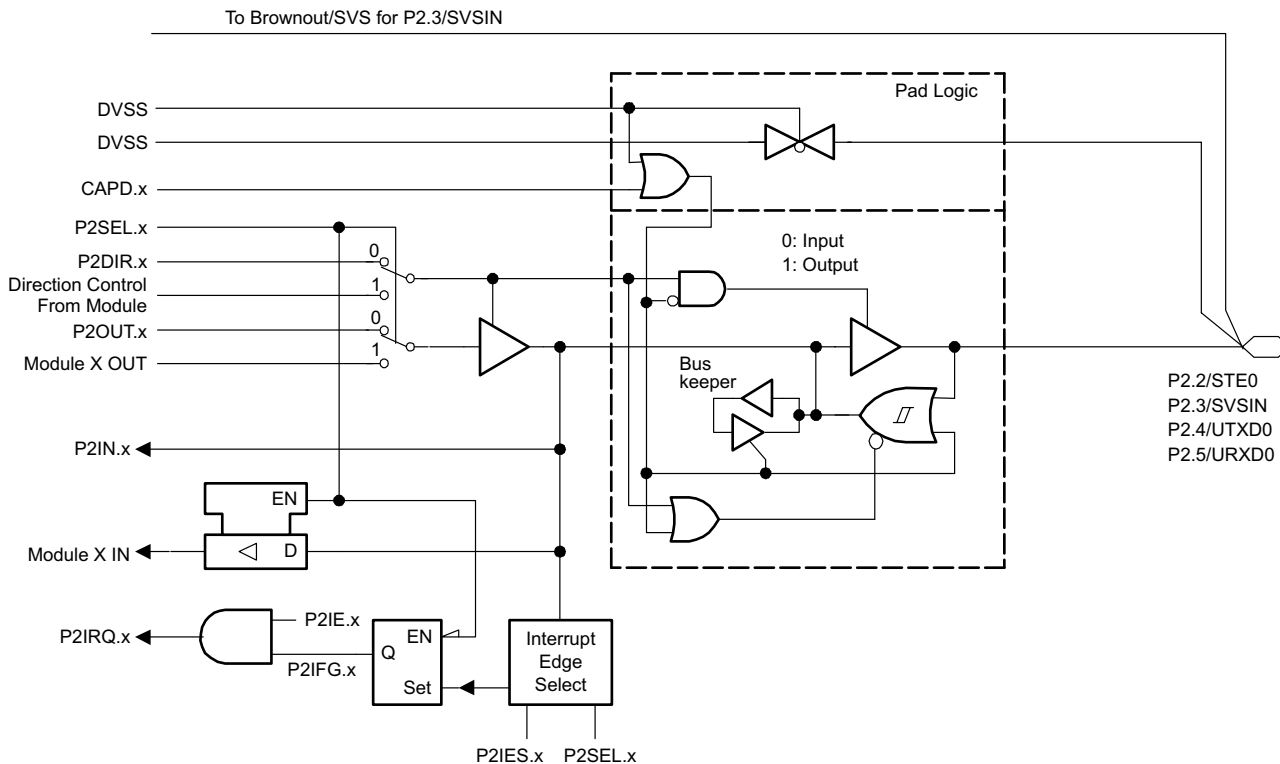


Figure 6-13. Port P2 (P2.2 to P2.5) Diagram

Table 6-16. Port P2 (P2.2 to P2.5) Pin Functions

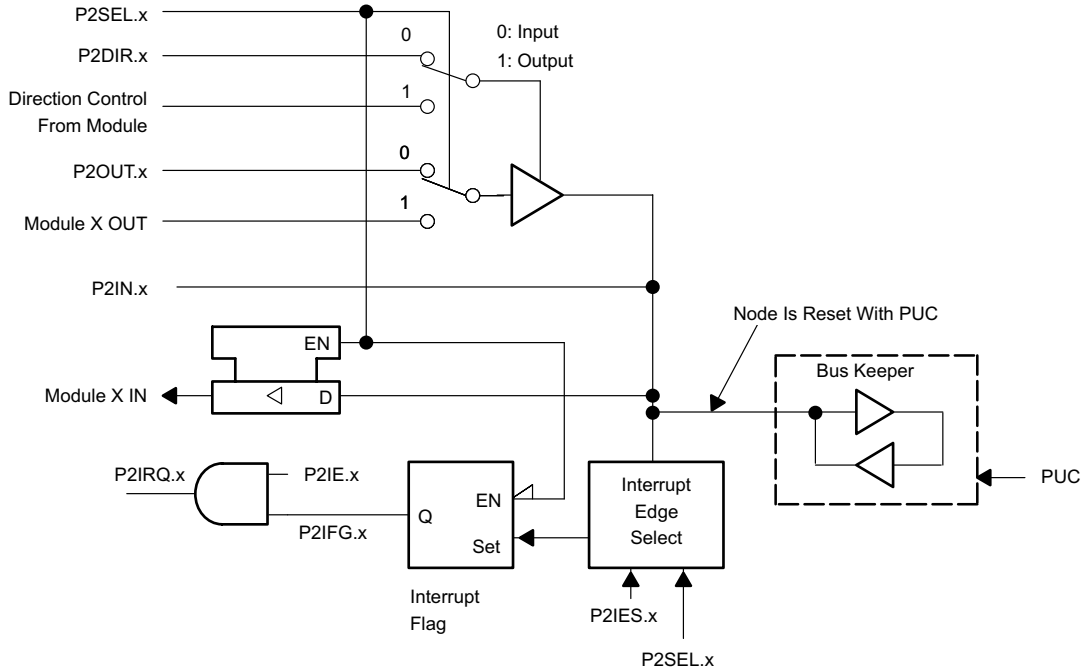
| P2SEL.x | P2DIR.x | DIRECTION CONTROL FROM MODULE | P2OUT.x | MODULE X OUT | P2IN.x | MODULE X IN | P2IE.x | P2IFG.x | P2IES.x | CAPD.x |
|---------|---------|-------------------------------|---------|----------------------|--------|----------------------|--------|---------|---------|-----------------------|
| P2SEL.2 | P2DIR.2 | DVSS | P2OUT.2 | DVSS | P2IN.2 | STE0 ⁽¹⁾ | P2IE.2 | P2IFG.2 | P2IES.2 | DVSS |
| P2SEL.3 | P2DIR.3 | P2DIR.3 | P2OUT.3 | DVSS | P2IN.3 | Unused | P2IE.3 | P2IFG.3 | P2IES.3 | SVSCTL VLD = 1111b |
| P2SEL.4 | P2DIR.4 | DVCC | P2OUT.4 | UTXD0 ⁽¹⁾ | P2IN.4 | Unused | P2IE.4 | P2IFG.4 | P2IES.4 | DVSS |
| P2SEL.5 | P2DIR.5 | DVSS | P2OUT.5 | DVSS | P2IN.5 | URXD0 ⁽¹⁾ | P2IE.5 | P2IFG.5 | P2IES.5 | DVSS |

(1) USART0

6.10.5 Port P2 (P2.6 and P2.7) Unbonded GPIOs

Unbonded GPIOs P2.6 and P2.7 can be used as interrupt flags. Only software can affect the interrupt flags. They work as software interrupts.

Figure 6-14 shows the port diagram. Table 6-17 summarizes the selection of the port function.



NOTE: x = Bit/identifier, 6 or 7 for Port P2 without external pins

Figure 6-14. Port P2 (P2.6 and P2.7) Diagram

Table 6-17. Port P2 (P2.6 and P2.7) Pin Functions

| P2SEL.x | P2DIR.x | DIRECTION CONTROL FROM MODULE | P2OUT.x | MODULE X OUT | P2IN.x | MODULE X IN | P2IE.x | P2IFG.x | P2IES.x |
|---------|---------|-------------------------------|---------|--------------|--------|-------------|--------|---------|---------|
| P2SEL.6 | P2DIR.6 | P2DIR.6 | P2OUT.6 | DVSS | P2IN.6 | Unused | P2IE.6 | P2IFG.6 | P2IES.6 |
| P2SEL.7 | P2DIR.7 | P2DIR.7 | P2OUT.7 | DVSS | P2IN.7 | Unused | P2IE.7 | P2IFG.7 | P2IES.7 |

6.10.6 JTAG Pins TMS, TCK, TDI/TCLK, TDO/TDI, Input/Output With Schmitt-Trigger or Output

Figure 6-15 shows the port diagram.

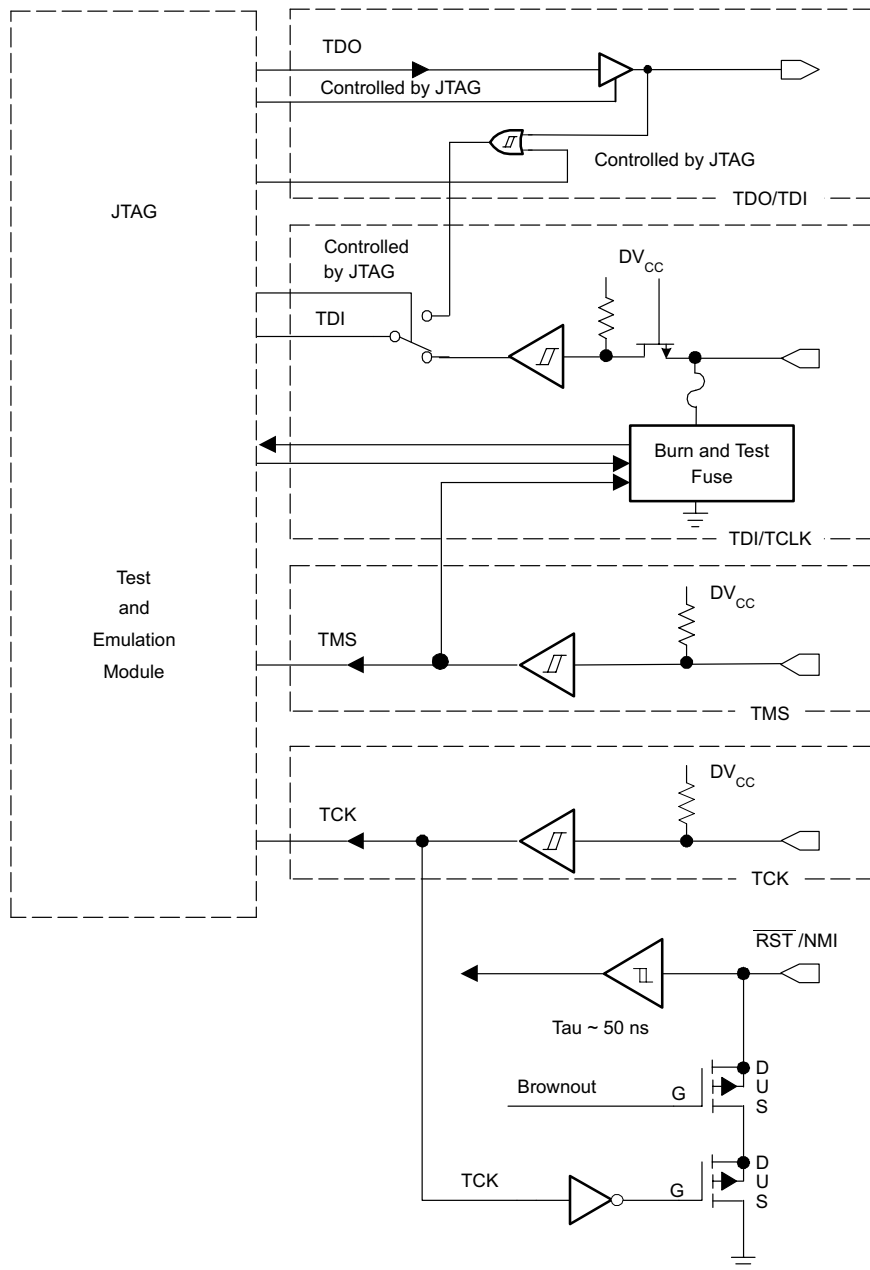


Figure 6-15. JTAG Pins Diagram

6.10.7 JTAG Fuse Check Mode

MSP430 devices that have the fuse on the TDI/TCLK terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current (I_{TF}) of 1.8 mA at 3 V can flow from the TDI/TCLK pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if the TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current flows only when the fuse check mode is active and the TMS pin is in a low state (see Figure 6-16). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition). The JTAG pins are terminated internally and therefore do not require external termination.

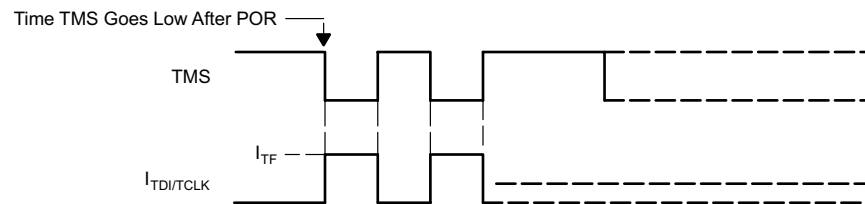


Figure 6-16. Fuse Check Mode Current

7 Device and Documentation Support

7.1 Getting Started and Next Steps

For more information on the MSP430 family of devices and the tools and libraries that are available to help with your development, visit the [Getting Started](#) page.

7.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP430 MCU devices and support tools. Each MSP430 MCU commercial family member has one of three prefixes: MSP, PMS, or XMS. TI recommends two of three possible prefix designators for its support tools: MSP and MSPX. These prefixes represent evolutionary stages of product development from engineering prototypes (with XMS for devices and MSPX for tools) through fully qualified production devices and tools (with MSP for devices and MSP for tools).

Device development evolutionary flow:

XMS – Experimental device that is not necessarily representative of the final electrical specifications of the device

MSP – Fully qualified production device

Support tool development evolutionary flow:

MSPX – Development-support product that has not yet completed TI's internal qualification testing.

MSP – Fully-qualified development-support product

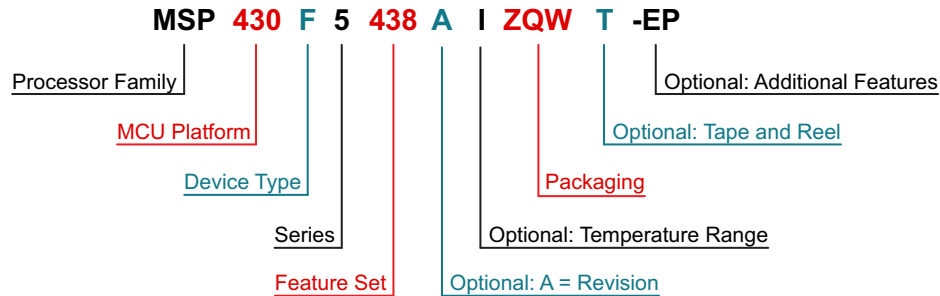
XMS devices and MSPX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices and MSP development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PZP) and temperature range (for example, T). [Figure 7-1](#) provides a legend for reading the complete device name for any family member.



| | | |
|--------------------------------------|--|---|
| Processor Family | CC = Embedded RF Radio MSP = Mixed-Signal Processor XMS = Experimental Silicon PMS = Prototype Device | |
| MCU Platform | 430 = MSP430 low-power microcontroller platform | |
| Device Type | Memory Type C = ROM F = Flash FR = FRAM G = Flash or FRAM (Value Line) L = No Nonvolatile Memory | Specialized Application AFE = Analog Front End BT = Preprogrammed with <i>Bluetooth</i> BQ = Contactless Power CG = ROM Medical FE = Flash Energy Meter FG = Flash Medical FW = Flash Electronic Flow Meter |
| Series | 1 Series = Up to 8 MHz 2 Series = Up to 16 MHz 3 Series = Legacy 4 Series = Up to 16 MHz with LCD | 5 Series = Up to 25 MHz 6 Series = Up to 25 MHz with LCD 0 = Low-Voltage Series |
| Feature Set | Various Levels of Integration Within a Series | |
| Optional: A = Revision | N/A | |
| Optional: Temperature Range | S = 0°C to 50°C C = 0°C to 70°C I = -40°C to 85°C T = -40°C to 105°C | |
| Packaging | http://www.ti.com/packaging | |
| Optional: Tape and Reel | T = Small Reel R = Large Reel No Markings = Tube or Tray | |
| Optional: Additional Features | -EP = Enhanced Product (-40°C to 105°C) -HT = Extreme Temperature Parts (-55°C to 150°C) -Q1 = Automotive Q100 Qualified | |

NOTE: This figure does not represent a complete list of the available features and options, and it does not indicate that all of these features and options are available for a given device or family.

Figure 7-1. Device Nomenclature – Part Number Decoder

7.3 Tools and Software

Table 7-1 lists the debug features supported by the MSP430FE42x microcontrollers. See the [Code Composer Studio for MSP430 User's Guide](#) for details on the available features.

Table 7-1. Hardware Features

| MSP430 ARCHITECTURE | 4-WIRE JTAG | 2-WIRE JTAG | BREAK-POINTS (N) | RANGE BREAK-POINTS | CLOCK CONTROL | STATE SEQUENCER | TRACE BUFFER |
|---------------------|-------------|-------------|------------------|--------------------|---------------|-----------------|--------------|
| MSP430 | Yes | No | 3 | No | Global | No | No |

Design Kits and Evaluation Modules

64-pin Target Development Board and MSP-FET Programmer Bundle - MSP430F1x, MSP430F2x, MSP430F4x MCUs The MSP-FET430U64 is a powerful flash emulation tool that includes the hardware and software required to quickly begin application development on the MSP430 MCU. It includes a ZIF socket target board (MSP-TS430PM64) and a USB debugging interface (MSP-FET) used to program and debug the MSP430 in-system through the JTAG interface or the pin-saving Spy-Bi-Wire (2-wire JTAG) protocol. The flash memory can be erased and programmed in seconds with only a few keystrokes, and because the MSP430 flash is ultra-low power, no external power supply is required.

Software

MSP430x41x, MSP430F42x Code Examples C Code examples are available for every MSP device that configures each of the integrated peripherals for various application needs.

Capacitive Touch Software Library Free C libraries for enabling capacitive touch capabilities on MSP430 MCUs. The MSP430 MCU version of the library features several capacitive touch implementations including the RO and RC method.

MSPWare Software MSPWare software is a collection of code examples, data sheets, and other design resources for all MSP devices delivered in a convenient package. In addition to providing a complete collection of existing MSP design resources, MSPWare software also includes a high-level API called MSP Driver Library. This library makes it easy to program MSP hardware. MSPWare software is available as a component of CCS or as a stand-alone package.

MSP Driver Library The abstracted API of MSP Driver Library provides easy-to-use function calls that free you from directly manipulating the bits and bytes of the MSP430 hardware. Thorough documentation is delivered through a helpful API Guide, which includes details on each function call and the recognized parameters. Developers can use Driver Library functions to write complete projects with minimal overhead.

MSP EnergyTrace Technology EnergyTrace technology for MSP430 microcontrollers is an energy-based code analysis tool that measures and displays the energy profile of the application and helps to optimize it for ultra-low power consumption.

ULP (Ultra-Low Power) Advisor ULP Advisor™ software is a tool for guiding developers to write more efficient code to fully use the unique ultra-low-power features of MSP and MSP432 microcontrollers. Aimed at both experienced and new microcontroller developers, ULP Advisor checks your code against a thorough ULP checklist to help minimize the energy consumption of your application. At build time, ULP Advisor provides notifications and remarks to highlight areas of your code that can be further optimized for lower power.

Fixed Point Math Library for MSP The MSP IQmath and Qmath Libraries are a collection of highly optimized and high-precision mathematical functions for C programmers to seamlessly port a floating-point algorithm into fixed-point code on MSP430 and MSP432 devices. These routines are typically used in computationally intensive real-time applications where optimal execution speed, high accuracy, and ultra-low energy are critical. By using the IQmath and Qmath libraries, it is possible to achieve execution speeds considerably faster and energy consumption considerably lower than equivalent code written using floating-point math.

Development Tools

Code Composer Studio™ Integrated Development Environment for MSP Microcontrollers Code Composer Studio (CCS) integrated development environment (IDE) supports all MSP microcontroller devices. CCS comprises a suite of embedded software utilities used to develop and debug embedded applications. CCS includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features.

MSPWare Software MSPWare software is a collection of code examples, data sheets, and other design resources for all MSP devices delivered in a convenient package. In addition to providing a complete collection of existing MSP design resources, MSPWare software also includes a high-level API called MSP Driver Library. This library makes it easy to program MSP hardware. MSPWare software is available as a component of CCS or as a stand-alone package.

Command-Line Programmer MSP Flasher is an open-source shell-based interface for programming MSP microcontrollers through a FET programmer or eZ430 using JTAG or Spy-Bi-Wire (SBW) communication. MSP Flasher can download binary files (.txt or .hex) directly to the MSP microcontroller without an IDE.

MSP MCU Programmer and Debugger The MSP-FET is a powerful emulation development tool – often called a debug probe – which lets users quickly begin application development on MSP low-power MCUs. Creating MCU software usually requires downloading the resulting binary program to the MSP device for validation and debugging.

MSP-GANG Production Programmer The MSP Gang Programmer is an MSP430 or MSP432 device programmer that can program up to eight identical MSP430 or MSP432 flash or FRAM devices at the same time. The MSP Gang Programmer connects to a host PC using a standard RS-232 or USB connection and provides flexible programming options that let the user fully customize the process.

7.4 Documentation Support

The following documents describe the MSP430FE42x MCUs. Copies of these documents are available on the Internet at www.ti.com.

Receiving Notification of Document Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com (see [Section 7.5](#) for links to product folders). In the upper right corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

Errata

MSP430FE427 Device Erratasheet Describes the known exceptions to the functional specifications for each silicon revision of this device.

MSP430FE425 Device Erratasheet Describes the known exceptions to the functional specifications for each silicon revision of this device.

MSP430FE423 Device Erratasheet Describes the known exceptions to the functional specifications for each silicon revision of this device.

User's Guides

MSP430x4xx Family User's Guide Detailed description of all modules and peripherals available in this device family.

ESP430CE1, ESP430CE1A, ESP430CE1B Peripheral Modules User's Guide The ESP430CE1/1A/1B module incorporates the SD16, hardware multiplier, and ESP430 embedded processor engine for use in single-phase energy metering applications.

Code Composer Studio v6.1 for MSP430 User's Guide This manual describes the use of TI Code Composer Studio IDE v6.1 (CCS v6.1) with the MSP430 ultra-low-power microcontrollers. This document applies only for the Windows® version of the Code Composer Studio IDE. The Linux® version is similar and, therefore, is not described separately.

IAR Embedded Workbench Version 3+ for MSP430 User's Guide This manual describes the use of IAR Embedded Workbench (EW430) with the MSP430 ultra-low-power microcontrollers.

MSP430 Programming With the JTAG Interface This document describes the functions that are required to erase, program, and verify the memory module of the MSP430 flash-based and FRAM-based microcontroller families using the JTAG communication port. In addition, it describes how to program the JTAG access security fuse that is available on all MSP430 devices. This document describes device access using both the standard 4-wire JTAG interface and the 2-wire JTAG interface, which is also referred to as Spy-Bi-Wire (SBW).

MSP430 Hardware Tools User's Guide This manual describes the hardware of the TI MSP-FET430 Flash Emulation Tool (FET). The FET is the program development tool for the MSP430 ultra-low-power microcontroller. Both available interface types, the parallel port interface and the USB interface, are described.

Application Reports

MSP430 32-kHz Crystal Oscillators Selection of the right crystal, correct load circuit, and proper board layout are important for a stable crystal oscillator. This application report summarizes crystal oscillator function and explains the parameters to select the correct crystal for MSP430 ultra-low-power operation. In addition, hints and examples for correct board layout are given. The document also contains detailed information on the possible oscillator tests to ensure stable oscillator operation in mass production.

MSP430 System-Level ESD Considerations System-Level ESD has become increasingly demanding with silicon technology scaling towards lower voltages and the need for designing cost-effective and ultra-low-power components. This application report addresses three different ESD topics to help board designers and OEMs understand and design robust system-level designs.

Designing With MSP430 and Segment LCDs Segment liquid crystal displays (LCDs) are needed to provide information to users in a wide variety of applications from smart meters to electronic shelf labels (ESL) to medical equipment. Several MSP430™ microcontroller families include built-in low-power LCD driver circuitry that allows the MSP430 MCU to directly control the segmented LCD glass. This application note helps explain how segmented LCDs work, the different features of the various LCD modules across the MSP430 MCU family, LCD hardware layout tips, guidance on writing efficient and easy-to-use LCD driver software, and an overview of the portfolio of MSP430 devices that include different LCD features to aid in device selection.

Understanding MSP430 Flash Data Retention The MSP430 family of microcontrollers, as part of its broad portfolio, offers both read-only memory (ROM)-based and flash-based devices. Understanding the MSP430 flash is extremely important for efficient, robust, and reliable system design. Data retention is one of the key aspects to flash reliability. In this application report, data retention for the MSP430 flash is discussed in detail and the effect of temperature is given primary importance.

Interfacing the 3-V MSP430 to 5-V Circuits The interfacing of the 3-V MSP430x1xx and MSP430x4xx microcontroller families to circuits with a supply of 5 V or higher is shown. Input, output and I/O interfaces are given and explained. Worse-case design equations are provided, where necessary. Some simple power supplies generating both voltages are shown, too.

Implementing An Electronic Watt-Hour Meter With MSP430FE42x(A)/FE42x2 This report shows how to implement an electronic watt-hour meter with the MSP430FE42x(A)/FE42x2 devices. It contains guidelines and recommendations for use of the MSP430FE42x(A) and MSP430FE42x2 devices. In addition, a reference board with hardware details and software examples are included.

Efficient Multiplication and Division Using MSP430 Multiplication and division in the absence of a hardware multiplier require many instruction cycles, especially in C. This report discusses a method that does not need a hardware multiplier and can perform multiplication and division with only shift and add instructions. The method described in this application report is based on Horner's method.

7.5 Related Links

[Table 7-2](#) lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 7-2. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|-------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| MSP430FE427 | Click here | Click here | Click here | Click here | Click here |
| MSP430FE425 | Click here | Click here | Click here | Click here | Click here |
| MSP430FE423 | Click here | Click here | Click here | Click here | Click here |

7.6 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

[TI E2E™ Community](#)

TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

[TI Embedded Processors Wiki](#)

Texas Instruments Embedded Processors Wiki. Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

7.7 Trademarks

MSP430, ULP Advisor, Code Composer Studio, E2E are trademarks of Texas Instruments.

Linux is a registered trademark of Linus Torvalds.

Windows is a registered trademark of Microsoft Corporation.

7.8 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.9 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

7.10 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| MSP430FE423IPM | ACTIVE | LQFP | PM | 64 | 160 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430FE423 | Samples |
| MSP430FE423IPMR | ACTIVE | LQFP | PM | 64 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430FE423 | Samples |
| MSP430FE425IPM | ACTIVE | LQFP | PM | 64 | 160 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430FE425 | Samples |
| MSP430FE425IPMR | ACTIVE | LQFP | PM | 64 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430FE425 | Samples |
| MSP430FE427IPM | ACTIVE | LQFP | PM | 64 | 160 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430FE427 | Samples |
| MSP430FE427IPMR | ACTIVE | LQFP | PM | 64 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | M430FE427 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430FE423IPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430FE425IPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| MSP430FE427IPMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |

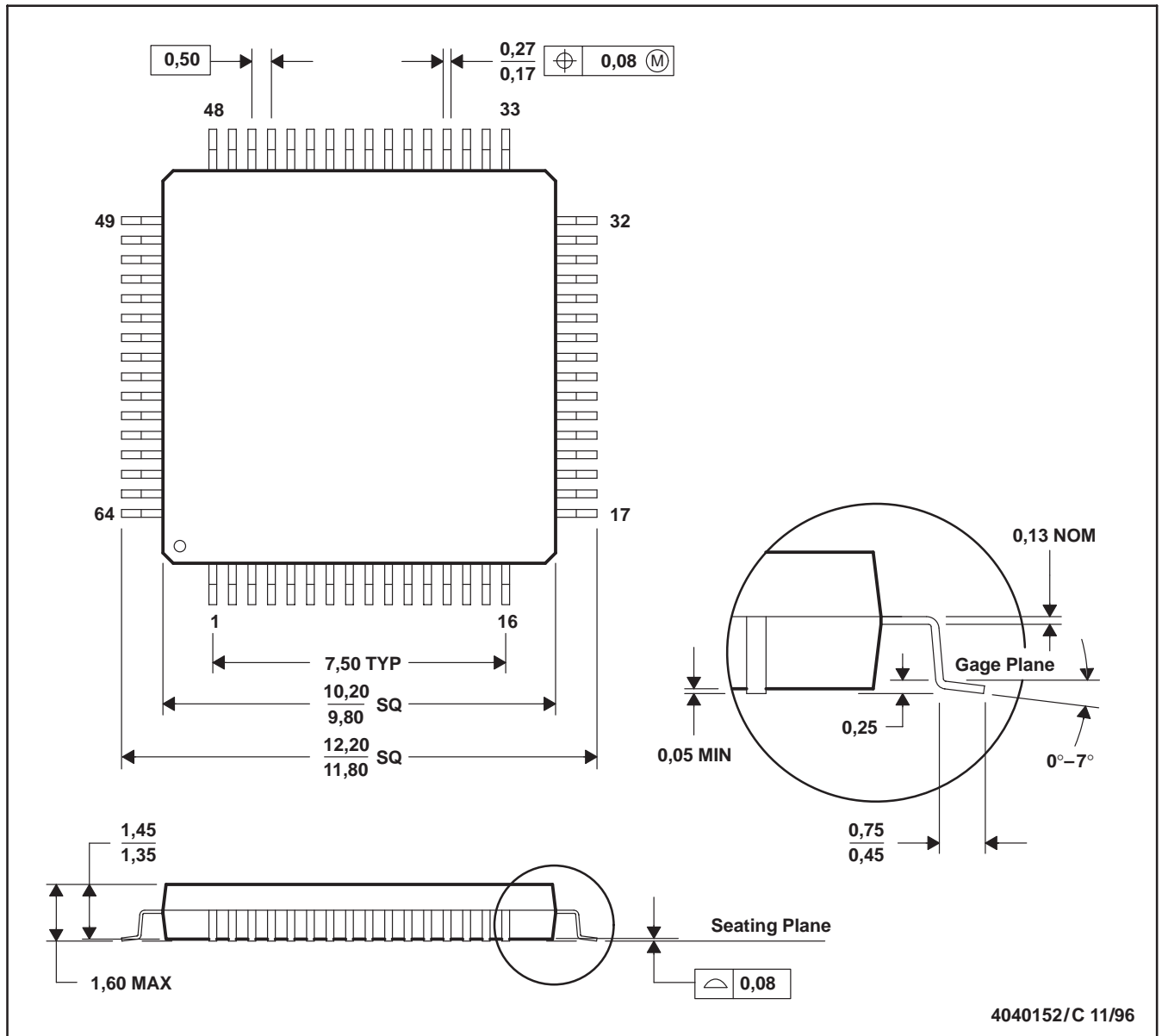
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MSP430FE423IPMR | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| MSP430FE425IPMR | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| MSP430FE427IPMR | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |

PM (S-PQFP-G64)

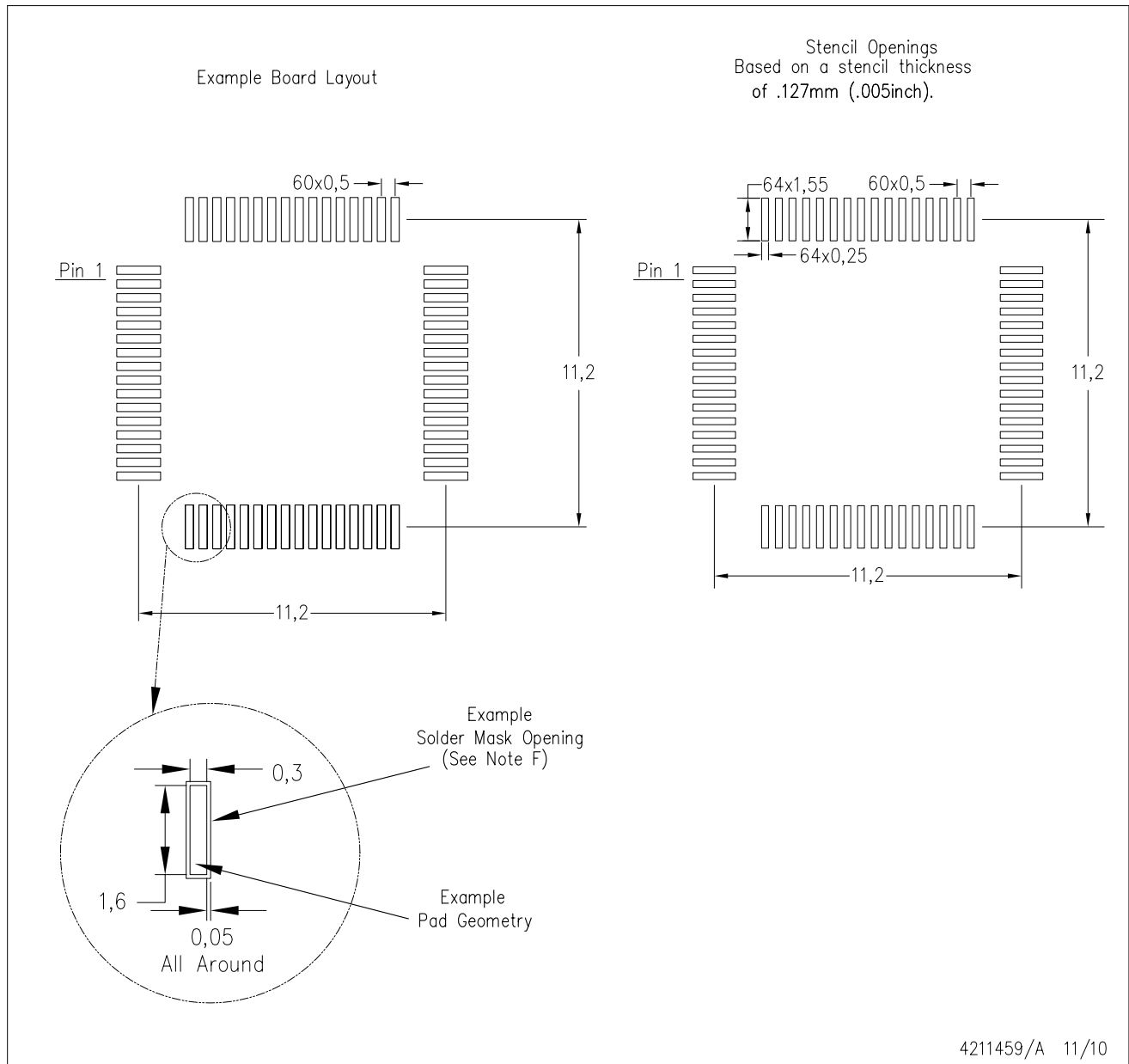
PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-026
 D. May also be thermally enhanced plastic with leads connected to the die pads.

PM (S-PQFP-G64)

PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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