# THE DATASHEET OF

# MSP430F6736IPNR

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TEXAS INSTRUMENTS

MSP430F6736, MSP430F6735, MSP430F6734, MSP430F6733, MSP430F6731, MSP430F6730
MSP430F6726, MSP430F6725, MSP430F6724, MSP430F6723, MSP430F6721, MSP430F6720

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# MSP430F673x, MSP430F672x Mixed-Signal Microcontrollers

## 1 Device Overview

### 1.1 Features

- Low Supply Voltage Range:
  3.6 V Down to 1.8 V
- Ultra-Low Power Consumption
  - Active Mode (AM):
    All System Clocks Active
    265 µA/MHz at 8 MHz, 3.0 V, Flash Program Execution (Typical)
    140 µA/MHz at 8 MHz, 3.0 V, RAM Program Execution (Typical)
  - Standby Mode (LPM3):
    Real-Time Clock (RTC) With Crystal, Watchdog, and Supply Supervisor Operational, Full RAM Retention, Fast Wakeup:
    1.7 µA at 2.2 V, 2.5 µA at 3.0 V (Typical)
  - Off Mode (LPM4):
    Full RAM Retention, Supply Supervisor Operational, Fast Wakeup:
    1.6 µA at 3.0 V (Typical)
  - Shutdown RTC Mode (LPM3.5):
    Shutdown Mode, Active Real-Time Clock (RTC) With Crystal:
    1.24 µA at 3.0 V (Typical)
  - Shutdown Mode (LPM4.5):
    0.78 µA at 3.0 V (Typical)
- Wake up From Standby Mode in 3 µs (Typical)
- 16-Bit RISC Architecture, Extended Memory, up to 25-MHz System Clock
- Flexible Power Management System
  - Fully Integrated LDO With Programmable Regulated Core Supply Voltage
  - Supply Voltage Supervision, Monitoring, and Brownout
  - System Operation From up to Two Auxiliary Power Supplies
- Unified Clock System
  - FLL Control Loop for Frequency Stabilization
  - Low-Power Low-Frequency Internal Clock Source (VLO)
  - Low-Frequency Trimmed Internal Reference Source (REFO)
  - 32-kHz Crystals (XT1)
- One 16-Bit Timer With Three Capture/Compare Registers
- Three 16-Bit Timers With Two Capture/Compare Registers Each
- Enhanced Universal Serial Communication Interfaces
  - eUSCI_A0, eUSCI_A1, and eUSCI_A2
    - Enhanced UART Supports Automatic Baud-Rate Detection
    - IrDA Encoder and Decoder
    - Synchronous SPI
  - eUSCI_B0
    - $I^2C$ With Multiple Slave Addressing
    - Synchronous SPI
- Password-Protected RTC With Crystal Offset Calibration and Temperature Compensation
- Separate Voltage Supply for Backup Subsystem
  - 32-kHz Low-Frequency Oscillator (XT1)
  - Real-Time Clock
  - Backup Memory (4 × 16 Bits)
- Three 24-Bit Sigma-Delta Analog-to-Digital Converters (ADCs) With Differential PGA Inputs
- Integrated LCD Driver With Contrast Control for up to 320 Segments in 8-Mux Mode
- Hardware Multiplier Supports 32-Bit Operations
- 10-Bit 200-ksps ADC
  - Internal Reference
  - Sample-and-Hold, Autoscan Feature
  - Up to Six External Channels and Two Internal Channels, Including Temperature Sensor
- 3-Channel Internal DMA
- Serial Onboard Programming, No External Programming Voltage Needed
- Single-Phase Electronic Watt-Hour Meter Development Tool (Also See Tools and Software)
  - EVM430-F6736 - MSP430F6736 EVM for Metering
  - Energy Measurement Design Center for MSP430™ MCUs
- Device Comparison Summarizes the Available Family Members
- Available in 100-Pin and 80-Pin LQFP Packages

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

## 1.2 Applications

- 2-Wire Single-Phase Metering
- 3-Wire Single-Phase Metering
- Tamper-Resistant Meters

## 1.3 Description

The TI MSP family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with extensive low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows the device to wake up from low-power modes to active mode in 3 µs (typical).

The MSP430F673x and MSP430F672x microcontrollers feature up to three high-performance 24-bit sigma-delta ADCs, a 10-bit ADC, four enhanced universal serial communication interfaces (three eUSCI_A modules and one eUSCI_B module), four 16-bit timers, a hardware multiplier, a DMA module, an RTC module with alarm capabilities, an LCD driver with integrated contrast control, an auxiliary supply system, and up to 72 I/O pins in the 100-pin devices and 52 I/O pins in the 80-pin devices.

For complete module descriptions, see the *MSP430F5xx and MSP430F6xx Family User's Guide*.

**Device Information**(1)

| PART NUMBER | PACKAGE | BODY SIZE(2) |
|---|---|---|
| MSP430F6736IPZ | LQFP (100) | 14 mm × 14 mm |
| MSP430F6736IPN | LQFP (80) | 12 mm × 12 mm |

(1) For the most current part, package, and ordering information, see the *Package Option Addendum* in Section 8, or see the TI website at www.ti.com.
(2) The sizes shown here are approximations. For the package dimensions with tolerances, see the *Mechanical Data* in Section 8.


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## 1.4 Functional Block Diagrams

Figure 1-1 shows the functional block diagram for all device variants in the PZ package.

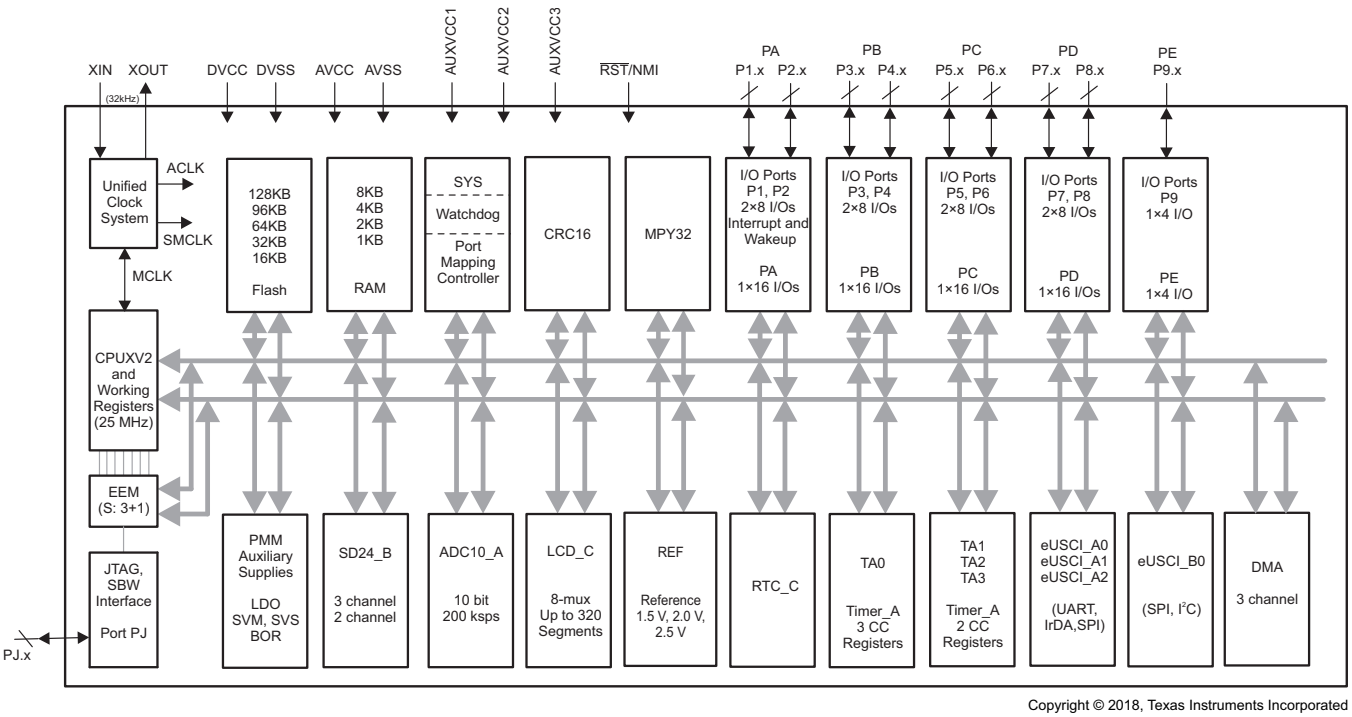


**Figure 1-1. Functional Block Diagram - MSP430F673xIPZ and MSP430F672xIPZ**

Figure 1-2 shows the functional block diagram for all device variants in the PN package.

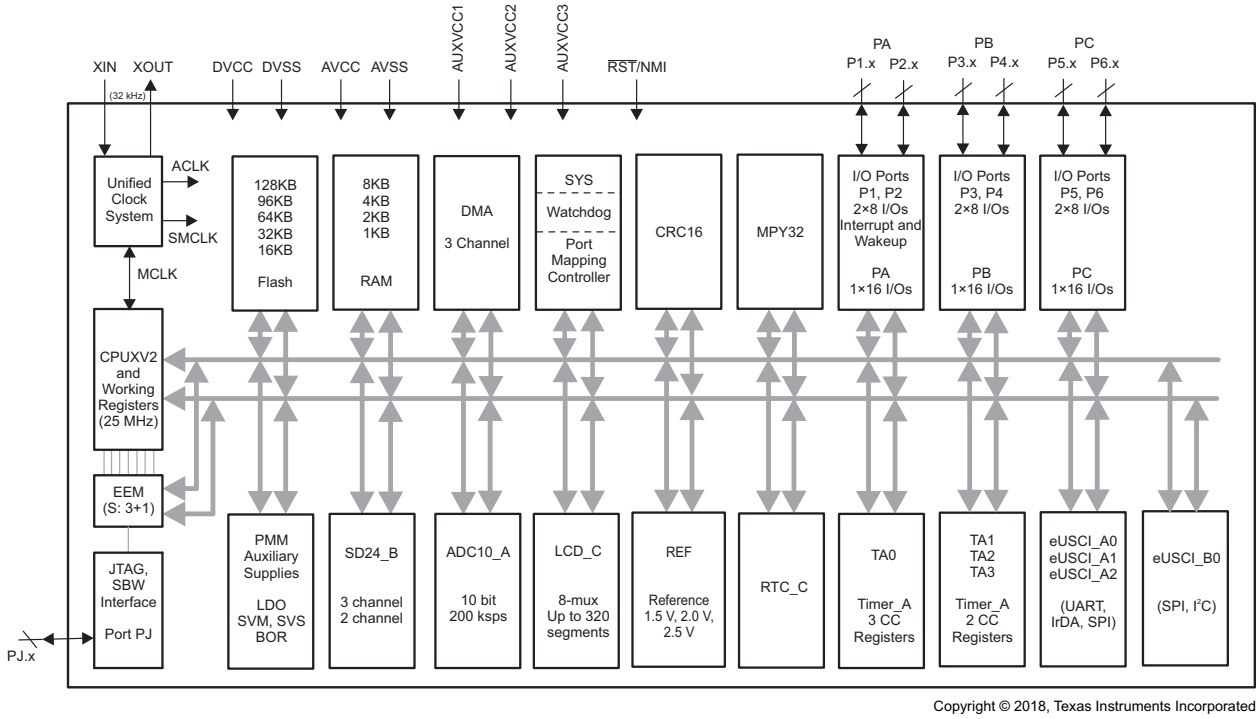


**Figure 1-2. Functional Block Diagram - MSP430F673xIPN and MSP430F672xIPN**

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## 2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from February 28, 2013 to September 28, 2018** **Page**

- Document format and organization changes throughout, including addition of section numbering ..... 1
- Added links to development tool and design center in , *Features* ..... 1
- Added *Device Information* table ..... 2
- Corrected the names of the AUXVCC1, AUXVCC2, and AUXVCC3 pins in Section 1.4, *Functional Block Diagrams* . 3
- Added Section 3 and moved Table 3-1 to it ..... 6
- Added Section 3.1, *Related Products* ..... 7
- Added note to $\overline{\text{RST}}$/NMI/SBWTDIO pin in Table 4-3, *Terminal Functions, PZ Package* ..... 17
- Added note to $\overline{\text{RST}}$/NMI/SBWTDIO pin in Table 4-4, *Terminal Functions, PN Package* ..... 22
- Added typical conditions statements at the beginning of Section 5, *Specifications* ..... 24
- Moved all electrical specifications to Section 5, *Specifications* ..... 24
- Added SD24_B input pins and AUXVCCx pins to exception list on "Voltage applied to pins" parameter, and added SD24_B input pin limits in "Diode current at pins" parameter in Section 5.1, *Absolute Maximum Ratings* ..... 24
- Added Section 5.2, *ESD Ratings* ..... 24
- Added note on $C_{VCORE}$ in Section 5.3, *Recommended Operating Conditions* ..... 24
- Added Section 5.7, *Thermal Resistance Characteristics* ..... 29
- Added note to $R_{Pull}$ in Table 5-1, *Schmitt-Trigger Inputs – General-Purpose I/O* ..... 30
- Changed TYP value of $C_{L,eff}$ with Test Conditions of "XTS = 0, XCAPx = 0" from 2 pF to 1 pF in Table 5-7, *Crystal Oscillator, XT1, Low-Frequency Mode* ..... 35
- Corrected the formula in note (1) [added "/ (85ºC – (–40ºC)"] in Table 5-8, *Internal Very-Low-Power Low-Frequency Oscillator (VLO)* ..... 36
- Corrected the formula in note (1) [added "/ (85ºC – (–40ºC)"] in Table 5-9, *Internal Reference, Low-Frequency Oscillator (REFO)* ..... 36
- Changed the MIN value of the $V_{(DVCC_BOR_hys)}$ parameter from 60 mV to 50 mV in Table 5-11, *PMM, Brownout Reset (BOR)* ..... 38
- Updated notes (1) and (2) and added note (3) in Table 5-17, *Wake-up Times From Low-Power Modes and Reset* ..... 40
- Corrected the names of the AUXVCC1, AUXVCC2, and AUXVCC3 pins in Auxiliary Supplies section ..... 41
- Corrected the name of the AUXCHCx bit in the Test Conditions of Table 5-25, *Auxiliary Supplies, Charge Limiting Resistor* ..... 43
- Replaced $f_{Frame}$ parameter with $f_{LCD}$, $f_{FRAME,4mux}$, and $f_{FRAME,8mux}$ parameters in Table 5-33, *LCD_C Recommended Operating Conditions* ..... 50
- Removed ADC10DIV from the formula for the TYP value in the second row of the $t_{CONVERT}$ parameter in Table 5-44, *10-Bit ADC, Timing Parameters*, because ADC10CLK is after division ..... 59
- Updated Test Conditions for all parameters in Table 5-45, *10-Bit ADC, Linearity Parameters*: Changed from "$C_{VREF+}$ = 20 pF" to "$C_{VeREF+}$ = 20 pF"; Changed from "$(V_{eREF+} – V_{eREF–})$min ≤ $(V_{eREF+} – V_{eREF–})$" to "1.4 V ≤ $(V_{eREF+} – V_{eREF–})$"; Added "$C_{VeREF+}$ = 20 pF" to $E_I$ Test Conditions ..... 60
- Added "ADC10SREFx = 11b" to Test Conditions for $E_G$ and $E_T$ in Table 5-45 ..... 60
- Throughout document, changed all instances of "bootstrap loader" to "bootloader" ..... 69
- Corrected spelling of NMIIFG in Table 6-11, *System Module Interrupt Vector Registers* ..... 75
- Removed mention of real-time clock mode (also called counter mode) in Section 6.11.21, *Real-Time Clock (RTC_C)* (feature is not supported in this device) ..... 80
- Removed SD24BTRGCTL, SD24BTRGOSR, and SD24BTRGPRE registers (not supported) in Table 6-55, *SD24_B Registers* ..... 93
- Added Section 7, *Device and Documentation Support*, and moved *Device and Development Tool Nomenclature* and *Trademarks* sections to it ..... 129
- Replaced former section *Development Tools Support* with Section 7.3, *Tools and Software* ..... 131
- Added Section 8, *Mechanical, Packaging, and Orderable Information* ..... 136

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# 3 Device Comparison

Table 3-1 summarizes the available family members.

**Table 3-1. Family Members(1)(2)**

| DEVICE | FLASH (KB) | SRAM (KB) | SD24_B CONVERTERS | ADC10_A CHANNELS | Timer_A(3) | eUSCI_A: UART, IrDA, SPI | eUSCI_B: SPI, I²C | I/Os | PACKAGE |
|---|---|---|---|---|---|---|---|---|---|
| MSP430F6736IPZ | 128 | 8 | 3 | 6 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 72 | 100 PZ |
| MSP430F6735IPZ | 128 | 4 | 3 | 6 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 72 | 100 PZ |
| MSP430F6734IPZ | 96 | 4 | 3 | 6 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 72 | 100 PZ |
| MSP430F6733IPZ | 64 | 4 | 3 | 6 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 72 | 100 PZ |
| MSP430F6731IPZ | 32 | 2 | 3 | 6 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 72 | 100 PZ |
| MSP430F6730IPZ | 16 | 1 | 3 | 6 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 72 | 100 PZ |
| MSP430F6726IPZ | 128 | 8 | 2 | 6 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 72 | 100 PZ |
| MSP430F6725IPZ | 128 | 4 | 2 | 6 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 72 | 100 PZ |
| MSP430F6724IPZ | 96 | 4 | 2 | 6 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 72 | 100 PZ |
| MSP430F6723IPZ | 64 | 4 | 2 | 6 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 72 | 100 PZ |
| MSP430F6721IPZ | 32 | 2 | 2 | 6 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 72 | 100 PZ |
| MSP430F6720IPZ | 16 | 1 | 2 | 6 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 72 | 100 PZ |
| MSP430F6736IPN | 128 | 8 | 3 | 3 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 52 | 80 PN |
| MSP430F6735IPN | 128 | 4 | 3 | 3 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 52 | 80 PN |
| MSP430F6734IPN | 96 | 4 | 3 | 3 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 52 | 80 PN |
| MSP430F6733IPN | 64 | 4 | 3 | 3 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 52 | 80 PN |
| MSP430F6731IPN | 32 | 2 | 3 | 3 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 52 | 80 PN |
| MSP430F6730IPN | 16 | 1 | 3 | 3 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 52 | 80 PN |
| MSP430F6726IPN | 128 | 8 | 2 | 3 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 52 | 80 PN |
| MSP430F6725IPN | 128 | 4 | 2 | 3 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 52 | 80 PN |
| MSP430F6724IPN | 96 | 4 | 2 | 3 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 52 | 80 PN |
| MSP430F6723IPN | 64 | 4 | 2 | 3 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 52 | 80 PN |
| MSP430F6721IPN | 32 | 2 | 2 | 3 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 52 | 80 PN |
| MSP430F6720IPN | 16 | 1 | 2 | 3 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 52 | 80 PN |

(1) For the most current package and ordering information, see the *Package Option Addendum* in Section 8, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.


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## 3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

**Products for TI Microcontrollers** TI's low-power and high-performance MCUs, with wired and wireless connectivity options, are optimized for a broad range of applications.

**Products for MSP430 Ultra-Low-Power Microcontrollers** One platform. One ecosystem. Endless possibilities. Enabling the connected world with innovations in ultra-low-power microcontrollers with advanced peripherals for precise sensing and measurement.

**Companion Products for MSP430F6736** Review products that are frequently purchased or used with this product.

**Reference Designs for MSP430F6736** The TI Designs Reference Design Library is a robust reference design library that spans analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market. Search and download designs at ti.com/tidesigns.

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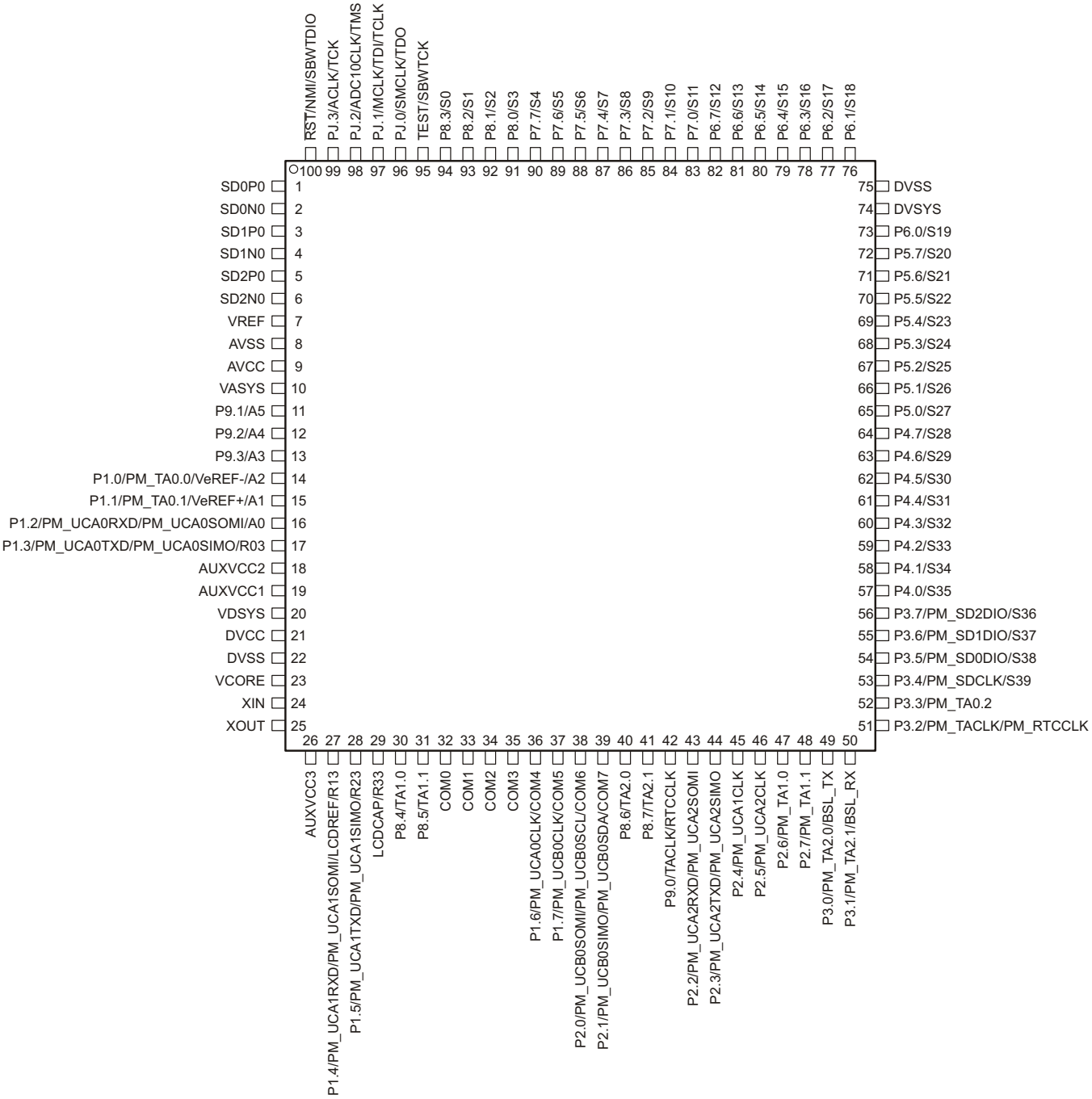
# 4 Terminal Configuration and Functions

## 4.1 Pin Diagrams

Figure 4-1 shows the pinout for the 100-pin PZ package. See Table 4-1 for differences between the MSP430F673x and MSP430F672x devices in this package.




NOTE: The secondary digital functions on Ports P1, P2, and P3 are fully mappable. This pinout shows the default mapping. See Table 6-9 for details.

NOTE: The pins VDSYS and DVSYS must be connected externally on board for proper device operation.

CAUTION: The LCDCAP/R33 pin must be connected to DVSS if not used.

**Figure 4-1. 100-Pin PZ Package (Top View)**


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**Table 4-1. Pinout Differences Between MSP430F673xIPZ and MSP430F672xIPZ(1)**

| PIN NUMBER | PIN NAME | |
|---|---|---|
| | MSP430F673xIPZ | MSP430F672xIPZ |
| 1 | SD0P0 | SD0P0 |
| 2 | SD0N0 | SD0N0 |
| 3 | SD1P0 | SD1P0 |
| 4 | SD1N0 | SD1N0 |
| 5 | *SD2P0* | *NC* |
| 6 | *SD2N0* | *NC* |
| 7 | VREF | VREF |
| 53 | P3.4/PM_SDCLK/S39 | P3.4/PM_SDCLK/S39 |
| 54 | P3.5/PM_SD0DIO/S38 | P3.5/PM_SD0DIO/S38 |
| 55 | P3.6/PM_SD1DIO/S37 | P3.6/PM_SD1DIO/S37 |
| 56 | P3.7/*PM_SD2DIO*/S36 | P3.7/*PM_NONE*/S36 |

(1) Signal names that differ between devices are indicated by *italic* typeface.

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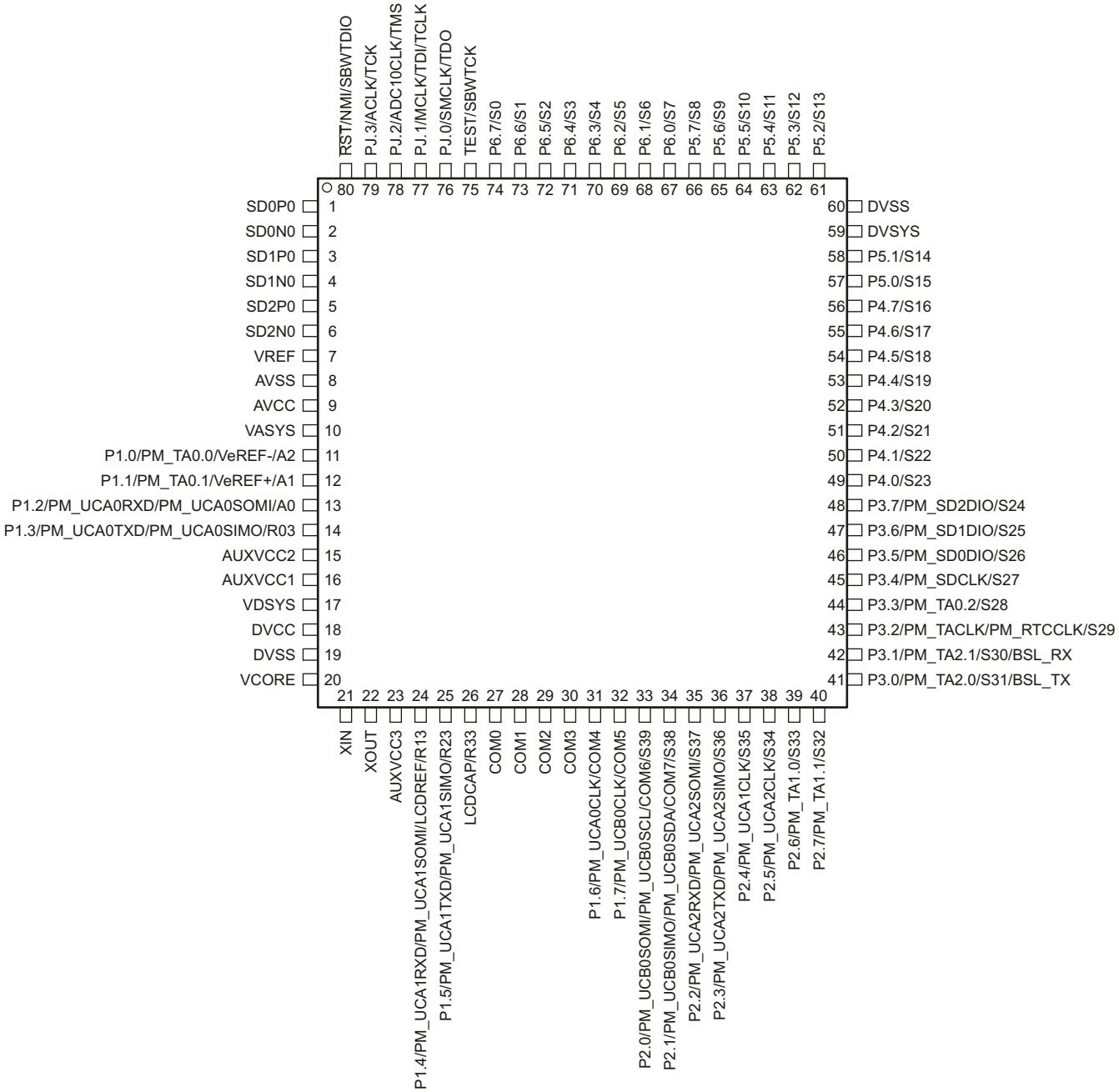
Figure 4-2 shows the pinout for the 80-pin PN package. See Table 4-2 for differences between the MSP430F673x and MSP430F672x devices in this package.




NOTE: The secondary digital functions on Ports P1, P2, and P3 are fully mappable. This pinout shows the default mapping. See Table 6-9 for details.

NOTE: The pins VDSYS and DVSYS must be connected externally on board for proper device operation.

CAUTION: The LCDCAP/R33 pin must be connected to DVSS if not used.

**Figure 4-2. 80-Pin PN Package (Top View)**


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**Table 4-2. Pinout Differences Between MSP430F673xIPN and MSP430F672xIPN(1)**

| PIN NUMBER | PIN NAME | |
|---|---|---|
| | MSP430F673xIPN | MSP430F672xIPN |
| 1 | SD0P0 | SD0P0 |
| 2 | SD0N0 | SD0N0 |
| 3 | SD1P0 | SD1P0 |
| 4 | SD1N0 | SD1N0 |
| 5 | *SD2P0* | *NC* |
| 6 | *SD2N0* | *NC* |
| 7 | VREF | VREF |
| 45 | P3.4/PM_SDCLK/S27 | P3.4/PM_SDCLK/S27 |
| 46 | P3.5/PM_SD0DIO/S26 | P3.5/PM_SD0DIO/S26 |
| 47 | P3.6/PM_SD1DIO/S25 | P3.6/PM_SD1DIO/S25 |
| 48 | P3.7/*PM_SD2DIO*/S24 | P3.7/*PM_NONE*/S24 |

(1) Signal names that differ between devices are indicated by *italic* typeface.

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## 4.2 Signal Descriptions

Table 4-3 describes the signals for all device variants in the PZ package. See Table 4-4 for signal descriptions in the PN package.

**Table 4-3. Terminal Functions, PZ Package**

| TERMINAL | | I/O(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| | PZ | | |
| SD0P0 | 1 | I | SD24_B positive analog input for converter 0(2) |
| SD0N0 | 2 | I | SD24_B negative analog input for converter 0(2) |
| SD1P0 | 3 | I | SD24_B positive analog input for converter 1(2) |
| SD1N0 | 4 | I | SD24_B negative analog input for converter 1(2) |
| SD2P0 | 5 | I | SD24_B positive analog input for converter 2(2) (not available on F672x devices) |
| SD2N0 | 6 | I | SD24_B negative analog input for converter 2(2) (not available on F672x devices) |
| VREF | 7 | I | SD24_B external reference voltage |
| AVSS | 8 | | Analog ground supply |
| AVCC | 9 | | Analog power supply |
| VASYS | 10 | | Analog power supply selected between AVCC, AUXVCC1, AUXVCC2. Connect recommended capacitor value of $C_{VSYS}$ (see Table 5-18). |
| P9.1/A5 | 11 | I/O | General-purpose digital I/O<br>Analog input A5 for 10-bit ADC |
| P9.2/A4 | 12 | I/O | General-purpose digital I/O<br>Analog input A4 for 10-bit ADC |
| P9.3/A3 | 13 | I/O | General-purpose digital I/O<br>Analog input A3 for 10-bit ADC |
| P1.0/PM_TA0.0/VeREF-/A2 | 14 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: Timer TA0 CCR0 capture: CCI0A input, compare: Out0 output<br>Negative terminal for the ADC reference voltage for an external applied reference voltage<br>Analog input A2 for 10-bit ADC |
| P1.1/PM_TA0.1/VeREF+/A1 | 15 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: Timer TA0 CCR1 capture: CCI1A input, compare: Out1 output<br>Positive terminal for the ADC reference voltage for an external applied reference voltage<br>Analog input A1 for 10-bit ADC |
| P1.2/PM_UCA0RXD/<br>PM_UCA0SOMI/A0 | 16 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: eUSCI_A0 UART receive data; eUSCI_A0 SPI slave out/master in<br>Analog input A0 for 10-bit ADC |
| P1.3/PM_UCA0TXD/<br>PM_UCA0SIMO/R03 | 17 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: eUSCI_A0 UART transmit data; eUSCI_A0 SPI slave in/master out<br>Input/output port of lowest analog LCD voltage (V5) |
| AUXVCC2 | 18 | | Auxiliary power supply AUXVCC2 |
| AUXVCC1 | 19 | | Auxiliary power supply AUXVCC1 |

(1) I = input, O = output
(2) Short unused analog input pairs and connect them to analog ground.


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**Table 4-3. Terminal Functions, PZ Package (continued)**

| TERMINAL | | I/O(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| | PZ | | |
| VDSYS(3) | 20 | | Digital power supply selected between DVCC, AUXVCC1, AUXVCC2. Connect recommended capacitor value of $C_{VSYS}$ (see Table 5-18). |
| DVCC | 21 | | Digital power supply |
| DVSS | 22 | | Digital ground supply |
| VCORE(4) | 23 | | Regulated core power supply (internal use only, no external current loading) |
| XIN | 24 | I | Input terminal for crystal oscillator |
| XOUT | 25 | O | Output terminal for crystal oscillator |
| AUXVCC3 | 26 | | Auxiliary power supply AUXVCC3 for back up subsystem |
| P1.4/PM_UCA1RXD/ PM_UCA1SOMI/LCDREF/R13 | 27 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: eUSCI_A1 UART receive data; eUSCI_A1 SPI slave out/master in<br>External reference voltage input for regulated LCD voltage<br>Input/output port of third most positive analog LCD voltage (V3 or V4) |
| P1.5/PM_UCA1TXD/ PM_UCA1SIMO/R23 | 28 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: eUSCI_A1 UART transmit data; eUSCI_A1 SPI slave in/master out<br>Input/output port of second most positive analog LCD voltage (V2) |
| LCDCAP/R33 | 29 | I/O | LCD capacitor connection<br>Input/output port of most positive analog LCD voltage (V1)<br>**CAUTION**: This pin must be connected to DVSS if not used. |
| P8.4/TA1.0 | 30 | I/O | General-purpose digital I/O<br>Timer TA1 CCR0 capture: CCI0A input, compare: Out0 output |
| P8.5/TA1.1 | 31 | I/O | General-purpose digital I/O<br>Timer TA1 CCR1 capture: CCI1A input, compare: Out1 output |
| COM0 | 32 | O | LCD common output COM0 for LCD backplane |
| COM1 | 33 | O | LCD common output COM1 for LCD backplane |
| COM2 | 34 | O | LCD common output COM2 for LCD backplane |
| COM3 | 35 | O | LCD common output COM3 for LCD backplane |
| P1.6/PM_UCA0CLK/COM4 | 36 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: eUSCI_A0 clock input/output<br>LCD common output COM4 for LCD backplane |
| P1.7/PM_UCB0CLK/COM5 | 37 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: eUSCI_B0 clock input/output<br>LCD common output COM5 for LCD backplane |
| P2.0/PM_UCB0SOMI/ PM_UCB0SCL/COM6 | 38 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: eUSCI_B0 SPI slave out/master in; eUSCI_B0 $I^2C$ clock<br>LCD common output COM6 for LCD backplane |

(3) The pins VDSYS and DVSYS must be connected externally on the board for proper device operation.
(4) VCORE is for internal use only. No external current loading is possible. VCORE should only be connected to the recommended capacitor value, $C_{VCORE}$.

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**Table 4-3. Terminal Functions, PZ Package (continued)**

| TERMINAL | | I/O(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. PZ | | |
| P2.1/PM_UCB0SIMO/<br>PM_UCB0SDA/COM7 | 39 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: eUSCI_B0 SPI slave in/master out; eUSCI_B0 $I^2C$ data<br>LCD common output COM7 for LCD backplane |
| P8.6/TA2.0 | 40 | I/O | General-purpose digital I/O<br>Timer TA2 CCR0 capture: CCI0A input, compare: Out0 output |
| P8.7/TA2.1 | 41 | I/O | General-purpose digital I/O<br>Timer TA2 CCR1 capture: CCI1A input, compare: Out1 output |
| P9.0/TACLK/RTCCLK | 42 | I/O | General-purpose digital I/O<br>Timer clock input TACLK for TA0, TA1, TA2, TA3<br>RTCCLK clock output |
| P2.2/PM_UCA2RXD/<br>PM_UCA2SOMI | 43 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: eUSCI_A2 UART receive data; eUSCI_A2 SPI slave out/master in |
| P2.3/PM_UCA2TXD/<br>PM_UCA2SIMO | 44 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: eUSCI_A2 UART transmit data; eUSCI_A2 SPI slave in/master out |
| P2.4/PM_UCA1CLK | 45 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: eUSCI_A1 clock input/output |
| P2.5/PM_UCA2CLK | 46 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: eUSCI_A2 clock input/output |
| P2.6/PM_TA1.0 | 47 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: Timer TA1 capture CCR0: CCI0A input, compare: Out0 output |
| P2.7/PM_TA1.1 | 48 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: Timer TA1 capture CCR1: CCI1A input, compare: Out1 output |
| P3.0/PM_TA2.0/BSL_TX | 49 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: Timer TA2 capture CCR0: CCI0A input, compare: Out0 output<br>Bootloader: Data transmit |
| P3.1/PM_TA2.1/BSL_RX | 50 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: Timer TA2 capture CCR1: CCI1A input, compare: Out1 output<br>Bootloader: Data receive |
| P3.2/PM_TACLK/PM_RTCCLK | 51 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: Timer clock input TACLK for TA0, TA1, TA2, TA3; RTCCLK clock output |
| P3.3/PM_TA0.2 | 52 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: Timer TA0 capture CCR2: CCI2A input, compare: Out2 output |
| P3.4/PM_SDCLK/S39 | 53 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: SD24_B bitstream clock input/output<br>LCD segment output S39 |


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**Table 4-3. Terminal Functions, PZ Package (continued)**

| TERMINAL | | I/O[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. PZ | | |
| P3.5/PM_SD0DIO/S38 | 54 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: SD24_B converter-0 bitstream data input/output<br>LCD segment output S38 |
| P3.6/PM_SD1DIO/S37 | 55 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: SD24_B converter-1 bitstream data input/output<br>LCD segment output S37 |
| P3.7/PM_SD2DIO/S36 | 56 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: SD24_B converter-2 bitstream data input/output (not available on F672x devices)<br>LCD segment output S36 |
| P4.0/S35 | 57 | I/O | General-purpose digital I/O<br>LCD segment output S35 |
| P4.1/S34 | 58 | I/O | General-purpose digital I/O<br>LCD segment output S34 |
| P4.2/S33 | 59 | I/O | General-purpose digital I/O<br>LCD segment output S33 |
| P4.3/S32 | 60 | I/O | General-purpose digital I/O<br>LCD segment output S32 |
| P4.4/S31 | 61 | I/O | General-purpose digital I/O<br>LCD segment output S31 |
| P4.5/S30 | 62 | I/O | General-purpose digital I/O<br>LCD segment output S30 |
| P4.6/S29 | 63 | I/O | General-purpose digital I/O<br>LCD segment output S29 |
| P4.7/S28 | 64 | I/O | General-purpose digital I/O<br>LCD segment output S28 |
| P5.0/S27 | 65 | I/O | General-purpose digital I/O<br>LCD segment output S27 |
| P5.1/S26 | 66 | I/O | General-purpose digital I/O<br>LCD segment output S26 |
| P5.2/S25 | 67 | I/O | General-purpose digital I/O<br>LCD segment output S25 |
| P5.3/S24 | 68 | I/O | General-purpose digital I/O<br>LCD segment output S24 |
| P5.4/S23 | 69 | I/O | General-purpose digital I/O<br>LCD segment output S23 |

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**Table 4-3. Terminal Functions, PZ Package (continued)**

| TERMINAL | | I/O[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| | PZ | | |
| P5.5/S22 | 70 | I/O | General-purpose digital I/O<br>LCD segment output S22 |
| P5.6/S21 | 71 | I/O | General-purpose digital I/O<br>LCD segment output S21 |
| P5.7/S20 | 72 | I/O | General-purpose digital I/O<br>LCD segment output S20 |
| P6.0/S19 | 73 | I/O | General-purpose digital I/O<br>LCD segment output S19 |
| DVSYS[3] | 74 | | Digital power supply for I/Os |
| DVSS | 75 | | Digital ground supply |
| P6.1/S18 | 76 | I/O | General-purpose digital I/O<br>LCD segment output S18 |
| P6.2/S17 | 77 | I/O | General-purpose digital I/O<br>LCD segment output S17 |
| P6.3/S16 | 78 | I/O | General-purpose digital I/O<br>LCD segment output S16 |
| P6.4/S15 | 79 | I/O | General-purpose digital I/O<br>LCD segment output S15 |
| P6.5/S14 | 80 | I/O | General-purpose digital I/O<br>LCD segment output S14 |
| P6.6/S13 | 81 | I/O | General-purpose digital I/O<br>LCD segment output S13 |
| P6.7/S12 | 82 | I/O | General-purpose digital I/O<br>LCD segment output S12 |
| P7.0/S11 | 83 | I/O | General-purpose digital I/O<br>LCD segment output S11 |
| P7.1/S10 | 84 | I/O | General-purpose digital I/O<br>LCD segment output S10 |
| P7.2/S9 | 85 | I/O | General-purpose digital I/O<br>LCD segment output S9 |
| P7.3/S8 | 86 | I/O | General-purpose digital I/O<br>LCD segment output S8 |
| P7.4/S7 | 87 | I/O | General-purpose digital I/O<br>LCD segment output S7 |


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**Table 4-3. Terminal Functions, PZ Package (continued)**

| TERMINAL | | I/O(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| | PZ | | |
| P7.5/S6 | 88 | I/O | General-purpose digital I/O<br>LCD segment output S6 |
| P7.6/S5 | 89 | I/O | General-purpose digital I/O<br>LCD segment output S5 |
| P7.7/S4 | 90 | I/O | General-purpose digital I/O<br>LCD segment output S4 |
| P8.0/S3 | 91 | I/O | General-purpose digital I/O<br>LCD segment output S3 |
| P8.1/S2 | 92 | I/O | General-purpose digital I/O<br>LCD segment output S2 |
| P8.2/S1 | 93 | I/O | General-purpose digital I/O<br>LCD segment output S1 |
| P8.3/S0 | 94 | I/O | General-purpose digital I/O<br>LCD segment output S0 |
| TEST/SBWTCK | 95 | I | Test mode pin – select digital I/O on JTAG pins<br>Spy-Bi-Wire input clock |
| PJ.0/SMCLK/TDO | 96 | I/O | General-purpose digital I/O<br>SMCLK clock output<br>Test data output |
| PJ.1/MCLK/TDI/TCLK | 97 | I/O | General-purpose digital I/O<br>MCLK clock output<br>Test data input or Test clock input |
| PJ.2/ADC10CLK/TMS | 98 | I/O | General-purpose digital I/O<br>ADC10_A clock output<br>Test mode select |
| PJ.3/ACLK/TCK | 99 | I/O | General-purpose digital I/O<br>ACLK clock output<br>Test clock |
| $\overline{\text{RST}}$/NMI/SBWTDIO | 100 | I/O | Reset input active low(5)<br>Nonmaskable interrupt input<br>Spy-Bi-Wire data input/output |

(5) When this pin is configured as reset, the internal pullup resistor is enabled by default.

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Table 4-4 describes the signals for all device variants in the PN package. See Table 4-3 for signal descriptions in the PZ package.

**Table 4-4. Terminal Functions, PN Package**

| TERMINAL | | I/O(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| | PN | | |
| SD0P0 | 1 | I | SD24_B positive analog input for converter 0(2) |
| SD0N0 | 2 | I | SD24_B negative analog input for converter 0(2) |
| SD1P0 | 3 | I | SD24_B positive analog input for converter 1(2) |
| SD1N0 | 4 | I | SD24_B negative analog input for converter 1(2) |
| SD2P0 | 5 | I | SD24_B positive analog input for converter 2(2) (not available on F672x devices) |
| SD2N0 | 6 | I | SD24_B negative analog input for converter 2(2) (not available on F672x devices) |
| VREF | 7 | I | SD24_B external reference voltage |
| AVSS | 8 | | Analog ground supply |
| AVCC | 9 | | Analog power supply |
| VASYS | 10 | | Analog power supply selected between AVCC, AUXVCC1, AUXVCC2. Connect recommended capacitor value of $C_{VSYS}$ (see Table 5-18). |
| P1.0/PM_TA0.0/VeREF-/A2 | 11 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: Timer TA0 CCR0 capture: CCI0A input, compare: Out0 output<br>Negative terminal for the ADC reference voltage for an external applied reference voltage<br>Analog input A2 for 10-bit ADC |
| P1.1/PM_TA0.1/VeREF+/A1 | 12 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: Timer TA0 CCR1 capture: CCI1A input, compare: Out1 output<br>Positive terminal for the ADC reference voltage for an external applied reference voltage<br>Analog input A1 for 10-bit ADC |
| P1.2/PM_UCA0RXD/<br>PM_UCA0SOMI/A0 | 13 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: eUSCI_A0 UART receive data; eUSCI_A0 SPI slave out/master in<br>Analog input A0 for 10-bit ADC |
| P1.3/PM_UCA0TXD/<br>PM_UCA0SIMO/R03 | 14 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: eUSCI_A0 UART transmit data; eUSCI_A0 SPI slave in/master out<br>Input/output port of lowest analog LCD voltage (V5) |
| AUXVCC2 | 15 | | Auxiliary power supply AUXVCC2 |
| AUXVCC1 | 16 | | Auxiliary power supply AUXVCC1 |
| VDSYS(3) | 17 | | Digital power supply selected between DVCC, AUXVCC1, AUXVCC2. Connect recommended capacitor value of $C_{VSYS}$ (see Table 5-18). |
| DVCC | 18 | | Digital power supply |
| DVSS | 19 | | Digital ground supply |
| VCORE(4) | 20 | | Regulated core power supply (internal use only, no external current loading) |
| XIN | 21 | I | Input terminal for crystal oscillator |
| XOUT | 22 | O | Output terminal for crystal oscillator |
| AUXVCC3 | 23 | | Auxiliary power supply AUXVCC3 for back up subsystem |

(1) I = input, O = output
(2) Short unused analog input pairs and connect them to analog ground.
(3) The pins VDSYS and DVSYS must be connected externally on the board for proper device operation.
(4) VCORE is for internal use only. No external current loading is possible. VCORE should only be connected to the recommended capacitor value, $C_{VCORE}$.


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**Table 4-4. Terminal Functions, PN Package (continued)**

| TERMINAL | | I/O(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. PN | | |
| P1.4/PM_UCA1RXD/ PM_UCA1SOMI/LCDREF/R13 | 24 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: eUSCI_A1 UART receive data; eUSCI_A1 SPI slave out/master in<br>External reference voltage input for regulated LCD voltage<br>Input/output port of third most positive analog LCD voltage (V3 or V4) |
| P1.5/PM_UCA1TXD/ PM_UCA1SIMO/R23 | 25 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: eUSCI_A1 UART transmit data; eUSCI_A1 SPI slave in/master out<br>Input/output port of second most positive analog LCD voltage (V2) |
| LCDCAP/R33 | 26 | I/O | LCD capacitor connection<br>Input/output port of most positive analog LCD voltage (V1)<br>**CAUTION**: This pin must be connected to DVSS if not used. |
| COM0 | 27 | O | LCD common output COM0 for LCD backplane |
| COM1 | 28 | O | LCD common output COM1 for LCD backplane |
| COM2 | 29 | O | LCD common output COM2 for LCD backplane |
| COM3 | 30 | O | LCD common output COM3 for LCD backplane |
| P1.6/PM_UCA0CLK/COM4 | 31 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: eUSCI_A0 clock input/output<br>LCD common output COM4 for LCD backplane |
| P1.7/PM_UCB0CLK/COM5 | 32 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: eUSCI_B0 clock input/output<br>LCD common output COM5 for LCD backplane |
| P2.0/PM_UCB0SOMI/ PM_UCB0SCL/COM6/S39 | 33 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: eUSCI_B0 SPI slave out/master in; eUSCI_B0 $I^2C$ clock<br>LCD common output COM6 for LCD backplane<br>LCD segment output S39 |
| P2.1/PM_UCB0SIMO/ PM_UCB0SDA/COM7/S38 | 34 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: eUSCI_B0 SPI slave in/master out; eUSCI_B0 $I^2C$ data<br>LCD common output COM7 for LCD backplane<br>LCD segment output S38 |
| P2.2/PM_UCA2RXD/ PM_UCA2SOMI/S37 | 35 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: eUSCI_A2 UART receive data; eUSCI_A2 SPI slave out/master in<br>LCD segment output S37 |
| P2.3/PM_UCA2TXD/ PM_UCA2SIMO/S36 | 36 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: eUSCI_A2 UART transmit data; eUSCI_A2 SPI slave in/master out<br>LCD segment output S36 |
| P2.4/PM_UCA1CLK/S35 | 37 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: eUSCI_A1 clock input/output<br>LCD segment output S35 |

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**Table 4-4. Terminal Functions, PN Package (continued)**

| TERMINAL | | I/O[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. PN | | |
| P2.5/PM_UCA2CLK/S34 | 38 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: eUSCI_A2 clock input/output<br>LCD segment output S34 |
| P2.6/PM_TA1.0/S33 | 39 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: Timer TA1 capture CCR0: CCI0A input, compare: Out0 output<br>LCD segment output S33 |
| P2.7/PM_TA1.1/S32 | 40 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function<br>Default mapping: Timer TA1 capture CCR1: CCI1A input, compare: Out1 output<br>LCD segment output S32 |
| P3.0/PM_TA2.0/S31/BSL_TX | 41 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: Timer TA2 capture CCR0: CCI0A input, compare: Out0 output<br>LCD segment output S31<br>Bootloader: Data transmit |
| P3.1/PM_TA2.1/S30/BSL_RX | 42 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: Timer TA2 capture CCR1: CCI1A input, compare: Out1 output<br>LCD segment output S30<br>Bootloader: Data receive |
| P3.2/PM_TACLK/PM_RTCCLK/ S29 | 43 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: Timer clock input TACLK for TA0, TA1, TA2, TA3; RTCCLK clock output<br>LCD segment output S29 |
| P3.3/PM_TA0.2/S28 | 44 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: Timer TA0 capture CCR2: CCI2A input, compare: Out2 output<br>LCD segment output S28 |
| P3.4/PM_SDCLK/S27 | 45 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: SD24_B bitstream clock input/output<br>LCD segment output S27 |
| P3.5/PM_SD0DIO/S26 | 46 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: SD24_B converter-0 bitstream data input/output<br>LCD segment output S26 |
| P3.6/PM_SD1DIO/S25 | 47 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: SD24_B converter-1 bitstream data input/output<br>LCD segment output S25 |
| P3.7/PM_SD2DIO/S24 | 48 | I/O | General-purpose digital I/O with mappable secondary function<br>Default mapping: SD24_B converter-2 bitstream data input/output (not available on F672x devices)<br>LCD segment output S24 |


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**Table 4-4. Terminal Functions, PN Package (continued)**

| TERMINAL | | I/O[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. PN | | |
| P4.0/S23 | 49 | I/O | General-purpose digital I/O<br>LCD segment output S23 |
| P4.1/S22 | 50 | I/O | General-purpose digital I/O<br>LCD segment output S22 |
| P4.2/S21 | 51 | I/O | General-purpose digital I/O<br>LCD segment output S21 |
| P4.3/S20 | 52 | I/O | General-purpose digital I/O<br>LCD segment output S20 |
| P4.4/S19 | 53 | I/O | General-purpose digital I/O<br>LCD segment output S19 |
| P4.5/S18 | 54 | I/O | General-purpose digital I/O<br>LCD segment output S18 |
| P4.6/S17 | 55 | I/O | General-purpose digital I/O<br>LCD segment output S17 |
| P4.7/S16 | 56 | I/O | General-purpose digital I/O<br>LCD segment output S16 |
| P5.0/S15 | 57 | I/O | General-purpose digital I/O<br>LCD segment output S15 |
| P5.1/S14 | 58 | I/O | General-purpose digital I/O<br>LCD segment output S14 |
| DVSYS[3] | 59 | | Digital power supply for I/Os |
| DVSS | 60 | | Digital ground supply |
| P5.2/S13 | 61 | I/O | General-purpose digital I/O<br>LCD segment output S13 |
| P5.3/S12 | 62 | I/O | General-purpose digital I/O<br>LCD segment output S12 |
| P5.4/S11 | 63 | I/O | General-purpose digital I/O<br>LCD segment output S11 |
| P5.5/S10 | 64 | I/O | General-purpose digital I/O<br>LCD segment output S10 |
| P5.6/S9 | 65 | I/O | General-purpose digital I/O<br>LCD segment output S9 |
| P5.7/S8 | 66 | I/O | General-purpose digital I/O<br>LCD segment output S8 |

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**Table 4-4. Terminal Functions, PN Package (continued)**

| TERMINAL | | I/O(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. PN | | |
| P6.0/S7 | 67 | I/O | General-purpose digital I/O<br>LCD segment output S7 |
| P6.1/S6 | 68 | I/O | General-purpose digital I/O<br>LCD segment output S6 |
| P6.2/S5 | 69 | I/O | General-purpose digital I/O<br>LCD segment output S5 |
| P6.3/S4 | 70 | I/O | General-purpose digital I/O<br>LCD segment output S4 |
| P6.4/S3 | 71 | I/O | General-purpose digital I/O<br>LCD segment output S3 |
| P6.5/S2 | 72 | I/O | General-purpose digital I/O<br>LCD segment output S2 |
| P6.6/S1 | 73 | I/O | General-purpose digital I/O<br>LCD segment output S1 |
| P6.7/S0 | 74 | I/O | General-purpose digital I/O<br>LCD segment output S0 |
| TEST/SBWTCK | 75 | I | Test mode pin – select digital I/O on JTAG pins<br>Spy-Bi-Wire input clock |
| PJ.0/SMCLK/TDO | 76 | I/O | General-purpose digital I/O<br>SMCLK clock output<br>Test data output |
| PJ.1/MCLK/TDI/TCLK | 77 | I/O | General-purpose digital I/O<br>MCLK clock output<br>Test data input or Test clock input |
| PJ.2/ADC10CLK/TMS | 78 | I/O | General-purpose digital I/O<br>ADC10_A clock output<br>Test mode select |
| PJ.3/ACLK/TCK | 79 | I/O | General-purpose digital I/O<br>ACLK clock output<br>Test clock |
| $\overline{\text{RST}}$/NMI/SBWTDIO | 80 | I/O | Reset input active low(5)<br>Nonmaskable interrupt input<br>Spy-Bi-Wire data input/output |

(5) When this pin is configured as reset, the internal pullup resistor is enabled by default.


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# 5 Specifications

All graphs in this section are for typical conditions, unless otherwise noted.

Typical (TYP) values are specified at $V_{CC}$ = 3.3 V and $T_A$ = 25°C, unless otherwise noted.

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage applied at DVCC to DVSS | | –0.3 | 4.1 | V |
| Voltage applied to pins(2) | All pins except VCORE(3), SD24_B input pins (SD0N0, SD0P0, SD1N0, SD1P0, SD2N0, SD2P0)(4), AUXVCC1, AUXVCC2, and AUXVCC3(5) | –0.3 | $V_{CC}$ + 0.3 | V |
| Diode current at pins | All pins except SD24_B input pins (SD0N0, SD0P0, SD1N0, SD1P0, SD2N0, SD2P0) | | ±2 | mA |
| | SD0N0, SD0P0, SD1N0, SD1P0, SD2N0, SD2P0(6) | | 2 | |
| Maximum junction temperature, $T_J$ | | | 95 | °C |
| Storage temperature, $T_{stg}$(7) | | –55 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to $V_{SS}$ = $V_{(DVSS)}$ = $V_{(AVSS)}$.
(3) VCORE is for internal device use only. Do not apply external DC loading or voltage.
(4) See Table 5-35 for SD24_B specifications.
(5) See Table 5-18 for AUX specifications.
(6) A protection diode is connected to $V_{CC}$ for the SD24_B input pins. No protection diode is connected to $V_{SS}$.
(7) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±1000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±250 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

## 5.3 Recommended Operating Conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage during program execution and flash programming, $V_{(AVCC)}$ = $V_{(DVCC)}$ = $V_{CC}$ (1)(2) | PMMCOREVx = 0 | 1.8 | | 3.6 | V |
| | | PMMCOREVx = 0, 1 | 2.0 | | 3.6 | |
| | | PMMCOREVx = 0, 1, 2 | 2.2 | | 3.6 | |
| | | PMMCOREVx = 0, 1, 2, 3 | 2.4 | | 3.6 | |
| $V_{SS}$ | Supply voltage $V_{(AVSS)}$ = $V_{(DVSS)}$ = $V_{SS}$ | | | 0 | | V |
| $T_A$ | Operating free-air temperature | | –40 | | 85 | °C |
| $T_J$ | Operating junction temperature | | –40 | | 85 | °C |
| $C_{VCORE}$ | Recommended capacitor at VCORE(3) | | | 470 | | nF |
| $C_{DVCC}/C_{VCORE}$ | Capacitor ratio of DVCC to VCORE | | 10 | | | |

(1) TI recommends powering AVCC and DVCC from the same source. A maximum difference of 0.3 V between $V_{(AVCC)}$ and $V_{(DVCC)}$ can be tolerated during power up and operation.
(2) The minimum supply voltage is defined by the supervisor SVS levels when it is enabled. See the Table 5-13 threshold parameters for the exact values and further details.
(3) A capacitor tolerance of ±20% or better is required.


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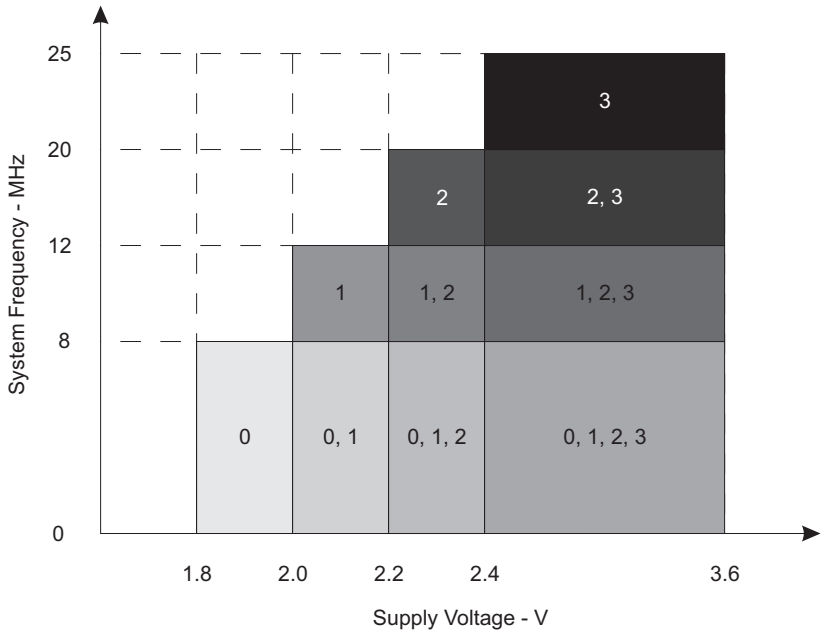
## Recommended Operating Conditions *(continued)*

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{SYSTEM}$ | Processor frequency (maximum MCLK frequency)[4][5] (see Figure 5-1) | PMMCOREVx = 0, 1.8 V ≤ $V_{CC}$ ≤ 3.6 V (default condition) | 0 | | 8.0 | MHz |
| | | PMMCOREVx = 1, 2.0 V ≤ $V_{CC}$ ≤ 3.6 V | 0 | | 12.0 | |
| | | PMMCOREVx = 2, 2.2 V ≤ $V_{CC}$ ≤ 3.6 V | 0 | | 20.0 | |
| | | PMMCOREVx = 3, 2.4 V ≤ $V_{CC}$ ≤ 3.6 V | 0 | | 25.0 | |
| $I_{LOAD, DVCCD}$ | Maximum load current that can be drawn from DVCC for core and IO ($I_{LOAD} = I_{CORE} + I_{IO}$) | | | | 20 | mA |
| $I_{LOAD, AUX1D}$ | Maximum load current that can be drawn from AUXVCC1 for core and IO ($I_{LOAD} = I_{CORE} + I_{IO}$) | | | | 20 | mA |
| $I_{LOAD, AUX2D}$ | Maximum load current that can be drawn from AUXVCC2 for core and IO ($I_{LOAD} = I_{CORE} + I_{IO}$) | | | | 20 | mA |
| $I_{LOAD, AVCCA}$ | Maximum load current that can be drawn from AVCC for analog modules ($I_{LOAD} = I_{Modules}$) | | | | 10 | mA |
| $I_{LOAD, AUX1A}$ | Maximum load current that can be drawn from AUXVCC1 for analog modules ($I_{LOAD} = I_{Modules}$) | | | | 5 | mA |
| $I_{LOAD, AUX2A}$ | Maximum load current that can be drawn from AUXVCC2 for analog modules ($I_{LOAD} = I_{Modules}$) | | | | 5 | mA |

(4) The MSP430 CPU is clocked directly with MCLK. Both the high and low phases of MCLK must not exceed the pulse duration of the specified maximum frequency.
(5) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.




The numbers within the fields denote the supported PMMCOREVx settings.

**Figure 5-1. Maximum System Frequency**

## 5.4 Active Mode Supply Current Into $V_{CC}$ Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)(1) (2) (3)

| PARAMETER | EXECUTION MEMORY | $V_{CC}$ | PMMCOREVx | FREQUENCY ($f_{DCO} = f_{MCLK} = f_{SMCLK}$) | | | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 1 MHz | | 8 MHz | | 12 MHz | | 20 MHz | | 25 MHz | | |
| | | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{AM, Flash}$ (4) | Flash | 3.0 V | 0 | 0.32 | 0.36 | 2.10 | 2.30 | | | | | | | mA |
| | | | 1 | 0.36 | | 2.39 | | 3.54 | 3.90 | | | | | |
| | | | 2 | 0.39 | | 2.65 | | 3.94 | | 6.54 | 7.23 | | | |
| | | | 3 | 0.42 | | 2.82 | | 4.20 | | 6.96 | | 8.65 | 9.54 | |
| $I_{AM, RAM}$ (5) | RAM | 3.0 V | 0 | 0.20 | 0.22 | 1.10 | 1.22 | | | | | | | mA |
| | | | 1 | 0.22 | | 1.30 | | 1.90 | 2.10 | | | | | |
| | | | 2 | 0.24 | | 1.45 | | 2.15 | | 3.55 | 4.0 | | | |
| | | | 3 | 0.26 | | 1.55 | | 2.30 | | 3.80 | | 4.70 | 5.30 | |

(1) All inputs are tied to 0 or to $V_{CC}$. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
(3) Characterized with program executing typical data processing.
$f_{ACLK}$ = 32786 Hz, $f_{DCO} = f_{MCLK} = f_{SMCLK}$ at specified frequency.
XTS = CPUOFF = SCG0 = SCG1 = OSCOFF = SMCLKOFF = 0.
(4) Active mode supply current when program executes in flash at a nominal supply voltage of 3 V.
(5) Active mode supply current when program executes in RAM at a nominal supply voltage of 3 V.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## 5.5 Low-Power Mode Supply Currents (Into $V_{CC}$) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)(2)

| PARAMETER | | $V_{CC}$ | PMMCOREVx | TEMPERATURE ($T_A$) | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | –40°C | | 25°C | | 60°C | | 85°C | | |
| | | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM0,1MHz}$ | Low-power mode 0(3)(4) | 2.2 V | 0 | 75 | | 78 | 87 | 81 | | 84 | 96 | µA |
| | | 3.0 V | 3 | 85 | | 89 | 99 | 93 | | 98 | 110 | |
| $I_{LPM2}$ | Low-power mode 2(5)(4) | 2.2 V | 0 | 5.9 | | 6.2 | 9 | 6.9 | | 9.4 | 17 | µA |
| | | 3.0 V | 3 | 6.9 | | 7.4 | 10 | 8.4 | | 11 | 19 | |
| $I_{LPM3,XT1LF}$ | Low-power mode 3, crystal mode(6)(4) | 2.2 V | 0 | 1.4 | | 1.7 | | 2.5 | | 4.9 | | µA |
| | | | 1 | 1.5 | | 1.9 | | 2.7 | | 5.2 | | |
| | | | 2 | 1.7 | | 2.0 | | 2.9 | | 5.5 | | |
| $I_{LPM3,XT1LF}$ | Low-power mode 3, crystal mode(6)(4) | 3.0 V | 0 | 2.2 | | 2.5 | 3.1 | 3.3 | | 5.5 | 12.7 | µA |
| | | | 1 | 2.3 | | 2.7 | | 3.5 | | 5.8 | | |
| | | | 2 | 2.5 | | 2.9 | | 3.7 | | 6.1 | | |
| | | | 3 | 2.5 | | 2.9 | 3.5 | 3.7 | | 6.1 | 14.0 | |
| $I_{LPM3,VLO}$ | Low-power mode 3, VLO mode(7)(4) | 3.0 V | 0 | 1.4 | | 1.7 | 2.2 | 2.4 | | 4.5 | 11.5 | µA |
| | | | 1 | 1.5 | | 1.8 | | 2.5 | | 4.7 | | |
| | | | 2 | 1.6 | | 1.9 | | 2.7 | | 4.9 | | |
| | | | 3 | 1.6 | | 1.9 | 2.4 | 2.7 | | 5.0 | 12.7 | |
| $I_{LPM4}$ | Low-power mode 4(8)(4) | 3.0 V | 0 | 1.3 | | 1.6 | 2.0 | 2.3 | | 4.4 | 11.1 | µA |
| | | | 1 | 1.4 | | 1.6 | | 2.4 | | 4.5 | | |
| | | | 2 | 1.4 | | 1.7 | | 2.5 | | 4.8 | | |
| | | | 3 | 1.4 | | 1.7 | 2.2 | 2.5 | | 4.8 | 12.2 | |
| $I_{LPM3.5}$ | Low-power mode 3.5, RTC active on AUXVCC3(9) | 2.2 V | | 0.65 | | 0.80 | | 0.90 | | 1.30 | | µA |
| | | 3.0 V | | 1.16 | | 1.24 | 2.05 | 1.43 | | 1.87 | 2.71 | |
| $I_{LPM4.5}$ | Low-power mode 4.5(10) | 3.0 V | | 0.70 | | 0.78 | 1.05 | 0.90 | | 1.20 | 1.85 | µA |

(1) All inputs are tied to 0 V or to $V_{CC}$. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
(3) Current for watchdog timer clocked by SMCLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0).
CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0), $f_{ACLK}$ = 32768 Hz, $f_{MCLK}$ = 0 MHz, $f_{SMCLK}$ = $f_{DCO}$ = 1 MHz
(4) Current for brownout, high-side supervisor ($SVS_H$) normal mode included. Low-side supervisor ($SVS_L$) and low-side monitor ($SVM_L$) disabled. High-side monitor ($SVM_H$) disabled. RAM retention enabled.
(5) Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0).
CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 (LPM2), $f_{ACLK}$ = 32768 Hz, $f_{MCLK}$ = 0 MHz, $f_{SMCLK}$ = $f_{DCO}$ = 0 MHz, DCO setting = 1-MHz operation, DCO bias generator enabled.
(6) Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0).
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), $f_{ACLK}$ = 32768 Hz, $f_{MCLK}$ = $f_{SMCLK}$ = $f_{DCO}$ = 0 MHz
(7) Current for watchdog timer clocked by ACLK included. RTC is disabled (RTCHOLD = 1). ACLK = VLO.
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), $f_{ACLK}$ = $f_{VLO}$, $f_{MCLK}$ = $f_{SMCLK}$ = $f_{DCO}$ = 0 MHz
(8) CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 (LPM4), $f_{DCO}$ = $f_{ACLK}$ = $f_{MCLK}$ = $f_{SMCLK}$ = 0 MHz
(9) $f_{DCO}$ = $f_{MCLK}$ = $f_{SMCLK}$ = 0 MHz, $f_{ACLK}$ = 32768 Hz, PMMREGOFF = 1, RTC active on AUXVCC3 supply
(10) $f_{DCO}$ = $f_{MCLK}$ = $f_{SMCLK}$ = 0 MHz, $f_{ACLK}$ = 0 Hz, PMMREGOFF = 1

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## 5.6 Low-Power Mode With LCD Supply Currents (Into $V_{CC}$) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)(2)

| PARAMETER | | $V_{CC}$ | PMMCOREVx | TEMPERATURE ($T_A$) | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | –40°C | | 25°C | | 60°C | | 85°C | | |
| | | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM3}$ LCD, int. bias | Low-power mode 3 (LPM3) current, LCD 4-mux mode, internal biasing, charge pump disabled(3)(4) | 2.2 V | 0 | 2.4 | | 2.9 | 3.6 | 3.8 | | 5.8 | 12.2 | µA |
| | | | 1 | 2.5 | | 3.1 | | 4.0 | | 6.0 | | |
| | | | 2 | 2.6 | | 3.3 | 3.9 | 4.2 | | 6.3 | 13.4 | |
| $I_{LPM3}$ LCD, int. bias | Low-power mode 3 (LPM3) current, LCD 4-mux mode, internal biasing, charge pump disabled(3)(4) | 3.0 V | 0 | 2.8 | | 3.2 | 3.9 | 4.1 | | 6.4 | 13.3 | µA |
| | | | 1 | 2.9 | | 3.4 | | 4.3 | | 6.7 | | |
| | | | 2 | 3.1 | | 3.6 | | 4.5 | | 7.0 | | |
| | | | 3 | 3.1 | | 3.6 | 4.5 | 4.5 | | 7.0 | 14.7 | |
| $I_{LPM3}$ LCD,CP | Low-power mode 3 (LPM3) current, LCD 4-mux mode, internal biasing, charge pump enabled(3)(5) | 2.2 V | 0 | | | 3.8 | | | | | | µA |
| | | | 1 | | | 3.9 | | | | | | |
| | | | 2 | | | 4.0 | | | | | | |
| | | 3.0 V | 0 | | | 4.0 | | | | | | |
| | | | 1 | | | 4.1 | | | | | | |
| | | | 2 | | | 4.2 | | | | | | |
| | | | 3 | | | 4.2 | | | | | | |

(1) All inputs are tied to 0 V or to $V_{CC}$. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
(3) Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0).
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), $f_{ACLK}$ = 32768 Hz, $f_{MCLK} = f_{SMCLK} = f_{DCO}$ = 0 MHz
Current for brownout, high-side supervisor ($SVS_H$) normal mode included. Low-side supervisor ($SVS_L$) and low-side monitor ($SVM_L$) disabled. High-side monitor ($SVM_H$) disabled. RAM retention enabled.
(4) LCDMx = 11 (4-mux mode), LCDREXT = 0, LCDEXTBIAS = 0 (internal biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 0 (charge pump disabled), LCDSSEL = 0, LCDPREx = 101, LCDDIVx = 00011 ($f_{LCD}$ = 32768 Hz / 32 / 4 = 256 Hz)
Even segments S0, S2, ... = 0 and odd segments S1, S3, ... = 1. No LCD panel load.
(5) LCDMx = 11 (4-mux mode), LCDREXT = 0, LCDEXTBIAS = 0 (internal biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 1 (charge pump enabled), VLCDx = 1000 ($V_{LCD}$ = 3 V, typical), LCDSSEL = 0, LCDPREx = 101, LCDDIVx = 00011 ($f_{LCD}$ = 32768 Hz / 32 / 4 = 256 Hz)
Even segments S0, S2, ... = 0 and odd segments S1, S3, ... = 1. No LCD panel load.


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## 5.7 Thermal Resistance Characteristics

| THERMAL METRIC(1) (2) | | | VALUE | UNIT |
|---|---|---|---|---|
| $R\theta_{JA}$ | Junction-to-ambient thermal resistance, still air | LQFP 80 (PN) | 46.3 | °C/W |
| | | LQFP 100 (PZ) | 45.6 | |
| $R\theta_{JC(TOP)}$ | Junction-to-case (top) thermal resistance | LQFP 80 (PN) | 11.5 | °C/W |
| | | LQFP 100 (PZ) | 11.0 | |
| $R\theta_{JC(BOTTOM)}$ | Junction-to-case (bottom) thermal resistance | LQFP 80 (PN) | N/A(3) | °C/W |
| | | LQFP 100 (PZ) | N/A | |
| $R\theta_{JB}$ | Junction-to-board thermal resistance | LQFP 80 (PN) | 21.9 | °C/W |
| | | LQFP 100 (PZ) | 23.4 | |
| $\Psi_{JT}$ | Junction-to-package-top thermal characterization parameter | LQFP 80 (PN) | 0.5 | °C/W |
| | | LQFP 100 (PZ) | 0.4 | |
| $\Psi_{JB}$ | Junction-to-board thermal characterization parameter | LQFP 80 (PN) | 21.6 | °C/W |
| | | LQFP 100 (PZ) | 23.0 | |

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(3) N/A = not applicable

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## 5.8 Digital I/O Ports

Table 5-1 lists the characteristics of the schmitt-trigger Inputs.

**Table 5-1. Schmitt-Trigger Inputs – General-Purpose I/O**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IT+}$ | Positive-going input threshold voltage | | 1.8 V | 0.80 | | 1.40 | V |
| | | | 3 V | 1.50 | | 2.10 | |
| $V_{IT-}$ | Negative-going input threshold voltage | | 1.8 V | 0.45 | | 1.00 | V |
| | | | 3 V | 0.75 | | 1.65 | |
| $V_{hys}$ | Input voltage hysteresis ($V_{IT+} - V_{IT-}$) | | 1.8 V | 0.3 | | 0.85 | V |
| | | | 3 V | 0.4 | | 1.0 | |
| $R_{Pull}$ | Pullup or pulldown resistor(1) | For pullup: $V_{IN} = V_{SS}$<br>For pulldown: $V_{IN} = V_{CC}$ | | 20 | 35 | 50 | kΩ |
| $C_I$ | Input capacitance | $V_{IN} = V_{SS}$ or $V_{CC}$ | | | 5 | | pF |

(1) Also applies to $\overline{RST}$ pin when pullup or pulldown resistor is enabled.

Table 5-2 lists the characteristics of the P1 and P2 inputs.

**Table 5-2. Inputs – Ports P1 and P2(1)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{(int)}$ | External interrupt timing(2) | Port P1, P2: P1.x to P2.x, External trigger pulse duration to set interrupt flag | 2.2 V, 3 V | 20 | | ns |

(1) Some devices may contain additional ports with interrupts. See the block diagram and terminal function descriptions.
(2) An external signal sets the interrupt flag every time the minimum interrupt pulse duration $t_{(int)}$ is met. It might be set by trigger signals shorter than $t_{(int)}$.

Table 5-3 lists the characteristics of the GPIO leakage current.

**Table 5-3. Leakage Current – General-Purpose I/O**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{lkg(Px.y)}$ | High-impedance leakage current | See (1)(2) | 1.8 V, 3 V | | ±50 | nA |

(1) The leakage current is measured with $V_{SS}$ or $V_{CC}$ applied to the corresponding pins, unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

Table 5-4 lists the characteristics of the full drive strength GPIO output.

**Table 5-4. Outputs – General-Purpose I/O (Full Drive Strength)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{(OHmax)}$ = –3 mA(1) | 1.8 V | $V_{CC}$ – 0.25 | $V_{CC}$ | V |
| | | $I_{(OHmax)}$ = –10 mA(1) | | $V_{CC}$ – 0.60 | $V_{CC}$ | |
| | | $I_{(OHmax)}$ = –5 mA(1) | 3 V | $V_{CC}$ – 0.25 | $V_{CC}$ | |
| | | $I_{(OHmax)}$ = –15 mA(1) | | $V_{CC}$ – 0.60 | $V_{CC}$ | |
| $V_{OL}$ | Low-level output voltage | $I_{(OLmax)}$ = 3 mA(2) | 1.8 V | $V_{SS}$ | $V_{SS}$ + 0.25 | V |
| | | $I_{(OLmax)}$ = 10 mA(3) | | $V_{SS}$ | $V_{SS}$ + 0.60 | |
| | | $I_{(OLmax)}$ = 5 mA(2) | 3 V | $V_{SS}$ | $V_{SS}$ + 0.25 | |
| | | $I_{(OLmax)}$ = 15 mA(3) | | $V_{SS}$ | $V_{SS}$ + 0.60 | |

(1) The maximum total current, $I_{(OHmax)}$, for all outputs combined should not exceed ±20 mA to hold the maximum voltage drop specified. See Section 5.3 for more details.
(2) The maximum total current, $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
(3) The maximum total current, $I_{(OLmax)}$, for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.


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### 5.8.1 Typical Characteristics – General-Purpose I/O (Full Drive Strength)

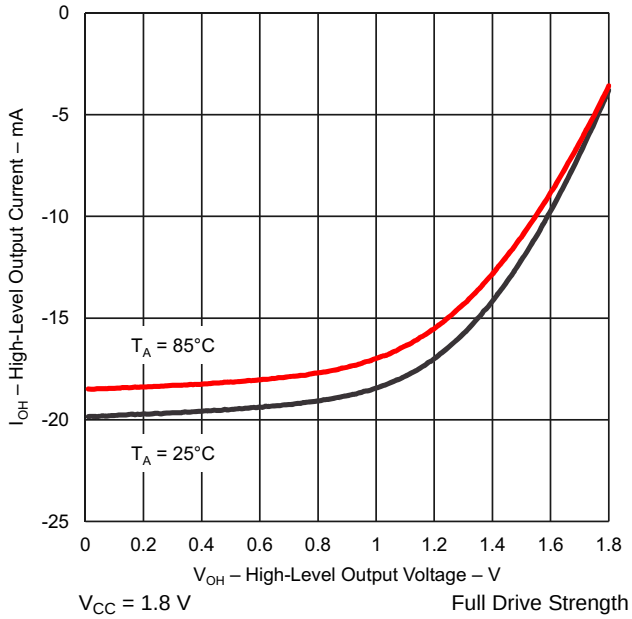


**Figure 5-2. High-Level Output Current vs High-Level Output Voltage**

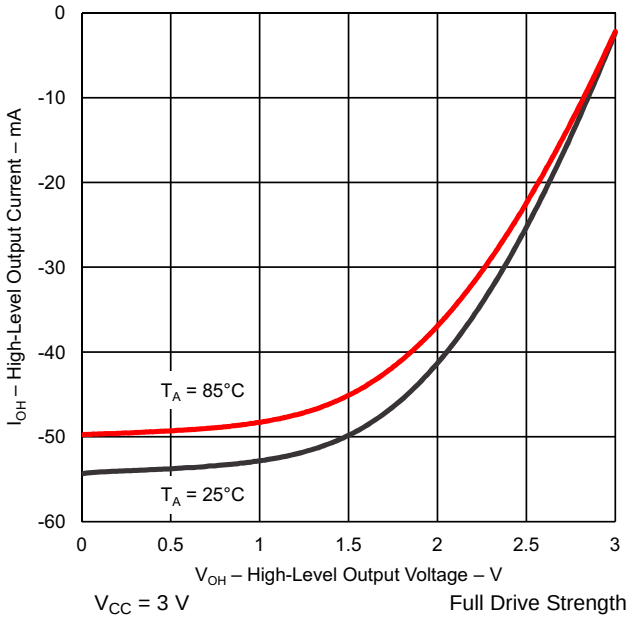


**Figure 5-3. High-Level Output Current vs High-Level Output Voltage**

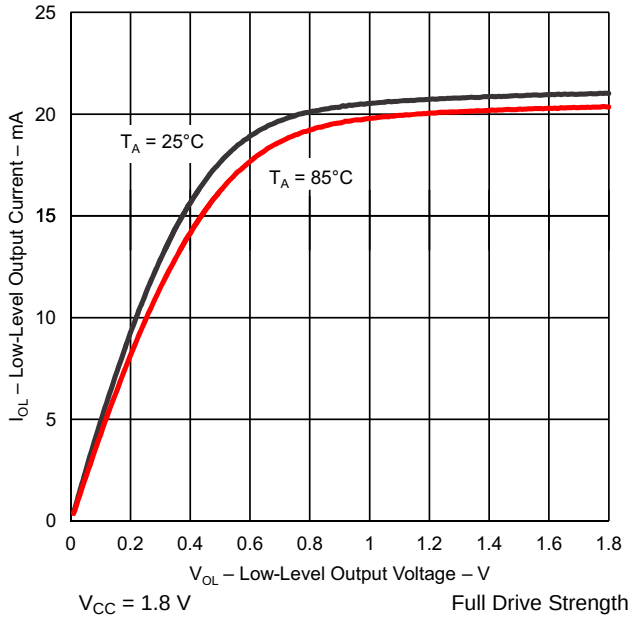


**Figure 5-4. Low-Level Output Current vs Low-Level Output Voltage**

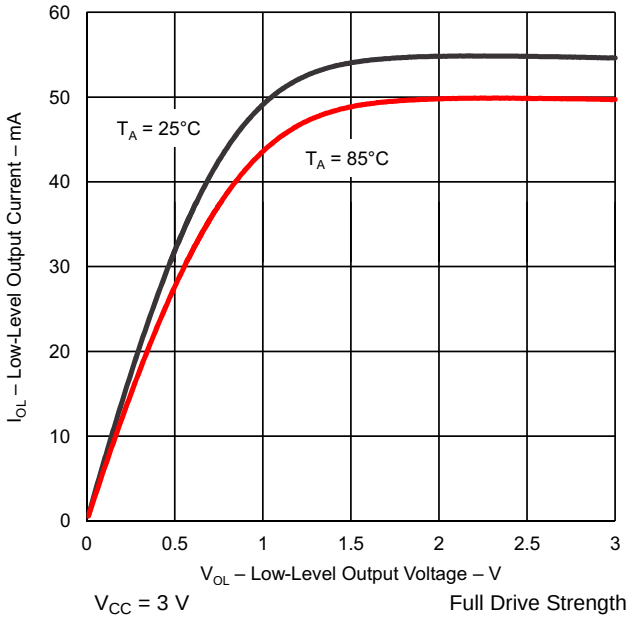


**Figure 5-5. Low-Level Output Current vs Low-Level Output Voltage**

Table 5-5 lists the characteristics of the reduced drive strength GPIO output.

**Table 5-5. Outputs – General-Purpose I/O (Reduced Drive Strength)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $I_{(OHmax)}$ = –1 mA(2) | 1.8 V | $V_{CC}$ – 0.25 | $V_{CC}$ | V |
| | | $I_{(OHmax)}$ = –3 mA(2) | | $V_{CC}$ – 0.60 | $V_{CC}$ | |
| | | $I_{(OHmax)}$ = –2 mA(2) | 3.0 V | $V_{CC}$ – 0.25 | $V_{CC}$ | |
| | | $I_{(OHmax)}$ = –6 mA(2) | | $V_{CC}$ – 0.60 | $V_{CC}$ | |
| $V_{OL}$ | Low-level output voltage | $I_{(OLmax)}$ = 1 mA(3) | 1.8 V | $V_{SS}$ | $V_{SS}$ + 0.25 | V |
| | | $I_{(OLmax)}$ = 3 mA(4) | | $V_{SS}$ | $V_{SS}$ + 0.60 | |
| | | $I_{(OLmax)}$ = 2 mA(3) | 3.0 V | $V_{SS}$ | $V_{SS}$ + 0.25 | |
| | | $I_{(OLmax)}$ = 6 mA(4) | | $V_{SS}$ | $V_{SS}$ + 0.60 | |

(1) Selecting reduced drive strength may reduce EMI.
(2) The maximum total current, $I_{(OHmax)}$, for all outputs combined should not exceed ±20 mA to hold the maximum voltage drop specified. See Section 5.3 for more details.
(3) The maximum total current, $I_{(OLmax)}$, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.
(4) The maximum total current, $I_{(OLmax)}$, for all outputs combined, should not exceed ±100 mA to hold the maximum voltage drop specified.


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### 5.8.2 Typical Characteristics – General-Purpose I/O (Reduced Drive Strength)

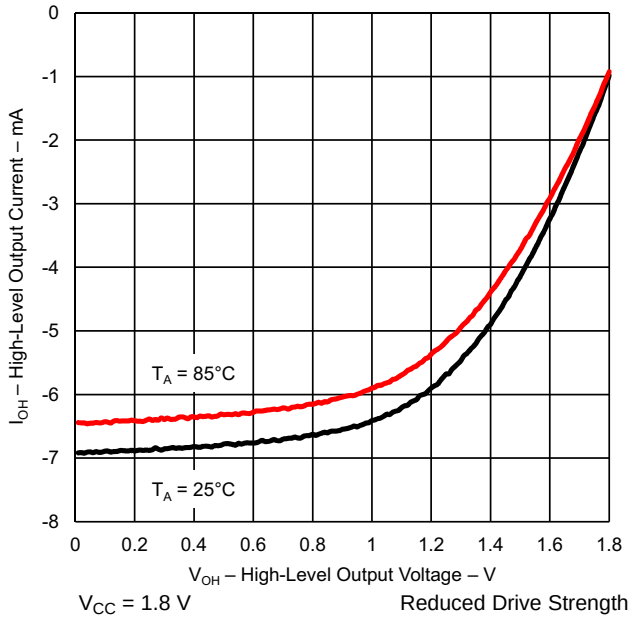


**Figure 5-6. High-Level Output Current vs High-Level Output Voltage**

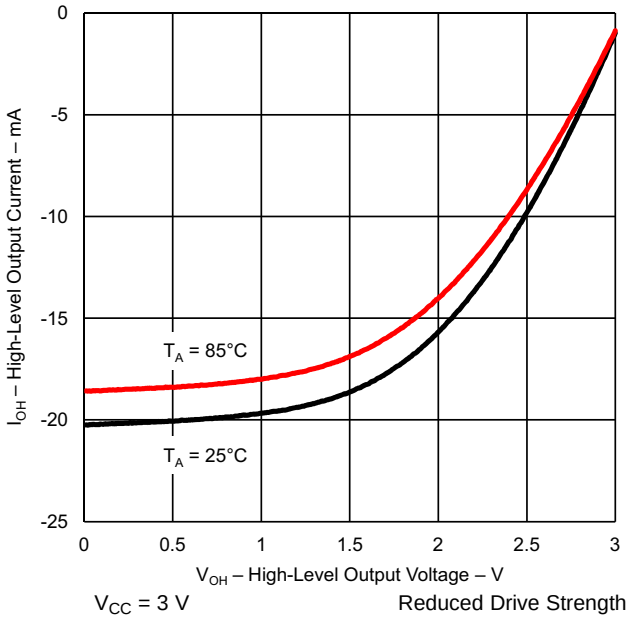


**Figure 5-7. High-Level Output Current vs High-Level Output Voltage**

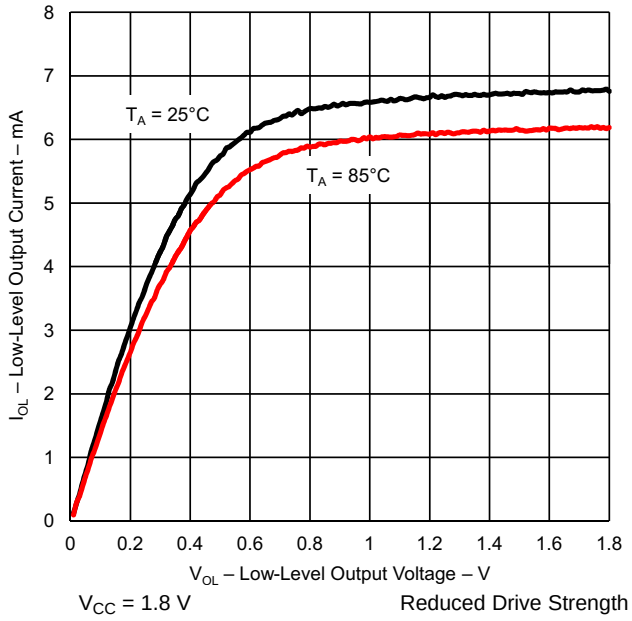


**Figure 5-8. Low-Level Output Current vs Low-Level Output Voltage**

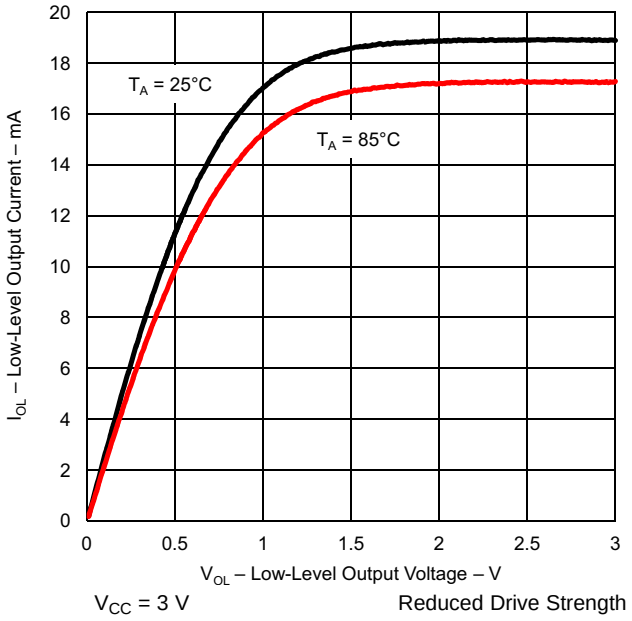


**Figure 5-9. Low-Level Output Current vs Low-Level Output Voltage**

Table 5-6 lists the characteristics of the GPIO output frequency.

**Table 5-6. Output Frequency – General-Purpose I/O**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{Px.y}$ | Port output frequency (with load) | See (1)(2) | $V_{CC}$ = 1.8 V, PMMCOREVx = 0 | | 16 | MHz |
| | | | $V_{CC}$ = 3 V, PMMCOREVx = 3 | | 25 | |
| $f_{Port_CLK}$ | Clock output frequency | ACLK, SMCLK, MCLK, $C_L$ = 20 pF(2) | $V_{CC}$ = 1.8 V, PMMCOREVx = 0 | | 16 | MHz |
| | | | $V_{CC}$ = 3 V, PMMCOREVx = 3 | | 25 | |

(1) A resistive divider with 2 × R1 between $V_{CC}$ and $V_{SS}$ is used as load. The output is connected to the center tap of the divider. For full drive strength, R1 = 550 Ω. For reduced drive strength, R1 = 1.6 kΩ. $C_L$ = 20 pF is connected to the output to $V_{SS}$.
(2) The output voltage reaches at least 10% and 90% $V_{CC}$ at the specified toggle frequency.


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## 5.9 Clock Specifications

Table 5-7 lists the characteristics of the XT1 oscillator in low-frequency mode.

**Table 5-7. Crystal Oscillator, XT1, Low-Frequency Mode(1)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $\Delta I_{DVCC.LF}$ | Differential XT1 oscillator crystal current consumption from lowest drive setting, LF mode | $f_{OSC}$ = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 1, $T_A$ = 25°C | 3.0 V | | 0.075 | | µA |
| | | $f_{OSC}$ = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 2, $T_A$ = 25°C | | | 0.170 | | |
| | | $f_{OSC}$ = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 3, $T_A$ = 25°C | | | 0.290 | | |
| $f_{XT1,LF0}$ | XT1 oscillator crystal frequency, LF mode | XTS = 0, XT1BYPASS = 0 | | | 32768 | | Hz |
| $f_{XT1,LF,SW}$ | XT1 oscillator logic-level square-wave input frequency, LF mode | XTS = 0, XT1BYPASS = 1(2) (3) | | 10 | 32.768 | 50 | kHz |
| $OA_{LF}$ | Oscillation allowance for LF crystals(4) | XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 0, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 6 pF | | | 210 | | kΩ |
| | | XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 1, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 12 pF | | | 300 | | |
| $C_{L,eff}$ | Integrated effective load capacitance, LF mode(5) | XTS = 0, XCAPx = 0(6) | | | 1 | | pF |
| | | XTS = 0, XCAPx = 1 | | | 5.5 | | |
| | | XTS = 0, XCAPx = 2 | | | 8.5 | | |
| | | XTS = 0, XCAPx = 3 | | | 12.0 | | |
| | Duty cycle, LF mode | XTS = 0, Measured at ACLK, $f_{XT1,LF}$ = 32768 Hz | | 30% | | 70% | |
| $f_{Fault,LF}$ | Oscillator fault frequency, LF mode(7) | XTS = 0(8) | | 10 | | 10000 | Hz |
| $t_{START,LF}$ | Start-up time, LF mode | $f_{OSC}$ = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 0, $T_A$ = 25°C, $C_{L,eff}$ = 6 pF | 3.0 V | | 1000 | | ms |
| | | $f_{OSC}$ = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 3, $T_A$ = 25°C, $C_{L,eff}$ = 12 pF | | | 500 | | |

(1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
- Keep the trace between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) When XT1BYPASS is set, XT1 circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger inputs section of this data sheet.

(3) Maximum frequency of operation of the entire device cannot be exceeded.

(4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the XT1DRIVEx settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
- For XT1DRIVEx = 0, $C_{L,eff} \le 6$ pF.
- For XT1DRIVEx = 1, 6 pF $\le C_{L,eff} \le 9$ pF.
- For XT1DRIVEx = 2, 6 pF $\le C_{L,eff} \le 10$ pF.
- For XT1DRIVEx = 3, $C_{L,eff} \ge 6$ pF.

(5) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Because the PCB adds additional capacitance, TI recommends verifying the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

(6) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

(7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag.

(8) Measured with logic-level input frequency but also applies to operation with crystals.

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Table 5-8 lists the characteristics of the VLO.

**Table 5-8. Internal Very-Low-Power Low-Frequency Oscillator (VLO)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{VLO}$ | VLO frequency | Measured at ACLK | 1.8 V to 3.6 V | 6 | 9.4 | 15 | kHz |
| $df_{VLO}/d_T$ | VLO frequency temperature drift | Measured at ACLK(1) | 1.8 V to 3.6 V | | 0.5 | | %/°C |
| $df_{VLO}/dV_{CC}$ | VLO frequency supply voltage drift | Measured at ACLK(2) | 1.8 V to 3.6 V | | 4 | | %/V |
| | Duty cycle | Measured at ACLK | 1.8 V to 3.6 V | 30% | | 70% | |

(1) Calculated using the box method: (MAX(–40°C to 85ºC) – MIN(–40°C to 85ºC)) / MIN(–40°C to 85ºC) / (85ºC – (–40ºC))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

Table 5-9 lists the characteristics of the REFO.

**Table 5-9. Internal Reference, Low-Frequency Oscillator (REFO)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{REFO}$ | REFO oscillator current consumption | $T_A$ = 25°C | 1.8 V to 3.6 V | | 3 | | µA |
| $f_{REFO}$ | REFO frequency calibrated | Measured at ACLK | 1.8 V to 3.6 V | | 32768 | | Hz |
| | REFO absolute tolerance calibrated | Full temperature range | 1.8 V to 3.6 V | | | ±3.5% | |
| | | $T_A$ = 25°C | 3 V | | | ±1.5% | |
| $df_{REFO}/d_T$ | REFO frequency temperature drift | Measured at ACLK(1) | 1.8 V to 3.6 V | | 0.01 | | %/°C |
| $df_{REFO}/dV_{CC}$ | REFO frequency supply voltage drift | Measured at ACLK(2) | 1.8 V to 3.6 V | | 1.0 | | %/V |
| | Duty cycle | Measured at ACLK | 1.8 V to 3.6 V | 40% | 50% | 60% | |
| $t_{START}$ | REFO start-up time | 40%/60% duty cycle | 1.8 V to 3.6 V | | 25 | | µs |

(1) Calculated using the box method: (MAX(–40°C to 85ºC) – MIN(–40°C to 85ºC)) / MIN(–40°C to 85ºC) / (85ºC – (–40ºC))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)


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Table 5-10 lists the frequency characteristics of the DCO.

**Table 5-10. DCO Frequency**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{DCO(0,0)}$ | DCO frequency (0, 0)(1) | DCORSELx = 0, DCOx = 0, MODx = 0 | 0.07 | | 0.20 | MHz |
| $f_{DCO(0,31)}$ | DCO frequency (0, 31)(1) | DCORSELx = 0, DCOx = 31, MODx = 0 | 0.70 | | 1.70 | MHz |
| $f_{DCO(1,0)}$ | DCO frequency (1, 0)(1) | DCORSELx = 1, DCOx = 0, MODx = 0 | 0.15 | | 0.36 | MHz |
| $f_{DCO(1,31)}$ | DCO frequency (1, 31)(1) | DCORSELx = 1, DCOx = 31, MODx = 0 | 1.47 | | 3.45 | MHz |
| $f_{DCO(2,0)}$ | DCO frequency (2, 0)(1) | DCORSELx = 2, DCOx = 0, MODx = 0 | 0.32 | | 0.75 | MHz |
| $f_{DCO(2,31)}$ | DCO frequency (2, 31)(1) | DCORSELx = 2, DCOx = 31, MODx = 0 | 3.17 | | 7.38 | MHz |
| $f_{DCO(3,0)}$ | DCO frequency (3, 0)(1) | DCORSELx = 3, DCOx = 0, MODx = 0 | 0.64 | | 1.51 | MHz |
| $f_{DCO(3,31)}$ | DCO frequency (3, 31)(1) | DCORSELx = 3, DCOx = 31, MODx = 0 | 6.07 | | 14.0 | MHz |
| $f_{DCO(4,0)}$ | DCO frequency (4, 0)(1) | DCORSELx = 4, DCOx = 0, MODx = 0 | 1.3 | | 3.2 | MHz |
| $f_{DCO(4,31)}$ | DCO frequency (4, 31)(1) | DCORSELx = 4, DCOx = 31, MODx = 0 | 12.3 | | 28.2 | MHz |
| $f_{DCO(5,0)}$ | DCO frequency (5, 0)(1) | DCORSELx = 5, DCOx = 0, MODx = 0 | 2.5 | | 6.0 | MHz |
| $f_{DCO(5,31)}$ | DCO frequency (5, 31)(1) | DCORSELx = 5, DCOx = 31, MODx = 0 | 23.7 | | 54.1 | MHz |
| $f_{DCO(6,0)}$ | DCO frequency (6, 0)(1) | DCORSELx = 6, DCOx = 0, MODx = 0 | 4.6 | | 10.7 | MHz |
| $f_{DCO(6,31)}$ | DCO frequency (6, 31)(1) | DCORSELx = 6, DCOx = 31, MODx = 0 | 39.0 | | 88.0 | MHz |
| $f_{DCO(7,0)}$ | DCO frequency (7, 0)(1) | DCORSELx = 7, DCOx = 0, MODx = 0 | 8.5 | | 19.6 | MHz |
| $f_{DCO(7,31)}$ | DCO frequency (7, 31)(1) | DCORSELx = 7, DCOx = 31, MODx = 0 | 60 | | 135 | MHz |
| $S_{DCORSEL}$ | Frequency step between range DCORSEL and DCORSEL + 1 | $S_{RSEL} = f_{DCO(DCORSEL+1,DCO)}/f_{DCO(DCORSEL,DCO)}$ | 1.2 | | 2.3 | ratio |
| $S_{DCO}$ | Frequency step between tap DCO and DCO + 1 | $S_{DCO} = f_{DCO(DCORSEL,DCO+1)}/f_{DCO(DCORSEL,DCO)}$ | 1.02 | | 1.12 | ratio |
| | Duty cycle | Measured at SMCLK | 40% | 50% | 60% | |
| $df_{DCO}/dT$ | DCO frequency temperature drift | $f_{DCO}$ = 1 MHz | | 0.1 | | %/°C |
| $df_{DCO}/dV_{CORE}$ | DCO frequency voltage drift | $f_{DCO}$ = 1 MHz | | 1.9 | | %/V |

(1) When selecting the proper DCO frequency range (DCORSELx), the target DCO frequency, $f_{DCO}$, should be set to reside within the range of $f_{DCO(n,\ 0),MAX} \le f_{DCO} \le f_{DCO(n,\ 31),MIN}$, where $f_{DCO(n,\ 0),MAX}$ represents the maximum frequency specified for the DCO frequency, range n, tap 0 (DCOx = 0) and $f_{DCO(n,31),MIN}$ represents the minimum frequency specified for the DCO frequency, range n, tap 31 (DCOx = 31). This ensures that the target DCO frequency resides within the range selected. If the actual $f_{DCO}$ frequency for the selected range causes the FLL or the application to select tap 0 or 31, the DCO fault flag is set to report that the selected range is at its minimum or maximum tap setting.

**Figure 5-10. Typical DCO Frequency**

## 5.10 Power-Management Module (PMM)

Table 5-11 lists the brownout characteristics of the PMM.

**Table 5-11. PMM, Brownout Reset (BOR)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{(DVCC_BOR_IT-)}$ | $BOR_H$ on voltage, $DV_{CC}$ falling level | $\lvert dDV_{CC}/d_t \rvert$ < 3 V/s | | | 1.45 | V |
| $V_{(DVCC_BOR_IT+)}$ | $BOR_H$ off voltage, $DV_{CC}$ rising level | $\lvert dDV_{CC}/d_t \rvert$ < 3 V/s | 0.80 | 1.30 | 1.50 | V |
| $V_{(DVCC_BOR_hys)}$ | $BOR_H$ hysteresis | | 50 | | 250 | mV |
| $t_{RESET}$ (1) | Pulse duration required at $\overline{RST}$/NMI pin to accept a reset | | 2 | | | µs |

(1) Pulse much shorter than 2 µs might trigger reset.

Table 5-12 lists the core voltage characteristics of the PMM.

**Table 5-12. PMM, Core Voltage**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CORE3}$(AM) | Core voltage, active mode, PMMCOREV = 3 | 2.4 V ≤ $DV_{CC}$ ≤ 3.6 V | | 1.93 | | V |
| $V_{CORE2}$(AM) | Core voltage, active mode, PMMCOREV = 2 | 2.2 V ≤ $DV_{CC}$ ≤ 3.6 V | | 1.83 | | V |
| $V_{CORE1}$(AM) | Core voltage, active mode, PMMCOREV = 1 | 2.0 V ≤ $DV_{CC}$ ≤ 3.6 V | | 1.62 | | V |
| $V_{CORE0}$(AM) | Core voltage, active mode, PMMCOREV = 0 | 1.8 V ≤ $DV_{CC}$ ≤ 3.6 V | | 1.42 | | V |
| $V_{CORE3}$(LPM) | Core voltage, low-current mode, PMMCOREV = 3 | 2.4 V ≤ $DV_{CC}$ ≤ 3.6 V | | 1.96 | | V |
| $V_{CORE2}$(LPM) | Core voltage, low-current mode, PMMCOREV = 2 | 2.2 V ≤ $DV_{CC}$ ≤ 3.6 V | | 1.94 | | V |
| $V_{CORE1}$(LPM) | Core voltage, low-current mode, PMMCOREV = 1 | 2.0 V ≤ $DV_{CC}$ ≤ 3.6 V | | 1.74 | | V |
| $V_{CORE0}$(LPM) | Core voltage, low-current mode, PMMCOREV = 0 | 1.8 V ≤ $DV_{CC}$ ≤ 3.6 V | | 1.54 | | V |


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Table 5-13 lists the characteristics of the high-side SVS.

**Table 5-13. PMM, SVS High Side**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{(SVSH)}$ | SVS current consumption | SVSHE = 0, $DV_{CC}$ = 3.6 V | | 0 | | nA |
| | | SVSHE = 1, $DV_{CC}$ = 3.6 V, SVSHFP = 0 | | 200 | | |
| | | SVSHE = 1, $DV_{CC}$ = 3.6 V, SVSHFP = 1 | | 1.5 | | µA |
| $V_{(SVSH_IT-)}$ | $SVS_H$ on voltage level(1) | SVSHE = 1, SVSHRVL = 0 | 1.60 | 1.65 | 1.70 | V |
| | | SVSHE = 1, SVSHRVL = 1 | 1.77 | 1.84 | 1.90 | |
| | | SVSHE = 1, SVSHRVL = 2 | 1.97 | 2.04 | 2.10 | |
| | | SVSHE = 1, SVSHRVL = 3 | 2.09 | 2.16 | 2.23 | |
| $V_{(SVSH_IT+)}$ | $SVS_H$ off voltage level(1) | SVSHE = 1, SVSMHRRL = 0 | 1.68 | 1.74 | 1.80 | V |
| | | SVSHE = 1, SVSMHRRL = 1 | 1.89 | 1.95 | 2.01 | |
| | | SVSHE = 1, SVSMHRRL = 2 | 2.08 | 2.14 | 2.21 | |
| | | SVSHE = 1, SVSMHRRL = 3 | 2.21 | 2.27 | 2.34 | |
| | | SVSHE = 1, SVSMHRRL = 4 | 2.35 | 2.41 | 2.49 | |
| | | SVSHE = 1, SVSMHRRL = 5 | 2.65 | 2.72 | 2.80 | |
| | | SVSHE = 1, SVSMHRRL = 6 | 2.96 | 3.04 | 3.13 | |
| | | SVSHE = 1, SVSMHRRL = 7 | 2.96 | 3.04 | 3.13 | |
| $t_{pd(SVSH)}$ | $SVS_H$ propagation delay | SVSHE = 1, $dV_{DVCC}/dt$ = 10 mV/µs, SVSHFP = 1 | | 2.5 | | µs |
| | | SVSHE = 1, $dV_{DVCC}/dt$ = 1 mV/µs, SVSHFP = 0 | | 20 | | |
| $t_{(SVSH)}$ | $SVS_H$ on or off delay time | SVSHE = 0 → 1, SVSHFP = 1 | | 12.5 | | µs |
| | | SVSHE = 0 → 1, SVSHFP = 0 | | 100 | | |
| $dV_{DVCC}/dt$ | $DV_{CC}$ rise time | | 0 | | 1000 | V/s |

(1) The $SVS_H$ settings available depend on the VCORE (PMMCOREVx) setting. Refer to the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* on recommended settings and usage.

Table 5-14 lists the characteristics of the high-side SVM.

**Table 5-14. PMM, SVM High Side**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{(SVMH)}$ | $SVM_H$ current consumption | SVMHE = 0, $DV_{CC}$ = 3.6 V | | 0 | | nA |
| | | SVMHE = 1, $DV_{CC}$ = 3.6 V, SVMHFP = 0 | | 200 | | |
| | | SVMHE = 1, $DV_{CC}$ = 3.6 V, SVMHFP = 1 | | 1.5 | | µA |
| $V_{(SVMH)}$ | $SVM_H$ on or off voltage level(1) | SVMHE = 1, SVSMHRRL = 0 | 1.68 | 1.74 | 1.80 | V |
| | | SVMHE = 1, SVSMHRRL = 1 | 1.89 | 1.95 | 2.01 | |
| | | SVMHE = 1, SVSMHRRL = 2 | 2.08 | 2.14 | 2.21 | |
| | | SVMHE = 1, SVSMHRRL = 3 | 2.21 | 2.27 | 2.34 | |
| | | SVMHE = 1, SVSMHRRL = 4 | 2.35 | 2.41 | 2.49 | |
| | | SVMHE = 1, SVSMHRRL = 5 | 2.65 | 2.72 | 2.80 | |
| | | SVMHE = 1, SVSMHRRL = 6 | 2.96 | 3.04 | 3.13 | |
| | | SVMHE = 1, SVSMHRRL = 7 | 2.96 | 3.04 | 3.13 | |
| | | SVMHE = 1, SVMHOVPE = 1 | | 3.79 | | |
| $t_{pd(SVMH)}$ | $SVM_H$ propagation delay | SVMHE = 1, $dV_{DVCC}/dt$ = 10 mV/µs, SVMHFP = 1 | | 2.5 | | µs |
| | | SVMHE = 1, $dV_{DVCC}/dt$ = 1 mV/µs, SVMHFP = 0 | | 20 | | |
| $t_{(SVMH)}$ | $SVM_H$ on or off delay time | SVMHE = 0 → 1, SVMHFP = 1 | | 12.5 | | µs |
| | | SVMHE = 0 → 1, SVMHFP = 0 | | 100 | | |

(1) The $SVM_H$ settings available depend on the VCORE (PMMCOREVx) setting. Refer to the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* on recommended settings and usage.

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Table 5-15 lists the characteristics of the low-side SVS.

**Table 5-15. PMM, SVS Low Side**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{(SVSL)}$ | $SVS_L$ current consumption | SVSLE = 0, PMMCOREV = 2 | | 0 | | nA |
| | | SVSLE = 1, PMMCOREV = 2, SVSLFP = 0 | | 200 | | |
| | | SVSLE = 1, PMMCOREV = 2, SVSLFP = 1 | | 1.5 | | µA |
| $t_{pd(SVSL)}$ | $SVS_L$ propagation delay | SVSLE = 1, $dV_{CORE}/dt$ = 10 mV/µs, SVSLFP = 1 | | 2.5 | | µs |
| | | SVSLE = 1, $dV_{CORE}/dt$ = 1 mV/µs, SVSLFP = 0 | | 20 | | |
| $t_{(SVSL)}$ | $SVS_L$ on or off delay time | SVSLE = 0 → 1, SVSLFP = 1 | | 12.5 | | µs |
| | | SVSLE = 0 → 1, SVSLFP = 0 | | 100 | | |

Table 5-16 lists the characteristics of the low-side SVM.

**Table 5-16. PMM, SVM Low Side**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{(SVML)}$ | $SVM_L$ current consumption | SVMLE = 0, PMMCOREV = 2 | | 0 | | nA |
| | | SVMLE = 1, PMMCOREV = 2, SVMLFP = 0 | | 200 | | |
| | | SVMLE = 1, PMMCOREV = 2, SVMLFP = 1 | | 1.5 | | µA |
| $t_{pd(SVML)}$ | $SVM_L$ propagation delay | SVMLE = 1, $dV_{CORE}/dt$ = 10 mV/µs, SVMLFP = 1 | | 2.5 | | µs |
| | | SVMLE = 1, $dV_{CORE}/dt$ = 1 mV/µs, SVMLFP = 0 | | 20 | | |
| $t_{(SVML)}$ | $SVM_L$ on or off delay time | SVMLE = 0 → 1, SVMLFP = 1 | | 12.5 | | µs |
| | | SVMLE = 0 → 1, SVMLFP = 0 | | 100 | | |

Table 5-17 lists the wake-up times.

**Table 5-17. Wake-up Times From Low-Power Modes and Reset**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{WAKE-UP-FAST}$ | Wake-up time from LPM2, LPM3, or LPM4 to active mode(1) | PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 1 | $f_{MCLK}$ ≥ 4 MHz | | 3 | 5 | µs |
| | | | 1 MHz < $f_{MCLK}$ < 4 MHz | | 4 | 6 | |
| $t_{WAKE-UP-SLOW}$ | Wake-up time from LPM2, LPM3, or LPM4 to active mode(2)(3) | PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 0 | | | 150 | 160 | µs |
| $t_{WAKE-UP-LPM4.5}$ | Wake-up time from LPM4.5 to active mode(4) | | | | 2 | 3 | ms |
| $t_{WAKE-UP-RESET}$ | Wake-up time from $\overline{RST}$ or BOR event to active mode(4) | | | | 2 | 3 | ms |

(1) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor ($SVS_L$) and low-side monitor ($SVM_L$). $t_{WAKE-UP-FAST}$ is possible with $SVS_L$ and $SVM_L$ in full performance mode or disabled. For specific register settings, see the *Low-Side SVS and SVM Control and Performance Mode Selection* section in the *Power Management Module and Supply Voltage Supervisor* chapter of the *MSP430x5xx and MSP430x6xx Family User's Guide*.

(2) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor ($SVS_L$) and low-side monitor ($SVM_L$). $t_{WAKE-UP-SLOW}$ is set with $SVS_L$ and $SVM_L$ in normal mode (low current mode). For specific register settings, see the *Low-Side SVS and SVM Control and Performance Mode Selection* section in the *Power Management Module and Supply Voltage Supervisor* chapter of the *MSP430x5xx and MSP430x6xx Family User's Guide*.

(3) The wake-up times from LPM0 and LPM1 to AM are not specified. They are proportional to MCLK cycle time but are not affected by the performance mode settings as for LPM2, LPM3, and LPM4.

(4) This value represents the time from the wake-up event to the reset vector execution.


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## 5.11 Auxiliary Supplies

Table 5-18 lists the operating conditions of the auxiliary supplies.

**Table 5-18. Auxiliary Supplies, Recommended Operating Conditions**

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range for all supplies at pins DVCC, AVCC, AUXVCC1, AUXVCC2, AUXVCC3 | | 1.8 | | 3.6 | V |
| $V_{DSYS}$ | Digital system supply voltage range, $V_{DSYS} = V_{CC} – R_{ON} \times I_{LOAD}$ | PMMCOREVx = 0 | 1.8 | | 3.6 | V |
| | | PMMCOREVx = 1 | 2.0 | | 3.6 | |
| | | PMMCOREVx = 2 | 2.2 | | 3.6 | |
| | | PMMCOREVx = 3 | 2.4 | | 3.6 | |
| $V_{ASYS}$ | Analog system supply voltage range, $V_{ASYS} = V_{CC} – R_{ON} \times I_{LOAD}$ | | See module specifications | | | V |
| $C_{VCC}$, $C_{AUX1/2}$ | Recommended capacitor at pins DVCC, AVCC, AUXVCC1, AUXVCC2 | | | 4.7 | | µF |
| $C_{VSYS}$ | Recommended capacitor at pins VDSYS and VASYS | | | 4.7 | | µF |
| $C_{VCORE}$ | Recommended capacitance at VCORE pin | | | 0.47 | | µF |
| $C_{AUX3}$ | Recommended capacitor at pin AUXVCC3 | | | 0.47 | | µF |

Table 5-19 lists the current consumption of AUX3.

**Table 5-19. Auxiliary Supplies, AUXVCC3 (Backup Subsystem) Currents**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $I_{AUX3,RTCon}$ | AUXVCC3 current with RTC enabled | RTC and 32-kHz oscillator in backup subsystem enabled | 3 V | 25°C | | | 0.83 | µA |
| | | | | 85°C | | | 0.95 | |
| $I_{AUX3,RTCoff}$ | AUXVCC3 current with RTC disabled | RTC and 32-kHz oscillator in backup subsystem disabled | 3 V | 25°C | | | 110 | nA |
| | | | | 85°C | | | 165 | |

Table 5-20 lists the characteristics of the auxiliary supply monitor.

**Table 5-20. Auxiliary Supplies, Auxiliary Supply Monitor**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{CC,Monitor}$ | Average supply current for monitoring circuitry drawn from VDSYS | LOCKAUX = 0, AUXMRx = 0, AUX0MD = 0, AUX1MD = 0, AUX2MD = 1, VDSYS = DVCC, VASYS = AVCC, Current measured at VDSYS pin (also see Figure 5-11) | 3 V | | | 0.70 | µA |
| $I_{Meas,Monitor}$ | Average current drawn from monitored supply during measurement cycle | LOCKAUX = 0, AUXMRx = 0, AUX0MD = 0, AUX1MD = 0, AUX2MD = 1, VDSYS = DVCC, VASYS = AVCC, AUXVCC1 = 3 V, Current measured at AUXVCC1 pin (also see Figure 5-12) | | | | 0.11 | µA |
| $V_{Monitor}$ | Auxiliary supply threshold level | AUXLVLx = 0 | | 1.67 | 1.74 | 1.80 | V |
| | | AUXLVLx = 1 | | 1.87 | 1.95 | 2.01 | |
| | | AUXLVLx = 2 | | 2.06 | 2.14 | 2.21 | |
| | | AUXLVLx = 3 | | 2.19 | 2.27 | 2.33 | |
| | | AUXLVLx = 4 | | 2.33 | 2.41 | 2.48 | |
| | | AUXLVLx = 5 | | 2.63 | 2.72 | 2.79 | |
| | | AUXLVLx = 6 | | 2.91 | 3.02 | 3.10 | |
| | | AUXLVLx = 7 | | 2.91 | 3.02 | 3.10 | |

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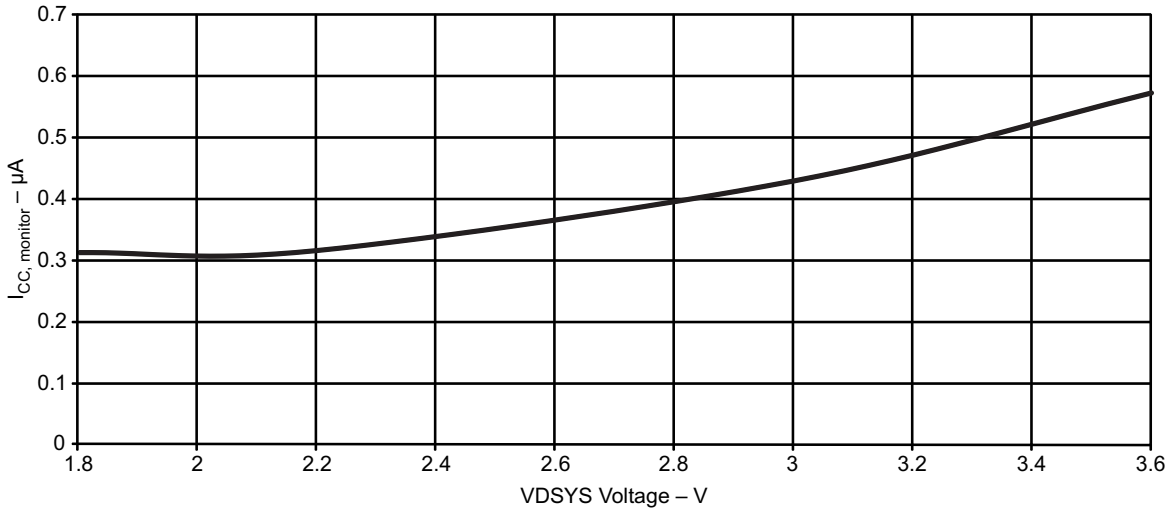


**Figure 5-11. VDSYS Voltage vs $I_{CC,Monitor}$**

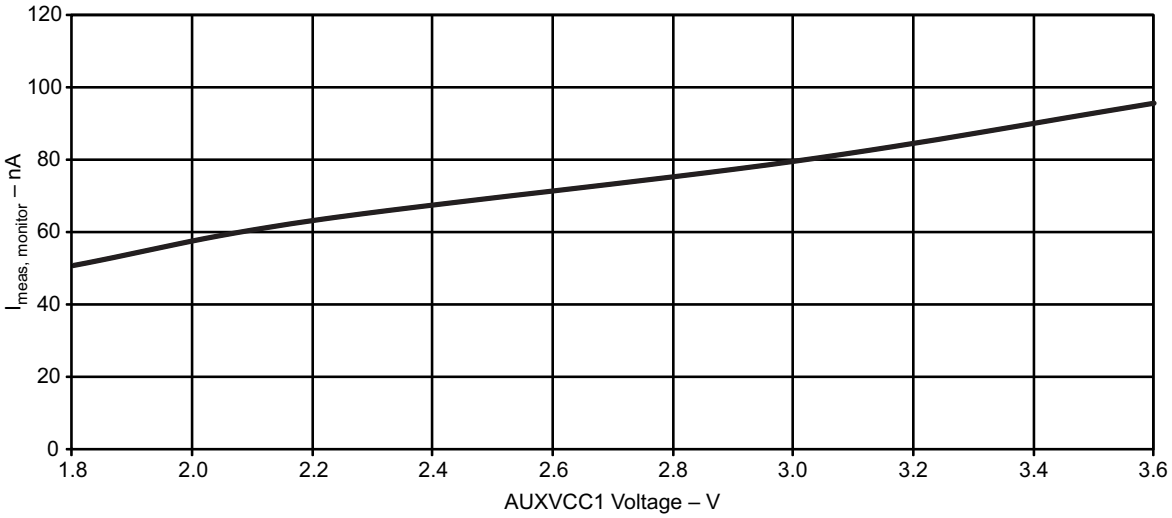


**Figure 5-12. AUXVCC1 Voltage vs $I_{Meas,Monitor}$**

Table 5-21 lists the ON-resistance characteristics of the auxiliary supplies.

**Table 5-21. Auxiliary Supplies, Switch ON-Resistance**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $R_{ON,DVCC}$ | ON-resistance of switch between DVCC and VDSYS | $I_{LOAD} = I_{CORE} + I_{IO}$ = 10 mA + 10 mA = 20 mA | | | 5 | Ω |
| $R_{ON,DAUX1}$ | ON-resistance of switch between AUXVCC1 and VDSYS | $I_{LOAD} = I_{CORE} + I_{IO}$ = 10 mA + 10 mA = 20 mA | | | 5 | Ω |
| $R_{ON,DAUX2}$ | ON-resistance of switch between AUXVCC2 and VDSYS | $I_{LOAD} = I_{CORE} + I_{IO}$ = 10 mA + 10 mA = 20 mA | | | 5 | Ω |
| $R_{ON,AVCC}$ | ON-resistance of switch between AVCC and $V_{ASYS}$ | $I_{LOAD} = I_{Modules}$ = 10 mA | | | 5 | Ω |
| $R_{ON,AAUX1}$ | ON-resistance of switch between AUXVCC1 and $V_{ASYS}$ | $I_{LOAD} = I_{Modules}$ = 5 mA | | | 20 | Ω |
| $R_{ON,AAUX2}$ | ON-resistance of switch between AUXVCC2 and $V_{ASYS}$ | $I_{LOAD} = I_{Modules}$ = 5 mA | | | 20 | Ω |


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Table 5-22 lists the switching times of the auxiliary supplies.

**Table 5-22. Auxiliary Supplies, Switching Time**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{Switch}$ | Time from occurence of trigger (SVM or software) to "new" supply connected to system supplies | | 100 | ns |
| $t_{Recover}$ | "Recovery time" after a switch over took place; during this time, no further switching takes place | 200 | 450 | µs |

Table 5-23 lists the switch leakage of the auxiliary supplies.

**Table 5-23. Auxiliary Supplies, Switch Leakage**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{SW,Lkg}$ | Current into DVCC, AVCC, AUXVCC1, or AUXVCC2 if not selected | Per supply (but not the highest supply) | | 50 | 100 | nA |
| $I_{Vmax}$ | Current drawn from highest supply | | | 450 | 730 | nA |

Table 5-24 lists the characteristics of the auxiliary supplies to ADC10_A.

**Table 5-24. Auxiliary Supplies, Auxiliary Supplies to ADC10_A**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_3$ | Supply voltage divider $V_3 = V_{Supply}/3$ | | | 1.8 V | 0.58 | 0.60 | 0.62 | V |
| | | | | 3.0 V | 0.98 | 1.00 | 1.02 | |
| | | | | 3.6 V | 1.18 | 1.20 | 1.22 | |
| $R_{V3}$ | Load resistance | AUXADCRx = 0 | | | | | 18 | kΩ |
| | | AUXADCRx = 1 | | | | | 1.5 | |
| | | AUXADCRx = 2 | | | | | 0.6 | |
| $t_{Sample,V3}$ | Sampling time required if $V_3$ selected | AUXADC = 1, ADC10ON = 1, INCH = 0Ch, Error of conversion result ≤ 1 LSB | AUXADCRx = 0 | | 1000 | | | ns |
| | | | AUXADCRx = 1 | | 1000 | | | |
| | | | AUXADCRx = 2 | | 1000 | | | |

Table 5-25 lists the charge limiting resistor characteristics of the auxiliary supplies.

**Table 5-25. Auxiliary Supplies, Charge Limiting Resistor**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $R_{CHARGE}$ | Charge limiting resistor | AUXCHCx = 1 | 3 V | | | 5 | kΩ |
| | | AUXCHCx = 2 | 3 V | | | 10 | |
| | | AUXCHCx = 3 | 3 V | | | 20 | |

## 5.12 Timer_A

Table 5-26 lists the characteristics of the Timer_A.

**Table 5-26. Timer_A**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{TA}$ | Timer_A input clock frequency | Internal: SMCLK or ACLK,<br>External: TACLK,<br>Duty cycle = 50% ±10% | 1.8 V, 3 V | | 25 | MHz |
| $t_{TA,cap}$ | Timer_A capture timing | All capture inputs, minimum pulse duration required for capture | 1.8 V, 3 V | 20 | | ns |

## 5.13 eUSCI

**Table 5-27. eUSCI (UART Mode) Clock Frequency**

| PARAMETER | | CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{eUSCI}$ | eUSCI input clock frequency | Internal: SMCLK or ACLK,<br>External: UCLK,<br>Duty cycle = 50% ±10% | | | $f_{SYSTEM}$ | MHz |
| $f_{BITCLK}$ | BITCLK clock frequency<br>(equals baud rate in MBaud) | | | | 5 | MHz |

Table 5-28 lists the switching characteristics of the eUSCI in UART mode.

**Table 5-28. eUSCI (UART Mode) Switching Characteristics**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_t$ | UART receive deglitch time(1) | UCGLITx = 0 | 2 V, 3 V | 10 | 15 | 25 | ns |
| | | UCGLITx = 1 | | 30 | 50 | 85 | |
| | | UCGLITx = 2 | | 50 | 80 | 150 | |
| | | UCGLITx = 3 | | 70 | 120 | 200 | |

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized their duration should exceed the maximum specification of the deglitch time.


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Table 5-29 lists the supported clock frequencies of the eUSCI in SPI master mode.

**Table 5-29. eUSCI (SPI Master Mode) Clock Frequency**

| PARAMETER | | CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{eUSCI}$ | eUSCI input clock frequency | Internal: SMCLK or ACLK,<br>Duty cycle = 50% ±10% | | | $f_{SYSTEM}$ | MHz |

Table 5-30 lists the switching characteristics of the eUSCI in SPI master mode.

**Table 5-30. eUSCI (SPI Master Mode) Switching Characteristics**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{STE,LEAD}$ | STE lead time, STE active to clock | UCSTEM = 0, UCMODEx = 01 or 10 | 2 V, 3 V | 150 | | ns |
| | | UCSTEM = 1, UCMODEx = 01 or 10 | 2 V, 3 V | 150 | | |
| $t_{STE,LAG}$ | STE lag time, Last clock to STE inactive | UCSTEM = 0, UCMODEx = 01 or 10 | 2 V, 3 V | 200 | | ns |
| | | UCSTEM = 1, UCMODEx = 01 or 10 | 2 V, 3 V | 200 | | |
| $t_{STE,ACC}$ | STE access time, STE active to SIMO data out | UCSTEM = 0, UCMODEx = 01 or 10 | 2 V | | 50 | ns |
| | | | 3 V | | 30 | |
| | | UCSTEM = 1, UCMODEx = 01 or 10 | 2 V | | 50 | |
| | | | 3 V | | 30 | |
| $t_{STE,DIS}$ | STE disable time, STE inactive to SIMO high impedance | UCSTEM = 0, UCMODEx = 01 or 10 | 2 V | | 40 | ns |
| | | | 3 V | | 25 | |
| | | UCSTEM = 1, UCMODEx = 01 or 10 | 2 V | | 40 | |
| | | | 3 V | | 25 | |
| $t_{SU,MI}$ | SOMI input data setup time | | 2 V | 50 | | ns |
| | | | 3 V | 30 | | |
| $t_{HD,MI}$ | SOMI input data hold time | | 2 V | 0 | | ns |
| | | | 3 V | 0 | | |
| $t_{VALID,MO}$ | SIMO output data valid time(2) | UCLK edge to SIMO valid, $C_L$ = 20 pF | 2 V | | 9 | ns |
| | | | 3 V | | 5 | |
| $t_{HD,MO}$ | SIMO output data hold time(3) | $C_L$ = 20 pF | 2 V | 0 | | ns |
| | | | 3 V | 0 | | |

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $tL_{O/HI} = \max(t_{VALID,MO(eUSCI)} + t_{SU,SI(Slave)}, t_{SU,MI(eUSCI)} + t_{VALID,SO(Slave)})$
For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, see the SPI parameters of the attached slave.

(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-13 and Figure 5-14.

(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in Figure 5-13 and Figure 5-14.

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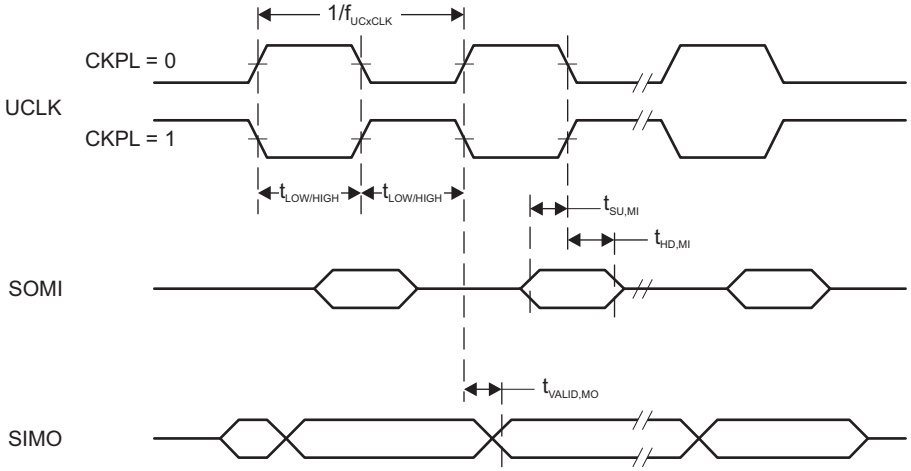


**Figure 5-13. SPI Master Mode, CKPH = 0**

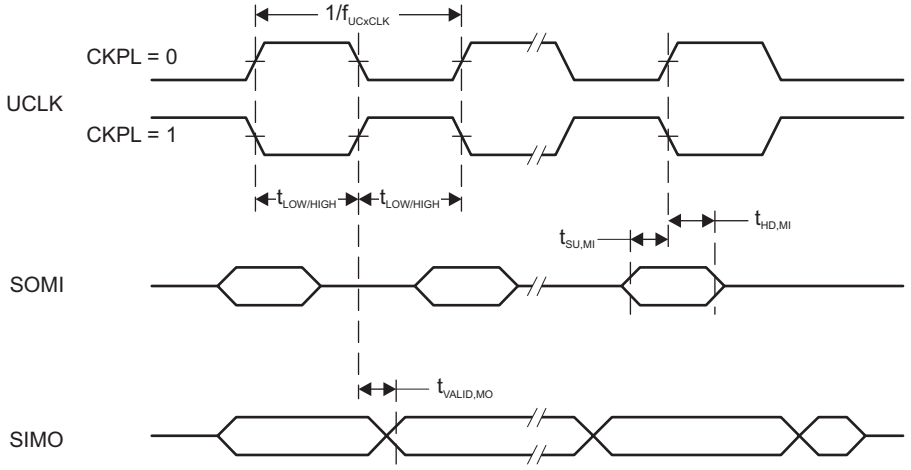


**Figure 5-14. SPI Master Mode, CKPH = 1**


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Table 5-31 lists the switching characteristics of the eUSCI in SPI slave mode.

**Table 5-31. eUSCI (SPI Slave Mode)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{STE,LEAD}$ | STE lead time, STE active to clock | | 2.0 V | 4 | | | ns |
| | | | 3.0 V | 3 | | | |
| $t_{STE,LAG}$ | STE lag time, Last clock to STE inactive | | 2.0 V | 0 | | | ns |
| | | | 3.0 V | 0 | | | |
| $t_{STE,ACC}$ | STE access time, STE active to SOMI data out | | 2.0 V | | | 46 | ns |
| | | | 3.0 V | | | 24 | |
| $t_{STE,DIS}$ | STE disable time, STE inactive to SOMI high impedance | | 2.0 V | | | 38 | ns |
| | | | 3.0 V | | | 25 | |
| $t_{SU,SI}$ | SIMO input data setup time | | 2.0 V | 2 | | | ns |
| | | | 3.0 V | 1 | | | |
| $t_{HD,SI}$ | SIMO input data hold time | | 2.0 V | 2 | | | ns |
| | | | 3.0 V | 2 | | | |
| $t_{VALID,SO}$ | SOMI output data valid time(2) | UCLK edge to SOMI valid, $C_L$ = 20 pF | 2.0 V | | | 55 | ns |
| | | | 3.0 V | | | 32 | |
| $t_{HD,SO}$ | SOMI output data hold time(3) | $C_L$ = 20 pF | 2.0 V | 24 | | | ns |
| | | | 3.0 V | 16 | | | |

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $tL_{O/HI} = max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached master.
(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-15 and Figure 5-16.
(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams inFigure 5-15 and Figure 5-16.

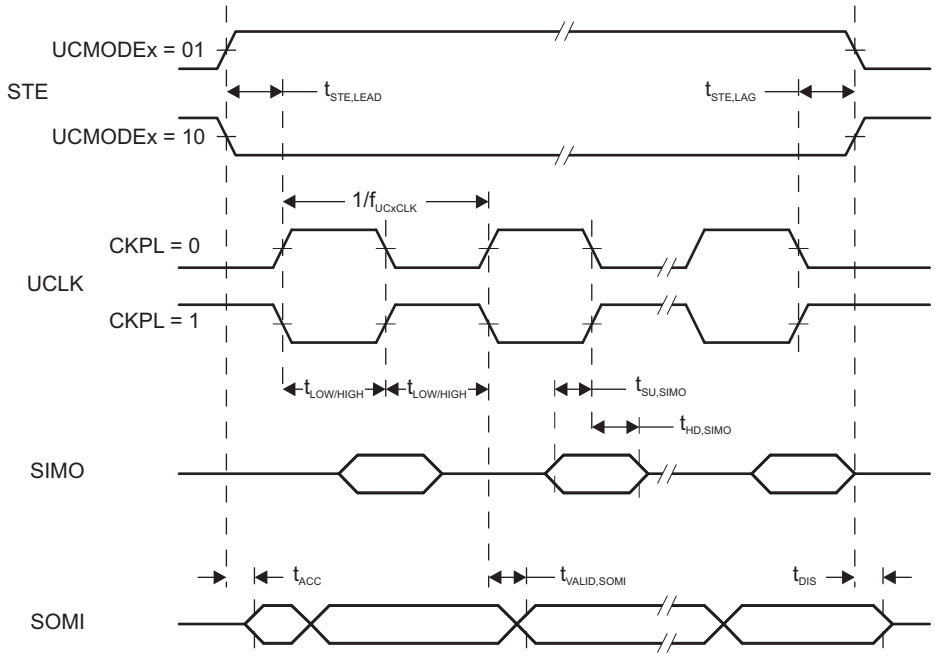


**Figure 5-15. SPI Slave Mode, CKPH = 0**

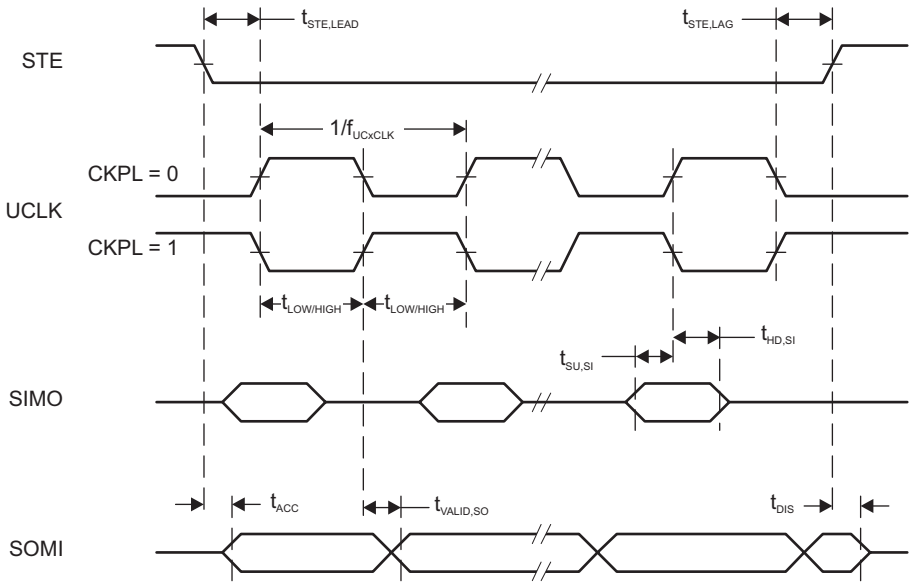


**Figure 5-16. SPI Slave Mode, CKPH = 1**


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Table 5-32 lists the switching characteristics of the eUSCI in I²C mode.

**Table 5-32. eUSCI (I²C Mode)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-17)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{eUSCI}$ | eUSCI input clock frequency | Internal: SMCLK, ACLK<br>External: UCLK<br>Duty cycle = 50% ±10% | | | | $f_{SYSTEM}$ | MHz |
| $f_{SCL}$ | SCL clock frequency | | 2 V, 3 V | 0 | | 400 | kHz |
| $t_{HD,STA}$ | Hold time (repeated) START | $f_{SCL}$ = 100 kHz | 2 V, 3 V | 5.1 | | | µs |
| | | $f_{SCL}$ > 100 kHz | | 1.5 | | | |
| $t_{SU,STA}$ | Setup time for a repeated START | $f_{SCL}$ = 100 kHz | 2 V, 3 V | 5.1 | | | µs |
| | | $f_{SCL}$ > 100 kHz | | 1.4 | | | |
| $t_{HD,DAT}$ | Data hold time | | 2 V, 3 V | 0.4 | | | µs |
| $t_{SU,DAT}$ | Data setup time | $f_{SCL}$ = 100 kHz | 2 V, 3 V | 5.0 | | | µs |
| | | $f_{SCL}$ > 100 kHz | 2 V, 3 V | 1.3 | | | |
| $t_{SU,STO}$ | Setup time for STOP | $f_{SCL}$ = 100 kHz | 2 V, 3 V | 5.2 | | | µs |
| | | $f_{SCL}$ > 100 kHz | | 1.7 | | | |
| $t_{SP}$ | Pulse duration of spikes suppressed by input filter | UCGLITx = 0 | 2 V, 3 V | 75 | | 220 | ns |
| | | UCGLITx = 1 | | 35 | | 120 | |
| | | UCGLITx = 2 | | 30 | | 60 | |
| | | UCGLITx = 3 | | 20 | | 35 | |
| $t_{TIMEOUT}$ | Clock low time-out | UCCLTOx = 1 | 2 V, 3 V | | 30 | | ms |
| | | UCCLTOx = 2 | | | 33 | | |
| | | UCCLTOx = 3 | | | 37 | | |

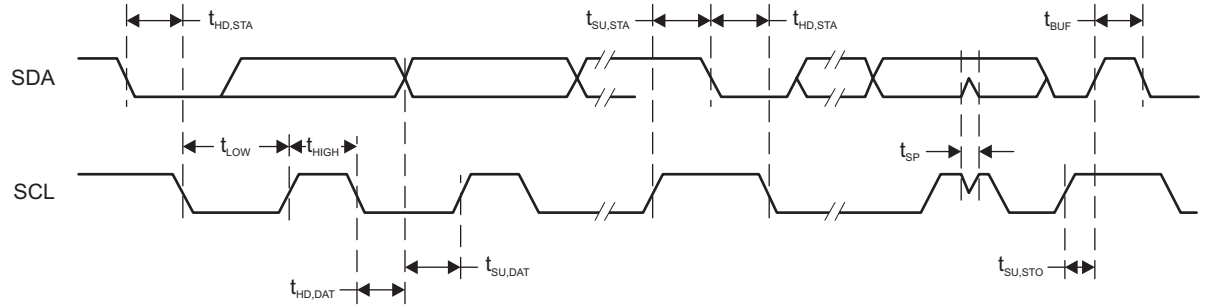


**Figure 5-17. I²C Mode Timing**

## 5.14 LCD Controller

Table 5-33 lists the recommended operating conditions of the LCD_C.

**Table 5-33. LCD_C Recommended Operating Conditions**

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC,LCD_C,CP\ en,3.6}$ | Supply voltage range, charge pump enabled, $V_{LCD} \le 3.6$ V | LCDCPEN = 1, 0000 < VLCDx ≤ 1111 (charge pump enabled, $V_{LCD} \le 3.6$ V) | 2.2 | | 3.6 | V |
| $V_{CC,LCD_C,CP\ en,3.3}$ | Supply voltage range, charge pump enabled, $V_{LCD} \le 3.3$ V | LCDCPEN = 1, 0000 < VLCDx ≤ 1100 (charge pump enabled, $V_{LCD} \le 3.3$ V) | 2.0 | | 3.6 | V |
| $V_{CC,LCD_C,int.\ bias}$ | Supply voltage range, internal biasing, charge pump disabled | LCDCPEN = 0, VLCDEXT = 0 | 2.4 | | 3.6 | V |
| $V_{CC,LCD_C,ext.\ bias}$ | Supply voltage range, external biasing, charge pump disabled | LCDCPEN = 0, VLCDEXT = 0 | 2.4 | | 3.6 | V |
| $V_{CC,LCD_C,VLCDEXT}$ | Supply voltage range, external LCD voltage, internal or external biasing, charge pump disabled | LCDCPEN = 0, VLCDEXT = 1 | 2.0 | | 3.6 | V |
| $V_{LCDCAP/R33}$ | External LCD voltage at LCDCAP/R33, internal or external biasing, charge pump disabled | LCDCPEN = 0, VLCDEXT = 1 | 2.4 | | 3.6 | V |
| $C_{LCDCAP}$ | Capacitor on LCDCAP when charge pump enabled | LCDCPEN = 1, VLCDx > 0000 (charge pump enabled) | | 4.7 | 10 | µF |
| $f_{LCD}$ | LCD frequency range | $f_{FRAME}$ = 1/(2 × mux) × $f_{LCD}$ with mux = 1 (static) to 8 | 0 | | 1024 | Hz |
| $f_{FRAME,4mux}$ | LCD frame frequency range | $f_{FRAME,4mux}$(MAX) = 1/(2 × 4) × $f_{LCD}$(MAX) = 1/(2 × 4) × 1024 Hz | | | 128 | Hz |
| $f_{FRAME,8mux}$ | LCD frame frequency range | $f_{FRAME,8mux}$(MAX) = 1/(2 × 4) × $f_{LCD}$(MAX) = 1/(2 × 8) × 1024 Hz | | | 64 | Hz |
| $f_{ACLK,in}$ | ACLK input frequency range | | 30 | 32 | 40 | kHz |
| $C_{Panel}$ | Panel capacitance | 100-Hz frame frequency | | | 10000 | pF |
| $V_{R33}$ | Analog input voltage at R33 | LCDCPEN = 0, VLCDEXT = 1 | 2.4 | | $V_{CC}$ + 0.2 | V |
| $V_{R23,1/3bias}$ | Analog input voltage at R23 | LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 0 | $V_{R13}$ | $V_{R03}$ + 2/3 × ($V_{R33}$-$V_{R03}$) | $V_{R33}$ | V |
| $V_{R13,1/3bias}$ | Analog input voltage at R13 with 1/3 biasing | LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 0 | $V_{R03}$ | $V_{R03}$ + 1/3 × ($V_{R33}$-$V_{R03}$) | $V_{R23}$ | V |
| $V_{R13,1/2bias}$ | Analog input voltage at R13 with 1/2 biasing | LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 1 | $V_{R03}$ | $V_{R03}$ + 1/2 × ($V_{R33}$-$V_{R03}$) | $V_{R33}$ | V |
| $V_{R03}$ | Analog input voltage at R03 | R0EXT = 1 | $V_{SS}$ | | | V |
| $V_{LCD}$–$V_{R03}$ | Voltage difference between $V_{LCD}$ and R03 | LCDCPEN = 0, R0EXT = 1 | 2.4 | | $V_{CC}$ + 0.2 | V |
| $V_{LCDREF/R13}$ | External LCD reference voltage applied at LCDREF/R13 | VLCDREFx = 01 | 0.8 | 1.2 | 1.5 | V |


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Table 5-34 lists the characteristics of the LCD_C.

**Table 5-34. LCD_C Electrical Characteristics**

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{LCD}$ | LCD voltage | VLCDx = 0000, VLCDEXT = 0 | 2.4 V to 3.6 V | | $V_{CC}$ | | V |
| | | LCDCPEN = 1, VLCDx = 0001 | 2 V to 3.6 V | | 2.58 | | |
| | | LCDCPEN = 1, VLCDx = 0010 | 2 V to 3.6 V | | 2.64 | | |
| | | LCDCPEN = 1, VLCDx = 0011 | 2 V to 3.6 V | | 2.71 | | |
| | | LCDCPEN = 1, VLCDx = 0100 | 2 V to 3.6 V | | 2.78 | | |
| | | LCDCPEN = 1, VLCDx = 0101 | 2 V to 3.6 V | | 2.83 | | |
| | | LCDCPEN = 1, VLCDx = 0110 | 2 V to 3.6 V | | 2.90 | | |
| | | LCDCPEN = 1, VLCDx = 0111 | 2 V to 3.6 V | | 2.96 | | |
| | | LCDCPEN = 1, VLCDx = 1000 | 2 V to 3.6 V | | 3.02 | | |
| | | LCDCPEN = 1, VLCDx = 1001 | 2 V to 3.6 V | | 3.07 | | |
| | | LCDCPEN = 1, VLCDx = 1010 | 2 V to 3.6 V | | 3.14 | | |
| | | LCDCPEN = 1, VLCDx = 1011 | 2 V to 3.6 V | | 3.21 | | |
| | | LCDCPEN = 1, VLCDx = 1100 | 2 V to 3.6 V | | 3.27 | | |
| | | LCDCPEN = 1, VLCDx = 1101 | 2.2 V to 3.6 V | | 3.32 | | |
| | | LCDCPEN = 1, VLCDx = 1110 | 2.2 V to 3.6 V | | 3.38 | | |
| | | LCDCPEN = 1, VLCDx = 1111 | 2.2 V to 3.6 V | | 3.44 | 3.6 | |
| $I_{CC,Peak,CP}$ | Peak supply currents due to charge pump activities | LCDCPEN = 1, VLCDx = 1111 | 2.2 V | | 400 | | µA |
| $t_{LCD,CP,on}$ | Time to charge $C_{LCD}$ when discharged | $C_{LCD}$ = 4.7µF, LCDCPEN = 0→1, VLCDx = 1111 | 2.2 V | | 150 | 500 | ms |
| $I_{CP,Load}$ | Maximum charge pump load current | LCDCPEN = 1, VLCDx = 1111 | 2.2 V | 50 | | | µA |
| $R_{LCD,Seg}$ | LCD driver output impedance, segment lines | LCDCPEN = 1, VLCDx = 1000, $I_{LOAD}$ = ±10 µA | 2.2 V | | | 10 | kΩ |
| $R_{LCD,COM}$ | LCD driver output impedance, common lines | LCDCPEN = 1, VLCDx = 1000, $I_{LOAD}$ = ±10 µA | 2.2 V | | | 10 | kΩ |

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## 5.15 SD24_B

Table 5-35 lists the power supply and recommended operating conditions of the SD24_B.

**Table 5-35. SD24_B Power Supply and Recommended Operating Conditions**

| | | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $AV_{CC}$ | Analog supply voltage | $AV_{CC} = DV_{CC}$, $AV_{SS} = DV_{SS} = 0$ V | | 2.4 | | 3.6 | V |
| $f_{SD}$ | Modulator clock frequency (1) | | | 0.03 | | 2.3 | MHz |
| $V_I$ | Absolute input voltage range | | | $AV_{SS} - 1$ | | $AV_{CC}$ | V |
| $V_{IC}$ | Common-mode input voltage range | | | $AV_{SS} - 1$ | | $AV_{CC}$ | V |
| $V_{ID,FS}$ | Differential full-scale input voltage | $V_{ID} = V_{I,A+} - V_{I,A-}$ | | $-V_{REF}$/GAIN | | $+V_{REF}$/GAIN | mV |
| $V_{ID}$ | Differential input voltage for specified performance (2) | SD24REFS = 1 | SD24GAINx = 1 | ±910 | ±920 | | mV |
| | | | SD24GAINx = 2 | ±455 | ±460 | | |
| | | | SD24GAINx = 4 | ±227 | ±230 | | |
| | | | SD24GAINx = 8 | ±113 | ±115 | | |
| | | | SD24GAINx = 16 | ±57 | ±58 | | |
| | | | SD24GAINx = 32 | ±28 | ±29 | | |
| | | | SD24GAINx = 64 | ±14 | ±14.5 | | |
| | | | SD24GAINx = 128 | ±7 | ±7.2 | | |
| $C_{REF}$ | VREF load capacitance (3) | SD24REFS = 1 | | | 100 | | nF |

(1) Modulator clock frequency: MIN = 32.768 kHz – 10% ≈ 30 kHz. MAX = 32.768 kHz × 64 + 10% ≈ 2.3 MHz
(2) The full-scale range (FSR) is defined by $V_{FS+} = +V_{REF}/GAIN$ and $V_{FS-} = -V_{REF}/GAIN$: $FSR = V_{FS+} - V_{FS-} = 2 \times V_{REF} / GAIN$. If $V_{REF}$ is sourced externally, the analog input range should not exceed 80% of $V_{FS+}$ or $V_{FS-}$; that is, $V_{ID} = 0.8\ V_{FS-}$ to $0.8\ V_{FS+}$. If $V_{REF}$ is sourced internally, the given $V_{ID}$ ranges apply.
(3) There is no capacitance required on VREF. However, a capacitance of 100 nF is recommended to reduce any reference voltage noise.

Table 5-36 lists the analog input characteristics of the SD24_B.

**Table 5-36. SD24_B Analog Input (1)**

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $C_I$ | Input capacitance | SD24GAINx = 1 | | | | 5 | | pF |
| | | SD24GAINx = 2 | | | | 5 | | |
| | | SD24GAINx = 4 | | | | 5 | | |
| | | SD24GAINx = 8 | | | | 5 | | |
| | | SD24GAINx = 16 | | | | 5 | | |
| | | SD24GAINx = 32, 64, 128 | | | | 5 | | |
| $Z_I$ | Input impedance (Pin A+ or A- to $AV_{SS}$) | $f_{SD24}$ = 1 MHz | SD24GAINx = 1 | 3 V | | 200 | | kΩ |
| | | | SD24GAINx = 8 | 3 V | | 200 | | |
| | | | SD24GAINx = 32 | 3 V | | 200 | | |
| $Z_{ID}$ | Differential input impedance (Pin A+ to pin A-) | $f_{SD24}$ = 1 MHz | SD24GAINx = 1 | 3 V | 300 | 400 | | kΩ |
| | | | SD24GAINx = 8 | 3 V | | 400 | | |
| | | | SD24GAINx = 32 | 3 V | 300 | 400 | | |

(1) All parameters pertain to each SD24_B converter.


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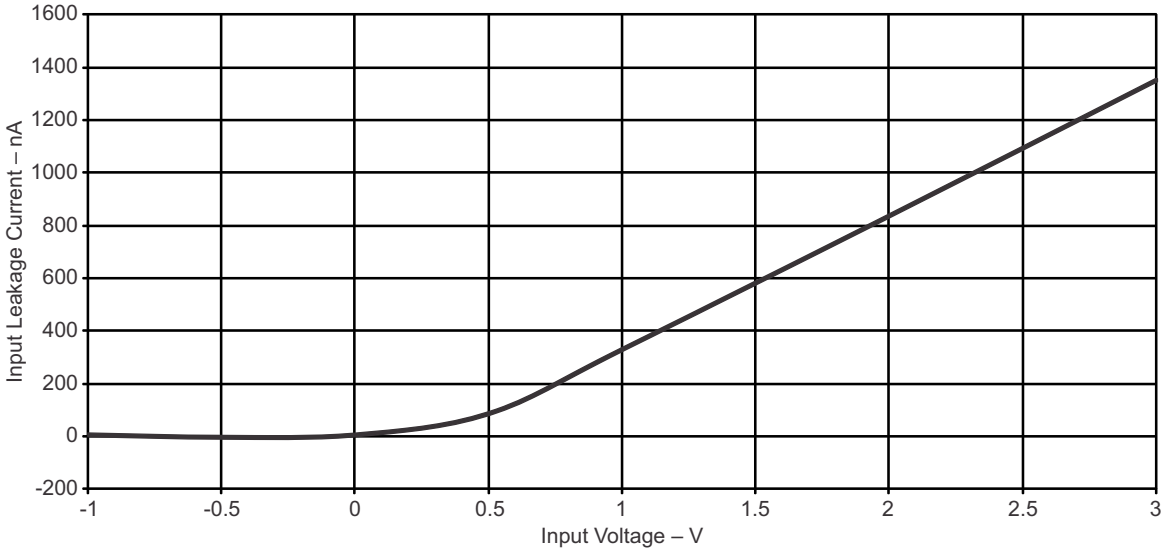


**Figure 5-18. Input Leakage Current vs Input Voltage (Modulator OFF)**

Table 5-37 lists the supply current of the SD24_B.

**Table 5-37. SD24_B Supply Currents**

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $I_{SD,256}$ | Analog plus digital supply current per converter (reference not included) | $f_{SD24}$ = 1 MHz, SD24OSR = 256 | SD24GAIN: 1 | 3 V | | 600 | 675 | µA |
| | | | SD24GAIN: 2 | 3 V | | 600 | 675 | |
| | | | SD24GAIN: 4 | 3 V | | 600 | 675 | |
| | | | SD24GAIN: 8 | 3 V | | 700 | 750 | |
| | | | SD24GAIN: 16 | 3 V | | 700 | 750 | |
| | | | SD24GAIN: 32 | 3 V | | 775 | 850 | |
| | | | SD24GAIN: 64 | 3 V | | 775 | 850 | |
| | | | SD24GAIN: 128 | 3 V | | 775 | 850 | |
| $I_{SD,512}$ | Analog plus digital supply current per converter (reference not included) | $f_{SD24}$ = 2 MHz, SD24OSR = 512 | SD24GAIN: 1 | 3 V | | 750 | 800 | µA |
| | | | SD24GAIN: 8 | 3 V | | 825 | 900 | |
| | | | SD24GAIN: 32 | 3 V | | 900 | 1000 | |

Table 5-38 lists the performance characteristics of the SD24_B.

**Table 5-38. SD24_B Performance**

$f_{SD24}$ = 1 MHz, SD24OSRx = 256, SD24REFS = 1

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| INL | Integral nonlinearity, end-point fit | SD24GAIN: 1 | 3 V | –0.01 | | 0.01 | % of FSR |
| | | SD24GAIN: 8 | 3 V | –0.01 | | 0.01 | |
| | | SD24GAIN: 32 | 3 V | –0.01 | | 0.01 | |
| $G_{nom}$ | Nominal gain | SD24GAIN: 1 | 3 V | | 1 | | |
| | | SD24GAIN: 2 | 3 V | | 2 | | |
| | | SD24GAIN: 4 | 3 V | | 4 | | |
| | | SD24GAIN: 8 | 3 V | | 8 | | |
| | | SD24GAIN: 16 | 3 V | | 16 | | |
| | | SD24GAIN: 32 | 3 V | | 31.7 | | |
| | | SD24GAIN: 64 | 3 V | | 63.4 | | |
| | | SD24GAIN: 128 | 3 V | | 126.8 | | |

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## Table 5-38. SD24_B Performance (continued)

$f_{SD24}$ = 1 MHz, SD24OSRx = 256, SD24REFS = 1

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $E_G$ | Gain error (1) | SD24GAIN: 1, with external reference (1.2 V) | 3 V | –1% | | +1% | |
| | | SD24GAIN: 8, with external reference (1.2 V) | 3 V | –2% | | +2% | |
| | | SD24GAIN: 32, with external reference (1.2 V) | 3 V | –2% | | +2% | |
| $\Delta E_G/\Delta T$ | Gain error temperature coefficient (2), internal reference | SD24GAIN: 1, 8, or 32 (with internal reference) | 3 V | | | 50 | ppm/°C |
| $\Delta E_G/\Delta V_{CC}$ | Gain error vs $V_{CC}$ (3) | SD24GAIN: 1 | | | 0.15 | | %/V |
| | | SD24GAIN: 8 | | | 0.15 | | |
| | | SD24GAIN: 32 | | | 0.4 | | |
| $E_{OS}$[V] | Offset error (4) | SD24GAIN: 1 (with $V_{diff}$ = 0 V) | 3 V | | | 2.3 | mV |
| | | SD24GAIN: 8 | 3 V | | | 0.73 | |
| | | SD24GAIN: 32 | 3 V | | | 0.18 | |
| $E_{OS}$[FS] | Offset error (4) | SD24GAIN: 1 (with $V_{diff}$ = 0 V) | 3 V | –0.2 | | 0.2 | % FS |
| | | SD24GAIN: 8 | 3 V | –0.5 | | 0.5 | |
| | | SD24GAIN: 32 | 3 V | –0.5 | | 0.5 | |
| $\Delta E_{OS}/\Delta T$ | Offset error temperature coefficient (5) | SD24GAIN: 1 | 3 V | | 1 | | µV/°C |
| | | SD24GAIN: 8 | 3 V | | 0.15 | | |
| | | SD24GAIN: 32 | 3 V | | 0.1 | | |
| $\Delta E_{OS}/\Delta V_{CC}$ | Offset error vs $V_{CC}$ (6) | SD24GAIN: 1 | | | 600 | | µV/V |
| | | SD24GAIN: 8 | | | 100 | | |
| | | SD24GAIN: 32 | | | 50 | | |
| CMRR,DC | Common-mode rejection at DC (7) | SD24GAIN: 1 | 3 V | | –110 | | dB |
| | | SD24GAIN: 8 | 3 V | | –110 | | |
| | | SD24GAIN: 32 | 3 V | | –110 | | |

(1) The gain error $E_G$ specifies the deviation of the actual gain $G_{act}$ from the nominal gain $G_{nom}$: $E_G = (G_{act} – G_{nom})/G_{nom}$. It covers process, temperature and supply voltage variations.

(2) The gain error temperature coefficient $\Delta E_G / \Delta T$ specifies the variation of the gain error $E_G$ over temperature ($E_G(T) = (G_{act}(T) – G_{nom})/G_{nom}$) using the box method (that is, MIN and MAX values):
$\Delta E_G/ \Delta T = (MAX(E_G(T)) – MIN(E_G(T)) / (MAX(T) – MIN(T)) = (MAX(G_{act}(T)) – MIN(G_{act}(T)) / G_{nom} / (MAX(T) – MIN(T))$
with T ranging from –40°C to +85°C.

(3) The gain error vs $V_{CC}$ coefficient $\Delta E_G/ \Delta V_{CC}$ specifies the variation of the gain error $E_G$ over supply voltage ($E_G(V_{CC}) = (G_{act}(V_{CC}) – G_{nom})/G_{nom}$) using the box method (that is, MIN and MAX values):
$\Delta E_G/ \Delta V_{CC} = (MAX(E_G(V_{CC})) – MIN(E_G(V_{CC})) / (MAX(V_{CC}) – MIN(V_{CC})) = (MAX(G_{act}(V_{CC})) – MIN(G_{act}(V_{CC})) / G_{nom} / (MAX(V_{CC}) – MIN(V_{CC}))$
with $V_{CC}$ ranging from 2.4 V to 3.6 V.

(4) The offset error $E_{OS}$ is measured with shorted inputs in 2s-complement mode with +100% FS = $V_{REF}$ / G and –100% FS = $–V_{REF}$ / G. Conversion between $E_{OS}$ [FS] and $E_{OS}$ [V] is as follows: $E_{OS}$ [FS] = $E_{OS}$ [V]×G/$V_{REF}$; $E_{OS}$ [V] = $E_{OS}$ [FS]×$V_{REF}$/G.

(5) The offset error temperature coefficient $\Delta E_{OS} / \Delta T$ specifies the variation of the offset error $E_{OS}$ over temperature using the box method (that is, MIN and MAX values):
$\Delta E_{OS} / \Delta T = (MAX(E_{OS}(T)) – MIN(E_{OS}(T)) / (MAX(T) – MIN(T))$
with T ranging from –40°C to +85°C.

(6) The offset error vs $V_{CC}$ $\Delta E_{OS} / \Delta V_{CC}$ specifies the variation of the offset error $E_{OS}$ over supply voltage using the box method (that is, MIN and MAX values):
$\Delta E_{OS} / \Delta V_{CC} = (MAX(E_{OS}(V_{CC})) – MIN(E_{OS}(V_{CC})) / (MAX(V_{CC}) – MIN(V_{CC}))$
with $V_{CC}$ ranging from 2.4 V to 3.6 V.

(7) The DC CMRR specifies the change in the measured differential input voltage value when the common-mode voltage varies:
DC CMRR = $–20\log(\Delta_{MAX}/FSR)$ with $\Delta_{MAX}$ being the difference between the minium value and the maximum value measured when sweeping the common-mode voltage (for example, calculating with 16-bit FSR = 65536, a maximum change by 1 LSB results in $–20\log(1/65536) \approx –96$ dB) .
The DC CMRR is measured with both inputs connected to the common-mode voltage (that is, no differential input signal is applied), and the common-mode voltage is swept from –1 V to $V_{CC}$.


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**Table 5-38. SD24_B Performance (continued)**

$f_{SD24}$ = 1 MHz, SD24OSRx = 256, SD24REFS = 1

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| CMRR,50Hz | Common-mode rejection at 50 Hz (8) | SD24GAIN: 1, $f_{CM}$ = 50 Hz, $V_{CM}$ = 930 mV | 3 V | | –110 | | dB |
| | | SD24GAIN: 8, $f_{CM}$ = 50 Hz, $V_{CM}$ = 120 mV | 3 V | | –110 | | |
| | | SD24GAIN: 32, $f_{CM}$ = 50 Hz, $V_{CM}$ = 30 mV | 3 V | | –110 | | |
| AC PSRR,ext | AC power supply rejection ratio, external reference (9) | SD24GAIN: 1, $V_{CC}$ = 3 V + 50 mV × sin(2π × $f_{Vcc}$ × t), $f_{Vcc}$ = 50 Hz | | | –61 | | dB |
| | | SD24GAIN: 8, $V_{CC}$ = 3 V + 50 mV × sin(2π × $f_{Vcc}$ × t), $f_{Vcc}$ = 50 Hz | | | –77 | | |
| | | SD24GAIN: 32, $V_{CC}$ = 3 V + 50 mV × sin(2π × $f_{Vcc}$ × t), $f_{Vcc}$ = 50 Hz | | | –79 | | |
| AC PSRR,int | AC power supply rejection ratio, internal reference (9) | SD24GAIN: 1, $V_{CC}$ = 3 V + 50 mV × sin(2π × $f_{Vcc}$ × t), $f_{Vcc}$ = 50 Hz | | | –61 | | dB |
| | | SD24GAIN: 8, $V_{CC}$ = 3 V + 50 mV × sin(2π × $f_{Vcc}$ × t), $f_{Vcc}$ = 50 Hz | | | –77 | | |
| | | SD24GAIN: 32, $V_{CC}$ = 3 V + 50 mV × sin(2π × $f_{Vcc}$ × t), $f_{Vcc}$ = 50 Hz | | | –79 | | |
| XT | Crosstalk between converters (10) | Crosstalk source: SD24GAIN: 1, Sine wave with maximum possible Vpp, $f_{IN}$ = 50 Hz or 100 Hz, Converter under test: SD24GAIN: 1 | 3 V | | –120 | | dB |
| | | Crosstalk source: SD24GAIN: 1, Sine wave with maximum possible Vpp, $f_{IN}$ = 50 Hz or 100 Hz, Converter under test: SD24GAIN: 8 | 3 V | | –115 | | |
| | | Crosstalk source: SD24GAIN: 1, Sine wave with maximum possible Vpp, $f_{IN}$ = 50 Hz or 100 Hz, Converter under test: SD24GAIN: 32 | 3 V | | –100 | | |

(8) The AC CMRR is the difference between a hypothetical signal with the amplitude and frequency of the applied common-mode ripple applied to the inputs of the ADC and the actual common-mode signal spur visible in the FFT spectrum:
AC CMRR = Error Spur [dBFS] – 20log($V_{CM}$ / 1.2 V / G) [dBFS] with a common-mode signal of $V_{CM}$ × sin(2π × $f_{CM}$ × t) applied to the analog inputs.
The AC CMRR is measured with the both inputs connected to the common-mode signal (that is, no differential input signal is applied).
With the specified typical values the error spur is within the noise floor (as specified by the SINAD values).

(9) The AC PSRR is the difference between a hypothetical signal with the amplitude and frequency of the applied supply voltage ripple applied to the inputs of the ADC and the actual supply ripple spur visible in the FFT spectrum:
AC PSRR = Error Spur [dBFS] – 20log(50 mV / 1.2 V / G) [dBFS] with a signal of 50 mV × sin(2π × $f_{Vcc}$ × t) added to $V_{CC}$.
The AC PSRR is measured with the inputs grounded (that is, no analog input signal is applied).
With the specified typical values the error spur is within the noise floor (as specified by the SINAD values).
SD24GAIN: 1 → Hypothetical signal: 20log(50 mV / 1.2 V / 1) = –27.6 dBFS
SD24GAIN: 8 → Hypothetical signal: 20log(50 mV / 1.2 V / 8) = –9.5 dBFS
SD24GAIN: 32 → Hypothetical signal: 20log(50 mV / 1.2 V / 32) = 2.5 dBFS

(10) The crosstalk (XT) is specified as the tone level of the signal applied to the crosstalk source seen in the spectrum of the converter under test. It is measured with the inputs of the converter under test being grounded.

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Table 5-39 lists the AC performance characteristics of the SD24_B.

**Table 5-39. SD24_B AC Performance**

$f_{SD24}$ = 1 MHz, SD24OSRx = 256, SD24REFS = 1

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| SINAD | Signal-to-noise + distortion ratio | SD24GAIN: 1 | $f_{IN}$ = 50 Hz (1) | 3 V | 85 | 87 | | dB |
| | | SD24GAIN: 2 | | 3 V | | 86 | | |
| | | SD24GAIN: 4 | | 3 V | | 85 | | |
| | | SD24GAIN: 8 | | 3 V | 82 | 84 | | |
| | | SD24GAIN: 16 | | 3 V | | 80 | | |
| | | SD24GAIN: 32 | | 3 V | 73 | 74 | | |
| | | SD24GAIN: 64 | | 3 V | | 68 | | |
| | | SD24GAIN: 128 | | 3 V | | 62 | | |
| THD | Total harmonic distortion | SD24GAIN: 1 | $f_{IN}$ = 50 Hz (1) | 3 V | | 100 | | dB |
| | | SD24GAIN: 8 | | 3 V | | 90 | | |
| | | SD24GAIN: 32 | | 3 V | | 80 | | |

(1) The following voltages were applied to the SD24_B inputs:
$V_{I,A+}(t) = 0\ V + V_{PP} / 2 \times \sin(2\pi \times f_{IN} \times t)$
$V_{I,A-}(t) = 0\ V - V_{PP} / 2 \times \sin(2\pi \times f_{IN} \times t)$
resulting in a differential voltage of $V_{ID} = V_{I,A+}(t) - V_{I,A-}(t) = V_{PP} \times \sin(2\pi \times f_{IN} \times t)$ with $V_{PP}$ being selected as the maximum value allowed for a given range (according to SD24_B recommended operating conditions).

Table 5-40 lists the AC performance characteristics of the SD24_B.

**Table 5-40. SD24_B AC Performance**

$f_{SD24}$ = 2 MHz, SD24OSRx = 512, SD24REFS = 1

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| SINAD | Signal-to-noise + distortion ratio | SD24GAIN: 1 | $f_{IN}$ = 50 Hz (1) | 3 V | | 87 | | dB |
| | | SD24GAIN: 2 | | 3 V | | 86 | | |
| | | SD24GAIN: 4 | | 3 V | | 85 | | |
| | | SD24GAIN: 8 | | 3 V | | 84 | | |
| | | SD24GAIN: 16 | | 3 V | | 81 | | |
| | | SD24GAIN: 32 | | 3 V | | 76 | | |
| | | SD24GAIN: 64 | | 3 V | | 71 | | |
| | | SD24GAIN: 128 | | 3 V | | 65 | | |

(1) The following voltages were applied to the SD24_B inputs:
$V_{I,A+}(t) = 0\ V + V_{PP} / 2 \times \sin(2\pi \times f_{IN} \times t)$
$V_{I,A-}(t) = 0\ V - V_{PP} / 2 \times \sin(2\pi \times f_{IN} \times t)$
resulting in a differential voltage of $V_{ID} = V_{I,A+}(t) - V_{I,A-}(t) = V_{PP} \times \sin(2\pi \times f_{IN} \times t)$ with $V_{PP}$ being selected as the maximum value allowed for a given range (according to SD24_B recommended operating conditions).


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Table 5-41 lists the AC performance characteristics of the SD24_B.

**Table 5-41. SD24_B AC Performance**

$f_{SD24}$ = 32 kHz, SD24OSRx = 512, SD24REFS = 1

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| SINAD | Signal-to-noise + distortion ratio | SD24GAIN: 1 | $f_{IN}$ = 12 Hz (1) | 3 V | | 89 | | dB |
| | | SD24GAIN: 2 | | 3 V | | 85 | | |
| | | SD24GAIN: 4 | | 3 V | | 84 | | |
| | | SD24GAIN: 8 | | 3 V | | 86 | | |
| | | SD24GAIN: 16 | | 3 V | | 80 | | |
| | | SD24GAIN: 32 | | 3 V | | 76 | | |
| | | SD24GAIN: 64 | | 3 V | | 67 | | |
| | | SD24GAIN: 128 | | 3 V | | 61 | | |

(1) The following voltages were applied to the SD24_B inputs:
$V_{I,A+}(t) = 0\ V + V_{PP} / 2 \times \sin(2\pi \times f_{IN} \times t)$
$V_{I,A-}(t) = 0\ V - V_{PP} / 2 \times \sin(2\pi \times f_{IN} \times t)$
resulting in a differential voltage of $V_{ID} = V_{I,A+}(t) - V_{I,A-}(t) = V_{PP} \times \sin(2\pi \times f_{IN} \times t)$ with $V_{PP}$ being selected as the maximum value allowed for a given range (according to SD24_B recommended operating conditions).

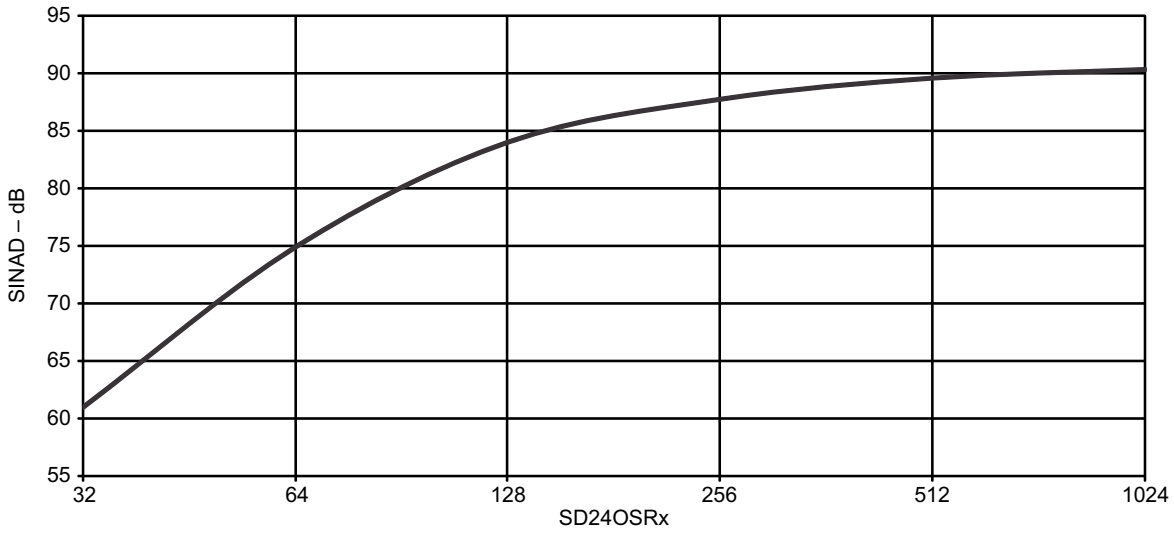


**Figure 5-19. SINAD vs OSR**
**($f_{SD24}$ = 1 MHz, SD24REFS = 1, SD24GAIN = 1)**

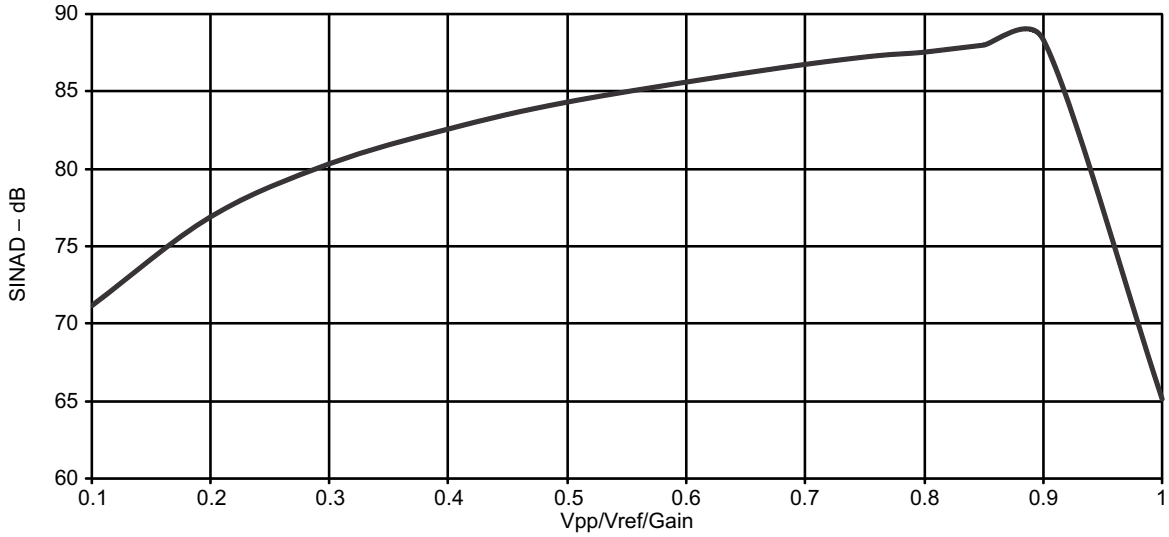


**Figure 5-20. SINAD vs $V_{PP}$**

Table 5-42 lists the external reference input requirements of the SD24_B.

**Table 5-42. SD24_B External Reference Input**

ensure correct input voltage range according to $V_{REF}$

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{REF(I)}$ | Input voltage | SD24REFS = 0 | 3 V | 1.0 | 1.20 | 1.5 | V |
| $I_{REF(I)}$ | Input current | SD24REFS = 0 | 3 V | | | 50 | nA |


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## 5.16 ADC10_A

Table 5-43 lists the power supply and input range conditions of the ADC10_A.

**Table 5-43. 10-Bit ADC, Power Supply and Input Range Conditions**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $AV_{CC}$ | Analog supply voltage | $AV_{CC}$ and $DV_{CC}$ are connected together, $AV_{SS}$ and $DV_{SS}$ are connected together, $V_{(AVSS)} = V_{(DVSS)} = 0$ V | | 1.8 | | 3.6 | V |
| $V_{(Ax)}$ | Analog input voltage range(1) | All ADC10_A pins | | 0 | | $AV_{CC}$ | V |
| $I_{ADC10_A}$ | Operating supply current into AVCC terminal, REF module and reference buffer off | $f_{ADC10CLK}$ = 5 MHz, ADC10ON =1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 00 | 2.2 V | | 70 | 105 | µA |
| | | | 3 V | | 80 | 115 | |
| | Operating supply current into AVCC terminal, REF module on, reference buffer on | $f_{ADC10CLK}$ = 5 MHz, ADC10ON = 1, REFON = 1, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 01 | 3 V | | 130 | 185 | |
| | Operating supply current into AVCC terminal, REF module off, reference buffer on | $f_{ADC10CLK}$ = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 10, VEREF = 2.5 V | 3 V | | 108 | 160 | |
| | Operating supply current into AVCC terminal, REF module off, reference buffer off | $f_{ADC10CLK}$ = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 11, VEREF = 2.5 V | 3 V | | 74 | 105 | |
| $C_I$ | Input capacitance | Only one terminal Ax can be selected at one time from the pad to the ADC10_A capacitor array including wiring and pad. | 2.2 V | | 3.5 | | pF |
| $R_I$ | Input MUX ON resistance | $AV_{CC}$ > 2 V, 0 V ≤ $V_{Ax}$ ≤ $AV_{CC}$ | | | | 36 | kΩ |
| | | 1.8 V < $AV_{CC}$ < 2 V, 0 V ≤ $V_{Ax}$ ≤ $AV_{CC}$ | | | | 96 | |

(1) The analog input voltage range must be within the selected reference voltage range $V_{R+}$ to $V_{R-}$ for valid conversion results. The external reference voltage requires decoupling capacitors. Two decoupling capacitors, 10 µF and 100 nF, should be connected to VREF to decouple the dynamic current required for an external reference source if it is used for the ADC10_A. Also see the *MSP430x5xx and MSP430x6xx Family User's Guide*.

Table 5-44 lists the timing parameters of the ADC10_A.

**Table 5-44. 10-Bit ADC, Timing Parameters**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{ADC10CLK}$ | | For specified performance of ADC10_A linearity parameters | 2.2 V, 3 V | 0.45 | 5 | 5.5 | MHz |
| $f_{ADC10OSC}$ | Internal ADC10_A oscillator(1) | ADC10DIV = 0, $f_{ADC10CLK}$ = $f_{ADC10OSC}$ | 2.2 V, 3 V | 4.4 | 5.0 | 5.6 | MHz |
| $t_{CONVERT}$ | Conversion time | REFON = 0, Internal oscillator, 12 ADC10CLK cycles, 10-bit mode $f_{ADC10OSC}$ = 4 MHz to 5 MHz | 2.2 V, 3 V | 2.4 | | 3.0 | µs |
| | | External $f_{ADC10CLK}$ from ACLK, MCLK or SMCLK, ADC10SSEL ≠ 0 | | | 12 × 1 / $f_{ADC10CLK}$ | | |
| $t_{ADC10ON}$ | Turnon settling time of the ADC | See (2) | | | | 100 | ns |
| $t_{Sample}$ | Sampling time | $R_S$ = 1000 Ω, $R_I$ = 96 kΩ, $C_I$ = 3.5 pF(3) | 1.8 V | 3 | | | µs |
| | | $R_S$ = 1000 Ω, $R_I$ = 36 kΩ, $C_I$ = 3.5 pF(3) | 3 V | 1 | | | |

(1) The ADC10OSC is sourced directly from MODOSC inside the UCS.
(2) The condition is that the error in a conversion started after $t_{ADC10ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.
(3) Approximately ei8ght Tau (t) are needed to get an error of less than ±0.5 LSB

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### Table 5-45. 10-Bit ADC, Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $E_I$ | Integral linearity error | 1.4 V ≤ ($V_{eREF+}$ – $V_{eREF–}$) ≤ 1.6 V, $C_{VeREF+}$ = 20 pF | 2.2 V, 3 V | | | ±1.0 | LSB |
| | | 1.6 V < ($V_{eREF+}$ – $V_{eREF–}$) ≤ $V_{AVCC}$, $C_{VeREF+}$ = 20 pF | | | | ±1.0 | |
| $E_D$ | Differential linearity error | 1.4 V ≤ ($V_{eREF+}$ – $V_{eREF–}$), $C_{VeREF+}$ = 20 pF | 2.2 V, 3 V | | | ±1.0 | LSB |
| $E_O$ | Offset error | 1.4 V ≤ ($V_{eREF+}$ – $V_{eREF–}$), $C_{VREF+}$ = 20 pF, Internal impedance of source $R_S$ < 100 Ω | 2.2 V, 3 V | | | ±1.0 | LSB |
| $E_G$ | Gain error | 1.4 V ≤ ($V_{eREF+}$ – $V_{eREF–}$), $C_{VeREF+}$ = 20 pF, ADC10SREFx = 11b | 2.2 V, 3 V | | | ±1.0 | LSB |
| $E_T$ | Total unadjusted error | 1.4 V ≤ ($V_{eREF+}$ – $V_{eREF–}$), $C_{VeREF+}$ = 20 pF, ADC10SREFx = 11b | 2.2 V, 3 V | | ±1.0 | ±2.0 | LSB |

Table 5-46 lists the external reference requirements of the ADC10_A.

### Table 5-46. 10-Bit ADC, External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{eREF+}$ | Positive external reference voltage input | $V_{eREF+}$ > $V_{eREF–}$ (2) | | 1.4 | | $AV_{CC}$ | V |
| $V_{eREF–}$ | Negative external reference voltage input | $V_{eREF+}$ > $V_{eREF–}$ (3) | | 0 | | 1.2 | V |
| ($V_{eREF+}$ – $V_{eREF–}$) | Differential external reference voltage input | $V_{eREF+}$ > $V_{eREF–}$ (4) | | 1.4 | | $AV_{CC}$ | V |
| $I_{VeREF+}$, $I_{VeREF–}$ | Static input current | 1.4 V ≤ $V_{eREF+}$ ≤ $V_{AVCC}$ , $V_{eREF–}$ = 0 V, $f_{ADC10CLK}$ = 5 MHz, ADC10SHTx = 0x0001, Conversion rate 200 ksps | 2.2 V, 3 V | | ±8.5 | ±26 | µA |
| | | 1.4 V ≤ $V_{eREF+}$ ≤ $V_{AVCC}$ , $V_{eREF–}$ = 0 V, $f_{ADC10CLK}$ = 5 MHz, ADC10SHTX = 0x1000, Conversion rate 20 ksps | 2.2 V, 3 V | | | ±1 | µA |
| $C_{VeREF+/-}$ | Capacitance at VeREF+ or VeREF- terminal | See (5) | | 10 | | | µF |

(1) The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance, $C_I$, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.
(2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
(3) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
(4) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
(5) Two decoupling capacitors, 10 µF and 100 nF, should be connected to VeREF to decouple the dynamic current required for an external reference source if it is used for the ADC10_A. Also see the *MSP430x5xx and MSP430x6xx Family User's Guide*.


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## 5.17 REF

Table 5-47 lists the characteristics of the REF.

**Table 5-47. REF, Built-In Reference**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{REF+}$ | Positive built-in reference voltage | REFVSEL = {2} for 2.5 V, REFON = 1 | 3 V | 2.47 | 2.51 | 2.55 | V |
| | | REFVSEL = {1} for 2.0 V, REFON = 1 | 3 V | 1.95 | 1.99 | 2.03 | |
| | | REFVSEL = {0} for 1.5 V, REFON = 1 | 2.2 V, 3 V | 1.46 | 1.50 | 1.54 | |
| $AV_{CC(min)}$ | AVCC minimum voltage, Positive built-in reference active | REFVSEL = {0} for 1.5 V | | 1.8 | | | V |
| | | REFVSEL = {1} for 2.0 V | | 2.2 | | | |
| | | REFVSEL = {2} for 2.5 V | | 2.7 | | | |
| $I_{REF+}$ | Operating supply current into AVCC terminal (1) | $f_{ADC10CLK}$ = 5 MHz, REFON = 1, REFBURST = 0, REFVSEL = {2} for 2.5 V | 3 V | | 23 | 30 | µA |
| | | $f_{ADC10CLK}$ = 5 MHz, REFON = 1, REFBURST = 0, REFVSEL = {1} for 2.0 V | 3 V | | 21 | 27 | |
| | | $f_{ADC10CLK}$ = 5 MHz, REFON = 1, REFBURST = 0, REFVSEL = {0} for 1.5 V | 3 V | | 19 | 25 | |
| $TC_{REF+}$ | Temperature coefficient of built-in reference (2) | REFVSEL = {0, 1, 2}, REFON = 1 | | | 10 | 50 | ppm/°C |
| $I_{SENSOR}$ | Operating supply current into AVCC terminal | REFON = 1, ADC10ON = 1, INCH = 0Ah, $T_A$ = 30°C | 2.2 V | | 145 | 220 | µA |
| | | | 3 V | | 170 | 245 | |
| $V_{SENSOR}$ | See (3) | REFON = 1, ADC10ON = 1, INCH = 0Ah, $T_A$ = 30°C | 2.2 V | | 780 | | mV |
| | | | 3 V | | 780 | | |
| $V_{MID}$ | $AV_{CC}$ divider at channel 11 | ADC10ON = 1, INCH = 0Bh, $V_{MID}$ is ~0.5 × $V_{AVCC}$ | 2.2 V | 1.08 | 1.1 | 1.12 | V |
| | | | 3 V | 1.48 | 1.5 | 1.52 | |
| $t_{SENSOR(sample)}$ | Sample time required if channel 10 is selected (4) | REFON = 1, ADC10ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB | | 30 | | | µs |
| $t_{VMID(sample)}$ | Sample time required if channel 11 is selected (5) | ADC10ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB | | 1 | | | µs |
| PSRR_DC | Power supply rejection ratio (DC) | $AV_{CC}$ = $AV_{CC\ (min)}$ to $AV_{CC(max)}$, $T_A$ = 25°C, REFVSEL = {0, 1, 2}, REFON = 1 | | | 120 | 300 | µV/V |
| PSRR_AC | Power supply rejection ratio (AC) | $AV_{CC}$ = $AV_{CC\ (min)}$ to $AV_{CC(max)}$, $T_A$ = 25°C, f = 1 kHz, ΔVpp = 100 mV REFVSEL = {0, 1, 2}, REFON = 1 | | | 1 | | mV/V |
| $t_{SETTLE}$ | Settling time of reference voltage (6) | $AV_{CC}$ = $AV_{CC\ (min)}$ to $AV_{CC(max)}$, REFVSEL = {0, 1, 2}, REFON = 0→1 | | | 75 | | µs |
| $V_{SD24REF}$ | SD24_B internal reference voltage | SD24REFS = 1 | 3 V | 1.137 | 1.151 | 1.165 | V |
| $t_{ON}$ | SD24_B internal reference turnon time (7) | SD24REFS = 0→1, $C_{REF}$ = 100 nF | 3 V | | 200 | | µs |

(1) The internal reference current is supplied through the AVCC terminal. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.
(2) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C)/(85°C – (–40°C)).
(3) The temperature sensor offset can be significant. TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor.
(4) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
(5) The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.
(6) The condition is that the error in a conversion started after $t_{REFON}$ is ≤ 1 LSB.
(7) The condition is that SD24_B conversion started after $t_{ON}$ should guarantee specified SINAD values for the selected Gain, OSR and $f_{SD24}$.

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## 5.18 Flash Memory

Table 5-48 lists the characteristics of the flash memory.

**Table 5-48. Flash Memory**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | $T_J$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $DV_{CC(PGM/ERASE)}$ | Program and erase supply voltage | | 1.8 | | 3.6 | V |
| $I_{PGM}$ | Average supply current from DVCC during program | | | 3 | 5 | mA |
| $I_{ERASE}$ | Average supply current from DVCC during erase | | | 6 | 11 | mA |
| $I_{MERASE}$, $I_{BANK}$ | Average supply current from DVCC during mass erase or bank erase | | | 6 | 11 | mA |
| $t_{CPT}$ | Cumulative program time(1) | | | | 16 | ms |
| | Program and erase endurance | | $10^4$ | $10^5$ | | cycles |
| $t_{Retention}$ | Data retention duration | 25°C | 100 | | | years |
| $t_{Word}$ | Word or byte program time(2) | | 64 | | 85 | µs |
| $t_{Block, 0}$ | Block program time for first byte or word(2) | | 49 | | 65 | µs |
| $t_{Block, 1–(N–1)}$ | Block program time for each additional byte or word, except for last byte or word(2) | | 37 | | 49 | µs |
| $t_{Block, N}$ | Block program time for last byte or word(2) | | 55 | | 73 | µs |
| $t_{Erase}$ | Erase time for segment erase, mass erase, and bank erase when available(2) | | 23 | | 32 | ms |
| $f_{MCLK,MGR}$ | MCLK frequency in marginal read mode (FCTL4.MGR0 = 1 or FCTL4. MGR1 = 1) | | 0 | | 1 | MHz |

(1) The cumulative program time must not be exceeded when writing to a 128-byte flash block. This parameter applies to all programming methods: individual word- or byte-write and block-write modes.
(2) These values are hardwired into the state machine of the flash controller.

## 5.19 Emulation and Debug

Table 5-49 lists the characteristics of the JTAG and Spy-Bi-Wire interface.

**Table 5-49. JTAG and Spy-Bi-Wire Interface**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{SBW}$ | Spy-Bi-Wire input frequency | 2.2 V, 3 V | 0 | | 20 | MHz |
| $t_{SBW,Low}$ | Spy-Bi-Wire low clock pulse duration | 2.2 V, 3 V | 0.025 | | 15 | µs |
| $t_{SBW, En}$ | Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge)(1) | 2.2 V, 3 V | | | 1 | µs |
| $t_{SBW,Rst}$ | Spy-Bi-Wire return to normal operation time | | 15 | | 100 | µs |
| $f_{TCK}$ | TCK input frequency for 4-wire JTAG(2) | 2.2 V | 0 | | 5 | MHz |
| | | 3 V | 0 | | 10 | |
| $R_{internal}$ | Internal pulldown resistance on TEST | 2.2 V, 3 V | 45 | 60 | 80 | kΩ |

(1) Tools that access the Spy-Bi-Wire interface must wait for the minimum $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.
(2) $f_{TCK}$ may be restricted to meet the timing requirements of the module selected.


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# 6 Detailed Description

## 6.1 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock. Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers (see Figure 6-1).

Peripherals are connected to the CPU using data, address, and control buses. Peripherals can be managed with all instructions.

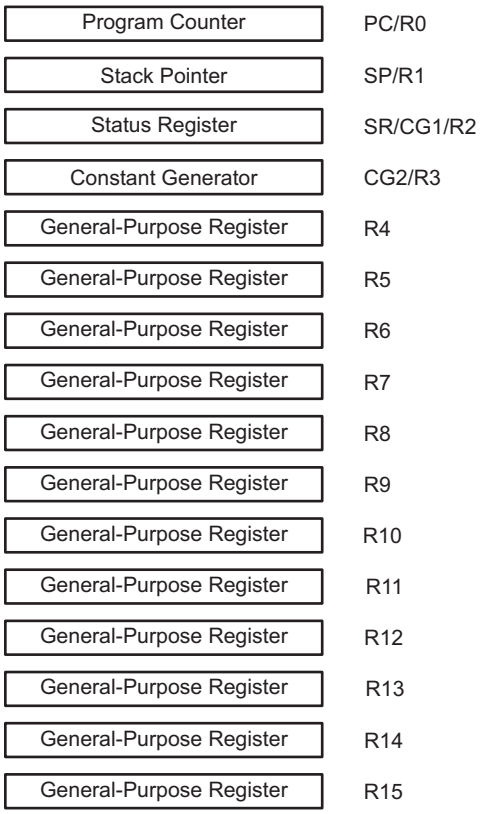


**Figure 6-1. Integrated CPU Registers**

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## 6.2 Instruction Set

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data. Table 6-1 lists examples of the three types of instruction formats. Table 6-2 lists the address modes.

**Table 6-1. Instruction Word Formats**

| INSTRUCTION WORD FORMAT | EXAMPLE | OPERATION |
|---|---|---|
| Dual operands, source and destination | ADD R4,R5 | R4 + R5 → R5 |
| Single operands, destination only | CALL R8 | PC → (TOS), R8 → PC |
| Relative jump, unconditional or conditional | JNE | Jump-on-equal bit = 0 |

**Table 6-2. Address Mode Descriptions**

| ADDRESS MODE | S(1) | D(1) | SYNTAX | EXAMPLE | OPERATION |
|---|---|---|---|---|---|
| Register | + | + | MOV Rs,Rd | MOV R10,R11 | R10 → R11 |
| Indexed | + | + | MOV X(Rn),Y(Rm) | MOV 2(R5),6(R6) | M(2+R5) → M(6+R6) |
| Symbolic (PC relative) | + | + | MOV EDE,TONI | | M(EDE) → M(TONI) |
| Absolute | + | + | MOV & MEM, & TCDAT | | M(MEM) → M(TCDAT) |
| Indirect | + | | MOV @Rn,Y(Rm) | MOV @R10,Tab(R6) | M(R10) → M(Tab+R6) |
| Indirect autoincrement | + | | MOV @Rn+,Rm | MOV @R10+,R11 | M(R10) → R11<br>R10 + 2 → R10 |
| Immediate | + | | MOV #X,TONI | MOV #45,TONI | #45 → M(TONI) |

(1) S = source, D = destination


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## 6.3 Operating Modes

These microcontrollers have one active mode and seven software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

Software can configure the following operating modes:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
  - FLL loop control remains active
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - FLL loop control is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK and FLL loop control and DCOCLK are disabled
  - DC generator of the DCO remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DC generator of the DCO is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DC generator of the DCO is disabled
  - Crystal oscillator is stopped
  - Complete data retention
- Low-power mode 3.5 (LPM3.5)
  - Internal regulator disabled
  - No RAM retention, Backup RAM retained
  - I/O pad state retention
  - RTC clocked by low-frequency oscillator
  - Wake-up input from $\overline{\text{RST}}$/NMI, RTC_C events, Ports P1 and P2
- Low-power mode 4.5 (LPM4.5)
  - Internal regulator disabled
  - No RAM retention, Backup RAM retained
  - RTC is disabled
  - I/O pad state retention
  - Wake-up input from $\overline{\text{RST}}$/NMI, Ports P1 and P2

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## 6.4 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are in the address range 0FFFFh to 0FF80h (see Table 6-3). The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

**Table 6-3. Interrupt Sources, Flags, and Vectors of MSP430F67xx Configurations**

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|---|---|---|---|---|
| **System Reset**<br>Power up<br>External reset<br>Watchdog time-out, key violation<br>Flash memory key violation | WDTIFG, KEYV (SYSRSTIV)(1)(2) | Reset | 0FFFEh | 63, highest |
| **System NMI**<br>PMM<br>Vacant memory access<br>JTAG mailbox | SVMLIFG, SVMHIFG, DLYLIFG, DLYHIFG, VLRLIFG, VLRHIFG, VMAIFG, JMBNIFG, JMBOUTIFG (SYSSNIV) (1)(3) | (Non)maskable | 0FFFCh | 62 |
| **User NMI**<br>NMI<br>Oscillator fault<br>Flash memory access violation<br>Supply switch | NMIIFG, OFIFG, ACCVIFG, AUXSWNMIFG (SYSUNIV)(1)(3) | (Non)maskable | 0FFFAh | 61 |
| Watchdog Timer_A interval timer mode | WDTIFG | Maskable | 0FFF8h | 60 |
| eUSCI_A0 receive or transmit | UCA0RXIFG, UCA0TXIFG (UCA0IV)(1)(4) | Maskable | 0FFF6h | 59 |
| eUSCI_B0 receive or transmit | UCB0RXIFG, UCB0TXIFG (UCB0IV)(1)(4) | Maskable | 0FFF4h | 58 |
| ADC10_A | ADC10IFG0, ADC10INIFG, ADC10LOIFG, ADC10HIIFG, ADC10TOVIFG, ADC10OVIFG (ADC10IV)(1)(4) | Maskable | 0FFF2h | 57 |
| SD24_B | SD24_B Interrupt Flags (SD24IV)(1)(4) | Maskable | 0FFF0h | 56 |
| Timer TA0 | TA0CCR0 CCIFG0(4) | Maskable | 0FFEEh | 55 |
| Timer TA0 | TA0CCR1 CCIFG1, TA0CCR2 CCIFG2, TA0IFG (TA0IV)(1)(4) | Maskable | 0FFECh | 54 |
| eUSCI_A1 receive or transmit | UCA1RXIFG, UCA1TXIFG (UCA1IV)(1)(4) | Maskable | 0FFEAh | 53 |
| eUSCI_A2 receive or transmit | UCA2RXIFG, UCA2TXIFG (UCA2IV)(1)(4) | Maskable | 0FFE8h | 52 |
| Auxiliary supplies | Auxiliary Supplies Interrupt Flags (AUXIV)(1)(4) | Maskable | 0FFE6h | 51 |
| DMA | DMA0IFG, DMA1IFG, DMA2IFG (DMAIV)(1)(4) | Maskable | 0FFE4h | 50 |
| Timer TA1 | TA1CCR0 CCIFG0(4) | Maskable | 0FFE2h | 49 |
| Timer TA1 | TA1CCR1 CCIFG1, TA1IFG (TA1IV)(1)(4) | Maskable | 0FFE0h | 48 |
| I/O port P1 | P1IFG.0 to P1IFG.7 (P1IV)(1)(4) | Maskable | 0FFDEh | 47 |
| Timer TA2 | TA2CCR0 CCIFG0(4) | Maskable | 0FFDCh | 46 |
| Timer TA2 | TA2CCR1 CCIFG1, TA2IFG (TA2IV)(1)(4) | Maskable | 0FFDAh | 45 |
| I/O port P2 | P2IFG.0 to P2IFG.7 (P2IV)(1)(4) | Maskable | 0FFD8h | 44 |
| Timer TA3 | TA3CCR0 CCIFG0(4) | Maskable | 0FFD6h | 43 |
| Timer TA3 | TA3CCR1 CCIFG1, TA3IFG (TA3IV)(1)(4) | Maskable | 0FFD4h | 42 |
| LCD_C | LCD_C Interrupt Flags (LCDCIV)(1)(4) | Maskable | 0FFD2h | 41 |
| RTC_C | RTCOFIFG, RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG (RTCIV)(1)(4) | Maskable | 0FFD0h | 40 |

(1) Multiple source flags
(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space.
(3) (Non)maskable: the individual interrupt enable bit can disable an interrupt event, but the general interrupt enable bit cannot disable it.
(4) Interrupt flags are in the module.


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**Table 6-3. Interrupt Sources, Flags, and Vectors of MSP430F67xx Configurations (continued)**

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|---|---|---|---|---|
| Reserved | Reserved(5) | | 0FFCEh | 39 |
| | | | ⋮ | ⋮ |
| | | | 0FF80h | 0, lowest |

(5) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, TI recommends reserving these locations.

## 6.5 Memory Organization

Table 6-4 and Table 6-5 summarize the memory map for the devices.

**Table 6-4. Memory Organization**

| | | MSP430F6730<br>MSP430F6720 | MSP430F6731<br>MSP430F6721 | MSP430F6733<br>MSP430F6723 |
|---|---|---|---|---|
| Main Memory (flash) | Total Size | 16KB | 32KB | 64KB |
| Main: Interrupt vector | | 00FFFFh to 00FF80h | 00FFFFh to 00FF80h | 00FFFFh to 00FF80h |
| Main: code memory | Bank 3 | not available | not available | not available |
| | Bank 2 | not available | not available | not available |
| | Bank 1 | not available | 16KB<br>00FFFFh to 00C000h | 32KB<br>013FFFh to 00C000h |
| | Bank 0 | 16KB<br>00FFFFh to 00C000h | 16KB<br>00BFFFh to 008000h | 32KB<br>00BFFFh to 004000h |
| RAM | Total Size | 1KB | 2KB | 4KB |
| | Sector 3 | not available | not available | not available |
| | Sector 2 | not available | not available | not available |
| | Sector 1 | not available | not available | 2KB<br>002BFFh to 002400h |
| | Sector 0 | 1KB<br>001FFFh to 001C00h | 2KB<br>0023FFh to 001C00h | 2KB<br>0023FFh to 001C00h |
| Information memory (flash) | Info A | 128 B<br>0019FFh to 001980h | 128 B<br>0019FFh to 001980h | 128 B<br>0019FFh to 001980h |
| | Info B | 128 B<br>00197Fh to 001900h | 128 B<br>00197Fh to 001900h | 128 B<br>00197Fh to 001900h |
| | Info C | 128 B<br>0018FFh to 001880h | 128 B<br>0018FFh to 001880h | 128 B<br>0018FFh to 001880h |
| | Info D | 128 B<br>00187Fh to 001800h | 128 B<br>00187Fh to 001800h | 128 B<br>00187Fh to 001800h |
| Bootloader (BSL) memory (flash) | BSL 3 | 512 B<br>0017FFh to 001600h | 512 B<br>0017FFh to 001600h | 512 B<br>0017FFh to 001600h |
| | BSL 2 | 512 B<br>0015FFh to 001400h | 512 B<br>0015FFh to 001400h | 512 B<br>0015FFh to 001400h |
| | BSL 1 | 512 B<br>0013FFh to 001200h | 512 B<br>0013FFh to 001200h | 512 B<br>0013FFh to 001200h |
| | BSL 0 | 512 B<br>0011FFh to 001000h | 512 B<br>0011FFh to 001000h | 512 B<br>0011FFh to 001000h |
| Peripherals | | 4KB<br>000FFFh to 0h | 4KB<br>000FFFh to 0h | 4KB<br>000FFFh to 0h |

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## Table 6-5. Memory Organization

| | | MSP430F6734<br>MSP430F6724 | MSP430F6735<br>MSP430F6725 | MSP430F6736<br>MSP430F6726 |
|---|---|---|---|---|
| Main Memory (flash) | Total Size | 96KB | 128KB | 128KB |
| Main: Interrupt vector | | 00FFFFh to 00FF80h | 00FFFFh to 00FF80h | 00FFFFh to 00FF80h |
| Main: code memory | Bank 3 | not available | 32KB<br>023FFFh to 01C000h | 32KB<br>023FFFh to 01C000h |
| | Bank 2 | 32KB<br>01BFFFh to 014000h | 32KB<br>01BFFFh to 014000h | 32KB<br>01BFFFh to 014000h |
| | Bank 1 | 32KB<br>013FFFh to 00C000h | 32KB<br>013FFFh to 00C000h | 32KB<br>013FFFh to 00C000h |
| | Bank 0 | 32KB<br>00BFFFh to 004000h | 32KB<br>00BFFFh to 004000h | 32KB<br>00BFFFh to 004000h |
| RAM | Total Size | 4KB | 4KB | 8KB |
| | Sector 3 | not available | not available | 2KB<br>003BFFh to 003400h |
| | Sector 2 | not available | not available | 2KB<br>0033FFh to 002C00h |
| | Sector 1 | 2KB<br>002BFFh to 002400h | 2KB<br>002BFFh to 002400h | 2KB<br>002BFFh to 002400h |
| | Sector 0 | 2KB<br>0023FFh to 001C00h | 2KB<br>0023FFh to 001C00h | 2KB<br>0023FFh to 001C00h |
| Information memory (flash) | Info A | 128 B<br>0019FFh to 001980h | 128 B<br>0019FFh to 001980h | 128 B<br>0019FFh to 001980h |
| | Info B | 128 B<br>00197Fh to 001900h | 128 B<br>00197Fh to 001900h | 128 B<br>00197Fh to 001900h |
| | Info C | 128 B<br>0018FFh to 001880h | 128 B<br>0018FFh to 001880h | 128 B<br>0018FFh to 001880h |
| | Info D | 128 B<br>00187Fh to 001800h | 128 B<br>00187Fh to 001800h | 128 B<br>00187Fh to 001800h |
| Bootloader (BSL) memory (flash) | BSL 3 | 512 B<br>0017FFh to 001600h | 512 B<br>0017FFh to 001600h | 512 B<br>0017FFh to 001600h |
| | BSL 2 | 512 B<br>0015FFh to 001400h | 512 B<br>0015FFh to 001400h | 512 B<br>0015FFh to 001400h |
| | BSL 1 | 512 B<br>0013FFh to 001200h | 512 B<br>0013FFh to 001200h | 512 B<br>0013FFh to 001200h |
| | BSL 0 | 512 B<br>0011FFh to 001000h | 512 B<br>0011FFh to 001000h | 512 B<br>0011FFh to 001000h |
| Peripherals | | 4KB<br>000FFFh to 0h | 4KB<br>000FFFh to 0h | 4KB<br>000FFFh to 0h |


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## 6.6 Bootloader (BSL)

The BSL enables users to program the flash memory or RAM using various serial interfaces. Access to the device memory through the BSL is protected by an user-defined password. BSL entry requires a specific entry sequence on the $\overline{\text{RST}}$/NMI/SBWTDIO and TEST/SBWTCK pins. For complete description of the features of the BSL and its implementation, see *MSP430™ Flash Device Bootloader (BSL) User's Guide*. Table 6-6 lists the BSL pin requirements.

**Table 6-6. UART BSL Pin Requirements and Functions**

| DEVICE SIGNAL | BSL FUNCTION |
|---|---|
| $\overline{\text{RST}}$/NMI/SBWTDIO | Entry sequence signal |
| TEST/SBWTCK | Entry sequence signal |
| P3.0 | Data transmit |
| P3.1 | Data receive |
| DVCC | Power supply |
| DVSS | Ground supply |

## 6.7 JTAG Operation

### 6.7.1 JTAG Standard Interface

The MSP430 family supports the standard JTAG interface, which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the $\overline{\text{RST}}$/NMI/SBWTDIO is required to interface with MSP430 development tools and device programmers. Table 6-7 lists the JTAG pin requirements. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide* and *MSP430 Programming With the JTAG Interface*.

**Table 6-7. JTAG Pin Requirements and Functions**

| DEVICE SIGNAL | DIRECTION | FUNCTION |
|---|---|---|
| PJ.3/ACLK/TCK | IN | JTAG clock input |
| PJ.2/ADC10CLK/TMS | IN | JTAG state control |
| PJ.1/MCLK/TDI/TCLK | IN | JTAG data input and TCLK input |
| PJ.0/SMCLK/TDO | OUT | JTAG data output |
| TEST/SBWTCK | IN | Enable JTAG pins |
| $\overline{\text{RST}}$/NMI/SBWTDIO | IN | External reset |
| DVCC | | Power supply |
| DVSS | | Ground supply |

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### 6.7.2 Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the MSP430 family supports the 2-wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. Table 6-8 lists the Spy-Bi-Wire interface pin requirements. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide* and *MSP430 Programming With the JTAG Interface*.

**Table 6-8. Spy-Bi-Wire Pin Requirements and Functions**

| DEVICE SIGNAL | DIRECTION | FUNCTION |
|---|---|---|
| TEST/SBWTCK | IN | Spy-Bi-Wire clock input |
| $\overline{\text{RST}}$/NMI/SBWTDIO | IN, OUT | Spy-Bi-Wire data input and output |
| DVCC | | Power supply |
| DVSS | | Ground supply |

## 6.8 Flash Memory

The flash memory can be programmed through the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. The CPU can perform single-byte, single-word, and long-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n. Segments A to D are also called *information memory*.
- Segment A can be locked separately.

## 6.9 RAM

The RAM is made up of n sectors. Each sector can be completely powered down to save leakage; however, all data are lost. Features of the RAM include:

- RAM has n sectors of 2KB each.
- Each sector 0 to n can be complete disabled; however, data retention is lost.
- Each sector 0 to n automatically enters low-power retention mode when possible.

## 6.10 Backup RAM

The backup RAM provides a limited number of bytes of RAM that are retained during LPMx.5. This backup RAM is part of the Backup subsystem in MSP430F67xx that operates on dedicated power supply AUXVCC3. There are 8 bytes of backup RAM available in this device. The backup RAM can be word-wise accessed through the registers BAKMEM0, BAKMEM1, BAKMEM2, and BAKMEM3. The backup RAM registers cannot be accessed by the CPU when the high-side SVS is disabled by the user.


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## 6.11 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. Peripherals can be managed using all instructions. For complete module descriptions, see the *MSP430x5xx and MSP430x6xx Family User's Guide*.

### 6.11.1 Oscillator and System Clock

The Unified Clock System (UCS) module includes support for a 32768-Hz watch crystal oscillator, an internal very-low-power low-frequency oscillator (VLO), an internal trimmed low-frequency oscillator (REFO), and an integrated internal digitally controlled oscillator (DCO). The UCS module is designed to meet the requirements of both low system cost and low power consumption. The UCS module features digital frequency-locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the selected FLL reference frequency. The internal DCO provides a fast turnon clock source and stabilizes in 3 µs (typical). The UCS module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal, the internal low-frequency oscillator (VLO), or the trimmed low-frequency oscillator (REFO).
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by same sources made available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources made available to ACLK.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, ACLK/8, ACLK/16, ACLK/32.

### 6.11.2 Power Management Module (PMM)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device and contains programmable output levels to provide for power optimization. The PMM also includes supply voltage supervisor (SVS) and supply voltage monitor (SVM) circuitry, as well as brownout protection. The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off. The SVS and SVM circuitry detects if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (the device is not automatically reset). SVS and SVM circuitry is available on the primary supply and core supply.

### 6.11.3 Auxiliary Supply System

The auxiliary supply system provides the possibility to operate the device from auxiliary supplies when the primary supply fails.There are two auxililary supplies AUXVCC1 and AUXVCC2 supported in MSP430F67xx. This module supports automatic and manual switching from primary supply to auxiliary suppllies while maintaining full functionality. It allows threshold based monitoring of primary and auxiliary supplies. The device can be started from primary supply or from AUXVCC1, whichever is higher. The auxiliary supply system enables internal monitoring of voltage levels on the primary and auxiliary supplies using ADC10_A. This module also implements a simple charger for the backup supplies.

### 6.11.4 Backup Subsystem

The backup subsystem operates on a dedicated power supply, AUXVCC3. This subsystem includes low-frequency oscillator (XT1), RTC module, and backup RAM. The functionality of backup subsystem is retained during LPM3.5. The backup subsystem module registers cannot be accessed by CPU when the high-side SVS is disabled by the user. Keep the high-side SVS enabled (SVSHMD = 1 and SVSMHACE = 0) to turn off the low-frequency oscillator (XT1) in LPM4.

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### 6.11.5 Digital I/O

Up to nine 8-bit I/O ports are implemented. For 100-pin options, Ports P1 to P8 are complete, and P9 is reduced to 4-bit I/O. For 80-pin options, Ports P1 to P6 are complete, and P7, P8, and P9 are completely removed. Port PJ contains four individual I/O pins, common to all devices. All I/O bits are individually programmable.

- Any combination of input, output, and interrupt conditions is possible.
- Pullup or pulldown on all ports is programmable.
- Programmable drive strength on all ports.
- Edge-selectable interrupt and LPM3.5 or LPM4.5 wake-up input are available for all bits of ports P1 and P2.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise (P1 through P9) or word-wise in pairs (PA through PE).

### 6.11.6 Port Mapping Controller

The port mapping controller allows flexible and reconfigurable mapping of digital functions to P1, P2, and P3 (see Table 6-9). Table 6-10 lists the default settings for all pins that support port mapping.

**Table 6-9. Port Mapping Mnemonics and Functions**

| VALUE | PxMAPy MNEMONIC | INPUT PIN FUNCTION | OUTPUT PIN FUNCTION |
|---|---|---|---|
| 0 | PM_NONE | None | DVSS |
| 1 | PM_UCA0RXD | eUSCI_A0 UART RXD (direction controlled by eUSCI – Input) | |
| | PM_UCA0SOMI | eUSCI_A0 SPI slave out master in (direction controlled by eUSCI) | |
| 2 | PM_UCA0TXD | eUSCI_A0 UART TXD (direction controlled by eUSCI – Output) | |
| | PM_UCA0SIMO | eUSCI_A0 SPI slave in master out (direction controlled by eUSCI) | |
| 3 | PM_UCA0CLK | eUSCI_A0 clock input/output (direction controlled by eUSCI) | |
| 4 | PM_UCA0STE | eUSCI_A0 SPI slave transmit enable (direction controlled by eUSCI) | |
| 5 | PM_UCA1RXD | eUSCI_A1 UART RXD (direction controlled by eUSCI – Input) | |
| | PM_UCA1SOMI | eUSCI_A1 SPI slave out master in (direction controlled by eUSCI) | |
| 6 | PM_UCA1TXD | eUSCI_A1 UART TXD (direction controlled by eUSCI – Output) | |
| | PM_UCA1SIMO | eUSCI_A1 SPI slave in master out (direction controlled by eUSCI) | |
| 7 | PM_UCA1CLK | eUSCI_A1 clock input/output (direction controlled by eUSCI) | |
| 8 | PM_UCA1STE | eUSCI_A1 SPI slave transmit enable (direction controlled by eUSCI) | |
| 9 | PM_UCA2RXD | eUSCI_A2 UART RXD (direction controlled by eUSCI – Input) | |
| | PM_UCA2SOMI | eUSCI_A2 SPI slave out master in (direction controlled by eUSCI) | |
| 10 | PM_UCA2TXD | eUSCI_A2 UART TXD (direction controlled by eUSCI – Output) | |
| | PM_ UCA2SIMO | eUSCI_A2 SPI slave in master out (direction controlled by eUSCI) | |
| 11 | PM_UCA2CLK | eUSCI_A2 clock input/output (direction controlled by eUSCI) | |
| 12 | PM_UCA2STE | eUSCI_A2 SPI slave transmit enable (direction controlled by eUSCI) | |
| 13 | PM_UCB0SIMO | eUSCI_B0 SPI slave in master out (direction controlled by eUSCI) | |
| | PM_UCB0SDA | eUSCI_B0 I2C data (open drain and direction controlled by eUSCI) | |
| 14 | PM_UCB0SOMI | eUSCI_B0 SPI slave out master in (direction controlled by eUSCI) | |
| | PM_UCB0SCL | eUSCI_B0 I2C clock (open drain and direction controlled by eUSCI) | |
| 15 | PM_UCB0CLK | eUSCI_B0 clock input/output (direction controlled by eUSCI) | |
| 16 | PM_UCB0STE | eUSCI_B0 SPI slave transmit enable (direction controlled by eUSCI) | |
| 17 | PM_TA0.0 | TA0 CCR0 capture input CCI0A | TA0 CCR0 compare output Out0 |
| 18 | PM_TA0.1 | TA0 CCR1 capture input CCI1A | TA0 CCR1 compare output Out1 |
| 19 | PM_TA0.2 | TA0 CCR2 capture input CCI2A | TA0 CCR2 compare output Out2 |
| 20 | PM_TA1.0 | TA1 CCR0 capture input CCI0A | TA1 CCR0 compare output Out0 |
| 21 | PM_TA1.1 | TA1 CCR1 capture input CCI1A | TA1 CCR1 compare output Out1 |


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**Table 6-9. Port Mapping Mnemonics and Functions (continued)**

| VALUE | PxMAPy MNEMONIC | INPUT PIN FUNCTION | OUTPUT PIN FUNCTION |
|---|---|---|---|
| 22 | PM_TA2.0 | TA2 CCR0 capture input CCI0A | TA2 CCR0 compare output Out0 |
| 23 | PM_TA2.1 | TA2 CCR1 capture input CCI1A | TA2 CCR1 compare output Out1 |
| 24 | PM_TA3.0 | TA3 CCR0 capture input CCI0A | TA3 CCR0 compare output Out0 |
| 25 | PM_TA3.1 | TA3 CCR1 capture input CCI1A | TA3 CCR1 compare output Out1 |
| 26 | PM_TACLK | Timer_A clock input to TA0, TA1, TA2, TA3 | None |
| | PM_RTCCLK | None | RTC_C clock output |
| 27 | PM_SDCLK | SD24_B bitstream clock input/output (direction controlled by SD24_B) | |
| 28 | PM_SD0DIO | SD24_B converter-0 bitstream data input/output (direction controlled by SD24_B) | |
| 29 | PM_SD1DIO | SD24_B converter-1 bitstream data input/output (direction controlled by SD24_B) | |
| 30 | PM_SD2DIO | SD24_B converter-2 bitstream data input/output (direction controlled by SD24_B) | |
| 31 (0FFh)(1) | PM_ANALOG | Disables the output driver and the input Schmitt-trigger to prevent parasitic cross currents when applying analog signals. | |

(1) The value of the PM_ANALOG mnemonic is set to 0FFh. The port mapping registers are only 5 bits wide, and the upper bits are ignored, which results in a read value of 31.

**Table 6-10. Default Mapping**

| PIN NAME | | PxMAPy MNEMONIC | INPUT PIN FUNCTION | OUTPUT PIN FUNCTION |
|---|---|---|---|---|
| PZ | PN | | | |
| P1.0/PM_TA0.0/ VeREF-/A2 | P1.0/PM_TA0.0/ VeREF-/A2 | PM_TA0.0 | TA0 CCR0 capture input CCI0A | TA0 CCR0 compare output Out0 |
| P1.1/PM_TA0.1/ VeREF+/A1 | P1.1/PM_TA0.1/ VeREF+/A1 | PM_TA0.1 | TA0 CCR1 capture input CCI1A | TA0 CCR1 compare output Out1 |
| P1.2/PM_UCA0RXD/ PM_UCA0SOMI/A0 | P1.2/PM_UCA0RXD/ PM_UCA0SOMI/A0 | PM_UCA0RXD, PM_UCA0SOMI | eUSCI_A0 UART RXD (direction controlled by eUSCI – input), eUSCI_A0 SPI slave out master in (direction controlled by eUSCI) | |
| P1.3/PM_UCA0TXD/ PM_UCA0SIMO/R03 | P1.3/PM_UCA0TXD/ PM_UCA0SIMO/R03 | PM_UCA0TXD, PM_UCA0SIMO | eUSCI_A0 UART TXD (direction controlled by eUSCI – output), eUSCI_A0 SPI slave in master out (direction controlled by eUSCI) | |
| P1.4/PM_UCA1RXD/ PM_UCA1SOMI/ LCDREF/R13 | P1.4/PM_UCA1RXD/ PM_UCA1SOMI/ LCDREF/R13 | PM_UCA1RXD, PM_UCA1SOMI | eUSCI_A1 UART RXD (direction controlled by eUSCI – input), eUSCI_A1 SPI slave out master in (direction controlled by eUSCI) | |
| P1.5/PM_UCA1TXD/ PM_UCA1SIMO/R23 | P1.5/PM_UCA1TXD/ PM_UCA1SIMO/R23 | PM_UCA1TXD, PM_UCA1SIMO | eUSCI_A1 UART TXD (direction controlled by eUSCI – output), eUSCI_A1 SPI slave in master out (direction controlled by eUSCI) | |
| P1.6/PM_UCA0CLK/ COM4 | P1.6/PM_UCA0CLK/ COM4 | PM_UCA0CLK | eUSCI_A0 clock input/output (direction controlled by eUSCI) | |
| P1.7/PM_UCB0CLK/ COM5 | P1.7/PM_UCB0CLK/ COM5 | PM_UCB0CLK | eUSCI_B0 clock input/output (direction controlled by eUSCI) | |
| P2.0/PM_UCB0SOMI/ PM_UCB0SCL/COM6 | P2.0/PM_UCB0SOMI/ PM_UCB0SCL/COM6/S39 | PM_UCB0SOMI, PM_UCB0SCL | eUSCI_B0 SPI slave out master in (direction controlled by eUSCI), eUSCI_B0 $I^2C$ clock (open drain and direction controlled by eUSCI) | |
| P2.1/PM_UCB0SIMO/ PM_UCB0SDA/COM7 | P2.1/PM_UCB0SIMO/ PM_UCB0SDA/COM7/S38 | PM_UCB0SIMO, PM_UCB0SDA | eUSCI_B0 SPI slave in master out (direction controlled by eUSCI), eUSCI_B0 $I^2C$ data (open drain and direction controlled by eUSCI) | |
| P2.2/PM_UCA2RXD/ PM_UCA2SOMI | P2.2/PM_UCA2RXD/ PM_UCA2SOMI/S37 | PM_UCA2RXD, PM_UCA2SOMI | eUSCI_A2 UART RXD (direction controlled by eUSCI – input), eUSCI_A2 SPI slave out master in (direction controlled by eUSCI) | |
| P2.3/PM_UCA2TXD/ PM_UCA2SIMO | P2.3/PM_UCA2TXD/ PM_UCA2SIMO/S36 | PM_UCA2TXD, PM_UCA2SIMO | eUSCI_A2 UART TXD (direction controlled by eUSCI – output), eUSCI_A2 SPI slave in master out (direction controlled by eUSCI) | |
| P2.4/PM_UCA1CLK | P2.4/PM_UCA1CLK/S35 | PM_UCA1CLK | eUSCI_A1 clock input/output (direction controlled by eUSCI) | |

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**Table 6-10. Default Mapping (continued)**

| PIN NAME | | PxMAPy MNEMONIC | INPUT PIN FUNCTION | OUTPUT PIN FUNCTION |
|---|---|---|---|---|
| PZ | PN | | | |
| P2.5/PM_UCA2CLK | P2.5/PM_UCA2CLK/S34 | PM_UCA2CLK | eUSCI_A2 clock input/output (direction controlled by eUSCI) | |
| P2.6/PM_TA1.0 | P2.6/PM_TA1.0/S33 | PM_TA1.0 | TA1 CCR0 capture input CCI0A | TA1 CCR0 compare output Out0 |
| P2.7/PM_TA1.1 | P2.7/PM_TA1.1/S32 | PM_TA1.1 | TA1 CCR1 capture input CCI1A | TA1 CCR1 compare output Out1 |
| P3.0/PM_TA2.0 | P3.0/PM_TA2.0/S31 | PM_TA2.0 | TA2 CCR0 capture input CCI0A | TA2 CCR0 compare output Out0 |
| P3.1/PM_TA2.1 | P3.1/PM_TA2.1/S30 | PM_TA2.1 | TA2 CCR1 capture input CCI1A | TA2 CCR1 compare output Out1 |
| P3.2/PM_TACLK/ PM_RTCCLK | P3.2/PM_TACLK/ PM_RTCCLK/S29 | PM_TACLK, PM_RTCCLK | Timer_A clock input to TA0, TA1, TA2, TA3 | RTC_C clock output |
| P3.3/PM_TA0.2 | P3.3/PM_TA0.2/S28 | PM_TA0.2 | TA0 CCR2 capture input CCI2A | TA0 CCR2 compare output Out2 |
| P3.4/PM_SDCLK/S39 | P3.4/PM_SDCLK/S27 | PM_SDCLK | SD24_B bitstream clock input/output (direction controlled by SD24_B) | |
| P3.5/PM_SD0DIO/S38 | P3.5/PM_SD0DIO/S26 | PM_SD0DIO | SD24_B converter-0 bitstream data input/output (direction controlled by SD24_B) | |
| P3.6/PM_SD1DIO/S37 | P3.6/PM_SD1DIO/S25 | PM_SD1DIO | SD24_B converter-1 bitstream data input/output (direction controlled by SD24_B) | |
| P3.7/PM_SD2DIO/S36 | P3.7/PM_SD2DIO/S24 | PM_SD2DIO | SD24_B converter-2 bitstream data input/output (direction controlled by SD24_B) | |

### 6.11.7 System Module (SYS)

The SYS module handles many of the system functions within the device. These include power-on reset (POR) and power-up clear (PUC) handling, NMI source selection and management, reset interrupt vector generators, bootloader entry mechanisms, as well as, configuration management (device descriptors). It also includes a data exchange mechanism through JTAG called a JTAG mailbox that can be used in the application. Table 6-11 lists the SYS module interrupt vector registers.

**Table 6-11. System Module Interrupt Vector Registers**

| INTERRUPT VECTOR REGISTER | INTERRUPT EVENT | WORD ADDRESS | OFFSET | PRIORITY |
|---|---|---|---|---|
| SYSRSTIV, System Reset | No interrupt pending | 019Eh | 00h | |
| | Brownout (BOR) | | 02h | Highest |
| | RST/NMI (POR) | | 04h | |
| | DoBOR (BOR) | | 06h | |
| | Wakeup from LPMx.5 (BOR) | | 08h | |
| | Security violation (BOR) | | 0Ah | |
| | SVSL (POR) | | 0Ch | |
| | SVSH (POR) | | 0Eh | |
| | SVML_OVP (POR) | | 10h | |
| | SVMH_OVP (POR) | | 12h | |
| | DoPOR (POR) | | 14h | |
| | WDT time-out (PUC) | | 16h | |
| | WDT key violation (PUC) | | 18h | |
| | KEYV flash key violation (PUC) | | 1Ah | |
| | Reserved | | 1Ch | |
| | Peripheral area fetch (PUC) | | 1Eh | |
| | PMM key violation (PUC) | | 20h | |
| | Reserved | | 22h to 3Eh | Lowest |


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**Table 6-11. System Module Interrupt Vector Registers (continued)**

| INTERRUPT VECTOR REGISTER | INTERRUPT EVENT | WORD ADDRESS | OFFSET | PRIORITY |
|---|---|---|---|---|
| SYSSNIV, System NMI | No interrupt pending | 019Ch | 00h | |
| | SVMLIFG | | 02h | Highest |
| | SVMHIFG | | 04h | |
| | DLYLIFG | | 06h | |
| | DLYHIFG | | 08h | |
| | VMAIFG | | 0Ah | |
| | JMBINIFG | | 0Ch | |
| | JMBOUTIFG | | 0Eh | |
| | VLRLIFG | | 10h | |
| | VLRHIFG | | 12h | |
| | Reserved | | 14h to 1Eh | Lowest |
| SYSUNIV, User NMI | No interrupt pending | 019Ah | 00h | |
| | NMIIFG | | 02h | Highest |
| | OFIFG | | 04h | |
| | ACCVIFG | | 06h | |
| | AUXSWNMIFG | | 08h | |
| | Reserved | | 0Ah to 1Eh | Lowest |

### 6.11.8 Watchdog Timer (WDT_A)

The primary function of the WDT_A module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the timer can be configured as an interval timer and can generate interrupts at selected time intervals.

### 6.11.9 DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC10_A conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral. Table 6-12 lists the triggers that are available to start DMA transfer.

**Table 6-12. DMA Trigger Assignments(1)**

| TRIGGER | CHANNEL | | |
|---|---|---|---|
| | 0 | 1 | 2 |
| 0 | DMAREQ | | |
| 1 | TA0CCR0 CCIFG | | |
| 2 | TA0CCR2 CCIFG | | |
| 3 | TA1CCR0 CCIFG | | |
| 4 | Reserved | | |
| 5 | TA2CCR0 CCIFG | | |
| 6 | Reserved | | |
| 7 | TA3CCR0 CCIFG | | |
| 8 | Reserved | | |

(1) Reserved DMA triggers may be used by other devices in the family. Reserved DMA triggers do not cause a DMA trigger event when selected.

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**Table 6-12. DMA Trigger Assignments[(1)] (continued)**

| TRIGGER | CHANNEL | | |
|---|---|---|---|
| | 0 | 1 | 2 |
| 9 | Reserved | | |
| 10 | Reserved | | |
| 11 | Reserved | | |
| 12 | Reserved | | |
| 13 | SD24IFG | | |
| 14 | Reserved | | |
| 15 | Reserved | | |
| 16 | UCA0RXIFG | | |
| 17 | UCA0TXIFG | | |
| 18 | UCA1RXIFG | | |
| 19 | UCA1TXIFG | | |
| 20 | UCA2RXIFG | | |
| 21 | UCA2TXIFG | | |
| 22 | UCB0RXIFG0 | | |
| 23 | UCB0TXIFG0 | | |
| 24 | ADC10IFG0 | | |
| 25 | Reserved | | |
| 26 | Reserved | | |
| 27 | Reserved | | |
| 28 | Reserved | | |
| 29 | MPY ready | | |
| 30 | DMA2IFG | DMA0IFG | DMA1IFG |
| 31 | Reserved | | |

### 6.11.10 CRC16

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

### 6.11.11 Hardware Multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-, 24-, 16-, and 8-bit operands. The module supports signed and unsigned multiplication as well as signed and unsigned multiply-and-accumulate operations.

### 6.11.12 Enhanced Universal Serial Communication Interface (eUSCI)

The eUSCI module is used for serial data communication. The eUSCI module supports synchronous communication protocols such as SPI (3- or 4-pin) and $I^2C$, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection, and IrDA.

The eUSCI_An module supports for SPI (3- or 4-pin), UART, enhanced UART, or IrDA.

The eUSCI_Bn module supports for SPI (3- or 4-pin) or $I^2C$.

Three eUSCI_A and one eUSCI_B modules are implemented in MSP430F67xx devices.


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### 6.11.13 ADC10_A

The ADC10_A module supports fast 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator, and a conversion results buffer. A window comparator with a lower and upper limits allows CPU-independent result monitoring with three window comparator interrupt flags.

### 6.11.14 SD24_B

The SD24_B module integrates up to three independent 24-bit sigma-delta analog-to-digital converters. Each converter is designed with a fully differential analog input pair and programmable gain amplifier input stage. The converters are based on second-order over-sampling sigma-delta modulators and digital decimation filters. The decimation filters are comb type filters with selectable oversampling ratios of up to 1024.

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### 6.11.15 TA0

TA0 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. TA0 can support multiple capture/compares, PWM outputs, and interval timing (see Table 6-13). TA0 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**Table 6-13. TA0 Signal Connections**

| DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|---|---|---|---|---|
| PM_TACLK | TACLK | Timer | NA | NA |
| ACLK (internal) | ACLK | | | |
| SMCLK (internal) | SMCLK | | | |
| PM_TACLK | INCLK | | | |
| PM_TA0.0 | CCI0A | CCR0 | TA0 | PM_TA0.0 |
| DVSS | CCI0B | | | |
| DVSS | GND | | | |
| DVCC | VCC | | | |
| PM_TA0.1 | CCI1A | CCR1 | TA1 | PM_TA0.1 |
| ACLK (internal) | CCI1B | | | ADC10_A (internal) ADC10SHSx = {1} |
| DVSS | GND | | | SD24_B (internal) SD24SCSx = {1} |
| DVCC | VCC | | | |
| PM_TA0.2 | CCI2A | CCR2 | TA2 | PM_TA0.2 |
| DVSS | CCI2B | | | |
| DVSS | GND | | | |
| DVCC | VCC | | | |

### 6.11.16 TA1

TA1 is a 16-bit timer/counter (Timer_A type) with two capture/compare registers. TA1 can support multiple capture/compares, PWM outputs, and interval timing (see Table 6-14). TA1 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**Table 6-14. TA1 Signal Connections**

| DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|---|---|---|---|---|
| | | | | PZ |
| PM_TACLK | TACLK | Timer | NA | NA |
| ACLK (internal) | ACLK | | | |
| SMCLK (internal) | SMCLK | | | |
| PM_TACLK | INCLK | | | |
| PM_TA1.0 | CCI0A | CCR0 | TA0 | PM_TA1.0 |
| DVSS | CCI0B | | | |
| DVSS | GND | | | |
| DVCC | VCC | | | |
| PM_TA1.1 | CCI1A | CCR1 | TA1 | PM_TA1.1 |
| ACLK (internal) | CCI1B | | | |
| DVSS | GND | | | |
| DVCC | VCC | | | |


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### 6.11.17 TA2

TA2 is a 16-bit timer/counter (Timer_A type) with two capture/compare registers. TA2 can support multiple capture/compares, PWM outputs, and interval timing (see Table 6-15). TA2 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**Table 6-15. TA2 Signal Connections**

| DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|---|---|---|---|---|
| PM_TACLK | TACLK | Timer | NA | NA |
| ACLK (internal) | ACLK | | | |
| SMCLK (internal) | SMCLK | | | |
| PM_TACLK | INCLK | | | |
| PM_TA2.0 | CCI0A | CCR0 | TA0 | PM_TA2.0 |
| DVSS | CCI0B | | | |
| DVSS | GND | | | |
| DVCC | VCC | | | |
| PM_TA2.1 | CCI1A | CCR1 | TA1 | PM_TA2.1 |
| ACLK (internal) | CCI1B | | | SD24_B (internal) SD24SCSx = {2} |
| DVSS | GND | | | |
| DVCC | VCC | | | |

### 6.11.18 TA3

TA3 is a 16-bit timer/counter (Timer_A type) with two capture/compare registers. TA3 can support multiple capture/compares, PWM outputs, and interval timing (see Table 6-16). TA3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

**Table 6-16. TA3 Signal Connections**

| DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|---|---|---|---|---|
| PM_TACLK | TACLK | Timer | NA | |
| ACLK (internal) | ACLK | | | |
| SMCLK (internal) | SMCLK | | | |
| PM_TACLK | INCLK | | | |
| PM_TA3.0 | CCI0A | CCR0 | TA0 | PM_TA3.0 |
| DVSS | CCI0B | | | ADC10_A (internal) ADC10SHSx = {2} |
| DVSS | GND | | | |
| DVCC | VCC | | | |
| PM_TA3.1 | CCI1A | CCR1 | TA1 | PM_TA3.1 |
| ACLK (internal) | CCI1B | | | SD24_B (internal) SD24SCSx = {3} |
| DVSS | GND | | | |
| DVCC | VCC | | | |

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### 6.11.19 SD24_B Triggers

Table 6-17 lists the input trigger connections to SD24_B converters from Timer_A modules and output trigger pulse connection from SD24_B to ADC10_A.

**Table 6-17. SD24_B Input/Output Trigger Connections**

| DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|---|---|---|---|---|
| TA0.1 (internal) | SD24_B<br>SD24SCSx = {1} | SD24_B | Trigger Pulse | ADC10_A (internal)<br>ADC10SHSx = {3} |
| TA2.1 (internal) | SD24_B<br>SD24SCSx = {2} | | | |
| TA3.1 (internal) | SD24_B<br>SD24SCSx = {3} | | | |

### 6.11.20 ADC10_A Triggers

Table 6-18 lists the input trigger connections to ADC10_A from Timer_A modules and SD24_B.

**Table 6-18. ADC10_A Input Trigger Connections**

| DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK |
|---|---|---|
| TA0.1 (internal) | ADC10_A<br>ADC10SHSx = {1} | ADC10_A |
| TA3.0 (internal) | ADC10_A<br>ADC10SHSx = {2} | |
| SD24_B<br>trigger pulse (internal) | ADC10_A<br>ADC10SHSx = {3} | |

### 6.11.21 Real-Time Clock (RTC_C)

The RTC_C module can be configured for calendar mode providing seconds, hours, day of week, day of month, month, and year. The RTC_C control and configuration registers are password protected to ensure clock integrity against runaway code. Calendar mode integrates an internal calendar that compensates for months with less than 31 days and includes leap year correction. The RTC_C also supports flexible alarm functions, offset calibration, and temperature compensation. The RTC_C on this device operates on dedicated AUXVCC3 supply and supports operation in LPM3.5.

### 6.11.22 Reference (REF) Module Voltage Reference

The REF module generates all critical reference voltages that can be used by the various analog peripherals in the device. These include the ADC10_A, LCD_C, and SD24_B modules.

### 6.11.23 LCD_C

The LCD_C driver generates the segment and common signals required to drive a liquid crystal display (LCD). The LCD_C controller has dedicated data memories to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-mux, 3-mux, 4-mux, up to 8-mux LCDs are supported. The module can provide a LCD voltage independent of the supply voltage with its integrated charge pump. It is possible to control the level of the LCD voltage, and thus contrast, by software. The module also provides an automatic blinking capability for individual segments in static, 2-mux, 3-mux, and 4-mux modes.


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### 6.11.24 Embedded Emulation Module (EEM) (S Version)

The EEM supports real-time in-system debugging. The S version of the EEM has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level

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### 6.11.25 Peripheral File Map

Table 6-19 lists the base address for the registers of each supported peripheral.

**Table 6-19. Peripherals**

| MODULE NAME | BASE ADDRESS | OFFSET ADDRESS RANGE |
|---|---|---|
| Special Functions (see Table 6-20) | 0100h | 000h to 01Fh |
| PMM (see Table 6-21) | 0120h | 000h to 01Fh |
| Flash Control (see Table 6-22) | 0140h | 000h to 00Fh |
| CRC16 (see Table 6-23) | 0150h | 000h to 007h |
| RAM Control (see Table 6-24) | 0158h | 000h to 001h |
| Watchdog (see Table 6-25) | 015Ch | 000h to 001h |
| UCS (see Table 6-26) | 0160h | 000h to 01Fh |
| SYS (see Table 6-27) | 0180h | 000h to 01Fh |
| Shared Reference (see Table 6-28) | 01B0h | 000h to 001h |
| Port Mapping Control (see Table 6-29) | 01C0h | 000h to 007h |
| Port Mapping Port P1 (see Table 6-30) | 01C8h | 000h to 007h |
| Port Mapping Port P2 (see Table 6-31) | 01D0h | 000h to 007h |
| Port Mapping Port P3 (see Table 6-32) | 01D8h | 000h to 007h |
| Port P1 and P2 (see Table 6-33) | 0200h | 000h to 01Fh |
| Port P3 and P4 (see Table 6-34) | 0220h | 000h to 00Bh |
| Port P5 and P6 (see Table 6-35) | 0240h | 000h to 00Bh |
| Port P7 and P8 (see Table 6-36) (Port P7 and P8 not available in MSP430F67xxIPN) | 0260h | 000h to 00Bh |
| Port P9 (Port P9 not available in MSP430F67xxIPN) (see Table 6-37) | 0280h | 000h to 00Bh |
| Port PJ (refer toTable 6-38) | 0320h | 000h to 01Fh |
| Timer TA0 (see Table 6-39) | 0340h | 000h to 03Fh |
| Timer TA1 (see Table 6-40) | 0380h | 000h to 03Fh |
| Timer TA2 (see Table 6-41) | 0400h | 000h to 03Fh |
| Timer TA3 (see Table 6-42) | 0440h | 000h to 03Fh |
| Backup Memory (see Table 6-43) | 0480h | 000h to 00Fh |
| RTC_C (see Table 6-44) | 04A0h | 000h to 01Fh |
| 32-Bit Hardware Multiplier (see Table 6-45) | 04C0h | 000h to 02Fh |
| DMA General Control (see Table 6-46) | 0500h | 000h to 00Fh |
| DMA Channel 0 (see Table 6-47) | 0500h | 010h to 01Fh |
| DMA Channel 1 (see Table 6-48) | 0500h | 020h to 02Fh |
| DMA Channel 2 (see Table 6-49) | 0500h | 030h to 03Fh |
| eUSCI_A0 (see Table 6-50) | 05C0h | 000h to 01Fh |
| eUSCI_A1 (see Table 6-51) | 05E0h | 000h to 01Fh |
| eUSCI_A2 (see Table 6-52) | 0600h | 000h to 01Fh |
| eUSCI_B0 (see Table 6-53) | 0640h | 000h to 02Fh |
| ADC10_A (see Table 6-54) | 0740h | 000h to 01Fh |
| SD24_B(see Table 6-55) | 0800h | 000h to 06Fh |
| Auxiliary Supply (see Table 6-49) | 09E0h | 000h to 01Fh |
| LCD_C (see Table 6-57) | 0A00h | 000h to 05Fh |


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**Table 6-20. Special Function Registers (Base Address: 0100h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| SFR interrupt enable | SFRIE1 | 00h |
| SFR interrupt flag | SFRIFG1 | 02h |
| SFR reset pin control | SFRRPCR | 04h |

**Table 6-21. PMM Registers (Base Address: 0120h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| PMM control 0 | PMMCTL0 | 00h |
| PMM control 1 | PMMCTL1 | 02h |
| SVS high-side control | SVSMHCTL | 04h |
| SVS low-side control | SVSMLCTL | 06h |
| PMM interrupt flags | PMMIFG | 0Ch |
| PMM interrupt enable | PMMIE | 0Eh |
| PMM power mode 5 control 0 | PM5CTL0 | 10h |

**Table 6-22. Flash Control Registers (Base Address: 0140h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Flash control 1 | FCTL1 | 00h |
| Flash control 3 | FCTL3 | 04h |
| Flash control 4 | FCTL4 | 06h |

**Table 6-23. CRC16 Registers (Base Address: 0150h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| CRC data input | CRC16DI | 00h |
| CRC data input reverse byte | CRC16DIRB | 02h |
| CRC result | CRCINIRES | 04h |
| CRC result reverse byte | CRCRESR | 06h |

**Table 6-24. RAM Control Registers (Base Address: 0158h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| RAM control 0 | RCCTL0 | 00h |

**Table 6-25. Watchdog Registers (Base Address: 015Ch)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Watchdog timer control | WDTCTL | 00h |

**Table 6-26. UCS Registers (Base Address: 0160h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| UCS control 0 | UCSCTL0 | 00h |
| UCS control 1 | UCSCTL1 | 02h |
| UCS control 2 | UCSCTL2 | 04h |
| UCS control 3 | UCSCTL3 | 06h |
| UCS control 4 | UCSCTL4 | 08h |
| UCS control 5 | UCSCTL5 | 0Ah |
| UCS control 6 | UCSCTL6 | 0Ch |
| UCS control 7 | UCSCTL7 | 0Eh |

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**Table 6-26. UCS Registers (Base Address: 0160h) (continued)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| UCS control 8 | UCSCTL8 | 10h |

**Table 6-27. SYS Registers (Base Address: 0180h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| System control | SYSCTL | 00h |
| Bootloader configuration area | SYSBSLC | 02h |
| JTAG mailbox control | SYSJMBC | 06h |
| JTAG mailbox input 0 | SYSJMBI0 | 08h |
| JTAG mailbox input 1 | SYSJMBI1 | 0Ah |
| JTAG mailbox output 0 | SYSJMBO0 | 0Ch |
| JTAG mailbox output 1 | SYSJMBO1 | 0Eh |
| Bus error vector generator | SYSBERRIV | 18h |
| User NMI vector generator | SYSUNIV | 1Ah |
| System NMI vector generator | SYSSNIV | 1Ch |
| Reset vector generator | SYSRSTIV | 1Eh |

**Table 6-28. Shared Reference Registers (Base Address: 01B0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Shared reference control | REFCTL | 00h |

**Table 6-29. Port Mapping Controller (Base Address: 01C0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port mapping password | PMAPPWD | 00h |
| Port mapping control | PMAPCTL | 02h |

**Table 6-30. Port Mapping for Port P1 (Base Address: 01C8h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P1.0 mapping | P1MAP0 | 00h |
| Port P1.1 mapping | P1MAP1 | 01h |
| Port P1.2 mapping | P1MAP2 | 02h |
| Port P1.3 mapping | P1MAP3 | 03h |
| Port P1.4 mapping | P1MAP4 | 04h |
| Port P1.5 mapping | P1MAP5 | 05h |
| Port P1.6 mapping | P1MAP6 | 06h |
| Port P1.7 mapping | P1MAP7 | 07h |

**Table 6-31. Port Mapping for Port P2 (Base Address: 01D0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P2.0 mapping | P2MAP0 | 00h |
| Port P2.1 mapping | P2MAP2 | 01h |
| Port P2.2 mapping | P2MAP2 | 02h |
| Port P2.3 mapping | P2MAP3 | 03h |
| Port P2.4 mapping | P2MAP4 | 04h |
| Port P2.5 mapping | P2MAP5 | 05h |
| Port P2.6 mapping | P2MAP6 | 06h |
| Port P2.7 mapping | P2MAP7 | 07h |


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**Table 6-32. Port Mapping for Port P3 (Base Address: 01D8h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P3.0 mapping | P3MAP0 | 00h |
| Port P3.1 mapping | P3MAP3 | 01h |
| Port P3.2 mapping | P3MAP2 | 02h |
| Port P3.3 mapping | P3MAP3 | 03h |
| Port P3.4 mapping | P3MAP4 | 04h |
| Port P3.5 mapping | P3MAP5 | 05h |
| Port P3.6 mapping | P3MAP6 | 06h |
| Port P3.7 mapping | P3MAP7 | 07h |

**Table 6-33. Port P1 and P2 Registers (Base Address: 0200h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P1 input | P1IN | 00h |
| Port P1 output | P1OUT | 02h |
| Port P1 direction | P1DIR | 04h |
| Port P1 resistor enable | P1REN | 06h |
| Port P1 drive strength | P1DS | 08h |
| Port P1 selection | P1SEL | 0Ah |
| Port P1 interrupt vector word | P1IV | 0Eh |
| Port P1 interrupt edge select | P1IES | 18h |
| Port P1 interrupt enable | P1IE | 1Ah |
| Port P1 interrupt flag | P1IFG | 1Ch |
| Port P2 input | P2IN | 01h |
| Port P2 output | P2OUT | 03h |
| Port P2 direction | P2DIR | 05h |
| Port P2 resistor enable | P2REN | 07h |
| Port P2 drive strength | P2DS | 09h |
| Port P2 selection | P2SEL | 0Bh |
| Port P2 interrupt vector word | P2IV | 1Eh |
| Port P2 interrupt edge select | P2IES | 19h |
| Port P2 interrupt enable | P2IE | 1Bh |
| Port P2 interrupt flag | P2IFG | 1Dh |

**Table 6-34. Port P3 and P4 Registers (Base Address: 0220h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P3 input | P3IN | 00h |
| Port P3 output | P3OUT | 02h |
| Port P3 direction | P3DIR | 04h |
| Port P3 resistor enable | P3REN | 06h |
| Port P3 drive strength | P3DS | 08h |
| Port P3 selection | P3SEL | 0Ah |
| Port P4 input | P4IN | 01h |
| Port P4 output | P4OUT | 03h |
| Port P4 direction | P4DIR | 05h |
| Port P4 resistor enable | P4REN | 07h |
| Port P4 drive strength | P4DS | 09h |
| Port P4 selection | P4SEL | 0Bh |

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**Table 6-35. Port P5 and P6 Registers (Base Address: 0240h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P5 input | P5IN | 00h |
| Port P5 output | P5OUT | 02h |
| Port P5 direction | P5DIR | 04h |
| Port P5 resistor enable | P5REN | 06h |
| Port P5 drive strength | P5DS | 08h |
| Port P5 selection | P5SEL | 0Ah |
| Port P6 input | P6IN | 01h |
| Port P6 output | P6OUT | 03h |
| Port P6 direction | P6DIR | 05h |
| Port P6 resistor enable | P6REN | 07h |
| Port P6 drive strength | P6DS | 09h |
| Port P6 selection | P6SEL | 0Bh |

**Table 6-36. Port P7 and P8 Registers (Base Address: 0260h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P7 input | P7IN | 00h |
| Port P7 output | P7OUT | 02h |
| Port P7 direction | P7DIR | 04h |
| Port P7 resistor enable | P7REN | 06h |
| Port P7 drive strength | P7DS | 08h |
| Port P7 selection | P7SEL | 0Ah |
| Port P8 input | P8IN | 01h |
| Port P8 output | P8OUT | 03h |
| Port P8 direction | P8DIR | 05h |
| Port P8 resistor enable | P8REN | 07h |
| Port P8 drive strength | P8DS | 09h |
| Port P8 selection | P8SEL | 0Bh |

**Table 6-37. Port P9 Registers (Base Address: 0280h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port P9 input | P9IN | 00h |
| Port P9 output | P9OUT | 02h |
| Port P9 direction | P9DIR | 04h |
| Port P9 resistor enable | P9REN | 06h |
| Port P9 drive strength | P9DS | 08h |
| Port P9 selection | P9SEL | 0Ah |

**Table 6-38. Port J Registers (Base Address: 0320h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Port PJ input | PJIN | 00h |
| Port PJ output | PJOUT | 02h |
| Port PJ direction | PJDIR | 04h |
| Port PJ resistor enable | PJREN | 06h |
| Port PJ drive strength | PJDS | 08h |
| Port PJ selection | PJSEL | 0Ah |


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**Table 6-39. TA0 Registers (Base Address: 0340h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| TA0 control | TA0CTL | 00h |
| Capture/compare control 0 | TA0CCTL0 | 02h |
| Capture/compare control 1 | TA0CCTL1 | 04h |
| Capture/compare control 2 | TA0CCTL2 | 06h |
| TA0 counter | TA0R | 10h |
| Capture/compare 0 | TA0CCR0 | 12h |
| Capture/compare 1 | TA0CCR1 | 14h |
| Capture/compare 2 | TA0CCR2 | 16h |
| TA0 expansion 0 | TA0EX0 | 20h |
| TA0 interrupt vector | TA0IV | 2Eh |

**Table 6-40. TA1 Registers (Base Address: 0380h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| TA1 control | TA1CTL | 00h |
| Capture/compare control 0 | TA1CCTL0 | 02h |
| Capture/compare control 1 | TA1CCTL1 | 04h |
| TA1 counter | TA1R | 10h |
| Capture/compare 0 | TA1CCR0 | 12h |
| Capture/compare 1 | TA1CCR1 | 14h |
| TA1 expansion 0 | TA1EX0 | 20h |
| TA1 interrupt vector | TA1IV | 2Eh |

**Table 6-41. TA2 Registers (Base Address: 0400h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| TA2 control | TA2CTL | 00h |
| Capture/compare control 0 | TA2CCTL0 | 02h |
| Capture/compare control 1 | TA2CCTL1 | 04h |
| TA2 counter | TA2R | 10h |
| Capture/compare 0 | TA2CCR0 | 12h |
| Capture/compare 1 | TA2CCR1 | 14h |
| TA2 expansion 0 | TA2EX0 | 20h |
| TA2 interrupt vector | TA2IV | 2Eh |

**Table 6-42. TA3 Registers (Base Address: 0440h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| TA3 control | TA3CTL | 00h |
| Capture/compare control 0 | TA3CCTL0 | 02h |
| Capture/compare control 1 | TA3CCTL1 | 04h |
| TA3 counter | TA3R | 10h |
| Capture/compare 0 | TA3CCR0 | 12h |
| Capture/compare 1 | TA3CCR1 | 14h |
| TA3 expansion 0 | TA3EX0 | 20h |
| TA3 interrupt vector | TA3IV | 2Eh |

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**Table 6-43. Backup Memory Registers (Base Address: 0480h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Backup memory 0 | BAKMEM0 | 00h |
| Backup memory 1 | BAKMEM1 | 02h |
| Backup memory 2 | BAKMEM2 | 04h |
| Backup memory 3 | BAKMEM3 | 06h |

**Table 6-44. RTC_C Registers (Base Address: 04A0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| RTC control 0 | RTCCTL0 | 00h |
| RTC password | RTCPWD | 01h |
| RTC control 1 | RTCCTL1 | 02h |
| RTC control 3 | RTCCTL3 | 03h |
| RTC offset calibration | RTCOCAL | 04h |
| RTC temperature compensation | RTCTCMP | 06h |
| RTC prescaler 0 control | RTCPS0CTL | 08h |
| RTC prescaler 1 control | RTCPS1CTL | 0Ah |
| RTC prescaler 0 | RTCPS0 | 0Ch |
| RTC prescaler 1 | RTCPS1 | 0Dh |
| RTC interrupt vector word | RTCIV | 0Eh |
| RTC seconds | RTCSEC | 10h |
| RTC minutes | RTCMIN | 11h |
| RTC hours | RTCHOUR | 12h |
| RTC day of week | RTCDOW | 13h |
| RTC days | RTCDAY | 14h |
| RTC month | RTCMON | 15h |
| RTC year | RTCYEAR | 16h |
| RTC alarm minutes | RTCAMIN | 18h |
| RTC alarm hours | RTCAHOUR | 19h |
| RTC alarm day of week | RTCADOW | 1Ah |
| RTC alarm days | RTCADAY | 1Bh |
| Binary-to-BCD conversion | BIN2BCD | 1Ch |
| BCD-to-binary conversion | BCD2BIN | 1Eh |


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**Table 6-45. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| 16-bit operand 1 – multiply | MPY | 00h |
| 16-bit operand 1 – signed multiply | MPYS | 02h |
| 16-bit operand 1 – multiply accumulate | MAC | 04h |
| 16-bit operand 1 – signed multiply accumulate | MACS | 06h |
| 16-bit operand 2 | OP2 | 08h |
| 16 × 16 result low word | RESLO | 0Ah |
| 16 × 16 result high word | RESHI | 0Ch |
| 16 × 16 sum extension | SUMEXT | 0Eh |
| 32-bit operand 1 – multiply low word | MPY32L | 10h |
| 32-bit operand 1 – multiply high word | MPY32H | 12h |
| 32-bit operand 1 – signed multiply low word | MPYS32L | 14h |
| 32-bit operand 1 – signed multiply high word | MPYS32H | 16h |
| 32-bit operand 1 – multiply accumulate low word | MAC32L | 18h |
| 32-bit operand 1 – multiply accumulate high word | MAC32H | 1Ah |
| 32-bit operand 1 – signed multiply accumulate low word | MACS32L | 1Ch |
| 32-bit operand 1 – signed multiply accumulate high word | MACS32H | 1Eh |
| 32-bit operand 2 – low word | OP2L | 20h |
| 32-bit operand 2 – high word | OP2H | 22h |
| 32 × 32 result 0 – least significant word | RES0 | 24h |
| 32 × 32 result 1 | RES1 | 26h |
| 32 × 32 result 2 | RES2 | 28h |
| 32 × 32 result 3 – most significant word | RES3 | 2Ah |
| MPY32 control 0 | MPY32CTL0 | 2Ch |

**Table 6-46. DMA General Control Registers (Base Address: 0500h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| DMA module control 0 | DMACTL0 | 00h |
| DMA module control 1 | DMACTL1 | 02h |
| DMA module control 2 | DMACTL2 | 04h |
| DMA module control 3 | DMACTL3 | 06h |
| DMA module control 4 | DMACTL4 | 08h |
| DMA interrupt vector | DMAIV | 0Eh |

**Table 6-47. DMA Channel 0 Registers (Base Address: 0500h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| DMA channel 0 control | DMA0CTL | 10h |
| DMA channel 0 source address low | DMA0SAL | 12h |
| DMA channel 0 source address high | DMA0SAH | 14h |
| DMA channel 0 destination address low | DMA0DAL | 16h |
| DMA channel 0 destination address high | DMA0DAH | 18h |
| DMA channel 0 transfer size | DMA0SZ | 1Ah |

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**Table 6-48. DMA Channel 1 Registers (Base Address: 0500h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| DMA channel 1 control | DMA1CTL | 20h |
| DMA channel 1 source address low | DMA1SAL | 22h |
| DMA channel 1 source address high | DMA1SAH | 24h |
| DMA channel 1 destination address low | DMA1DAL | 26h |
| DMA channel 1 destination address high | DMA1DAH | 28h |
| DMA channel 1 transfer size | DMA1SZ | 2Ah |

**Table 6-49. DMA Channel 2 Registers (Base Address: 0500h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| DMA channel 2 control | DMA2CTL | 30h |
| DMA channel 2 source address low | DMA2SAL | 32h |
| DMA channel 2 source address high | DMA2SAH | 34h |
| DMA channel 2 destination address low | DMA2DAL | 36h |
| DMA channel 2 destination address high | DMA2DAH | 38h |
| DMA channel 2 transfer size | DMA2SZ | 3Ah |

**Table 6-50. eUSCI_A0 Registers (Base Address: 05C0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| eUSCI_A control word 0 | UCA0CTLW0 | 00h |
| eUSCI _A control word 1 | UCA0CTLW1 | 02h |
| eUSCI_A baud rate 0 | UCA0BR0 | 06h |
| eUSCI_A baud rate 1 | UCA0BR1 | 07h |
| eUSCI_A modulation control | UCA0MCTLW | 08h |
| eUSCI_A status | UCA0STAT | 0Ah |
| eUSCI_A receive buffer | UCA0RXBUF | 0Ch |
| eUSCI_A transmit buffer | UCA0TXBUF | 0Eh |
| eUSCI_A LIN control | UCA0ABCTL | 10h |
| eUSCI_A IrDA transmit control | UCA0IRTCTL | 12h |
| eUSCI_A IrDA receive control | UCA0IRRCTL | 13h |
| eUSCI_A interrupt enable | UCA0IE | 1Ah |
| eUSCI_A interrupt flags | UCA0IFG | 1Ch |
| eUSCI_A interrupt vector word | UCA0IV | 1Eh |


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**Table 6-51. eUSCI_A1 Registers (Base Address:05E0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| eUSCI_A control word 0 | UCA1CTLW0 | 00h |
| eUSCI _A control word 1 | UCA1CTLW1 | 02h |
| eUSCI_A baud rate 0 | UCA1BR0 | 06h |
| eUSCI_A baud rate 1 | UCA1BR1 | 07h |
| eUSCI_A modulation control | UCA1MCTLW | 08h |
| eUSCI_A status | UCA1STAT | 0Ah |
| eUSCI_A receive buffer | UCA1RXBUF | 0Ch |
| eUSCI_A transmit buffer | UCA1TXBUF | 0Eh |
| eUSCI_A LIN control | UCA1ABCTL | 10h |
| eUSCI_A IrDA transmit control | UCA1IRTCTL | 12h |
| eUSCI_A IrDA receive control | UCA1IRRCTL | 13h |
| eUSCI_A interrupt enable | UCA1IE | 1Ah |
| eUSCI_A interrupt flags | UCA1IFG | 1Ch |
| eUSCI_A interrupt vector word | UCA1IV | 1Eh |

**Table 6-52. eUSCI_A2 Registers (Base Address:0600h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| eUSCI_A control word 0 | UCA2CTLW0 | 00h |
| eUSCI _A control word 1 | UCA2CTLW1 | 02h |
| eUSCI_A baud rate 0 | UCA2BR0 | 06h |
| eUSCI_A baud rate 1 | UCA2BR1 | 07h |
| eUSCI_A modulation control | UCA2MCTLW | 08h |
| eUSCI_A status | UCA2STAT | 0Ah |
| eUSCI_A receive buffer | UCA2RXBUF | 0Ch |
| eUSCI_A transmit buffer | UCA2TXBUF | 0Eh |
| eUSCI_A LIN control | UCA2ABCTL | 10h |
| eUSCI_A IrDA transmit control | UCA2IRTCTL | 12h |
| eUSCI_A IrDA receive control | UCA2IRRCTL | 13h |
| eUSCI_A interrupt enable | UCA2IE | 1Ah |
| eUSCI_A interrupt flags | UCA2IFG | 1Ch |
| eUSCI_A interrupt vector word | UCA2IV | 1Eh |

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**Table 6-53. eUSCI_B0 Registers (Base Address: 0640h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| eUSCI_B control word 0 | UCB0CTLW0 | 00h |
| eUSCI_B control word 1 | UCB0CTLW1 | 02h |
| eUSCI_B bit rate 0 | UCB0BR0 | 06h |
| eUSCI_B bit rate 1 | UCB0BR1 | 07h |
| eUSCI_B status word | UCB0STATW | 08h |
| eUSCI_B byte counter threshold | UCB0TBCNT | 0Ah |
| eUSCI_B receive buffer | UCB0RXBUF | 0Ch |
| eUSCI_B transmit buffer | UCB0TXBUF | 0Eh |
| eUSCI_B I2C own address 0 | UCB0I2COA0 | 14h |
| eUSCI_B I2C own address 1 | UCB0I2COA1 | 16h |
| eUSCI_B I2C own address 2 | UCB0I2COA2 | 18h |
| eUSCI_B I2C own address 3 | UCB0I2COA3 | 1Ah |
| eUSCI_B received address | UCB0ADDRX | 1Ch |
| eUSCI_B address mask | UCB0ADDMASK | 1Eh |
| eUSCI I2C slave address | UCB0I2CSA | 20h |
| eUSCI interrupt enable | UCB0IE | 2Ah |
| eUSCI interrupt flags | UCB0IFG | 2Ch |
| eUSCI interrupt vector word | UCB0IV | 2Eh |

**Table 6-54. ADC10_A Registers (Base Address: 0740h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| ADC10_A control 0 | ADC10CTL0 | 00h |
| ADC10_A control 1 | ADC10CTL1 | 02h |
| ADC10_A control 2 | ADC10CTL2 | 04h |
| ADC10_A window comparator low threshold | ADC10LO | 06h |
| ADC10_A window comparator high threshold | ADC10HI | 08h |
| ADC10_A memory control 0 | ADC10MCTL0 | 0Ah |
| ADC10_A conversion memory | ADC10MCTL0 | 12h |
| ADC10_A interrupt enable | ADC10IE | 1Ah |
| ADC10_A interrupt flags | ADC10IGH | 1Ch |
| ADC10_A interrupt vector word | ADC10IV | 1Eh |


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**Table 6-55. SD24_B Registers (Base Address: 0800h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| SD24_B control 0 | SD24BCTL0 | 00h |
| SD24_B control 1 | SD24BCTL1 | 02h |
| SD24_B interrupt flag | SD24BIFG | 0Ah |
| SD24_B interrupt enable | SD24BIE | 0Ch |
| SD24_B interrupt vector | SD24BIV | 0Eh |
| SD24_B converter 0 control | SD24BCCTL0 | 10h |
| SD24_B converter 0 input control | SD24BINCTL0 | 12h |
| SD24_B converter 0 OSR control | SD24BOSR0 | 14h |
| SD24_B converter 0 preload | SD24BPRE0 | 16h |
| SD24_B converter 1 control | SD24BCCTL1 | 18h |
| SD24_B converter 1 input control | SD24BINCTL1 | 1Ah |
| SD24_B converter 1 OSR control | SD24BOSR1 | 1Ch |
| SD24_B converter 1 preload | SD24BPRE1 | 1Eh |
| SD24_B converter 2 control | SD24BCCTL2 | 20h |
| SD24_B converter 2 input control | SD24BINCTL2 | 22h |
| SD24_B converter 2 OSR control | SD24BOSR2 | 24h |
| SD24_B converter 2 preload | SD24BPRE2 | 26h |
| SD24_B converter 0 conversion memory low word | SD24BMEML0 | 50h |
| SD24_B converter 0 conversion memory high word | SD24BMEMH0 | 52h |
| SD24_B converter 1 conversion memory low word | SD24BMEML1 | 54h |
| SD24_B converter 1 conversion memory high word | SD24BMEMH1 | 56h |
| SD24_B converter 2 conversion memory low word | SD24BMEML2 | 58h |
| SD24_B converter 2 conversion memory high word | SD24BMEMH2 | 5Ah |

**Table 6-56. Auxiliary Supplies Registers (Base Address: 09E0h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| Auxiliary supply control 0 | AUXCTL0 | 00h |
| Auxiliary supply control 1 | AUXCTL1 | 02h |
| Auxiliary supply control 2 | AUXCTL2 | 04h |
| AUX2 charger control | AUX2CHCTL | 12h |
| AUX3 charger control | AUX3CHCTL | 14h |
| AUX ADC control | AUXADCCTL | 16h |
| AUX interrupt flag | AUXIFG | 1Ah |
| AUX interrupt enable | AUXIE | 1Ch |
| AUX interrupt vector word | AUXIV | 1Eh |

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**Table 6-57. LCD_C Registers (Base Address: 0A00h)**

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|---|---|
| LCD_C control 0 | LCDCCTL0 | 000h |
| LCD_C control 1 | LCDCCTL1 | 002h |
| LCD_C blinking control | LCDCBLKCTL | 004h |
| LCD_C memory control | LCDCMEMCTL | 006h |
| LCD_C voltage control | LCDCVCTL | 008h |
| LCD_C port control 0 | LCDCPCTL0 | 00Ah |
| LCD_C port control 1 | LCDCPCTL1 | 00Ch |
| LCD_C port control 2 | LCDCPCTL2 | 00Eh |
| LCD_C charge pump control | LCDCCPCTL | 012h |
| LCD_C interrupt vector | LCDCIV | 01Eh |
| **Static and 2- to 4-mux modes** | | |
| LCD_C memory 1 | LCDM1 | 020h |
| LCD_C memory 2 | LCDM2 | 021h |
| ⋮ | ⋮ | ⋮ |
| LCD_C memory 20 | LCDM20 | 033h |
| LCD_C blinking memory 1 | LCDBM1 | 040h |
| LCD_C blinking memory 2 | LCDBM2 | 041h |
| ⋮ | ⋮ | ⋮ |
| LCD_C blinking memory 20 | LCDBM20 | 053h |
| **5- to 8-mux modes** | | |
| LCD_C memory 1 | LCDM1 | 020h |
| LCD_C memory 2 | LCDM2 | 021h |
| ⋮ | ⋮ | ⋮ |
| LCD_C memory 40 | LCDM40 | 047h |


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## 6.12 Input/Output Diagrams

### 6.12.1 Port P1 (P1.0 and P1.1) Input/Output With Schmitt Trigger (MSP430F67xxIPZ and MSP430F67xxIPN)

Figure 6-2 shows the port diagram. Table 6-58 summarizes the selection of the pin functions.

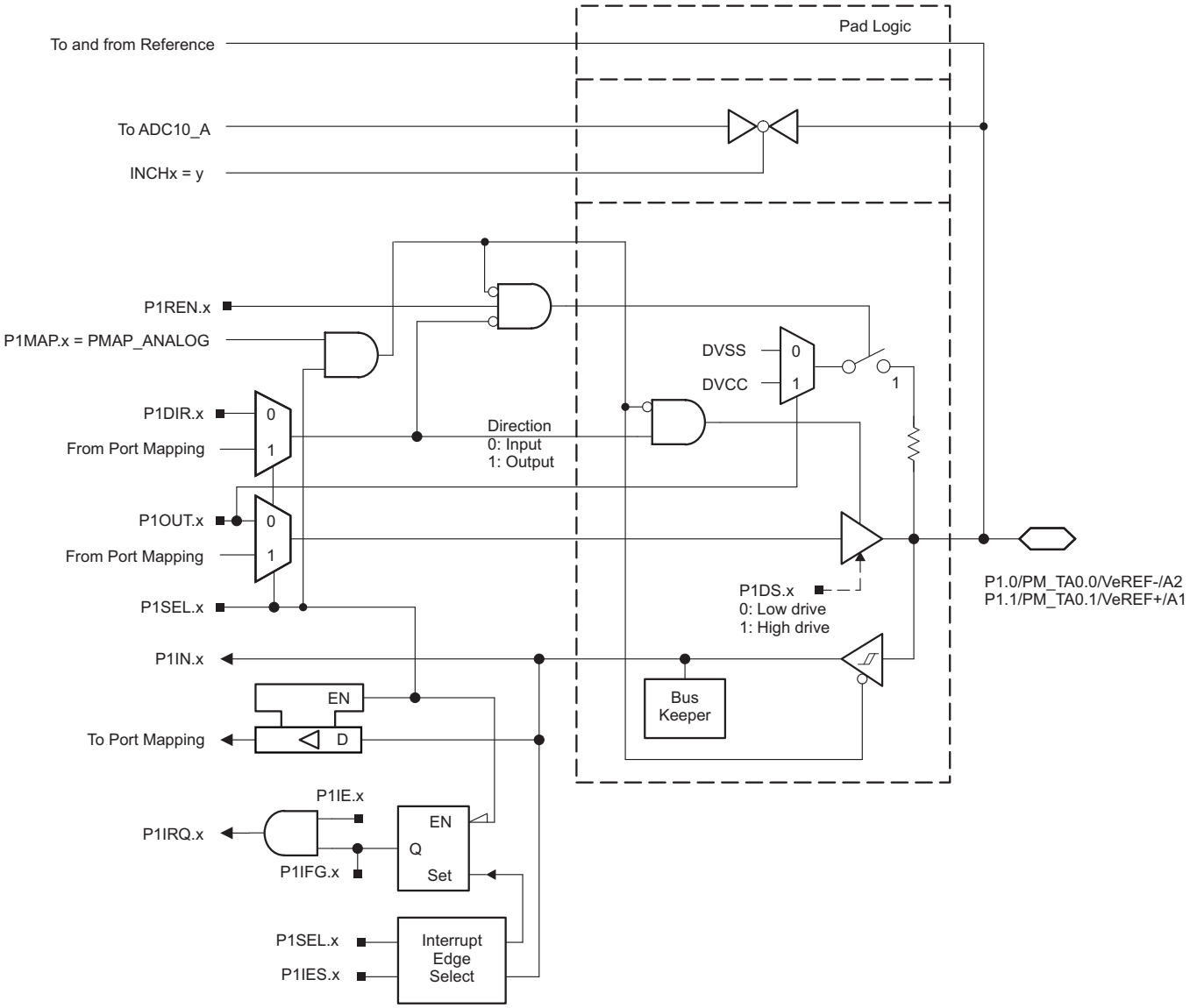


**Figure 6-2. Port P1 (P1.0 and P1.1) Diagram (MSP430F67xxIPZ and MSP430F67xxIPN)**

**Table 6-58. Port P1 (P1.0 and P1.1) Pin Functions (MSP430F67xxIPZ and MSP430F67xxIPN)**

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P1DIR.x | P1SEL.x | P1MAPx |
| P1.0/PM_TA0.0/ VeREF-/A2 | 0 | P1.0 (I/O) | I: 0; O: 1 | 0 | X |
| | | TA0.CCI0A | 0 | 1 | default |
| | | TA0.TA0 | 1 | 1 | default |
| | | VeREF-/A2(2) | X | 1 | = 31 |
| P1.1/PM_TA0.1/ VeREF+/A1 | 1 | P1.1 (I/O) | I: 0; O: 1 | 0 | X |
| | | TA0.CCI1A | 0 | 1 | default |
| | | TA0.TA1 | 1 | 1 | default |
| | | VeREF+/A1(2) | X | 1 | = 31 |

(1) X = Don't care
(2) Setting P1SEL.x bit together with P1MAPx = PM_ANALOG disables the output driver and the input Schmitt trigger.


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### 6.12.2 Port P1 (P1.2) Input/Output With Schmitt Trigger (MSP430F67xxIPZ and MSP430F67xxIPN)

Figure 6-3 shows the port diagram. Table 6-59 summarizes the selection of the pin functions.

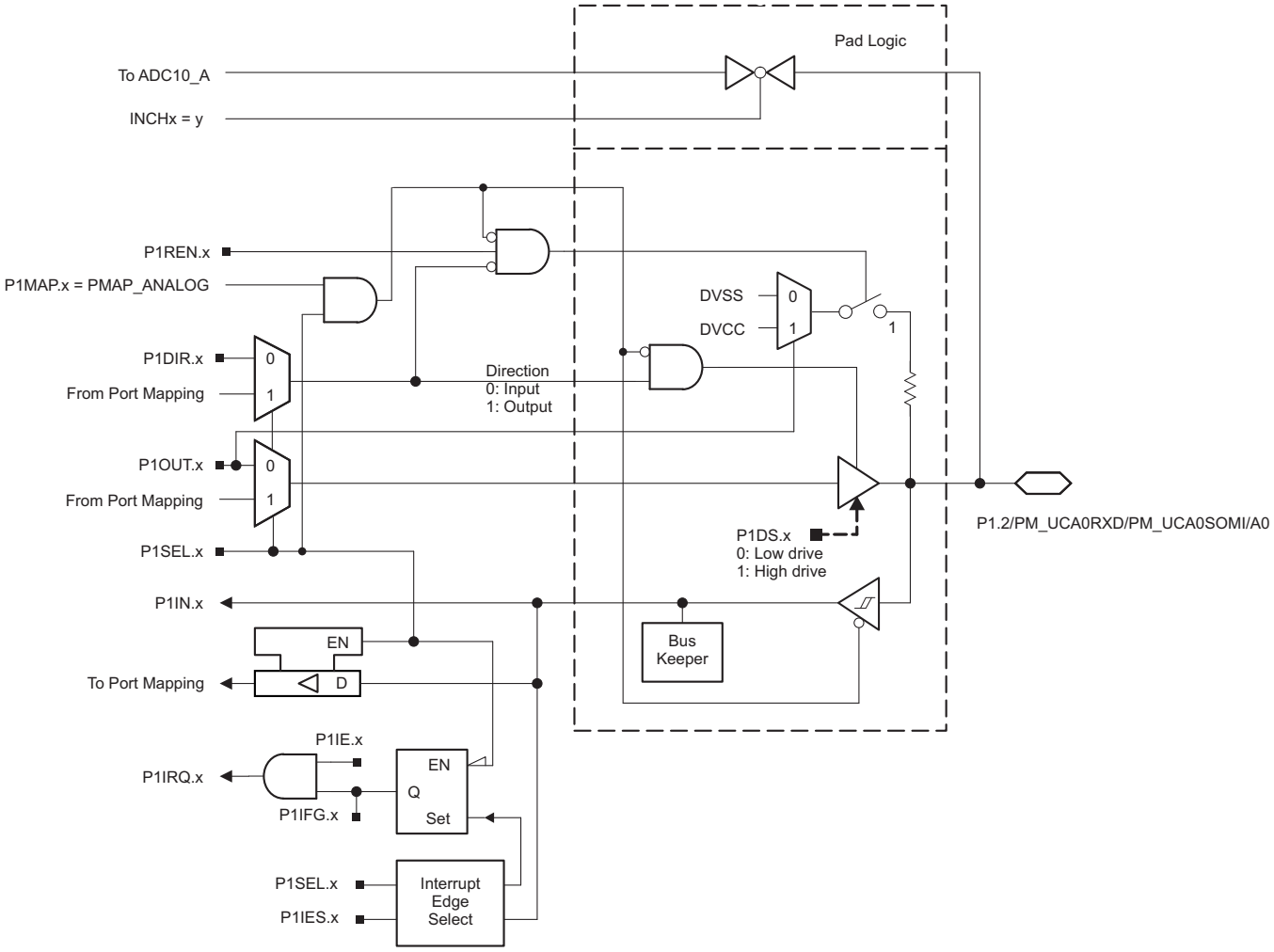


**Figure 6-3. Port P1 (P1.2) Pin Functions (MSP430F67xxIPZ and MSP430F67xxIPN)**

**Table 6-59. Port P1 (P1.2) Pin Functions (MSP430F67xxIPZ and MSP430F67xxIPN)**

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P1DIR.x | P1SEL.x | P1MAPx |
| P1.2/PM_UCA0RXD/ PM_UCA0SOMI/A0 | 2 | P1.2 (I/O) | I: 0; O: 1 | 0 | X |
| | | UCA0RXD/UCA0SOMI | X | 1 | default |
| | | A0(2) | X | 1 | = 31 |

(1) X = Don't care
(2) Setting P1SEL.x bit together with P1MAPx = PM_ANALOG disables the output driver and the input Schmitt trigger.

### 6.12.3 Port P1 (P1.3 to P1.5) Input/Output With Schmitt Trigger (MSP430F67xxIPZ and MSP430F67xxIPN)

Figure 6-4 shows the port diagram. Table 6-60 summarizes the selection of the pin functions.

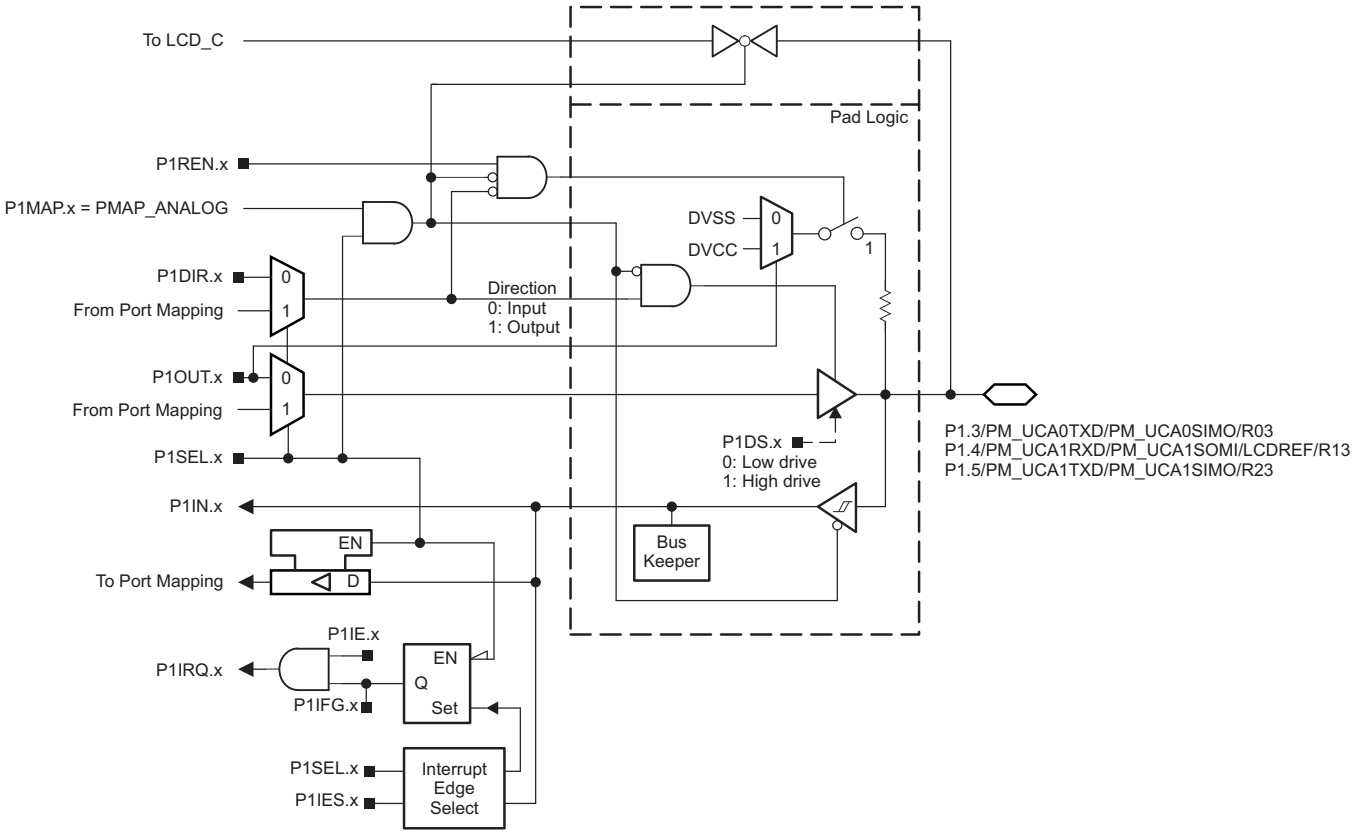


**Figure 6-4. Port P1 (P1.3 to P1.5) Diagram (MSP430F67xxIPZ and MSP430F67xxIPN)**

**Table 6-60. Port P1 (P1.3 to P1.5) Pin Functions (MSP430F67xxIPZ and MSP430F67xxIPN)**

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P1DIR.x | P1SEL.x | P1MAPx |
| P1.3/PM_UCA0TXD/ PM_UCA0SIMO/R03 | 3 | P1.3 (I/O) | I: 0; O: 1 | 0 | X |
| | | UCA0TXD/UCA0SIMO | X | 1 | default |
| | | R03(2) | X | 1 | = 31 |
| P1.4/PM_UCA1RXD/ PM_UCA1SOMI/ LCDREF/R13 | 4 | P1.4 (I/O) | I: 0; O: 1 | 0 | X |
| | | UCA1RXD/UCA1SOMI | X | 1 | default |
| | | LCDREF/R13(2) | X | 1 | = 31 |
| P1.5/PM_UCA1TXD/ PM_UCA1SIMO/R23 | 5 | P1.5 (I/O) | I: 0; O: 1 | 0 | X |
| | | UCA1TXD/UCA1SIMO | X | 1 | default |
| | | R23(2) | X | 1 | = 31 |

(1) X = Don't care
(2) Setting P1SEL.x bit together with P1MAPx = PM_ANALOG disables the output driver and the input Schmitt trigger.


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### 6.12.4 Port P1 (P1.6 and P1.7) (MSP430F67xxIPZ and MSP430F67xxIPN), Port P2 (P2.0 and P2.1) (MSP430F67xxIPZ Only) Input/Output With Schmitt Trigger

Figure 6-5 shows the port diagram. Table 6-61 and Table 6-62 summarize the selection of the pin functions.

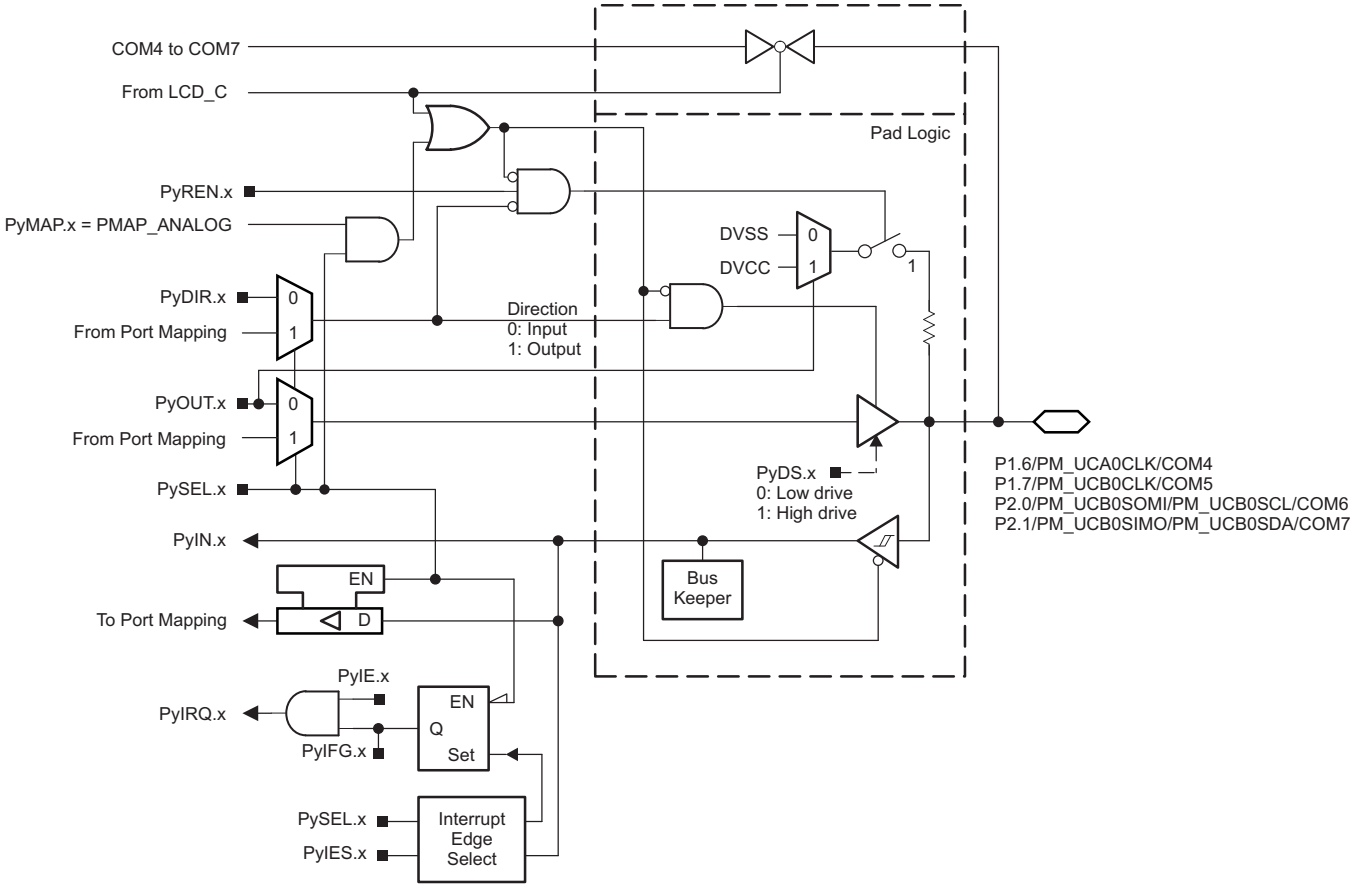


**Figure 6-5. Port P1 (P1.6 and P1.7) (MSP430F67xxIPZ and MSP430F67xxIPN), Port P2 (P2.0 and P2.1) (MSP430F67xxIPZ Only) Diagram**

### Table 6-61. Port P1 (P1.6 and P1.7) Pin Functions (MSP430F67xxIPZ and MSP430F67xxIPN)

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | | |
|---|---|---|---|---|---|---|
| | | | P1DIR.x | P1SEL.x | P1MAPx | COM4, COM5 Enable Signal |
| P1.6/PM_UCA0CLK/COM4 | 6 | P1.6 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | UCA0CLK | X | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | COM4 | X | X | X | 1 |
| P1.7/PM_UCB0CLK/COM5 | 7 | P1.7 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | UCB0CLK | X | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | COM5 | X | X | X | 1 |

(1) X = Don't care

### Table 6-62. Port P2 (P2.0 and P2.1) Pin Functions (MSP430F67xxIPZ Only)

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | | |
|---|---|---|---|---|---|---|
| | | | P2DIR.x | P2SEL.x | P2MAPx | COM6, COM7 Enable Signal |
| P2.0/PM_UCB0SOMI/ PM_UCB0SCL/COM6 | 0 | P2.0 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | UCB0SOMI/UCB0SCL | X | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | COM6 | X | X | X | 1 |
| P2.1/PM_UCB0SIMO/ PM_UCB0SDA/COM7 | 1 | P2.1 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | UCB0SIMO/UCB0SDA | X | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | COM7 | X | X | X | 1 |

(1) X = Don't care


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### 6.12.5 Port P2 (P2.2 to P2.7) Input/Output With Schmitt Trigger (MSP430F67xxIPZ Only)

Figure 6-6 shows the port diagram. Table 6-63 summarizes the selection of the pin functions.

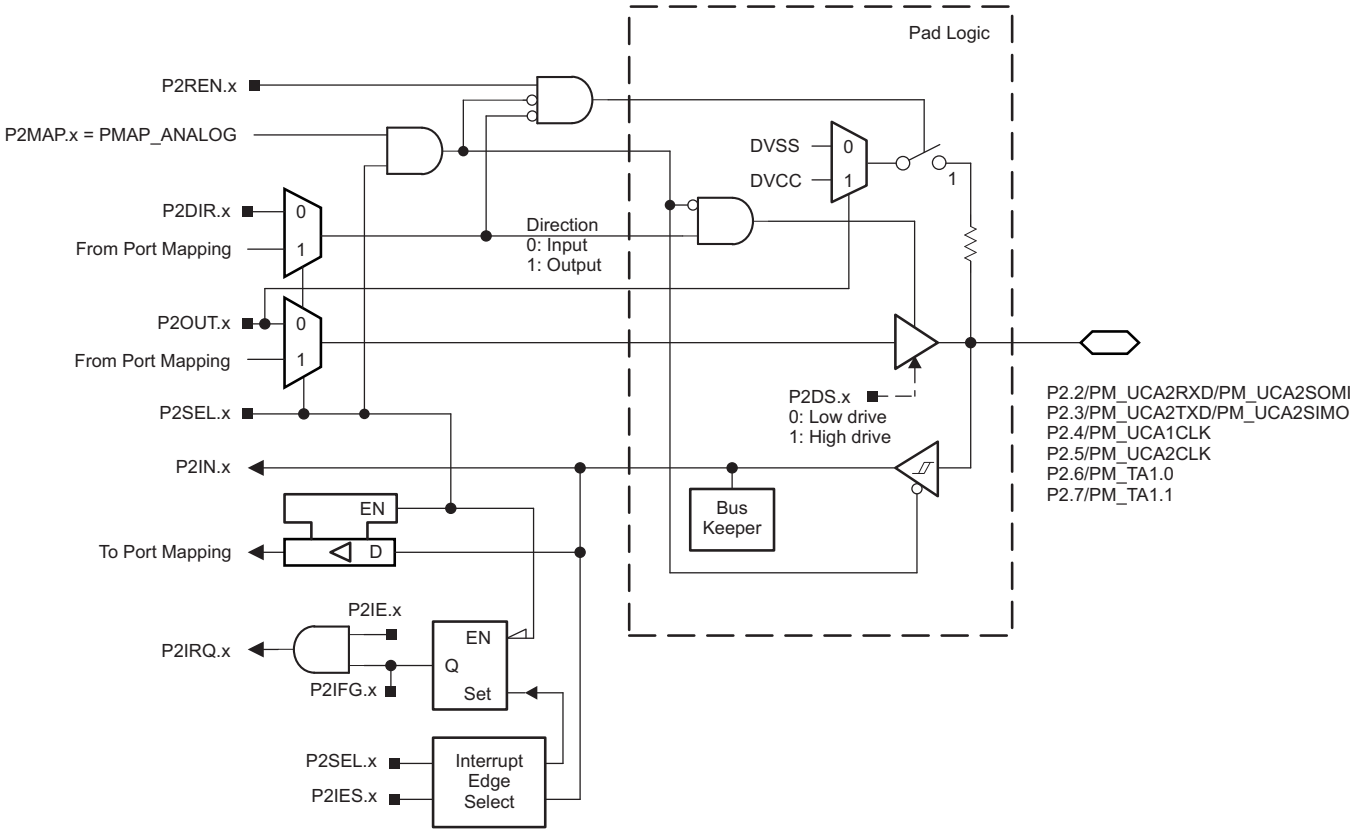


**Figure 6-6. Port P2 (P2.2 to P2.7) Diagram (MSP430F67xxIPZ Only)**

**Table 6-63. Port P2 (P2.2 to P2.7) Pin Functions (MSP430F67xxIPZ Only)**

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P2DIR.x | P2SEL.x | P2MAPx |
| P2.2/PM_UCA2RXD/ PM_UCA2SOMI | 2 | P2.2 (I/O) | I: 0; O: 1 | 0 | X |
| | | UCA2RXD/UCA2SOMI | X | 1 | default |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P2.3/PM_UCA2TXD/ PM_UCA2SIMO | 3 | P2.3 (I/O) | I: 0; O: 1 | 0 | X |
| | | UCA2TXD/UCA2SIMO | X | 1 | default |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P2.4/PM_UCA1CLK | 4 | P2.4 (I/O) | I: 0; O: 1 | 0 | X |
| | | UCA1CLK | X | 1 | default |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P2.5/PM_UCA2CLK | 5 | P2.5 (I/O) | I: 0; O: 1 | 0 | X |
| | | UCA2CLK | X | 1 | default |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P2.6/PM_TA1.0 | 6 | P2.6 (I/O) | I: 0; O: 1 | 0 | X |
| | | TA1.CC10A | 0 | 1 | default |
| | | TA1.TA0 | 1 | 1 | default |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P2.7/PM_TA1.1 | 7 | P2.7 (I/O) | I: 0; O: 1 | 0 | X |
| | | TA1.CCI1A | 0 | 1 | default |
| | | TA1.TA1 | 1 | 1 | default |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |

(1) X = Don't care


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### 6.12.6 Port P3 (P3.0 to P3.3) Input/Output With Schmitt Trigger (MSP430F67xxIPZ Only)

Figure 6-7 shows the port diagram. Table 6-64 summarizes the selection of the pin functions.

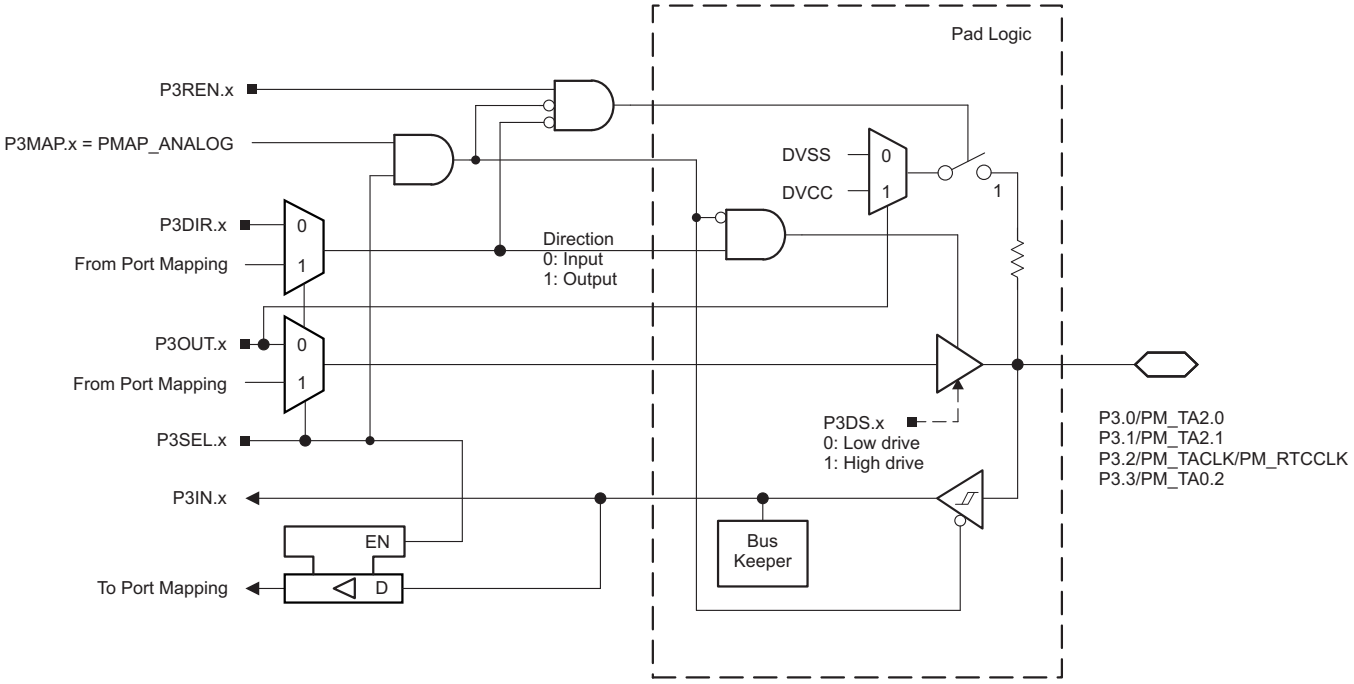


**Figure 6-7. Port P3 (P3.0 to P3.3) Diagram (MSP430F67xxIPZ Only)**

**Table 6-64. Port P3 (P3.0 to P3.3) Pin Functions (MSP430F67xxIPZ Only)**

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P3DIR.x | P3SEL.x | P3MAPx |
| P3.0/PM_TA2.0 | 0 | P3.0 (I/O) | I: 0; O: 1 | 0 | X |
| | | TA2.CC10A | 0 | 1 | default |
| | | TA2.TA0 | 1 | 1 | default |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P3.1/PM_TA2.1 | 1 | P3.1 (I/O) | I: 0; O: 1 | 0 | X |
| | | TA2.CCI1A | 0 | 1 | default |
| | | TA2.TA1 | 1 | 1 | default |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P3.2/PM_TACLK/ PM_RTCCLK | 2 | P3.2 (I/O) | I: 0; O: 1 | 0 | X |
| | | TACLK | 0 | 1 | default |
| | | RTCCLK | 1 | 1 | default |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P3.3/PM_TA0.2 | 3 | P3.3 (I/O) | I: 0; O: 1 | 0 | X |
| | | TA0.CCI2A | 0 | 1 | default |
| | | TA0.TA2 | 1 | 1 | default |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |

(1) X = Don't care

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### 6.12.7 Port P3 (P3.4 to P3.7) Input/Output With Schmitt Trigger (MSP430F67xxIPZ Only)

Figure 6-8 shows the port diagram. Table 6-65 summarizes the selection of the pin functions.

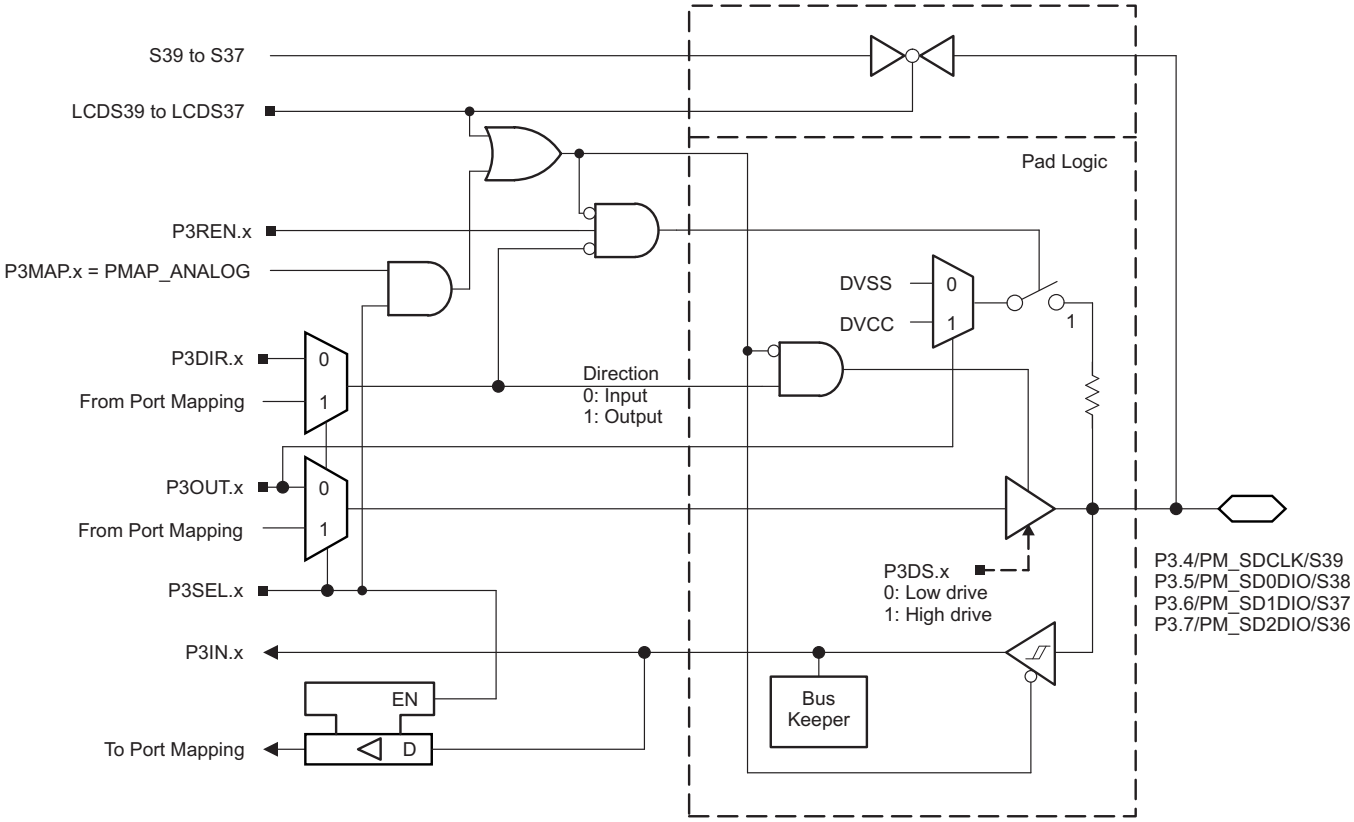


**Figure 6-8. Port P3 (P3.4 to P3.7) Diagram (MSP430F67xxIPZ Only)**


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**Table 6-65. Port P3 (P3.4 to P3.7) Pin Functions (MSP430F67xxIPZ Only)**

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | | |
|---|---|---|---|---|---|---|
| | | | P3DIR.x | P3SEL.x | P3MAPx | LCDS39... LCDS36 |
| P3.4/PM_SDCLK/S39 | 4 | P3.4 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | SDCLK | X | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S39 | X | X | X | 1 |
| P3.5/PM_SD0DIO/S38 | 5 | P3.5 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | SD0DIO | X | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S38 | X | X | X | 1 |
| P3.6/PM_SD1DIO/S37 | 6 | P3.6 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | SD1DIO | X | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S37 | X | X | X | 1 |
| P3.7/PM_SD2DIO/S36 | 7 | P3.7 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | SD2DIO | X | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S36 | X | X | X | 1 |

(1) X = Don't care

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### 6.12.8 Port P4 (P4.0 to P4.7), Port P5 (P5.0 to P5.7), Port P6 (P6.0 to P6.7), Port P7 (P7.0 to P7.7), Port P8 (P8.0 to P8.3) Input/Output With Schmitt Trigger (MSP430F67xxIPZ Only)

Figure 6-9 shows the port diagram. Table 6-66 through Table 6-70 summarize the selection of the pin functions.

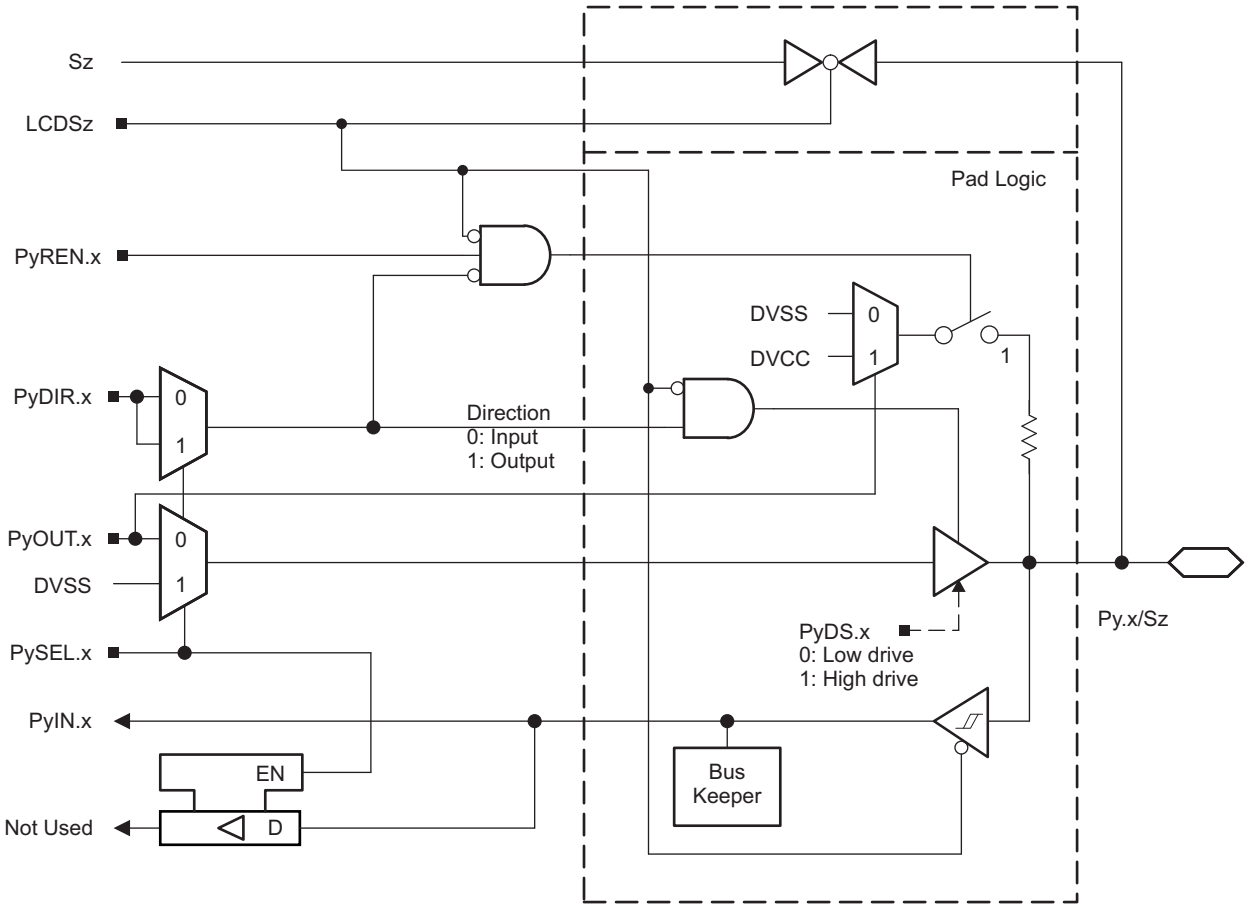


**Figure 6-9. Port P4 (P4.0 to P4.7), Port P5 (P5.0 to P5.7), Port P6 (P6.0 to P6.7), Port P7 (P7.0 to P7.7), Port P8 (P8.0 to P8.3) Diagram (MSP430F67xxIPZ Only)**


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**Table 6-66. Port P4 (P4.0 to P4.7) Pin Functions (MSP430F67xxIPZ Only)**

| PIN NAME (P4.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P4DIR.x | P4SEL.x | LCDS35... LCDS28 |
| P4.0/S35 | 0 | P4.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S35 | X | X | 1 |
| P4.1/S34 | 1 | P4.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S34 | X | X | 1 |
| P4.2/S33 | 2 | P4.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S33 | X | X | 1 |
| P4.3/S32 | 3 | P4.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S32 | X | X | 1 |
| P4.4/S31 | 4 | P4.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S31 | X | X | 1 |
| P4.5/S30 | 5 | P4.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S30 | X | X | 1 |
| P4.6/S29 | 6 | P4.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S29 | X | X | 1 |
| P4.7/S28 | 7 | P4.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S28 | X | X | 1 |

(1) X = Don't care

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**Table 6-67. Port P5 (P5.0 to P5.7) Pin Functions (MSP430F67xxIPZ Only)**

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P5DIR.x | P5SEL.x | LCDS27... LCDS20 |
| P5.0/S27 | 0 | P5.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S27 | X | X | 1 |
| P5.1/S26 | 1 | P5.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S26 | X | X | 1 |
| P5.2/S25 | 2 | P5.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S25 | X | X | 1 |
| P5.3/S24 | 3 | P5.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S24 | X | X | 1 |
| P5.4/S23 | 4 | P5.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S23 | X | X | 1 |
| P5.5/S22 | 5 | P5.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S22 | X | X | 1 |
| P5.6/S21 | 6 | P5.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S21 | X | X | 1 |
| P5.7/S20 | 7 | P5.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S20 | X | X | 1 |

(1) X = Don't care


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**Table 6-68. Port P6 (P6.0 to P6.7) Pin Functions (MSP430F67xxIPZ Only)**

| PIN NAME (P6.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P6DIR.x | P6SEL.x | LCDS19... LCDS12 |
| P6.0/S19 | 0 | P6.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S19 | X | X | 1 |
| P6.1/S18 | 1 | P6.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S18 | X | X | 1 |
| P6.2/S17 | 2 | P6.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S17 | X | X | 1 |
| P6.3/S16 | 3 | P6.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S16 | X | X | 1 |
| P6.4/S15 | 4 | P6.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S15 | X | X | 1 |
| P6.5/S14 | 5 | P6.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S14 | X | X | 1 |
| P6.6/S13 | 6 | P6.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S13 | X | X | 1 |
| P6.7/S12 | 7 | P6.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S12 | X | X | 1 |

(1) X = Don't care

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## Table 6-69. Port P7 (P7.0 to P7.7) Pin Functions (MSP430F67xxIPZ Only)

| PIN NAME (P7.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P7DIR.x | P7SEL.x | LCDS11... LCDS4 |
| P7.0/S11 | 0 | P7.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S11 | X | X | 1 |
| P7.1/S10 | 1 | P7.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S10 | X | X | 1 |
| P7.2/S9 | 2 | P7.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S9 | X | X | 1 |
| P7.3/S8 | 3 | P7.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S8 | X | X | 1 |
| P7.4/S7 | 4 | P7.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S7 | X | X | 1 |
| P7.5/S6 | 5 | P7.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S6 | X | X | 1 |
| P7.6/S5 | 6 | P7.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S5 | X | X | 1 |
| P7.7/S4 | 7 | P7.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S4 | X | X | 1 |

(1) X = Don't care


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**Table 6-70. Port P8 (P8.0 to P8.3) Pin Functions (MSP430F67xxIPZ Only)**

| PIN NAME (P8.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P8DIR.x | P8SEL.x | LCDS3... LCDS0 |
| P8.0/S3 | 0 | P8.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S3 | X | X | 1 |
| P8.1/S2 | 1 | P8.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S2 | X | X | 1 |
| P8.2/S1 | 2 | P8.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S1 | X | X | 1 |
| P8.3/S0 | 3 | P8.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S0 | X | X | 1 |

(1) X = Don't care

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### 6.12.9 Port P8 (P8.4 to P8.7) Input/Output With Schmitt Trigger (MSP430F67xxIPZ Only)

Figure 6-10 shows the port diagram. Table 6-71 summarizes the selection of the pin functions.

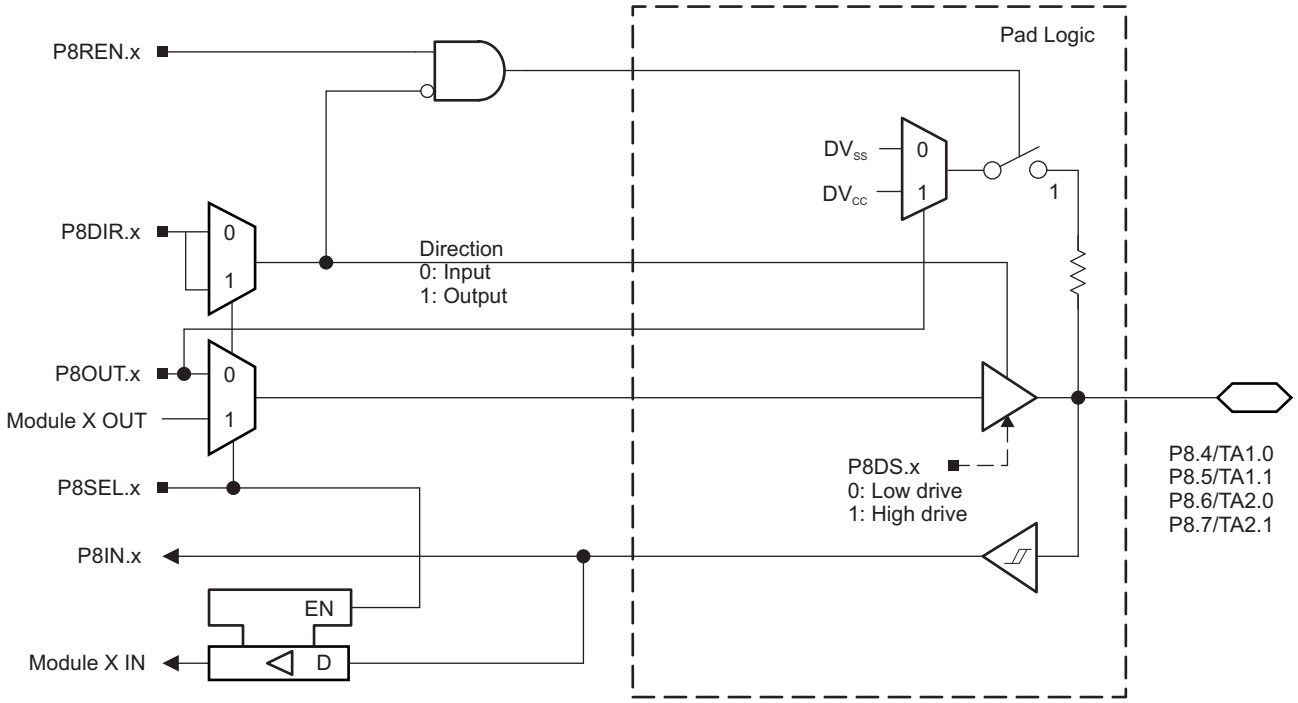


**Figure 6-10. Port P8 (P8.4 to P8.7) Diagram (MSP430F67xxIPZ Only)**

**Table 6-71. Port P8 (P8.4 to P8.7) Pin Functions (MSP430F67xxIPZ Only)**

| PIN NAME (P8.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | |
|---|---|---|---|---|
| | | | P8DIR.x | P8SEL.x |
| P8.4/TA1.0 | 4 | P8.4 (I/O) | I: 0; O: 1 | 0 |
| | | TA1.CCI0A | 0 | 1 |
| | | TA1.TA0 | 1 | 1 |
| P8.5/TA1.1 | 5 | P8.5 (I/O) | I: 0; O: 1 | 0 |
| | | TA1.CCI1A | 0 | 1 |
| | | TA1.TA1 | 1 | 1 |
| P8.6/TA2.0 | 6 | P8.6 (I/O) | I: 0; O: 1 | 0 |
| | | TA2.CCI0A | 0 | 1 |
| | | TA2.TA0 | 1 | 1 |
| P8.7/TA2.1 | 7 | P8.7 (I/O) | I: 0; O: 1 | 0 |
| | | TA2.CCI1A | 0 | 1 |
| | | TA2.TA1 | 1 | 1 |


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### 6.12.10 Port P9 (P9.0) Input/Output With Schmitt Trigger (MSP430F67xxIPZ Only)

Figure 6-11 shows the port diagram. Table 6-72 summarizes the selection of the pin functions.

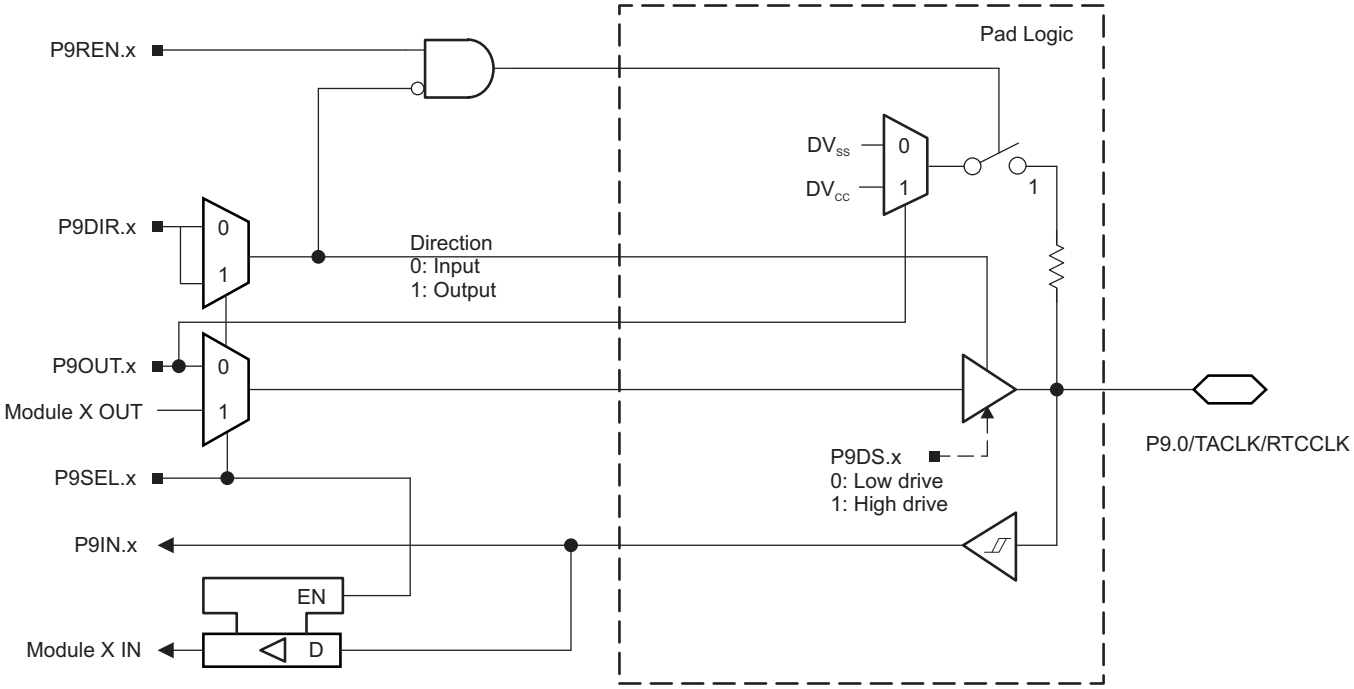


**Figure 6-11. Port P9 (P9.0) Diagram (MSP430F67xxIPZ Only)**

**Table 6-72. Port P9 (P9.0) Pin Functions (MSP430F67xxIPZ Only)**

| PIN NAME (P9.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | |
|---|---|---|---|---|
| | | | P9DIR.x | P9SEL.x |
| P9.0/TACLK/RTCCLK | 0 | P9.0 (I/O) | I: 0; O: 1 | 0 |
| | | TACLK | 0 | 1 |
| | | RTCCLK | 1 | 1 |

### 6.12.11 Port P9 (P9.1 to P9.3) Input/Output With Schmitt Trigger (MSP430F67xxIPZ Only)

Figure 6-12 shows the port diagram. Table 6-73 summarizes the selection of the pin functions.

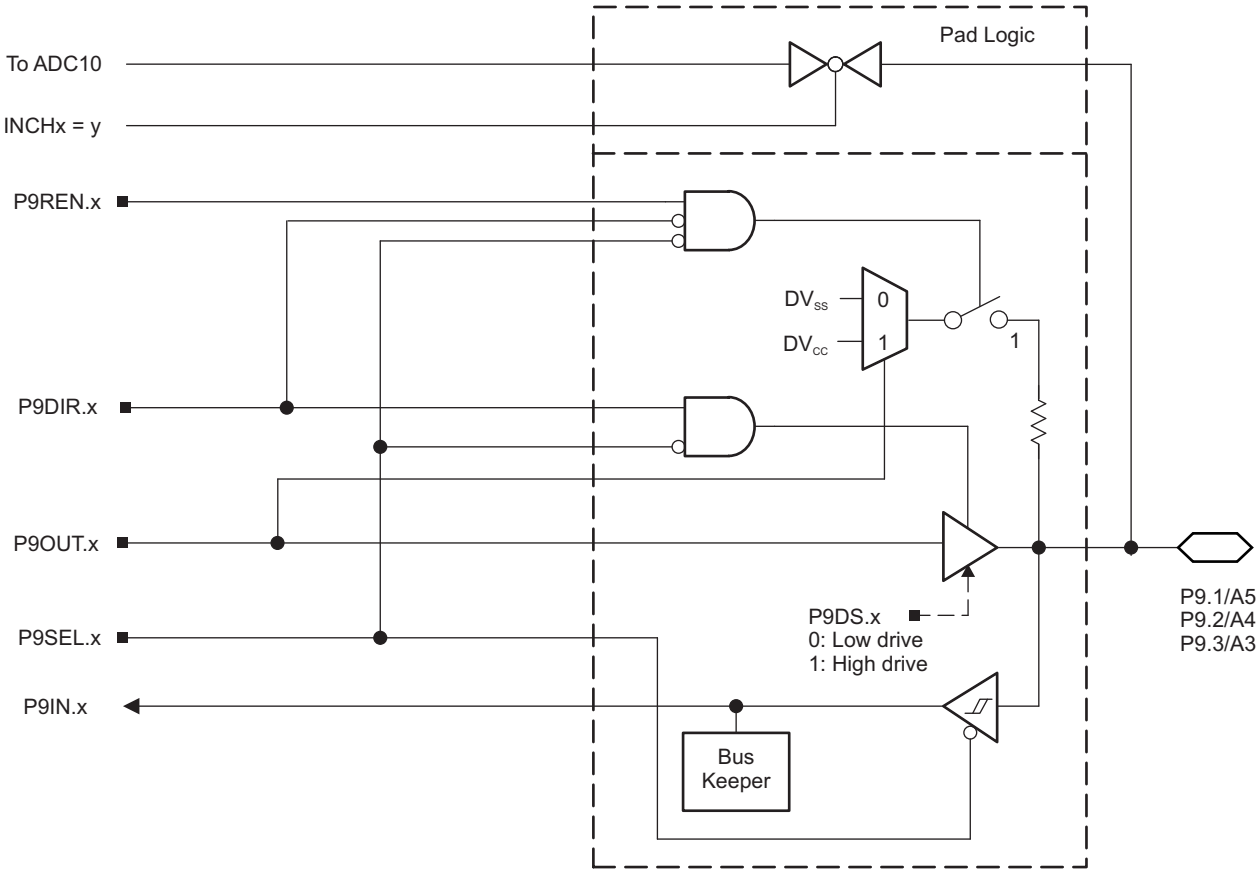


**Figure 6-12. Port P9 (P9.1 to P9.3) Diagram (MSP430F67xxIPZ Only)**

**Table 6-73. Port P9 (P9.1 to P9.3) Pin Functions (MSP430F67xxIPZ Only)**

| PIN NAME (P9.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | |
|---|---|---|---|---|
| | | | P9DIR.x | P9SEL.x |
| P9.1/A5 | 1 | P9.1 (I/O) | I: 0; O: 1 | 0 |
| | | A5(2) | X | 1 |
| P9.2/A4 | 2 | P9.2 (I/O) | I: 0; O: 1 | 0 |
| | | A4(2) | X | 1 |
| P9.3/A3 | 3 | P9.3 (I/O) | I: 0; O: 1 | 0 |
| | | A3(2) | X | 1 |

(1) X = Don't care
(2) Setting P9SEL.x bit disables the output driver and the input Schmitt trigger.


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### 6.12.12 Port P2 (P2.0 and P2.1) Input/Output With Schmitt Trigger (MSP430F67xxIPN Only)

Figure 6-13 shows the port diagram. Table 6-74 summarizes the selection of the pin functions.

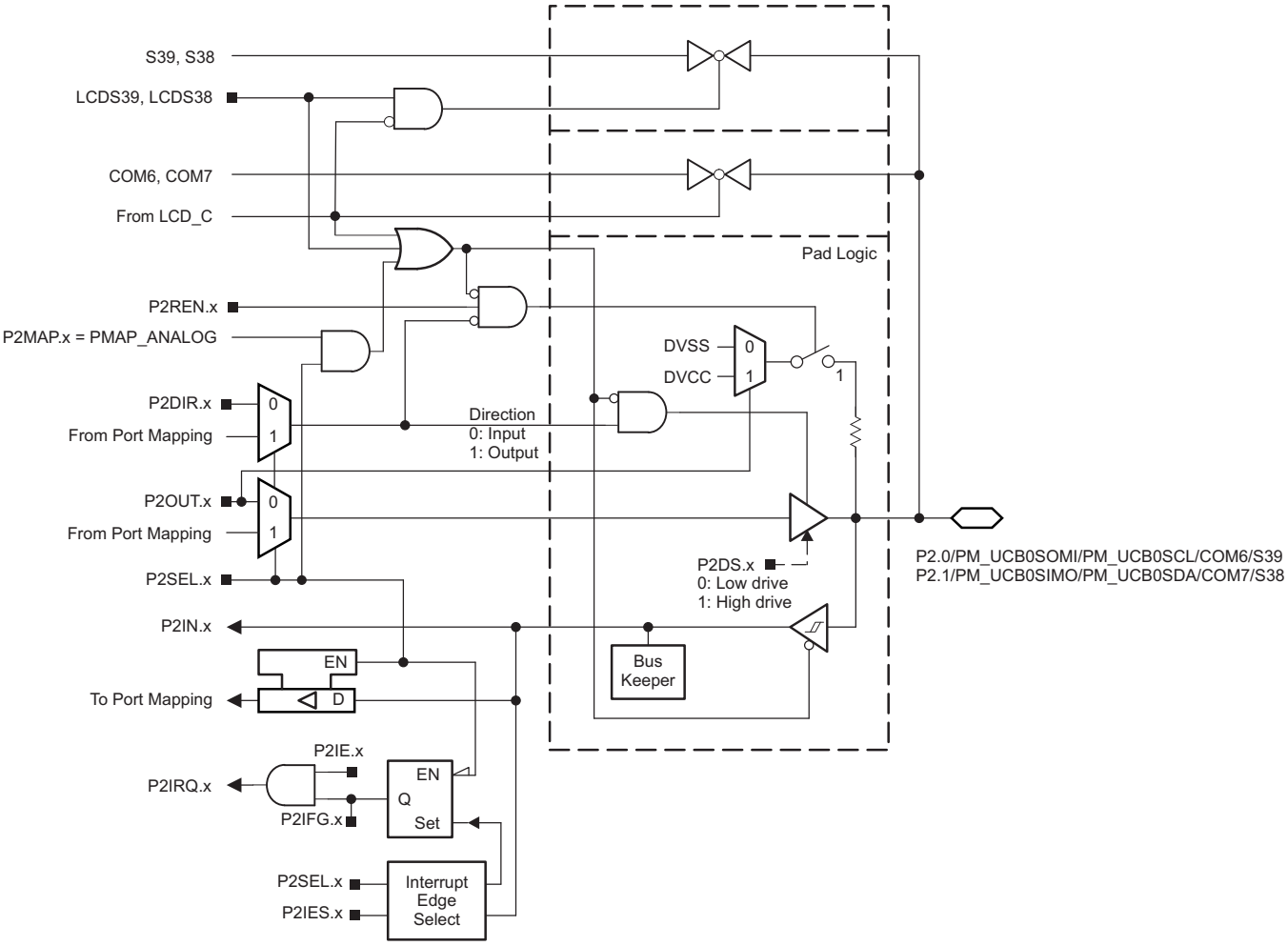


**Figure 6-13. Port P2 (P2.0 and P2.1) Diagram (MSP430F67xxIPN Only)**

**Table 6-74. Port P2 (P2.0 and P2.1) Pin Functions (MSP430F67xxIPN Only)**

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | | | |
|---|---|---|---|---|---|---|---|
| | | | P2DIR.x | P2SEL.x | P2MAPx | LCDS39, LCDS38 | COM6, COM7 Enable Signal |
| P2.0/PM_UCB0SOMI/ PM_UCB0SCL/COM6/ S39 | 0 | P2.0 (I/O) | I: 0; O: 1 | 0 | X | 0 | 0 |
| | | UCB0SOMI/UCB0SCL | X | 1 | default | 0 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 | 0 |
| | | COM6 | X | X | X | X | 1 |
| | | S39 | X | X | X | 1 | 0 |
| P2.1/PM_UCB0SIMO/ PM_UCB0SDA/COM7/ S38 | 1 | P2.1 (I/O) | I: 0; O: 1 | 0 | X | 0 | 0 |
| | | UCB0SIMO/UCB0SDA | X | 1 | default | 0 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 | 0 |
| | | COM7 | X | X | X | X | 1 |
| | | S38 | X | X | X | 1 | 0 |

(1) X = Don't care


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### 6.12.13 Port P2 (P2.2 to P2.7) Input/Output With Schmitt Trigger (MSP430F67xxIPN Only)

Figure 6-14 shows the port diagram. Table 6-75 summarizes the selection of the pin functions.

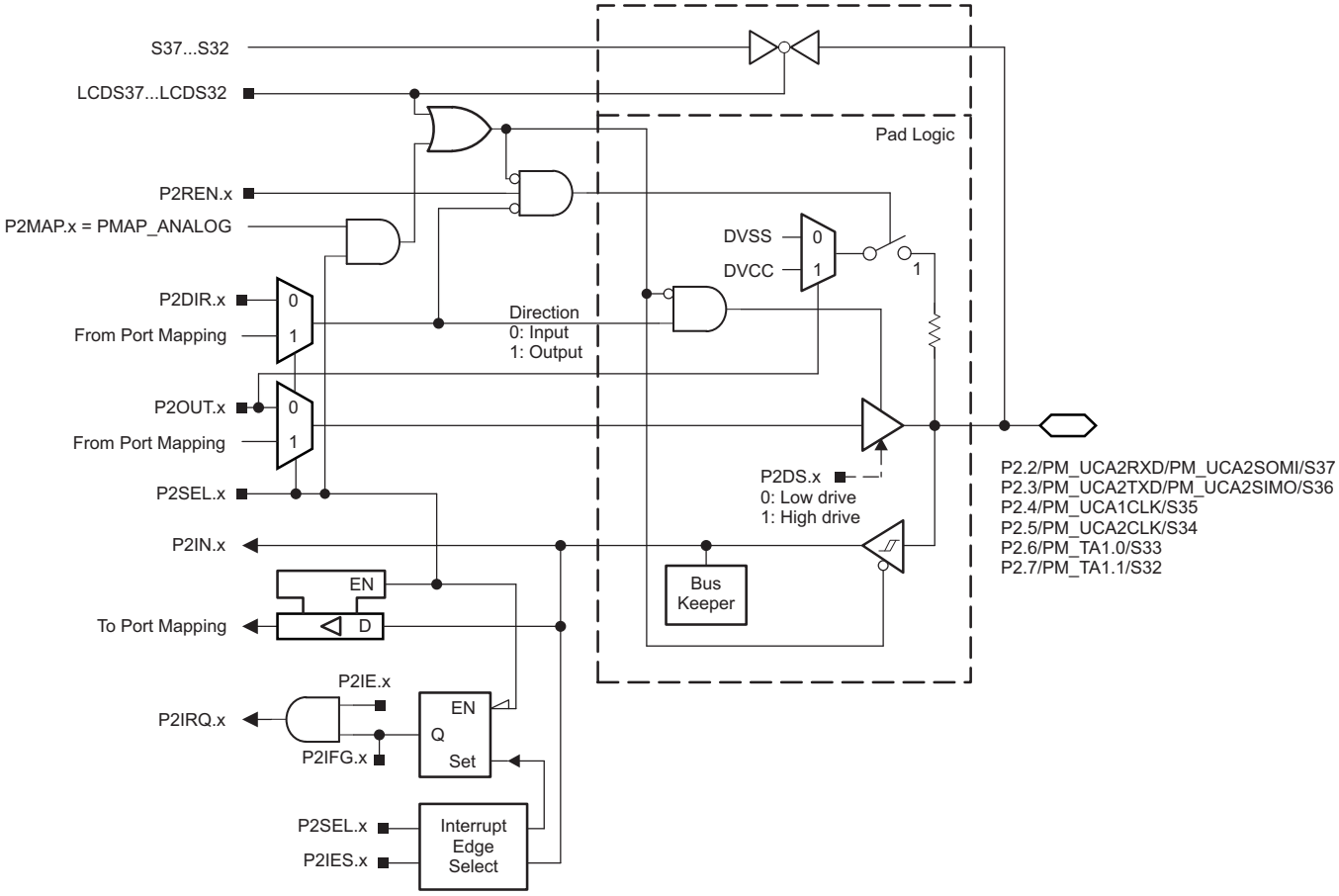


**Figure 6-14. Port P2 (P2.2 to P2.7) Diagram (MSP430F67xxIPN Only)**

**Table 6-75. Port P2 (P2.2 to P2.7) Pin Functions (MSP430F67xxIPN Only)**

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | | |
|---|---|---|---|---|---|---|
| | | | P2DIR.x | P2SEL.x | P2MAPx | LCDS37... LCDS32 |
| P2.2/PM_UCA2RXD/ PM_UCA2SOMI/S37 | 2 | P2.2 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | UCA2RXD/UCA2SOMI | X | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S37 | X | X | X | 1 |
| P2.3/PM_UCA2TXD/ PM_UCA2SIMO/S36 | 3 | P2.3 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | UCA2TXD/UCA2SIMO | X | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S36 | X | X | X | 1 |
| P2.4/PM_UCA1CLK/S35 | 4 | P2.4 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | UCA1CLK | X | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S35 | X | X | X | 1 |
| P2.5/PM_UCA2CLK/S34 | 5 | P2.5 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | UCA2CLK | X | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S34 | X | X | X | 1 |
| P2.6/PM_TA1.0/S33 | 6 | P2.6 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | TA1.CCI0A | 0 | 1 | default | 0 |
| | | TA1.TA0 | 1 | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S33 | X | X | X | 1 |
| P2.7/PM_TA1.1/S32 | 7 | P2.7 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | TA1.CCI1A | 0 | 1 | default | 0 |
| | | TA1.TA1 | 1 | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S32 | X | X | X | 1 |

(1) X = Don't care


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### 6.12.14 Port P3 (P3.0 to P3.7) Input/Output With Schmitt Trigger (MSP430F67xxIPN Only)

Figure 6-15 shows the port diagram. Table 6-76 summarizes the selection of the pin functions.

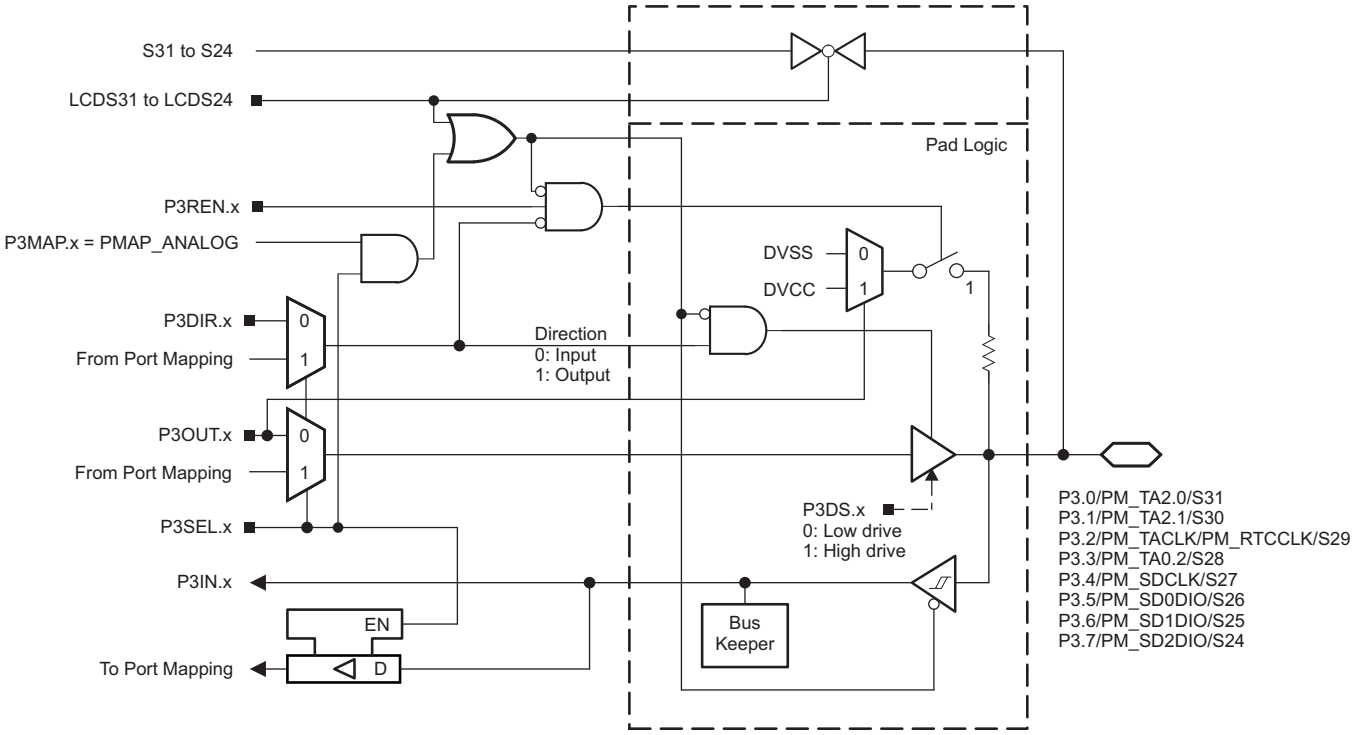


**Figure 6-15. Port P3 (P3.0 to P3.7) Diagram (MSP430F67xxIPN Only)**

**Table 6-76. Port P3 (P3.0 to P3.7) Pin Functions (MSP430F67xxIPN Only)**

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | | |
|---|---|---|---|---|---|---|
| | | | P3DIR.x | P3SEL.x | P3MAPx | LCDS31... LCDS24 |
| P3.0/PM_TA2.0/S31 | 0 | P3.0 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | TA2.CCI0A | 0 | 1 | default | 0 |
| | | TA2.TA0 | 1 | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S31 | X | X | X | 1 |
| P3.1/PM_TA2.1/S30 | 1 | P3.1 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | TA2.CCI1A | 0 | 1 | default | 0 |
| | | TA2.TA1 | 1 | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S30 | X | X | X | 1 |
| P3.2/PM_TACLK/ PM_RTCCLK/S29 | 2 | P3.2 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | TACLK | 0 | 1 | default | 0 |
| | | RTCCLK | 1 | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S29 | X | X | X | 1 |
| P3.3/PM_TA0.2/S28 | 3 | P3.3 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | TA0.CCI2A | 0 | 1 | default | 0 |
| | | TA0.TA2 | 1 | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S28 | X | X | X | 1 |
| P3.4/PM_SDCLK/S27 | 4 | P3.4 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | SDCLK | X | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S27 | X | X | X | 1 |
| P3.5/PM_SD0DIO/S26 | 5 | P3.5 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | SD0DIO | X | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S26 | X | X | X | 1 |
| P3.6/PM_SD1DIO/S25 | 6 | P3.6 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | SD1DIO | X | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S25 | X | X | X | 1 |
| P3.7/PM_SD2DIO/S24 | 7 | P3.7 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | SD2DIO | X | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S24 | X | X | X | 1 |

(1) X = Don't care


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### 6.12.15 Port P4 (P4.0 to P4.7), Port P5 (P5.0 to P5.7), Port P6 (P6.0 to P6.7) Input/Output With Schmitt Trigger (MSP430F67xxIPN Only)

Figure 6-16 shows the port diagram. Table 6-77 through Table 6-79 summarize the selection of the pin functions.

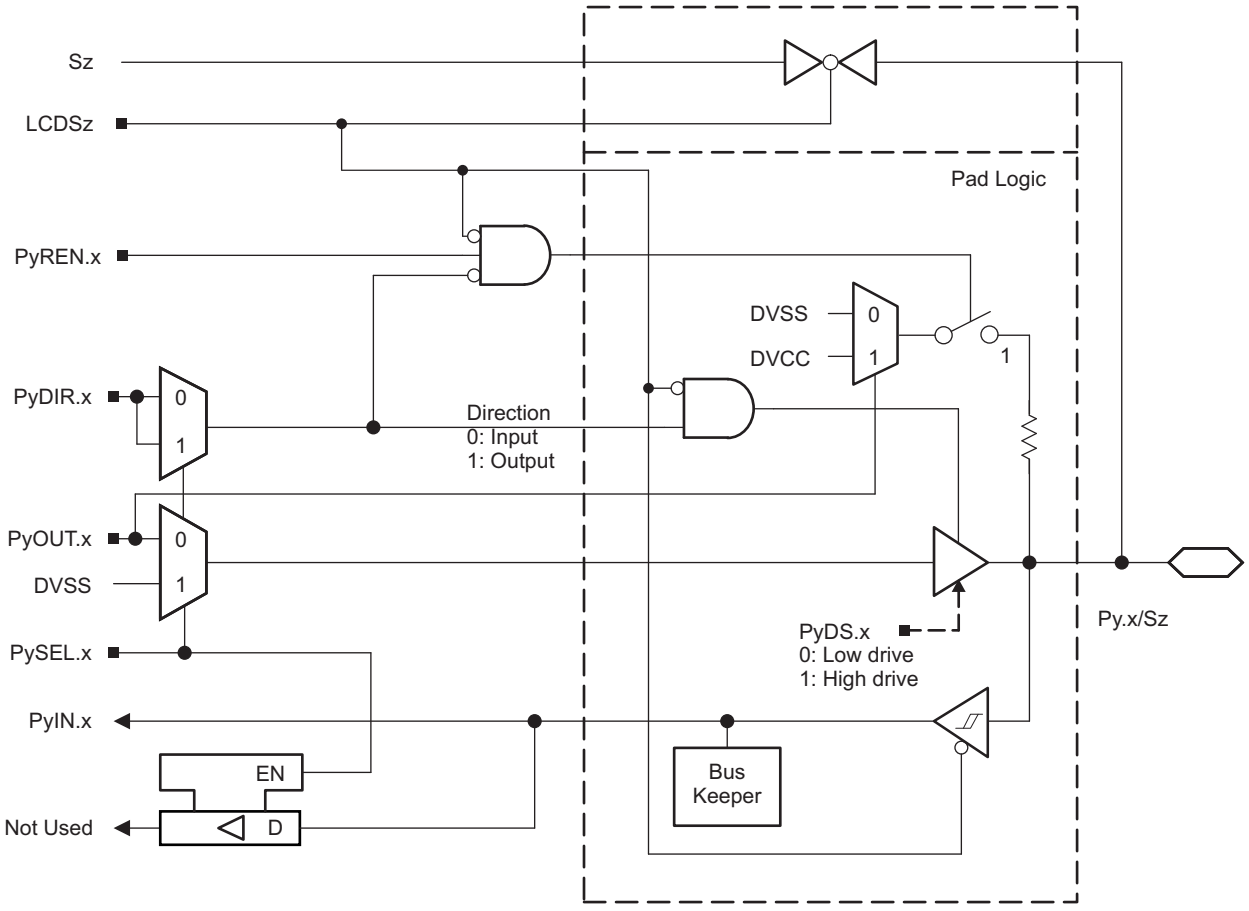


**Figure 6-16. Port P4 (P4.0 to P4.7), Port P5 (P5.0 to P5.7), Port P6 (P6.0 to P6.7) Diagram (MSP430F67xxIPN Only)**

**Table 6-77. Port P4 (P4.0 to P4.7) Pin Functions (MSP430F67xxIPN Only)**

| PIN NAME (P4.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P4DIR.x | P4SEL.x | LCDS23... LCDS16 |
| P4.0/S23 | 0 | P4.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S23 | X | X | 1 |
| P4.1/S22 | 1 | P4.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S22 | X | X | 1 |
| P4.2/S21 | 2 | P4.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S21 | X | X | 1 |
| P4.3/S20 | 3 | P4.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S20 | X | X | 1 |
| P4.4/S19 | 4 | P4.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S19 | X | X | 1 |
| P4.5/S18 | 5 | P4.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S18 | X | X | 1 |
| P4.6/S17 | 6 | P4.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S17 | X | X | 1 |
| P4.7/S16 | 7 | P4.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S16 | X | X | 1 |

(1) X = Don't care


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**Table 6-78. Port P5 (P5.0 to P5.7) Pin Functions (MSP430F67xxIPN Only)**

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P5DIR.x | P5SEL.x | LCDS15... LCDS8 |
| P5.0/S15 | 0 | P5.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S15 | X | X | 1 |
| P5.1/S14 | 1 | P5.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S14 | X | X | 1 |
| P5.2/S13 | 2 | P5.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S13 | X | X | 1 |
| P5.3/S12 | 3 | P5.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S12 | X | X | 1 |
| P5.4/S11 | 4 | P5.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S11 | X | X | 1 |
| P5.5/S10 | 5 | P5.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S10 | X | X | 1 |
| P5.6/S9 | 6 | P5.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S9 | X | X | 1 |
| P5.7/S8 | 7 | P5.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S8 | X | X | 1 |

(1) X = Don't care

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**Table 6-79. Port P6 (P6.0 to P6.7) Pin Functions (MSP430F67xxIPN Only)**

| PIN NAME (P6.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P6DIR.x | P6SEL.x | LCDS7... LCDS0 |
| P6.0/S7 | 0 | P6.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S7 | X | X | 1 |
| P6.1/S6 | 1 | P6.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S6 | X | X | 1 |
| P6.2/S5 | 2 | P6.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S5 | X | X | 1 |
| P6.3/S4 | 3 | P6.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S4 | X | X | 1 |
| P6.4/S3 | 4 | P6.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S3 | X | X | 1 |
| P6.5/S2 | 5 | P6.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S2 | X | X | 1 |
| P6.6/S1 | 6 | P6.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S1 | X | X | 1 |
| P6.7/S0 | 7 | P6.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S0 | X | X | 1 |

(1) X = Don't care


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### 6.12.16 Port PJ (PJ.0) JTAG Pin TDO, Input/Output With Schmitt Trigger or Output

Figure 6-17 shows the port diagram. Table 6-80 summarizes the selection of the pin functions.

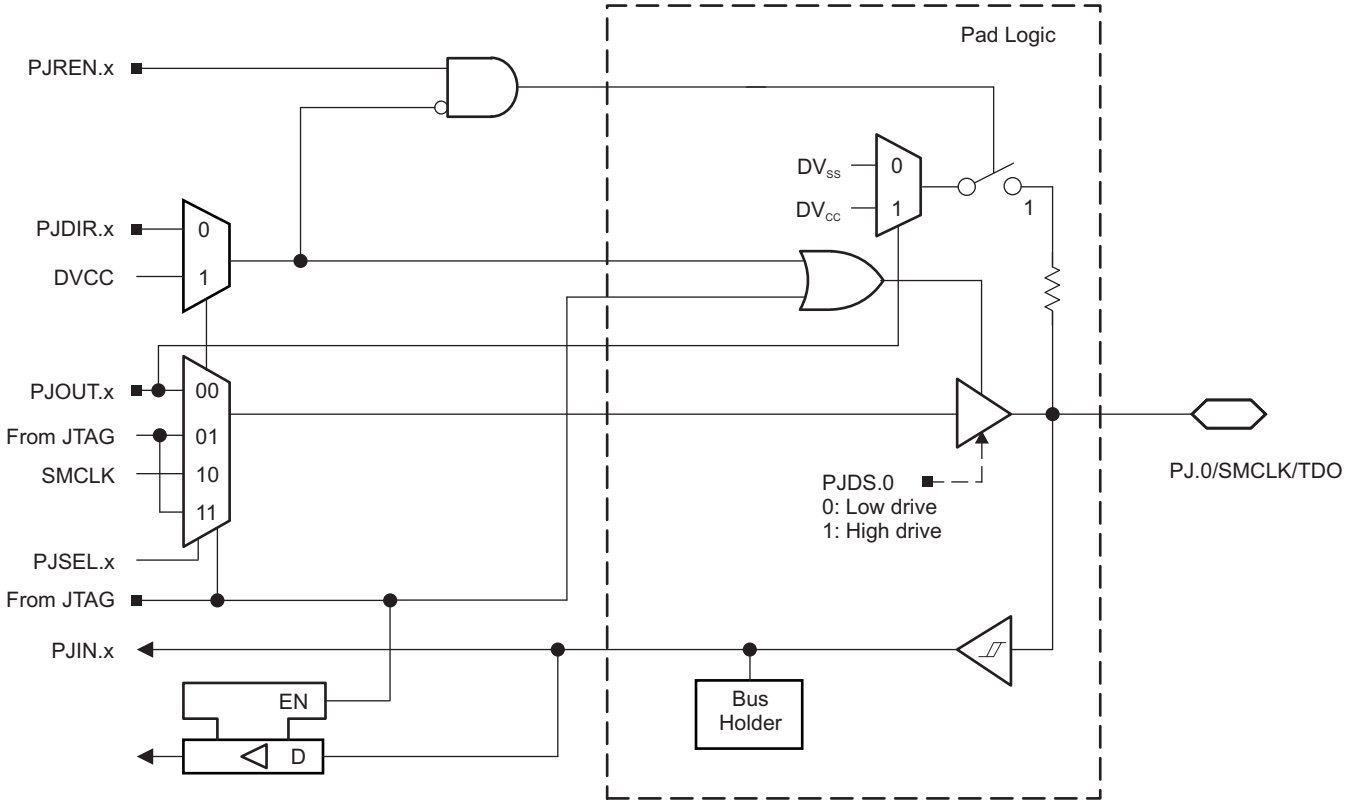


**Figure 6-17. Port PJ (PJ.0) Diagram**

### 6.12.17 Port PJ (PJ.1 to PJ.3) JTAG Pins TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger or Output

Figure 6-18 shows the port diagram. Table 6-80 summarizes the selection of the pin functions.

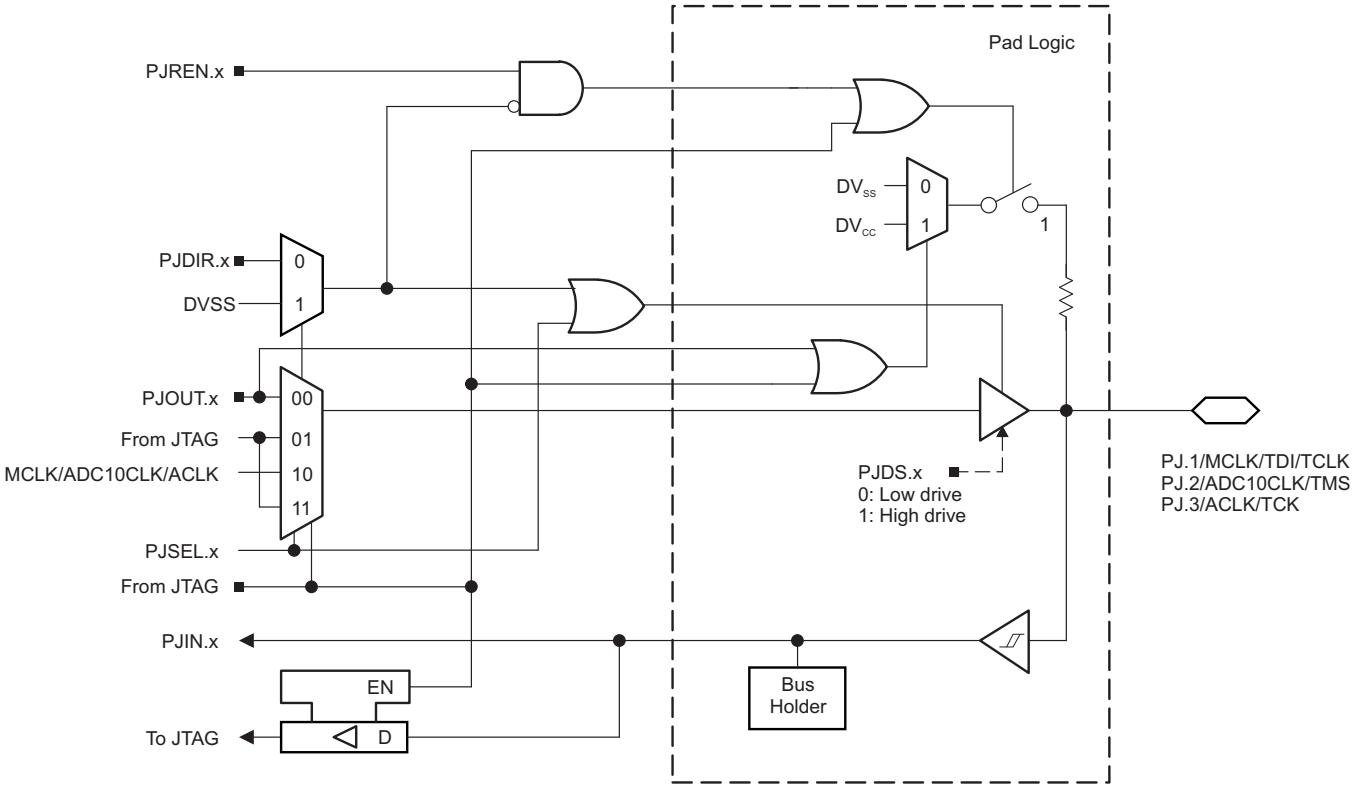


**Figure 6-18. Port PJ (PJ.1 to PJ.3) Diagram**

**Table 6-80. Port PJ (PJ.0 to PJ.3) Pin Functions**

| PIN NAME (PJ.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | PJDIR.x | PJSEL.x | JTAG Mode Signal |
| PJ.0/SMCLK/TDO | 0 | PJ.0 (I/O)(2) | I: 0; O: 1 | 0 | 0 |
| | | SMCLK | 1 | 1 | 0 |
| | | TDO(3) | X | X | 1 |
| PJ.1/MCLK/TDI/TCLK | 1 | PJ.1 (I/O)(2) | I: 0; O: 1 | 0 | 0 |
| | | MCLK | 1 | 1 | 0 |
| | | TDI/TCLK (3)(4) | X | X | 1 |
| PJ.2/ADC10CLK/TMS | 2 | PJ.2 (I/O)(2) | I: 0; O: 1 | 0 | 0 |
| | | ADC10CLK | 1 | 1 | 0 |
| | | TMS (3)(4) | X | X | 1 |
| PJ.3/ACLK/TCK | 3 | PJ.3 (I/O)(2) | I: 0; O: 1 | 0 | 0 |
| | | ACLK | 1 | 1 | 0 |
| | | TCK (3)(4) | X | X | 1 |

(1) X = Don't care
(2) Default condition
(3) The pin direction is controlled by the JTAG module.
(4) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are don't care.


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## 6.13 Device Descriptors (TLV)

Table 6-81 and Table 6-82 list the contents of the device descriptor tag-length-value (TLV) structure for each device type.

**Table 6-81. MSP430F673x Device Descriptors**

| DESCRIPTION | | ADDRESS | SIZE (bytes) | VALUE | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | F6736PZ F6736PN | F6735PZ F6735PN | F6734PZ F6734PN | F6733PZ F6733PN | F6731PZ F6731PN | F6730PZ F6730PN |
| Info Block | Info length | 01A00h | 1 | 06h | 06h | 06h | 06h | 06h | 06h |
| | CRC length | 01A01h | 1 | 06h | 06h | 06h | 06h | 06h | 06h |
| | CRC value | 01A02h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Device ID | 01A04h | 1 | 6Ch | 6Bh | 6Ah | 65h | 63h | 62h |
| | Device ID | 01A05h | 1 | 81h | 81h | 81h | 80h | 80h | 80h |
| | Hardware revision | 01A06h | 1 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Firmware revision | 01A07h | 1 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| Die Record | Die record tag | 01A08h | 1 | 08h | 08h | 08h | 08h | 08h | 08h |
| | Die record length | 01A09h | 1 | 0Ah | 0Ah | 0Ah | 0Ah | 0Ah | 0Ah |
| | Lot/wafer ID | 01A0Ah | 4 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Die X position | 01A0Eh | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Die Y position | 01A10h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Test results | 01A12h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| ADC10 Calibration | ADC10 calibration tag | 01A14h | 1 | 13h | 13h | 13h | 13h | 13h | 13h |
| | ADC10 calibration length | 01A15h | 1 | 10h | 10h | 10h | 10h | 10h | 10h |
| | ADC gain factor | 01A16h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC offset | 01A18h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 1.5-V reference Temperature sensor 30°C | 01A1Ah | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 1.5-V reference Temperature sensor 85°C | 01A1Ch | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 2.0-V reference Temperature sensor 30°C | 01A1Eh | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 2.0-V reference Temperature sensor 85°C | 01A20h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 2.5-V reference Temperature sensor 30°C | 01A22h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 2.5-V reference Temperature sensor 85°C | 01A24h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |

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## Table 6-82. MSP430F672x Device Descriptors

| DESCRIPTION | | ADDRESS | SIZE (bytes) | VALUE | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | F6726PZ F6726PN | F6725PZ F6725PN | F6724PZ F6724PN | F6723PZ F6723PN | F6721PZ F6721PN | F6720PZ F6720PN |
| Info Block | Info length | 01A00h | 1 | 06h | 06h | 06h | 06h | 06h | 06h |
| | CRC length | 01A01h | 1 | 06h | 06h | 06h | 06h | 06h | 06h |
| | CRC value | 01A02h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Device ID | 01A04h | 1 | 6Fh | 6Eh | 6Dh | 61h | 59h | 58h |
| | Device ID | 01A05h | 1 | 81h | 81h | 81h | 80h | 80h | 80h |
| | Hardware revision | 01A06h | 1 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Firmware revision | 01A07h | 1 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| Die Record | Die record tag | 01A08h | 1 | 08h | 08h | 08h | 08h | 08h | 08h |
| | Die record length | 01A09h | 1 | 0Ah | 0Ah | 0Ah | 0Ah | 0Ah | 0Ah |
| | Lot/wafer ID | 01A0Ah | 4 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Die X position | 01A0Eh | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Die Y position | 01A10h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Test results | 01A12h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| ADC10 Calibration | ADC10 calibration tag | 01A14h | 1 | 13h | 13h | 13h | 13h | 13h | 13h |
| | ADC10 calibration length | 01A15h | 1 | 10h | 10h | 10h | 10h | 10h | 10h |
| | ADC gain factor | 01A16h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC offset | 01A18h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 1.5-V reference Temperature sensor 30°C | 01A1Ah | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 1.5-V reference Temperature sensor 85°C | 01A1Ch | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 2.0-V reference Temperature sensor 30°C | 01A1Eh | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 2.0-V reference Temperature sensor 85°C | 01A20h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 2.5-V reference Temperature sensor 30°C | 01A22h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 2.5-V reference Temperature sensor 85°C | 01A24h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |


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# 7 Device and Documentation Support

## 7.1 Getting Started and Next Steps

For more information on the MSP430™ family of devices and the tools and libraries that are available to help with your development, visit the Getting Started page.

## 7.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices. Each MSP MCU commercial family member has one of two prefixes: MSP or XMS. These prefixes represent evolutionary stages of product development from engineering prototypes (XMS) through fully qualified production devices (MSP).

**XMS** – Experimental device that is not necessarily representative of the final device's electrical specifications

**MSP** – Fully qualified production device

XMS devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. Figure 7-1 provides a legend for reading the complete device name.

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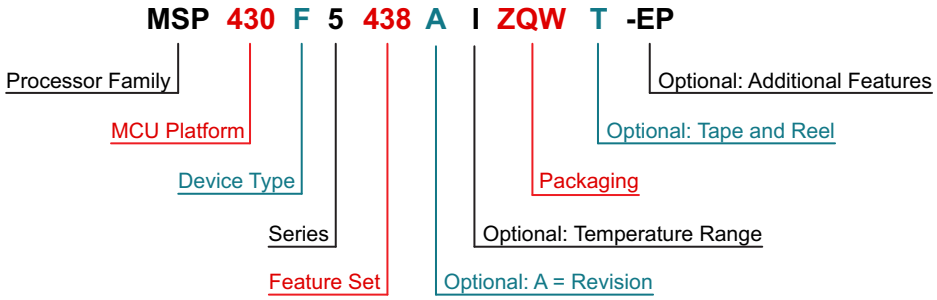


| | | |
|---|---|---|
| **Processor Family** | CC = Embedded RF Radio<br>MSP = Mixed-Signal Processor<br>XMS = Experimental Silicon<br>PMS = Prototype Device | |
| **MCU Platform** | 430 = MSP430 low-power microcontroller platform | |
| **Device Type** | **Memory Type**<br>C = ROM<br>F = Flash<br>FR = FRAM<br>G = Flash or FRAM (Value Line)<br>L = No Nonvolatile Memory | **Specialized Application**<br>AFE = Analog Front End<br>BQ = Contactless Power<br>CG = ROM Medical<br>FE = Flash Energy Meter<br>FG = Flash Medical<br>FW = Flash Electronic Flow Meter |
| **Series** | 1 = Up to 8 MHz<br>2 = Up to 16 MHz<br>3 = Legacy<br>4 = Up to 16 MHz with LCD | 5 = Up to 25 MHz<br>6 = Up to 25 MHz with LCD<br>0 = Low-Voltage Series |
| **Feature Set** | Various levels of integration within a series | |
| **Optional: A = Revision** | N/A | |
| **Optional: Temperature Range** | S = 0°C to 50°C<br>C = 0°C to 70°C<br>I = –40°C to 85°C<br>T = –40°C to 105°C | |
| **Packaging** | http://www.ti.com/packaging | |
| **Optional: Tape and Reel** | T = Small reel<br>R = Large reel<br>No markings = Tube or tray | |
| **Optional: Additional Features** | -EP = Enhanced Product (–40°C to 105°C)<br>-HT = Extreme Temperature Parts (–55°C to 150°C)<br>-Q1 = Automotive Q100 Qualified | |

**Figure 7-1. Device Nomenclature**


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## 7.3 Tools and Software

All MSP microcontrollers are supported by a wide variety of software and hardware development tools. Tools are available from TI and various third parties. See them all at MSP430 Ultra-Low-Power MCUs – Tools & software.

Table 7-1 lists the debug features of the MSP430F673x and MSP430F672x MCUs. See the *Code Composer Studio for MSP430 User's Guide* for details on the available features.

**Table 7-1. Hardware Debug Features**

| MSP430 ARCHITECTURE | 4-WIRE JTAG | 2-WIRE JTAG | BREAK-POINTS (N) | RANGE BREAK-POINTS | CLOCK CONTROL | STATE SEQUENCER | TRACE BUFFER | LPMX.5 DEBUGGING SUPPORT |
|---|---|---|---|---|---|---|---|---|
| MSP430Xv2 | Yes | Yes | 3 | Yes | Yes | No | No | No |

### Design Kits and Evaluation Modules

**MSP-TS430PZ100B - 100-pin Target Development Board for MSP430F6x MCUs** The MSP-TS430PZ100B is a stand-alone 100-pin ZIF socket target board used to program and debug the MSP430 MCU in-system through the JTAG interface or the Spy Bi-Wire (2-wire JTAG) protocol.

**100-pin Target Development Board and MSP-FET Programmer Bundle for MSP430F6x MCUs** The MSP-FET is a powerful flash emulation tool to quickly begin application development on the MSP430 MCU. It includes USB debugging interface used to program and debug the MSP430 in-system through the JTAG interface or the pin saving Spy Bi-Wire (2-wire JTAG) protocol.

**EVM430-F6736 - MSP430F6736 EVM for Metering** This EVM430-F6736 is a single-phase electricity meter evaluation module based on the MSP430F6736 device. The E-meter can be connected to the main power lines and has inputs for voltage and current, as well as a third connection to setup anti-tampering.

### Software

**MSP430Ware™ Software** MSP430Ware software is a collection of code examples, data sheets, and other design resources for all MSP430 devices delivered in a convenient package. In addition to providing a complete collection of existing MSP430 design resources, MSP430Ware software also includes a high-level API called MSP Driver Library. This library makes it easy to program MSP430 hardware. MSP430Ware software is available as a component of CCS or as a stand-alone package.

**Energy Measurement Design Center for MSP430 MCUs** The Energy Measurement Design Center is a rapid development tool that enables energy measurement using TI MSP430i20xx and MSP430F67xx flash-based microcontrollers (MCUs). It includes a graphical user interface (GUI), documentation, software library, and examples that can simplify development and accelerate designs in a wide range of power monitoring and energy measurement applications, including smart grid and building automation. Using the Design Center, you can configure, calibrate, and view results without writing a single line of code.

**MSP Driver Library** The abstracted API of MSP Driver Library provides easy-to-use function calls that free you from directly manipulating the bits and bytes of the MSP430 hardware. Thorough documentation is delivered through a helpful API Guide, which includes details on each function call and the recognized parameters. Developers can use Driver Library functions to write complete projects with minimal overhead.

**IEC60730 Software Package** The IEC60730 MSP430 software package was developed to help customers comply with IEC 60730-1:2010 (Automatic Electrical Controls for Household and Similar Use – Part 1: General Requirements) for up to Class B products, which includes home appliances, arc detectors, power converters, power tools, e-bikes, and many others. The IEC60730 MSP430 software package can be embedded in customer applications running on MSP430s to help simplify the customer's certification efforts of functional safety-compliant consumer devices to IEC 60730-1:2010 Class B.

**MSP430F673x, MSP430F672x Code Examples** C code examples are available for every MSP device that configures each of the integrated peripherals for various application needs.

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**Capacitive Touch Software Library** Free C libraries for enabling capacitive touch capabilities on MSP430 MCUs. The MSP430 MCU version of the library features several capacitive touch implementations including the RO and RC method.

**MSP EnergyTrace™ Technology** EnergyTrace technology for MSP430 microcontrollers is an energy-based code analysis tool that measures and displays the energy profile of the application and helps to optimize it for ultra-low-power consumption.

**ULP (Ultra-Low Power) Advisor** ULP Advisor™ software is a tool for guiding developers to write more efficient code to fully use the unique ultra-low-power features of MSP and MSP432 microcontrollers. Aimed at both experienced and new microcontroller developers, ULP Advisor checks your code against a thorough ULP checklist to help minimize the energy consumption of your application. At build time, ULP Advisor provides notifications and remarks to highlight areas of your code that can be further optimized for lower power.

**Fixed Point Math Library for MSP** The MSP IQmath and Qmath Libraries are a collection of highly optimized and high-precision mathematical functions for C programmers to seamlessly port a floating-point algorithm into fixed-point code on MSP430 and MSP432 devices. These routines are typically used in computationally intensive real-time applications where optimal execution speed, high accuracy, and ultra-low energy are critical. By using the IQmath and Qmath libraries, it is possible to achieve execution speeds considerably faster and energy consumption considerably lower than equivalent code written using floating-point math.

**Floating Point Math Library for MSP430** Continuing to innovate in the low-power and low-cost microcontroller space, TI provides MSPMATHLIB. Leveraging the intelligent peripherals of our devices, this floating-point math library of scalar functions that are up to 26 times faster than the standard MSP430 math functions. Mathlib is easy to integrate into your designs. This library is free and is integrated in both Code Composer Studio IDE and IAR Embedded Workbench IDE.

### Development Tools

**Code Composer Studio™ Integrated Development Environment for MSP Microcontrollers** Code Composer Studio (CCS) integrated development environment (IDE) supports all MSP microcontroller devices. CCS comprises a suite of embedded software utilities used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features.

**Command-Line Programmer** MSP Flasher is an open-source shell-based interface for programming MSP microcontrollers through a FET programmer or eZ430 using JTAG or Spy-Bi-Wire (SBW) communication. MSP Flasher can download binary files (.txt or .hex) directly to the MSP microcontroller without an IDE.

**MSP MCU Programmer and Debugger** The MSP-FET is a powerful emulation development tool – often called a debug probe – which lets users quickly begin application development on MSP low-power MCUs. Creating MCU software usually requires downloading the resulting binary program to the MSP device for validation and debugging.

**MSP-GANG Production Programmer** The MSP Gang Programmer is an MSP430 or MSP432 device programmer that can program up to eight identical MSP430 or MSP432 flash or FRAM devices at the same time. The MSP Gang Programmer connects to a host PC using a standard RS-232 or USB connection and provides flexible programming options that let the user fully customize the process.


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## 7.4 Documentation Support

The following documents describe the MSP430F673x and MSP430F672x MCUs. Copies of these documents are available on the Internet at www.ti.com.

### Receiving Notification of Document Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com (for links to the product folders, see Section 7.5). In the upper right corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

### Errata

**MSP430F6736 Device Erratasheet** Describes the known exceptions to the functional specifications.

**MSP430F6735 Device Erratasheet** Describes the known exceptions to the functional specifications.

**MSP430F6734 Device Erratasheet** Describes the known exceptions to the functional specifications.

**MSP430F6733 Device Erratasheet** Describes the known exceptions to the functional specifications.

**MSP430F6731 Device Erratasheet** Describes the known exceptions to the functional specifications.

**MSP430F6730 Device Erratasheet** Describes the known exceptions to the functional specifications.

**MSP430F6726 Device Erratasheet** Describes the known exceptions to the functional specifications.

**MSP430F6725 Device Erratasheet** Describes the known exceptions to the functional specifications.

**MSP430F6724 Device Erratasheet** Describes the known exceptions to the functional specifications.

**MSP430F6723 Device Erratasheet** Describes the known exceptions to the functional specifications.

**MSP430F6721 Device Erratasheet** Describes the known exceptions to the functional specifications.

**MSP430F6720 Device Erratasheet** Describes the known exceptions to the functional specifications.

### User's Guides

**MSP430x5xx and MSP430x6xx Family User's Guide** Detailed information on the modules and peripherals available in this device family.

**MSP430 Flash Device Bootloader (BSL) User's Guide** The MSP430 bootloader (BSL) (formerly known as the bootstrap loader) lets users communicate with embedded memory in the MSP430 microcontroller during the prototyping phase, final production, and in service. Both the programmable memory (flash memory) and the data memory (RAM) can be modified as required. Do not confuse the bootloader with the bootstrap loader programs found in some digital signal processors (DSPs) that automatically load program code (and data) from external memory to the internal memory of the DSP.

**MSP430 Programming With the JTAG Interface** This document describes the functions that are required to erase, program, and verify the memory module of the MSP430 flash-based and FRAM-based microcontroller families using the JTAG communication port. In addition, it describes how to program the JTAG access security fuse that is available on all MSP430 devices. This document describes device access using both the standard 4-wire JTAG interface and the 2-wire JTAG interface, which is also referred to as Spy-Bi-Wire (SBW).

**MSP430 Hardware Tools User's Guide** This manual describes the hardware of the TI MSP-FET430 Flash Emulation Tool (FET). The FET is the program development tool for the MSP430 ultra-low-power microcontroller. Both available interface types, the parallel port interface and the USB interface, are described.

### Application Reports

**MSP430 32-kHz Crystal Oscillators** Selection of the correct crystal, correct load circuit, and proper board layout are important for a stable crystal oscillator. This application report summarizes crystal oscillator function and explains the parameters to select the correct crystal for MSP430 ultra-low-power operation. In addition, hints and examples for correct board layout are given. The document also contains detailed information on the possible oscillator tests to ensure stable oscillator operation in mass production.

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**MSP430 System-Level ESD Considerations** System-Level ESD has become increasingly demanding with silicon technology scaling towards lower voltages and the need for designing cost-effective and ultra-low-power components. This application report addresses three different ESD topics to help board designers and OEMs understand and design robust system-level designs.

**Designing With MSP430 and Segment LCDs** Segment liquid crystal displays (LCDs) are needed to provide information to users in a wide variety of applications from smart meters to electronic shelf labels (ESLs) to medical equipment. Several MSP430 microcontroller families include built-in low-power LCD driver circuitry that allows the MSP430 MCU to directly control the segmented LCD glass. This application note helps explain how segmented LCDs work, the different features of the various LCD modules across the MSP430 MCU family, LCD hardware layout tips, guidance on writing efficient and easy-to-use LCD driver software, and an overview of the portfolio of MSP430 devices that include different LCD features to aid in device selection.

## 7.5 Related Links

Table 7-2 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 7-2. Related Links**

| PARTS | PRODUCT FOLDER | ORDER NOW | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| MSP430F6736 | Click here | Click here | Click here | Click here | Click here |
| MSP430F6735 | Click here | Click here | Click here | Click here | Click here |
| MSP430F6734 | Click here | Click here | Click here | Click here | Click here |
| MSP430F6733 | Click here | Click here | Click here | Click here | Click here |
| MSP430F6731 | Click here | Click here | Click here | Click here | Click here |
| MSP430F6730 | Click here | Click here | Click here | Click here | Click here |
| MSP430F6726 | Click here | Click here | Click here | Click here | Click here |
| MSP430F6725 | Click here | Click here | Click here | Click here | Click here |
| MSP430F6724 | Click here | Click here | Click here | Click here | Click here |
| MSP430F6723 | Click here | Click here | Click here | Click here | Click here |
| MSP430F6721 | Click here | Click here | Click here | Click here | Click here |
| MSP430F6720 | Click here | Click here | Click here | Click here | Click here |

## 7.6 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Community

*TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

TI Embedded Processors Wiki

*Texas Instruments Embedded Processors Wiki*. Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

## 7.7 Trademarks

MSP430, MSP430Ware, EnergyTrace, ULP Advisor, Code Composer Studio, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.


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## 7.8 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 7.9 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

## 7.10 Glossary

**TI Glossary** This glossary lists and explains terms, acronyms, and definitions.

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# 8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MSP430F6720IPN | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6720 | Samples |
| MSP430F6720IPNR | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6720 | Samples |
| MSP430F6720IPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6720 | Samples |
| MSP430F6720IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6720 | Samples |
| MSP430F6721IPN | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6721 | Samples |
| MSP430F6721IPNR | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6721 | Samples |
| MSP430F6721IPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6721 | Samples |
| MSP430F6721IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6721 | Samples |
| MSP430F6723IPN | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6723 | Samples |
| MSP430F6723IPNR | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6723 | Samples |
| MSP430F6723IPNR-S | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6723 | Samples |
| MSP430F6723IPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6723 | Samples |
| MSP430F6723IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6723 | Samples |
| MSP430F6724IPN | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6724 | Samples |
| MSP430F6724IPNR | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6724 | Samples |
| MSP430F6724IPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6724 | Samples |
| MSP430F6724IPZR | ACTIVE | LQFP | PZ | 100 | | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6724 | Samples |
| MSP430F6725IPN | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6725 | Samples |
| MSP430F6725IPNR | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6725 | Samples |
| MSP430F6725IPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6725 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MSP430F6725IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6725 | Samples |
| MSP430F6726IPN | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6726 | Samples |
| MSP430F6726IPNR | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6726 | Samples |
| MSP430F6726IPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6726 | Samples |
| MSP430F6726IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6726 | Samples |
| MSP430F6730IPN | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6730 | Samples |
| MSP430F6730IPNR | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6730 | Samples |
| MSP430F6730IPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6730 | Samples |
| MSP430F6731IPN | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6731 | Samples |
| MSP430F6731IPNR | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6731 | Samples |
| MSP430F6731IPZ | OBSOLETE | LQFP | PZ | 100 | | TBD | Call TI | Call TI | | F6731 | |
| MSP430F6731IPZR | OBSOLETE | LQFP | PZ | 100 | | TBD | Call TI | Call TI | | F6731 | |
| MSP430F6733IPN | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6733 | Samples |
| MSP430F6733IPNR | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6733 | Samples |
| MSP430F6733IPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | | F6733 | Samples |
| MSP430F6733IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | | F6733 | Samples |
| MSP430F6734IPN | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6734 | Samples |
| MSP430F6734IPNR | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6734 | Samples |
| MSP430F6734IPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6734 | Samples |
| MSP430F6734IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6734 | Samples |
| MSP430F6735IPN | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6735 | Samples |
| MSP430F6735IPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6735 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MSP430F6736IPN | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6736 | Samples |
| MSP430F6736IPNR | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6736 | Samples |
| MSP430F6736IPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6736 | Samples |
| MSP430F6736IPZR | ACTIVE | LQFP | PZ | 100 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6736 | Samples |
| SN0806723IPNR | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6723 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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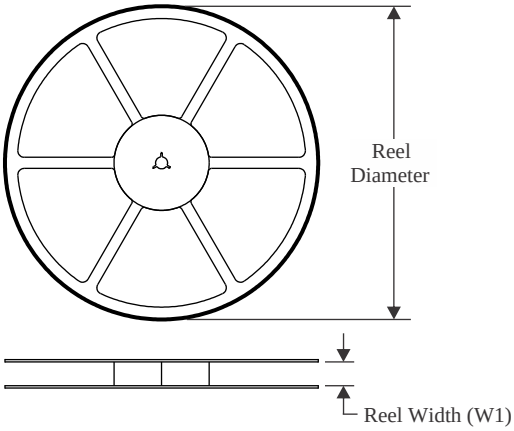
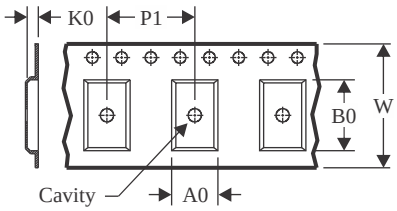
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

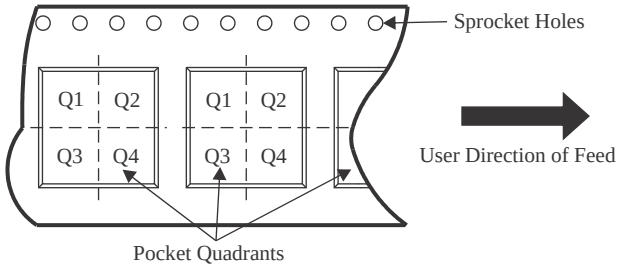



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

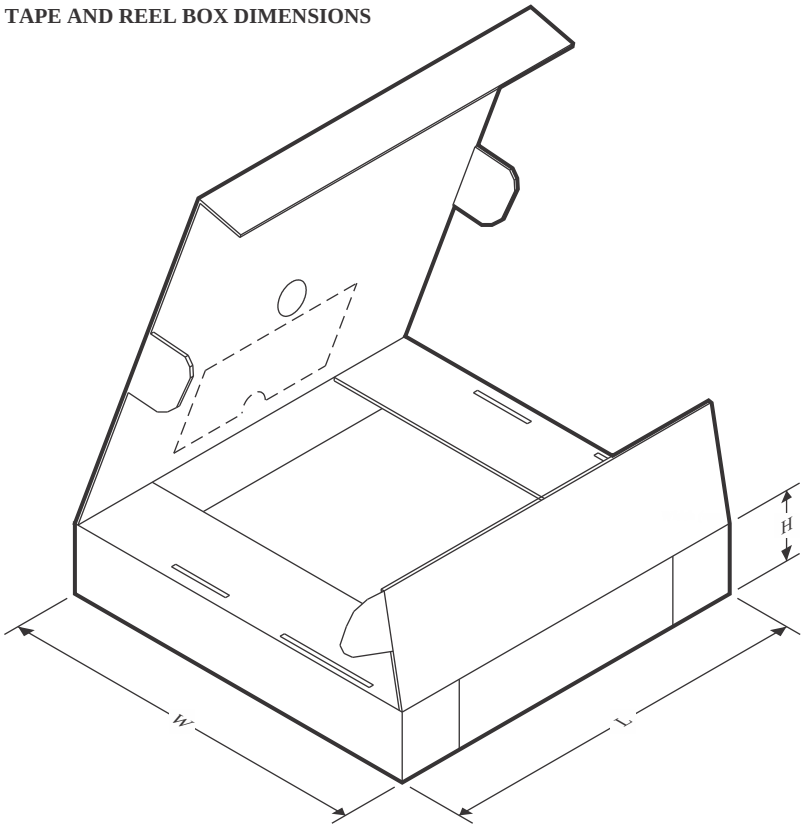



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MSP430F6720IPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6720IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6721IPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6721IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6723IPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6723IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6724IPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6725IPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6725IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6726IPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6726IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6730IPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6731IPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6733IPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6733IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6734IPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MSP430F6734IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6736IPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6736IPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS

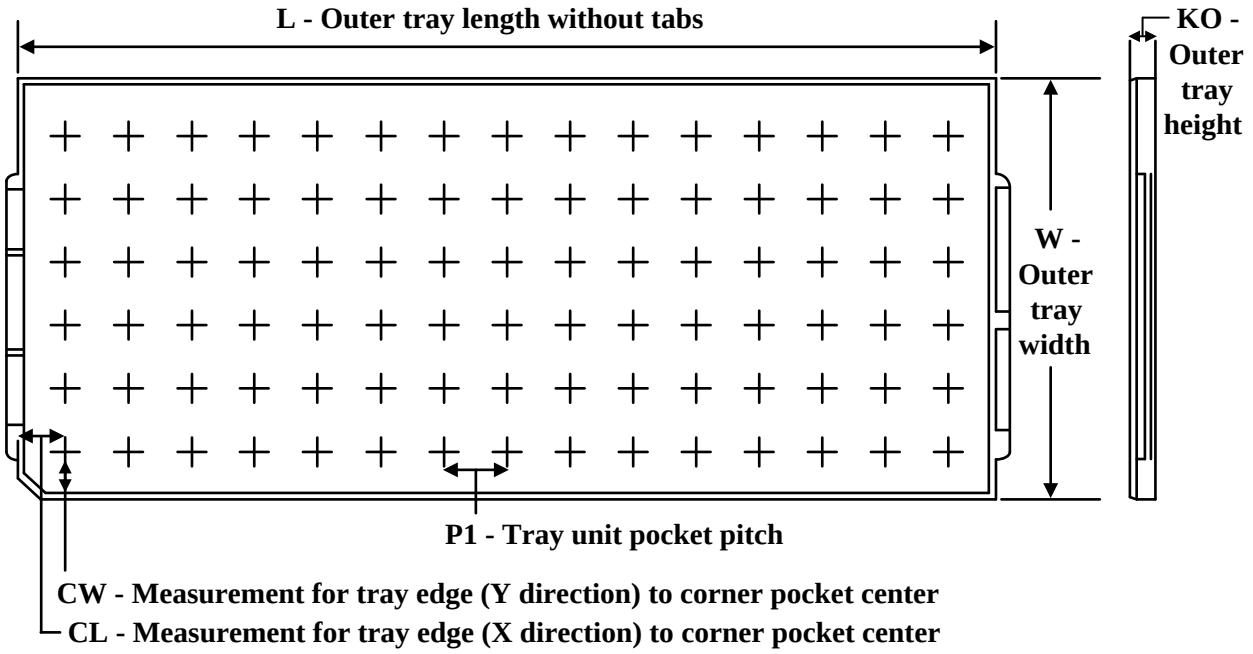



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| MSP430F6720IPNR | LQFP | PN | 80 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F6720IPZR | LQFP | PZ | 100 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F6721IPNR | LQFP | PN | 80 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F6721IPZR | LQFP | PZ | 100 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F6723IPNR | LQFP | PN | 80 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F6723IPZR | LQFP | PZ | 100 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F6724IPNR | LQFP | PN | 80 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F6725IPNR | LQFP | PN | 80 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F6725IPZR | LQFP | PZ | 100 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F6726IPNR | LQFP | PN | 80 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F6726IPZR | LQFP | PZ | 100 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F6730IPNR | LQFP | PN | 80 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F6731IPNR | LQFP | PN | 80 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F6733IPNR | LQFP | PN | 80 | 1000 | 367.0 | 367.0 | 45.0 |
| MSP430F6733IPZR | LQFP | PZ | 100 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F6734IPNR | LQFP | PN | 80 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F6734IPZR | LQFP | PZ | 100 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F6736IPNR | LQFP | PN | 80 | 1000 | 350.0 | 350.0 | 43.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| MSP430F6736IPZR | LQFP | PZ | 100 | 1000 | 350.0 | 350.0 | 43.0 |

## TRAY




Chamfer on Tray corner indicates Pin 1 orientation of packed units.

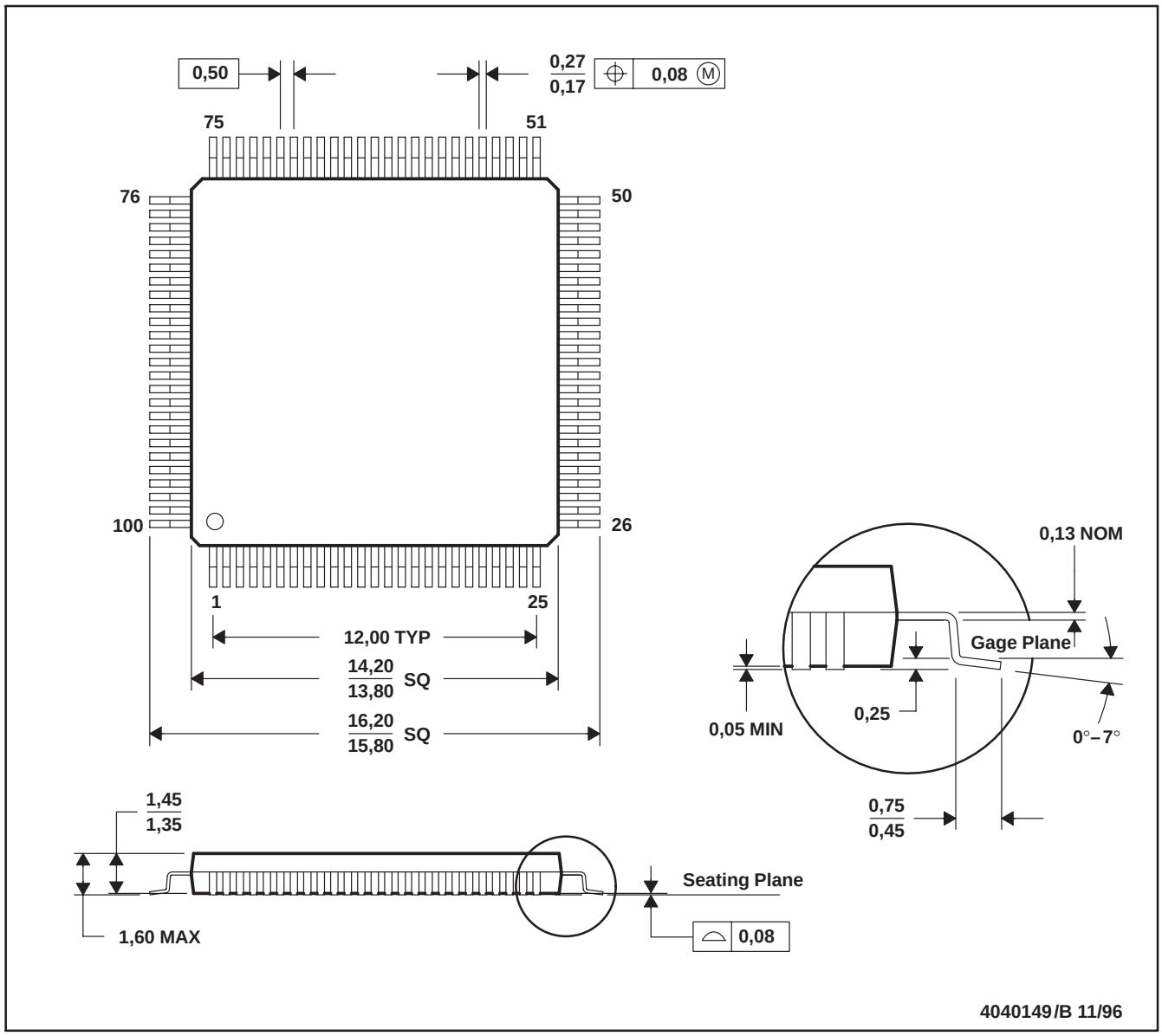
*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MSP430F6720IPN | PN | LQFP | 80 | 119 | 7 x 17 | 150 | 315 | 135.9 | 7620 | 17.9 | 14.3 | 13.95 |
| MSP430F6720IPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F6721IPN | PN | LQFP | 80 | 119 | 7 x 17 | 150 | 315 | 135.9 | 7620 | 17.9 | 14.3 | 13.95 |
| MSP430F6721IPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F6723IPN | PN | LQFP | 80 | 119 | 7 x 17 | 150 | 315 | 135.9 | 7620 | 17.9 | 14.3 | 13.95 |
| MSP430F6723IPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F6724IPN | PN | LQFP | 80 | 119 | 7 x 17 | 150 | 315 | 135.9 | 7620 | 17.9 | 14.3 | 13.95 |
| MSP430F6724IPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F6725IPN | PN | LQFP | 80 | 119 | 7 x 17 | 150 | 315 | 135.9 | 7620 | 17.9 | 14.3 | 13.95 |
| MSP430F6725IPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F6726IPN | PN | LQFP | 80 | 119 | 7 x 17 | 150 | 315 | 135.9 | 7620 | 17.9 | 14.3 | 13.95 |
| MSP430F6726IPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F6730IPN | PN | LQFP | 80 | 119 | 7 x 17 | 150 | 315 | 135.9 | 7620 | 17.9 | 14.3 | 13.95 |
| MSP430F6730IPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F6731IPN | PN | LQFP | 80 | 119 | 7 x 17 | 150 | 315 | 135.9 | 7620 | 17.9 | 14.3 | 13.95 |
| MSP430F6733IPN | PN | LQFP | 80 | 119 | 7 x 17 | 150 | 315 | 135.9 | 7620 | 17.9 | 14.3 | 13.95 |
| MSP430F6733IPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |

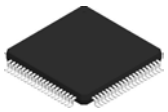
| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MSP430F6734IPN | PN | LQFP | 80 | 119 | 7 x 17 | 150 | 315 | 135.9 | 7620 | 17.9 | 14.3 | 13.95 |
| MSP430F6734IPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F6735IPN | PN | LQFP | 80 | 119 | 7 x 17 | 150 | 315 | 135.9 | 7620 | 17.9 | 14.3 | 13.95 |
| MSP430F6735IPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F6736IPN | PN | LQFP | 80 | 119 | 7 x 17 | 150 | 315 | 135.9 | 7620 | 17.9 | 14.3 | 13.95 |
| MSP430F6736IPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |

MTQF013A – OCTOBER 1994 – REVISED DECEMBER 1996

**PZ (S-PQFP-G100)** **PLASTIC QUAD FLATPACK**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

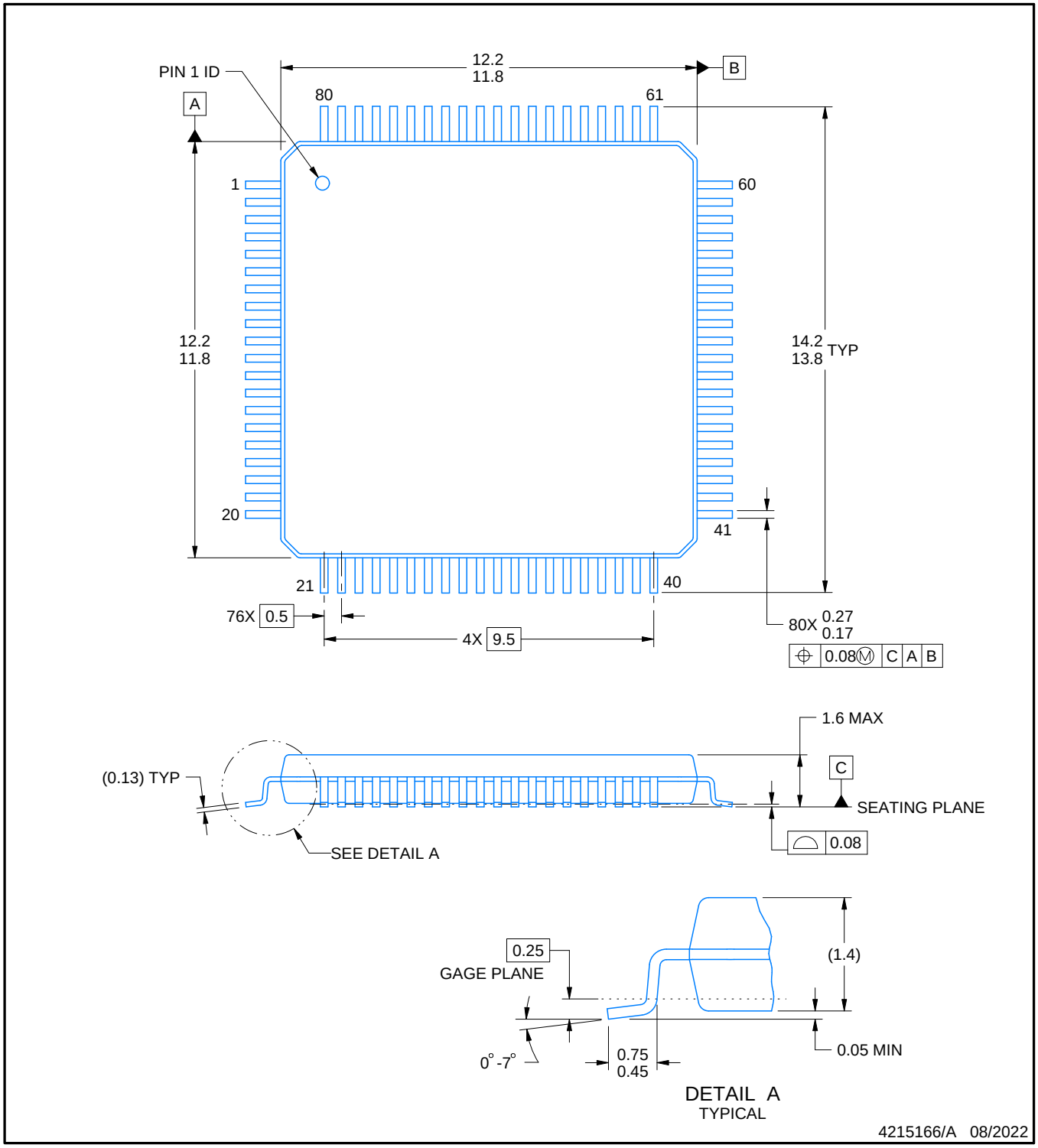


# PACKAGE OUTLINE

## PN0080A

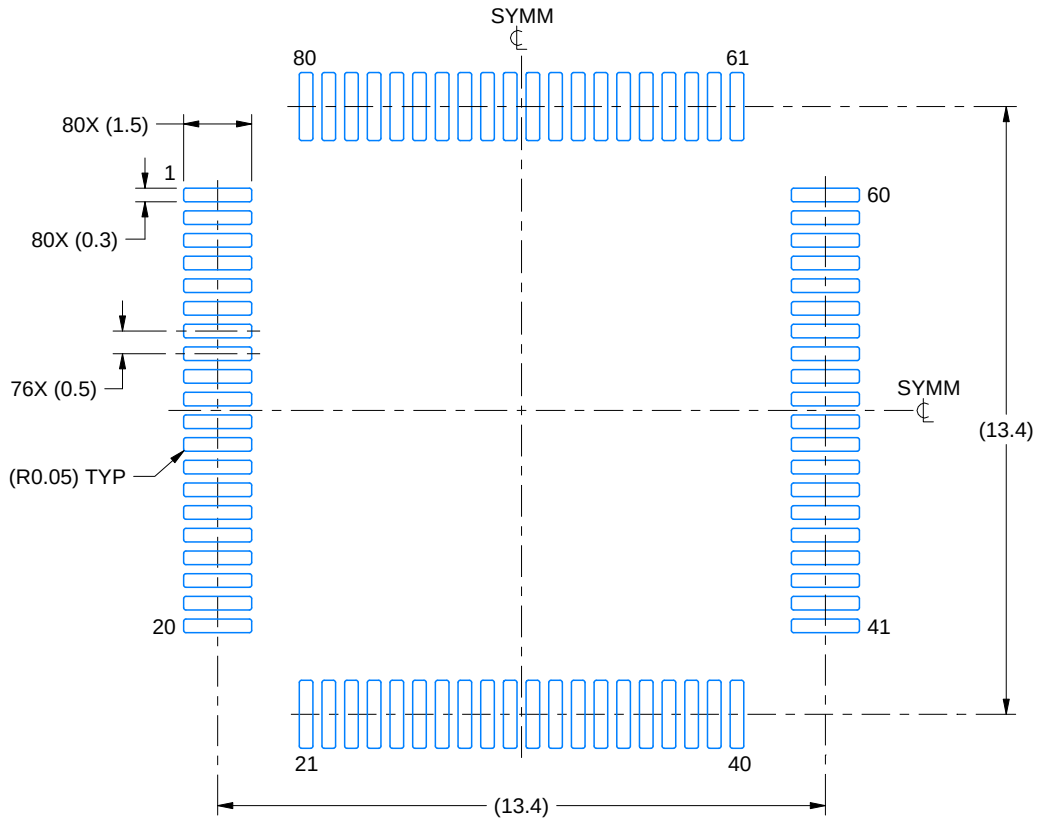
## LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK

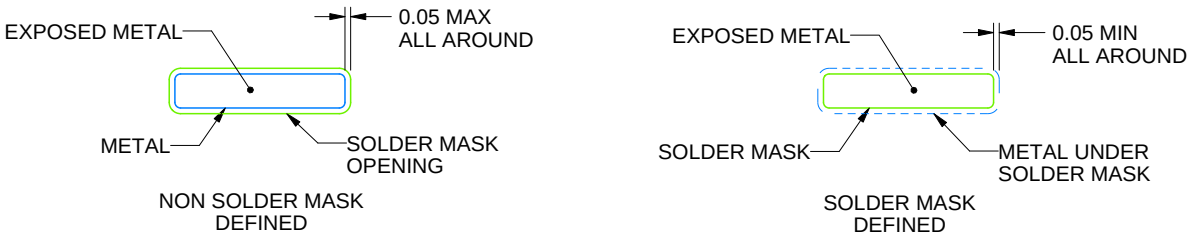



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

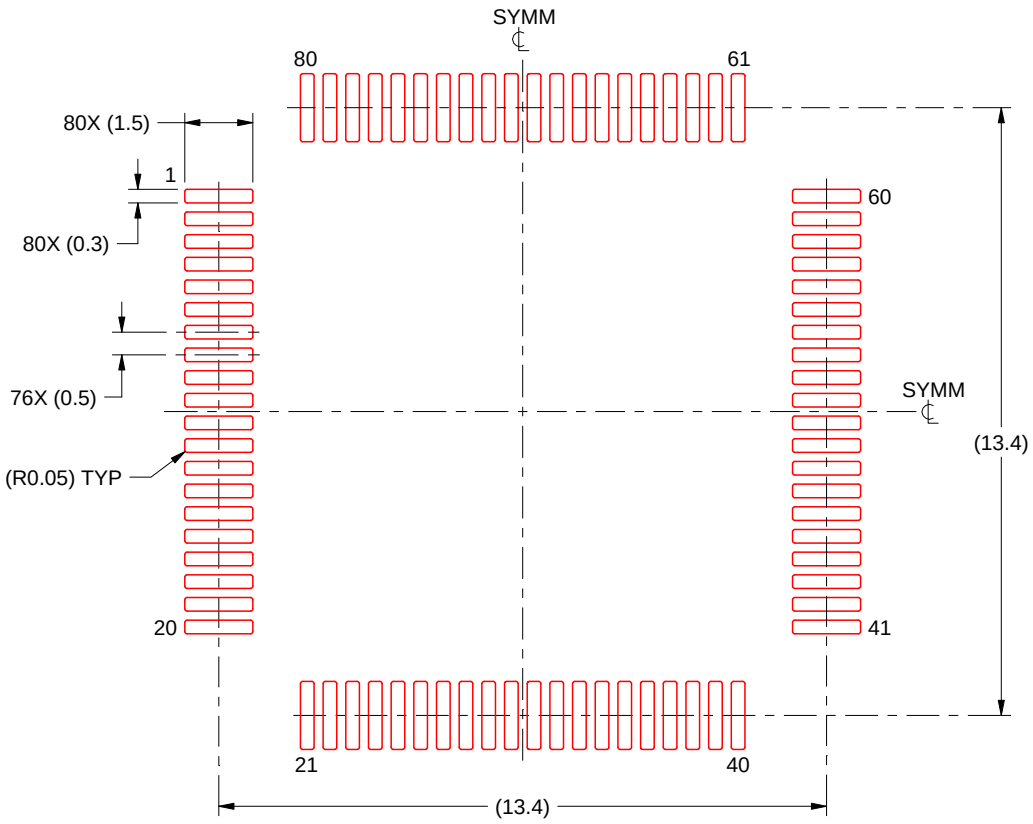



SOLDER MASK DETAILS

4215166/A 08/2022

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:6X

4215166/A 08/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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