THE DATASHEET OF

MPC8567EVTAQGG

Freescale Semiconductor
Technical Data

Document Number: MPC8568EEC
Rev. 1, 10/2010

MPC8568E/MPC8567E PowerQUICC III Integrated Processor Hardware Specifications

Due to feature similarities, this document covers both the MPC8568E and MPC8567E features. For simplicity, MPC8568 may only be mentioned throughout the document.

The MPC8567E feature differences are as follows:

- The MPC8567E PCI-Express supports x1/x2/x4, but does not have x8 support.
- Does not have eTSEC1, eTSEC2, or TLU

Note that both the MPC8568E and MPC8567E have their own pin assignment tables.

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1 MPC8568E Overview

This section provides a high-level overview of MPC8568E features. Figure 1 shows the major functional units within the MPC8568E.

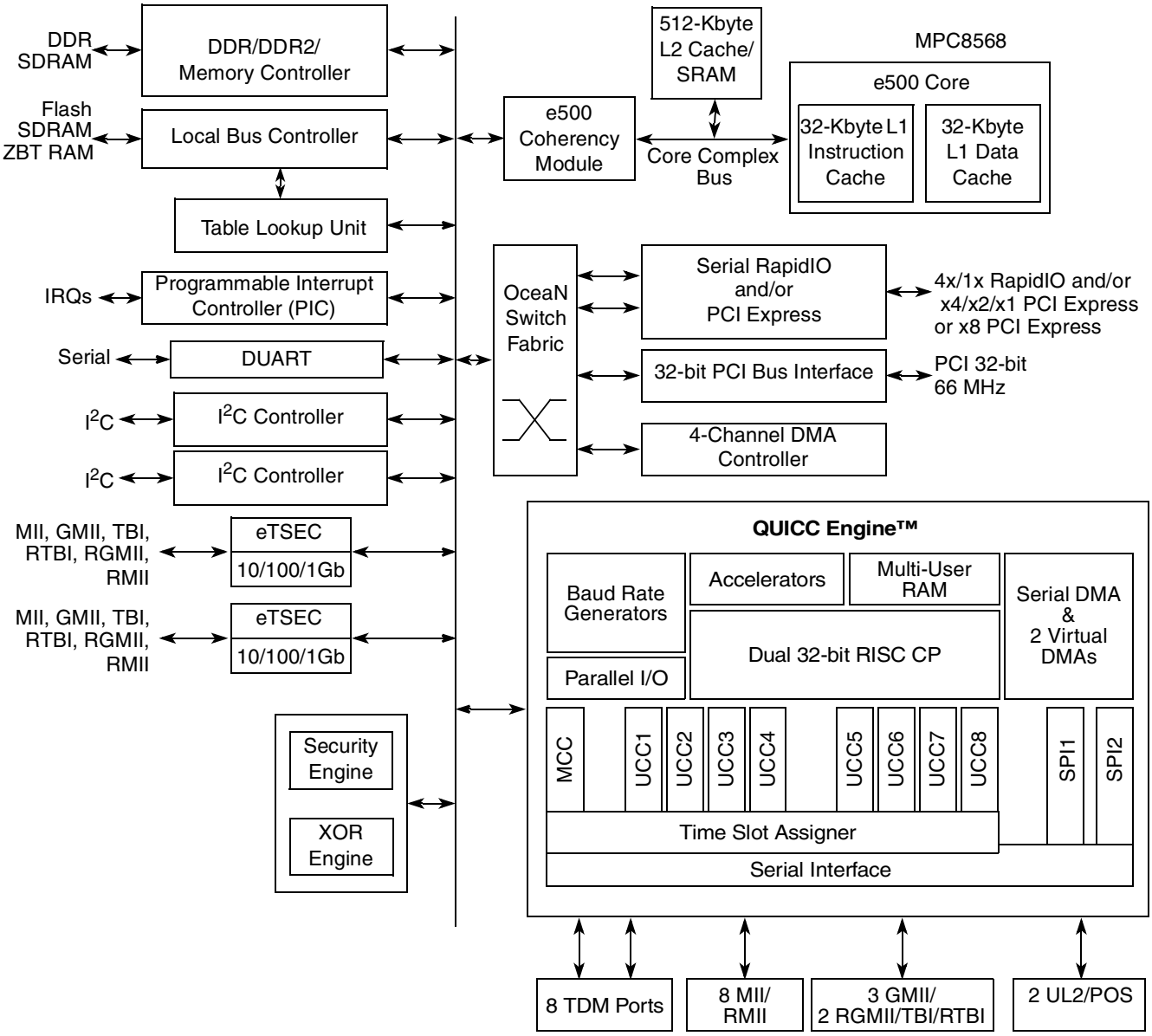


Figure 1. MPC8568E Block Diagram

1.1 MPCP8568E Key Features

- High-performance, Power Architecture® e500v2 core with 36-bit physical addressing
- 512 Kbytes of level-2 cache
- QUICC Engine (QE)
- Integrated security engine with XOR acceleration
- Two integrated 10/100/1Gb enhanced three-speed Ethernet controllers (eTSECs) with TCP/IP acceleration and classification capabilities
- DDR/DDR2 memory controller
- Table lookup unit (TLU) to access application-defined routing topology and control tables
- 32-bit PCI controller
- A 1x/4x Serial RapidIO® and/or x1/x2/x4 PCI Express interface. If x8 PCI Express is needed, then RapidIO is not available due to the limitation of the pin multiplexing.
- Programmable interrupt controller (PIC)
- Four-channel DMA controller, two I^2C controllers, DUART, and local bus controller (LBC)

NOTE

The MPC8568E and MPC8567E are also available without a security engine in a configuration known as the MPC8568 and MPC8567. All specifications other than those relating to security apply to the MPC8568 and MPC8567 exactly as described in this document.

1.2 MPC8568E Architecture Overview

1.2.1 e500 Core and Memory Unit

The MPC8568E contains a high-performance, 32-bit, Book E–enhanced e500v2 Power Architecture core. In addition to 36-bit physical addressing, this version of the e500 core includes the following:

- Double-precision floating-point APU—Provides an instruction set for double-precision (64-bit) floating-point instructions that use the 64-bit GPRs
- Embedded vector and scalar single-precision floating-point APUs—Provide an instruction set for single-precision (32-bit) floating-point instructions

The MPC8568E also contains 512 Kbytes of L2 cache/SRAM, as follows:

- Eight-way set-associative cache organization with 32-byte cache lines
- Flexible configuration (can be configured as part cache, part SRAM)
- External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
- SRAM features include the following:
  - I/O devices access SRAM regions by marking transactions as snoopable (global).
  - Regions can reside at any aligned location in the memory map.

— Byte-accessible ECC uses read-modify-write transaction accesses for smaller-than-cache-line accesses.

1.2.2 e500 Coherency Module (ECM) and Address Map

The e500 coherency module (ECM) provides a mechanism for I/O-initiated transactions to snoop the bus between the e500 core and the integrated L2 cache in order to maintain coherency across local cacheable memory. It also provides a flexible switch-type structure for core- and I/O-initiated transactions to be routed or dispatched to target modules on the device.

The MPC8568E supports a flexible 36-bit physical address map. Conceptually, the address map consists of local space and external address space. The local address map is supported by eight local access windows that define mapping within the local 36-bit (64-Gbyte) address space.

The MPC8568E can be made part of a larger system address space through the mapping of translation windows. This functionality is included in the address translation and mapping units (ATMUs). Both inbound and outbound translation windows are provided. The ATMUs allows the MPC8568E to be part of larger address maps such as the PCI or PCI Express 64-bit address environment and the RapidIO environment.

1.2.3 QUICC Engine

- Integrated 8-port L2 Ethernet switch
  - 8 connection ports of 10/100 Mbps MII/RMII & one CPU internal port
  - Each port supports four priority levels
  - Priority levels used with VLAN tags or IP TOS field to implement QoS
  - QoS types of traffic, such as voice, video, and data
- Includes support for the following protocols:
  - ATM SAR up to 622 Mbps (OC-12) full duplex, with ATM traffic shaping (ATF TM4.1) for up to 64K ATM connections
  - ATM AAL1 structured and unstructured Circuit Emulation Service (CES 2.0)
  - IMA and ATM Transmission convergence sub-layer
  - ATM OAM handling features compatible with ITU-T I.610
  - PPP, Multi-Link (ML-PPP), Multi-Class (MC-PPP) and PPP mux in accordance with the following RFCs: 1661, 1662, 1990, 2686 and 3153
  - IP termination support for IPv4 and IPv6 packets including TOS, TTL and header checksum processing
  - ATM (AAL2/AAL5) to Ethernet (IP) interworking
  - Extensive support for ATM statistics and Ethernet RMON/MIB statistics.
  - 256 channels of HDLC/Transparent or 128 channels of SS#7
- Includes support for the following serial interfaces:
  - Two UL2/POS-PHY interfaces with 124 Multi-PHY addresses on UTOPIA interface each or 31 Multi-PHY addresses on the POS interface each.

— Three 1-Gbps Ethernet interfaces using three GMII, two RGMII/TBI/RTBI
— Up to eight 10/100-Mbps Ethernet interfaces using MII or RMII
— Up to eight T1/E1/J1/E3 or DS-3 serial interfaces

1.2.4 Integrated Security Engine (SEC)

The SEC is a modular and scalable security core optimized to process all the algorithms associated with IPSec, IKE, WTLS/WAP, SSL/TLS, and 3GPP. Although it is not a protocol processor, the SEC is designed to perform multi-algorithmic operations (for example, 3DES-HMAC-SHA-1) in a single pass of the data. The version of the SEC used in the MPC8568E is specifically capable of performing single-pass security cryptographic processing for SSL 3.0, SSL 3.1/TLS 1.0, IPSec, SRTP, and 802.11i.

- Optimized to process all the algorithms associated with IPSec, IKE, WTLS/WAP, SSL/TLS, and 3GPP
- Compatible with code written for the Freescale MPC8541E and MPC8555E devices
- XOR engine for parity checking in RAID storage applications.
- Four crypto-channels, each supporting multi-command descriptor chains
- Cryptographic execution units:
  — PKEU—public key execution unit
  — DEU—Data Encryption Standard execution unit
  — AESU—Advanced Encryption Standard unit
  — AFEU—ARC four execution unit
  — MDEU—message digest execution unit
  — KEU—Kasumi execution unit
  — RNG—Random number generator

1.2.5 Enhanced Three-Speed Ethernet Controllers

The MPC8568E has two on-chip enhanced three-speed Ethernet controllers (eTSECs). The eTSECs incorporate a media access control (MAC) sublayer that supports 10- and 100-Mbps and 1-Gbps Ethernet/802.3 networks with MII, RMII, GMII, RGMII, TBI, and RTBI physical interfaces. The eTSECs include 2-Kbyte receive and 10-Kbyte transmit FIFOs and DMA functions.

The MPC8568E eTSECs support programmable CRC generation and checking, RMON statistics, and jumbo frames of up to 9.6 Kbytes. Frame headers and buffer descriptors can be forced into the L2 cache to speed classification or other frame processing. They are IEEE Std 802.3™, IEEE 802.3u, IEEE 802.3x, IEEE 802.3z, IEEE 802.3ac, IEEE 802.3ab-compatible.

The buffer descriptors are based on the MPC8260 and MPC860T 10/100 Ethernet programming models. Each eTSEC can emulate a PowerQUICC III TSEC, allowing existing driver software to be re-used with minimal change.

Some of the key features of these controllers include:

- Flexible configuration for multiple PHY interface configurations. Table 1 lists available configurations.

Table 1. Supported eTSEC1 and eTSEC2 Configurations[1]

Mode Option	eTSEC1	eTSEC2
Ethernet standard interfaces	TBI, GMII, or MII	TBI, GMII, or MII
Ethernet reduced interfaces	RTBI, RGMII, or RMII	RTBI, RGMII, or RMII
FIFO and mixed interfaces	8-bit FIFO	TBI, GMII, MII, RTBI, RGMII, RMII, or 8-bit FIFO
	TBI, GMII, MII, RTBI, RGMII, RMII, or 8-bit FIFO	8-bit FIFO
	16-bit FIFO	Not used/not available

1 Both interfaces must use the same voltage (2.5 or 3.3 V).

- TCP/IP acceleration and QoS features:
  - IP v4 and IP v6 header recognition on receive
  - IP v4 header checksum verification and generation
  - TCP and UDP checksum verification and generation
  - Per-packet configurable acceleration
  - Recognition of VLAN, stacked (queue in queue) VLAN, 802.2, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
  - Supported in all FIFO modes
  - Transmission from up to eight physical queues
  - Reception to up to eight physical queues
- Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex):
  - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
- IEEE Std 802.1™ virtual local area network (VLAN) tags and priority
- VLAN insertion and deletion
  - Per-frame VLAN control word or default VLAN for each eTSEC
  - Extracted VLAN control word passed to software separately
- Programmable Ethernet preamble insertion and extraction of up to 7 bytes
- MAC address recognition
- Ability to force allocation of header information and buffer descriptors into L2 cache

1.2.6 DDR SDRAM Controller

The MPC8568E supports DDR SDRAM and DDR2 SDRAM. The memory interface controls main memory accesses and provides for a maximum of 16 Gbytes of main memory.

The MPC8568E supports a variety of SDRAM configurations. SDRAM banks can be built using DIMMs or directly-attached memory devices. Sixteen multiplexed address signals provide for device densities of 64 Mbits, 128 Mbits, 256 Mbits, 512 Mbits, 1 Gbits, 2 Gbits and 4 Gbits. Four chip select signals support

up to four banks of memory. The MPC8568E supports bank sizes from 64 Mbytes to 4 Gbytes. Nine column address strobes (MDM[0:8]) are used to provide byte selection for memory bank writes.

The MPC8568E can be configured to retain the currently active SDRAM page for pipelined burst accesses. Page mode support of up to 16 simultaneously open pages (32 for DDR2) can dramatically reduce access latencies for page hits. Depending on the memory system design and timing parameters, using page mode can save 3 to 4 clock cycles from subsequent burst accesses that hit in an active page.

Using ECC, the MPC8568E detects and corrects all single-bit errors and detects all double-bit errors and all errors within a nibble.

The MPC8568E can invoke a level of system power management by asserting the MCKE SDRAM signal on-the-fly to put the memory into a low-power sleep mode.

1.2.7 Table Lookup Unit (TLU)

The table lookup unit (TLU) provides access to application-defined routing topology and control tables in external memory. It accesses an external memory array attached to the local bus controller (LBC). Communication between the CPU and the TLU occurs via messages passed through the TLU's memory-mapped configuration and status registers.

The TLU provides resources for efficient generation of table entry addresses in memory, hash generation of addresses, and binary table searching algorithms for both exact-match and longest-prefix-match strategies.It supports the following TLU complex table types:

- Hash-Trie-Key table for hash-based exact-match algorithms
- Chained-Hash table for partially indexed and hashed exact-match algorithms
- Longest-prefix-match algorithm
- Flat-Data table for retrieving search results and simple indexed algorithms

1.2.8 PCI Controller

The MPC8568E supports one 32-bit PCI controller, which supports speeds of up to 66 MHz. Other features include:

- Compatible with the *PCI Local Bus Specification, Revision 2.2*, supporting 32- and 64-bit addressing
- Can function as host or agent bridge interface
- As a master, supports read and write operations to PCI memory space, PCI I/O space, and PCI configuration space
- Can generate PCI special-cycle and interrupt-acknowledge commands. As a target, it supports read and write operations to system memory as well as configuration accesses.
- Supports PCI-to-memory and memory-to-PCI streaming, memory prefetching of PCI read accesses, and posting of processor-to-PCI and PCI-to-memory writes
- PCI 3.3-V compatible with selectable hardware-enforced coherency

1.2.9 High Speed I/O Interfaces

The MPC8568E supports two high-speed I/O interface standards: serial RapidIO and PCI Express. It can be configured as x1/x4 SRIO and 1x/2x/4x PCI Express simultaneously with the following limitation:

- Both SRIO and PCI-Express are limited to use the same clock and are limited to 2.5G.
- Spread spectrum clocking can not be used because SRIO doesn't support this (PCI-Express does support it).

If x8 PCI Express is needed, then SRIO is not available due to the pin multiplex limitation.

1.2.10 Serial RapidIO

The serial RapidIO interface is based on the *RapidIO Interconnect Specification, Revision 1.2*. RapidIO is a high-performance, point-to-point, low-pin-count, packet-switched system-level interconnect that can be used in a variety of applications as an open standard. The RapidIO architecture has a rich variety of features including high data bandwidth, low-latency capability, and support for high-performance I/O devices, as well as support for message-passing and software-managed programming models. Key features of the serial RapidIO interface unit include:

- Support for *RapidIO Interconnect Specification, Revision 1.2* (all transaction flows and priorities)
- Both 1x and 4x LP-serial link interfaces, with transmission rates of 1.25, 2.5, and 3.125 Gbaud (data rates of 1.0, 2.0, and 2.5 Gbps) per lane
- Auto detection of 1x or 4x mode operation during port initialization
- 34-bit addressing and up to 256-byte data payload
- Receiver-controlled flow control
- Support for RapidIO error injection

The RapidIO messaging unit supports two inbox/outbox mailboxes (queues) for data and one doorbell message structure. Both chaining and direct modes are provided for the outbox, and messages can hold up to 16 packets of 256 bytes, or a total of 4 Kbytes.

1.2.11 PCI Express Interface

The MPC8568E supports a PCI Express interface compatible with the *PCI Express Base Specification Revision 1.0a*. It is configurable at boot time to act as either root complex or endpoint.The physical layer of the PCI Express interface operates at a 2.5-Gbaud data rate per lane.

Other features of the PCI Express interface include:

- x8, x4, x2, and x1 link widths supported
- Selectable operation as root complex or endpoint
- Both 32- and 64-bit addressing and 256-byte maximum payload size
- Full 64-bit decode with 32-bit wide windows

1.2.12 Programmable Interrupt Controller (PIC)

The MPC8568E PIC implements the logic and programming structures of the OpenPIC architecture, providing for external interrupts (with fully nested interrupt delivery), message interrupts, internal-logic driven interrupts, and global high-resolution timers. Up to 16 programmable interrupt priority levels are supported.

The PIC can be bypassed to allow use of an external interrupt controller.

1.2.13 DMA Controller, I^2C, DUART, and Local Bus Controller

The MPC8568E provides an integrated four-channel DMA controller, which can transfer data between any of its I/O or memory ports or between two devices or locations on the same port. The DMA controller also:

- Allows chaining (both extended and direct) through local memory-mapped chain descriptors.
- Scattering, gathering, and misaligned transfers are supported. In addition, stride transfers and complex transaction chaining are supported.
- Local attributes such as snoop and L2 write stashing can be specified.

There are two I^2C controllers. These synchronous, multimaster buses can be connected to additional devices for expansion and system development.

The DUART supports full-duplex operation and is compatible with the PC16450 and PC16550 programming models. 16-byte FIFOs are supported for both the transmitter and the receiver.

The MPC8568E local bus controller (LBC) port allows connections with a wide variety of external memories, DSPs, and ASICs. Three separate state machines share the same external pins and can be programmed separately to access different types of devices. The general-purpose chip select machine (GPCM) controls accesses to asynchronous devices using a simple handshake protocol. The user programmable machine (UPM) can be programmed to interface to synchronous devices or custom ASIC interfaces. The SDRAM controller provides access to standard SDRAM. Each chip select can be configured so that the associated chip interface can be controlled by the GPCM, UPM, or SDRAM controller. All may exist in the same system. The local bus controller supports the following features:

- Multiplexed 32-bit address and data bus operating at up to 133 MHz
- Eight chip selects support eight external slaves
- Up to eight-beat burst transfers
- 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- Three protocol engines available on a per-chip-select basis
- Parity support
- Default boot ROM chip select with configurable bus width (8, 16, or 32 bits)
- Supports zero-bus-turnaround (ZBT) RAM

1.2.14 Power Management

In addition to low-voltage operation and dynamic power management, which automatically minimizes power consumption of blocks when they are idle, four power consumption modes are supported: full on, doze, nap, and sleep.

1.2.15 System Performance Monitor

The performance monitor facility supports eight 32-bit counters that can count up to 512 counter-specific events. It supports duration and quantity threshold counting and a burstiness feature that permits counting of burst events with a programmable time between bursts.

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8568E. This device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings [1]

Characteristic	Symbol	Max Value	Unit	Notes
Core supply voltage	V_{DD}	–0.3 to 1.21	V	—
PLL supply voltage	AV_{DD_PLAT}, AV_{DD_CORE}, AV_{DD_CE}, AV_{DD_PCI}, AV_{DD_LBIU}, AV_{DD_SRDS}	–0.3 to 1.21	V	—
Core power supply for SerDes transceiver	SCOREVDD	–0.3 to 1.21	V	—
Pad power supply for SerDes transceiver	XV_{DD}	–0.3 to 1.21	V	—
DDR and DDR2 DRAM I/O voltage	GV_{DD}	–0.3 to 2.75 –0.3 to 1.98	V	—
eTSEC1, eTSEC2 I/O Voltage	LV_{DD}	–0.3 to 3.63 –0.3 to 2.75	V	—
QE UCC1/UCC2 Ethernet Interface I/O Voltage	TV_{DD}	–0.3 to 3.63 –0.3 to 2.75	V	—
PCI, DUART, system control and power management, I^2C, and JTAG I/O voltage	OV_{DD}	–0.3 to 3.63	V	3
Local bus I/O voltage	BV_{DD}	–0.3 to 3.63 –0.3 to 2.75	V	3

Table 2. Absolute Maximum Ratings [1] (continued)

Characteristic		Symbol	Max Value	Unit	Notes
Input voltage	DDR/DDR2 DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	DDR/DDR2 DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	–0.3 to (LV_{DD} + 0.3) –0.3 to (TV_{DD} + 0.3)	V	4, 5
	Local bus signals	BV_{IN}	–0.3 to (BV_{DD} + 0.3)		—
	DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	5
	PCI	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	6
Storage temperature range		T_{STG}	–55 to 150	•C	—

Notes:
1. Functional and tested operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** L/TV_{IN} must not exceed L/TV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. $(M,L,O)V_{IN}$ and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
6. OV_{IN} on the PCI interface may overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 2.

2.1.2 Recommended Operating Conditions

Table 3 provides the recommended operating conditions for this device. Note that the values in Table 3 are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

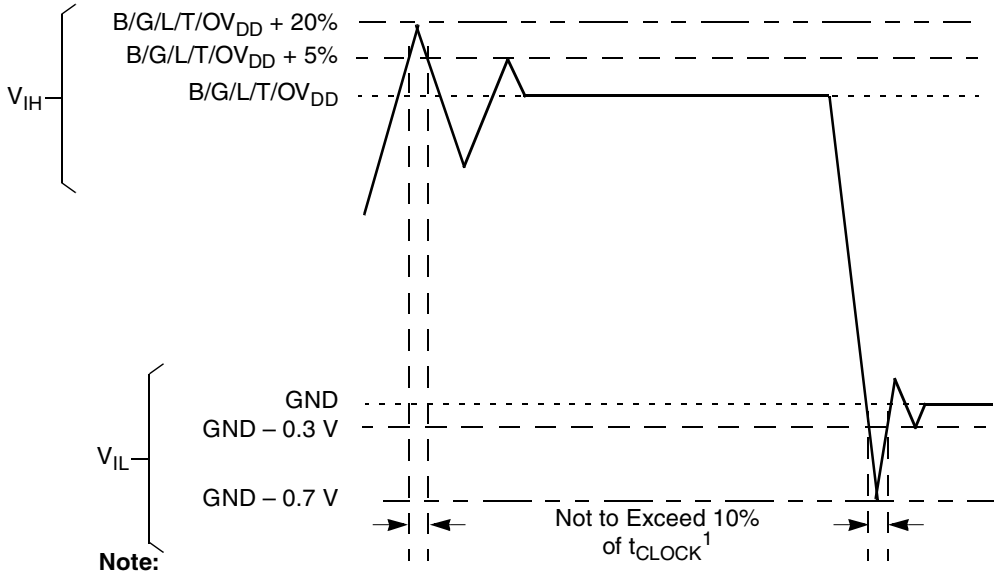
Table 3. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value	Unit	Notes
Core supply voltage	V_{DD}	1.1 V ± 55 mV	V	—
PLL supply voltage	AV_{DD_PLAT}, AV_{DD_CORE}, AV_{DD_CE}, AV_{DD_PCI}, AV_{DD_LBIU}, AV_{DD_SRDS}	1.1 V ± 55 mV	V	—
Core power supply for SerDes transceiver	SCOREVDD	1.1 V ± 55 mV	V	—
Pad power supply for SerDes transceiver	XV_{DD}	1.1 V ± 55 mV	V	—
DDR and DDR2 DRAM I/O voltage	GV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	—

Table 3. Recommended Operating Conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Notes
Three-speed Ethernet I/O voltage		LV_{DD} TV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV	V	—
PCI, DUART, system control and power management, I^2C, and JTAG I/O voltage		OV_{DD}	3.3 V ± 165 mV	V	—
Local bus I/O voltage		BV_{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV	V	—
Input voltage	DDR and DDR2 DRAM signals	MV_{IN}	GND to GV_{DD}	V	—
	DDR and DDR2 DRAM reference	MV_{REF}	GND to $GV_{DD}/2$	V	—
	Three-speed Ethernet signals	LV_{IN} TV_{IN}	GND to LV_{DD} GND to TV_{DD}	V	—
	Local bus signals	BV_{IN}	GND to BV_{DD}	V	—
	PCI, DUART, SYSCLK, system control and power management, I^2C, and JTAG signals	OV_{IN}	GND to OV_{DD}	V	—
Junction temperature range		Tj	0 to105	°C	—

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8568E.



Note:
1. Note that t_{CLOCK} refers to the clock period associated with the respective interface
   For I2C and JTAG, t_{CLOCK} references SYSCLK.
   For DDR, t_{CLOCK} references MCLK.
   For eTSEC, tCLOCK references EC_GTX_CLK125.
   For LBIU, t_{CLOCK} references LCLK.
   For PCI, t_{CLOCK} references PCI_CLK or SYSCLK.
   For SerDes, t_{CLOCK} references SD_REF_CLK.
2. Note that with the PCI overshoot allowed (as specified above), the device does not fully comply with the maximum AC ratings and device protection guideline outlined in the PCI rev. 2.2 standard (section 4.2.2.3)

Figure 2. Overshoot/Undershoot Voltage for $BV_{DD}/GV_{DD}/LV_{DD}/TV_{DD}/OV_{DD}$

The core voltage must always be provided at nominal 1.1V. (See Table 3 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses a single-ended differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL2 electrical signaling standard.

2.1.3 Output Driver Characteristics

Table 4 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 4. Output Drive Capability

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Local bus interface utilities signals	25 25	BV_{DD} = 3.3 V BV_{DD} = 2.5 V	1
	45(default) 45(default)	BV_{DD} = 3.3 V BV_{DD} = 2.5 V	
PCI signals	25	OV_{DD} = 3.3 V	2
	42 (default)		
DDR signal	20	GV_{DD} = 2.5 V	—
DDR2 signal	16 32 (half strength mode)	GV_{DD} = 1.8 V	—
eTSEC 10/100/1000 signals	42	L/TV_{DD} = 2.5/3.3 V	—
DUART, system control, JTAG	42	OV_{DD} = 3.3 V	—
I2C	150	OV_{DD} = 3.3 V	—

Notes:
1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSCR.
2. The drive strength of the PCI interface is determined by the setting of the $\overline{\text{PCI\_GNT}}[1]$ signal at reset.

2.2 Power Sequencing

The MPC8568E requires its power rails to be applied in specific sequence in order to ensure proper device operation. These requirements are as follows for power up:

1. V_{DD}, AV_{DD}_n, BV_{DD}, $SCOREV_{DD}$, LV_{DD}, TV_{DD}, XV_{DD}, OV_{DD}
2. GV_{DD}

All supplies must be at their stable values within 50 ms.

NOTE

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

In order to guarantee MCKE low during power-up, the above sequencing for GVDD is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-up, then the sequencing for GVDD is not required.

3 Power Characteristics

The power dissipation of V_{DD} for various core complex bus (CCB) versus the core and QE frequency for MPC8568E is shown in Table 5. Note that this is based on the design estimate only. More accurate power number will be available after we have done the measurement on the silicon.

Table 5. MPC8568E Power Dissipation

CCB Frequency	Core Frequency	QE Frequency	Typical 65°C	Typical 105°C	Maximum	Unit
400	800	400	8.7	12.0	13.0	W
400	1000	400	8.9	12.3	13.6	W
400	1200	400	11.3	15.7	16.9	W
533	1333	533	12.4	17.2	18.7	W

Notes:
1. CCB Frequency is the SoC platform frequency which corresponds to DDR data rate.
2. Typical 65 °C based on V_{DD}=1.1V, Tj=65.
3. Typical 105 °C based on V_{DD}=1.1V, Tj=105.
4. Maximum based on V_{DD}=1.1V, Tj=105.

Table 6. Typical MPC8568E I/O Power Dissipation

Interface	Parameters	GV_{DD}		BV_{DD}		OV_{DD}	LV_{DD}		TV_{DD}		XV_{DD}	Unit	Comment
		2.5 V	1.8 V	3.3 V	2.5 V		3.3 V	2.5 V	3.3 V	2.5 V			
DDR/DDR2	333 MHz	0.76	0.50									W	Data rate 64-bit with ECC 60% utilization
	400 MHz		0.56									W	
	533 MHz		0.68									W	
Local Bus	33 MHz, 32b			0.07	0.04							W	—
	66 MHz, 32b			0.13	0.07							W	—
	133 MHz, 32b			0.24	0.14							W	—
PCI	33 MHz					0.04						W	—
	66 MHz					0.07						W	—
SRIO	4x, 3.125G										0.49	W	—
PCI Express	8x, 2.5G										0.71	W	—

Table 6. Typical MPC8568E I/O Power Dissipation (continued)

Interface	Parameters	GV_{DD}		BV_{DD}		OV_{DD}	LV_{DD}		TV_{DD}		XV_{DD}	Unit	Comment
		2.5 V	1.8 V	3.3 V	2.5 V		3.3 V	2.5 V	3.3 V	2.5 V			
eTSEC Ethernet	MII						0.01					W	Multiply with number of the interfaces
	GMII/TBI						0.07					W	
	RGMII/RTBI							0.04				W	
eTSEC FIFO I/O	16b, 200 MHz						0.20					W	Multiply with number of the interfaces
	16b, 155 MHz						0.16					W	
	8b, 200 MHz						0.11					W	
	8b, 155 MHz						0.08					W	
QE UCC	MII/RMII								0.01			W	Multiply with number of the interfaces If UCC is programmed for other protocols, scale Ethernet power dissipation to the number of signals and the clock rate
	GMII/TBI								0.07			W	
	RGMII/RTBI									0.04		W	

Note: This is the power for each individual interface. The power must be calculated for each interface being utilized.

4 Input Clocks

4.1 System Clock Timing

Table 7 provides the system clock (SYSCLK) AC timing specifications for the MPC8568E.

Table 7. SYSCLK AC Timing Specifications

At recommended operating conditions (see Table 3) with OV_{DD} = 3.3 V ± 165 mV.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	—	—	166	MHz	1
SYSCLK cycle time	t_{SYSCLK}	6.0	—	—	ns	—
SYSCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.3	ns	2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	3

Table 7. SYSCLK AC Timing Specifications (continued)

At recommended operating conditions (see Table 3) with OV_{DD} = 3.3 V ± 165 mV.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK jitter	—	—	—	+/– 150	ps	4, 5

Notes:
1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 core frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 23.2, "CCB/SYSCLK PLL Ratio and Section 23.3, "e500 Core PLL Ratio," for ratio settings.
2. Rise and fall times for SYSCLK are measured at 0.4 V and 2.7 V.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The SYSCLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.

4.2 PCI Clock Timing

Table 8 provides the PCI clock (PCI_CLK) AC timing specifications for the MPC8568E.

Table 8. PCI_CLK AC Timing Specifications

At recommended operating conditions (see Table 3) with OV_{DD} = 3.3 V ± 165 mV.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
PCI_CLK frequency	f_{PCI_CLK}	—	—	66.7	MHz	—
PCI_CLK cycle time	t_{PCI_CLK}	15	—	—	ns	—
PCI_CLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.3	ns	1
PCI_CLK duty cycle	t_{KHK}/t_{PCI_CLK}	40	—	60	%	2
PCI_CLK jitter	—	—	—	+/– 150	ps	3,4

Notes:
1. Rise and fall times for PCI_CLK are measured at 0.4 V and 2.7 V.
2. Timing is guaranteed by design and characterization.
3. This represents the total input jitter—short term and long term—and is guaranteed by design.
4. The SYSCLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.

4.3 Real Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the Time Base unit of the e500. There is no need for jitter specification. The minimum pulse width of the RTC signal should be greater than 2x the period of the CCB clock. That is, minimum clock high time is $2 \times t_{CCB}$, and minimum clock low time is $2 \times t_{CCB}$. There is no minimum RTC frequency. RTC may be grounded if not needed.

4.4 eTSEC Gigabit Reference Clock Timing

Table 9 provides the eTSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications for the MPC8568E.

Table 9. EC_GTX_CLK125 AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 frequency	f_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK125 rise and fall time L/TVDD = 2.5 V L/TVDD = 3.3 V	t_{G125R}, t_{G125F}	 — —	 — —	 0.75 1.0	ns	—
EC_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	 45 47	—	 55 53	%	1, 2

Notes:
1. Timing is guaranteed by design and characterization.
2. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 8.2.6, "RGMII and RTBI AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.
3. Rise and fall times for EC_GTX_CLK125 are measured from 0.5 and 2.0 V for L/TVDD = 2.5 V, and from 0.6 and 2.7 V for L/TVDD = 3.3 V.

4.5 FIFO Clock Speed Restrictions

Note the following FIFO maximum speed restrictions based on the platform speed.

For FIFO GMII mode:

FIFO TX/RX clock frequency <= platform clock frequency / 4.2

For example, if the platform frequency is 533 MHz, the FIFO TX/RX clock frequency should be no higher than 127 MHz.

For FIFO encoded mode:

FIFO TX/RX clock frequency <= platform clock frequency / 3.2

For example, if the platform frequency is 533 MHz, the FIFO TX/RX clock frequency should be no higher than 167 MHz

4.6 Other Input Clocks

For information on the input clocks of other functional blocks of the platform such as SerDes, and eTSEC, see the specific section of this document.

5 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the MPC8568E. Table 10 provides the RESET initialization AC timing specifications for the DDR SDRAM component(s).

Table 10. RESET Initialization Timing Specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$	100	—	µs	—
Minimum assertion time for $\overline{\text{SRESET}}$	3	—	SYSCLKs	1
PLL input setup time with stable SYSCLK before $\overline{\text{HRESET}}$ negation	100	—	µs	—
Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$	4	—	SYSCLKs	1
Input hold time for all POR configs (including PLL config) with respect to negation of $\overline{\text{HRESET}}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{HRESET}}$	—	5	SYSCLKs	1

Notes:
1. SYSCLK is the primary clock input for the MPC8568E.

Table 11 provides the PLL lock times.

Table 11. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
Platform PLL lock times	—	100	µs	—
QE PLL lock times	—	100	µs	—
CPU PLL lock times	—	100	µs	—
PCI PLL lock times	—	100	µs	—
Local bus PLL	—	100	µs	—

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8568E. Note that DDR SDRAM is GV_{DD}(typ) = 2.5 V and DDR2 SDRAM is GV_{DD}(typ) = 1.8 V.

6.1 DDR SDRAM DC Electrical Characteristics

Table 12 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8568E when GV_{DD}(typ) = 1.8 V.

Table 12. DDR2 SDRAM DC Electrical Characteristics for GV_{DD}(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	1.7	1.9	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF}+ 0.125	GV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.125	V	—
Output leakage current	I_{OZ}	–10	10	µA	4
Output high current (V_{OUT} = 1.420 V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

Table 13 provides the DDR capacitance when GV_{DD}(typ) = 1.8 V.

Table 13. DDR2 SDRAM Capacitance for GV_{DD}(typ)=1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.2 V.

Table 14 provides the recommended operating conditions for the DDR SDRAM component(s) when GV_{DD}(typ) = 2.5 V.

Table 14. DDR SDRAM DC Electrical Characteristics for GV_{DD} (typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV_{DD}	2.3	2.7	V	1
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2
I/O termination voltage	V_{TT}	MV_{REF} – 0.04	MV_{REF} + 0.04	V	3
Input high voltage	V_{IH}	MV_{REF} + 0.15	GV_{DD} + 0.3	V	—

Table 14. DDR SDRAM DC Electrical Characteristics for GV_{DD} (typ) = 2.5 V (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input low voltage	V_{IL}	–0.3	MV_{REF}– 0.15	V	—
Output leakage current	I_{OZ}	–10	10	μA	4
Output high current (V_{OUT} = 1.95 V)	I_{OH}	–16.2	—	mA	—
Output low current (V_{OUT} = 0.35 V)	I_{OL}	16.2	—	mA	—

Notes:
1. GV_{DD} is expected to be within 50 mV of the DRAM GV_{DD} at all times.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD}, and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF}. This rail should track variations in the DC level of MV_{REF}.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

Table 15 provides the DDR capacitance when GV_{DD} (typ)=2.5 V.

Table 15. DDR SDRAM Capacitance for GV_{DD} (typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GV_{DD} = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GVDD/2, V_{OUT} (peak-to-peak) = 0.2 V.

Table 16 provides the current draw characteristics for MV_{REF}.

Table 16. Current Draw Characteristics for MV_{REF}

Parameter / Condition	Symbol	Min	Max	Unit	Note
Current draw for MV_{REF}	I_{MVREF}	—	500	μA	1

1. The voltage regulator for MV_{REF} must be able to supply up to 500 μA current.

6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

6.2.1 DDR SDRAM Input AC Timing Specifications

Table 17 provides the input AC timing specifications for the DDR2 SDRAM when $GV_{DD}(typ)$=1.8 V.

Table 17. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.25	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.25	—	V	—

Table 18 provides the input AC timing specifications for the DDR SDRAM when $GV_{DD}(typ)$=2.5 V.

Table 18. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.31	—	V	—

Table 19 provides the input AC timing specifications for the DDR SDRAM interface.

Table 19. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC/MDM	t_{CISKEW}			ps	1, 2
533 MHz		–300	300		3
400 MHz		–365	365		—
333 MHz		–390	390		—

Note:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}.This can be determined by the following equation: t_{DISKEW} =+/-(T/4 – abs(t_{CISKEW})) where T is the clock period and abs(t_{CISKEW}) is the absolute value of t_{CISKEW}.
3. Maximum DDR1 frequency is 400 MHz.

Figure 3 provides the input timing diagram for the DDR SDRAM interface. t_{DISKEW} can be calculated from t_{CISKEW}. See Table 19 footnote 2.

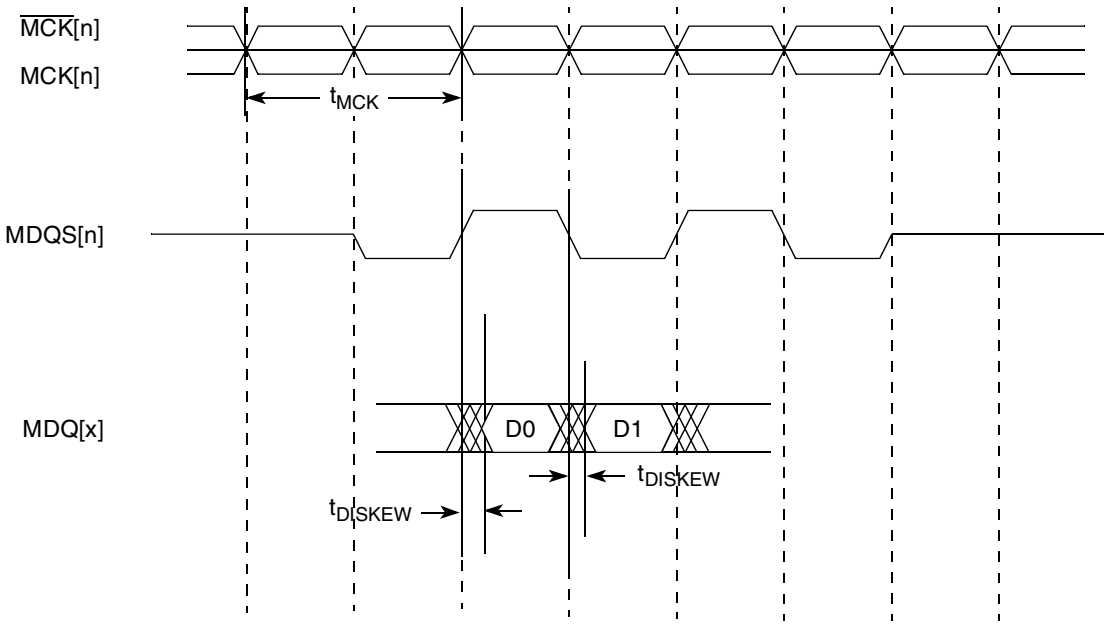


Figure 3. DDR SDRAM Input Timing Diagram

6.2.2 DDR SDRAM Output AC Timing Specifications

Table 20. DDR SDRAM Output AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol [1]	Min	Max	Unit	Notes
MCK[n] cycle time, MCK[n]/$\overline{\text{MCK}}$[n] crossing	t_{MCK}	3.75	10	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		
333 MHz		2.40	—		
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		
333 MHz		2.40	—		
$\overline{\text{MCS}}$[n] output setup with respect to MCK	t_{DDKHCS}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		
333 MHz		2.40	—		

Table 20. DDR SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions.

Parameter	Symbol [1]	Min	Max	Unit	Notes
$\overline{\text{MCS}}$[n] output hold with respect to MCK	t_{DDKHCX}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		
333 MHz		2.40	—		
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}			ps	5
533 MHz		538	—		7
400 MHz		700	—		
333 MHz		900	—		
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}			ps	5
533 MHz		538	—		7
400 MHz		700	—		
333 MHz		900	—		
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6
MDQS epilogue end	t_{DDKHME}	–0.6	0.6	ns	6

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8568E Integrated Communications Processor Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
7. Maximum DDR1 frequency is 400 MHz

NOTE

For the ADDR/CMD setup and hold specifications in Table 20, it is assumed that the Clock Control register is set to adjust the memory clocks by 1/2 applied cycle.

Figure 4 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (tDDKHMH).

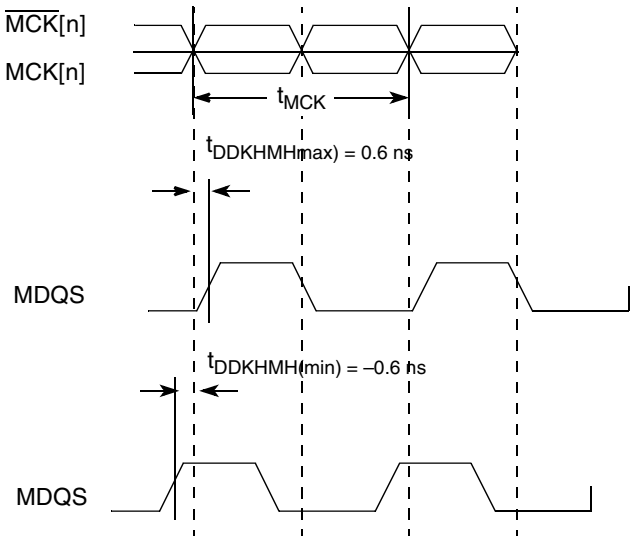


Figure 4. Timing Diagram for tDDKHMH

Figure 5 shows the DDR SDRAM output timing diagram.

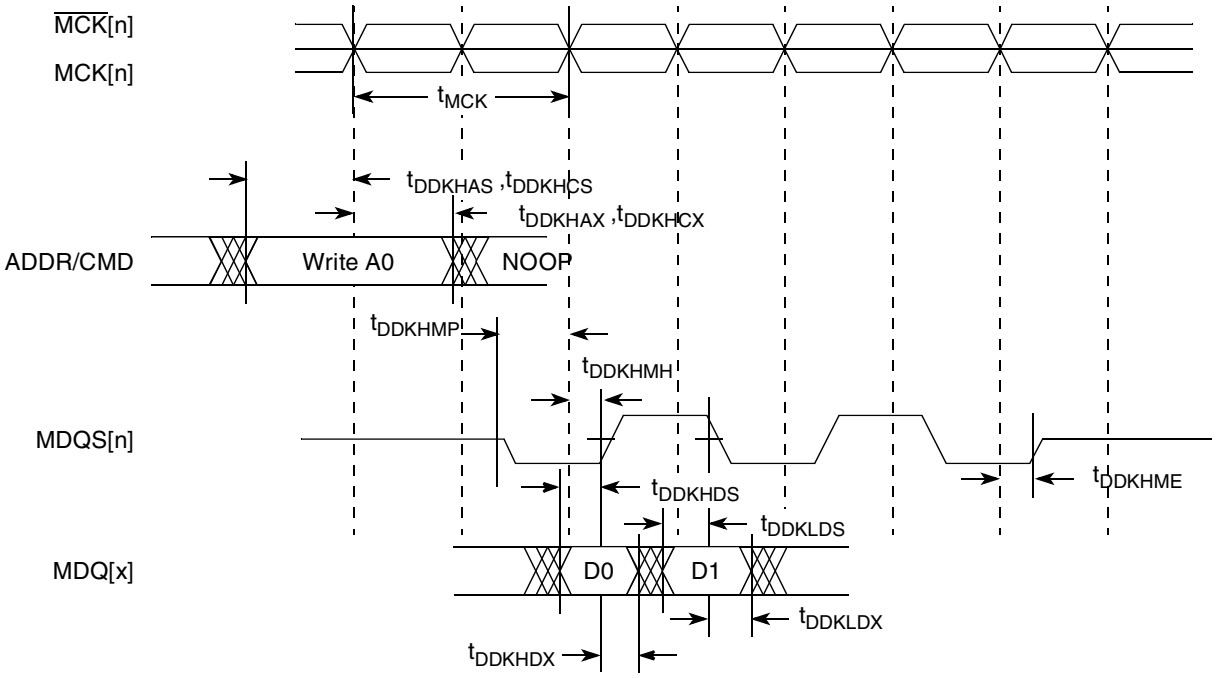


Figure 5. DDR SDRAM Output Timing Diagram

Figure 6 provides the AC test load for the DDR bus.

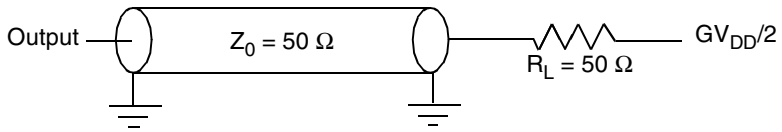


Figure 6. DDR AC Test Load

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8568E.

7.1 DUART DC Electrical Characteristics

Table 21 provides the DC electrical characteristics for the DUART interface.

Table 21. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	– 0.3	0.8	V

Table 21. DUART DC Electrical Characteristics (continued)

Parameter	Symbol	Min	Max	Unit
Input current (V_{IN} [1] = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±10	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –100 μA)	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage (OV_{DD} = min, I_{OL} = 100 μA)	V_{OL}	—	0.2	V

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2 and Table 3.

7.2 DUART AC Electrical Specifications

Table 22 provides the AC timing parameters for the DUART interface.

Table 22. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	CCB clock/1,048,576	baud	1,2
Maximum baud rate	CCB clock/16	baud	1,3
Oversample rate	16	—	1,4

Notes:
1. Guaranteed by design
2. CCB clock refers to the platform clock.
3. Actual attainable baud rate will be limited by the latency of interrupt processing.
4. The middle of a start bit is detected as the 8^{th} sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16^{th} sample.

8 Ethernet Interface and MII Management

This section provides the AC and DC electrical characteristics for eTSEC, MII management and Ethernet interface inside QUICC Engine. Note that eTSEC and QE Ethernet have the same DC/AC characteristics.

8.1 GMII/MII/TBI/RGMII/RTBI/RMII Electrical Characteristics

The electrical characteristics specified here apply to all gigabit media independent interface (GMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC). The RGMII and RTBI interfaces are defined for 2.5 V, while the GMII and TBI interfaces can be operated at 3.3 or 2.5 V. Whether the GMII, MII, or TBI interface is operated at 3.3 or 2.5 V, the timing is compatible with the IEEE 802.3 standard. The RGMII and RTBI interfaces follow the Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3 (12/10/2000). The RMII interface follows the RMII Consortium RMII

Specification Version 1.2 (3/20/1998). The electrical characteristics for MDIO and MDC are specified in Section 8, “Ethernet Interface and MII Management.”

8.1.1 Ethernet Interface DC Electrical Characteristics

All GMII, MII, TBI, RGMII, RMII and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 23 and Table 24. The potential applied to the input of a GMII, MII, TBI, RGMII, RMII or RTBI receiver may exceed the potential of the receiver’s power supply (that is, a GMII driver powered from a 3.6-V supply driving V_{OH} into a GMII receiver powered from a 2.5-V supply). Tolerance for dissimilar GMII driver and receiver supply potentials is implicit in these specifications. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 23. GMII, MII, RMII, and TBI DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage 3.3 V	LV_{DD} TV_{DD}	3.135	3.465	V	1, 2
Output high voltage (LV_{DD}/TV_{DD} = Min, IOH = –4.0 mA)	VOH	2.40	LV_{DD}/TV_{DD} + 0.3	V	—
Output low voltage (LV_{DD}/TV_{DD} = Min, IOL = 4.0 mA)	VOL	GND	0.50	V	—
Input high voltage	V_{IH}	2.0	LV_{DD}/TV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.90	V	—

Table 23. GMII, MII, RMII, and TBI DC Electrical Characteristics (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Input high current (V_{IN} = LV_{DD}, V_{IN} = TV_{DD})	I_{IH}	—	40	µA	1, 2, 3
Input low current (V_{IN} = GND)	I_{IL}	–600	—	µA	3

Notes:
1. LV_{DD} supports eTSECs 1 and 2.
2. TV_{DD} supports QE UCC1 and UCC2 ethernet ports.
3. The symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 2 and Table 3.

Table 24. GMII, MII, RMII, RGMII, RTBI, TBI and FIFO DC Electrical Characteristics

Parameters	Symbol	Min	Max	Unit	Notes
Supply voltage 2.5 V	LV_{DD}/TV_{DD}	2.37	2.63	V	1, 2
Output high voltage (LV_{DD}/TV_{DD} = Min, IOH = –1.0 mA)	V_{OH}	2.00	LV_{DD}/TV_{DD} + 0.3	V	—
Output low voltage (LV_{DD}/TV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND – 0.3	0.40	V	—
Input high voltage	V_{IH}	1.70	LV_{DD}/TV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.70	V	—
Input high current (V_{IN} = LV_{DD}, V_{IN} = TV_{DD})	I_{IH}	—	10	µA	1, 2, 3
Input low current (V_{IN} = GND)	I_{IL}	–15	—	µA	3

Note:
1. LV_{DD} supports eTSECs 1 and 2.
2. TV_{DD} supports QE UCC1 and UCC2 ethernet ports.
3. Note that the symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 2 and Table 3.

8.2 FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII and RTBI are presented in this section.

8.2.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC's FIFO modes is the double data rate RGMII and RTBI specifications, since they have similar performance and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSEC*n*'s TSEC*n*_TX_CLK, while the receive clock must be applied to pin TSEC*n*_RX_CLK. The eTSEC internally uses the transmit clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back out onto the TSEC*n*_GTX_CLK pin (while transmit data appears on TSEC*n*_TXD[7:0], for example). It is intended that external receivers capture eTSEC transmit data using the clock on TSEC*n*_GTX_CLK as a source- synchronous timing reference. Typically, the clock edge that launched the data can be used, since the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver. Note that there is relationship between the maximum FIFO speed and the platform speed. For more information see Section 4.4, "Platform to FIFO restrictions.

A summary of the FIFO AC specifications appears in Table 25 and Table 26.

Table 25. FIFO Mode Transmit AC Timing Specification

Parameter/Condition	Symbol	Min	Typ	Max	Unit
TX_CLK, GTX_CLK clock period	t_{FIT}	5.0	8.0	100	ns
TX_CLK, GTX_CLK duty cycle	t_{FITH}	45	50	55	%
TX_CLK, GTX_CLK peak-to-peak jitter	t_{FITJ}	—	—	250	ps
Rise time TX_CLK (20%–80%)	t_{FITR}	—	0.75	1.5	ns
Fall time TX_CLK (80%–20%)	t_{FITF}	—	0.75	1.5	ns
FIFO data TXD[7:0], TX_ER, TX_EN setup time to GTX_CLK	t_{FITDV}	2.0	—	—	ns
GTX_CLK to FIFO data TXD[7:0], TX_ER, TX_EN hold time	t_{FITDX}	0.5 [1]	—	3.0	ns

Table 26. FIFO Mode Receive AC Timing Specification

Parameter/Condition	Symbol	Min	Typ	Max	Unit
RX_CLK clock period	t_{FIR}	5.0	8.0	100	ns
RX_CLK duty cycle	t_{FIRH}/t_{FIRH}	45	50	55	%
RX_CLK peak-to-peak jitter	t_{FIRJ}	—	—	250	ps
Rise time RX_CLK (20%–80%)	t_{FIRR}	—	0.75	1.5	ns
Fall time RX_CLK (80%–20%)	t_{FIRF}	—	0.75	1.5	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{FIRDV}	1.5	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{FIRDX}	0.5	—	—	ns

Timing diagrams for FIFO appear in Figure 7 and Figure 8.

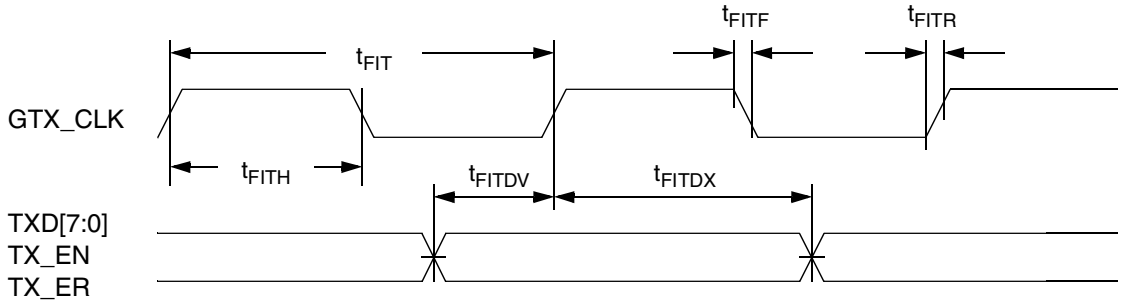


Figure 7. FIFO Transmit AC Timing Diagram

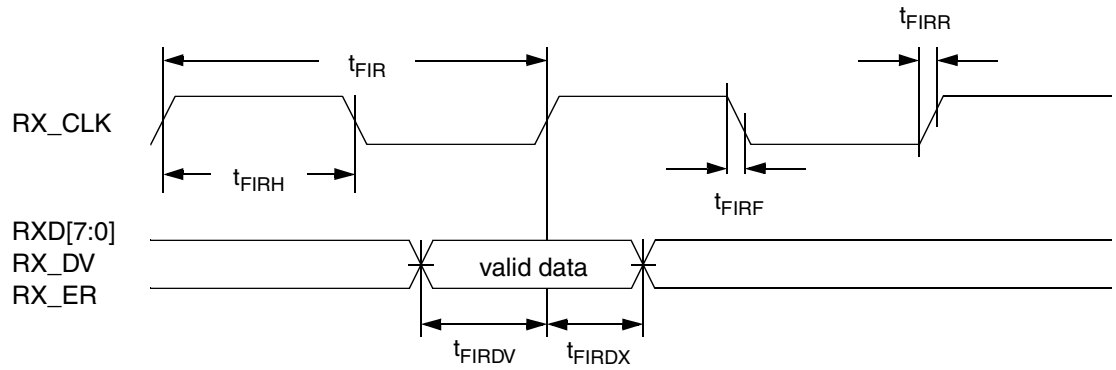


Figure 8. FIFO Receive AC Timing Diagram

8.2.2 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

8.2.2.1 GMII Transmit AC Timing Specifications

Table 27 provides the GMII transmit AC timing specifications.

Table 27. GMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
GTX_CLK clock period	t_{GTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{GTXH}/t_{GTX}	45	—	55	%
GMII data TXD[7:0], TX_ER, TX_EN setup time	t_{GTKHDV}	2.5	—	—	ns
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t_{GTKHDX}	0.5	—	5.0	ns
GTX_CLK data clock rise time (20%-80%)	t_{GTXR}^2	—	1.0	2.0	ns
GTX_CLK data clock fall time (80%-20%)	t_{GTXF}^2	—	1.0	2.0	ns
EC_GTX_CLK125 clock rise time (20%-80%)	t_{G125R}	—	1.0	2.0	ns
EC_GTX_CLK125 clock fall time (80%-20%)	t_{G125F}	—	1.0	2.0	ns

Table 27. GMII Transmit AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
EC_GTX_CLK125 duty cycle	t_{G125H}/t_{G125}	45		55	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design

Figure 9 shows the GMII transmit AC timing diagram.

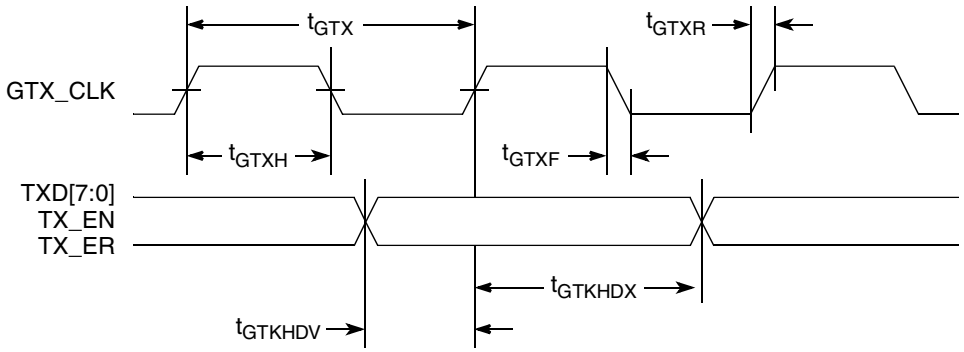


Figure 9. GMII Transmit AC Timing Diagram

8.2.2.2 GMII Receive AC Timing Specifications

Table 28 provides the GMII receive AC timing specifications.

Table 28. GMII Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period	t_{GRX}	—	8.0	—	ns
RX_CLK duty cycle	t_{GRXH}/t_{GRX}	40	—	60	ns
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t_{GRDVKH}	2.0	—	—	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t_{GRDXKH}	0.5	—	—	ns
RX_CLK clock rise (20%-80%)	t_{GRXR} [2]	—	1.0	2.0	ns

Table 28. GMII Receive AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock fall time (80%-20%)	t_{GRXF}[2]	—	1.0	2.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design

Figure 10 provides the AC test load for eTSEC.

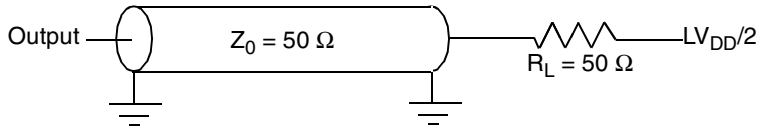


Figure 10. eTSEC AC Test Load

Figure 11 shows the GMII receive AC timing diagram.

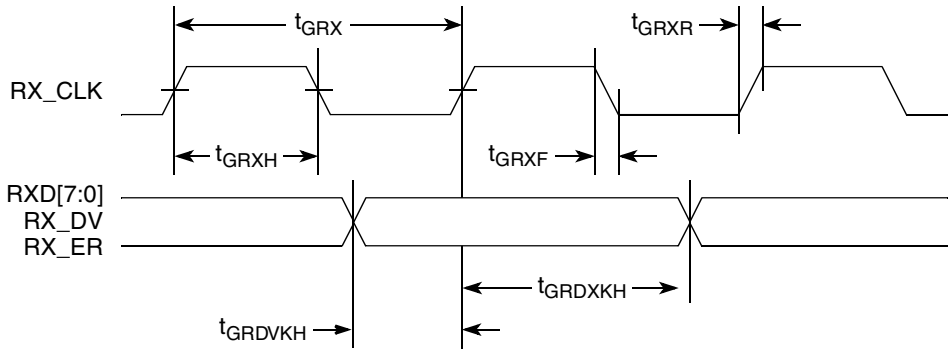


Figure 11. GMII Receive AC Timing Diagram

8.2.3 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.3.1 MII Transmit AC Timing Specifications

Table 29 provides the MII transmit AC timing specifications.

Table 29. MII Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}[2]	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise (20%-80%)	t_{MTXR}[2]	1.0	—	4.0	ns
TX_CLK data clock fall (80%-20%)	t_{MTXF}[2]	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 12 shows the MII transmit AC timing diagram.

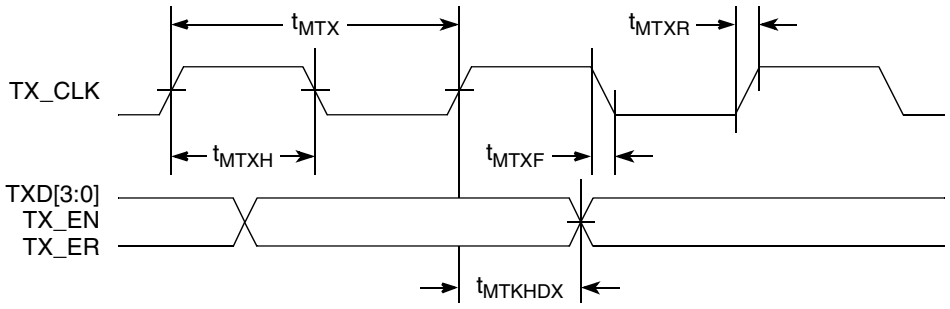


Figure 12. MII Transmit AC Timing Diagram

8.2.3.2 MII Receive AC Timing Specifications

Table 30 provides the MII receive AC timing specifications.

Table 30. MII Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}[2]	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%

Table 30. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise (20%-80%)	t_{MRXR}[2]	1.0	—	4.0	ns
RX_CLK clock fall time (80%-20%)	t_{MRXF}[2]	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 13 provides the AC test load for eTSEC.

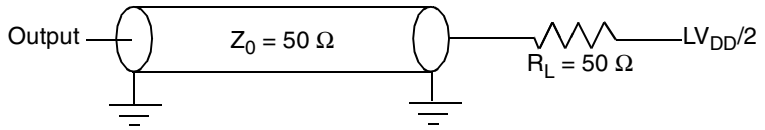


Figure 13. eTSEC AC Test Load

Figure 14 shows the MII receive AC timing diagram.

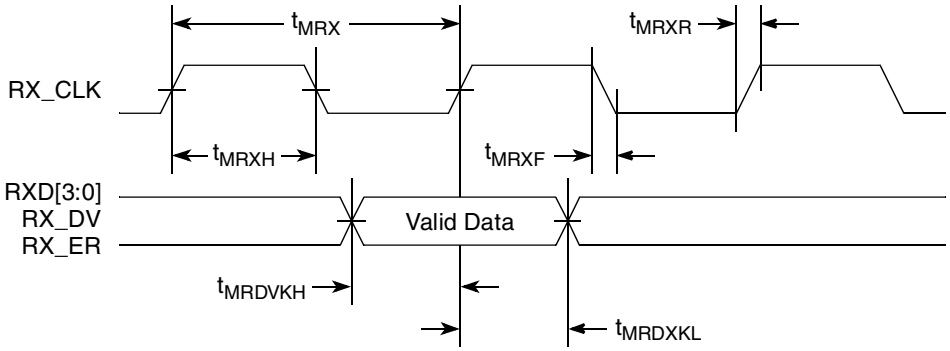


Figure 14. MII Receive AC Timing Diagram

8.2.4 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.4.1 TBI Transmit AC Timing Specifications

Table 31 provides the TBI transmit AC timing specifications.

Table 31. TBI Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
GTX_CLK clock period	t_{TTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{TTXH}/t_{TTX}	47	—	53	%
TCG[9:0] setup time GTX_CLK going high	t_{TTKHDV}	2.0	—	—	ns
TCG[9:0] hold time from GTX_CLK going high	t_{TTKHDX} [3]	1.0	—	—	ns
GTX_CLK rise (20%–80%)	t_{TTXR} [2]	—	1.0	2.0	ns
GTX_CLK fall time (80%–20%)	t_{TTXF} [2]	—	1.0	2.0	ns
EC_GTX_CLK125 clock rise time (20%-80%)	t_{G125R}	—	1.0	2.0	ns
EC_GTX_CLK125 clock fall time (80%-20%)	t_{G125F}	—	1.0	2.0	ns
EC_GTX_CLK125 duty cycle	t_{G125H}/t_{G125}	45	—	55	ns

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Guaranteed by design.

Figure 15 shows the TBI transmit AC timing diagram.

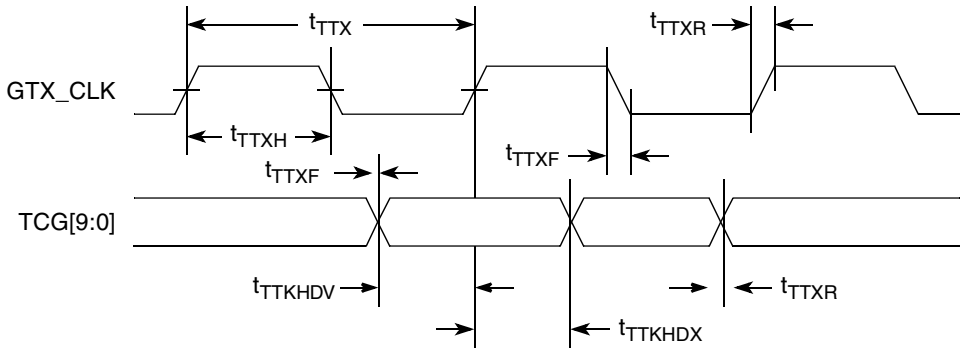


Figure 15. TBI Transmit AC Timing Diagram

8.2.4.2 TBI Receive AC Timing Specifications

Table 32 provides the TBI receive AC timing specifications.

Table 32. TBI Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
PMA_RX_CLK[0:1] clock period	t_{TRX}	—	16.0	—	ns
PMA_RX_CLK[0:1] skew	t_{SKTRX}	7.5	—	8.5	ns
PMA_RX_CLK[0:1] duty cycle	t_{TRXH}/t_{TRX}	40	—	60	%
RCG[9:0] setup time to rising PMA_RX_CLK	t_{TRDVKH}	2.5	—	—	ns
RCG[9:0] hold time to rising PMA_RX_CLK	t_{TRDXKH}	1.5	—	—	ns
PMA_RX_CLK[0:1] clock rise time (20%-80%)	t_{TRXR} [2]	0.7	—	2.4	ns
PMA_RX_CLK[0:1] clock fall time (80%-20%)	t_{TRXF} [2]	0.7	—	2.4	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).
2. Guaranteed by design.

Figure 16 shows the TBI receive AC timing diagram.

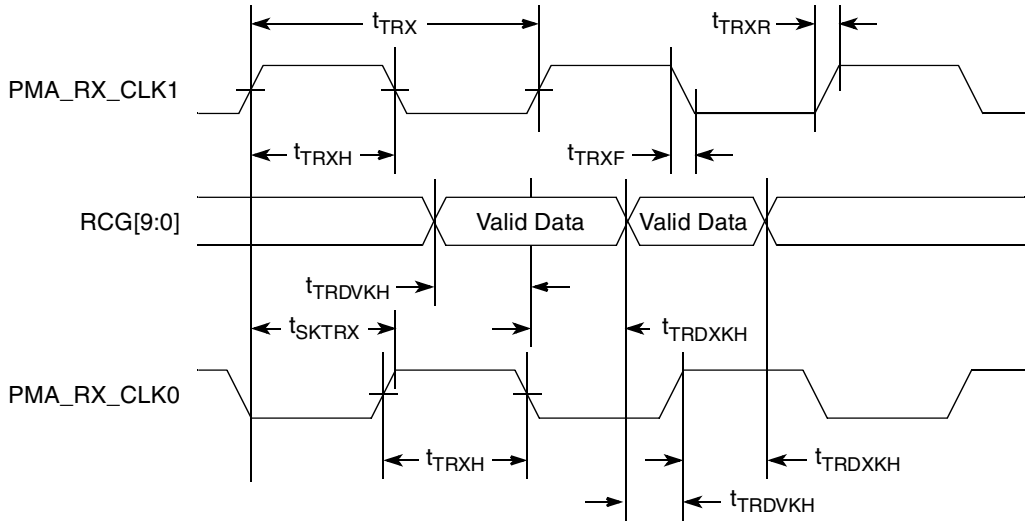


Figure 16. TBI Receive AC Timing Diagram

8.2.5 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when TBICON[CLKSEL] = 1 a 125-MHz TBI receive clock is supplied on TSEC*n* TSECn_RX_CLK pin (no receive clock is used on TSEC*n*_TX_CLK in this mode, whereas for the dual-clock mode this is the PMA1 receive clock). The 125-MHz transmit clock is applied on the TSEC_GTX_CLK125 pin in all TBI modes.

A summary of the single-clock TBI mode AC specifications for receive appears in Table 33.

Table 33. TBI single-clock Mode Receive AC Timing Specification

Parameter/Condition	Symbol	Min	Typ	Max	Unit
RX_CLK clock period	t_{TRR}	7.5	8.0	8.5	ns
RX_CLK duty cycle	t_{TRRH}	40	50	60	%
RX_CLK peak-to-peak jitter	t_{TRRJ}	—	—	250	ps
Rise time RX_CLK (20%–80%)	t_{TRRR}	—	1.0	2.0	ns
Fall time RX_CLK (80%–20%)	t_{TRRF}	—	1.0	2.0	ns
RCG[9:0] setup time to RX_CLK rising edge	t_{TRRDV}	2.0	—	—	ns
RCG[9:0] hold time to RX_CLK rising edge	t_{TRRDX}	1.0	—	—	ns

A timing diagram for TBI receive appears in Figure 17.

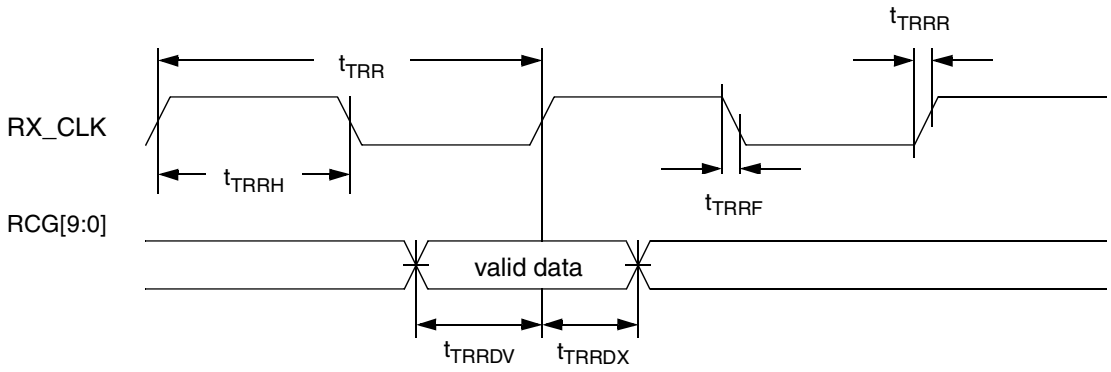


Figure 17. TBI Single-Clock Mode Receive AC Timing Diagram

8.2.6 RGMII and RTBI AC Timing Specifications

Table 34 presents the RGMII and RTBI AC timing specifications.

Table 34. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}[5]	–500[6]	0	500[6]	ps
Data to clock input skew (at receiver) [2]	t_{SKRGT}	1.0	—	2.8	ns
Clock period duration [3]	t_{RGT}[5]	7.2	8.0	8.8	ns

Table 34. RGMII and RTBI AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Duty cycle for 10BASE-T and 100BASE-TX [3, 4]	t_{RGTH}/t_{RGT}[5]	40	50	60	%
Rise time (20%–80%)	t_{RGTR}[5]	—	0.75	1.5	ns
Fall time (20%–80%)	t_{RGTF}[5]	—	0.75	1.5	ns
EC_GTX_CLK125 clock rise time (20%-80%)	t_{G125R}	—	0.75	1.5	ns
EC_GTX_CLK125 clock fall time (80%-20%)	t_{G125F}	—	0.75	1.5	ns
EC_GTX_CLK125 duty cycle[6]	t_{G125H}/t_{G125}	47		53	ns

Notes:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Guaranteed by characterization
6. EC_GTX_CLK125 is used to generate GTX_CLK for the eTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosen from 47/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK.

Figure 18 shows the RGMII and RTBI AC timing and multiplexing diagrams.

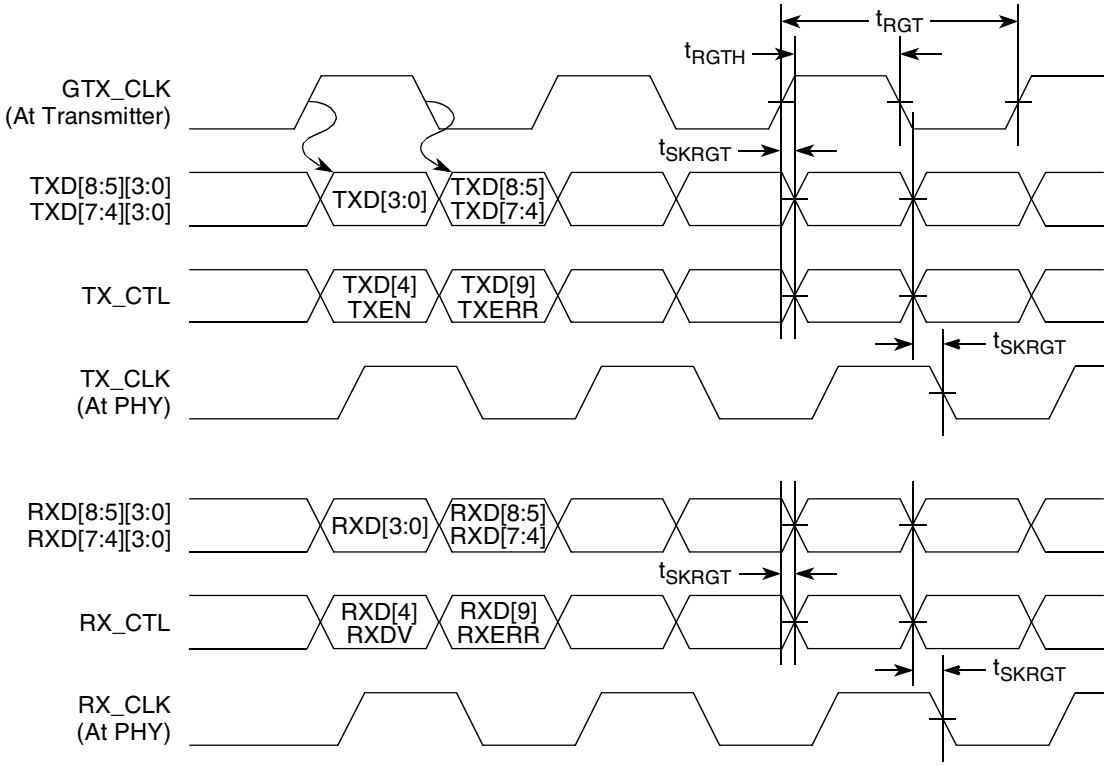


Figure 18. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.2.7 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.2.7.1 RMII Transmit AC Timing Specifications

The RMII transmit AC timing specifications are in Table 35.

Table 35. RMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
REF_CLK clock period	t_{RMT}	15.0	20.0	25.0	ns
REF_CLK duty cycle	t_{RMTH}	35	50	65	%
REF_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps
Rise time REF_CLK (20%–80%)	t_{RMTR}	1.0	—	2.0	ns
Fall time REF_CLK (80%–20%)	t_{RMTF}	1.0	—	2.0	ns

Table 35. RMII Transmit AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
REF_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	1.0	—	10.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 19 shows the RMII transmit AC timing diagram.

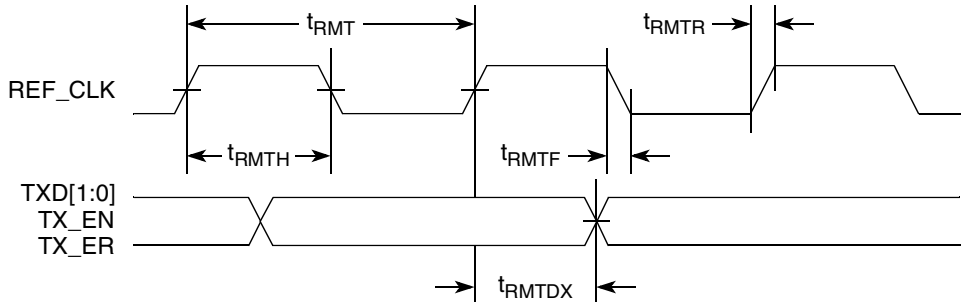


Figure 19. RMII Transmit AC Timing Diagram

8.2.7.2 RMII Receive AC Timing Specifications

Table 36. RMII Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
REF_CLK clock period	t_{RMR}	15.0	20.0	25.0	ns
REF_CLK duty cycle	t_{RMRH}	35	50	65	%
REF_CLK peak-to-peak jitter	t_{RMRJ}	—	—	250	ps
Rise time REF_CLK (20%–80%)	t_{RMRR}	1.0	—	2.0	ns
Fall time REF_CLK (80%–20%)	t_{RMRF}	1.0	—	2.0	ns
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK rising edge	t_{RMRDV}	4.0	—	—	ns

Table 36. RMII Receive AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK rising edge	t_{RMRDX}	2.0	—	—	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 20 provides the AC test load for eTSEC.

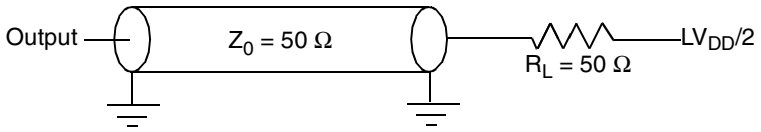


Figure 20. eTSEC AC Test Load

Figure 21 shows the RMII receive AC timing diagram.

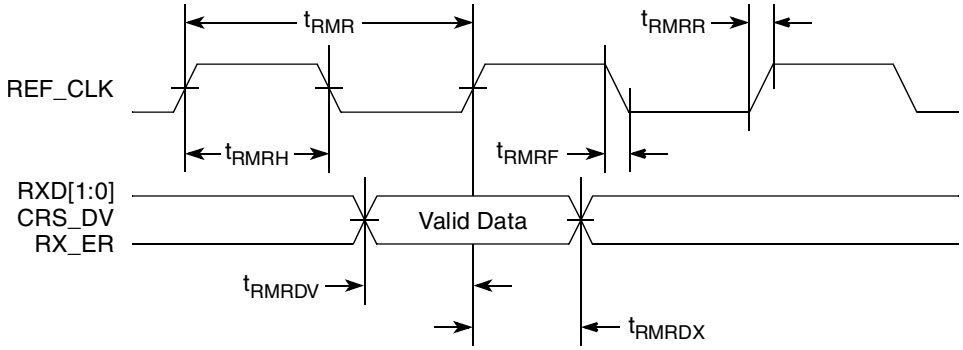


Figure 21. RMII Receive AC Timing Diagram

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock).

8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 37.

Table 37. MII Management DC Electrical Characteristics

Parameters	Symbol	Min	Max	Unit
Supply voltage 3.3 V	OV_{DD}	3.13	3.47	V
Output high voltage (OV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.10	OV_{DD} + 0.3	V
Output low voltage (OV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND	0.50	V
Input high voltage	V_{IH}	2.0	—	V
Input low voltage	V_{IL}	—	0.90	V
Input high current (OV_{DD}= Max, V_{IN} [1]= 2.1 V)	I_{IH}	—	40	µA
Input low current (OV_{DD}= Max, V_{IN} [1]= 0.5 V)	I_{IL}	–600	—	µA

Note:
1. The symbol V_{IN}, in this case, represents the OV_{IN} symbols referenced in Table 2 and Table 3.

8.3.2 MII Management AC Electrical Characteristics

Table 38 provides the MII management AC timing specifications.

Table 38. MII management AC timing specifications

Parameters	Symbol	Min	Max	Unit	Notes
MDC frequency	f_{MDC}	—	2.5	MHz	2

Table 38. MII management AC timing specifications (continued)

Parameters	Symbol	Min	Max	Unit	Notes
MDC period	t_{MDC}	400	—	ns	2
MDC clock pulse width high	t_{MDCH}	32	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	$(16*t_{plb\_clk})-3$	$(16*t_{plb\_clk})+3$	ns	3, 5
MDIO to MDC setup time	t_{MDDVKH}	5	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	ns	—
MDC rise time	t_{MDCR}	—	10	ns	4
MDC fall time	t_{MDCF}	—	10	ns	4

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. IEEE 802.3 standard specifies that the max MDC frequency to be 2.5MHz. The frequency is programmed through MIIMCFG[MgmtClk].
3. This parameter is dependent on the platform clock speed. The delay is equal to 16 platform clock periods +/-3ns. With a platform clock of 333MHz, the min/max delay is 48ns +/- 3ns.
4. Guaranteed by design
5. t_{plb_clk} is the platform (CCB) clock period.
6. MDC to MDIO data valid t_{MDKHDV} is a function of clock period and max delay time (t_{MDKHDX}). (Min Setup time = Cycle time – Max delay).

Figure 22 shows the MII management AC timing diagram.

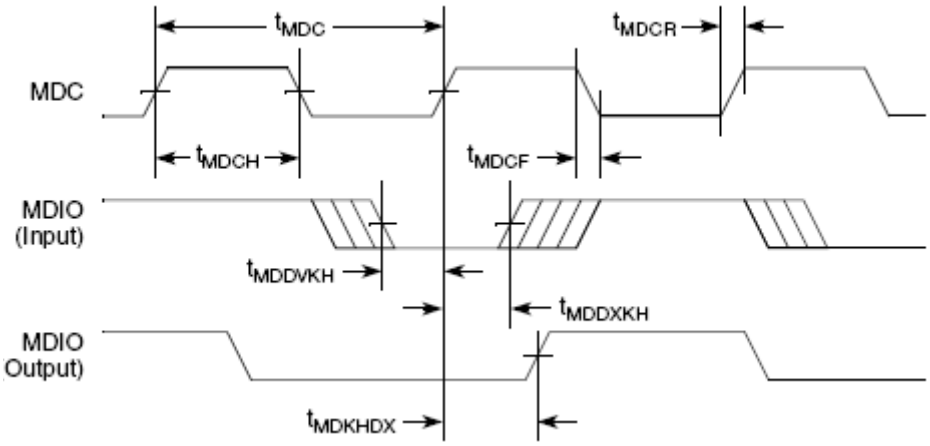


Figure 22. MII Management Interface Timing Diagram

9 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8568.

9.1 Local Bus DC Electrical Characteristics

Table 39 provides the DC electrical characteristics for the local bus interface operating at BV_{DD} = 3.3 V DC.

Table 39. Local Bus DC Electrical Characteristics (3.3 V DC)

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	BV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current (V_{IN} [1] = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±5	μA
High-level output voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V
Low-level output voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V

Note:
1. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 2 and Table 3.

Table 40 provides the DC electrical characteristics for the local bus interface operating at BV_{DD} = 2.5 V DC.

Table 40. Local Bus DC Electrical Characteristics (2.5 V DC)

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	1.70	BV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.7	V
Input current (V_{IN} [1] = 0 V or V_{IN} = BV_{DD})	I_{IH}	—	10	μA
	I_{IL}		–15	
High-level output voltage (BV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	—	V
Low-level output voltage (BV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.4	V

Note:
1. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 2 and Table 3.

9.2 Local Bus AC Electrical Specifications

Table 41 describes the timing parameters of the local bus interface at BV_{DD} = 3.3 V. For information about the frequency range of local bus see Section 23.1, "Clock Ranges."

Table 41. Local Bus Timing Parameters (BV_{DD} = 3.3 V)—PLL Enabled

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	12	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	150	ps	7, 8
Input setup to local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIVKH1}$	1.8	—	ns	3, 4
$\overline{\text{LGTA}}$/LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	1.7	—	ns	3, 4
Input hold from local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIXKH1}$	1.0	—	ns	3, 4
$\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock	$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	3.0	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	3.2	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	3.2	ns	3
Local bus clock to LALE assertion	$t_{LBKHOV4}$	—	3.2	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	0.7	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	0.7	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKHOZ1}$	—	2.5	ns	5
Local bus clock to output high impedance for LAD/LDP	$t_{LBKHOZ2}$	—	2.5	ns	5

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
8. Guaranteed by design.

Table 42 describes the timing parameters of the local bus interface at BV_{DD} = 2.5 V.

Table 42. Local Bus Timing Parameters (BV_{DD} = 2.5 V)—PLL Enabled

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	12	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	150	ps	7, 8
Input setup to local bus clock (except $\overline{\text{LGTA}}$/UPWAIT)	$t_{LBIVKH1}$	1.9	—	ns	3, 4
$\overline{\text{LGTA}}$/LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	1.8	—	ns	3, 4
Input hold from local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIXKH1}$	1.1	—	ns	3, 4
$\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock	$t_{LBIXKH2}$	1.1	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	3.0	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	3.2	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	3.2	ns	3
Local bus clock to LALE assertion	$t_{LBKHOV4}$	—	3.2	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	0.8	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	0.8	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKHOZ1}$	—	2.6	ns	5
Local bus clock to output high impedance for LAD/LDP	$t_{LBKHOZ2}$	—	2.6	ns	5

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.
3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV^{DD}/2$.
8. Guaranteed by design.

Figure 23 provides the AC test load for the local bus.

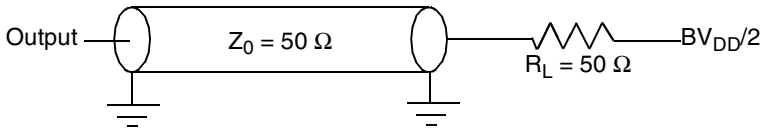


Figure 23. Local Bus AC Test Load

NOTE

PLL bypass mode is required when LBIU frequency is at or below 83 MHz. When LBIU operates above 83 MHz, LBIU PLL is recommended to be enabled.

Figure 24 to Figure 29 show the local bus signals.

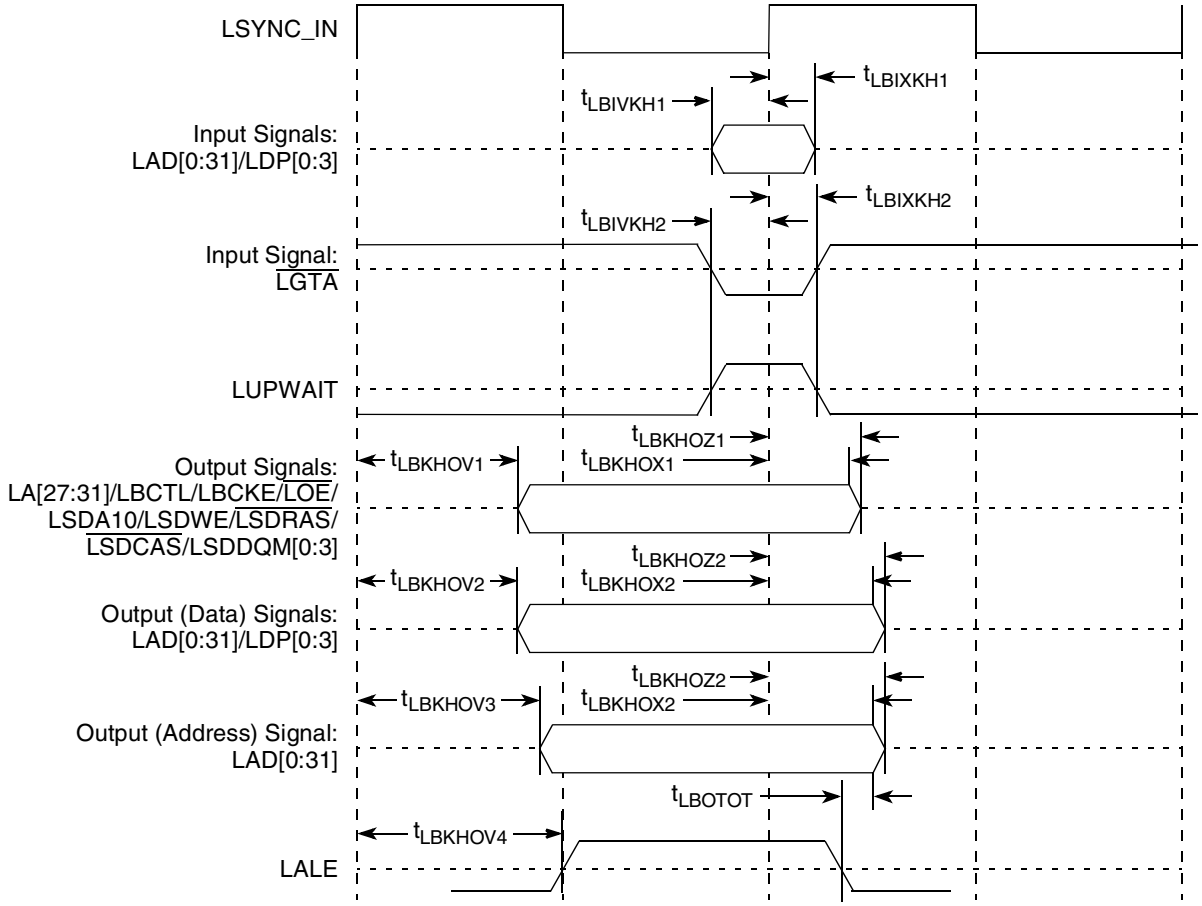


Figure 24. Local Bus Signals (PLL Enabled)

Table 43 describes the timing parameters of the local bus interface at BV_{DD} = 3.3 V with PLL disabled.

Table 43. Local Bus Timing Parameters—PLL Bypassed

Parameter	Symbol [1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	12	—	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—

Table 43. Local Bus Timing Parameters—PLL Bypassed (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
Internal launch/capture clock to LCLK delay	t_{LBKHKT}	2.3	4.4	ns	8
Input setup to local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIVKH1}$	6.2	—	ns	4, 5
$\overline{\text{LGTA}}$/LUPWAIT input setup to local bus clock	$t_{LBIVKL2}$	6.1	—	ns	4, 5
Input hold from local bus clock (except $\overline{\text{LGTA}}$/LUPWAIT)	$t_{LBIXKH1}$	–1.8	—	ns	4, 5
$\overline{\text{LGTA}}$/LUPWAIT input hold from local bus clock	$t_{LBIXKL2}$	–1.3	—	ns	4, 5
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKLOV1}$	—	-0.3	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKLOV2}$	—	-0.1	ns	4
Local bus clock to address valid for LAD	$t_{LBKLOV3}$	—	0	ns	4
Local bus clock to LALE assertion	$t_{LBKLOV4}$	—	0	ns	4
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKLOX1}$	–3.7	—	ns	4
Output hold from local bus clock for LAD/LDP	$t_{LBKLOX2}$	–3.7	—	ns	4
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKLOZ1}$	—	0.2	ns	7
Local bus clock to output high impedance for LAD/LDP	$t_{LBKLOZ2}$	—	0.2	ns	7

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one(1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to local bus clock for PLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which precedes LCLK by t_{LBKHKT}.
3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
4. All signals are measured from BVDD/2 of the rising edge of local bus clock for PLL bypass mode to 0.4 x BVDD of the signal in question for 3.3-V signaling levels.
5. Input timings are measured at the pin.
6. The value of t_{LBOTOT} is the measurement of the minimum time between the negation of LALE and any change in LAD
7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
8. Guaranteed by characterization.
9. Guaranteed by design.

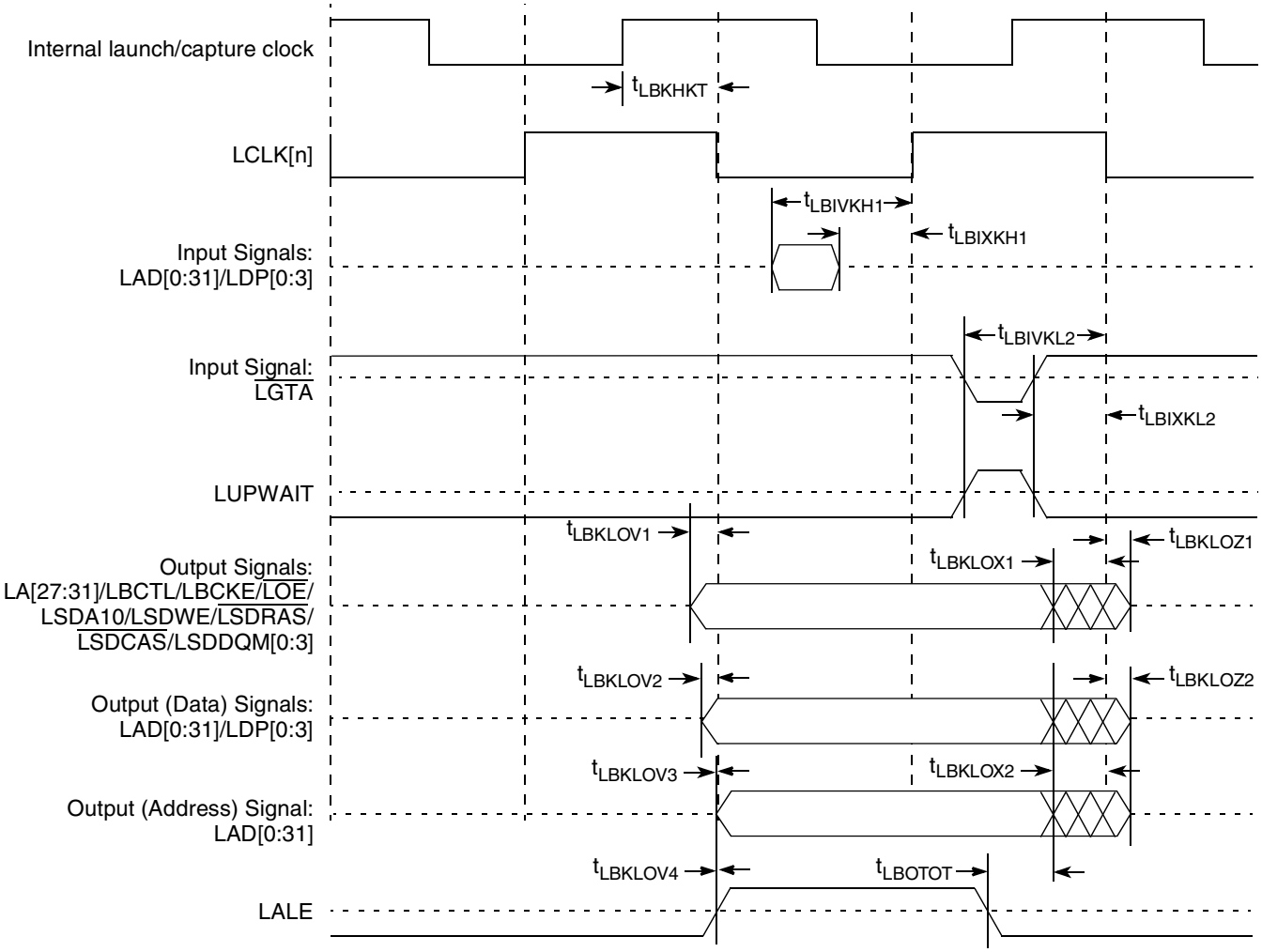


Figure 25. Local Bus Signals (PLL Bypass Mode)

NOTE

In PLL bypass mode, LCLK[n] is the inverted version of the internal clock with the delay of t_{LBKHKT}. In this mode, signals are launched at the rising edge of the internal clock and are captured at falling edge of the internal clock with the exception of $\overline{\text{LGTA}}$/LUPWAIT (which is captured on the rising edge of the internal clock).

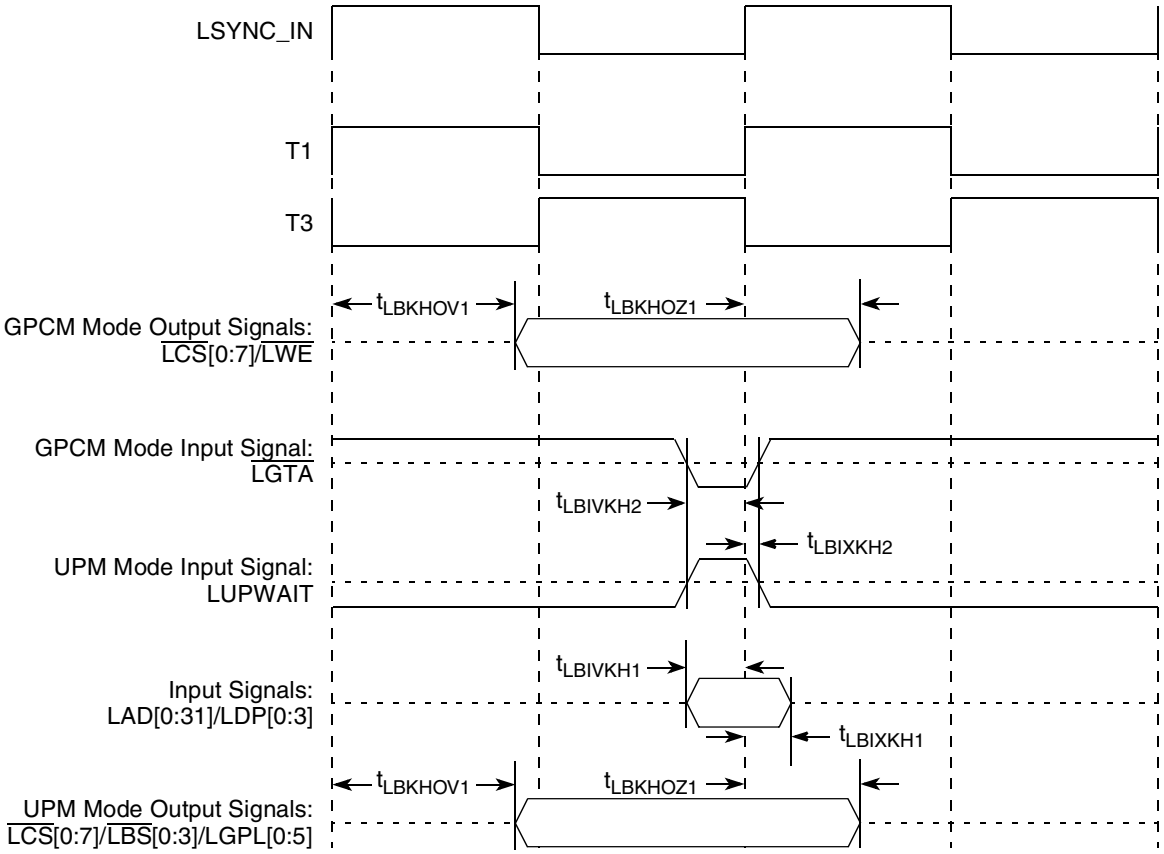


Figure 26. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Enabled)

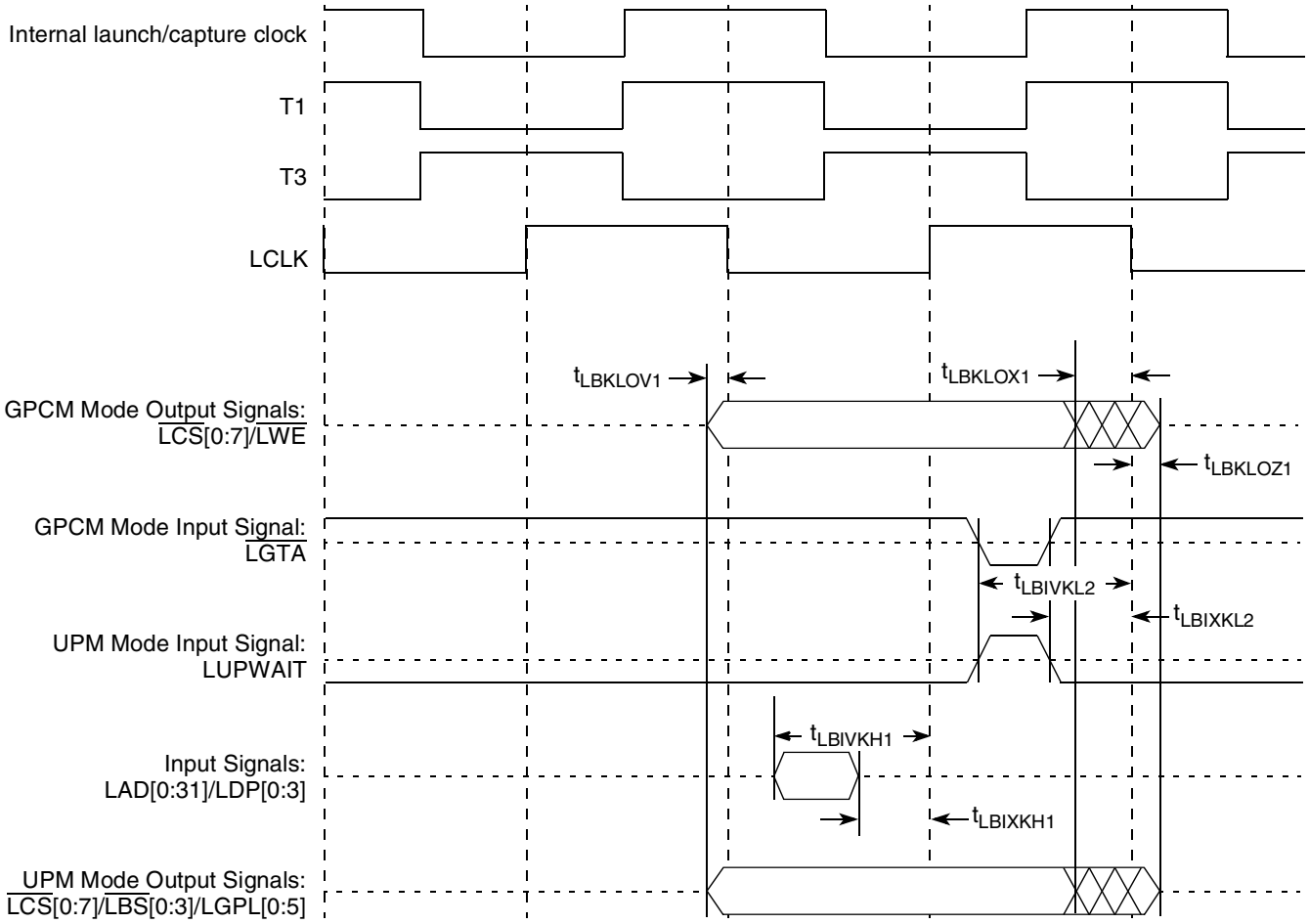


Figure 27. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Bypass Mode)

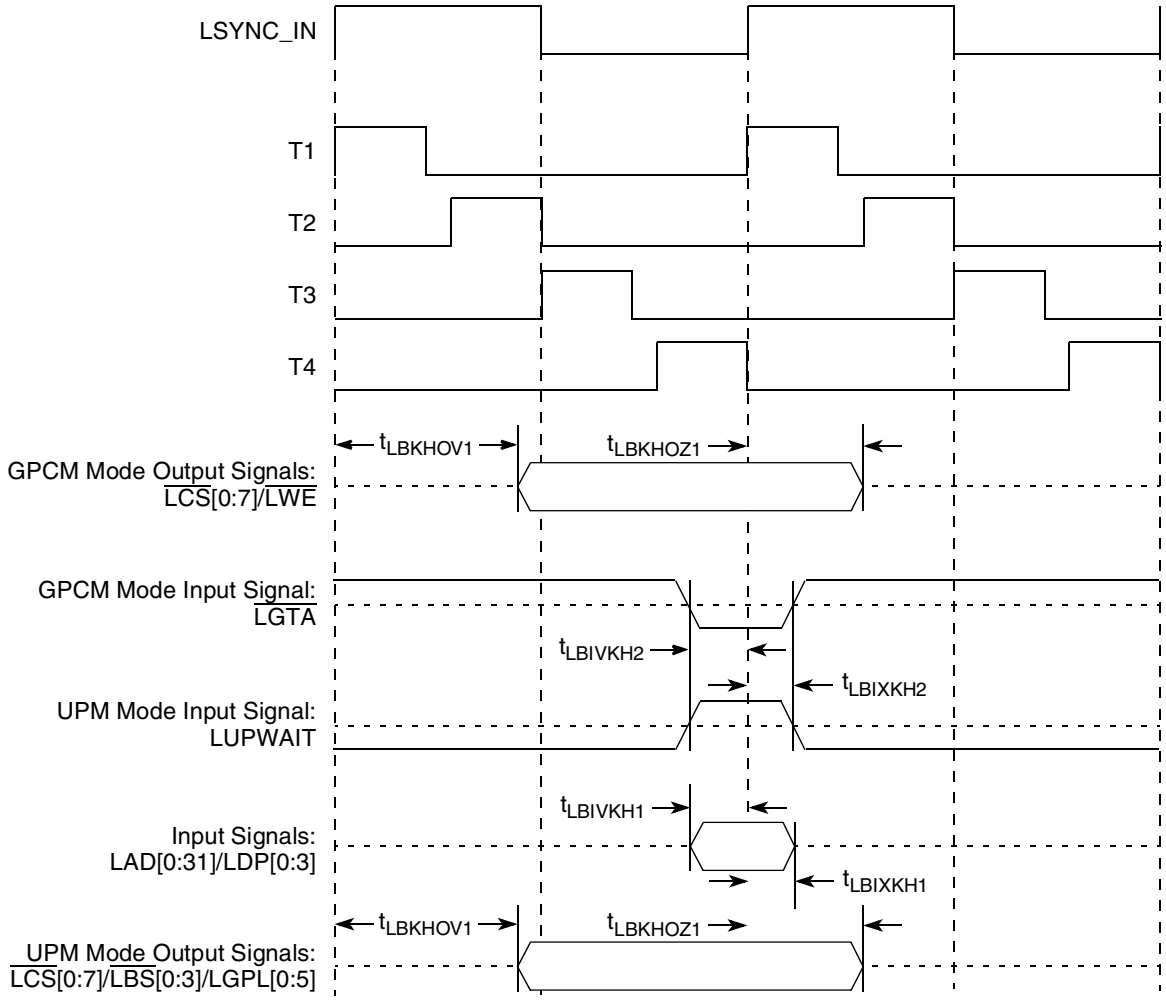


Figure 28. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Enabled)

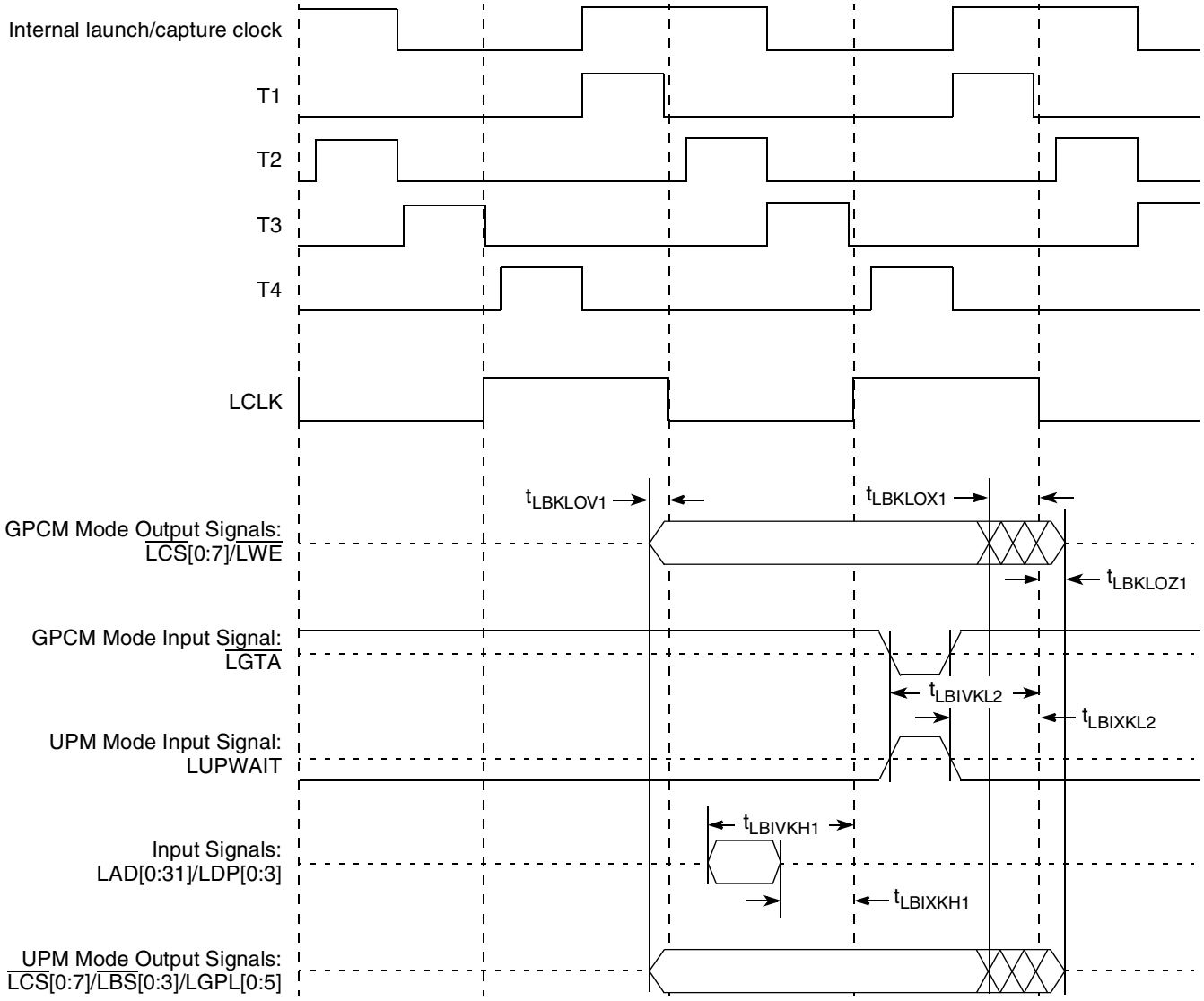


Figure 29. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Bypass Mode)

10 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std 1149.1™ (JTAG) interface of the MPC8568E.

10.1 JTAG DC Electrical Characteristics

Table provides the DC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8568E.

Table 44. JTAG DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = -6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.5	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	$0 < V_{IN} < OV_{DD}$	—	±10	uA

10.2 JTAG AC Electrical Characteristics

Table 45 provides the JTAG AC timing specifications as defined in Figure 31 through Figure 33.

Table 45. JTAG AC Timing Specifications (Independent of SYSCLK) [1]

At recommended operating conditions (see Table 3).

Parameter	Symbol [2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} & t_{JTGF}	0	2	ns	6
$\overline{TRST}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 0	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 20 25	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 4 4	 20 25	ns	5
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 30 30	 — —	ns	5

Table 45. JTAG AC Timing Specifications (Independent of SYSCLK) [1] (continued)

At recommended operating conditions (see Table 3).

Parameter	Symbol [2]	Min	Max	Unit	Notes
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 3 3	 19 9	ns	5, 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 30). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design

Figure 30 provides the AC test load for TDO and the boundary-scan outputs.

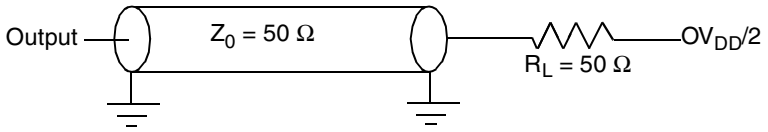


Figure 30. AC Test Load for the JTAG Interface

Figure 31 provides the JTAG clock input timing diagram.

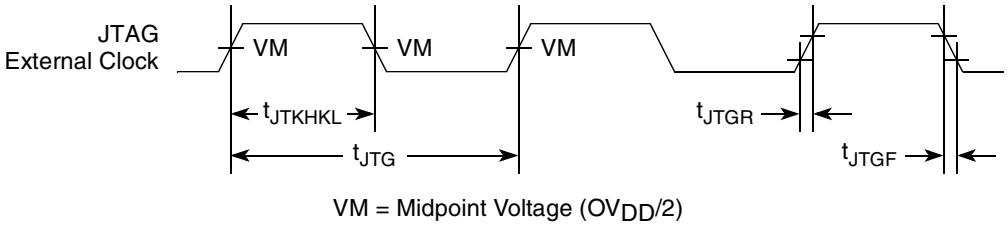


Figure 31. JTAG Clock Input Timing Diagram

Figure 32 provides the $\overline{\text{TRST}}$ timing diagram.

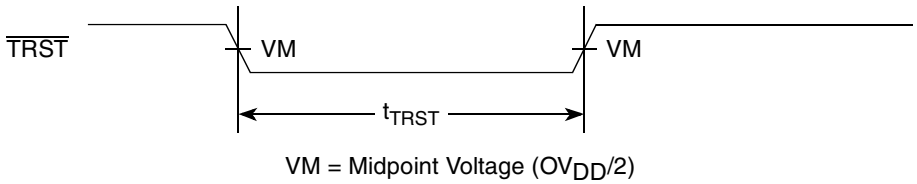


Figure 32. $\overline{\text{TRST}}$ Timing Diagram

Figure 33 provides the boundary-scan timing diagram.

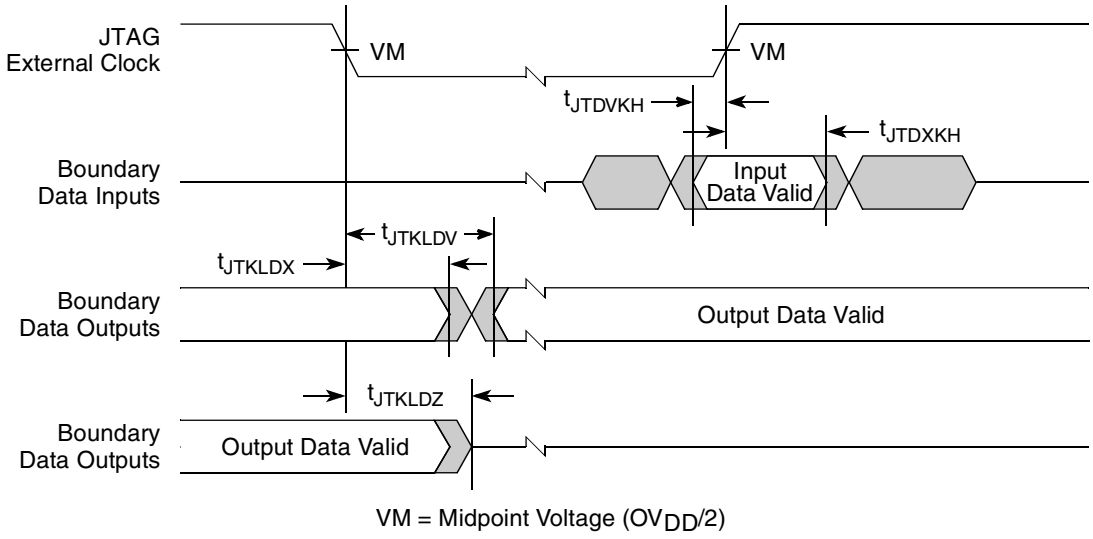


Figure 33. Boundary-Scan Timing Diagram

11 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the MPC8568E. Note that I²C2 is multiplexed with QE Port C.

PC[18] IIC2_SCL

PC[19] IIC2_SDA

11.1 I²C DC Electrical Characteristics

Table 46 provides the DC electrical characteristics for the I²C interfaces.

Table 46. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	—
Low level output voltage	V_{OL}	0	0.4	V	1
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	2
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max)	I_I	–10	10	µA	3

Table 46. I²C DC Electrical Characteristics (continued)

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Capacitance for each I/O pin	C_I	—	10	pF	—

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. Refer to the *MPC8568E PowerQUICC III Integrated Communications Processor Reference Manual* for information on the digital filter used.
3. I/O pins will obstruct the SDA and SCL lines if OV_{DD} is switched off.

11.2 I²C AC Electrical Specifications

Table 47 provides the AC timing parameters for the I²C interfaces.

Table 47. I²C AC Electrical Specifications

At recommended operating conditions with OV_{DD} of 3.3V ± 5%. All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 46).

Parameter	Symbol [1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}	1.3	—	µs
High period of the SCL clock	t_{I2CH}	0.6	—	µs
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	µs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	µs
Data setup time	t_{I2DVKH}	100	—	ns
Data input hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	— 0 [2]	— —	µs
Data output delay time	t_{I2OVKL}	—	0.9 [3]	µs
Set-up time for STOP condition	t_{I2PVKH}	0.6	—	µs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	µs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V

Table 47. I²C AC Electrical Specifications (continued)

At recommended operating conditions with OV_{DD} of 3.3V ± 5%. All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 46).

Parameter	Symbol [1]	Min	Max	Unit
Capacitive load for each bus line	C_b	—	400	pF

Note:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the STOP condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.
2. As a transmitter, the MPC8568 provides a delay time of at least 300 ns for the SDA signal (referred to the V_{IH}min of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of START or STOP condition. When the MPC8568 acts as the I²C bus master while transmitting, the MPC8568 drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the MPC8568 would not cause unintended generation of START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the MPC8568 as transmitter, application note AN2919 referred to in note 4 below is recommended.
3. The maximum t_{I2DXKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. The requirements for I²C frequency calculation must be followed. Refer to Freescale application note AN2919, *Determining the I²C Frequency Divider Ratio for SCL*

Figure 30 provides the AC test load for the I²C.

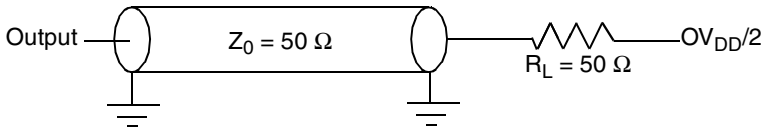


Figure 34. I²C AC Test Load

Figure 35 shows the AC timing diagram for the I²C bus.

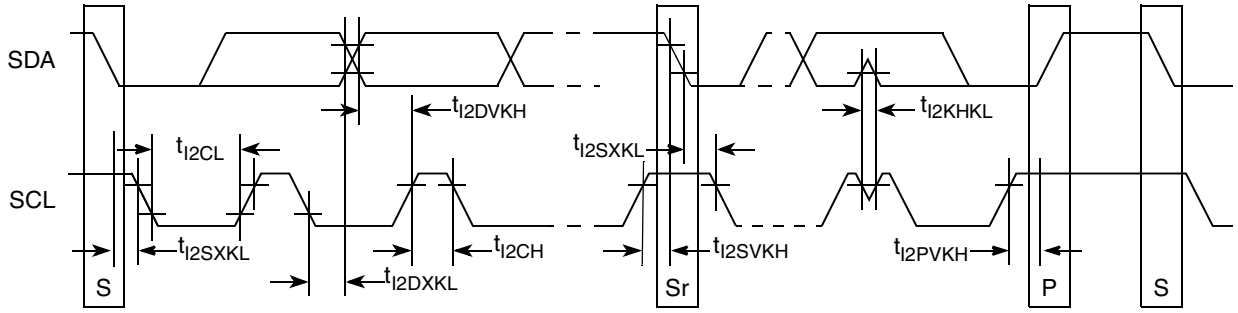


Figure 35. I²C Bus AC Timing Diagram

12 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8568E.

12.1 PCI DC Electrical Characteristics

Table 48 provides the DC electrical characteristics for the PCI interface.

Table 48. PCI DC Electrical Characteristics [1]

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	0.5*OV_{DD}	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.5	0.3*OV_{DD}	V
Input current (V_{IN} [1]= 0 V or V_{IN} = V_{DD})	I_{IN}	—	±10	μA
High-level output voltage (OV_{DD} = min, I_{OH} = –500 μA)	V_{OH}	0.9*OV_{DD}	—	V
Low-level output voltage (OV_{DD} = max, I_{OL} = 1500 μA)	V_{OL}	—	0.1*OV_{DD}	V

Notes:
1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 2 and Table 3.

12.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus. Note that the SYSCLK signal is used as the PCI input clock. Table 49 provides the PCI AC timing specifications at 66 MHz.

Table 49. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol [1]	Min	Max	Unit	Notes
SYSCLK to output valid	t_{PCKHOV}	—	6.0	ns	2, 3
Output hold from SYSCLK	t_{PCKHOX}	2.0	—	ns	2, 10
SYSCLK to output high impedance	t_{PCKHOZ}	—	14	ns	2, 4, 11
Input setup to SYSCLK	t_{PCIVKH}	3.0	—	ns	2, 5, 10
Input hold from SYSCLK	t_{PCIXKH}	0	—	ns	2, 5, 10

Table 49. PCI AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol [1]	Min	Max	Unit	Notes
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	8, 11

Notes:

1. Note that the symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the SYSCLK clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. All PCI signals are measured from $OV_{DD}/2$ of the rising edge of PCI_CLK to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V PCI signaling levels.
4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Input timings are measured at the pin.
6. The timing parameter t_{SYS} indicates the minimum and maximum CLK cycle times for the various specified frequencies. The system clock period must be kept within the minimum and maximum defined ranges. For values see Section 23, "Clocking."
7. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$.
8. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI 2.2 Local Bus Specifications*.
9. The reset assertion timing requirement for $\overline{\text{HRESET}}$ is 100 µs.
10. Guaranteed by characterization
11. Guaranteed by design

Figure 30 provides the AC test load for PCI.

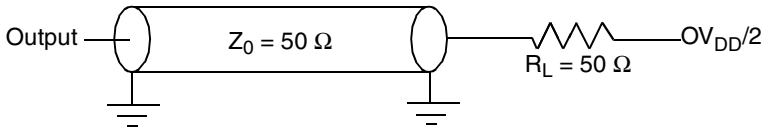


Figure 36. PCI AC Test Load

Figure 37 shows the PCI input AC timing conditions.

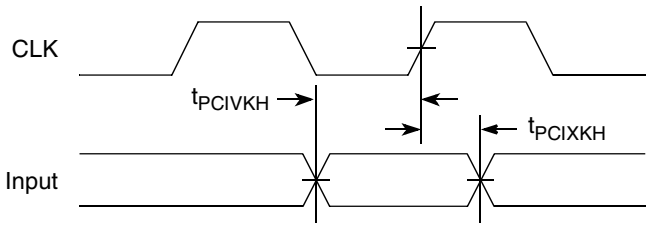


Figure 37. PCI Input AC Timing Measurement Conditions

Figure 38 shows the PCI output AC timing conditions.

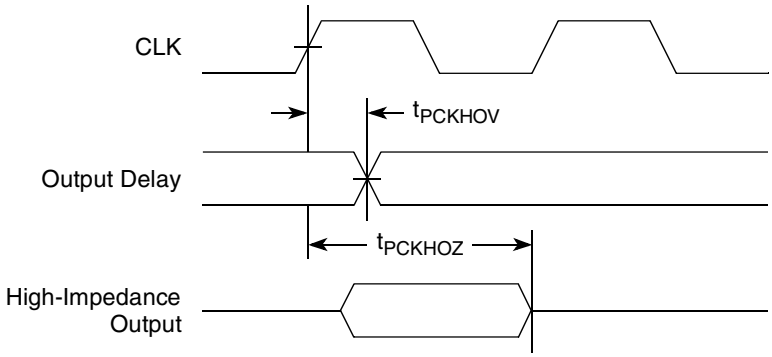


Figure 38. PCI Output AC Timing Measurement Condition

13 High-Speed Serial Interfaces (HSSI)

The MPC8568E features one Serializer/Deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. It can be used for PCI Express and/or Serial RapidIO data transfers.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

13.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 39 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SD_TX and $\overline{\text{SD\_TX}}$) or a receiver input (SD_RX and $\overline{\text{SD\_RX}}$). Each signal swings between A Volts and B Volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. **Single-Ended Swing**

   The transmitter output signals and the receiver input signals SD_TX, $\overline{\text{SD\_TX}}$, SD_RX and $\overline{\text{SD\_RX}}$ each have a peak-to-peak swing of A – B Volts. This is also referred as each signal wire's Single-Ended Swing.

2. **Differential Output Voltage, V_{OD}** (or **Differential Output Swing**):

   The Differential Output Voltage (or Swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SD\_TX} - V_{\overline{SD\_TX}}$. The V_{OD} value can be either positive or negative.

3. **Differential Input Voltage, V_{ID}** (or **Differential Input Swing**):

The Differential Input Voltage (or Swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{SD\_RX} - V_{\overline{SD\_RX}}$. The V_{ID} value can be either positive or negative.

4. **Differential Peak Voltage, V_{DIFFp}**

   The peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak Voltage, $V_{DIFFp} = |A - B|$ Volts.

5. **Differential Peak-to-Peak, $V_{DIFFp-p}$**

   Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) Volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak-to-Peak Voltage, $V_{DIFFp-p} = 2*V_{DIFFp} = 2 * |(A - B)|$ Volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2*|V_{OD}|$.

6. **Common Mode Voltage, V_{cm}**

   The Common Mode Voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = V_{SD\_TX} + V_{\overline{SD\_TX}} = (A + B) / 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred as the DC offset in some occasion.

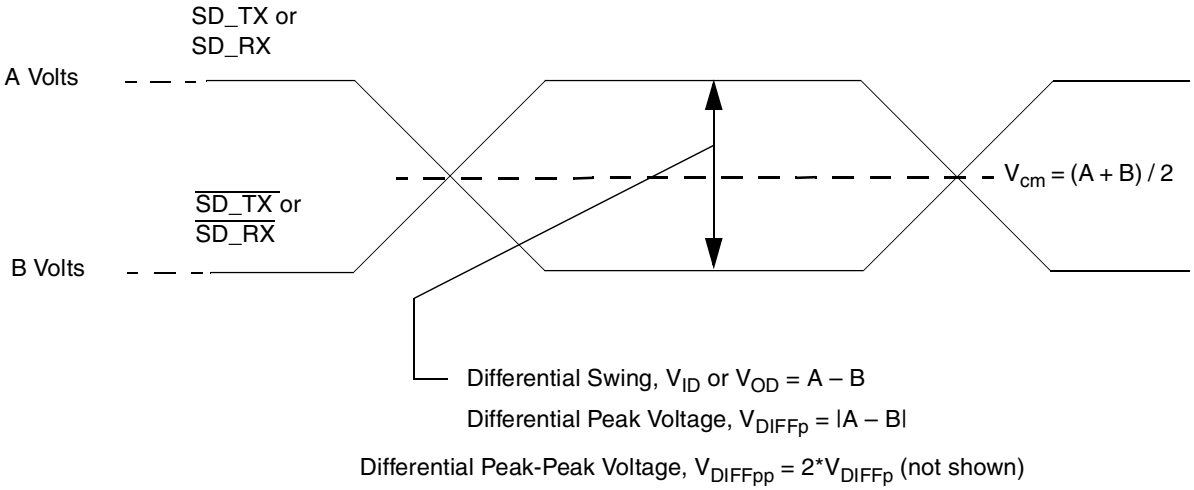


Figure 39. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{TD}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{TD}$) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges

between 500 mV and –500 mV, in other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

13.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$.

The following sections describe the SerDes reference clock requirements and some application information.

13.2.1 SerDes Reference Clock Receiver Characteristics

Figure 40 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for SCOREVDD and XVDD are specified in Table 2 and Table 3.
- SerDes Reference Clock Receiver Reference Circuit Structure
  - The SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 40. Each differential clock input (SD_REF_CLK or $\overline{\text{SD\_REF\_CLK}}$) has a 50-Ω termination to SCOREGND followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. Refer to the Differential Mode and Single-ended Mode description below for further detailed requirements.
- The maximum average current requirement that also determines the common mode voltage range
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), since the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4V (0.4V/50 = 8mA) while the minimum common mode input level is 0.1V above SCOREGND. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0mA to 16mA (0-0.8V), such that each phase of the differential input has a single-ended swing from 0V to 800mV with the common mode voltage at 400mV.
  - If the device driving the SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ inputs cannot drive 50 ohms to SCOREGND DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement
  - This requirement is described in detail in the following sections.

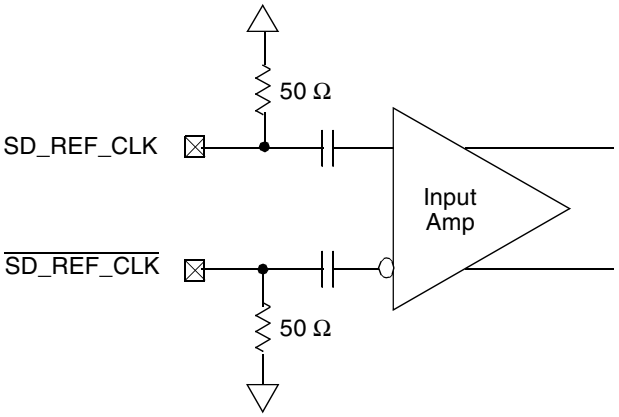


Figure 40. Receiver of SerDes Reference Clocks

13.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the MPC8568E SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- **Differential Mode**
  - The input amplitude of the differential clock must be between 400mV and 1600mV differential peak-peak (or between 200mV and 800mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800mV and greater than 200mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For **external DC-coupled** connection, as described in section 13.2.1, the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 mV and 400 mV. Figure 41 shows the SerDes reference clock input requirement for DC-coupled connection scheme.
  - For **external AC-coupled** connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SCOREGND. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SCOREGND). Figure 42 shows the SerDes reference clock input requirement for AC-coupled connection scheme.
- **Single-ended Mode**
  - The reference clock can also be single-ended. The SD_REF_CLK input amplitude (single-ended swing) must be between 400mV and 800mV peak-peak (from Vmin to Vmax) with $\overline{\text{SD\_REF\_CLK}}$ either left unconnected or tied to ground.
  - The SD_REF_CLK input average voltage must be between 200 and 400 mV. Figure 43 shows the SerDes reference clock input requirement for single-ended signaling mode.
  - To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC

or AC-coupled into the unused phase ($\overline{\text{SD\_REF\_CLK}}$) through the same source impedance as the clock input (SD_REF_CLK) in use.

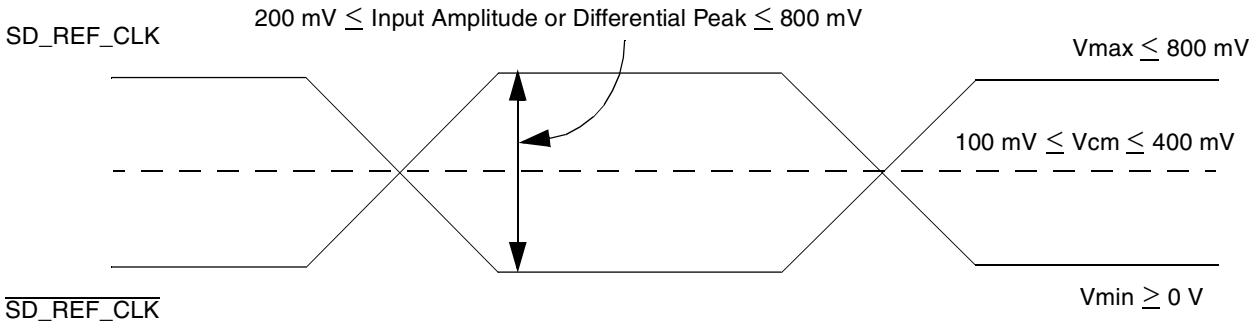


Figure 41. Differential Reference Clock Input DC Requirements (External DC-Coupled)

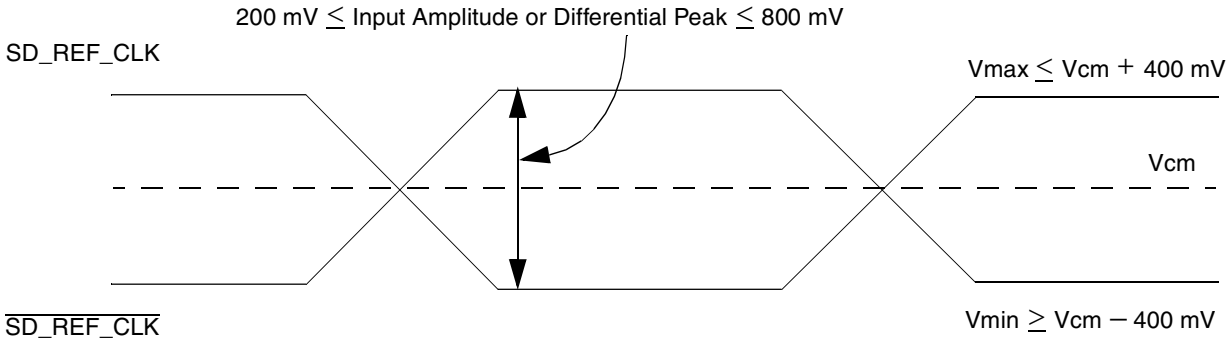


Figure 42. Differential Reference Clock Input DC Requirements (External AC-Coupled)

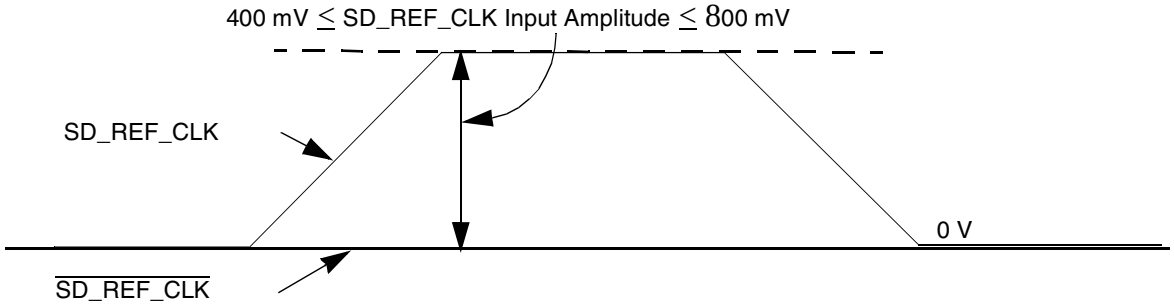


Figure 43. Single-Ended Reference Clock Input DC Requirements

13.2.3 Interfacing With Other Differential Signaling Levels

- With on-chip termination to SCOREGND, the differential reference clocks inputs are HCSL (High-Speed Current Steering Logic) compatible DC-coupled.
- Many other low voltage differential type outputs like LVDS (Low Voltage Differential Signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.
- LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

NOTE

Figure 44 to Figure 47 below are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the MPC8568 SerDes reference clock receiver requirement provided in this document.

Figure 44 shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with MPC8568 SerDes reference clock input's DC requirement.

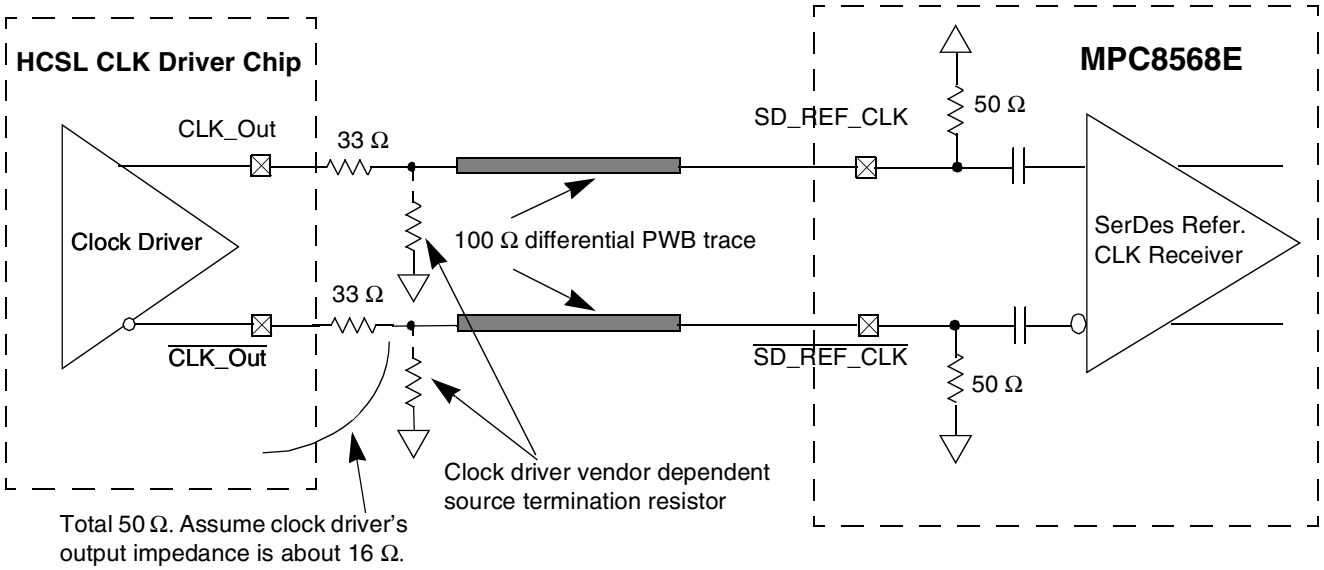


Figure 44. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

Figure 45 shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the MPC8568 SerDes reference clock input's allowed range (100 to 400mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

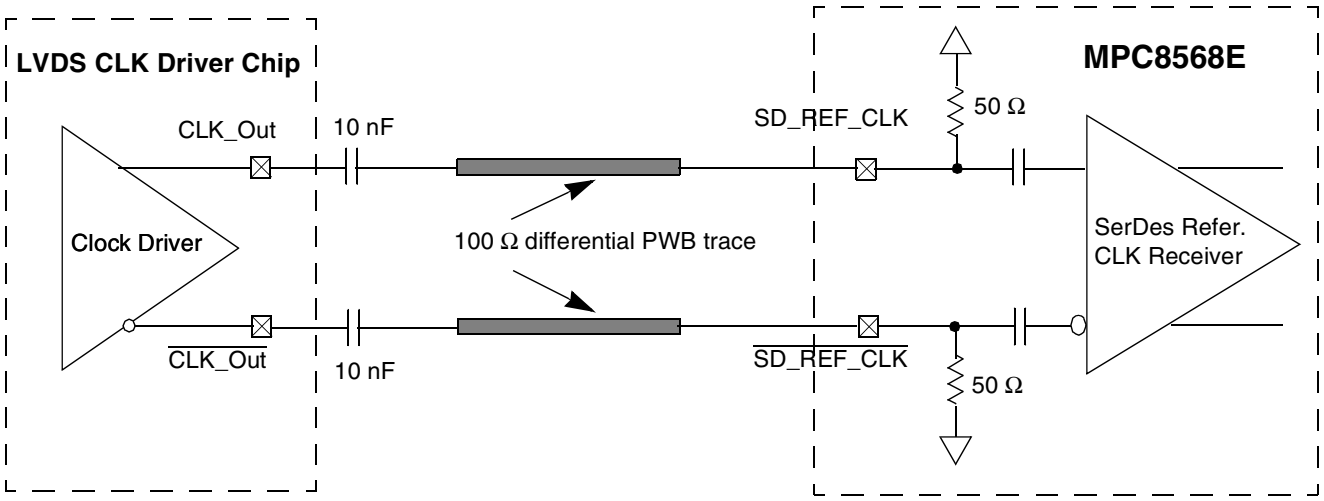


Figure 45. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

Figure 46 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with MPC8568 SerDes reference clock input's DC requirement, AC-coupling has to be used. Figure 46 assumes that the LVPECL clock driver's output impedance is 50Ω. R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value could be ranged from 140Ω to 240Ω depending on clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50-Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the MPC8568 SerDes reference clock's differential input amplitude requirement (between 200mV and 800mV differential peak). For example, if the LVPECL output's differential peak is 900mV and the desired SerDes reference clock input amplitude is selected as 600mV, the attenuation factor is 0.67, which requires R2 = 25Ω. Consult clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

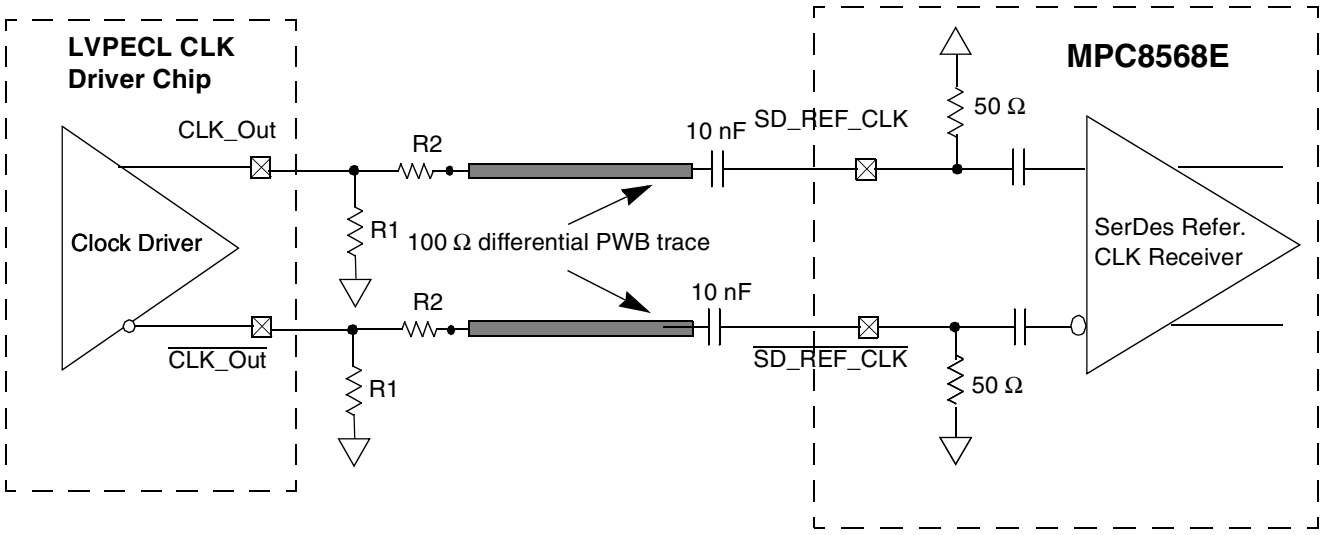


Figure 46. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

Figure 47 shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with MPC8568E SerDes reference clock input's DC requirement.

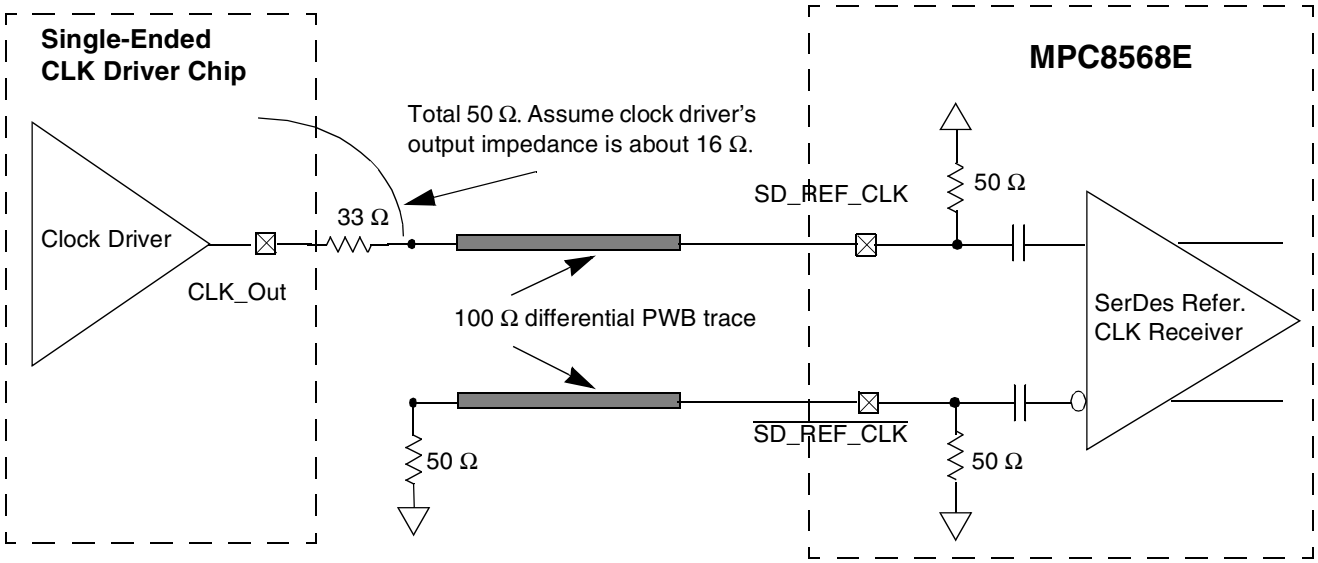


Figure 47. Single-Ended Connection (Reference Only)

13.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100 kHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise occurs in the 1–15 MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

The detailed AC requirements of the SerDes Reference Clocks is defined by each interface protocol based on application usage. Refer to the following sections for detailed information:

- Section 14.2, "AC Requirements for PCI Express SerDes Clocks"
- Section 15.2, "AC Requirements for Serial RapidIO SD_REF_CLK and SD_REF_CLK"

13.2.4.1 Spread Spectrum Clock

SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ were designed to work with a spread spectrum clock (+0 to –0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock. For better results, a source without significant unintended modulation should be used.

13.3 SerDes Transmitter and Receiver Reference Circuits

Figure 48 shows the reference circuits for SerDes data lane's transmitter and receiver.

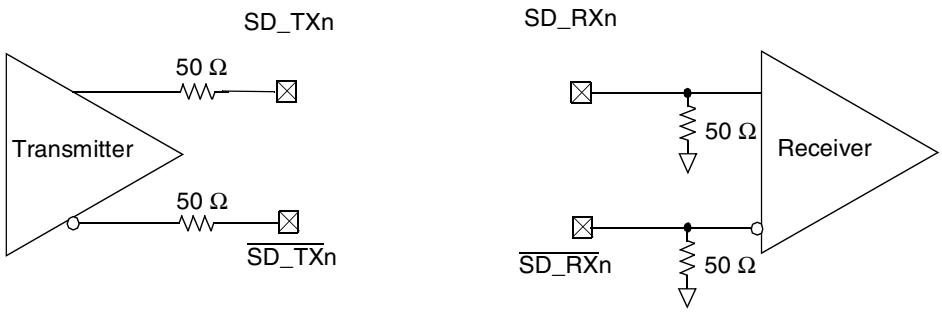


Figure 48. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below (PCI Express, Serial Rapid IO or SGMII) in this document based on the application usage:

- Section 14, "PCI Express"
- Section 15, "Serial RapidIO"

Note that external AC Coupling capacitor is required for the above three serial transmission protocols with the capacitor value defined in specification of each protocol section.

14 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the MPC8568E.

14.1 DC Requirements for PCI Express SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

For more information, see Section 13, "High-Speed Serial Interfaces (HSSI)."

14.2 AC Requirements for PCI Express SerDes Clocks

Table 50 lists AC requirements.

Table 50. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Notes
t_{REF}	REFCLK cycle time	—	10	—	ns	1
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps	—

Table 50. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Notes
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–50	—	50	ps	—

Notes:
1. Typical based on PCI Express Specification 2.0.

14.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a +/– 300 ppm tolerance.

14.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the Transport and Data Link layer please use the PCI EXPRESS Base Specification. REV. 1.0a document.

14.4.1 Differential Transmitter (TX) Output

Table 51 defines the specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 51. Differential Transmitter (TX) Output Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
$V_{TX\text{-}DIFFp\text{-}p}$	Differential Peak-to-Peak Output Voltage	0.8	—	1.2	V	$V_{TX\text{-}DIFFp\text{-}p} = 2*\lvert V_{TX\text{-}D+} - V_{TX\text{-}D-}\rvert$ See Note 2.
$V_{TX\text{-}DE\text{-}RATIO}$	De- Emphasized Differential Output Voltage (Ratio)	–3.0	–3.5	–4.0	dB	Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition. See Note 2.
$T_{TX\text{-}EYE}$	Minimum TX Eye Width	0.70	—	—	UI	The maximum Transmitter jitter can be derived as $T_{TX\text{-}MAX\text{-}JITTER} = 1 - T_{TX\text{-}EYE} = 0.3$ UI. See Notes 2 and 3.
$T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX\text{-}DIFFp\text{-}p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3.
$T_{TX\text{-}RISE}$, $T_{TX\text{-}FALL}$	D+/D- TX Output Rise/Fall Time	0.125	—	—	UI	See Notes 2 and 5

Table 51. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$V_{TX-CM-ACp}$	RMS AC Peak Common Mode Output Voltage	—	—	20	mV	$V_{TX-CM-ACp}$ = RMS($\|V_{TXD+} + V_{TXD-}\|/2 - V_{TX-CM-DC}$) $V_{TX-CM-DC}$ = $DC_{(avg)}$ of $\|V_{TX-D+} + V_{TX-D-}\|/2$ See Note 2
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	0	—	100	mV	$\|V_{TX-CM-DC\ (during\ L0)} - V_{TX-CM-Idle-DC\ (During\ Electrical\ Idle)}\|$<=100 mV $V_{TX-CM-DC}$ = $DC_{(avg)}$ of $\|V_{TX-D+} + V_{TX-D-}\|/2$ [L0] $V_{TX-CM-Idle-DC}$ = $DC_{(avg)}$ of $\|V_{TX-D+} + V_{TX-D-}\|/2$ [Electrical Idle] See Note 2.
$V_{TX-CM-DC-LINE-DELTA}$	Absolute Delta of DC Common Mode between D+ and D–	0	—	25	mV	$\|V_{TX-CM-DC-D+} - V_{TX-CM-DC-D-}\|$ <= 25 mV $V_{TX-CM-DC-D+}$ = $DC_{(avg)}$ of $\|V_{TX-D+}\|$ $V_{TX-CM-DC-D-}$ = $DC_{(avg)}$ of $\|V_{TX-D-}\|$ See Note 2.
$V_{TX-IDLE-DIFFp}$	Electrical Idle differential Peak Output Voltage	0	—	20	mV	$V_{TX-IDLE-DIFFp}$ = $\|V_{TX-IDLE-D+} - V_{TX-IDLE-D-}\|$ <= 20 mV See Note 2.
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during Receiver Detection	—	—	600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance Receiver is present. See Note 6.
$V_{TX-DC-CM}$	The TX DC Common Mode Voltage	0	—	3.6	V	The allowed DC Common Mode voltage under any conditions. See Note 6.
$I_{TX-SHORT}$	TX Short Circuit Current Limit	—	—	90	mA	The total current the Transmitter can provide when shorted to its ground
$T_{TX-IDLE-MIN}$	Minimum time spent in Electrical Idle	50	—	—	UI	Minimum time a Transmitter must be in Electrical Idle Utilized by the Receiver to start looking for an Electrical Idle Exit after successfully receiving an Electrical Idle ordered set
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid Electrical idle after sending an Electrical Idle ordered set	—	—	20	UI	After sending an Electrical Idle ordered set, the Transmitter must meet all Electrical Idle Specifications within this time. This is considered a debounce time for the Transmitter to meet Electrical Idle after transitioning from L0.
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition to valid TX specifications after leaving an Electrical idle condition	—	—	20	UI	Maximum time to meet all TX specifications when transitioning from Electrical Idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving Electrical Idle
$RL_{TX-DIFF}$	Differential Return Loss	10	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4

Table 51. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
RL_{TX-CM}	Common Mode Return Loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	Ω	TX DC Differential mode Low Impedance
Z_{TX-DC}	Transmitter DC Impedance	40	—	—	Ω	Required TX D+ as well as D- DC Impedance during all states
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	—	—	500 + 2 UI	ps	Static skew between any two Transmitter Lanes within a single Link
C_{TX}	AC Coupling Capacitor	75	—	200	nF	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See note 8.
$T_{crosslink}$	Crosslink Random Timeout	0	—	1	ms	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one Downstream and one Upstream Port. See Note 7.

Notes:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 51 and measured over any 250 consecutive TX UIs. (Also refer to the transmitter compliance eye diagram shown in Figure 49)
3. A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.30 UI for the Transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The Transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 ohm probes—see Figure 51). Note that the series capacitors C_{TX} is optional for the return loss measurement.
5. Measured between 20-80% at transmitter package pins into a test load as shown in Figure 51 for both V_{TX-D+} and V_{TX-D-}.
6. See Section 4.3.1.8 of the PCI Express Base Specifications Rev 1.0a
7. See Section 4.2.6.3 of the PCI Express Base Specifications Rev 1.0a
8. MPC8568E SerDes transmitter does not have C_{TX} built-in. An external AC Coupling capacitor is required.

14.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in Figure 49 is specified using the passive compliance/test measurement load (see Figure 51) in place of any real PCI Express interconnect + RX component.

There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams will differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit will always be relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (that is, least squares and median deviation fits).

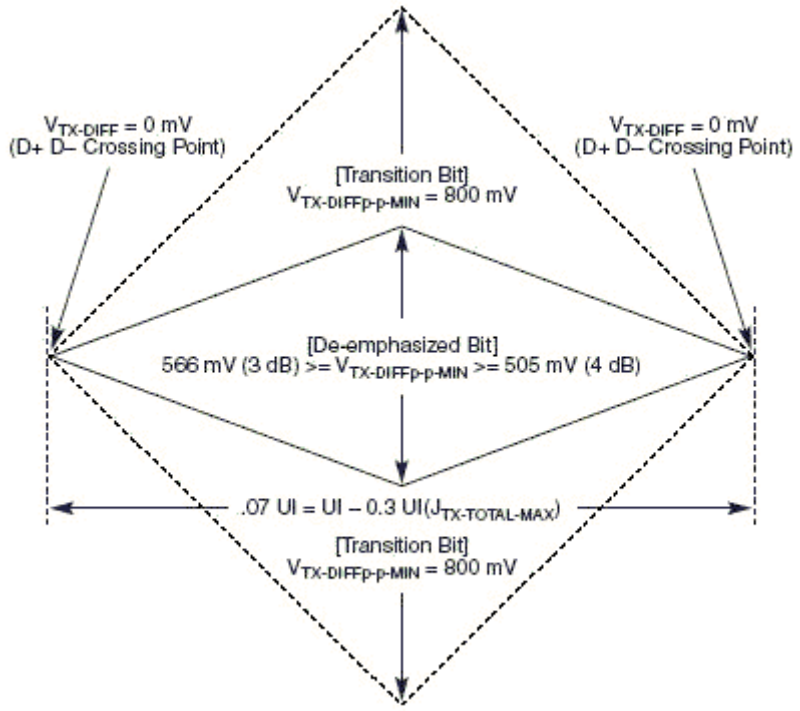


Figure 49. Minimum Transmitter Timing and Voltage Output Compliance Specifications

14.4.3 Differential Receiver (RX) Input Specifications

Table 52 defines the specifications for the differential input at all receivers (RXs). The parameters are specified at the component pins.

Table 52. Differential Receiver (RX) Input Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit Interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
$V_{RX-DIFFp-p}$	Differential Peak-to-Peak Output Voltage	0.175	—	1.200	V	$V_{RX-DIFFp-p} = 2*\|V_{RX-D+} - V_{RX-D-}\|$ See Note 2.

Table 52. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
T_{RX-EYE}	Minimum Receiver Eye Width	0.4	—	—	UI	The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER}$ = 1 – T_{RX-EYE}= 0.6 UI. See Notes 2 and 3.
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3 and 7.
$V_{RX-CM-ACp}$	AC Peak Common Mode Input Voltage	—	—	150	mV	$V_{RX-CM-ACp}$ = $\lvert V_{RXD+} + V_{RXD-}\rvert/2 - V_{RX-CM-DC}$ $V_{RX-CM-DC}$ = $DC_{(avg)}$ of $\lvert V_{RX-D+} + V_{RX-D-}\rvert/2$ See Note 2
$RL_{RX-DIFF}$	Differential Return Loss	10	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at +300 mV and -300 mV, respectively. See Note 4
RL_{RX-CM}	Common Mode Return Loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D- lines biased at 0 V. See Note 4
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	Ω	RX DC Differential mode impedance. See Note 5
Z_{RX-DC}	DC Input Impedance	40	50	60	Ω	Required RX D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 2 and 5.
$Z_{RX-HIGH-IMP-DC}$	Powered Down DC Input Impedance	200 k	—	—	Ω	Required RX D+ as well as D- DC Impedance when the Receiver terminations do not have power. See Note 6.
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p}$ = $2*\lvert V_{RX-D+} - V_{RX-D-}\rvert$ Measured at the package pins of the Receiver
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	—	—	10	ms	An unexpected Electrical Idle ($V_{RX-DIFFp-p}$ < $V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition.

Table 52. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
$L_{TX-SKEW}$	Total Skew	—	—	20	ns	Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (for example, COM and one to five Symbols) at the RX as well as any delay differences arising from the interconnect itself.

Notes:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 51 should be used as the RX device when taking measurements (also refer to the Receiver compliance eye diagram shown in Figure 50). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. The Receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D- line biased to -300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 ohms to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 ohm probes—see Figure 51). Note: that the series capacitors CTX is optional for the return loss measurement.
5. Impedance during all LTSSM states. When transitioning from a Fundamental Reset to Detect (the initial state of the LTSSM) there is a 5 ms transition time before Receiver termination values must be met on all un-configured Lanes of a Port.
6. The RX DC Common Mode Impedance that exists when no power is present or Fundamental Reset is asserted. This helps ensure that the Receiver Detect circuit will not falsely assume a Receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

14.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 50 is specified using the passive compliance/test measurement load (see Figure 51) in place of any real PCI Express RX component.

Note: In general, the minimum Receiver eye diagram measured with the compliance/test measurement load (see Figure 51) will be larger than the minimum Receiver eye diagram measured over a range of systems at the input Receiver of any real PCI Express component. The degraded eye diagram at the input Receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input Receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum Receiver eye diagram (shown in Figure 50) expected at the input Receiver based on some adequate combination of system simulations and the Return Loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50. to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50. probes—see Figure 51). Note that the series capacitors, CTX, are optional for the return loss measurement.

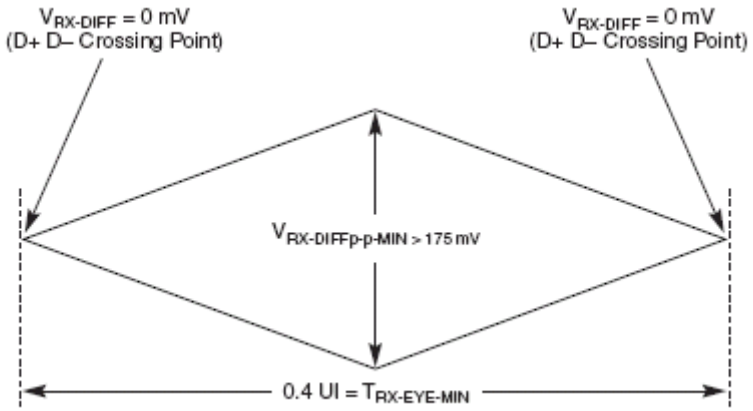


Figure 50. Minimum Receiver Eye Timing and Voltage Compliance Specification

14.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 51.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

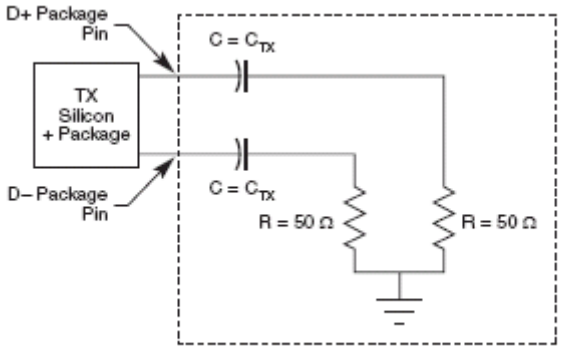


Figure 51. Compliance Test/Measurement Load

15 Serial RapidIO

This section describes the DC and AC electrical specifications for the RapidIO interface of the MPC8568E, for the LP-Serial physical layer. The electrical specifications cover both single and multiple-lane links. Two transmitters (short run and long run) and a single receiver are specified for each of three baud rates, 1.25, 2.50, and 3.125 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that will accept signals from both the short run and long run transmitter specifications.

The short run transmitter should be used mainly for chip-to-chip connections on either the same printed circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short run specification reduce the overall power used by the transceivers.

The long run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The specifications allow a distance of at least 50 cm at all baud rates.

All unit intervals are specified with a tolerance of +/– 100 ppm. The worst case frequency difference between any transmit and receive clock will be 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC coupling at the receiver input must be used.

15.1 DC Requirements for Serial RapidIO SD_REF_CLK and SD_REF_CLK

For more information, see Section 13.2, “SerDes Reference Clocks.”

15.2 AC Requirements for Serial RapidIO SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

Table 50 lists AC requirements.

Table 53. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Units	Comments
t_{REF}	REFCLK cycle time	—	10(8)	—	ns	8 ns applies only to serial RapidIO with 125-MHz reference clock
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	80	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–40	—	40	ps	—

15.3 Signal Definitions

LP-Serial links use differential signaling. This section defines terms used in the description and specification of differential signals. Figure 52 shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and $\overline{\text{TD}}$) or a receiver input (RD and $\overline{\text{RD}}$). Each signal swings between A Volts and B Volts where A > B. Using these waveforms, the definitions are as follows:

7. The transmitter output signals and the receiver input signals TD, $\overline{\text{TD}}$, RD and $\overline{\text{RD}}$ each have a peak-to-peak swing of A – B Volts
8. The differential output signal of the transmitter, V_{OD}, is defined as $V_{TD}–V_{\overline{TD}}$
9. The differential input signal of the receiver, V_{ID}, is defined as $V_{RD}-V_{\overline{RD}}$
10. The differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) Volts
11. The peak value of the differential transmitter output signal and the differential receiver input signal is A – B Volts
12. The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is 2 * (A – B) Volts

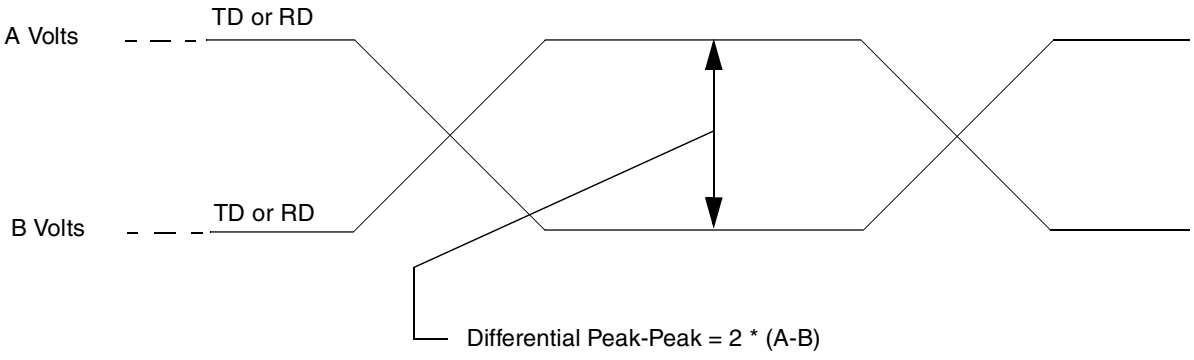


Figure 52. Differential Peak-Peak Voltage of Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{\text{TD}}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of the signals TD and $\overline{\text{TD}}$ is 500 mV p-p. The differential output signal ranges between 500 mV and –500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mV p-p.

15.4 Equalization

With the use of high speed serial links, the interconnect media will cause degradation of the signal at the receiver. Effects such as Inter-Symbol Interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are:

- A passive high pass filter network placed at the receiver. This is often referred to as passive equalization.
- The use of active circuits in the receiver. This is often referred to as adaptive equalization.

15.5 Explanatory Note on Transmitter and Receiver Specifications

AC electrical specifications are given for transmitter and receiver. Long run and short run interfaces at three baud rates (a total of six cases) are described.

The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002.

XAUI has similar application goals to serial RapidIO, as described in Section 8.1. The goal of this standard is that electrical designs for serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.

15.6 Transmitter Specifications

LP-Serial transmitter electrical and timing specifications are stated in the text and tables of this section.

The differential return loss, S11, of the transmitter in each case shall be better than

- –10 dB for (Baud Frequency)/10 < Freq(f) < 625 MHz, and
- –10 dB + 10log(f/625 MHz) dB for 625 MHz ≤ Freq(f) ≤ Baud Frequency

The reference impedance for the differential return loss measurements is 100 Ohm resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

It is recommended that the 20%-80% rise/fall time of the transmitter, as measured at the transmitter output, in each case have a minimum value 60 ps.

It is recommended that the timing skew at the output of an LP-Serial transmitter between the two signals that comprise a differential pair not exceed 25 ps at 1.25 GB, 20 ps at 2.50 GB and 15 ps at 3.125 GB.

Table 54. Short Run Transmitter AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	+/– 100 ppm

Table 55. Short Run Transmitter AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple Output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	+/– 100 ppm

Table 56. Short Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	500	1000	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—

Table 56. Short Run Transmitter AC Timing Specifications—3.125 GBaud (continued)

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	320	320	ps	+/– 100 ppm

Table 57. Long Run Transmitter AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	800	800	ps	+/–100 ppm

Table 58. Long Run Transmitter AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	400	400	ps	+/– 100 ppm

Table 59. Long Run Transmitter AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Output Voltage,	V_O	–0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair
Differential Output Voltage	V_{DIFFPP}	800	1600	mV p-p	—
Deterministic Jitter	J_D	—	0.17	UI p-p	—
Total Jitter	J_T	—	0.35	UI p-p	—
Multiple output skew	S_{MO}	—	1000	ps	Skew at the transmitter output between lanes of a multilane link
Unit Interval	UI	320	320	ps	+/– 100 ppm

For each baud rate at which an LP-Serial transmitter is specified to operate, the output eye pattern of the transmitter shall fall entirely within the unshaded portion of the Transmitter Output Compliance Mask shown in Figure 53 with the parameters specified in Table 60 when measured at the output pins of the device and the device is driving a 100 Ohm +/–5% differential resistive load. The output eye pattern of an LP-Serial transmitter that implements pre-emphasis (to equalize the link and reduce inter-symbol interference) need only comply with the Transmitter Output Compliance Mask when pre-emphasis is disabled or minimized.

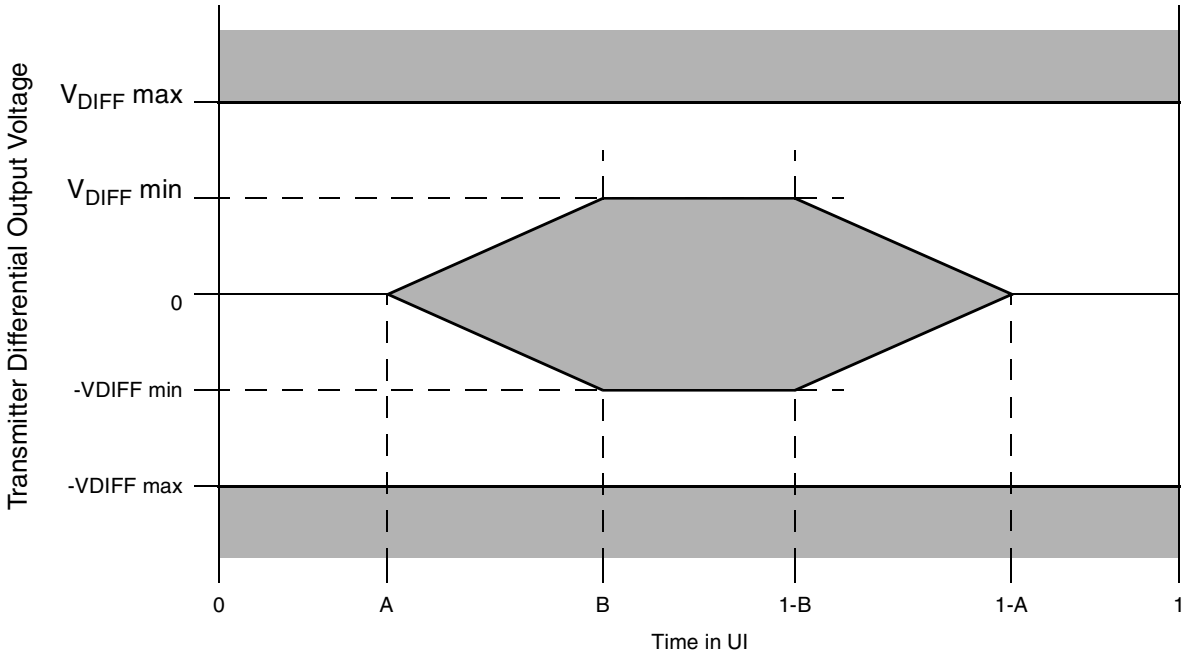


Figure 53. Transmitter Output Compliance Mask

Table 60. Transmitter Differential Output Eye Diagram Parameters

Transmitter Type	V_{DIFF}min (mV)	V_{DIFF}max (mV)	A (UI)	B (UI)
1.25 GBaud short range	250	500	0.175	0.39
1.25 GBaud long range	400	800	0.175	0.39
2.5 GBaud short range	250	500	0.175	0.39
2.5 GBaud long range	400	800	0.175	0.39
3.125 GBaud short range	250	500	0.175	0.39
3.125 GBaud long range	400	800	0.175	0.39

15.7 Receiver Specifications

LP-Serial receiver electrical and timing specifications are stated in the text and tables of this section.

Receiver input impedance shall result in a differential return loss better that 10 dB and a common mode return loss better than 6 dB from 100 MHz to (0.8)*(Baud Frequency). This includes contributions from on-chip circuitry, the chip package and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100 Ω resistive for differential return loss and 25 Ω resistive for common mode.

Table 61. Receiver AC Timing Specifications—1.25 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37	—	UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55	—	UI p-p	Measured at receiver
Total Jitter Tolerance[1]	J_T	0.65	—	UI p-p	Measured at receiver
Multiple Input Skew	S_{MI}	—	24	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER	—	10^{-12}	—	—
Unit Interval	UI	800	800	ps	+/– 100 ppm

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 54. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

Table 62. Receiver AC Timing Specifications—2.5 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37	—	UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55	—	UI p-p	Measured at receiver
Total Jitter Tolerance[1]	J_T	0.65	—	UI p-p	Measured at receiver
Multiple Input Skew	S_{MI}	—	24	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER	—	10^{-12}	—	—
Unit Interval	UI	400	400	ps	+/– 100 ppm

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 54. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

Table 63. Receiver AC Timing Specifications—3.125 GBaud

Characteristic	Symbol	Range		Unit	Notes
		Min	Max		
Differential Input Voltage	V_{IN}	200	1600	mV p-p	Measured at receiver
Deterministic Jitter Tolerance	J_D	0.37	—	UI p-p	Measured at receiver
Combined Deterministic and Random Jitter Tolerance	J_{DR}	0.55	—	UI p-p	Measured at receiver
Total Jitter Tolerance[1]	J_T	0.65	—	UI p-p	Measured at receiver
Multiple Input Skew	S_{MI}	—	22	ns	Skew at the receiver input between lanes of a multilane link
Bit Error Rate	BER	—	10^{-12}	—	—
Unit Interval	UI	320	320	ps	+/- 100 ppm

Note:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 54. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

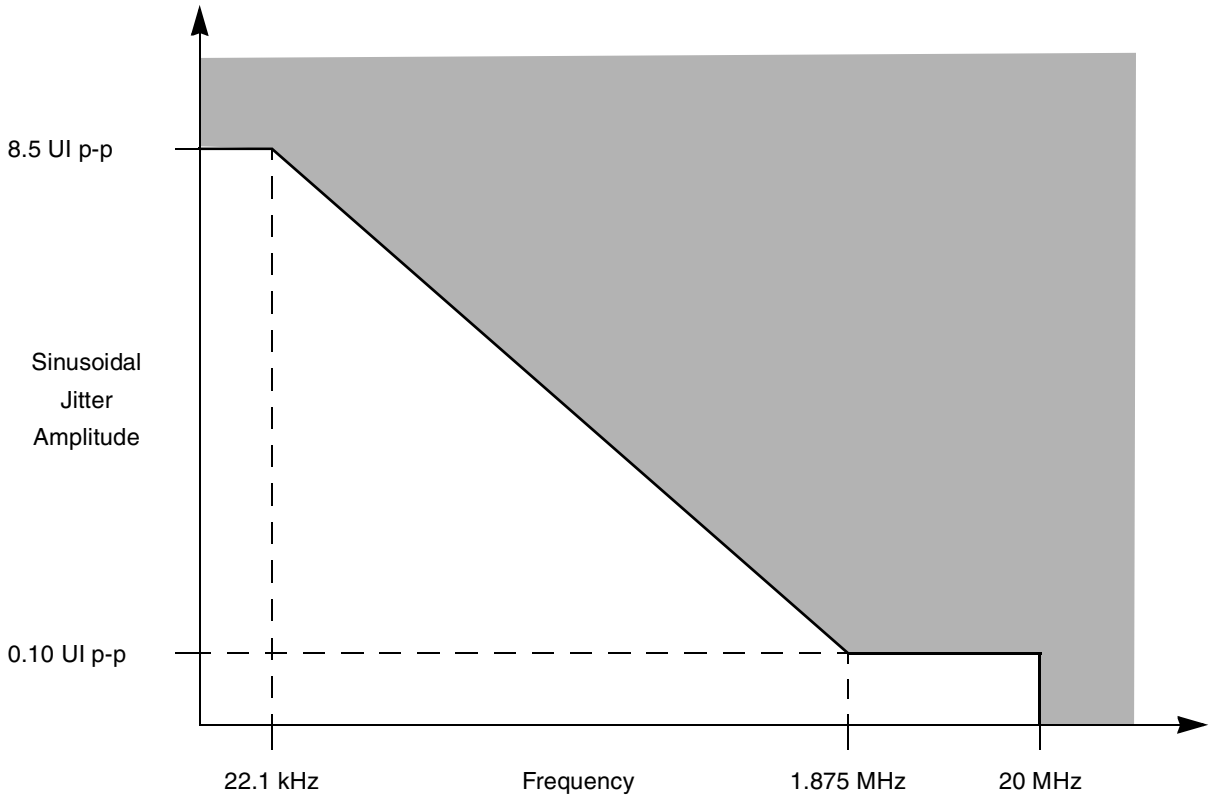


Figure 54. Single Frequency Sinusoidal Jitter Limits

15.8 Receiver Eye Diagrams

For each baud rate at which an LP-Serial receiver is specified to operate, the receiver shall meet the corresponding Bit Error Rate specification (Table 61, Table 62, Table 63) when the eye pattern of the receiver test signal (exclusive of sinusoidal jitter) falls entirely within the unshaded portion of the Receiver Input Compliance Mask shown in Figure 55 with the parameters specified in Table . The eye pattern of the receiver test signal is measured at the input pins of the receiving device with the device replaced with a 100 Ω +/– 5% differential resistive load.

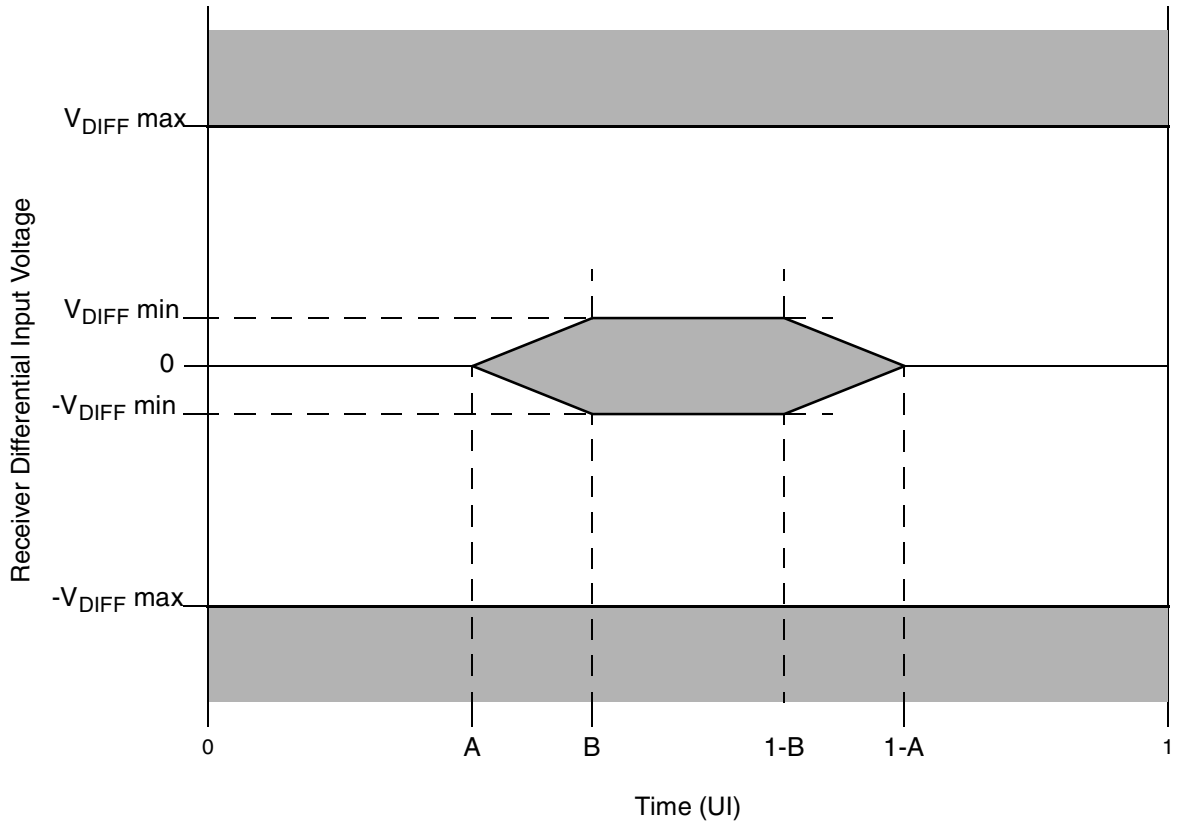


Figure 55. Receiver Input Compliance Mask

Table 64. Receiver Input Compliance Mask Parameters Exclusive of Sinusoidal Jitter

Receiver Type	V_{DIFF}min (mV)	V_{DIFF}max (mV)	A (UI)	B (UI)
1.25 GBaud	100	800	0.275	0.400
2.5 GBaud	100	800	0.275	0.400
3.125 GBaud	100	800	0.275	0.400

15.9 Measurement and Test Requirements

Since the LP-Serial electrical specification are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002, the measurement and test requirements defined here are similarly guided by Clause 47. In addition, the CJPAT test pattern defined in Annex 48A of IEEE 802.3ae-2002 is specified as the test pattern for use in eye pattern and jitter measurements. Annex 48B of IEEE 802.3ae-2002 is recommended as a reference for additional information on jitter test methods.

15.9.1 Eye Template Measurements

For the purpose of eye template measurements, the effects of a single-pole high pass filter with a 3 dB point at (Baud Frequency)/1667 is applied to the jitter. The data pattern for template measurements is the

Continuous Jitter Test Pattern (CJPAT) defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. The amount of data represented in the eye shall be adequate to ensure that the bit error ratio is less than 10^{-12}. The eye pattern shall be measured with AC coupling and the compliance template centered at 0 Volts differential. The left and right edges of the template shall be aligned with the mean zero crossing points of the measured data eye. The load for this test shall be 100 Ohms resistive +/– 5% differential to 2.5 GHz.

15.9.2 Jitter Test Measurements

For the purpose of jitter measurement, the effects of a single-pole high pass filter with a 3 dB point at (Baud Frequency)/1667 is applied to the jitter. The data pattern for jitter measurements is the Continuous Jitter Test Pattern (CJPAT) pattern defined in Annex 48A of IEEE 802.3ae. All lanes of the LP-Serial link shall be active in both the transmit and receive directions, and opposite ends of the links shall use asynchronous clocks. Four lane implementations shall use CJPAT as defined in Annex 48A. Single lane implementations shall use the CJPAT sequence specified in Annex 48A for transmission on lane 0. Jitter shall be measured with AC coupling and at 0 Volts differential. Jitter measurement for the transmitter (or for calibration of a jitter tolerance setup) shall be performed with a test procedure resulting in a BER curve such as that described in Annex 48B of IEEE 802.3ae.

15.9.3 Transmit Jitter

Transmit jitter is measured at the driver output when terminated into a load of 100 Ohms resistive +/– 5% differential to 2.5 GHz.

15.9.4 Jitter Tolerance

Jitter tolerance is measured at the receiver using a jitter tolerance test signal. This signal is obtained by first producing the sum of deterministic and random jitter defined in and then adjusting the signal amplitude until the data eye contacts the 6 points of the minimum eye opening of the receive template shown in and . Note that for this to occur, the test signal must have vertical waveform symmetry about the average value and have horizontal symmetry (including jitter) about the mean zero crossing. Eye template measurement requirements are as defined above. Random jitter is calibrated using a high pass filter with a low frequency corner at 20 MHz and a 20 dB/decade roll-off below this. The required sinusoidal jitter specified in is then added to the signal and the test load is replaced by the receiver being tested.

16 Timers

This section describes the DC and AC electrical specifications for the timers of the MPC8568E.

16.1 Timers DC Electrical Characteristics

Table 65 provides the DC electrical characteristics for the MPC8568E timers pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$ and RTC_CLK.

Table 65. Timers DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD}+0.3	V
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	± 10	µA

16.2 Timers AC Timing Specifications

Table 66 provides the timers input and output AC timing specifications.

Table 66. Timers Input AC Timing Specifications [1]

Characteristic	Symbol [2]	Typ	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:

1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs should be synchronized before use by any external synchronous logic. Timers inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation

Figure 56 provides the AC test load for the timers.

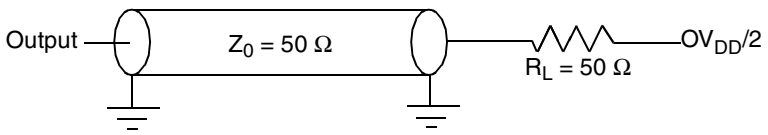


Figure 56. Timers AC Test Load

17 PIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the MPC8568E.

17.1 PIC DC Electrical Characteristics

Table 67 provides the DC electrical characteristics for the external interrupt pins of the MPC8568E.

Table 67. PIC DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD}+0.3	V
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	—		±10	μA
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Notes:
1. This table applies for pins $\overline{\text{IRQ}}$[0:7], $\overline{\text{IRQ\_OUT}}$, $\overline{\text{MCP\_OUT}}$, and CE ports Interrupts.
2. $\overline{\text{IRQ\_OUT}}$ and $\overline{\text{MCP\_OUT}}$ are open drain pins, thus V_{OH} is not relevant for those pins.

17.2 PIC AC Timing Specifications

Table 68 provides the PIC input and output AC timing specifications.

Table 68. PIC Input AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

Notes:
1. Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.
2. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least tPIWID ns to ensure proper operation when working in edge triggered mode.

18 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8568E.

18.1 SPI DC Electrical Characteristics

Table 69 provides the DC electrical characteristics for the MPC8568E SPI.

Table 69. SPI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –6.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	OV_{DD}+0.3	V
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	± 10	μA

18.2 SPI AC Timing Specifications

Table 70 and provide the SPI input and output AC timing specifications.

Table 70. SPI AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Max	Unit
SPI outputs—Master mode (internal clock) delay	t_{NIKHOV}	0	6	ns
SPI outputs—Slave mode (external clock) delay	t_{NEKHOV}	2	8	ns
SPI inputs—Master mode (internal clock) input setup time	t_{NIIVKH}	4	—	ns
SPI inputs—Master mode (internal clock) input hold time	t_{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t_{NEIVKH}	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t_{NEIXKH}	2	—	ns

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).

Figure 57 provides the AC test load for the SPI.

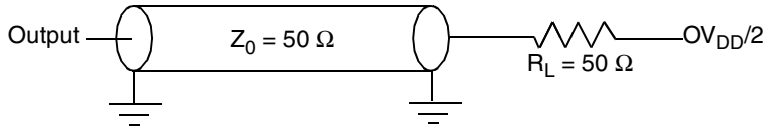
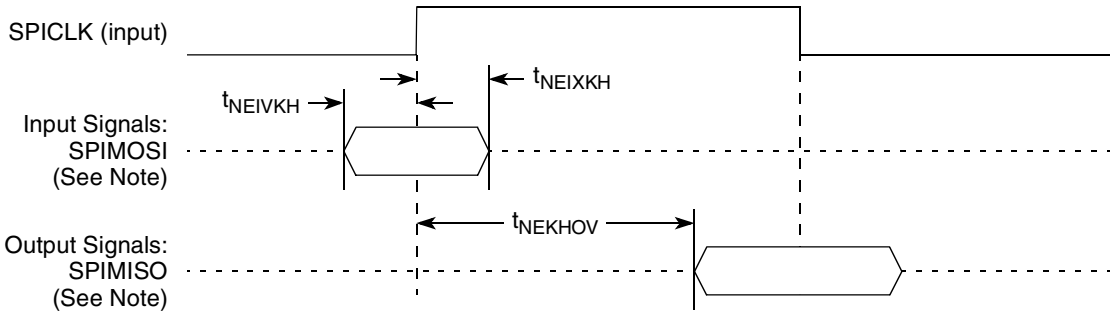


Figure 57. SPI AC Test Load

Figure 58 through Figure 59 represent the AC timing from Table 72. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

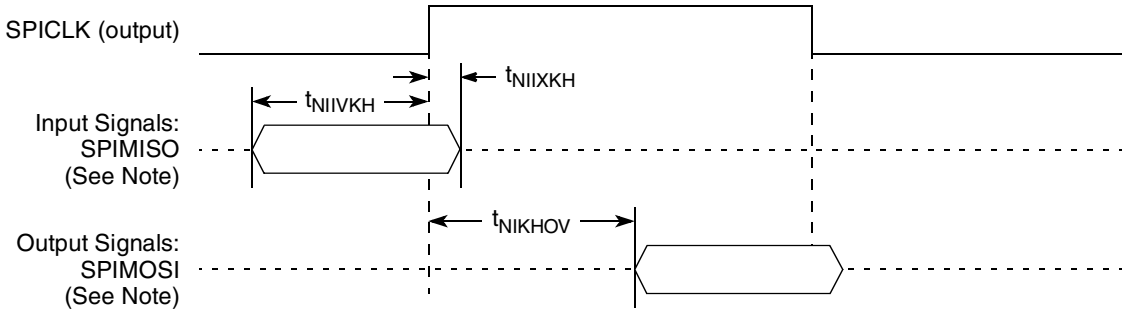
Figure 58 shows the SPI timing in Slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 58. SPI AC Timing in Slave mode (External Clock) Diagram

Figure 59 shows the SPI timing in Master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 59. SPI AC Timing in Master mode (Internal Clock) Diagram

19 TDM/SI

This section describes the DC and AC electrical specifications for the time-division-multiplexed and serial interface of the MPC8568E.

19.1 TDM/SI DC Electrical Characteristics

Table 71 provides the DC electrical characteristics for the MPC8568E TDM/SI.

Table 71. TDM/SI DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –2.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD}+0.3	V

Table 71. TDM/SI DC Electrical Characteristics (continued)

Characteristic	Symbol	Condition	Min	Max	Unit
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$	—	± 10	μA

19.2 TDM/SI AC Timing Specifications

Table 72 provides the TDM/SI input and output AC timing specifications.

Table 72. TDM/SI AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Max	Unit
TDM/SI outputs—External clock delay	t_{SEKHOV}	2	11	ns
TDM/SI outputs—External clock High Impedance	t_{SEKHOX}	2	10	ns
TDM/SI inputs—External clock input setup time	t_{SEIVKH}	5	—	ns
TDM/SI inputs—External clock input hold time	t_{SEIXKH}	2	—	ns

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{SEKHOX} symbolizes the TDM/SI outputs external timing (SE) for the time $t_{TDM/SI}$ memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 60 provides the AC test load for the TDM/SI.

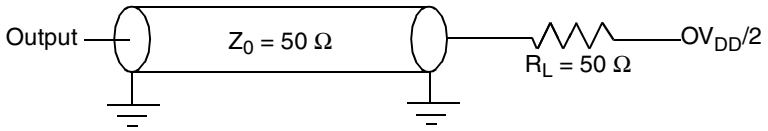
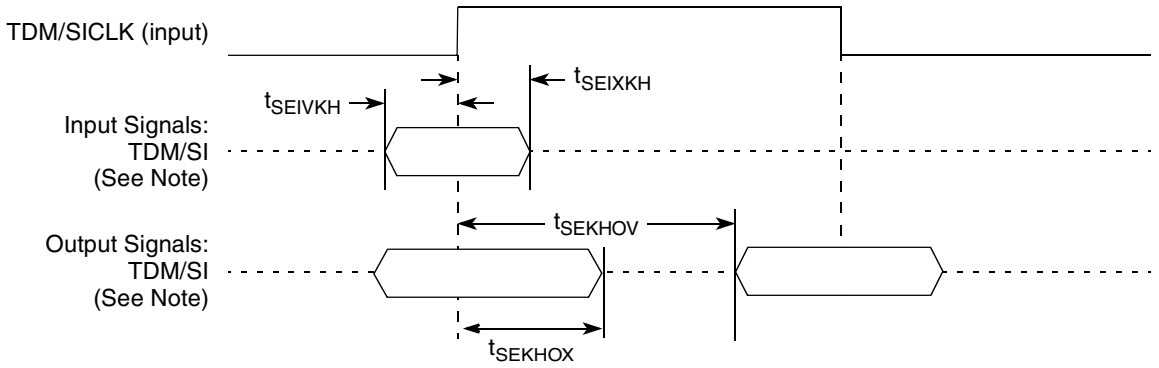


Figure 60. TDM/SI AC Test Load

Figure 61 represents the AC timing from Table 72. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 61 shows the TDM/SI timing with external clock.



Note: The clock edge is selectable on TDM/SI

Figure 61. TDM/SI AC Timing (External Clock) Diagram

20 UTOPIA/POS

This section describes the DC and AC electrical specifications for the UTOPIA-packet over sonnet of the MPC8568E.

20.1 UTOPIA/POS DC Electrical Characteristics

Table 73 provides the DC electrical characteristics for the MPC8568E UTOPIA.

Table 73. Utopia DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD}+0.3	V
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ OV_{DD}	—	± 10	μA

20.2 Utopia/POS AC Timing Specifications

Table 74 provides the UTOPIA input and output AC timing specifications.

Table 74. Utopia AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Max	Unit
Utopia outputs—Internal clock delay	t_{UIKHOV}	0	8.0	ns
Utopia outputs—External clock delay	t_{UEKHOV}	1	10.0	ns
Utopia outputs—Internal clock High Impedance	t_{UIKHOX}	0	8.0	ns
Utopia outputs—External clock High Impedance	t_{UEKHOX}	1	10.0	ns

Table 74. Utopia AC Timing Specifications [1] (continued)

Characteristic	Symbol [2]	Min	Max	Unit
Utopia inputs—Internal clock input setup time	t_{UIIVKH}	6	—	ns
Utopia inputs—External clock input setup time	t_{UEIVKH}	4	—	ns
Utopia inputs—Internal clock input Hold time	t_{UIIXKH}	0	—	ns
Utopia inputs—External clock input hold time	t_{UEIXKH}	1	—	ns

Notes:

1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{UIKHOX} symbolizes the Utopia outputs internal timing (UI) for the time t_{Utopia} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 62 provides the AC test load for the Utopia.

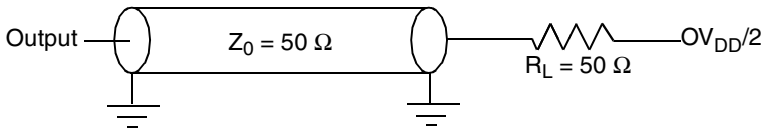


Figure 62. Utopia AC Test Load

Figure 63 through Figure 64 represent the AC timing from Table 74. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 63 shows the Utopia timing with external clock.

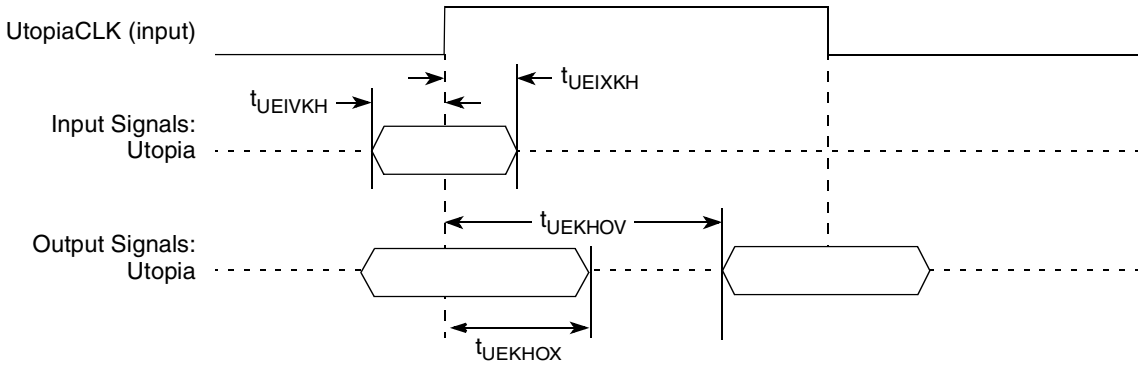


Figure 63. Utopia AC Timing (External Clock) Diagram

Figure 64 shows the Utopia timing with internal clock.

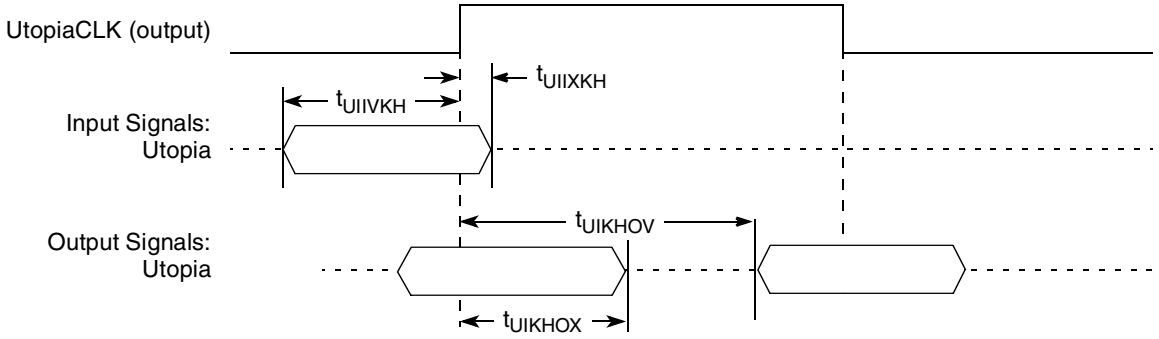


Figure 64. Utopia AC Timing (Internal Clock) Diagram

21 HDLC, BISYNC, Transparent and Synchronous UART

This section describes the DC and AC electrical specifications for the high level data link control (HDLC), BISYNC, transparent and synchronous UART of the MPC8568E.

21.1 HDLC, BISYNC, Transparent and Synchronous UART DC Electrical Characteristics

Table 75 provides the DC electrical characteristics for the MPC8568E HDLC, BISYNC, Transparent and Synchronous UART protocols.

Table 75. HDLC, BiSync, Transparent and Synchronous UART DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –2.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.5	V
Input high voltage	V_{IH}	—	2.0	OV_{DD}+0.3	V
Input low voltage	V_{IL}	—	-0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le OV_{DD}$	—	± 10	μA

21.2 HDLC, BISYNC, Transparent and Synchronous UART AC Timing Specifications

Table 76 provides the input and output AC timing specifications for HDLC, BiSync, Transparent and Synchronous UART protocols.

Table 76. HDLC, BiSync, Transparent AC Timing Specifications [1]

Characteristic	Symbol [2]	Min	Max	Unit
Outputs—Internal clock delay	t_{HIKHOV}	0	6.5	ns
Outputs—External clock delay	t_{HEKHOV}	1	8	ns

Table 76. HDLC, BiSync, Transparent AC Timing Specifications [1] (continued)

Characteristic	Symbol [2]	Min	Max	Unit
Outputs—Internal clock High Impedance	t_{HIKHOX}	0	5.5	ns
Outputs—External clock High Impedance	t_{HEKHOX}	1	8	ns
Inputs—Internal clock input setup time	t_{HIIVKH}	6	—	ns
Inputs—External clock input setup time	t_{HEIVKH}	4	—	ns
Inputs—Internal clock input Hold time	t_{HIIXKH}	0	—	ns
Inputs—External clock input hold time	t_{HEIXKH}	1	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Table 77. Synchronous UART AC Timing Specifications

Characteristic	Symbol [2]	Min	Max	Unit
Outputs—Internal clock delay	t_{HIKHOV}	0	11	ns
Outputs—External clock delay	t_{HEKHOV}	1	14	ns
Outputs—Internal clock High Impedance	t_{HIKHOX}	0	11	ns
Outputs—External clock High Impedance	t_{HEKHOX}	1	14	ns
Inputs—Internal clock input setup time	t_{HIIVKH}	6	—	ns
Inputs—External clock input setup time	t_{HEIVKH}	8	—	ns
Inputs—Internal clock input Hold time	t_{HIIXKH}	0	—	ns
Inputs—External clock input hold time	t_{HEIXKH}	1	—	ns

Notes:
1. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{HIKHOX} symbolizes the outputs internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).

Figure 65 provides the AC test load.

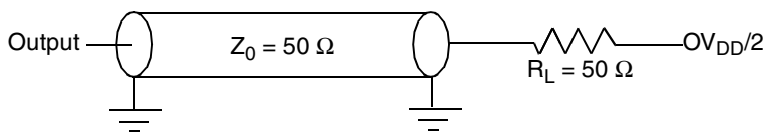
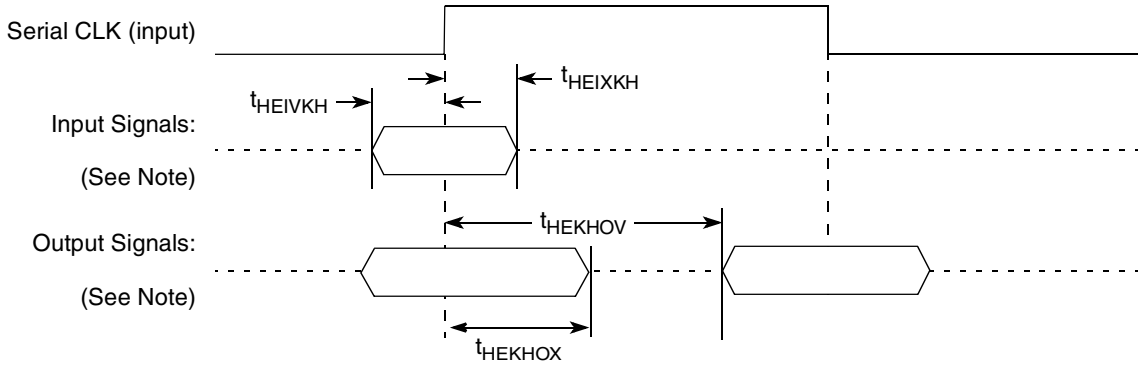


Figure 65. AC Test Load

Figure 66 through Figure 67 represent the AC timing from Table 76. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

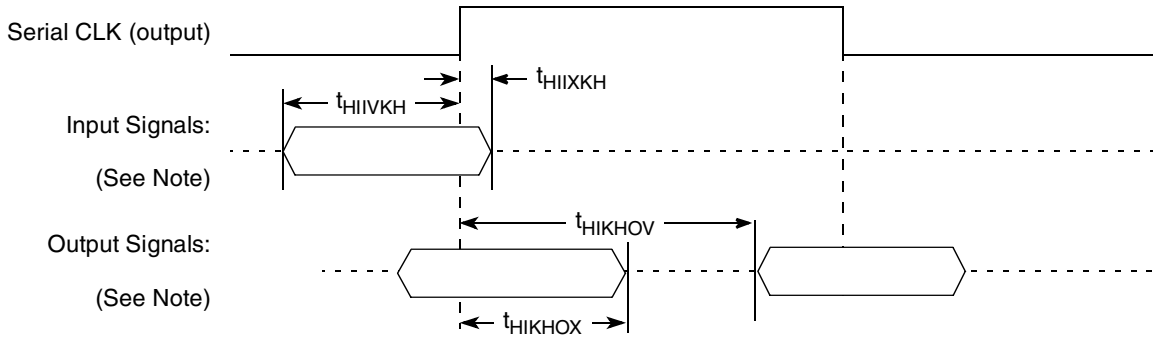
Figure 66 shows the timing with external clock.



Note: The clock edge is selectable

Figure 66. AC Timing (External Clock) Diagram

Figure 67 shows the timing with internal clock.



Note: The clock edge is selectable

Figure 67. AC Timing (Internal Clock) Diagram

22 Package and Pinout

This section details package parameters, pin assignments, and dimensions.

22.1 Package Parameters for the MPC8568E FC-PBGA

The package parameters are as provided in the following list. The package type is 33mm × 33mm, 1023 flip chip plastic ball grid array (FC-PBGA).

Package outline	33 mm × 33 mm
Interconnects	1023
Pitch	1 mm
Module height	2.23 – 2.75 mm
Solder Balls	96.5% Sn 3.5% Ag
Ball diameter (typical)	0.6 mm

22.2 Mechanical Dimensions of the MPC8568E FC-PBGA

Figure 68 shows the top view, bottom and side view of the MPC8568E 1023 FC-PBGA package.

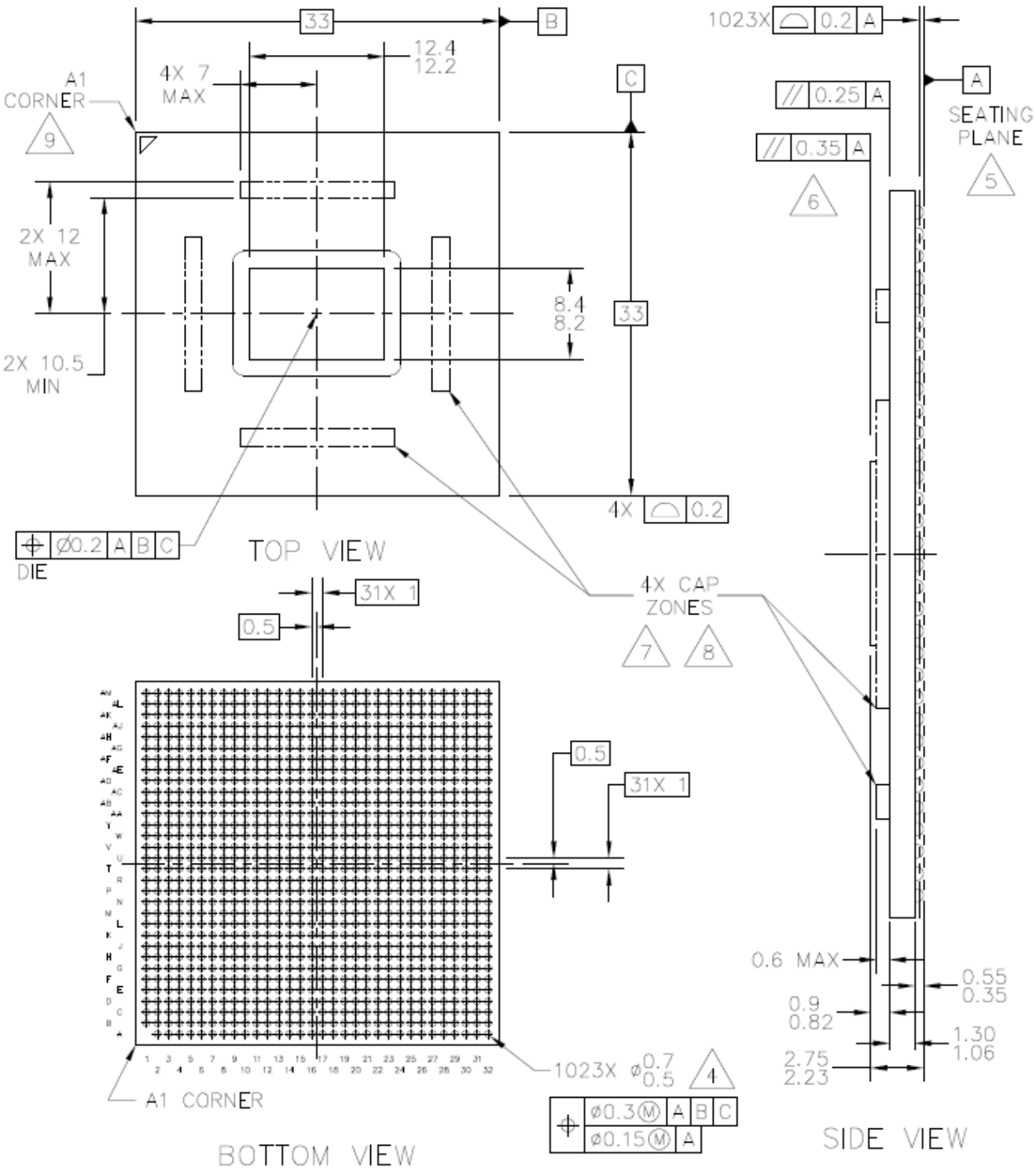


Figure 68. Top, Bottom, Side Views

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. All dimensions are symmetric across the package center lines, unless dimensioned otherwise.

4. Maximum solder ball diameter measured parallel to datum A.
5. Datum A, the seating plane, is defined by the spherical crowns of the solder balls.
6. ParalleUsm measurement shall exclude any effect of mark on top surface of package
7. Capacitors may not be present on all devices.
8. Caution must be taken not to short capacitors or exposed metal capacitor pads on top of package.

22.3 Pinout Listings

Some of the non-QE signals are multiplexed with QE port pins, as follows:

PC[0] UART_SOUT[1]
PC[1] $\overline{\text{UART\_RTS}}$[1]
PC[2] $\overline{\text{UART\_CTS}}$[1]
PC[3] UART_SIN[1]

PC[11] IRQ[8]
PC[12] IRQ[9]/$\overline{\text{DMA\_DREQ}}$[3]
PC[13] IRQ[10]/$\overline{\text{DMA\_DACK}}$[3]
PC[14] IRQ[11]/$\overline{\text{DMA\_DDONE}}$[3]
PC[15] $\overline{\text{DMA\_DREQ}}$[1]
PC[16] $\overline{\text{DMA\_DACK}}$[1]
PC[17] $\overline{\text{DMA\_DDONE}}$[1]
PC[18] IIC2_SCL
PC[19] IIC2_SDA

PD[28] UART_SOUT[1]
PD[29] $\overline{\text{UART\_RTS}}$[1]
PD[30] $\overline{\text{UART\_CTS}}$[1]
PD[31] UART_SIN[1]

This applies to both MPC8568E and MPC8568E. Note that for DUART1, there are two options. DUART0 is multiplexed with PCI Req/Grant pins.

$\overline{\text{PCI\_REQ}}$[3] $\overline{\text{UART\_CTS}}$[0]
$\overline{\text{PCI\_REQ}}$[4] UART_SIN[0]
$\overline{\text{PCI\_GNT}}$[3] $\overline{\text{UART\_RTS}}$[0]
$\overline{\text{PCI\_GNT}}$[4] UART_SOUT[0]

For MPC8568E, GPIO is multiplexed with the TSEC2 interface:

TSEC2_TXD[7:0] GPOUT[0:7]

TSEC2_RXD[7:0] GPIN[0:7]

Other muxing includes:

$\overline{\text{LCS}}$[5] $\overline{\text{DMA\_DREQ}}$[2]

$\overline{\text{LCS}}$[6] $\overline{\text{DMA\_DACK}}$[2]

$\overline{\text{LCS}}$[7] $\overline{\text{DMA\_DDONE}}$[2]

Table 79 provides the pin-out listing for the MPC8568E 1023 FC-PBGA package.

Table 78. MPC8568E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI				
PCI_AD[31:0]	AE19, AG20, AF19, AB20, AC20, AG21, AG22, AB21, AF22, AH22, AE22, AF20, AB22, AE20, AE23, AJ23, AJ24, AF27, AJ26, AE29, AH24, AD24, AE25, AE26, AH27, AG27, AJ25, AE30, AF26, AG26, AF28, AH26	I/O	OV_{DD}	—
PCI_C_$\overline{\text{BE}}$[3:0]	AC22, AD20, AE28, AH25	I/O	OV_{DD}	—
$\overline{\text{PCI\_GNT}}$[4:1]	AF29, AB18, AC18, AD18	O	OV_{DD}	5,9,35
$\overline{\text{PCI\_GNT0}}$	AE18	I/O	OV_{DD}	—
$\overline{\text{PCI\_IRDY}}$	AF23	I/O	OV_{DD}	2
PCI_PAR	AJ22	I/O	OV_{DD}	
$\overline{\text{PCI\_PERR}}$	AF24	I/O	OV_{DD}	2
$\overline{\text{PCI\_SERR}}$	AD22	I/O	OV_{DD}	2,4
$\overline{\text{PCI\_STOP}}$	AE24	I/O	OV_{DD}	2
$\overline{\text{PCI\_TRDY}}$	AK24	I/O	OV_{DD}	2
$\overline{\text{PCI\_REQ}}$[4:1]	AG29, AJ27, AH29, AB17	I	OV_{DD}	—
$\overline{\text{PCI\_REQ[0]}}$	AC17	I/O	OV_{DD}	—
PCI_CLK	AM26	I	OV_{DD}	39
$\overline{\text{PCI\_DEVSEL}}$	AK23	I/O	OV_{DD}	2
$\overline{\text{PCI\_FRAME}}$	AE21	I/O	OV_{DD}	2
PCI_IDSEL	AB19	I	OV_{DD}	—
DDR SDRAM Memory Interface				
MDQ[0:63]	B22, C22, E20, A19, C23, A22, A20, C20, G22, E22, E16, F16, E23, F23, F17, H17, A18, A17, B16, C16, B19, C19, E17, A16, A13, A14, A12, C12, A15, B15, B13, C13, G12, G11, H8, F8, D13, F12, E9, F9, A7, B7, C5, E5, C8, E8, D6, A5, E6, G6, E1, F1, G7, E7, E2, D1, C4, A3, B1, C1, A4, B4, C2, D2	I/O	GV_{DD}	—
MECC[0:7]	C11, E11, D9, A8, D12, A11, A9, C9	I/O	GV_{DD}	—
MDM[0:8]	A21, E21, D18, B14, F11, A6, G5, A2, A10	O	GV_{DD}	—

Table 78. MPC8568E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MDQS[0:8]	D21, G20, C17, D14, E10, C6, F4, C3, C10	I/O	GV_{DD}	—
$\overline{\text{MDQS}}$[0:8]	C21, G21, C18, D15, F10, C7, F5, D3, B10	I/O	GV_{DD}	—
MA[0:15]	K7, H7, L7, J8, K8, L10, H9, K9, H10, G10, L6, K10, K11, H3, J11, J12	O	GV_{DD}	—
MBA[0:2]	K4, H6, L13	O	GV_{DD}	—
$\overline{\text{MWE}}$	K3	O	GV_{DD}	—
$\overline{\text{MCAS}}$	L3	O	GV_{DD}	—
$\overline{\text{MRAS}}$	K6	O	GV_{DD}	—
MCKE[0:3]	L14, G13, K12, J13	O	GV_{DD}	11
$\overline{\text{MCS}}$[0:3]	J5, H2, K5, K2,	O	GV_{DD}	—
MCK[0:5]	G15, F20, E4, F14, E19, G3	O	GV_{DD}	—
$\overline{\text{MCK}}$[0:5]	G14, F19, E3, F13, E18, G2	O	GV_{DD}	—
MODT[0:3]	G4, J1, J4, K1	O	GV_{DD}	—
MDIC[0:1]	G1, H1	I/O	GV_{DD}	36
Local Bus Controller Interface				
LAD[0:31]	M26, C30, F31, L24, G26, D30, M25, L26, D29, G32, G28, K26, B32, M24, G29, L25, E29, J23, B30, A31, J24, K23, H25, H23, F26, C28, B29, E25, D26, G24, A29, E27,	I/O	BV_{DD}	—
LDP[0:3]	G30, J26, H28, E26	I/O	BV_{DD}	—
LA[27]	F29	O	BV_{DD}	5,9
LA[28:31]	H24, C32, F30, H26	O	BV_{DD}	5,7,9
LALE	G31	O	BVdd	8
LBCTL	L27	O	BVdd	8
$\overline{\text{LCS}}$[0:4]	M27, H32, J28, J30, B31	O	BV_{DD}	—
$\overline{\text{LCS5}}$	G25	I/O	BV_{DD}	1
$\overline{\text{LCS6}}$	C29	O	BV_{DD}	1
$\overline{\text{LCS7}}$	A30	O	BV_{DD}	1
$\overline{\text{LWE}}$[0]	H30	O	BV_{DD}	5,9
$\overline{\text{LWE}}$[1]	E28	O	BV_{DD}	5,9
$\overline{\text{LWE}}$[2]	E32	O	BV_{DD}	5,9
$\overline{\text{LWE}}$[3]	G27	O	BV_{DD}	5,9
LGPL0	E30	O	BV_{DD}	5,9
LGPL1	J27	O	BV_{DD}	5,9,46
LGPL2	D32	O	BV_{DD}	5,8,9

Table 78. MPC8568E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LGPL3	J25	O	BV_{DD}	5,9
LGPL4	C25	I/O	BV_{DD}	49
LGPL5	F32	O	BV_{DD}	5,9
LCKE	C31	O	BV_{DD}	—
LCLK[0:2]	C27, C26, D25	O	BV_{DD}	—
LSYNC_IN	A28	I	BV_{DD}	—
LSYNC_OUT	A27	O	BV_{DD}	—
DMA				
$\overline{\text{DMA\_DACK}}$[0]	AM27	O	OV_{DD}	5,9,46
$\overline{\text{DMA\_DREQ}}$[0]	AK28	I	OV_{DD}	—
$\overline{\text{DMA\_DDONE}}$[0]	AK26	O	OV_{DD}	—
Programmable Interrupt Controller				
$\overline{\text{UDE}}$	AG32	I	OV_{DD}	—
$\overline{\text{MCP}}$	AF32	I	OV_{DD}	—
IRQ[0:7]	AD30, AG31, AL30, AF31, AD29, AK30, AG30, AF30	I	OV_{DD}	—
$\overline{\text{IRQ\_OUT}}$	AD28	O	OV_{DD}	2,4
Interface				
EC_MDC	AE17	O	OV_{DD}	5,9
EC_MDIO	AF17	I/O	OV_{DD}	—
Gigabit Reference Clock				
EC_GTX_CLK125	AM14	I	LV_{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_RXD[7:0]	AE14, AM11, AK11, AF11, AJ14, AJ13, AD12, AE13	I	LV_{DD}	—
TSEC1_TXD[7]	AH12	O	LV_{DD}	5, 9
TSEC1_TXD[6:1]	AL13, AL11, AK13, AH13, AG11, AD13	O	LV_{DD}	—
TSEC1_TXD[0]	AM13	O	LV_{DD}	5, 9
TSEC1_COL	AG13	I	LV_{DD}	—
TSEC1_CRS	AB13	I/O	LV_{DD}	20
TSEC1_GTX_CLK	AG12	O	LV_{DD}	—
TSEC1_RX_CLK	AE11	I	LV_{DD}	—
TSEC1_RX_DV	AH11	I	LV_{DD}	—
TSEC1_RX_ER	AM12	I	LV_{DD}	—

Table 78. MPC8568E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSEC1_TX_CLK	AJ11	I	LV_{DD}	—
TSEC1_TX_EN	AC13	O	LV_{DD}	30
TSEC1_TX_ER	AL12	O	LV_{DD}	5,9
Three-Speed Ethernet Controller (Gigabit Ethernet 2)				
TSEC2_RXD[7:0]	AC14, AD15, AB14, AH15, AD14, AH17, AE15, AC15	I	LV_{DD}	—
TSEC2_TXD[7]	AM16	O	LV_{DD}	5, 9
TSEC2_TXD[6:1]	AJ15, AJ17, AF13, AK17, AH16, AG17	O	LV_{DD}	—
TSEC2_TXD[0]	AL15	O	LV_{DD}	5, 9
TSEC2_COL	AB15	I	LV_{DD}	—
TSEC2_CRS	AB16	I/O	LV_{DD}	20
TSEC2_GTX_CLK	AJ16	O	LV_{DD}	—
TSEC2_RX_CLK	AE16	I	LV_{DD}	—
TSEC2_RX_DV	AG15	I	LV_{DD}	—
TSEC2_RX_ER	AF15	I	LV_{DD}	—
TSEC2_TX_CLK	AH14	I	LV_{DD}	—
TSEC2_TX_EN	AM15	O	LV_{DD}	30
TSEC2_TX_ER	AK15	O	LV_{DD}	—
I^2C interface				
IIC1_SCL	AE32	I/O	OV_{DD}	4,27
IIC1_SDA	AD32	I/O	OV_{DD}	4,27
SerDes				
SD_RX[0:7]	L30, M32, N30, P32, U30, V32, W30, Y32	I	SCOREVDD	43,44
$\overline{\text{SD\_RX}}$[0:7]	L29, M31, N29, P31, U29, V31, W29, Y31	I	SCOREVDD	43,44
SD_TX[0:7]	P26, R24, T26, U24, W24, Y26, AA24, AB26	O	XV_{DD}	44
$\overline{\text{SD\_TX}}$[0:7]	P27, R25, T27, U25, W25, Y27, AA25, AB27	O	XV_{DD}	44
SD_PLL_TPD	R32	O	SCOREVDD	24
$\overline{\text{SD\_RX\_CLK}}$	U28	I	XV_{DD}	41,44
$\overline{\text{SD\_RX\_FRM\_CTL}}$	V28	I	XV_{DD}	41,44
Reserved	V26	—	—	48
Reserved	V27	—	—	48
SD_REF_CLK	T32	I	SCOREVDD	44
$\overline{\text{SD\_REF\_CLK}}$	T31	I	SCOREVDD	44

Table 78. MPC8568E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
QUICC Engine				
PA[0:4]	M1, M2, M5, M4, M3	I/O	OV_{DD}	5,17
PA[5]	N3	I/O	OV_{DD}	29
PA[6:31]	M6, M7, M8, N5, M10, N1, M11, M9, P1, N9, N7, R6, R2, P7, P5, R4, P3, P11, P10, P9, R8, R7, R5, R3, R1, T2	I/O	OV_{DD}	—
PB[4:31]	T1, R11, R9, T6, T5, T4, T3, U10, T9, T8, T7, U5, U3, U1, T11, V1, U11, U9, U7, V5, W4, V3, W2, V9, W8, V7, W6, W3	I/O	OV_{DD}	—
PC[0:31]	W1, V11, V10, W11, W9, W7, W5, Y4, Y3, Y2, Y1, Y8, Y7, Y6, Y5, AA1, Y11, AA10, Y9, AA9, AA7, AA5, AA3, AB3, AC2, AB1, AA11, AB7, AC6, AB5, AC4, AB9	I/O	OV_{DD}	—
PD[4:31]	AC8, AD1, AC1, AC7, AB10, AC5, AD3, AD2, AC3, AE4, AF1, AE3, AE1, AD6, AG2, AG1, AD5, AD7, AD4, AH1, AK3, AD8, AF5, AM4, AC9, AL2, AE5, AF3	I/O	OV_{DD}	—
PE[5:7]	AM6, AL5, AL9	I/O	TV_{DD}	—
PE[8:10]	AM9, AM10, AL10	I/O	TV_{DD}	5
PE[11:19]	AJ9, AH10, AM8, AK9, AL7, AL8, AH9, AM7, AH8	I/O	TV_{DD}	—
PE[20]	AH6	I/O	OV_{DD}	—
PE[21:23]	AM1, AE10, AG5	I/O	OV_{DD}	5
PE[24]	AJ1	I/O	OV_{DD}	5
PE[25:31]	AH2, AM2, AE9, AH5, AL1, AD9, AL4	I/O	OV_{DD}	—
PF[7]	AG9	I/O	TV_{DD}	—
PF[8:10]	AF10, AK7, AJ6	I/O	TV_{DD}	5
PF[11:19]	AH7, AF9, AJ7, AJ5, AF7, AG8, AG7, AM5, AK5	I/O	TV_{DD}	—
PF[20]	AK1	I/O	OV_{DD}	—
PF[21:22]	AH3, AL3	I/O	OV_{DD}	5,33
PF[23:31]	AB11, AE7, AJ3, AC11, AG6, AG3, AH4, AM3, AD11	I/O	OV_{DD}	—
System Control				
$\overline{\text{HRESET}}$	AL21	I	OV_{DD}	—
$\overline{\text{HRESET\_REQ}}$	AL23	O	OV_{DD}	29
$\overline{\text{SRESET}}$	AK18	I	OV_{DD}	—
$\overline{\text{CKSTP\_IN}}$	AL17	I	OV_{DD}	—
$\overline{\text{CKSTP\_OUT}}$	AM17	O	OV_{DD}	2,4

Table 78. MPC8568E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Debug				
TRIG_IN	AL29	I	OV_{DD}	—
TRIG_OUT	AM29	O	OV_{DD}	6,9,19,29
MSRCID[0:1]	AK29, AJ29	O	OV_{DD}	5,6,9
MSRCID[2:4]	AM28, AL28, AK27	O	OV_{DD}	6,19,29
MDVAL	AJ28	O	OV_{DD}	6
CLK_OUT	AF18	O	OV_{DD}	11
Clock				
RTC	AH20	I	OV_{DD}	—
SYSCLK	AK22	I	OV_{DD}	—
JTAG				
TCK	AH18	I	OV_{DD}	—
TDI	AH19	I	OV_{DD}	12
TDO	AJ18	O	OV_{DD}	11
TMS	AK19	I	OV_{DD}	12
$\overline{\text{TRST}}$	AK20	I	OV_{DD}	12
DFT				
L1_TSTCLK	AJ20	I	OV_{DD}	25
L2_TSTCLK	AJ19	I	OV_{DD}	25
$\overline{\text{LSSD\_MODE}}$	AH31	I	OV_{DD}	25
$\overline{\text{TEST\_SEL}}$	AJ31	I	OV_{DD}	25
Thermal Management				
THERM0	AB30	—	—	14
THERM1	AB31	—	—	14
Power Management				
ASLEEP	AK21	O	OV_{DD}	9,19,29

Table 78. MPC8568E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Power and Ground Signals				
GND	A23, A26, A32, B3, B6, B9, B12, B18, B21, B23, B24, B25, B26, B27, C15, C24, D5, D8, D11, D17, D20, D23, D24, D28, E13, E14, E24, E31, F3, F7, F15, F18, F22, F24, F27, G8, G16, G19, G23, H5, H12, H13, H15, H16, H18, H19, H21, H22, J2, J7, J10, J14, J15, J16, J17, J18, J19, J20, J21, J22, J29, J31, J32, K14, K15, K16, K17, K18, K19, K20, K21, K22, K24, L1, L4, L9, L12, L15, L16, L17, L18, L19, L20, L21, L22, L23, M12, M13, M18, M20, M21, M23, N4, N8, N11, N13, N15, N17, N19, N21, N23, P2, P6, P12, P14, P16, P18, P20, P22, P23, R10, R13, R15, R17, R19, R21, R23, T12, T14, T16, T18, T20, T22, T23, U4, U8, U13, U15, U17, U19, U21, U23, V2, V6, V12, V14, V16, V18, V20, V22, V23, W10, W13, W15, W17, W19, W21, W23, Y12, Y14, Y16, Y18, Y20, Y22, Y23, AA4, AA8, AA12, AA13, AA15, AA17, AA19, AA21, AA22, AA23, AB2, AB6, AB12, AB23, AB29, AB32, AC10, AC23, AC24, AC25, AC28, AC29, AC30, AC31, AC32, AD16, AD17, AD19, AD21, AD25, AD26, AD27, AD31, AE8, AE12, AF2, AF4, AF6, AF16, AF21, AF25, AG10, AG14, AG18, AG24, AG28, AH23, AJ4, AJ8, AJ12, AJ21, AJ30, AJ32, AK2, AK10, AK16, AK32, AL6, AL14, AL18, AL19, AL20, AL22, AL24, AL25, AL26, AL31, AL32, AM19, AM21, AM23, AM25, AM30, AM31, AM32	—	—	—
SCOREGND	K28, K29, K30, L28, L31, M28, M30, N32, P28, P30, R28, T29, U32, V30, W28, W31, Y28, Y29, AA29, AA30, AA32, AB28	Ground for SerDes receiver	—	—
XGND	N24, N26, P25, R27, T24, U26, V25, W27, Y24, AA26, AB25, AC27	Ground for SerDes transmitter	—	—
OVDD	N2, N6, N10, P4, P8, T10, U2, U6, V4, V8, Y10, AA2, AA6, AB4, AB8, AC19, AC21, AD10, AD23, AE2, AE6, AE27, AE31, AG4, AG19, AG23, AG25, AH21, AH28, AH30, AH32, AJ2, AK4, AK25, AK31, AL27	Power for PCI and other standards (3.3V)	OVDD	—
LVDD	AC12, AC16, AF12, AF14, AG16, AK12, AK14, AL16	Power for eTSEC1 and eTSEC2 (2.5V,3.3V)	LVDD	—
TVDD	AF8, AJ10, AK6, AK8	Power for QE UCC1 and UCC2 Ethernet Interface (2,5V,3.3V)	TVDD	—

Table 78. MPC8568E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GVDD	B2, B5, B8, B11, B17, B20, C14, D4, D7, D10, D16, D19, D22, E12, E15, F2, F6, F21, G9, G17, G18, H4, H11, H14, H20, J3, J6, J9, K13, L2, L5, L8, L11	Power for DDR1 and DDR2 DRAM I/O voltage (1.8V,2.5V)	GVDD	—
BVDD	B28, D27, D31, F25, F28, H27, H29, H31, K25, K27	Power for Local Bus (1.8V, 2.5V, 3.3V)	BVDD	—
VDD	M14, M15, M19, M22, N12, N14, N16, N18, N20, N22, P13, P15, P17, P19, P21, R12, R14, R16, R18, R20, R22, T13, T15, T17, T19, T21, U12, U14, U16, U18, U20, U22, V13, V15, V17, V19, V21, W12, W14, W16, W18, W20, W22, Y13, Y15, Y17, Y19, Y21, AA14, AA16, AA18, AA20	Power for Core (1.1)	VDD	—
SCOREVDD	K31, L32, M29, N28, N31, P29, T28, T30, U31, V29, W32, Y30, AA31	Core Power for SerDes transceivers (1.1V)	SCOREVDD	—
XVDD	N25, N27, P24, R26, T25, U27, V24, W26, Y25, AA27, AB24, AC26	Pad Power for SerDes transceivers (1.1V)	XVDD	—
AV_{DD_LBIU}	A25	Power for local bus PLL (1.1V)	—	26
AV_{DD_PCI}	AM22	Power for PCI PLL (1.1V)	—	26
AV_{DD_CE}	AM18	Power for QE PLL (1.1V)	—	26
AV_{DD_CORE}	AM24	Power for e500 PLL (1.1V)	—	26
AV_{DD_PLAT}	AM20	Power for CCB PLL (1.1V)	—	26
AV_{DD_SRDS}	R29	Power for SRDSPLL (1.1V)	—	26
AGND_SRDS	R31	Ground for SRDSPLL	—	—
SENSEVDD	M17	O	V_{DD}	13

Table 78. MPC8568E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
SENSEVSS	M16	—	—	13
Analog Signals				
MVREF	A24	I Reference voltage signal for DDR	MVREF	—
SD_IMP_CAL_RX	K32	I	200Ω to GND	—
SD_IMP_CAL_TX	AA28	I	100Ω to GND	—
SD_PLL_TPA	R30	O	—	24

Table 78. MPC8568E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes

Notes:

1. All multiplexed signals are listed only once and do not re-occur. For example, $\overline{\text{LCS5}}$/$\overline{\text{DMA\_REQ2}}$ is listed only once in the local bus controller section, and is not mentioned in the DMA section even though the pin also functions as $\overline{\text{DMA\_REQ2}}$.
2. Recommend a weak pull-up resistor (2–10 KΩ) be placed on this pin to OV_{DD}.
4. This pin is an open drain signal.
5. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pullup or active driver is needed.
6. Treat these pins as no connects (NC) unless using debug address functionality.
7. The value of LA[28:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 23.2, "CCB/SYSCLK PLL Ratio."
8. The value of LALE, LGPL2 and LBCTL at reset set the e500 core clock to CCB Clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See the Section 23.3, "e500 Core PLL Ratio."
9. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.
11. This output is actively driven during reset rather than being three-stated during reset.
12. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
13. These pins are connected to the V_{DD}/GND planes internally and may be used by the core power supply to improve tracking and regulation.
14. Internal thermally sensitive resistor. These two pins are not ESD protected.
17. . The value of PA[0:4] during reset set the QE clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 23.4, "QE/SYSCLK PLL Ratio."
19. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
20. This pin is only an output in FIFO mode when used as Rx Flow Control.
24. Do not connect.
25. These are test signals for factory use only and must be pulled up (100 - 1 K) to OVDD for normal machine operation.
26. Independent supplies derived from board VDD.
27. Recommend a pull-up resistor (~1 K.) be placed on this pin to OV_{DD}.
29. The following pins must NOT be pulled down during power-on reset: HRESET_REQ, TRIG_OUT/READY/$\overline{\text{QUIESCE}}$, MSRCID[2:4], ASLEEP, PA[5]

Table 78. MPC8568E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes

30. This pin requires an external 4.7-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
33. PF[21:22] are multiplexed as cfg_dram_type[0:1]. THEY MUST BE VALID AT POWER-UP, EVEN BEFORE $\overline{\text{HRESET}}$ ASSERTION.
35. When a PCI block is disabled, either the POR config pin that selects between internal and external arbiter must be pulled down to select external arbiter if there is any other PCI device connected on the PCI bus, or leave the PCI*n*_AD pins as "No Connect" or terminated through 2–10 KΩ pull-up resistors with the default of internal arbiter if the PCI*n*_AD pins are not connected to any other PCI device. The PCI block will drive the PCI*n*_AD pins if it is configured to be the PCI arbiter—through POR config pins—irrespective of whether it is disabled via the DEVDISR register or not. It may cause contention if there is any other PCI device connected on the bus.
36. MDIC[0] is grounded through an 18.2-Ω precision 1% resistor and MDIC[1] is connected to GV_{DD} through an 18.2-Ω precision 1% resistor. These pins are used for automatic calibration of the DDR IOs.
39. If PCI is configured as PCI asynchronous mode, a valid clock must be provided on pin PCI_CLK . Otherwise the processor will not boot up.
41. These pins should be tied to SCOREGND through a 300 ohm resistor if the high speed interface is used.
43. It is highly recommended that unused SD_RX/$\overline{\text{SD\_RX}}$ lanes should be powered down with lane_x_pd. Otherwise the receivers will burn extra power and the internal circuitry may develop long term reliability problems.
44. See Section 25.9, "Guidelines for High-Speed Interface Termination."
46. Must be high during $\overline{\text{HRESET}}$. It is recommended to leave the pin open during $\overline{\text{HRESET}}$ since it has internal pullup resistor.
47. Must be pulled down with 4.7-kΩ resistor.
48. This pin must be left no connect.
49. A pull-up on LGPL4 is required for systems that boot from local bus (GPCM)-controlled NOR Flash.

Table 79 provides the pin-out listing for the MPC8567E 1023 FC-PBGA package.

Table 79. MPC8567E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI				
PCI_AD[31:0]	AE19, AG20, AF19, AB20, AC20, AG21, AG22, AB21, AF22, AH22, AE22, AF20, AB22, AE20, AE23, AJ23, AJ24, AF27, AJ26, AE29, AH24, AD24, AE25, AE26, AH27, AG27, AJ25, AE30, AF26, AG26, AF28, AH26	I/O	OV_{DD}	—
PCI_C_$\overline{\text{BE}}$[3:0]	AC22, AD20, AE28, AH25	I/O	OV_{DD}	—
$\overline{\text{PCI\_GNT}}$[4:1]	AF29, AB18, AC18, AD18	O	OV_{DD}	5,9,35
$\overline{\text{PCI\_GNT0}}$	AE18	I/O	OV_{DD}	—
$\overline{\text{PCI\_IRDY}}$	AF23	I/O	OV_{DD}	2
PCI_PAR	AJ22	I/O	OV_{DD}	—
$\overline{\text{PCI\_PERR}}$	AF24	I/O	OV_{DD}	2
$\overline{\text{PCI\_SERR}}$	AD22	I/O	OV_{DD}	2,4
$\overline{\text{PCI\_STOP}}$	AE24	I/O	OV_{DD}	2
$\overline{\text{PCI\_TRDY}}$	AK24	I/O	OV_{DD}	2

Table 79. MPC8567E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI_REQ[4:1]	AG29, AJ27, AH29, AB17	I	OV_{DD}	—
PCI_REQ[0]	AC17	I/O	OV_{DD}	—
PCI_CLK	AM26	I	OV_{DD}	39
PCI_DEVSEL	AK23	I/O	OV_{DD}	2
PCI_FRAME	AE21	I/O	OV_{DD}	2
PCI_IDSEL	AB19	I	OV_{DD}	—
DDR SDRAM Memory Interface				
MDQ[0:63]	B22, C22, E20, A19, C23, A22, A20, C20, G22, E22, E16, F16, E23, F23, F17, H17, A18, A17, B16, C16, B19, C19, E17, A16, A13, A14, A12, C12, A15, B15, B13, C13, G12, G11, H8, F8, D13, F12, E9, F9, A7, B7, C5, E5, C8, E8, D6, A5, E6, G6, E1, F1, G7, E7, E2, D1, C4, A3, B1, C1, A4, B4, C2, D2	I/O	GV_{DD}	—
MECC[0:7]	C11, E11, D9, A8, D12, A11, A9, C9	I/O	GV_{DD}	—
MDM[0:8]	A21, E21, D18, B14, F11, A6, G5, A2, A10	O	GV_{DD}	—
MDQS[0:8]	D21, G20, C17, D14, E10, C6, F4, C3, C10	I/O	GV_{DD}	—
MDQS[0:8]	C21, G21, C18, D15, F10, C7, F5, D3, B10	I/O	GV_{DD}	—
MA[0:15]	K7, H7, L7, J8, K8, L10, H9, K9, H10, G10, L6, K10, K11, H3, J11, J12	O	GV_{DD}	—
MBA[0:2]	K4, H6, L13	O	GV_{DD}	—
MWE	K3	O	GV_{DD}	—
MCAS	L3	O	GV_{DD}	—
MRAS	K6	O	GV_{DD}	—
MCKE[0:3]	L14, G13, K12, J13	O	GV_{DD}	11
MCS[0:3]	J5, H2, K5, K2,	O	GV_{DD}	—
MCK[0:5]	G15, F20, E4, F14, E19, G3	O	GV_{DD}	—
MCK[0:5]	G14, F19, E3, F13, E18, G2	O	GV_{DD}	—
MODT[0:3]	G4, J1, J4, K1	O	GV_{DD}	—
MDIC[0:1]	G1, H1	I/O	GV_{DD}	36
Local Bus Controller Interface				
LAD[0:31]	M26, C30, F31, L24, G26, D30, M25, L26, D29, G32, G28, K26, B32, M24, G29, L25, E29, J23, B30, A31, J24, K23, H25, H23, F26, C28, B29, E25, D26, G24, A29, E27,	I/O	BV_{DD}	—
LDP[0:3]	G30, J26, H28, E26	I/O	BV_{DD}	—
LA[27]	F29	O	BV_{DD}	5,9
LA[28:31]	H24, C32, F30, H26	O	BV_{DD}	5,7,9

Table 79. MPC8567E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LALE	G31	O	BVdd	8
LBCTL	L27	O	BVdd	8
$\overline{\text{LCS}}$[0:4]	M27, H32, J28, J30, B31	O	BV_{DD}	—
$\overline{\text{LCS5}}$	G25	I/O	BV_{DD}	1
$\overline{\text{LCS6}}$	C29	O	BV_{DD}	1
$\overline{\text{LCS7}}$	A30	O	BV_{DD}	1
$\overline{\text{LWE}}$[0]	H30	O	BV_{DD}	5,9
$\overline{\text{LWE}}$[1]	E28	O	BV_{DD}	5,9
$\overline{\text{LWE}}$[2]	E32	O	BV_{DD}	5,9
$\overline{\text{LWE}}$[3]	G27	O	BV_{DD}	5,9
LGPL0	E30	O	BV_{DD}	5,9
LGPL1	J27	O	BV_{DD}	5,9,46
LGPL2	D32	O	BV_{DD}	5,8,9
LGPL3	J25	O	BV_{DD}	5,9
LGPL4	C25	I/O	BV_{DD}	49
LGPL5	F32	O	BV_{DD}	5,9
LCKE	C31	O	BV_{DD}	—
LCLK[0:2]	C27, C26, D25	O	BV_{DD}	—
LSYNC_IN	A28	I	BV_{DD}	—
LSYNC_OUT	A27	O	BV_{DD}	—
DMA				
$\overline{\text{DMA\_DACK}}$[0]	AM27	O	OV_{DD}	5,9,47
$\overline{\text{DMA\_DREQ}}$[0]	AK28	I	OV_{DD}	—
$\overline{\text{DMA\_DDONE}}$[0]	AK26	O	OV_{DD}	—
Programmable Interrupt Controller				
$\overline{\text{UDE}}$	AG32	I	OV_{DD}	—
$\overline{\text{MCP}}$	AF32	I	OV_{DD}	—
IRQ[0:7]	AD30, AG31, AL30, AF31, AD29, AK30, AG30, AF30	I	OV_{DD}	—
$\overline{\text{IRQ\_OUT}}$	AD28	O	OV_{DD}	2,4
GPIO				
GPIN[0:7]	AC14, AD15, AB14, AH15, AD14, AH17, AE15, AC15	I	LV_{DD}	—

Table 79. MPC8567E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPOUT[0:7]	AM16, AJ15, AJ17, AF13, AK17, AH16, AG17, AL15	O	LV_{DD}	—
I^2C interface				
IIC1_SCL	AE32	I/O	OV_{DD}	4,27
IIC1_SDA	AD32	I/O	OV_{DD}	4,27
SerDes				
SD_RX[0:7]	L30, M32, N30, P32, U30, V32, W30, Y32	I	SCOREVDD	43,44
$\overline{\text{SD\_RX}}$[0:7]	L29, M31, N29, P31, U29, V31, W29, Y31	I	SCOREVDD	43,44
SD_TX[0:7]	P26, R24, T26, U24, W24, Y26, AA24, AB26	O	XV_{DD}	44
$\overline{\text{SD\_TX}}$[0:7]	P27, R25, T27, U25, W25, Y27, AA25, AB27	O	XV_{DD}	44
SD_PLL_TPD	R32	O	SCOREVDD	24
$\overline{\text{SD\_RX\_CLK}}$	U28	I	XV_{DD}	41,44
$\overline{\text{SD\_RX\_FRM\_CTL}}$	V28	I	XV_{DD}	41,44
Reserved	V26	—	—	48
Reserved	V27	—	—	48
SD_REF_CLK	T32	I	SCOREVDD	44
$\overline{\text{SD\_REF\_CLK}}$	T31	I	SCOREVDD	44
QUICC Engine				
PA[0:4]	M1, M2, M5, M4, M3	I/O	OV_{DD}	5,17
PA[5]	N3	I/O	OV_{DD}	29
PA[6:31]	M6, M7, M8, N5, M10, N1, M11, M9, P1, N9, N7, R6, R2, P7, P5, R4, P3, P11, P10, P9, R8, R7, R5, R3, R1, T2	I/O	OV_{DD}	—
PB[4:31]	T1, R11, R9, T6, T5, T4, T3, U10, T9, T8, T7, U5, U3, U1, T11, V1, U11, U9, U7, V5, W4, V3, W2, V9, W8, V7, W6, W3	I/O	OV_{DD}	—
PC[0:31]	W1, V11, V10, W11, W9, W7, W5, Y4, Y3, Y2, Y1, Y8, Y7, Y6, Y5, AA1, Y11, AA10, Y9, AA9, AA7, AA5, AA3, AB3, AC2, AB1, AA11, AB7, AC6, AB5, AC4, AB9	I/O	OV_{DD}	—
PD[4:31]	AC8, AD1, AC1, AC7, AB10, AC5, AD3, AD2, AC3, AE4, AF1, AE3, AE1, AD6, AG2, AG1, AD5, AD7, AD4, AH1, AK3, AD8, AF5, AM4, AC9, AL2, AE5, AF3	I/O	OV_{DD}	—
PE[5:7]	AM6, AL5, AL9	I/O	TV_{DD}	—
PE[8:10]	AM9, AM10, AL10	I/O	TV_{DD}	5
PE[11:19]	AJ9, AH10, AM8, AK9, AL7, AL8, AH9, AM7, AH8	I/O	TV_{DD}	—

Table 79. MPC8567E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PE[20]	AH6	I/O	OV_{DD}	—
PE[21:23]	AM1, AE10, AG5	I/O	OV_{DD}	5
PE[24]	AJ1	I/O	OV_{DD}	5
PE[25:31]	AH2, AM2, AE9, AH5, AL1, AD9, AL4	I/O	OV_{DD}	—
PF[7]	AG9	I/O	TV_{DD}	—
PF[8:10]	AF10, AK7, AJ6	I/O	TV_{DD}	5
PF[11:19]	AH7, AF9, AJ7, AJ5, AF7, AG8, AG7, AM5, AK5	I/O	TV_{DD}	—
PF[20]	AK1	I/O	OV_{DD}	—
PF[21:22]	AH3, AL3	I/O	OV_{DD}	5,33
PF[23:31]	AB11, AE7, AJ3, AC11, AG6, AG3, AH4, AM3, AD11	I/O	OV_{DD}	—
System Control				
$\overline{\text{HRESET}}$	AL21	I	OV_{DD}	—
$\overline{\text{HRESET\_REQ}}$	AL23	O	OV_{DD}	29
$\overline{\text{SRESET}}$	AK18	I	OV_{DD}	—
$\overline{\text{CKSTP\_IN}}$	AL17	I	OV_{DD}	—
$\overline{\text{CKSTP\_OUT}}$	AM17	O	OV_{DD}	2,4
Debug				
TRIG_IN	AL29	I	OV_{DD}	—
TRIG_OUT	AM29	O	OV_{DD}	6,9,19, 29
MSRCID[0:1]	AK29, AJ29	O	OV_{DD}	5,6,9
MSRCID[2:4]	AM28, AL28, AK27	O	OV_{DD}	6,19,29
MDVAL	AJ28	O	OV_{DD}	6
CLK_OUT	AF18	O	OV_{DD}	11
Clock				
RTC	AH20	I	OV_{DD}	—
SYSCLK	AK22	I	OV_{DD}	—
JTAG				
TCK	AH18	I	OV_{DD}	—
TDI	AH19	I	OV_{DD}	12
TDO	AJ18	O	OV_{DD}	11
TMS	AK19	I	OV_{DD}	12
$\overline{\text{TRST}}$	AK20	I	OV_{DD}	12

Table 79. MPC8567E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DFT				
L1_TSTCLK	AJ20	I	OV_{DD}	25
L2_TSTCLK	AJ19	I	OV_{DD}	25
$\overline{\text{LSSD\_MODE}}$	AH31	I	OV_{DD}	25
$\overline{\text{TEST\_SEL}}$	AJ31	I	OV_{DD}	25
Thermal Management				
THERM0	AB30	—	—	14
THERM1	AB31	—	—	14
Power Management				
ASLEEP	AK21	O	OV_{DD}	9,19,29
Power and Ground Signals				
GND	A23, A26, A32, B3, B6, B9, B12, B18, B21, B23, B24, B25, B26, B27, C15, C24, D5, D8, D11, D17, D20, D23, D24, D28, E13, E14, E24, E31, F3, F7, F15, F18, F22, F24, F27, G8, G16, G19, G23, H5, H12, H13, H15, H16, H18, H19, H21, H22, J2, J7, J10, J14, J15, J16, J17, J18, J19, J20, J21, J22, J29, J31, J32, K14, K15, K16, K17, K18, K19, K20, K21, K22, K24, L1, L4, L9, L12, L15, L16, L17, L18, L19, L20, L21, L22, L23, M12, M13, M18, M20, M21, M23, N4, N8, N11, N13, N15, N17, N19, N21, N23, P2, P6, P12, P14, P16, P18, P20, P22, P23, R10, R13, R15, R17, R19, R21, R23, T12, T14, T16, T18, T20, T22, T23, U4, U8, U13, U15, U17, U19, U21, U23, V2, V6, V12, V14, V16, V18, V20, V22, V23, W10, W13, W15, W17, W19, W21, W23, Y12, Y14, Y16, Y18, Y20, Y22, Y23, AA4, AA8, AA12, AA13, AA15, AA17, AA19, AA21, AA22, AA23, AB2, AB6, AB12, AB23, AB29, AB32, AC10, AC23, AC24, AC25, AC28, AC29, AC30, AC31, AC32, AD16, AD17, AD19, AD21, AD25, AD26, AD27, AD31, AE8, AE12, AF2, AF4, AF6, AF16, AF21, AF25, AG10, AG14, AG18, AG24, AG28, AH23, AJ4, AJ8, AJ12, AJ21, AJ30, AJ32, AK2, AK10, AK16, AK32, AL6, AL14, AL18, AL19, AL20, AL22, AL24, AL25, AL26, AL31, AL32, AM19, AM21, AM23, AM25, AM30, AM31, AM32	—	—	—
SCOREGND	K28, K29, K30, L28, L31, M28, M30, N32, P28, P30, R28, T29, U32, V30, W28, W31, Y28, Y29, AA29, AA30, AA32, AB28	Ground for SerDes receiver	—	—
XGND	N24, N26, P25, R27, T24, U26, V25, W27, Y24, AA26, AB25, AC27	Ground for SerDes transmitter	—	—

Table 79. MPC8567E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
OVDD	N2, N6, N10, P4, P8, T10, U2, U6, V4, V8, Y10, AA2, AA6, AB4, AB8, AC19, AC21, AD10, AD23, AE2, AE6, AE27, AE31, AG4, AG19, AG23, AG25, AH21, AH28, AH30, AH32, AJ2, AK4, AK25, AK31, AL27	Power for PCI and other standards (3.3V)	OVDD	—
LVDD	AC12, AC16, AF12, AF14, AG16, AK12, AK14, AL16	Power for GPIO	LVDD	—
TVDD	AF8, AJ10, AK6, AK8	Power for QE UCC1 and UCC2 Ethernet Interface (2,5V,3.3V)	TVDD	—
GVDD	B2, B5, B8, B11, B17, B20, C14, D4, D7, D10, D16, D19, D22, E12, E15, F2, F6, F21, G9, G17, G18, H4, H11, H14, H20, J3, J6, J9, K13, L2, L5, L8, L11	Power for DDR1 and DDR2 DRAM I/O voltage (1.8V,2.5V)	GVDD	—
BVDD	B28, D27, D31, F25, F28, H27, H29, H31, K25, K27	Power for Local Bus (1.8V, 2.5V, 3.3V)	BVDD	—
VDD	M14, M15, M19, M22, N12, N14, N16, N18, N20, N22, P13, P15, P17, P19, P21, R12, R14, R16, R18, R20, R22, T13, T15, T17, T19, T21, U12, U14, U16, U18, U20, U22, V13, V15, V17, V19, V21, W12, W14, W16, W18, W20, W22, Y13, Y15, Y17, Y19, Y21, AA14, AA16, AA18, AA20	Power for Core (1.1)	VDD	—
SCOREVDD	K31, L32, M29, N28, N31, P29, T28, T30, U31, V29, W32, Y30, AA31	Core Power for SerDes transceivers (1.1V)	SCOREVDD	—
XVDD	N25, N27, P24, R26, T25, U27, V24, W26, Y25, AA27, AB24, AC26	Pad Power for SerDes transceivers (1.1V)	XVDD	—
AV_{DD_LBIU}	A25	Power for local bus PLL (1.1V)	—	26
AV_{DD_PCI}	AM22	Power for PCI PLL (1.1V)	—	26
AV_{DD_CE}	AM18	Power for QE PLL (1.1V)	—	26

Table 79. MPC8567E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
AV_{DD_CORE}	AM24	Power for e500 PLL (1.1V)	—	26
AV_{DD_PLAT}	AM20	Power for CCB PLL (1.1V)	—	26
AV_{DD_SRDS}	R29	Power for SRDSPLL (1.1V)	—	26
AGND_SRDS	R31	Ground for SRDSPLL	—	
SENSEVDD	M17	O	V_{DD}	13
SENSEVSS	M16	—	—	13
Analog Signals				
MVREF	A24	I Reference voltage signal for DDR	MVREF	—
SD_IMP_CAL_RX	K32	I	200Ω to GND	—
SD_IMP_CAL_TX	AA28	I	100Ω to GND	—
SD_PLL_TPA	R30	O	—	24
Reserved Pins				
Reserved	AE17, AH12, AL13, AL11, AK13, AH13, AG11, AD13, AM13, AG12, AC13, AL12, AJ16, AM15, AK15	N/A	N/A	42
Reserved	AF17, AM14, AE14, AM11, AK11, AF11, AJ14, AJ13, AD12, AE13, AG13, AB13, AE11, AH11, AM12, AJ11, AB15, AB16, AE16, AG15, AF15, AH14	N/A	N/A	45

Table 79. MPC8567E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes

Notes:

1. All multiplexed signals are listed only once and do not re-occur. For example, $\overline{\text{LCS5}}/\overline{\text{DMA\_REQ2}}$ is listed only once in the local bus controller section, and is not mentioned in the DMA section even though the pin also functions as $\overline{\text{DMA\_REQ2}}$.
2. Recommend a weak pull-up resistor (2–10 KΩ) be placed on this pin to OV_{DD}.
4. This pin is an open drain signal.
5. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pullup or active driver is needed.
6. Treat these pins as no connects (NC) unless using debug address functionality.
7. The value of LA[28:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 23.2, "CCB/SYSCLK PLL Ratio."
8. The value of LALE, LGPL2 and LBCTL at reset set the e500 core clock to CCB Clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See the Section 23.3, "e500 Core PLL Ratio."
9. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.
11. This output is actively driven during reset rather than being three-stated during reset.
12. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
13. These pins are connected to the V_{DD}/GND planes internally and may be used by the core power supply to improve tracking and regulation.
14. Internal thermally sensitive resistor. These two pins are not ESD protected.
17. . The value of PA[0:4] during reset set the QE clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 23.4, "QE/SYSCLK PLL Ratio."
19. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
20. This pin is only an output in FIFO mode when used as Rx Flow Control.
24. Do not connect.
25. These are test signals for factory use only and must be pulled up (100 - 1 K) to OVDD for normal machine operation.
26. Independent supplies derived from board VDD.
27. Recommend a pull-up resistor (~1 K.) be placed on this pin to OV_{DD}.
29. The following pins must NOT be pulled down during power-on reset: HRESET_REQ, TRIG_OUT/READY/$\overline{\text{QUIESCE}}$, MSRCID[2:4], ASLEEP, PA[5].

Table 79. MPC8567E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes

30. This pin requires an external 4.7-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
33. PF[21:22] are multiplexed as cfg_dram_type[0:1]. THEY MUST BE VALID AT POWER-UP, EVEN BEFORE $\overline{\text{HRESET}}$ ASSERTION.
35. When a PCI block is disabled, either the POR config pin that selects between internal and external arbiter must be pulled down to select external arbiter if there is any other PCI device connected on the PCI bus, or leave the PCI*n*_AD pins as "No Connect" or terminated through 2–10 KΩ pull-up resistors with the default of internal arbiter if the PCI*n*_AD pins are not connected to any other PCI device. The PCI block will drive the PCI*n*_AD pins if it is configured to be the PCI arbiter—through POR config pins—irrespective of whether it is disabled via the DEVDISR register or not. It may cause contention if there is any other PCI device connected on the bus.
36. MDIC[0] is grounded through an 18.2-Ω precision 1% resistor and MDIC[1] is connected to GV_{DD} through an 18.2-Ω precision 1% resistor. These pins are used for automatic calibration of the DDR IOs.
39. If PCI is configured as PCI asynchronous mode, a valid clock must be provided on pin PCI_CLK . Otherwise the processor will not boot up.
41. These pins should be tied to SCOREGND through a 300 ohm resistor if the high speed interface is used.
43. It is highly recommended that unused SD_RX/$\overline{\text{SD\_RX}}$ lanes should be powered down with lane_x_pd. Otherwise the receivers will burn extra power and the internal circuitry may develop long term reliability problems.
44. See Section 25.9, "Guidelines for High-Speed Interface Termination."
46. Must be high during $\overline{\text{HRESET}}$. It is recommended to leave the pin open during $\overline{\text{HRESET}}$ since it has internal pullup resistor.
47. Must be pulled down with 4.7-kΩ resistor.
48. This pin must be left no connect.
49. A pull-up on LGPL4 is required for systems that boot from local bus (GPCM)-controlled NOR Flash.

23 Clocking

This section describes the PLL configuration of the MPC8568E. Note that the platform clock is identical to the core complex bus (CCB) clock.

23.1 Clock Ranges

Table 80 provides the clocking specifications for the processor cores and Table 81 provides the clocking specifications for the DDR/DDR2 memory bus. Table 82 provides the clocking specifications for the local bus.

Table 80. Processor Core Clocking Specifications

Characteristic	Maximum Processor Core Frequency						Unit	Notes
	800 MHz		1000 MHz		1333 MHz			
	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	533	800	533	1000	533	1333	MHz	1, 2

Notes:
1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 23.2, "CCB/SYSCLK PLL Ratio," and Section 23.3, "e500 Core PLL Ratio," for ratio settings.
2.)The minimum e500 core frequency is based on the minimum platform frequency of 333 MHz.

Table 81. DDR/DDR2 Memory Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	800, 1000, 1333 MHz			
	Min	Max		
DDR/DDR2 Memory bus clock frequency	166	266	MHz	1, 2

Notes:
1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 core frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies.
2. The memory bus clock speed is half the DDR/DDR2 data rate, hence, half the platform clock frequency.

Table 82. Local Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	800, 1000, 1333 MHz			
	Min	Max		
Local bus clock speed (for Local Bus Controller)	25	166	MHz	1

Notes:
1. The Local bus clock speed on LCLK[0:2] is determined by CCB clock divided by the Local Bus PLL ratio programmed in LCCR[CLKDIV]. See the reference manual for more information on this.

23.2 CCB/SYSCLK PLL Ratio

The CCB clock is the clock that drives the e500 core complex bus (CCB) and is also called the platform clock. The frequency of the CCB is set using the following reset signals, as shown in Table 83:

- SYSCLK input signal
- Binary value on LA[28:31] at power up

Note that there is no default for this PLL ratio; these signals must be pulled to the desired values. Also note that the DDR data rate is the determining factor in selecting the CCB bus frequency, since the CCB frequency must equal the DDR data rate.

For specifications on the PCI_CLK, refer to the PCI 2.2 Specification.

Table 83. CCB Clock Ratio

Binary Value of LA[28:31] Signals	CCB:SYSCLK Ratio	Binary Value of LA[28:31] Signals	CCB:SYSCLK Ratio
0000	16:1	1000	8:1
0001	Reserved	1001	9:1
0010	2:1	1010	10:1
0011	3:1	1011	Reserved
0100	4:1	1100	12:1

Table 83. CCB Clock Ratio (continued)

Binary Value of LA[28:31] Signals	CCB:SYSCLK Ratio	Binary Value of LA[28:31] Signals	CCB:SYSCLK Ratio
0101	5:1	1101	20:1
0110	6:1	1110	Reserved
0111	Reserved	1111	Reserved

23.3 e500 Core PLL Ratio

Table 84 describes the clock ratio between the e500 core complex bus (CCB)platform and the e500 core clock. This ratio is determined by the binary value of LBCTL, LALE and LGPL2 at power up, as shown in Table 84.

Table 84. e500 Core to CCB Clock Ratio

Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core:CCB Clock Ratio	Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core:CCB Clock Ratio
000	4:1	100	2:1
001	9:2	101	5:2
010	Reserved	110	3:1
011	3:2	111	7:2

23.4 QE/SYSCLK PLL Ratio

The QE clock is defined by a multiplier and divisor applied to the SYSCLK input signal, as shown in the following equation:

QE clock = SYSCLK * cfg_ce_pll[0:4].

The multiplier and divisor is determined by the binary value of PA[0:4] at power up.

Table 85. QE Clock Multiplier cfg_ce_pll[0:4]

Binary Value of PA[0:4] Signals	cfg_ce_pll[0:4]	Binary Value of PA[0:4] Signals	cfg_ce_pll[0:4]
0_0000	16	1_0000	16
0_0001	Reserved	1_0001	17
0_0010	2	1_0010	18
0_0011	3	1_0011	19
0_0100	4	1_0100	20
0_0101	5	1_0101	21
0_0110	6	1_0110	22
0_0111	7	1_0111	23

Table 85. QE Clock Multiplier cfg_ce_pll[0:4] (continued)

Binary Value of PA[0:4] Signals	cfg_ce_pll[0:4]	Binary Value of PA[0:4] Signals	cfg_ce_pll[0:4]
0_1000	8	1_1000	24
0_1001	9	1_1001	25
0_1010	10	1_1010	26
0_1011	11	1_1011	27
0_1100	12	1_1100	28
0_1101	13	1_1101	29
0_1110	14	1_1110	30
0_1111	15	1_1111	31

23.5 Frequency Options

23.5.1 SYSCLK to Platform Frequency Options

Table 86 shows the expected frequency values for the platform frequency when using a CCB clock to SYSCLK ratio in comparison to the memory bus clock speed.

Table 86. Frequency Options of SYSCLK with Respect to Memory Bus Speeds

CCB clock to SYSCLK Ratio	SYSCLK (MHz)									
	16.66	25	33.33	41.66	66.66	83	100	111	133.33	166
	Platform /CCB clock Frequency (MHz)									
2										333
3								333	400	500
4						333	400	445	533	
5					333	415	500			
6					400	500				
8				333	533					
9				375						
10			333	417						
12			400	500						
16		400	533							
20	333	500								

23.5.2 Minimum Platform Frequency Requirements for PCI Express, SRIO, PCI interfaces Operation

For proper PCI Express operation, the CCB clock frequency must be greater than:

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{8}$$

Note that the “PCI Express link width” in the above equation refers to the negotiated link width as the result of PCI Express link training, which may or may not be the same as the link width POR selection.

For proper Serial RapidIO operation, the CCB clock frequency must be greater than:

$$\frac{2 \times (0.80) \times (\text{serial RapidIO interface frequency}) \times (\text{serial RapidIO link width})}{64}$$

For proper PCI operation in synchronous mode, the minimum CCB:SYSCLK ratio is 6:1.

24 Thermal

This section describes the thermal specifications of the MPC8568E.

24.1 Thermal Characteristics

Table 87 provides the package thermal characteristics.

Table 87. Package Thermal Characteristics

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient Natural Convection on single layer board (1s)	$R_{\theta JA}$	21	°C/W	1, 2
Junction-to-ambient Natural Convection on four layer board (2s2p)	$R_{\theta JA}$	17	°C/W	1, 2
Junction-to-ambient (@200 ft/min or 1 m/s) on single layer board (1s)	$R_{\theta JA}$	16	•C/W	1, 2
Junction-to-ambient (@200 ft/min or 1 m/s) on four layer board (2s2p)	$R_{\theta JA}$	13	•C/W	1, 2
Junction-to-board	$R_{\theta JB}$	9	•C/W	3
Junction-to-case	$R_{\theta JC}$	<0.1	•C/W	4

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
2. Per JEDEC JESD51-6 with the board horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the active surface of the die and the case top surface determined by the cold plate method (MIL SPEC-883, Method 1012.1) with the calculated case temperature. Actual thermal resistance is less than 0.1 °C/W.

24.2 Thermal Management Information

This section provides thermal management information for the flip chip plastic ball grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the

system-level design—the heat sink, airflow, and thermal interface material. The recommended attachment method to the heat sink is illustrated in Figure 69. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 10 pounds force.

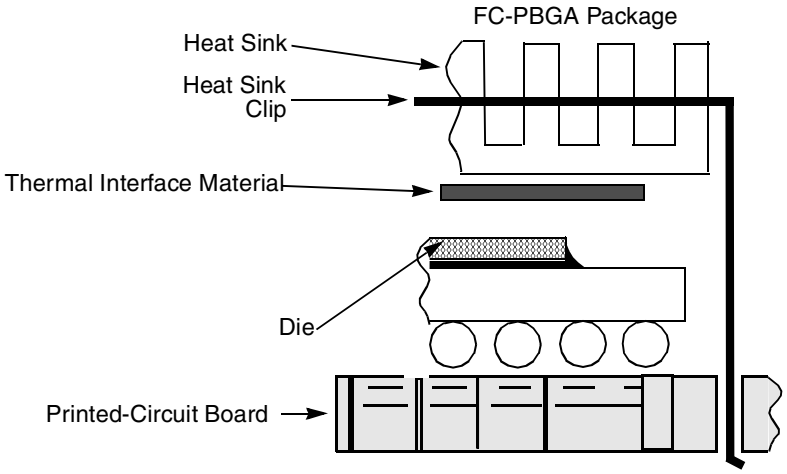


Figure 69. Package Exploded Cross-Sectional View with Several Heat Sink Options

The system board designer can choose between several types of heat sinks to place on the device. There are several commercially-available heat sinks from the following vendors:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Advanced Thermal Solutions 89 Access Road #27. Norwood, MA02062 Internet: www.qats.com	781-769-2800
Alpha Novatech 473 Sapena Ct. #15 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-749-7601
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Millennium Electronics (MEI) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-millennium.com	408-436-8770

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Several heat sinks offered by Aavid Thermalloy, Advanced Thermal Solutions, Alpha Novatech, IERC, and

Millennium Electronics offer different heat sink-to-ambient thermal resistances, that will allow the MPC8568E to function in various environments.

24.2.1 Recommended Thermal Model

For system thermal modeling, the MPC8568E thermal model without a lid is shown in Figure 70. The substrate is modeled as a block 33x33x1.18 mm with an in-plane conductivity of 24 W/mK and a through-plane conductivity of 0.92 W/mK. The solder balls and air are modeled as a single block 33x33x0.58 mm with an in-plane conductivity of 0.034 W/mK and a through plane conductivity of 12.2 W/mK. The die is modeled as 8.2x12.1 mm with a thickness of 0.75 mm. The bump/underfill layer is modeled as a collapsed thermal resistance between the die and substrate assuming a conductivity of 5.3 W/m•K in the thickness dimension of 0.07 mm. The die is centered on the substrate. The thermal model uses approximate dimensions to reduce grid. See the case outline for actual dimensions.

Conductivity	Value	Unit
Die (8.2 × 12.1 × 0.75mm)		
Silicon	Temperature dependent	W/(m × K)
Bump/Underfill (8.2 × 12.1 × 0.75 mm) Collapsed Resistance		
k_z	5.3	
Substrate (33 × 33× 1.18 mm)		
k_x	24	
k_y	24	
k_z	0.92	
Soldera and Air (33 × 33 × 0.58 mm)		
k_x	0.034	
k_y	0.034	
k_z	12.2	

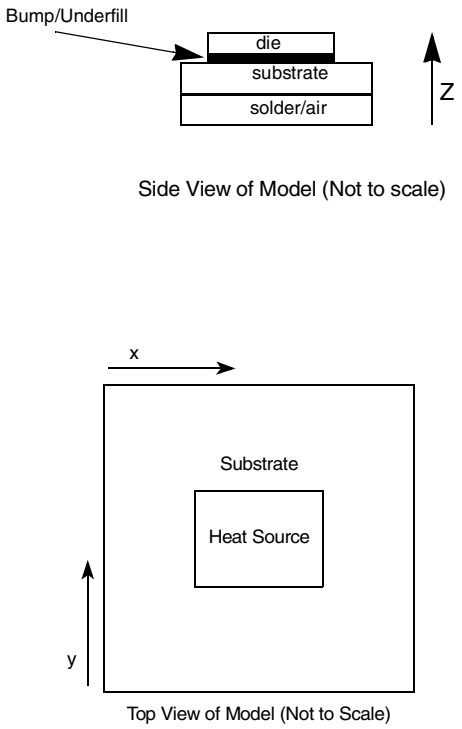


Figure 70. MPC8568E Thermal Model

24.2.2 Internal Package Conduction Resistance

For the packaging technology, shown in Table 87, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance

- The die junction-to-board thermal resistance

Figure 71 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

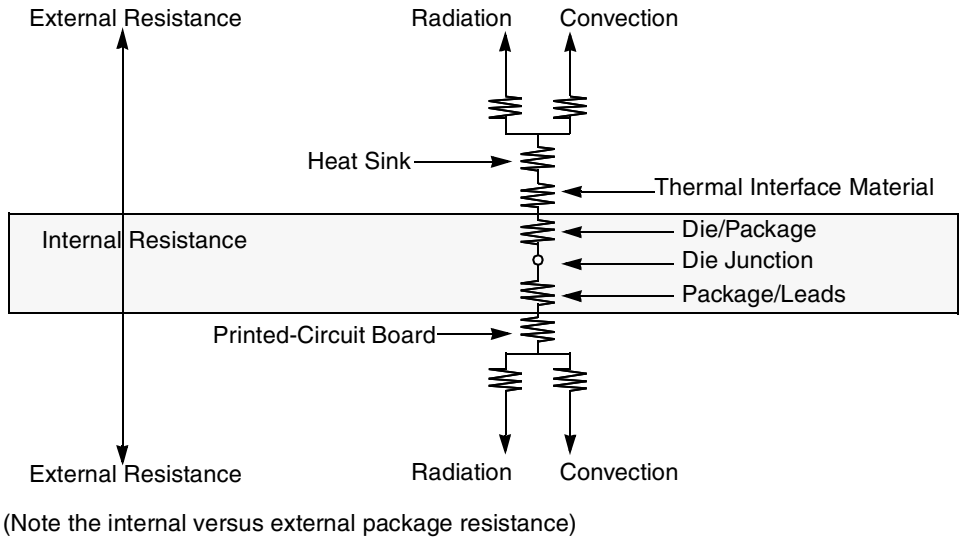


Figure 71. Package with Heat Sink Mounted to a Printed-Circuit Board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon, then through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

24.2.3 Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 72 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. The bare joint results in a thermal resistance approximately six times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 69). Therefore, the synthetic grease offers the best thermal performance, especially at the low interface pressure.

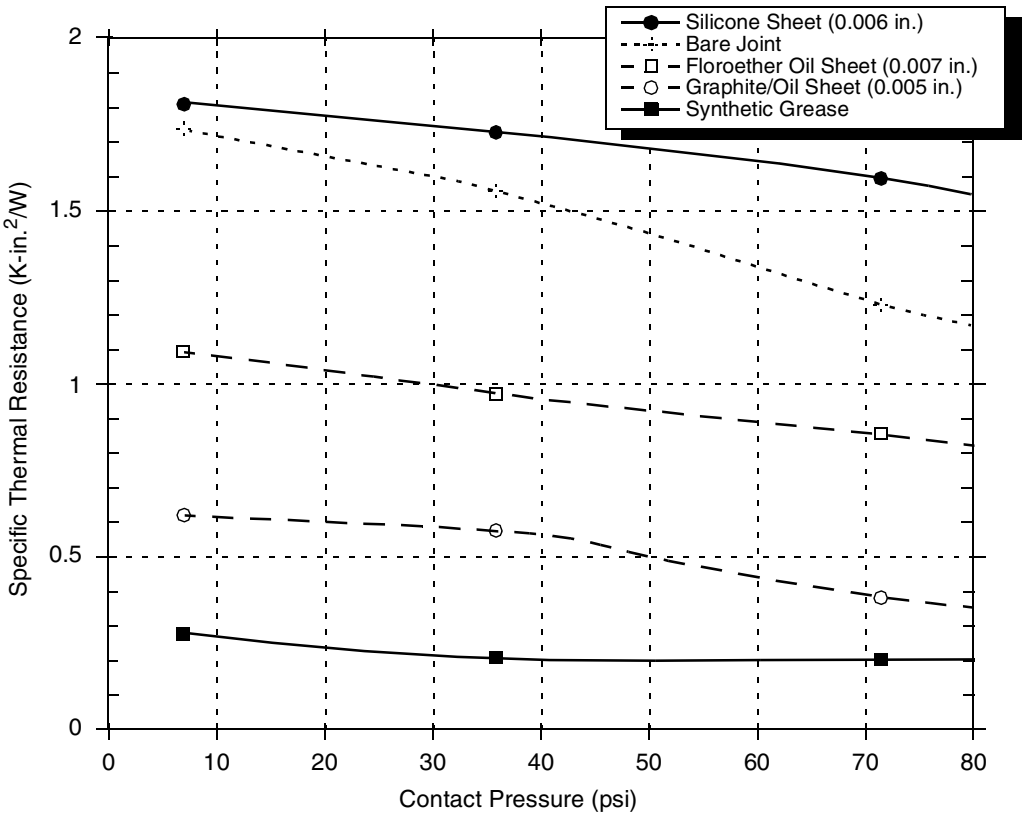


Figure 72. Thermal Performance of Select Thermal Interface Materials

The system board designer can choose between several types of thermal interface. There are several commercially-available thermal interfaces provided by the following vendors:

Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01888-4014 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials 2200 W. Salzburg Rd. Midland, MI 48686-0997 Internet: www.dow.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572

Thermagon Inc.
4707 Detroit Ave.
Cleveland, OH 44102
Internet: www.thermagon.com

888-246-9050

25 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8568E.

25.1 System Clocking

This device includes six PLLs, as follows:

1. The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 23.2, “CCB/SYSCLK PLL Ratio.”
2. The e500 core PLL generates the core clock using the platform clock as the input. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 23.3, “e500 Core PLL Ratio.”
3. The PCI PLL generates the clocking for the PCI bus
4. The local bus PLL generates the clock for the local bus.
5. There is a PLL for the SerDes block.
6. QE PLL generates the QE clock from the externally supplied SYSCLK.

25.2 Power Supply Design and Sequencing

25.2.1 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD_PLAT}, AV_{DD_CORE}, AV_{DD_PCI}, AV_{DD_LBIU}, and AV_{DD_SRDS}, AV_{DD_CE} respectively). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages will be derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in Figure 73, one to each of the AV_{DD} type pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} type pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} type pin, which is on the periphery of 1023FC-PBGA the footprint, without the inductance of vias.

Figure 73 shows the PLL power supply filter circuits for all PLLs except SerDes PLL.

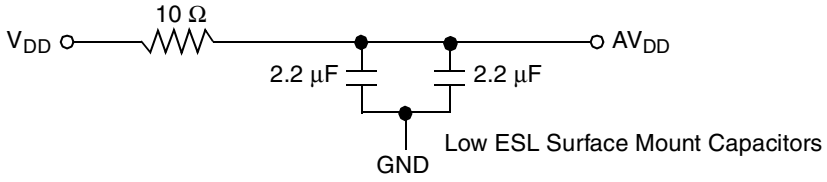
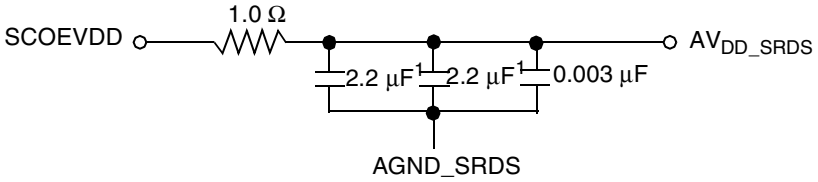


Figure 73. MPC8568E PLL Power Supply Filter Circuit

The AV_{DD_SRDS} signal provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following figure. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD_SRDS} and AGND_SRDS ball to ensure it filters out as much noise as possible. The 0.003-µF capacitor is closest to the ball, followed by the 2.2-µF capacitors, and finally the 1 ohm resistor to the board supply plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide and direct.



1. An 0805 sized capacitor is recommended for system initial bring-up.

Figure 74. SerDes PLL Power Supply Filter

Note the following:

- AV_{DD_SRDS} should be a filtered version of SCOREVDD.
- The transmitter output signals on the SerDes interface are fed from the XV_{DD} power plan.
- Power: XVDD consumes less than 300mW. SCOREVDD + AV_{DD_SRDS} consumes less than 750mW.

25.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. MPC8568E system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pin of the device. These decoupling capacitors should receive their power from separate $V_{DD,}TV_{DD}$, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

25.4 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power (SCOREVDD and XV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

- First, the board should have at least 10 x 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there should be a 1-µF ceramic chip capacitor on each side of the device. This should be done for all SerDes supplies.
- Third, between the device and any SerDes voltage regulator there should be a 10-µF, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100-µF, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

25.5 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. All unused active low inputs should be tied to $V_{DD,}$ TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD} and LV_{DD} as required. All unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external $V_{DD,}$ $L_{VDD,}$ TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD} and GND pins of the device.

25.6 Pull-Up and Pull-Down Resistor Requirements

The MPC8568E requires weak pull-up resistors (2–10 kΩ is recommended) on open drain type pins including I^2C pins and MPIC interrupt pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 75. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Refer to the PCI 2.2 specification for all pull-ups required for PCI.

The following pins must NOT be pulled down during power-on reset: HRESET_REQ, TRIG_OUT/READY/QUIESCE, MSRCID[2:4], ASLEEP, PA[5].

Three test pins also require pull-up resistors (100 Ω–1 KΩ). These pins are L1_TSTCLK, L2_TSTCLK, and LSSD_MODE. These signals are for factory use only and must be pulled up to OV_{DD} for normal machine operation.

Refer to the PCI 2.2 specification for all pull-ups required for PCI.

25.7 Configuration Pin Muxing

The MPC8568E provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins. These pins are generally used as output only pins in normal operation.

While HRESET is asserted however, these pins are treated as inputs. The value presented on these pins while HRESET is asserted, is latched when HRESET deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip pull-up resistors of approximately 20 kΩ. This value should permit the 4.7-kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during HRESET (and for platform /system clocks after HRESET deassertion to ensure capture of the reset value). When the HRESET is negated, the pull-up resistor is also disabled, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

25.8 JTAG Configuration Signals

Boundary scan testing is enabled through the JTAG interface signals. The TRST signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement Power Architecture. The device requires TRST to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, generally systems will assert TRST during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying TRST to HRESET is not practical.

The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert HRESET or TRST in order

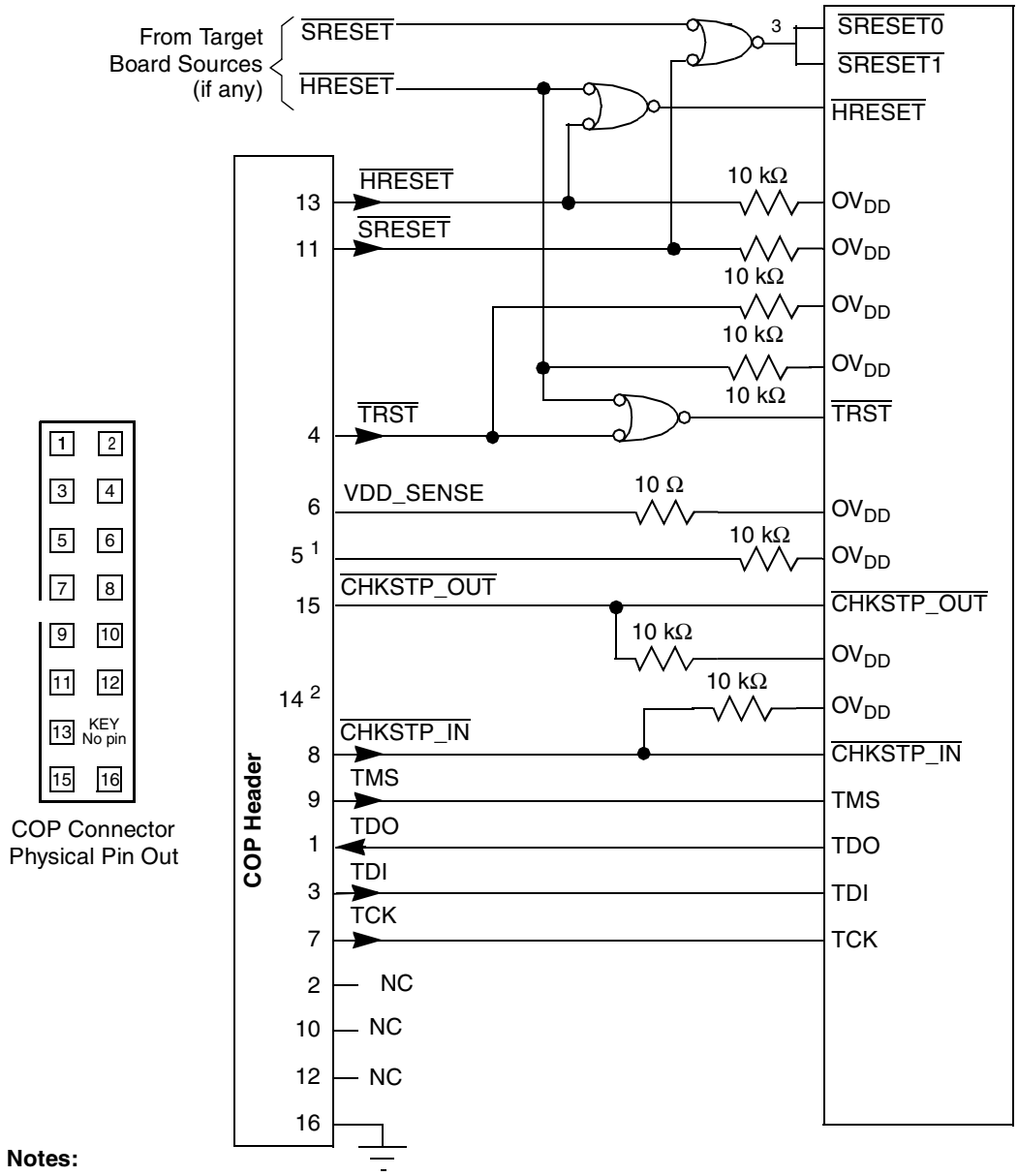
to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 75 allows the COP to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted.

The COP header shown in Figure 75 adds many benefits—breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface—and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header).

There is no standardized way to number the COP header shown in Figure 75; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 75 is common to all known emulators.



Notes:

1. RUN/$\overline{\text{STOP}}$, normally found on pin 5 of the COP header, is not implemented. Connect pin 5 of the COP header to OV_{DD} with a 10-kΩ pull-up resistor.
2. Key location; pin 14 is not physically present on the COP header.
3. Use a NOR gate with sufficient drive strength to drive two inputs.

Figure 75. JTAG Interface Connection

25.9 Guidelines for High-Speed Interface Termination

25.9.1 Unused output

Any of the outputs that are unused should be left unconnected. These signals are:

- SD_TX[7:0]

- $\overline{\text{SD\_TX}}$[7:0]

25.9.2 Unused input

25.9.2.1 SerDes block power not supplied

If the high speed interface is not used at all, then SCOREVDD/XVDD/AV_{DD_SRDS} can be tied to GND, all receiver inputs should be tied to the GND as well. This includes:

- SD_RX[7:0]
- $\overline{\text{SD\_RX}}$[7:0]
- SD_REF_CLK
- $\overline{\text{SD\_REF\_CLK}}$
- $\overline{\text{SD\_RX\_CLK}}$
- $\overline{\text{SD\_RX\_FRM\_CTL}}$

25.9.2.2 SerDes Interface Partly used

If the high-speed SerDes interface is partly unused, any of the unused receiver pins should be terminated as follows:

- SD_RX[7:0] = tied to SCOREGND
- $\overline{\text{SD\_RX}}$[7:0] = tied to SCOREGND
- SD_REF_CLK = tied to SCOREGND
- $\overline{\text{SD\_REF\_CLK}}$ = tied to SCOREGND

NOTE

Power down the unused lane through SERDESCR1[0:7] register (offset = 0xE_0F08) (This prevents the oscillations and holds the receiver output in a fixed state.) that maps to SERDES lane 0 to lane 7 accordingly.

During HRESET/POR, the high-speed interface must be in Serial RapidIO mode and/or PCI Express mode according to the state of the PE[8:10]. Software must disable this mode through DEVDISR[SRIO] or DEVDISR[PCIE] accordingly during software initialization.

26 Ordering Information

Contact your local Freescale sales office or regional marketing team for order information.

26.1 Part Marking

Parts are marked as the example shown in Figure 76.

FC-PBGA

Notes:

MPC856Xxxxxxx is the orderable part number
ATWLYYWW is the freescale assembly, year and workweek code
MMMMM is the mask code
CCCC is the contry code for assembly.
YWWLAZ is the trace code for assembly.

Figure 76. Part Marking for FC-PBGA Device

26.2 Part Number Decoder

Figure 77 shows the MPC8568E/MPC8567E number decoder.

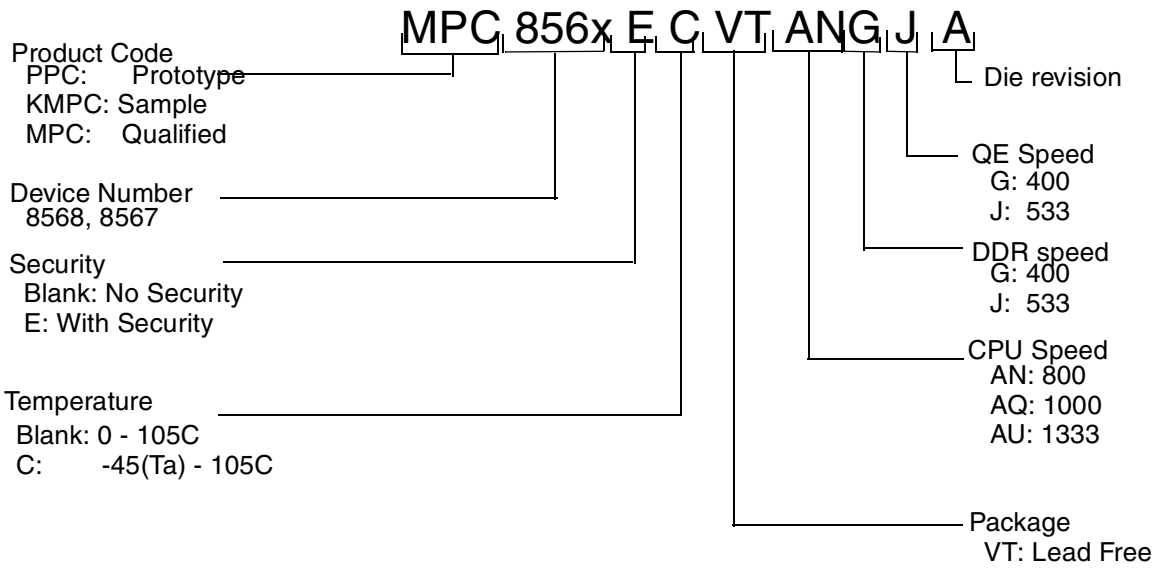


Figure 77. MPC8568E Part Number Decoder

27 Document Revision History

Table 88 provides a revision history for the MPC8568E hardware specification.

Table 88. Document Revision History

Rev Number	Date	Substantive Change(s)
1	10/2010	In Table 78, “MPC8568E Pinout Listing,” and Table 78, “MPC8568E Pinout Listing,” added footnote 49 to LGPL4.
0	05/2009	Initial public release.

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