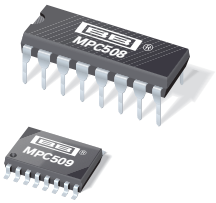
THE DATASHEET OF

MPC509AU/1K

Burr-Brown Products from Texas Instruments



MPC508A
MPC509A

SBFS019A – JANUARY 1988 — REVISED OCTOBER 2003

Single-Ended 8-Channel/Differential 4-Channel CMOS ANALOG MULTIPLEXERS

FEATURES

- **ANALOG OVERVOLTAGE PROTECTION: 70V_{PP}**
- **NO CHANNEL INTERACTION DURING OVERVOLTAGE**
- **BREAK-BEFORE-MAKE SWITCHING**
- **ANALOG SIGNAL RANGE: ±15V**
- **STANDBY POWER: 7.5mW typ**
- **TRUE SECOND SOURCE**

DESCRIPTION

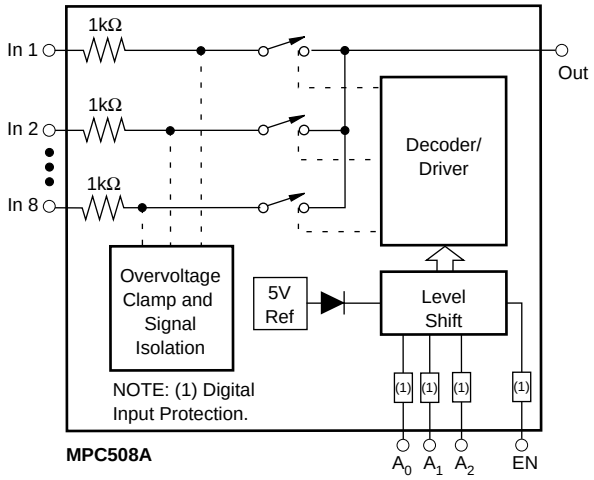
The MPC508A is an 8-channel single-ended analog multiplexer and the MPC509A is a 4-channel differential multiplexer.

The MPC508A and MPC509A multiplexers have input overvoltage protection. Analog input voltages may exceed either power supply voltage without damaging the device or disturbing the signal path of other channels. The protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand 70V_{PP} signal levels and standard ESD tests. Signal sources are protected from short circuits should multiplexer power loss occur; each input presents a 1kΩ resistance under this condition. Digital inputs can also sustain continuous faults up to 4V greater than either supply voltage.

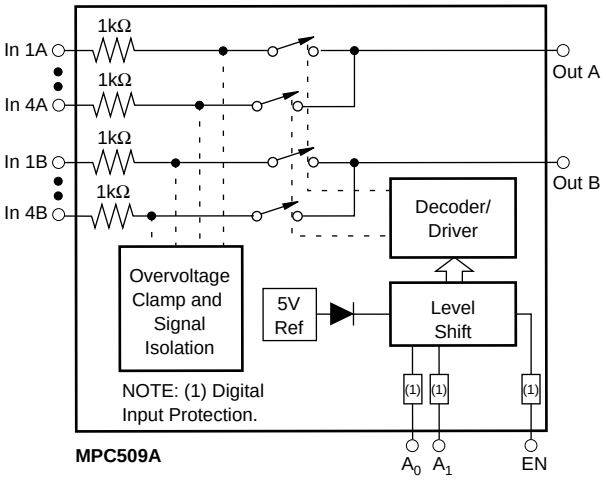
These features make the MPC508A and MPC509A ideal for use in systems where the analog signals originate from external equipment or separately powered sources.

The MPC508A and MPC509A are fabricated with Burr-Brown's dielectrically isolated CMOS technology. The multiplexers are available in plastic DIP and plastic SOIC packages. Temperature range is –40°C to +85°C.

FUNCTIONAL DIAGRAMS



MPC508A



MPC509A

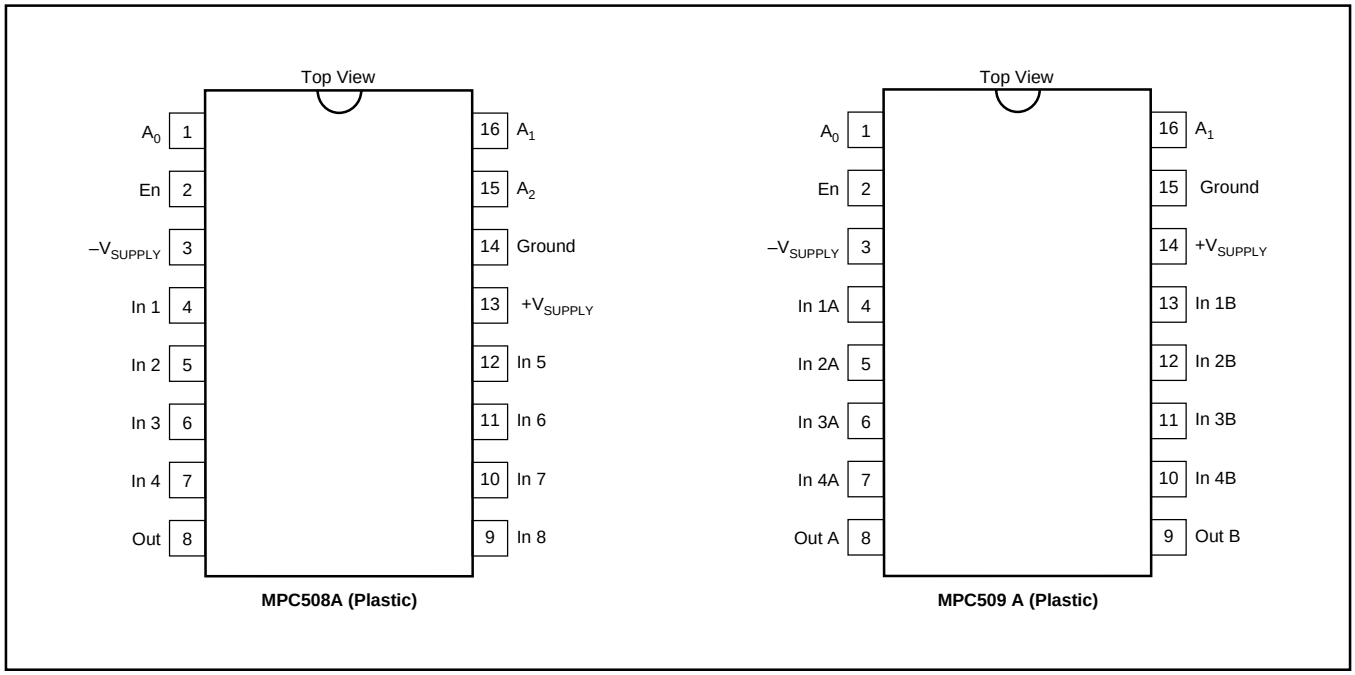
ELECTRICAL CHARACTERISTICS

Supplies = +15V, –15V; V_{AH} (Logic Level High) = +4.0V, V_{AL} (Logic Level Low) = +0.8V, unless otherwise specified.

PARAMETER	TEMP	MPC508A/509A MIN	MPC508A/509A TYP	MPC508A/509A MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS					
V_S, Analog Signal Range	Full	–15		+15	V
R_{ON}, On Resistance(1)	+25°C		1.3	1.5	kΩ
	Full		1.5	1.8	kΩ
I_S (OFF), Off Input Leakage Current	+25°C		0.5		nA
	Full			10	nA
I_D (OFF), Off Output Leakage Current	+25°C		0.2		nA
MPC508A	Full			5	nA
MPC509A	Full			5	nA
I_D (OFF) with Input Overvoltage Applied(2)	+25°C		2.0		µA
I_D (ON), On Channel Leakage Current	+25°C		2		nA
MPC508A	Full			10	nA
MPC509A	Full			10	nA
I_{DIFF} Differential Off Output Leakage Current (MPC509A Only)	Full			10	nA
DIGITAL INPUT CHARACTERISTICS					
V_{AL}, Input Low Threshold Drive	Full			0.8	V
V_{AH}, Input High Threshold(3)	Full	4.0			V
I_A, Input Leakage Current (High or Low)(4)	Full			1.0	µA
SWITCHING CHARACTERISTICS					
t_A, Access Time	+25°C		0.5		µs
	Full			0.6	µs
t_{OPEN}, Break-Before-Make Delay	+25°C	25	80		ns
t_{ON} (EN), Enable Delay (ON)	+25°C		200		ns
	Full			500	ns
t_{OFF} (EN), Enable Delay (OFF)	+25°C		250		ns
	Full			500	ns
Settling Time (0.1%)	+25°C		1.2		µs
(0.01%)	+25°C		3.5		µs
"OFF Isolation"(5)	+25°C	50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		5		pF
C_D (OFF), Channel Output Capacitance: MPC508A	+25°C		25		pF
MPC509A	+25°C		12		pF
C_A, Digital Input Capacitance	25°C		5		pF
C_{DS} (OFF), Input to Output Capacitance	+25°C		0.1		pF
POWER REQUIREMENTS					
P_D, Power Dissipation	Full		7.5		mW
I+, Current Pin 1(6)	Full		0.7	1.5	mA
I–, Current Pin 27(6)	Full		5	20	µA

NOTES: (1) V_{OUT} = ±10V, I_{OUT} = –100µA. (2) Analog overvoltage = ±33V. (3) To drive from DTL/TTL circuits. 1kΩ pull-up resistors to +5.0V supply are recommended. (4) Digital input leakage is primarily due to the clamp diodes. Typical leakage is less than 1nA at 25°C. (5) V_{EN} = 0.8V, R_L = 1kΩ, C_L = 15pF, V_S = 7Vrms, f = 100kHz. Worst-case isolation occurs on channel 4 due to proximity of the output pins. (6) V_{EN}, V_A = 0V or 4.0V.

PIN CONFIGURATIONS



TRUTH TABLES

MPC508A

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

MPC509A

A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	L	None
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

ABSOLUTE MAXIMUM RATINGS(1)

Voltage between supply pins 44V
V+ to ground 22V
V– to ground 25V
Digital input overvoltage V_{EN}, V_A:
V_{SUPPLY} (+) ..... +4V
V_{SUPPLY} (–) ..... –4V
or 20mA, whichever occurs first.
Analog input overvoltage V_S:
V_{SUPPLY} (+) ..... +20V
V_{SUPPLY} (–) ..... –20V
Continuous current, S or D 20mA
Peak current, S or D
(pulsed at 1ms, 10% duty cycle max) 40mA
Power dissipation(2) 1.28W
Operating temperature range ..... –40°C to +85°C
Storage temperature range ..... –65°C to +150°C

NOTE: (1) Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. (2) Derate 1.28mW/°C above T_A = +70°C.

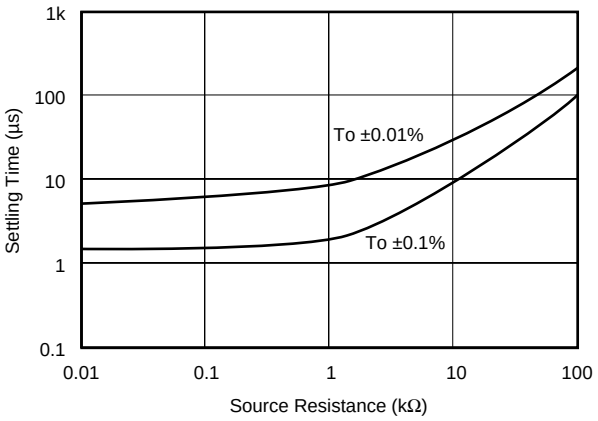
PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

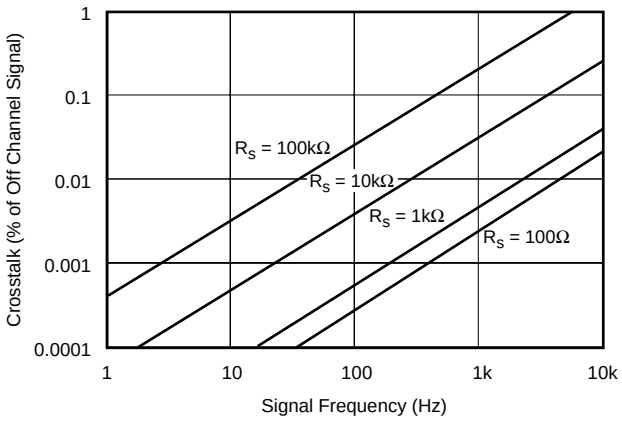
TYPICAL PERFORMANCE CURVES

Typical at +25°C unless otherwise noted.

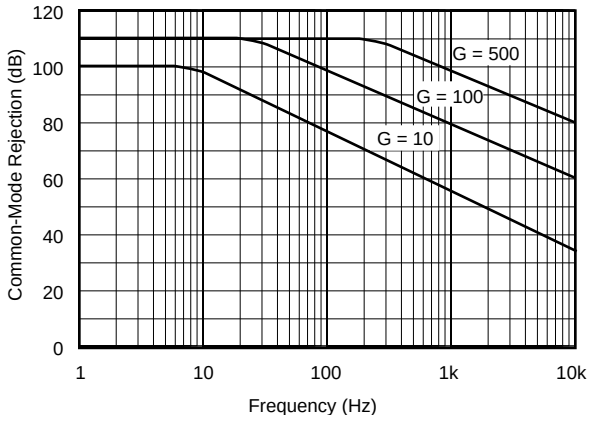
SETTLING TIME vs
SOURCE RESISTANCE FOR 20V STEP CHANGE



CROSSTALK vs SIGNAL FREQUENCY



COMBINED CMR vs
FREQUENCY MPC509A AND INA110



DISCUSSION OF PERFORMANCE

DC CHARACTERISTICS

The static or dc transfer accuracy of transmitting the multiplexer input voltage to the output depends on the channel ON resistance (R_{ON}), the load impedance, the source impedance, the load bias current and the multiplexer leakage current.

Single-Ended Multiplexer Static Accuracy

The major contributors to static transfer accuracy for single-ended multiplexers are:

Source resistance loading error;
Multiplexer ON resistance error;
and, dc offset error caused by both load bias current and multiplexer leakage current.

Resistive Loading Errors

The source and load impedances will determine the input resistive loading errors. To minimize these errors:

- *Keep loading impedance as high as possible.* This minimizes the resistive loading effects of the source resistance and multiplexer ON resistance. As a guideline, load impedances of $10^8\Omega$, or greater, will keep resistive loading errors to 0.002% or less for 1000Ω source impedances. A $10^6\Omega$ load impedance will increase source loading error to 0.2% or more.
- *Use sources with impedances as low as possible.* 1000Ω source resistance will present less than 0.001% loading error and $10k\Omega$ source resistance will increase source loading error to 0.01% with a 10^8 load impedance.

Input resistive loading errors are determined by the following relationship (see Figure 1).

Source and Multiplexer Resistive Loading Error

$$\in (R_S + R_{ON}) = \frac{R_S + R_{ON}}{R_S + R_{ON} + R_L} \times 100\%$$

where R_S = source resistance
R_L = load resistance
R_{ON} = multiplexer ON resistance

Input Offset Voltage

Bias current generates an input OFFSET voltage as a result of the IR drop across the multiplexer ON resistance and source resistance. A load bias current of 10nA will generate an offset voltage of $20\mu V$ if a $1k\Omega$ source is used. In general, for the MPC508A, the OFFSET voltage at the output is determined by:

$$V_{OFFSET} = (I_B + I_L)(R_{ON} + R_S)$$

where I_B = Bias current of device multiplexer is driving
I_L = Multiplexer leakage current
R_{ON} = Multiplexer ON resistance
R_S = source resistance

Differential Multiplexer Static Accuracy

Static accuracy errors in a differential multiplexer are difficult to control, especially when it is used for multiplexing low-level signals with full-scale ranges of 10mV to 100mV.

The matching properties of the multiplexer, source and output load play a very important part in determining the transfer accuracy of the multiplexer. The source impedance unbalance, common-mode impedance, load bias current mismatch, load differential impedance mismatch, and common-mode impedance of the load all contribute errors to the multiplexer. The multiplexer ON resistance mismatch, leakage current mismatch and ON resistance also contribute to differential errors.

The effects of these errors can be minimized by following the general guidelines described in this section, especially for low-level multiplexing applications. Refer to Figure 2.

Load (Output Device) Characteristics

- *Use devices with very low bias current.* Generally, FET input amplifiers should be used for low-level signals less than 50mV FSR. Low bias current bipolar input amplifiers are acceptable for signal ranges higher than 50mV FSR. Bias current matching will determine the input offset.
- The system dc common-mode rejection (CMR) can never be better than the combined CMR of the multiplexer and driven load. System CMR will be less than the device which has the lower CMR figure.
- Load impedances, differential and common-mode, should be $10^{10}\Omega$ or higher.

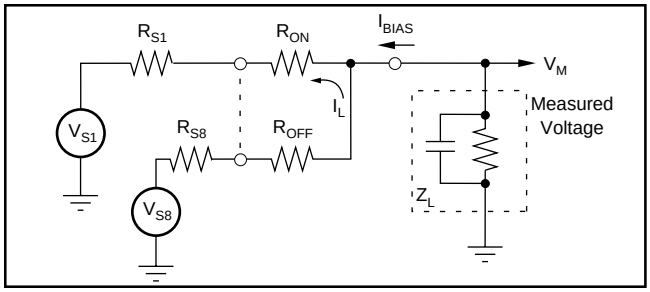


FIGURE 1. MPC508A DC Accuracy Equivalent Circuit.

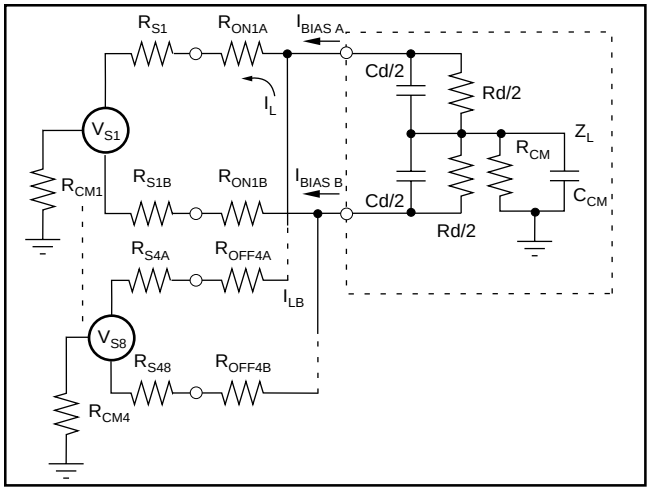


FIGURE 2. MPC509A DC Accuracy Equivalent Circuit.

Source Characteristics

- *The source impedance unbalance* will produce offset, common-mode and channel-to-channel gain-scatter errors. Use sources which do not have large impedance unbalances if at all possible.
- *Keep source impedances as low as possible* to minimize resistive loading errors.
- *Minimize ground loops.* If signal lines are shielded, ground all shields to a common point at the system analog common.

If the MPC509A is used for multiplexing high-level signals of ±1V to ±10V full-scale ranges, the foregoing precautions should still be taken, but the parameters are not as critical as for low-level signal applications.

DYNAMIC CHARACTERISTICS

Settling Time

The gate-to-source and gate-to-drain capacitance of the CMOS FET switches, the RC time constants of the source and the load determine the settling time of the multiplexer.

Governed by the charge transfer relation i = C (dV/dt), the charge currents transferred to both load and source by the analog switches are determined by the amplitude and rise time of the signal driving the CMOS FET switches and the gate-to-drain and gate-to-source junction capacitances as shown in Figures 3 and 4. Using this relationship, one can see that the amplitude of the switching transients, seen at the source and load, decrease proportionally as the capacitance of the load and source increase. The trade-off for reduced switching transient amplitude is increased settling time. In effect, the amplitude of the transients seen at the source and load are:

$$dV_L = (i/C)\ dt$$

where i = C (dV/dt) of the CMOS FET switches
C = load or source capacitance

The source must then redistribute this charge, and the effect of source resistance on settling time is shown in the Typical Performance Curves. This graph shows the settling time for a 20V step change on the input. The settling time for smaller step changes on the input will be less than that shown in the curve.

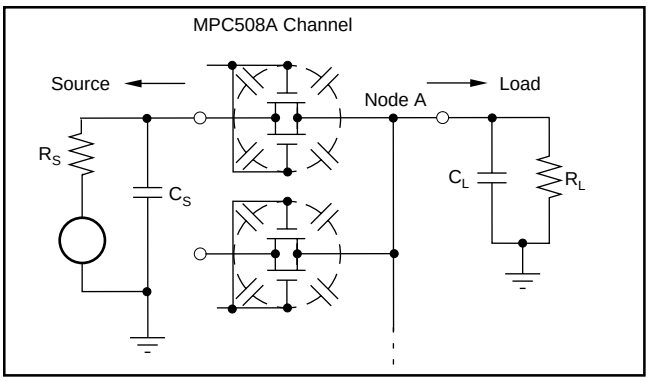


FIGURE 3. Settling Time Effects—MPC508A

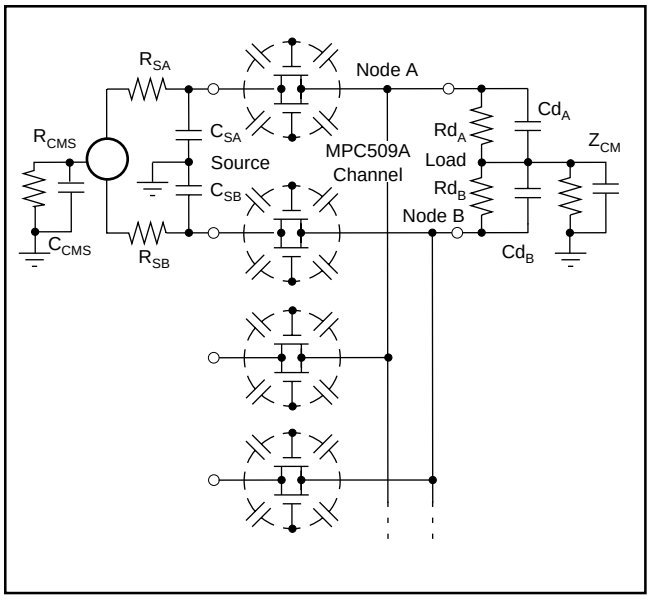


FIGURE 4. Settling and Common-Mode-Effects—MPC509A

Switching Time

This is the time required for the CMOS FET to turn ON after a new digital code has been applied to the Channel Address inputs. It is measured from the 50 percent point of the address input signal to the 90 percent point of the analog signal seen at the output for a 10V signal change between channels.

Crosstalk

Crosstalk is the amount of signal feedthrough from the three (MPC509A) or seven (MPC508A) OFF channels appearing at the multiplexer output. Crosstalk is caused by the voltage divider effect of the OFF channel, OFF resistance and junction capacitances in series with the R_{ON} and R_S impedances of the ON channel. Crosstalk is measured with a 20Vp-p 1kHz sine wave applied to all OFF channels. The crosstalk for these multiplexers is shown in the Typical Performance Curves.

Common-Mode Rejection (MPC509A Only)

The matching properties of the load, multiplexer and source affect the common-mode rejection (CMR) capability of a differentially multiplexed system. CMR is the ability of the multiplexer and input amplifier to reject signals that are common to both inputs, and to pass on only the signal difference to the output. For the MPC509A, protection is provided for common-mode signals of ±20V above the power supply voltages with no damage to the analog switches.

The CMR of the MPC509A and Burr-Brown's INA110 instrumentation amplifier is 110dB at DC to 10Hz (G = 100) with a 6dB/octave roll off to 70dB at 1000Hz. This measurement of CMR is shown in the Typical Performance Curves and is made with a Burr-Brown model INA110 instrumentation amplifier connected for gains of 10, 100, and 500.

Factors which will degrade multiplexer and system DC CMR are:

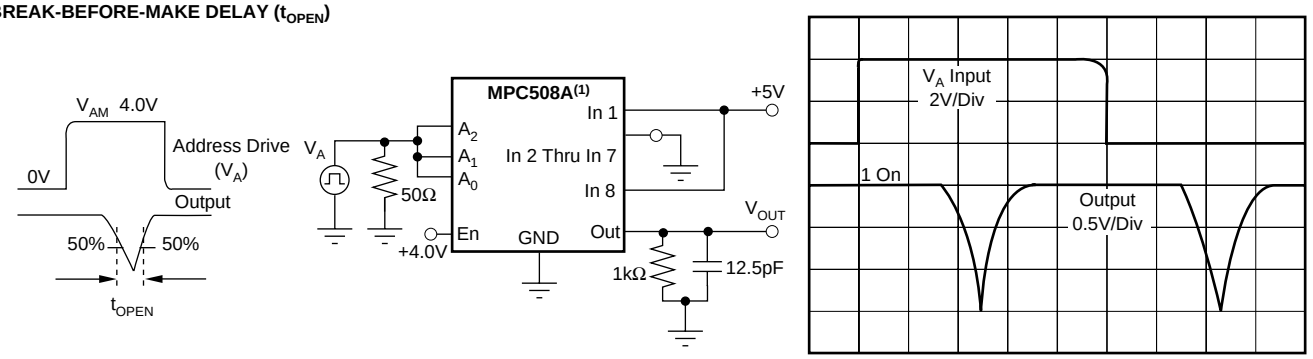
- Amplifier bias current and differential impedance mismatch
- Load impedance mismatch
- Multiplexer impedance and leakage current mismatch
- Load and source common-mode impedance

AC CMR roll off is determined by the amount of common-mode capacitances (absolute and mismatch) from each signal line to ground. Larger capacitances will limit CMR at higher frequencies; thus, if good CMR is desired at higher frequencies, the common-mode capacitances and unbalance of signal lines and multiplexer-to-amplifier wiring must be minimized. Use twisted-shielded-pair signal lines wherever possible.

SWITCHING WAVEFORMS

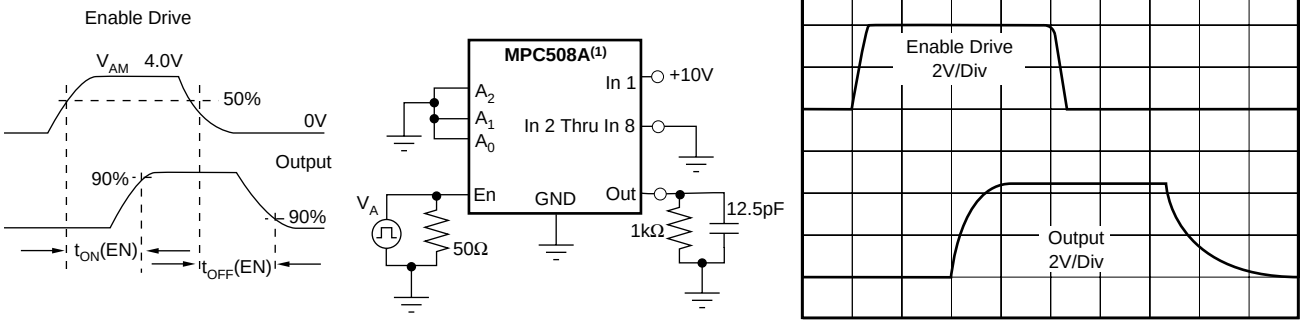
Typical at +25°C, unless otherwise noted.

BREAK-BEFORE-MAKE DELAY (t_{OPEN})



NOTE: (1) Similar connection for MPC509A.

ENABLE DELAY (t_{ON} (EN), t_{OFF} (EN))

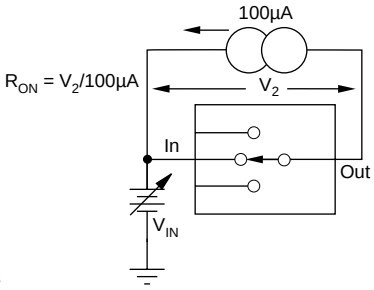


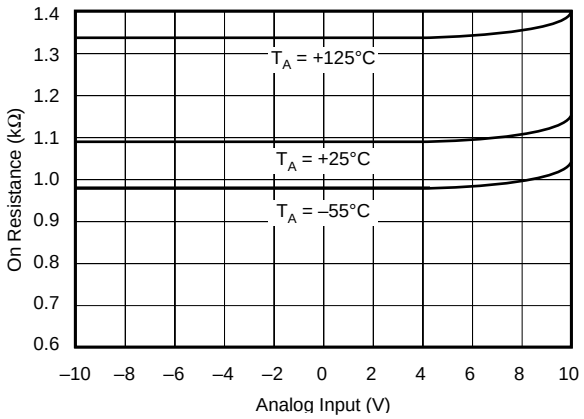
NOTE: (1) Similar connection for MPC509A.

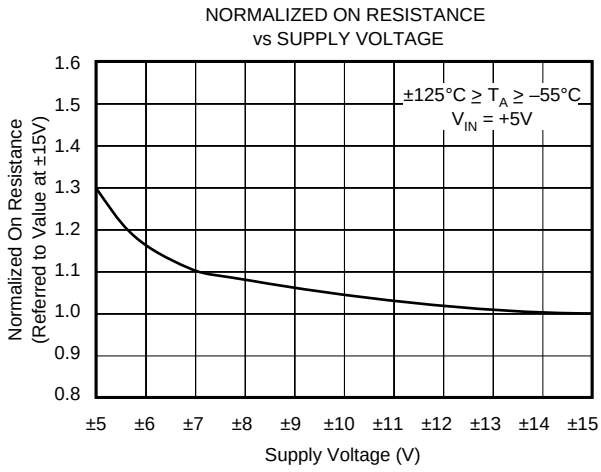
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

Unless otherwise specified: T_A = +25, V_S = ±15V, V_{AM} = +4V, V_{AL} = 0.8V.

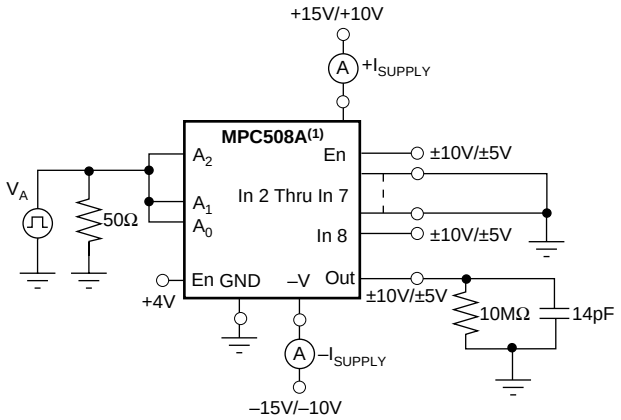
ON RESISTANCE vs ANALOG INPUT SIGNAL, SUPPLY VOLTAGE



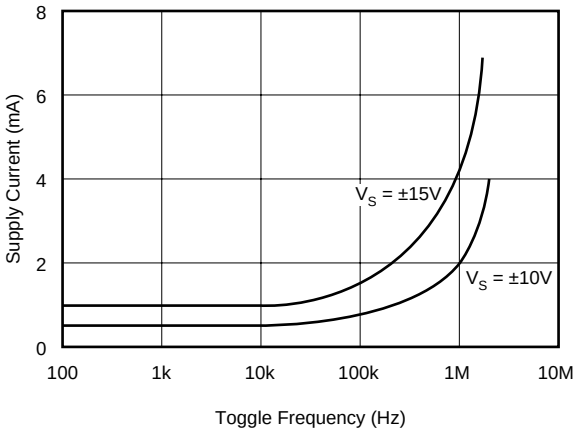




SUPPLY CURRENT vs TOGGLE FREQUENCY

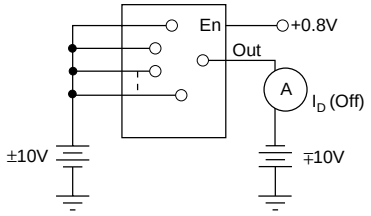


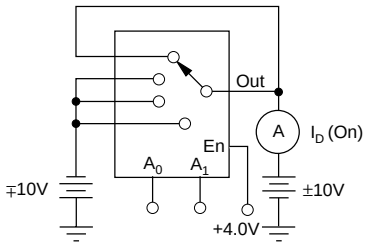
NOTE: (1) Similar connection for MPC509A.

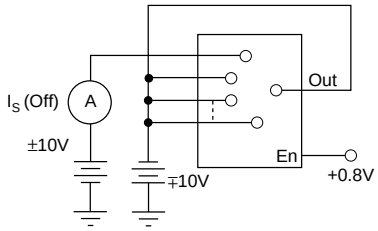


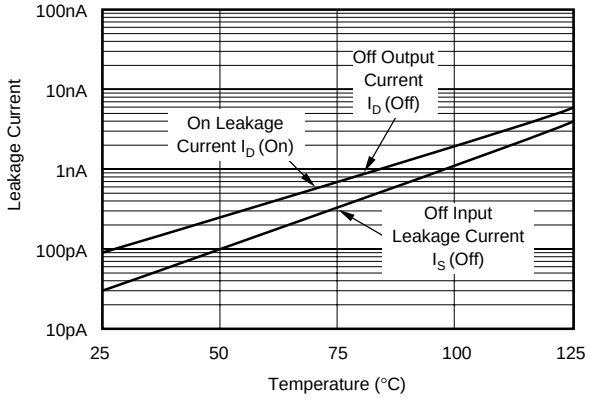
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (CONT)

LEAKAGE CURRENT vs TEMPERATURE



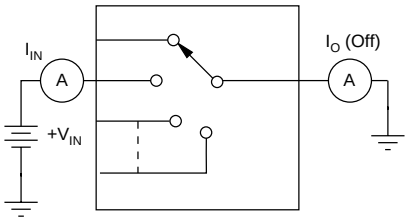


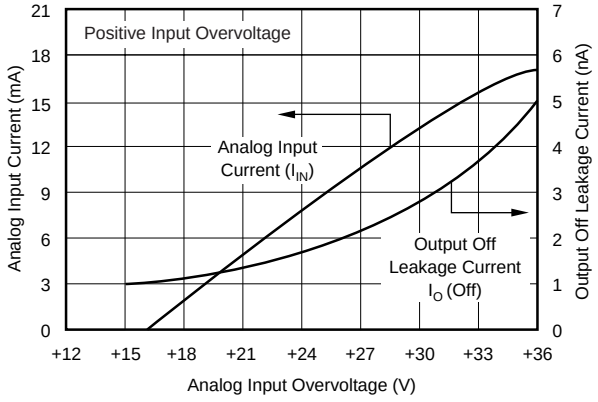


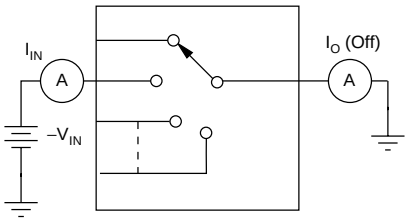


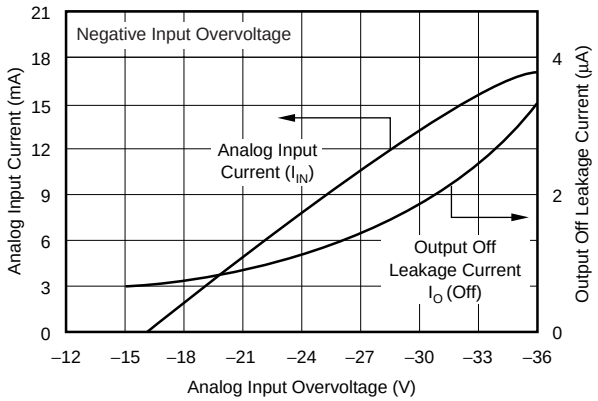
NOTE: (1) Two measurements per channel: +10V/–10V and –10V/+10V. (Two measurements per device for I_D (Off): +10V/–10V and –10V/+10V).

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



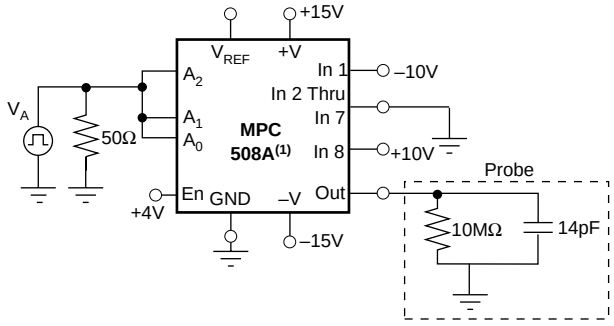




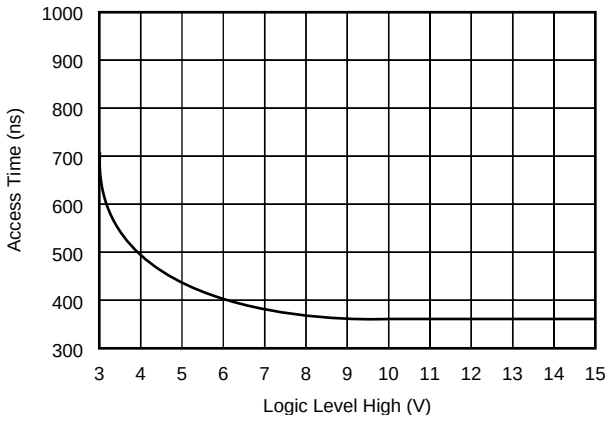


PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (CONT)

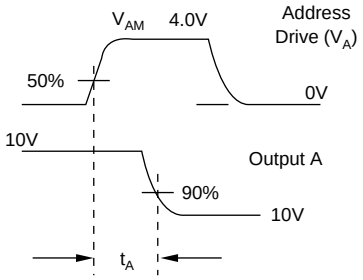
ACCESS TIME vs LOGIC LEVEL (High)

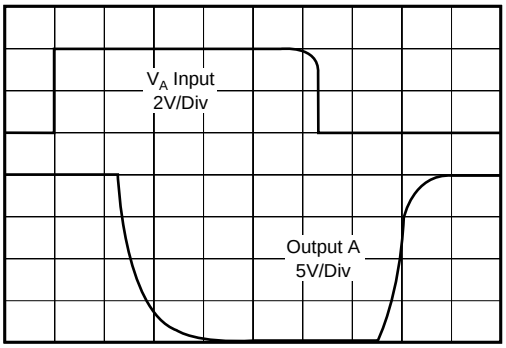


NOTE: (1) Similar connection for MPC509A.

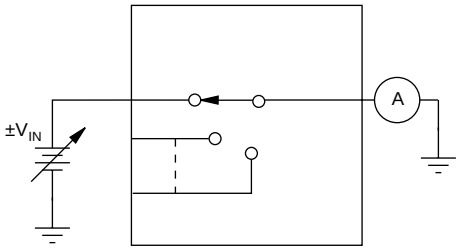


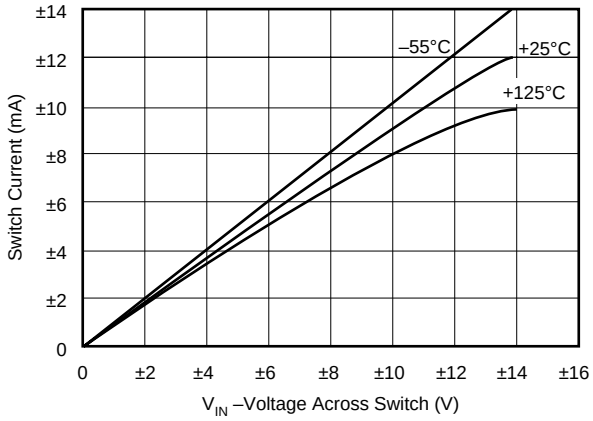
ACCESS TIME WAVEFORM





ON-CHANNEL CURRENT vs VOLTAGE





INSTALLATION AND OPERATING INSTRUCTIONS

The ENABLE input, pin 2, is included for expansion of the number of channels on a single node as illustrated in Figure 5. With ENABLE line at a logic 1, the channel is selected by the 2-bit (MPC509A) or 3-bit (MPC508A) Channel Select Address (shown in the Truth Tables). If ENABLE is at logic 0, all channels are turned OFF, even if the Channel Address Lines are active. If the ENABLE line is not to be used, simply tie it to $+V_{SUPPLY}$.

If the +15V and/or –15V supply voltage is absent or shorted to ground, the MPC509A and MPC508A multiplexers will not be damaged; however, some signal feedthrough to the output will occur. Total package power dissipation must not be exceeded.

For best settling speed, the input wiring and interconnections between multiplexer output and driven devices should be kept as short as possible. When driving the digital inputs from TTL, open collector output with pull-up resistors are recommended

To preserve common-mode rejection of the MPC509A, use twisted-shielded pair wire for signal lines and inter-tier connections and/or multiplexer output lines. This will help common-mode capacitance balance and reduce stray signal pickup. If shields are used, all shields should be connected as close as possible to system analog common or to the common-mode guard driver.

CHANNEL EXPANSION

Single-Ended Multiplexer (MPC508A)

Up to 32 channels (four multiplexers) can be connected to a single node, or up to 64 channels using nine MPC508A multiplexers on a two-tiered structure as shown in Figures 5 and 6.

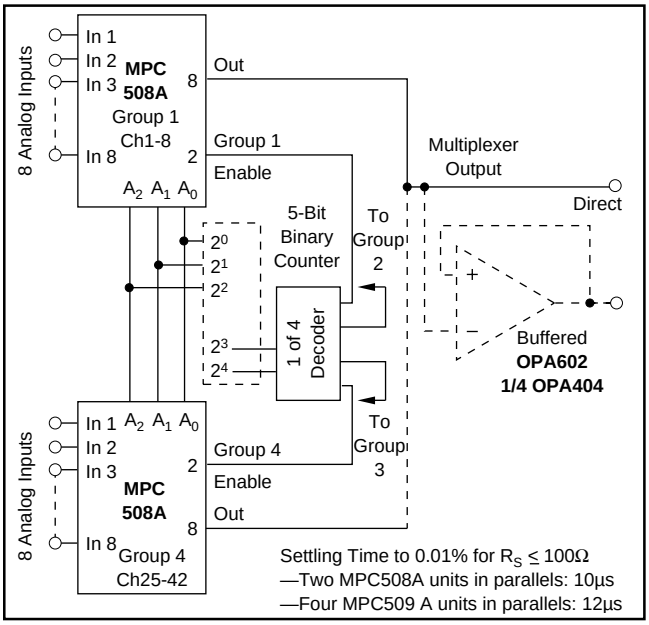


FIGURE 5. 32-Channel, Single-Tier Expansion.

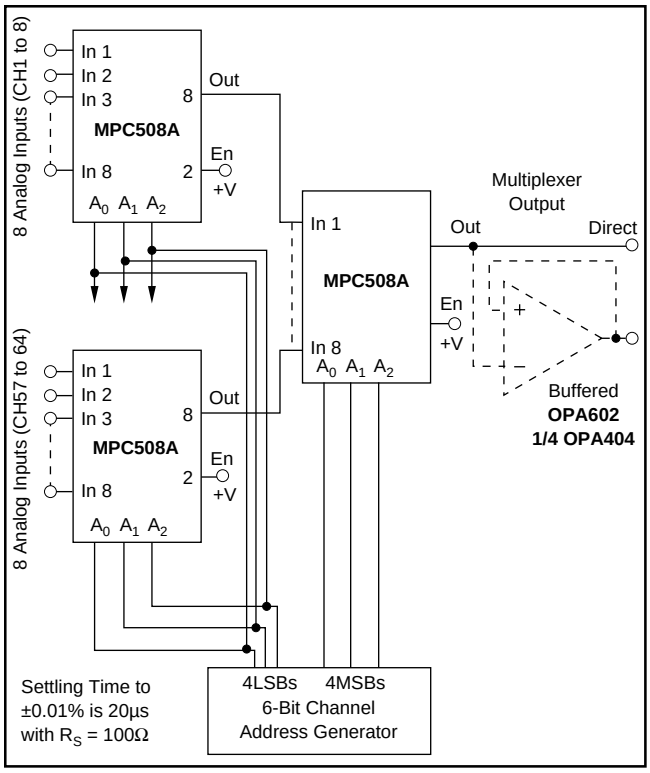


FIGURE 6. Channel Expansion Up to 64 Channels Using 8 x 8 Two-Tiered Expansion.

Differential Multiplexer (MPC509A)

Single or multitiered configurations can be used to expand multiplexer channel capacity up to 32 channels using a 32 x 1 or 16 channels using a 4 x 4 configuration.

Single-Node Expansion

The 32 x 1 configuration is simply eight (MPC509A) units tied to a single node. Programming is accomplished with a 5-bit counter, using the 2LSBs of the counter to control Channel Address inputs A_0 and A_1 and the 3MSBs of the counter to drive a 1-of-8 decoder. The 1-of-8 decoder then is used to drive the ENABLE inputs (pin 2) of the MPC509A multiplexers.

Two-Tier Expansion

Using a 4 x 4 two-tier structure for expansion to 16 channels, the programming is simplified. A 4-bit counter output does not require a 1-of-8 decoder. The 2LSBs of the counter drive the A_0 and A_1 inputs of the four first-tier multiplexers and the 2MSBs of the counter are applied to the A_0 and A_1 inputs of the second-tier multiplexer.

Single vs Multitiered Channel Expansion

In addition to reducing programming complexity, two-tier configuration offers the added advantages over single-node expansion of reduced OFF channel current leakage (reduced OFFSET), better CMR, and a more reliable configuration if a channel should fail in the ON condition (short). Should a channel fail ON in the single-node configuration, data cannot be taken from any channel, whereas only one channel group is failed (4 or 8) in the multitiered configuration.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MPC508AP	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type		MPC508AP	Samples
MPC508AU	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MPC508AU	Samples
MPC508AU/1K	ACTIVE	SOIC	DW	16	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MPC508AU	Samples
MPC508AU/1KG4	ACTIVE	SOIC	DW	16	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MPC508AU	Samples
MPC508AUG4	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MPC508AU	Samples
MPC509AP	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type		MPC509AP	Samples
MPC509AU	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		MPC509AU	Samples
MPC509AU/1K	ACTIVE	SOIC	DW	16	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MPC509AU	Samples
MPC509AU/1KG4	ACTIVE	SOIC	DW	16	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MPC509AU	Samples
MPC509AUG4	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MPC509AU	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

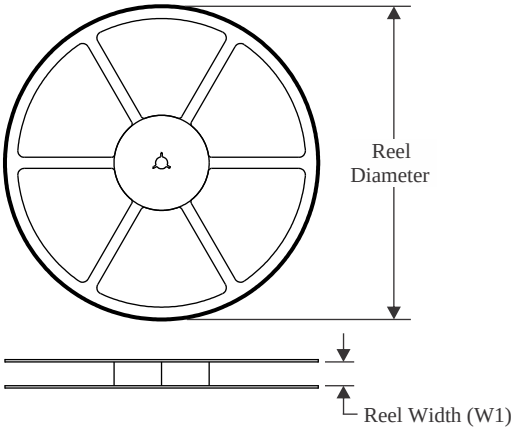
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

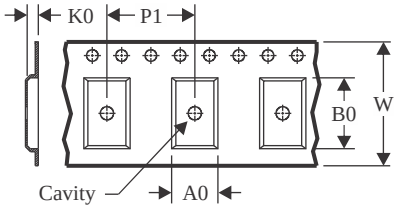
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

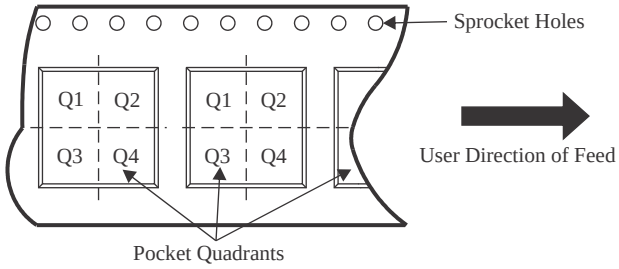


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

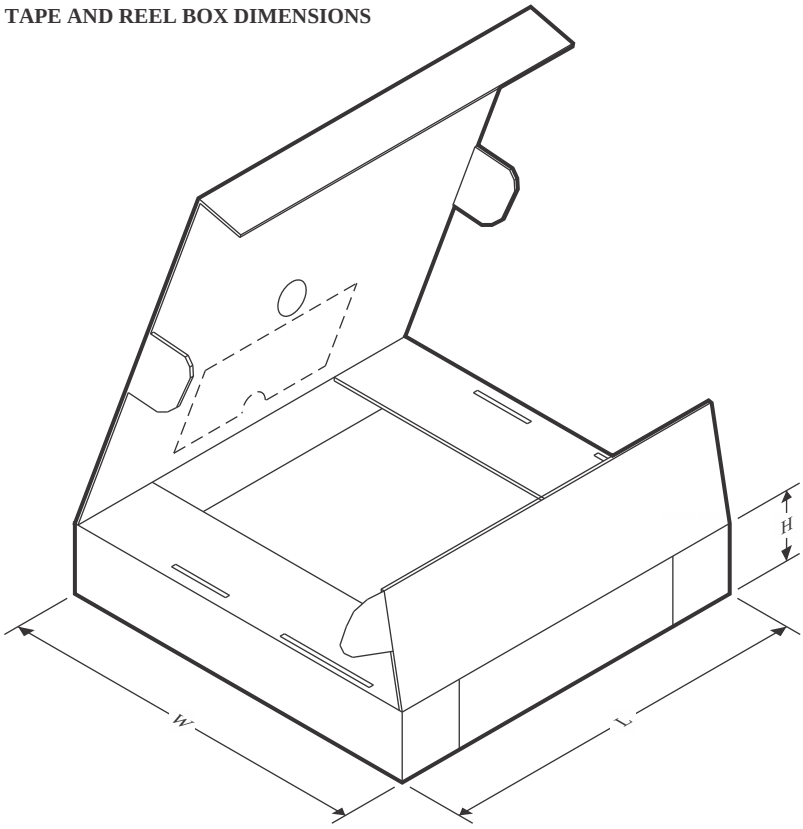
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MPC508AU/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
MPC509AU/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

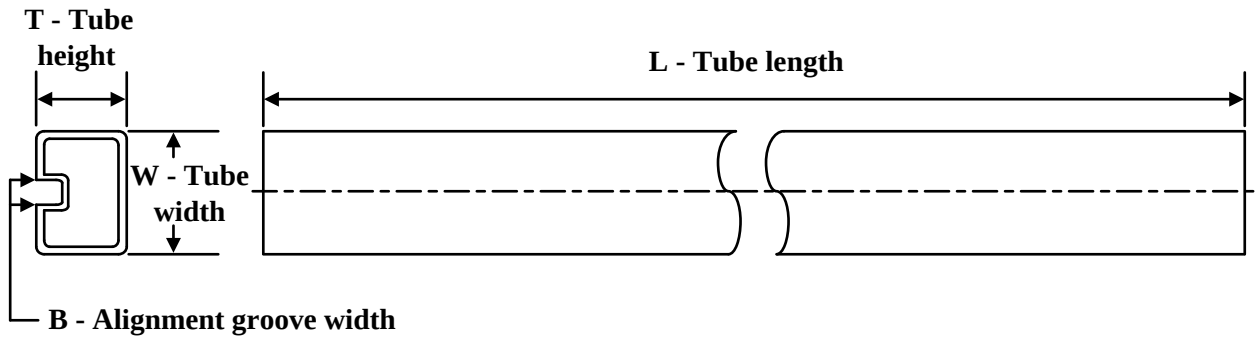
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MPC508AU/1K	SOIC	DW	16	1000	350.0	350.0	43.0
MPC509AU/1K	SOIC	DW	16	1000	356.0	356.0	35.0

TUBE



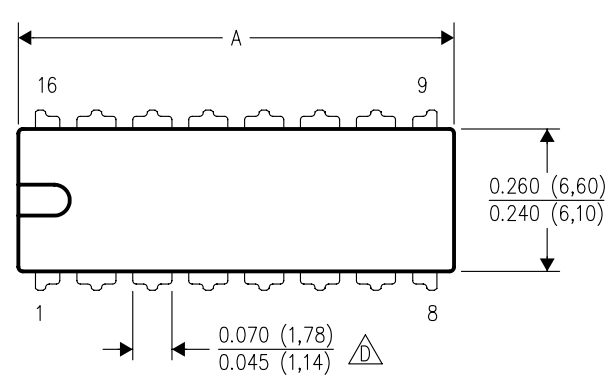
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
MPC508AP	N	PDIP	16	25	506	13.97	11230	4.32
MPC508AU	DW	SOIC	16	40	506.98	12.7	4826	6.6
MPC508AUG4	DW	SOIC	16	40	506.98	12.7	4826	6.6
MPC509AP	N	PDIP	16	25	506	13.97	11230	4.32
MPC509AU	DW	SOIC	16	40	507	12.83	5080	6.6
MPC509AUG4	DW	SOIC	16	40	507	12.83	5080	6.6

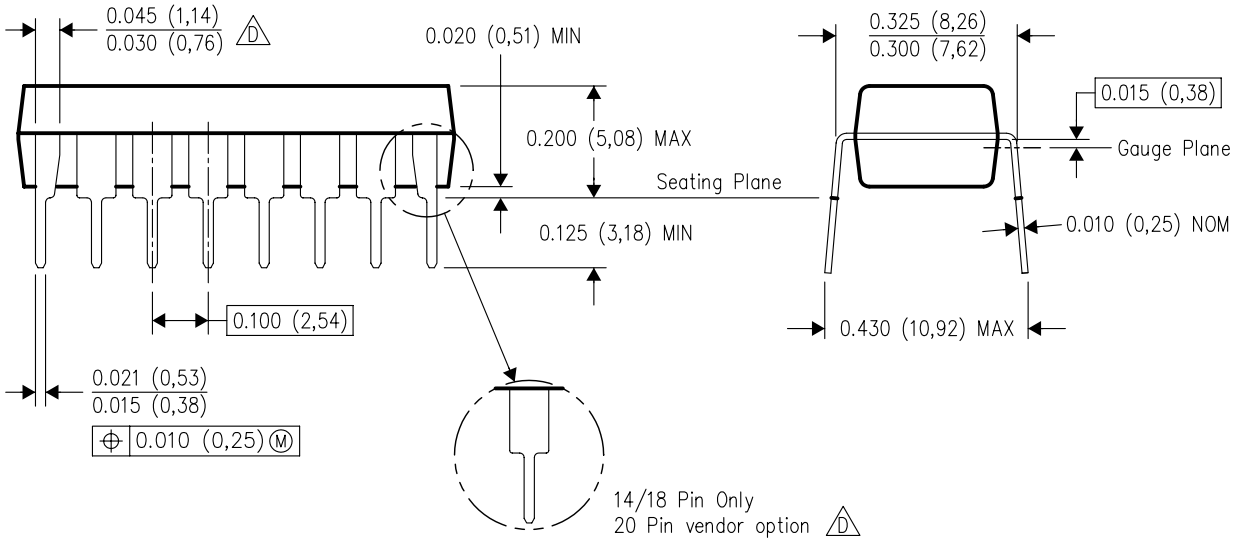
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

GENERIC PACKAGE VIEW

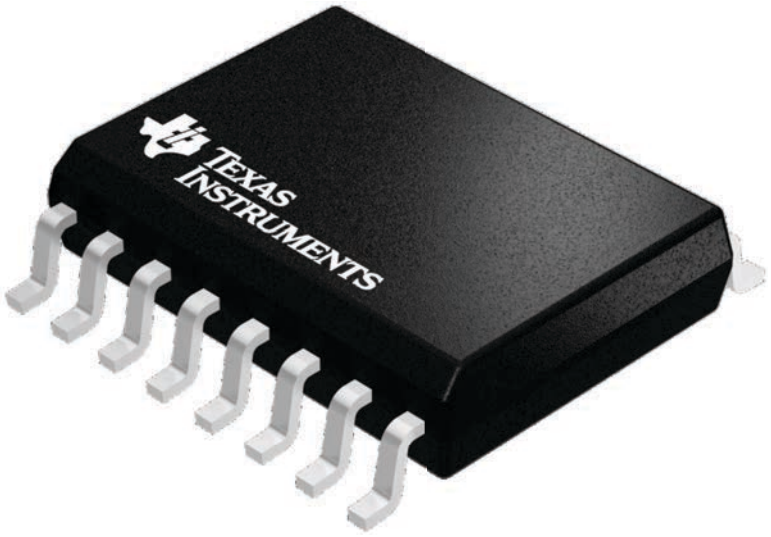
DW 16

SOIC - 2.65 mm max height

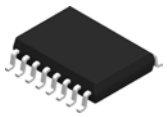
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

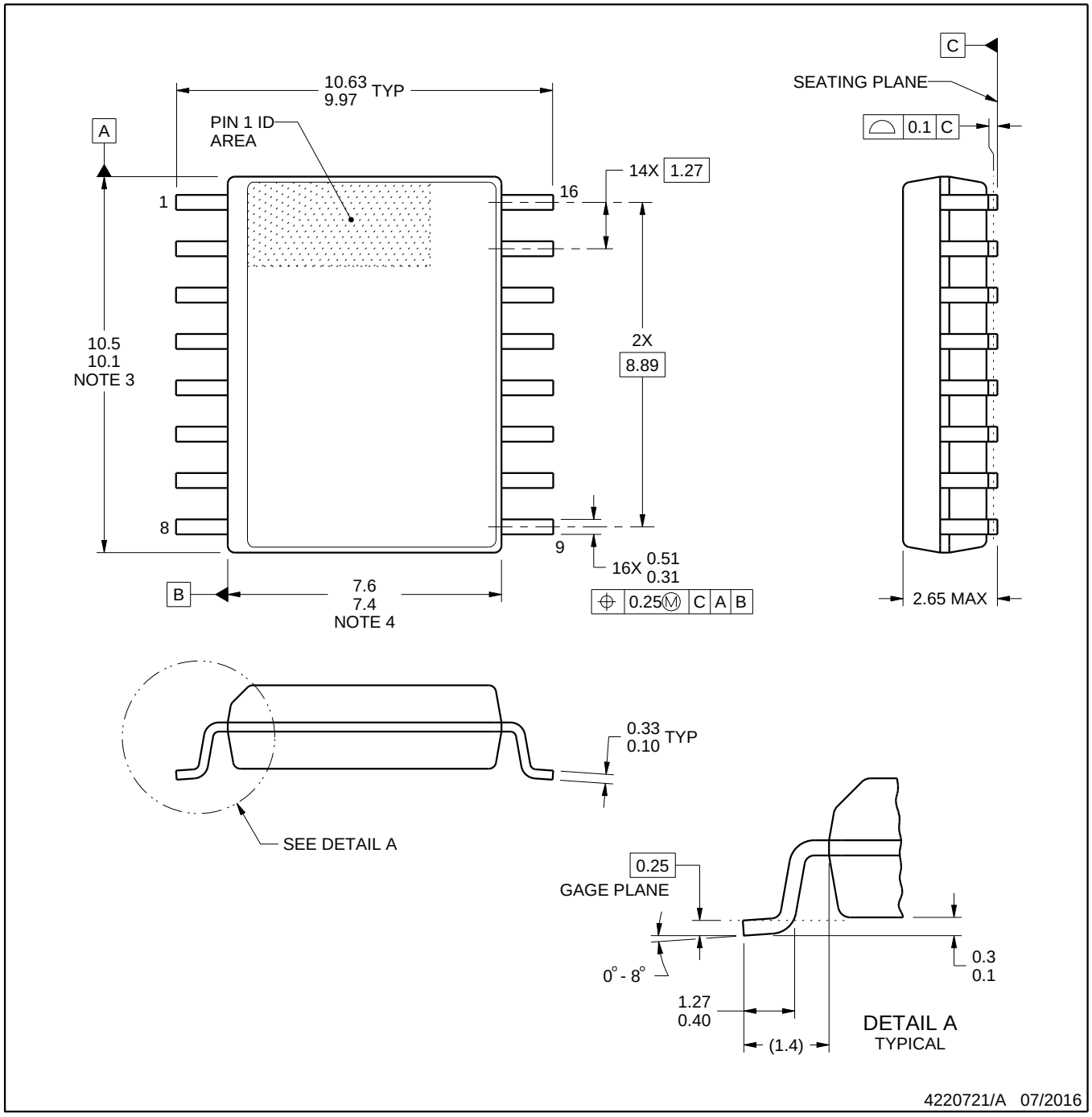


PACKAGE OUTLINE

DW0016A

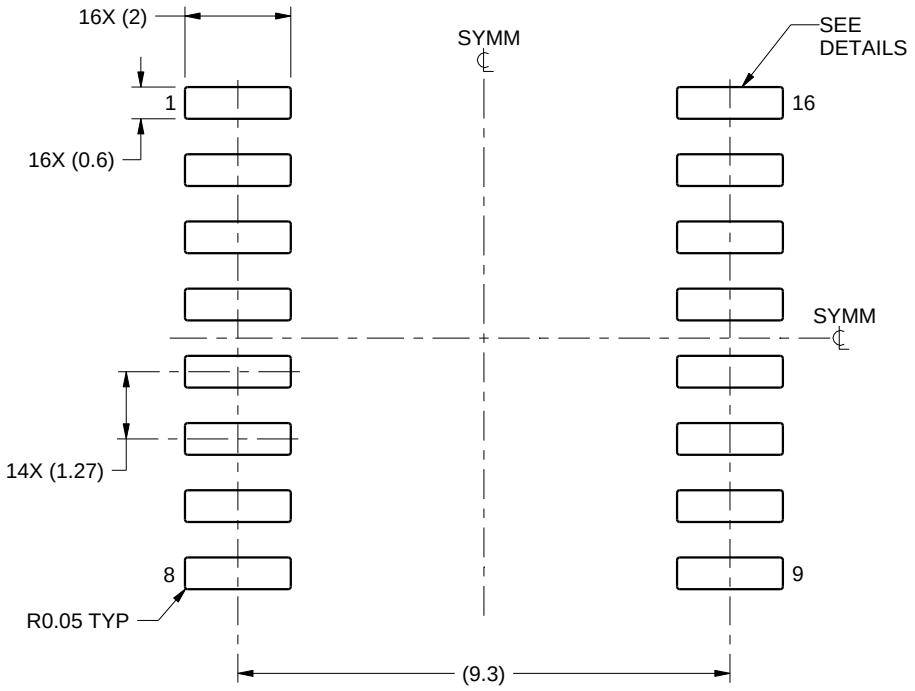
SOIC - 2.65 mm max height

SOIC

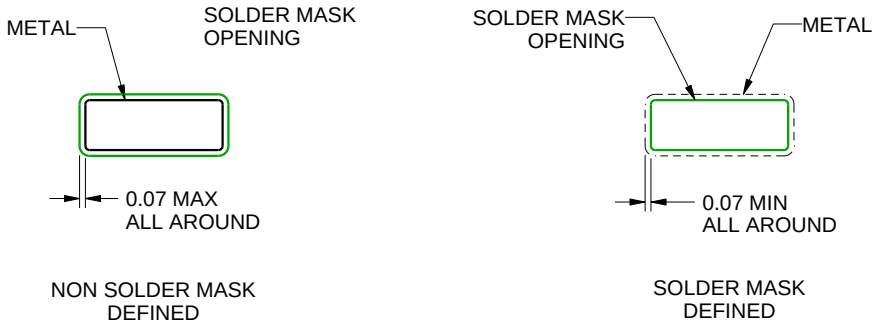


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

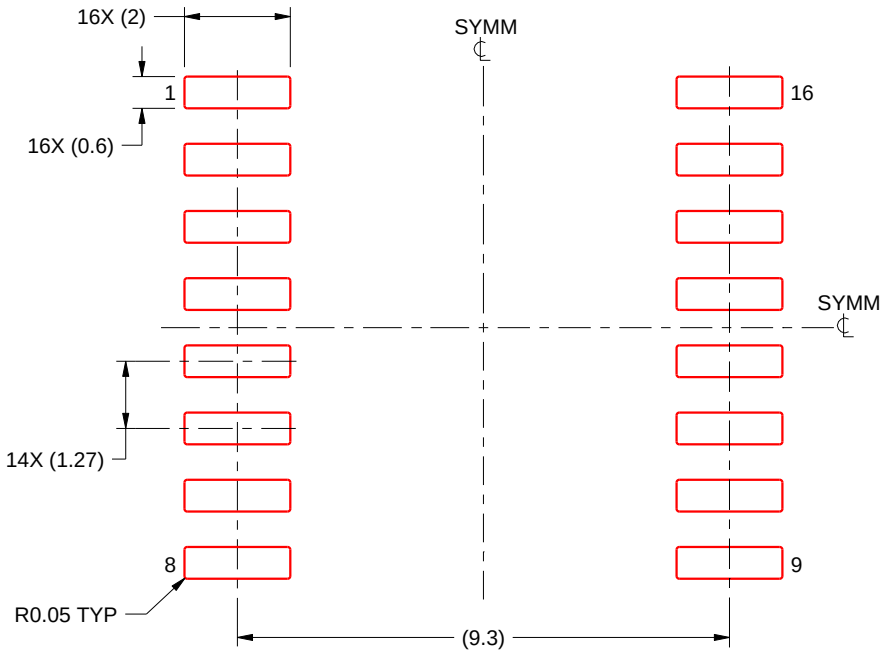


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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