



**THE DATASHEET OF
MM74HC126MX**



3-STATE Quad Buffers

MM74HC125, MM74HC126

General Description

The MM74HC125 and MM74HC126 are general purpose 3-STATE high speed non-inverting buffers utilizing advanced silicon-gate CMOS technology. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits. Both circuits are capable of driving up to 15 low power Schottky inputs.

The MM74HC125 require the 3-STATE control input C to be taken high to put the output into the high impedance condition, whereas the MM74HC126 require the control input to be low to put the output into high impedance.

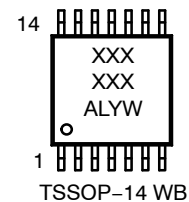
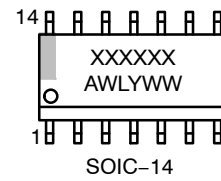
All inputs are protected from damage due to static discharge by diodes to VCC and ground.

Features

- Typical Propagation Delay: 13 ns
- Wide Operating Voltage Range: 2 V – 6 V
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 160 μA maximum (74HC Series)
- Fanout of 15 LS-TTL Loads
- These Devices are Pb-Free, Halide Free and are RoHS Compliant



MARKING DIAGRAM



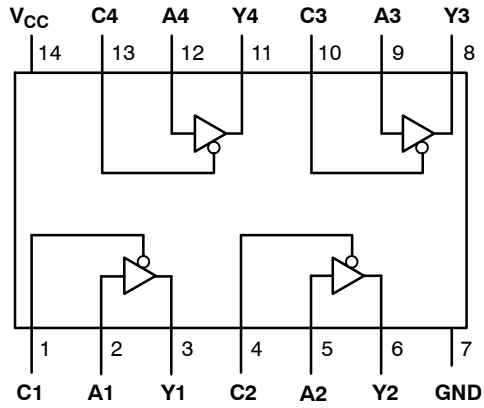
XXXXX = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week

ORDERING INFORMATION

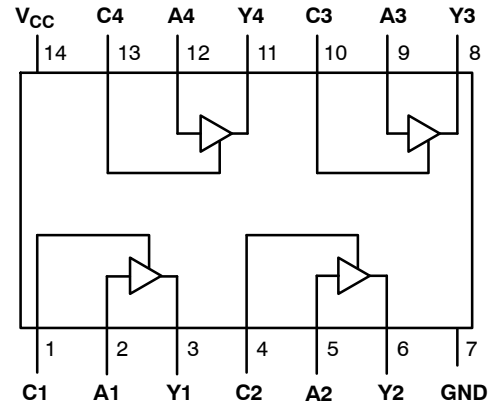
See detailed ordering and shipping information on page 6 of this data sheet.

MM74HC125, MM74HC126

Connection Diagram



Top View (MM74HC125)



Top View (MM74HC126)

Figure 1. Pin Assignments for SOIC and TSSOP

TRUTH TABLE (MM74HC125)

Inputs		Output
A	C	Y
H	L	H
L	L	L
X	H	Z

TRUTH TABLE (MM74HC126)

Inputs		Output
A	C	Y
H	H	H
L	H	L
X	L	Z

MM74HC125, MM74HC126

ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	-0.5 to +6.5 V
V_{IN}	DC Input Voltage	-0.5 to $V_{CC} + 0.5$ V
V_{OUT}	DC Output Voltage	-0.5 to $V_{CC} + 0.5$ V
I_{IK}, I_{OK}	Clamp Diode Current	± 20 mA
I_{OUT}	DC Output Current, per Pin	35 mA
I_{CC}	DC V_{CC} or GND Current, per Pin	± 70 mA
T_{STG}	Storage Temperature Range	-65°C to +150°C
P_D	Power Dissipation	SOIC TSSOP 1077 mW 833 mW
T_L	Lead Temperature (Soldering 10 Seconds)	260°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Unless otherwise specified all voltages are referenced to ground.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit	
V_{CC}	Supply Voltage	2	6	V	
V_{IN}, V_{OUT}	DC Input or Output Voltage	0	V_{CC}	V	
T_A	Operating Temperature Range	-55	+125	°C	
t_r, t_f	Input Rise or Fall Time	$V_{CC} = 2.0$ V	-	1000	ns
		$V_{CC} = 4.5$ V	-	500	ns
		$V_{CC} = 6.0$ V	-	400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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DC CHARACTERISTICS (Note 2)

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C		T _A = -40°C	T _A = -55°C	Unit
				Typ	Guaranteed Limits			
V _{IH}	Minimum HIGH Level Input Voltage		2.0	-	1.5	1.5	1.5	V
			4.5	-	3.15	3.15	3.15	
			6.0	-	4.2	4.2	4.2	
V _{IL}	Maximum LOW Level Input Voltage		2.0	-	0.5	0.5	0.5	V
			4.5	-	1.35	1.35	1.35	
			6.0	-	1.8	1.8	1.8	
V _{OH}	Minimum HIGH Level Output Voltage	V _{IN} = V _{IH} or V _{IL} , I _{OUT} ≤ 20 μA	2.0	2.0	1.9	1.9	1.9	V
			4.5	4.5	4.4	4.4	4.4	
			6.0	6.0	5.9	5.9	5.9	
		4.5	4.2	3.98	3.84	3.7		
		6.0	5.7	5.48	5.34	5.2		
V _{OL}	Maximum LOW Level Output Voltage	V _{IN} = V _{IH} or V _{IL} , I _{OUT} ≤ 20 μA	2.0	0	0.1	0.1	0.1	V
			4.5	0	0.1	0.1	0.1	
			6.0	0	0.1	0.1	0.1	
		4.5	0.2	0.26	0.33	0.4		
		6.0	0.2	0.26	0.33	0.4		
I _{OZ}	Maximum 3-STATE Output Leakage Current	V _{IN} = V _{IH} or V _{IL} , V _{OUT} = V _{CC} or GND C _n = Disabled	6.0	-	±0.5	±5	±10	μA
I _{IN}	Maximum Input Current	V _{IN} = V _{CC} or GND	6.0	-	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND, I _{OUT} = 0 μA	6.0	-	8.0	80	160	μA

2. For a power supply of 5 V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5 V. Thus the 4.5 V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5 V and 4.5 V respectively. (The V_{IH} value at 5.5 V is 3.85 V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0 V values should be used.

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AC CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $C_L = 45\text{ pF}$, $t_r = t_f = 6\text{ ns}$)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Unit
t_{PHL} , t_{PLH}	Maximum Propagation Delay Time		13	18	ns
t_{PZH}	Maximum Output Enable Time to HIGH Level	$R_L = 1\text{ k}\Omega$	13	25	ns
t_{PHZ}	Maximum Output Disable Time from HIGH Level	$R_L = 1\text{ k}\Omega$, $C_L = 5\text{ pF}$	17	25	ns
t_{PZL}	Maximum Output Enable Time to LOW Level	$R_L = 1\text{ k}\Omega$	18	25	ns
t_{PLZ}	Maximum Output Disable Time from LOW Level	$R_L = 1\text{ k}\Omega$, $C_L = 5\text{ pF}$	13	25	ns

AC CHARACTERISTICS ($V_{CC} = 2.0\text{ V}$ to 6.0 V , $C_L = 50\text{ pF}$, $t_r = t_f = 6\text{ ns}$ (unless otherwise specified))

Symbol	Parameter	V_{CC} (V)	Conditions	$T_A = 25^\circ\text{C}$		$T_A = -40^\circ\text{C}$ to 85°C	$T_A = -55^\circ\text{C}$ to 125°C	Unit
				Typ	Guaranteed Limits			
t_{PHL} , t_{PLH}	Maximum Propagation Delay Time	2.0		40	100	125	150	ns
		4.5		14	20	25	30	
		6.0		12	17	21	25	
t_{PLH} , t_{PHL}	Maximum Propagation Delay Time	2.0	$C_L = 150\text{ pF}$,	35	130	163	195	ns
		4.5		14	26	33	39	
		6.0		12	22	28	39	
t_{PZH} , t_{PZL}	Maximum Output Enable Time	2.0	$R_L = 1\text{ k}\Omega$	25	125	156	188	ns
		4.5		14	25	31	38	
		6.0		12	21	26	31	
t_{PHZ} , t_{PLZ}	Maximum Output Disable Time	2.0	$R_L = 1\text{ k}\Omega$	25	125	156	188	ns
		4.5		14	25	31	38	
		6.0		12	21	26	31	
t_{PZL} , t_{PZH}	Maximum Output Enable Time	2.0	$C_L = 150\text{ pF}$, $R_L = 1\text{ k}\Omega$	35	140	175	210	ns
		4.5		15	28	35	42	
		6.0		13	24	30	36	
t_{TLH} , t_{THL}	Maximum Output Rise and Fall Time	2.0	$C_L = 50\text{ pF}$	30	60	75	90	ns
		4.5		7	12	15	18	
		6.0		6	10	13	15	
C_{IN}	Input Capacitance			5	10	10	10	pF
C_{OUT}	Output Capacitance Outputs			15	20	20	20	pF
C_{PD}	Power Dissipation Capacitance (per gate) (Note 3)		Enabled	45	-	-	-	pF
			Disabled	6	-	-	-	

3. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

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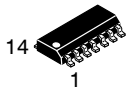
ORDERING INFORMATION

Part Number	Marking	Package	Shipping [†]
MM74HC125M	HC125A	SOIC-14, Case 751A (Pb-Free, Halide Free)	55 Units / Tube
MM74HC125MX	HC125A	SOIC-14, Case 751A (Pb-Free, Halide Free)	2500 / Tape & Reel
MM74HC125MTC	HC 125A	TSSOP-14, Case 948G (Pb-Free, Halide Free)	96 Units / Tube
MM74HC125MTCX	HC 125A	TSSOP-14 WB, Case 948G (Pb-Free, Halide Free)	2500 / Tape & Reel
MM74HC126M	HC126A	SOIC-14, Case 751A (Pb-Free, Halide Free)	55 Units / Tube
MM74HC126MX	HC126A	SOIC-14, Case 751EF (Pb-Free, Halide Free)	2500 / Tape & Reel
MM74HC126MTCX	HC 126A	TSSOP-14 WB, Case 948G (Pb-Free, Halide Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NOTE: Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

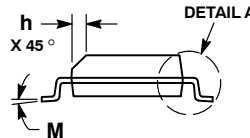
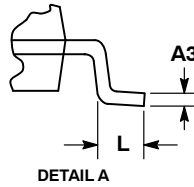
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-14 NB
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

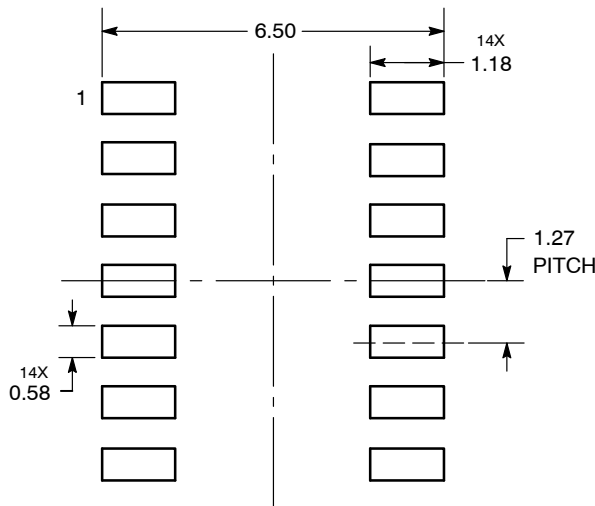


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

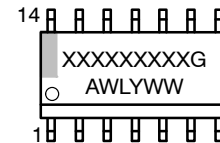
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC-14
CASE 751A-03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. NO CONNECTION
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 2:
 CANCELLED

STYLE 3:
 PIN 1. NO CONNECTION
 2. ANODE
 3. ANODE
 4. NO CONNECTION
 5. ANODE
 6. NO CONNECTION
 7. ANODE
 8. ANODE
 9. ANODE
 10. NO CONNECTION
 11. ANODE
 12. ANODE
 13. NO CONNECTION
 14. COMMON CATHODE

STYLE 4:
 PIN 1. NO CONNECTION
 2. CATHODE
 3. CATHODE
 4. NO CONNECTION
 5. CATHODE
 6. NO CONNECTION
 7. CATHODE
 8. CATHODE
 9. CATHODE
 10. NO CONNECTION
 11. CATHODE
 12. CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 5:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. NO CONNECTION
 7. COMMON ANODE
 8. COMMON CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. ANODE/CATHODE
 12. ANODE/CATHODE
 13. NO CONNECTION
 14. COMMON ANODE

STYLE 6:
 PIN 1. CATHODE
 2. CATHODE
 3. CATHODE
 4. CATHODE
 5. CATHODE
 6. CATHODE
 7. CATHODE
 8. ANODE
 9. ANODE
 10. ANODE
 11. ANODE
 12. ANODE
 13. ANODE
 14. ANODE

STYLE 7:
 PIN 1. ANODE/CATHODE
 2. COMMON ANODE
 3. COMMON CATHODE
 4. ANODE/CATHODE
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. ANODE/CATHODE
 8. ANODE/CATHODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. COMMON CATHODE
 12. COMMON ANODE
 13. ANODE/CATHODE
 14. ANODE/CATHODE

STYLE 8:
 PIN 1. COMMON CATHODE
 2. ANODE/CATHODE
 3. ANODE/CATHODE
 4. NO CONNECTION
 5. ANODE/CATHODE
 6. ANODE/CATHODE
 7. COMMON ANODE
 8. COMMON ANODE
 9. ANODE/CATHODE
 10. ANODE/CATHODE
 11. NO CONNECTION
 12. ANODE/CATHODE
 13. ANODE/CATHODE
 14. COMMON CATHODE

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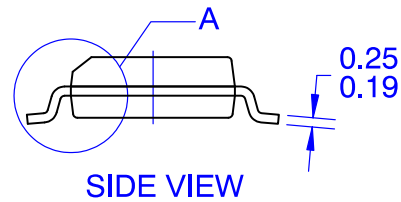
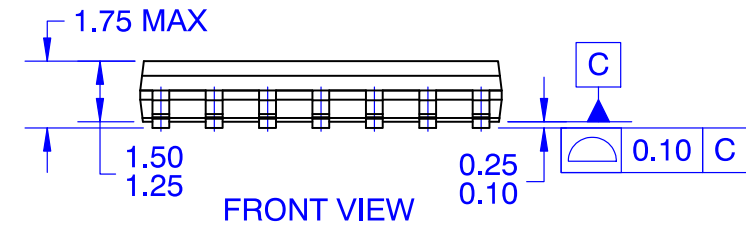
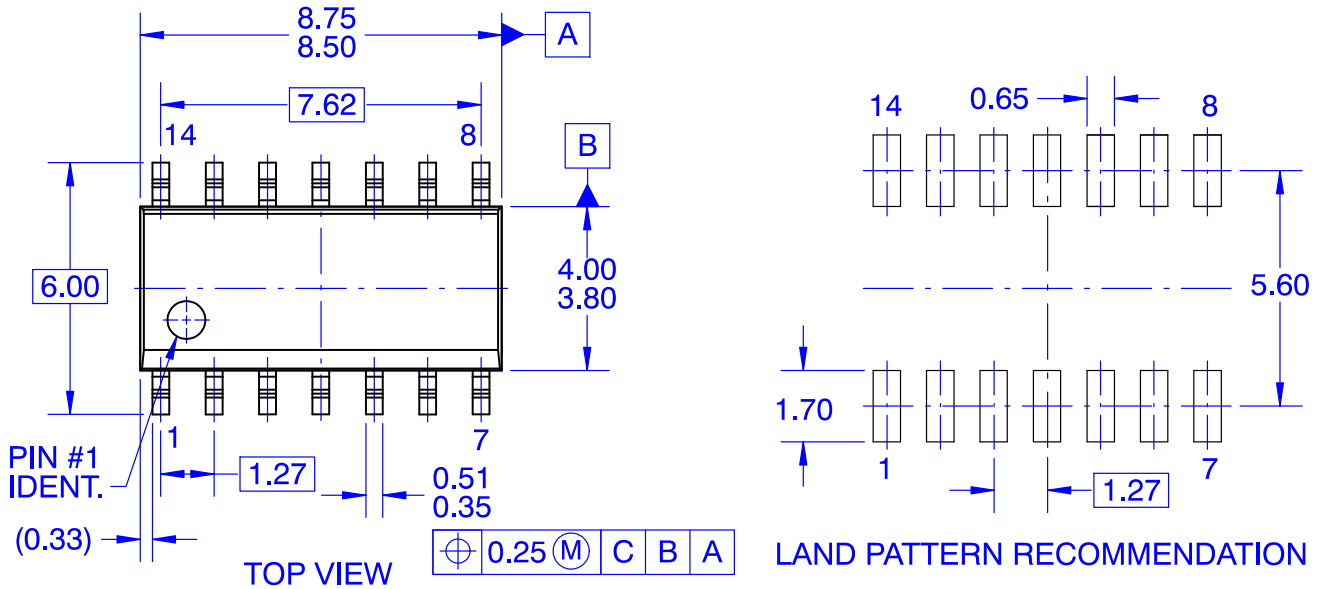
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®



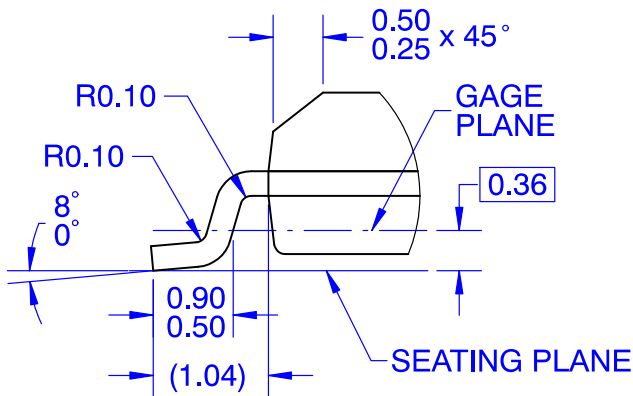
SOIC14
CASE 751EF
ISSUE O

DATE 30 SEP 2016



NOTES:

- A. CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C
- B. ALL DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
- D. LAND PATTERN STANDARD: SOIC127P600X145-14M
- E. CONFORMS TO ASME Y14.5M, 2009

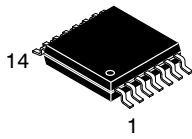


DETAIL A
SCALE 16 : 1

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



TSSOP-14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016

SCALE 2:1



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

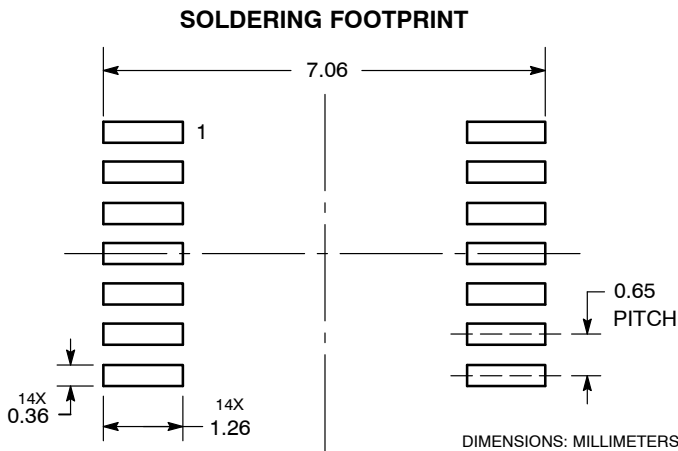
GENERIC MARKING DIAGRAM*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



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