THE DATASHEET OF

ML4812IQ

ML4812

Power Factor Controller

Features

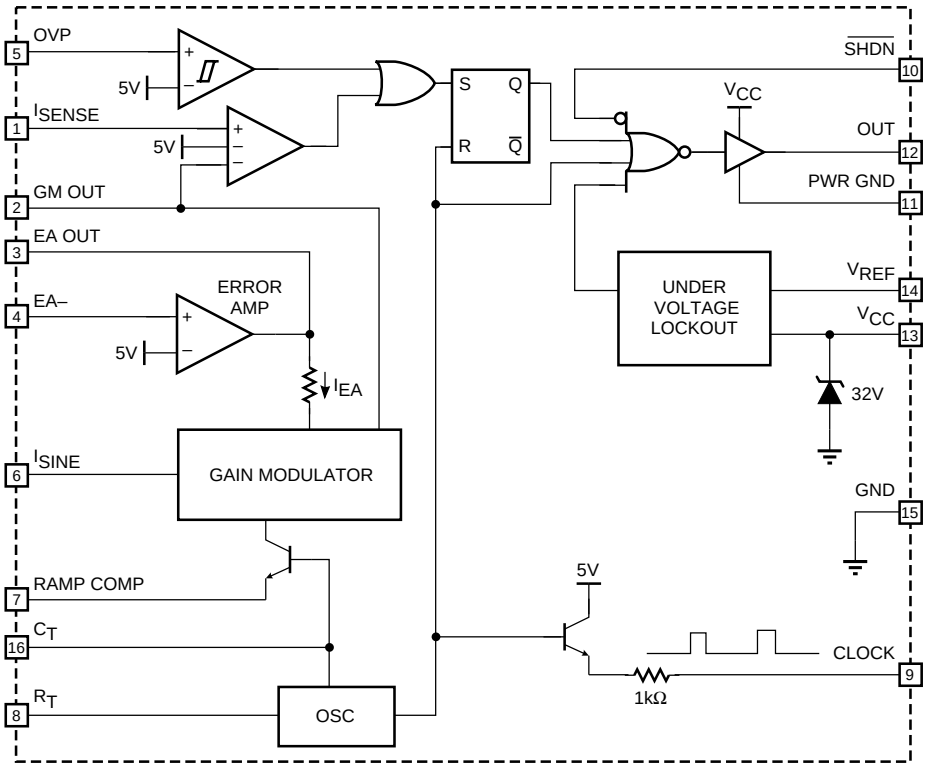
- Precision buffered 5V reference (±0.5%)
- Current-input gain modulator reduces external components and improves noise immunity
- Programmable ramp compensation circuit
- 1A peak current totem-pole output drive
- Overvoltage comparator helps prevent output voltage "runaway"
- Wide common mode range in current sense comparators for better noise immunity
- Large oscillator amplitude for better noise immunity

Description

The ML4812 is designed to optimally facilitate a peak current control boost type power factor correction system. Special care has been taken in the design of the ML4812 to increase system noise immunity. The circuit includes a precision reference, gain modulator, error amplifier, over-voltage protection, ramp compensation, as well as a high current output. In addition, start-up is simplified by an under-voltage lockout circuit with 6V hysteresis.

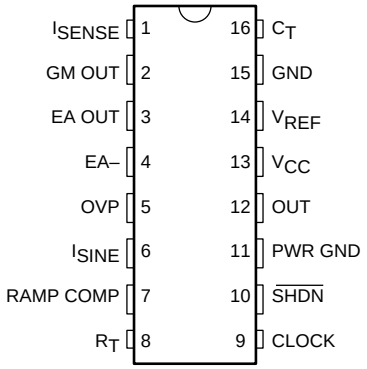
In a typical application, the ML4812 functions as a current mode regulator. The current which is necessary to terminate the cycle is a product of the sinusoidal line voltage times the output of the error amplifier which is regulating the output DC voltage. Ramp compensation is programmable with an external resistor, to provide stable operation when the duty cycle exceeds 50%.

Block Diagram (Pin Configuration Shown is for DIP Version)



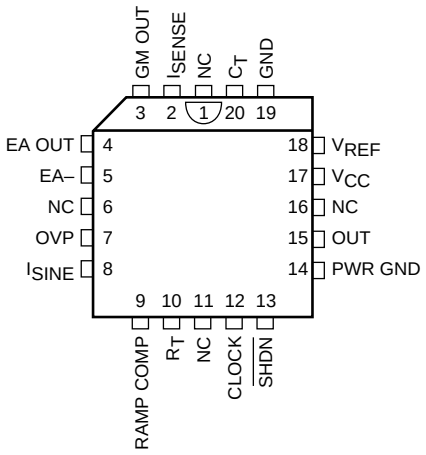
Pin Configuration

ML4812
16-Pin PDIP (P16)



Top View

ML4812
20-Pin PLCC (Q20)



Top View

Pin Description

Number	Name	Function
1	I_{SENSE}	Input from the current sense transformer to the non-inverting input of the PWM comparator.
2	GM OUT	Output of gain modulator. A resistor to ground on this pin converts the current to a voltage. This pin is clamped to 5V and tied to the inverting input of the PWM comparator.
3	EA OUT	Output of error amplifier.
4	EA–	Inverting input to error amplifier.
5	OVP	Input to over voltage comparator.
6	I_{SINE}	Current gain modulator input.
7	RAMP COMP	Buffered output from the oscillator ramp (C_T). A resistor to ground sets the current which is internally subtracted from the product of I_{SINE} and I_{EA} in the gain modulator.
8	R_T	Oscillator timing resistor pin. A 5V source sets a current in the external resistor which is mirrored to charge C_T.
9	CLOCK	Digital clock output.
10	$\overline{SHDN}$	A TTL compatible low level on this pin turns off the output.
11	PWR GND	Return for the high current totem pole output.
12	OUT	High current totem pole output.
13	V_{CC}	Positive Supply for the IC.
14	V_{REF}	Buffered output for the 5V voltage reference.
15	GND	Analog signal ground.
16	C_T	Timing capacitor for the oscillator.

Absolute Maximum Ratings[1]

Supply Current (I_{CC})	30mA
Output Current Source or Sink (OUT) DC	1.0A
Output Energy (capacitive load per cycle)	5µJ
Gain Modulator I_{SINE} Input (I_{SINE})	1.2mA
Error Amp Sink Current (EA OUT)	10mA
Oscillator Charge Current	2mA
Analog Inputs (I_{SENSE}, EA–, OVP)	–0.3V to 5.5V
Junction Temperature	150°C
Storage Temperature Range	–65°C to 150°C
Lead Temperature (soldering 10 sec.)	260°C
Thermal Resistance (θ_{JA}) 20-Pin PLCC 16-Pin PDIP	 60°C/W 65°C/W

Note:
1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Operating Conditions

Temperature Range ML4812CX	 0°C to 70°C

Electrical Characteristics

Unless otherwise specified, V_{CC} = 15V , R_T = 14kΩ, C_T = 1000pF, T_A = Operating Temperature Range (Notes 1, 2).

Parameter	Conditions	Min.	Typ.	Max.	Units
Oscillator					
Initial Accuracy	T_J = 25°C	91	98	105	kHz
Voltage Stability	12V < V_{CC} < 18V		0.3		%
Temperature Stability			2		%
Total Variation	Line, temperature	90		108	kHz
Ramp Valley to Peak			3.3		V
R_T Voltage		4.8	5.0	5.2	V
Discharge Current (R_T open)	T_J = 25°C, V_{CT} = 2V	7.8	8.4	9.0	mA
	V_{CT} = 2V	7.3	8.4	9.3	mA
Clock Out Voltage Low	RL = 16kΩ		0.2	0.5	V
Clock Out Voltage High	RL = 16kΩ	3.0	3.5		V
Reference					
Output Voltage	T_J = 25°C, I_O = 1mA	4.95	5.00	5.05	V
Line Regulation	12V < V_{CC} < 25V		2	20	mV
Load Regulation	1mA < IO < 20mA		2	20	mV
Temperature Stability			0.4		%
Total Variation	Line, load, temp.	4.9		5.1	V
Output Noise Voltage	10Hz to 10kHz		50		µV
Long Term Stability	T_J = 125°C, 1000 hours		5	25	mV
Short Circuit Current	V_{REF} = 0V	–30	–85	–180	mA
Error Amplifier					
Input Offset Voltage				±15	mV
Input Bias Current			–0.1	–1.0	µA
Open Loop Gain	1 < $V_{EA\ OUT}$ < 5V	60	75		dB
PSRR	12V < V_{CC} < 25V	60	75		dB
Output Sink Current	$V_{EA\ OUT}$ = 1.1V, V_{EA-} = 6.2V	2	12		mA
Output Source Current	$V_{EA\ OUT}$ = 5.0V, V_{EA-} = 4.8V	–0.5	–1.0		mA
Output High Voltage	$I_{EA\ OUT}$ = –0.5mA, V_{EA-} = 4.8V	5.3	5.5		V
Output Low Voltage	$I_{EA\ OUT}$ = 1mA, V_{EA-} = 6.2V		0.5	1.0	V
Unity Gain Bandwidth			1.0		MHz
Gain Modulator					
I_{SINE} Input Voltage	I_{SINE} = 500µA	0.4	0.7	0.9	V
Output Current (GM OUT)	I_{SINE} = 500µA, EA– = V_{REF} – 20mV	430	470	510	µA
	I_{SINE} = 500µA, EA– = V_{REF} + 20mV		3	10	µA
	I_{SINE} = 1mA, EA– = V_{REF} – 20mV	860	940	1020	µA
	I_{SINE} = 500µA, EA– = V_{REF} – 20mV, $I_{RAMP\ COMP}$ = 50µA		455		µA
Bandwidth			200		kHz
PSRR	12V < V_{CC} < 25V		70		dB

Electrical Characteristics (Continued)

Unless otherwise specified, V_{CC} = 15V , R_T = 14kΩ, C_T = 1000pF, T_A = Operating Temperature Range (Notes 1, 2).

Parameter	Conditions	Min.	Typ.	Max.	Units
OVP Comparator					
Input Offset Voltage	Output Off	–25		+5	mV
Hysteresis	Output On	95	105	115	mV
Input Bias Current			–0.3	–3	µA
Propagation Delay			150		ns
PWM Comparator: I_{SENSE}					
Input Offset Voltage				±15	mV
Input Offset Current				±1	µA
Input Common Mode Range		–0.2		5.5	V
Input Bias Current			–2	–10	µA
Propagation Delay			150		ns
I_{LIMIT} Trip Point	$V_{GM\ OUT}$ = 5.5V	4.8	5	5.2	V
Output					
Output Voltage Low	I_{OUT} = –20mA		0.1	0.4	V
	I_{OUT} = –200mA		1.6	2.2	V
Output Voltage High	I_{OUT} = 20mA	13	13.5		V
	I_{OUT} = 200mA	12	13.4		V
Output Voltage Low in UVLO	I_{OUT} = –5mA, V_{CC} = 8V		0.1	0.8	V
Output Rise/Fall Time	C_L = 1000pF		50		ns
Shutdown	V_{IH}	2.0			V
	V_{IL}			0.8	V
	I_{IL}, $V_{\overline{SHDN}}$ = 0V			–1.5	mA
	IIH, $V_{\overline{SHDN}}$ = 5V			10	µA
Under-Voltage Lockout					
Startup Threshold		15	16	17	V
Shutdown Threshold		9	10	11	V
V_{REF} Good Threshold			4.4		V
Supply					
Supply Current	Start-Up, V_{CC} = 14V, T_J = 25°C		0.8	1.2	mA
	Operating, T_J = 25°C		20	25	mA
Internal Shunt Zener Voltage	I_{CC} = 30mA	25	30	34	V

Notes:

1. Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.
2. V_{CC} is raised above the Startup Threshold first to activate the IC, then returned to 15V.

Functional Description

Oscillator

The ML4812 oscillator charges the external capacitor (C_T) with a current (I_{SET}) equal to $5/R_{SET}$. When the capacitor voltage reaches the upper threshold, the comparator changes state and the capacitor discharges to the lower threshold through Q1. While the capacitor is discharging, Q2 provides a high pulse.

The Oscillator period can be described by the following relationship:

$$T_{OSC} = T_{RAMP} + T_{DEADTIME}$$

where:

$$V_{OUT} = \frac{V_{IN}}{1 - D_{ON}}$$

and:

$$T_{DEADTIME} = \frac{C_T \times V_{RAMPVALLEYTOPEAK}}{8.4mA - I_{SET}}$$

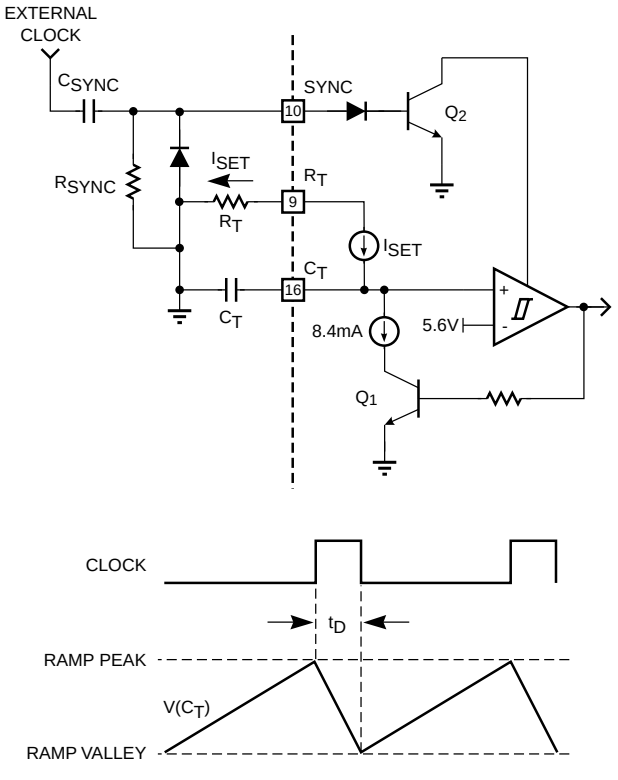


Figure 1. Oscillator Block Diagram

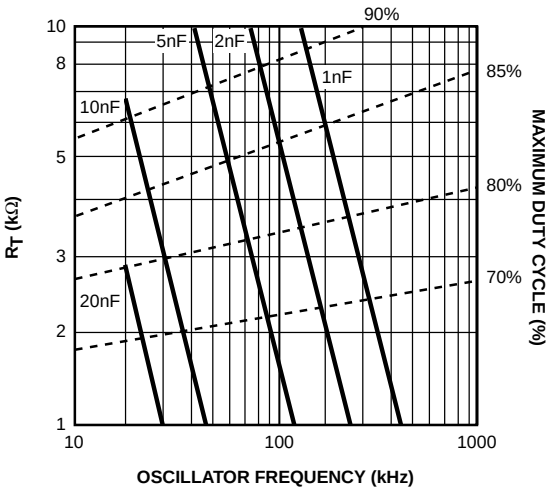


Figure 2. Oscillator Timing Resistance vs. Frequency

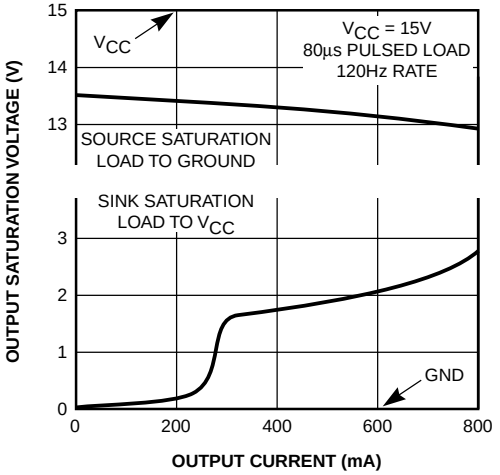


Figure 3. Output Saturation Voltage vs. Output Current

Output Driver Stage

The ML4812 output driver is a 1A peak output high speed totem pole circuit designed to quickly drive capacitive loads, such as power MOSFET gates. (Figure 3)

Error Amplifier

The ML4812 error amplifier is a high open loop gain, wide bandwidth, amplifier.(Figures 4-5)

Gain Modulator

The ML4812 gain modulator is of the current-input type to provide high immunity to the disturbances caused by high power switching. The rectified line input sine wave is converted to a current via a dropping resistor. In this way, small amounts of ground noise produce an insignificant effect on the reference to the PWM comparator. The output of the gain modulator is a current of the form: I_{OUT} is proportional to $I_{SINE} \leftrightarrow I_{EA}$, where I_{SINE} is the current in the dropping resistor, and I_{EA} is a current proportional to the output of the error amplifier. When the error amplifier is saturated high, the output of the gain modulator is approximately equal to the I_{SINE} input current. The gain modulator output current is converted into the reference voltage for the PWM comparator through a resistor to ground on the gain modulator output. The gain modulator output is clamped to 5V to provide current limiting.

Ramp compensation is accomplished by subtracting 1/2 of the current flowing out of RAMP COMP through a buffer transistor driven by C_T which is set by an external resistor.

Under Voltage Lockout

On power-up the ML4812 remains in the UVLO condition; output low and quiescent current low. The IC becomes operational when V_{CC} reaches 16V. When V_{CC} drops below 10V, the UVLO condition is imposed. During the UVLO condition, the 5V VREF pin is "off", making it usable as a "flag" for starting up a downstream PWM converter.

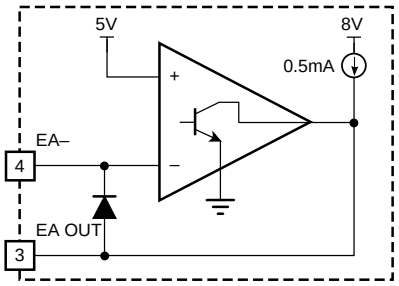


Figure 4. Error Amplifier Configuration

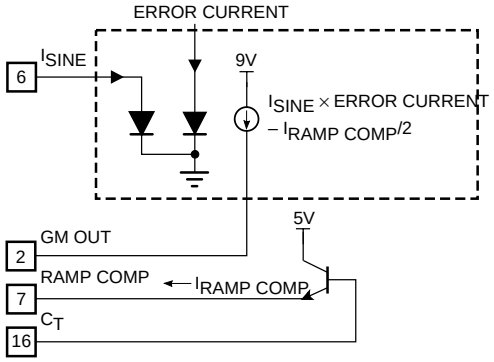


Figure 6. Gain Modulator Block Diagram

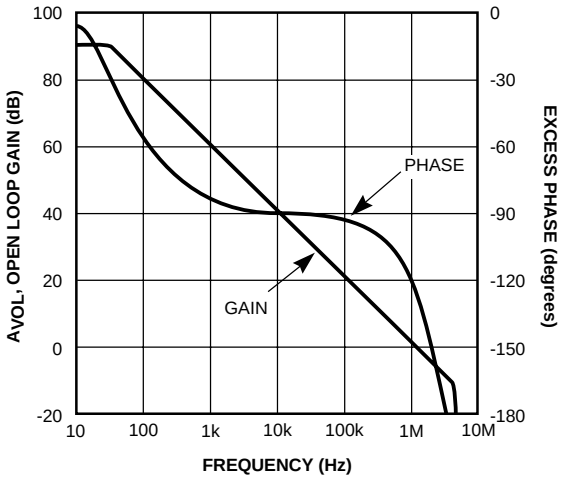


Figure 5. Error Amplifier Open-Loop Gain and Phase vs Frequency

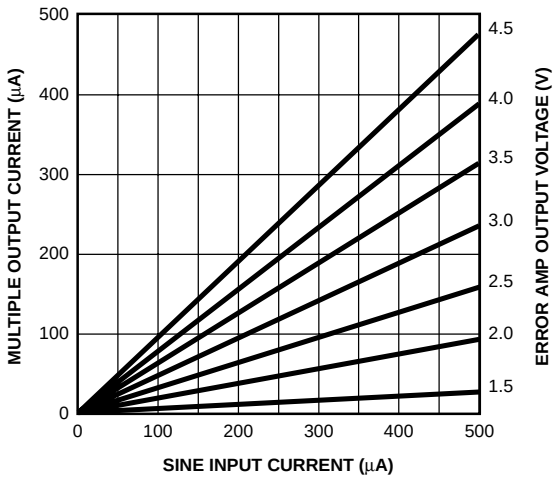


Figure 7. Gain Modulator Linearity

Typical Applications

Input Inductor (L1) Selection

The central component in the regulator is the input boost inductor. The value of this inductor controls various critical operational aspects of the regulator. If the value is too low, the input current distortion will be high and will result in low power factor and increased noise at the input. This will require more input filtering. In addition, when the value of the inductor is low the inductor dries out (runs out of current) at low currents. Thus the power factor will decrease at lower power levels and/or higher line voltages. If the inductor value is too high, then for a given operating current the required size of the inductor core will be large and/or the required number of turns will be high. So a balance must be reached between distortion and core size.

One more condition where the inductor can dry out is analyzed below where it is shown to be maximum duty cycle dependent.

For the boost converter at steady state:

$$V_{OUT} = \frac{V_{IN}}{1 - D_{ON}} \quad (1)$$

Where D_{ON} is the duty cycle [$T_{ON}/(T_{ON} + T_{OFF})$]. The input boost inductor will dry out when the following condition is satisfied:

$$V_{IN}(t) < V_{OUT} \times (1 - D_{ON}) \quad (2)$$

or

$$V_{INDRY} = [1 - D_{ON}(max)] \times V_{OUT} \quad (3)$$

V_{INDRY}: voltage where the inductor dries out.
V_{OUT}: output DC voltage.

Effectively, the above relationship shows that the resetting volt-seconds are more than setting volt-seconds. In energy transfer terms this means that less energy is stored in the inductor during the ON time than it is asked to deliver during the OFF time. The net result is that the inductor dries out.

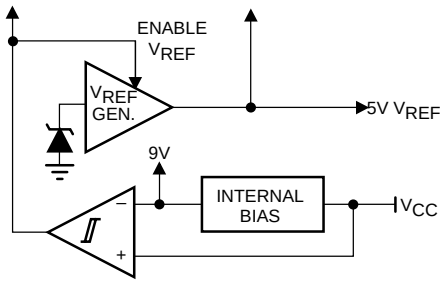


Figure 8. Under-Voltage Lockout Block Diagram

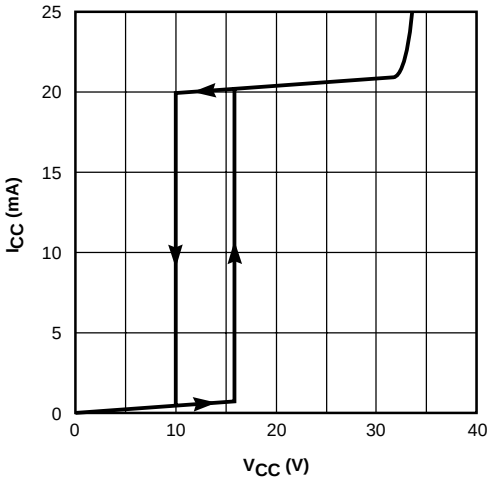


Figure 9a. Total Supply Current vs. Supply Voltage

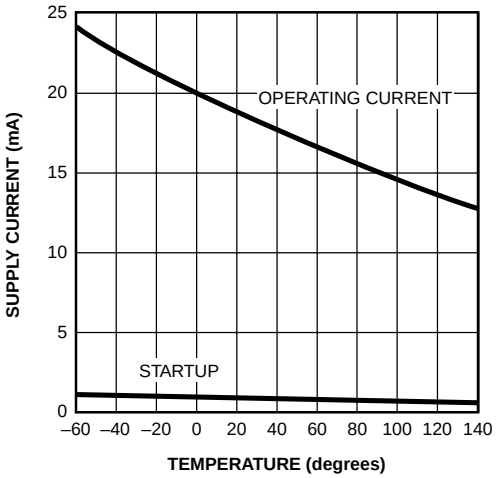


Figure 9b. Supply Current (I_{CC}) vs. Temperature

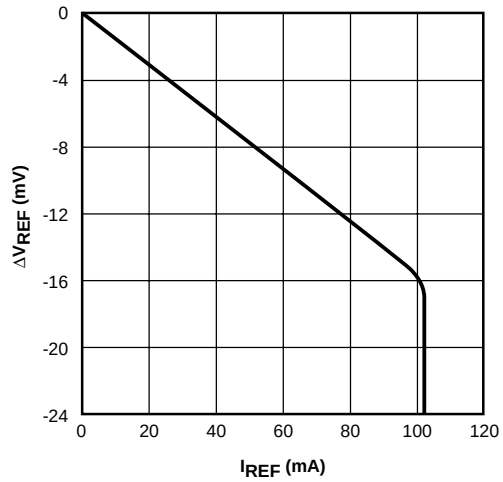


Figure 10. Reference Load Regulation

The recommended maximum duty cycle is 95% at 100KHz to allow time for the input inductor to dump its energy to the output capacitors. For example, if: V_{OUT} = 380V and D_{ON} (max) = 0.95, then substituting in (3) yields V_{INDRY} = 20V. The effect of drying out is an increase in distortion at low voltages.

For a given output power, the instantaneous value of the input current is a function of the input sinusoidal voltage waveform, i.e. as the input voltage sweeps from zero volts to a maximum value equal to its peak so does the current.

The load of the power factor regulator is usually a switching power supply which is essentially a constant power load. As a result, an increase in the input voltage will be offset by a decrease in the input current.

By combining the ideas set forth above, some ground rules can be obtained for the selection and design of the input inductor:

Step 1: Find minimum operating current.

$$I_{IN}(min)_{PEAK} = \frac{1.414 \times P_{IN}(min)}{V_{IN}(max)} \quad (4)$$

$$V_{IN}(max) = 260V$$

$$P_{IN}(min) = 50W$$

then:

$$I_{IN}(min)_{PEAK} = 0.272A$$

Step 2: Choose a minimum current at which point the inductor current will be on the verge of drying out. For this example 40% of the peak current found in step 1 was chosen.

then:

$$I_{LDRY} = 100mA$$

Step 3: The value of the inductance can now be found using previously calculated data.

$$L1 = \frac{V_{INDRY} \times D_{ON}(max)}{I_{LDRY} \times f_{OSC}} = \frac{20V \times 0.95}{100mA \times 100KHz} = 2mH \quad (5)$$

The inductor can be allowed to decrease in value when the current sweeps from minimum to maximum value. This allows the use of smaller core sizes. The only requirement is that the ramp compensation must be adequate for the lower inductance value of the core so that there is adequate compensation at high current.

Step 4: The presence of the ramp compensation will change the dry out point, but the value found above can be considered a good starting point. Based on the amount of power factor correction the above value of L1 can be optimized after a few iterations.

Gapped Ferrites, Molypermalloy, and Powdered Iron cores are typical choices for core material. The core material selected should have a high saturation point and acceptable losses at the operating frequency.

One ferrite core that is suitable at around 200W is the #4119PL00-3C8 made by Philips Components (Ferroxcube). This ungapped core will require a total gap of 0.180" for this application.

Oscillator Component Selection

The oscillator timing components can be calculated by using the following expression:

$$f_{OSC} = \frac{1.36}{R_T \times C_T} \quad (6)$$

For example:

Step 1: At 100kHz with 95% duty cycle T_{OFF} = 500ns calculate C_T using the following formula:

$$C_T = \frac{T_{OFF} \times I_{DIS}}{V_{OSC}} = 1000pF \quad (7)$$

Step 2: Calculate the required value of the timing resistor.

$$R_T = \frac{1.36}{f_{OSC} \times C_T} = \frac{1.36}{100KHz \times 100pF} = 13.6k\Omega \quad (8)$$

choose $R_T = 14k\Omega$

Current Sense and Slope (Ramp) Compensation Component Selection

Slope compensation in the ML4812 is provided internally. Rather than adding slope to the noninverting input of the PWM comparator, it is actually subtracted from the voltage present at the inverting input of the PWM comparator. The amount of slope compensation should be at least 50% of the downslope of the inductor current during the off time, as reflected to the inverting input of the PWM comparator. Note that slope compensation is required only when the inductor current is continuous and the duty cycle is more than 50%. The downslope of the inductor current at the verge of discontinuity can be found using the expression given below:

$$\frac{di_L}{dt} = \frac{V_{OUT} - V_{INDRY}}{L} = \frac{380V - 20V}{2mH} = 0.18A/\mu s \quad (9)$$

The downslope as reflected to the input of the PWM comparator is given by:

$$S_{PWM} = \frac{V_{OUT} - V_{INDRY}}{L} = \frac{R_S}{N_C} \quad (10)$$

$$S_{PWM} = \frac{380V - 20V}{2mH} \times \frac{100}{80} = 0.225V/\mu s$$

Where R_S is the current sense resistor and N_C is the turns ratio of the current transformer (T1) used. In general, current transformers simplify the sensing of switch currents (especially at high power levels where the use of sense resistors is complicated by the amount of power they have to dissipate). Normally the primary side of the transformer consists of a single turn and the secondary consists of several turns of either enameled magnet wire or insulated wire. The diameter of the ferrite core used in this example is 0.5" (SPANG/Magnetics F41206-TC). The rectifying diode at the output of the current transformer can be a 1N4148 for secondary currents up to 75mA average.

Sense FETs or resistive sensing can also be used to sense the switch current. The sensed signal has to be amplified to the proper level before it is applied to the ML4812.

The value of the ramp compensation (SC_{PWM}) as seen at the inverting terminal of the PWM comparator is:

$$SC_{PWM} = \frac{2.5 \times R_M}{R_T \times C_T \times R_{SC}} \quad (11)$$

The required value for R_{SC} can therefore be found by equating: $SC_{PWM} = A_{SC} \times S_{PWM}$, where A_{SC} is the amount of slope compensation and solving for R_{SC}. The value of GM OUT depends on the selection of RAMP COMP.

$$R_P = \frac{V_{IN}(max)_{PEAK}}{I_{SINE(PEAK)}} = \frac{260 \times 1.414}{0.5mA} = 750k\Omega \quad (12)$$

$$R_M = \frac{V_{CLAMP} \times R_P}{V_{IN(PEAK)}} = \frac{4.9 \times 750k\Omega}{90 \times 1.414} = 28.8k\Omega \quad (13)$$

The peak of the inductor current can be found approximately by:

$$I_{LPEAK} = \frac{1.414 \times P_{POUT}}{V_{IN(RMS)}} = \frac{1.414 \times 200}{90} = 3.14A \quad (14)$$

Selection of N_C which depends on the maximum switch current, assume 4A for this example is 80 turns.

$$R_S = \frac{V_{CLAMP} \times N_C}{I_{LPEAK}} = \frac{4.9 \times 80}{4} = 100\Omega \quad (15)$$

Where R_S is the sense resistor, and V_{CLAMP} is the current clamp at the inverting input of the PWM comparator. This clamp is internally set to 5V. In actual application it is a good idea to assume a value less than 5V to avoid unwanted current limiting action due to component tolerances. In this application, V_{CLAMP} was chosen as 4.9V.

Having calculated RS, the value S_{PWM} and of R_{SC} can now be calculated:

$$R_{SC} = \frac{2.5 \times R_M}{A_{SC} \times S_{PWM} \times R_T \times C_T} \quad (16)$$

$$R_{SC} = \frac{2.5 \times 28.8k\Omega}{0.7 \times (0.225 \times 10^6) \times 14K \times 1nF} = 33k\Omega$$

The following values were used in the calculation:

$R_M = 28.8k\Omega$ $A_{SC} = 0.7$
$R_T = 14k\Omega$ $C_T = 1nF$

Voltage Regulation Components

The values of the voltage regulation loop components are calculated based on the operating output voltage. Note that voltage safety regulations require the use of sense resistors that have adequate voltage rating. As a rule of thumb if 1/4W resistors are chosen, two of them should be used in series. The input bias current of the error amplifier is approximately 0.5µA, therefore the current available from the voltage sense resistors should be significantly higher than this value. Since two 1/4W resistors have to be used the total power rating is 1/2W. The operating power is set to be 0.4W then with 380V output voltage the value can be calculated as follows:

$$R_1 = (380V)^2 / 0.4W = 360k\Omega \quad (17)$$

Choose two 178kΩ, 1% connected in series. Then R2 can be calculated using the formula below:

$$R_2 = \frac{V_{REF} \times R_1}{V_{OUT} - V_{REF}} = \frac{5V \times 356k\Omega}{380V - 5V} = 4.747k\Omega \quad (18)$$

Choose 4.75kΩ, 1%. One more critical component in the voltage regulation loop is the feedback capacitor for the error amplifier. The voltage loop bandwidth should be set such that it rejects the 120Hz ripple which is present at the output. If this ripple is not adequately attenuated it will cause distortion on the input current waveform. Typical bandwidths range anywhere from a few Hertz to 15Hz. The main compromise is between transient response and distortion. The feedback capacitor can be calculated using the following formula:

$$C_F = \frac{1}{3.142 \times R_1 \times BW} \quad (19)$$

$$C_F = \frac{1}{3.142 \times 356k\Omega \times 2Hz} = 0.44\mu F$$

Overvoltage Protection (OVP) Components

The OVP loop should be set so that there is no interaction with the voltage control loop. Typically it should be set to a level where the power components are safe to operate. Ten to fifteen volts above V_{OUT} is generally a good setpoint. This sets the maximum transient output voltage to about 395V. By choosing the high voltage side resistor of the OVP circuit the same way as above i.e. R_4 = 356K then R_5 can be calculated as:

$$R_5 = \frac{V_{REF} \times R_4}{V_{OVP} - V_{REF}} = \frac{5V \times 356k\Omega}{395V - 5V} = 4.564k\Omega \qquad (20)$$

Choose 4.53kΩ, 1%. Note that R_1, R_2, R_4 and R_5 should be tight tolerance resistors such as 1% or better.

Controller Shutdown

The ML4812 provides a shutdown pin which could be used to shutdown the IC. Care should be taken when this pin is used because power supply sequencing problems could arise if another regulator with its own bootstrapping follows the ML4812. In such a case a special circuit should be used to allow for orderly start up. One way to accomplish this is by using the reference voltage of the ML4812 to inhibit the other controller IC or to shut down its bias supply current.

Off-line Start-up and Bias Supply Generation

The ML4812 can be started using a “bleed resistor” from the high voltage bus. After the voltage on V_{CC} exceeds 16V, the IC starts up. The energy stored on the 330µF, C15, capacitor supplies the IC with running power until the supplemental winding on L1 can provide the power to sustain operation.

The values of the start-up resistor R10 and capacitor C15 may need to be optimized depending on the application. The charging waveform for the secondary winding of L1 is an inverted chopped sinusoid which reaches its peak when the line voltage is at its minimum. In this example, C9 = 0.1µF, C15 = 330µF, D8 = 1N4148, R10 = 39kΩ, 2W.

Enhancement Circuit

The power factor enhancement circuit shown in Figure 12 is described in detail in Application Note 11. It improves the power factor and lowers the input current harmonics. Note that the circuit meets IEC 1000-3-2 specifications (with the enhancement) on the harmonics by a large margin while correcting the input power factor to better than 0.99 under most steady state operating conditions.

Construction and Layout Tips

High frequency power circuits require special care during breadboard construction and layout. Double sided printed circuit boards with ground plane on one side are highly recommended. All critical switching leads (power FET, output diode, IC output and ground leads, bypass capacitors) should be kept as small as possible. This is to minimize both the transmission and pick-up of switching noise.

There are two kinds of noise coupling; inductive and capacitive. As the name implies inductive coupling is due to fast changing (high di/dt) circulating switching currents. The main source is the loop formed by Q1, D5, and C3–C4. Therefore this loop should be as small as possible, and the above capacitors should be good high frequency types.

The second form of noise coupling is due to fast changing voltages (high dv/dt). The main source in this case is the drain of the power FET. The radiated noise in this case can be minimized by insulating the drain of the FET from the heatsink and then tying the heatsink to the source of the FET with a high frequency capacitor (C_H in Figure 12).

The IC has two ground pins named PWR GND and Signal GND. These two pins should be connected together with a very short lead at the printed circuit board exit point. In general grounding is very important and ground loops should be avoided. Star grounding or ground plane techniques are preferred.

Magnetics Tips

L1 — Main Inductor

As shown in Table 1, one of several toroidal cores can be used for L1. The T184-40 core above is the most economical, but has lower inductance at high current. This would yield higher ripple current and require more line EMI filtering. The value for R_{SC} (slope compensation resistor on RAMP COMP) was calculated for the T225-8/90 and should be recalculated for other inductor characteristics. The various core manufacturers have a range of applications literature available. A gapped ferrite core can also be used in place of the powdered iron core. One such core is a Philips Components (Ferroxcube) core #4229PL00-3C8. This is an ungapped core. Using 145 turns of #24 AWG wire, a total air gap of 0.180" is required to give a total inductance of about 2mH. Since 1/2 of the gap will be on the outside of the core and 1/2 the gap on the inside, putting a 0.09" spacer in the center will yield a 0.180" total gap. To prevent leakage fields

Table 1. Toroidal Cores (L1)

Material	Manufacturer	Part #	Turns (#24AWG)
Powdered Iron	Micrometals	T225-8/90	200
Powdered Iron	Micrometals	T184-40	120
Molypermalloy	SPANG (Mag. Inc.)	58076-A2 (high flux)	180

from generating RFI, a shorted turn of copper tape should be wrapped around the gap as shown in Figure 11. For production, a gapped center leg can be ordered from most core vendors, eliminating the need for the external shorted copper turn when using a potentiometer core.

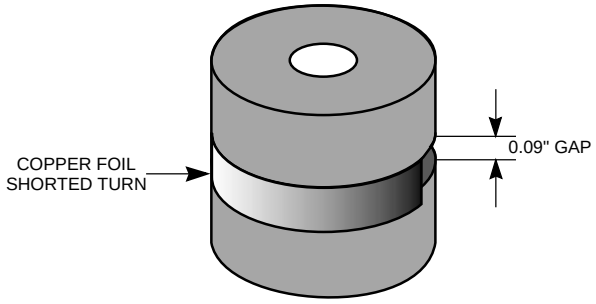


Figure 11. Copper Foil Shorted Turn

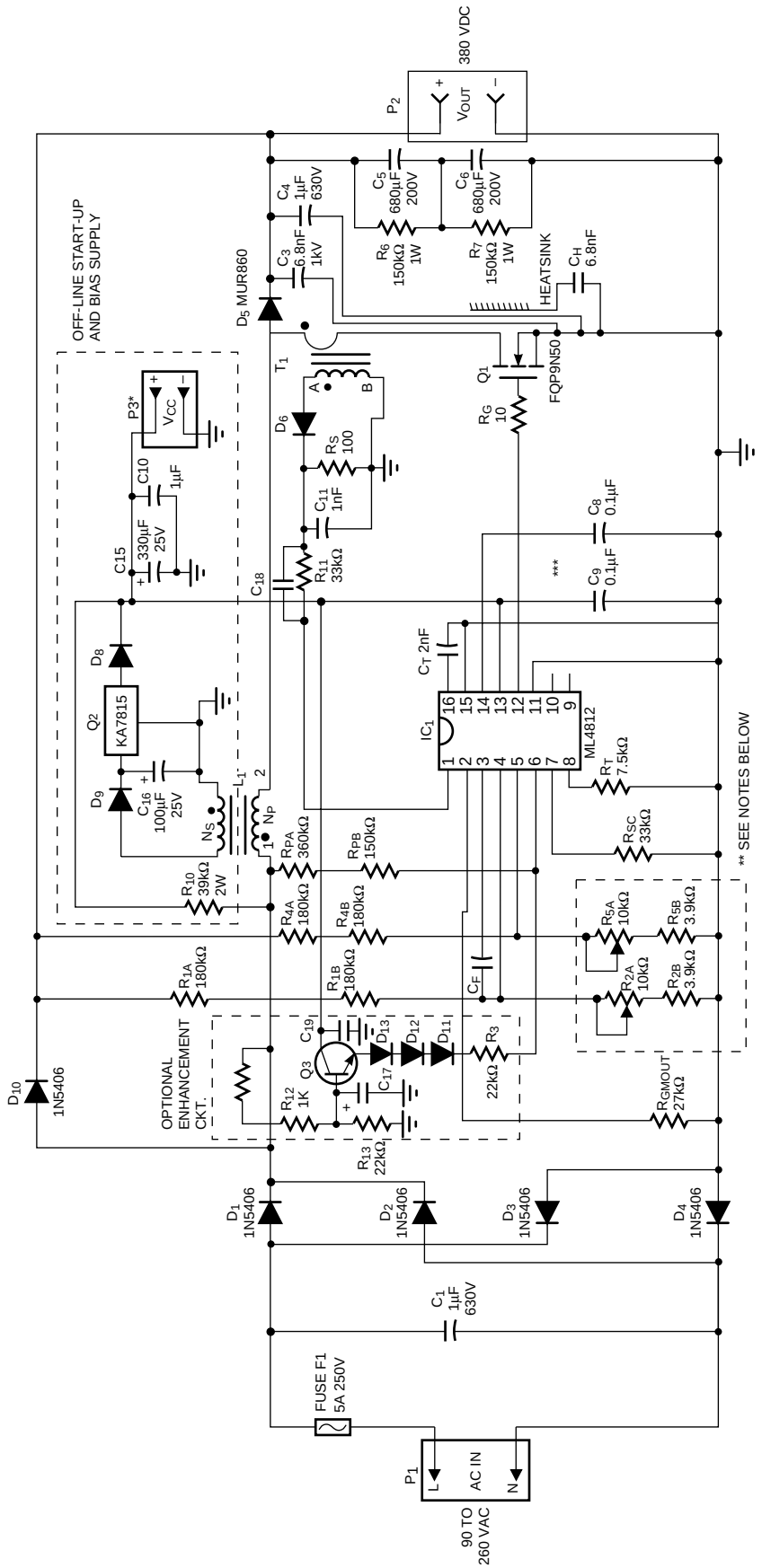
T1 — Sense Transformer

In addition to the core type mentioned in the parts list, the following Siemens cores should be suitable for substitution and may be more readily available in Europe.

Material	Size Code	Part #
N27	R16/6.3	B64290-K45-X27
N30	R16/6.3	B64290-K45-X830

The N27 material is for high frequency and will work better above 100KHz but both are adequate. In addition, Philips Components (Ferroxcube) core 768T188-3C8 can be used. Please also refer to the list of core vendors below

SPANG/Magnetics Inc.	1 (800) 245-3984, or (412) 282-8282
Micrometals	1 (800) 356-5977
Philips Components	(914) 247-2064



* P3 IS USED AT INITAL TURN-ON TO CHECK THE IC FOR PROPER OPERATION. APPLY ≈ 16VDC.

** FIXED RESISTORS CAN BE USED FOR THE SENSING COMPONENTS. BELOW ARE 1% STANDARD RESISTORS THAT WILL FORCE THE CORRECT OUTPUT VOLTAGES R1A, R1B, R4A, R4B = 178kΩ 1%, R2B = 4.75 1%, R5B = 4.53kΩ 1%. USE JUMPERS INSTEAD OF R2A AND R5A (POTS).

*** FOR HIGHER POWER USE MORE V_{CC} DECOUPLING. 2µF OR MORE BE REQUIRED AT 1KW LEVELS.

NOTES:
1. ALL UNSPECIFIED DIODES ARE 1N4148.
2. ALL UNSPECIFIED RESISTORS ARE 1/4 WATT.
3. ALL UNSPECIFIED CAPACITOR VOLTAGE RATINGS ARE 50V.
4. ADJUST R_{2A} AND R_{5A} WITH CAUTION TO AVOID OVER VOLTAGE CONDITIONS.

Q_3 = PN2222

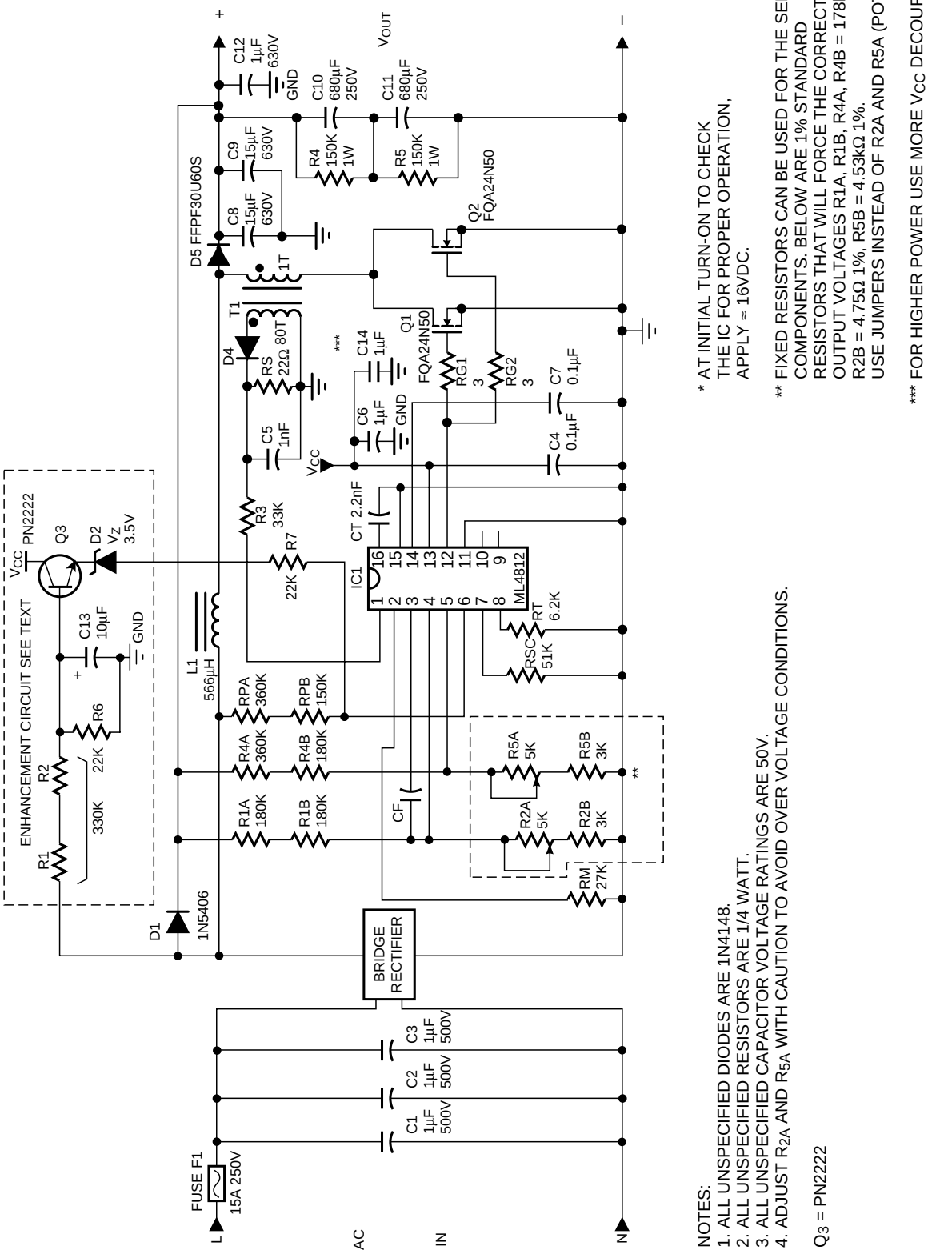
Figure 12. Typical Application 200W Power Factor Correction Circuit

Table 2. Component Values/Bill of Materials for Figure 12

Reference	Description
C1, C4	1µF, 630V Film (250VAC)
C3, C_H	6.8nF, 1KV Ceramic disk
C5, C6	680µF, 200V Electrolytic
C8, C9	0.1µF, 50V Ceramic
C10, C19	1µF, 50V Ceramic
C11	0.001µF, 50V Ceramic
C15	330µF, 25V Electrolytic
C16	100µF, 25V Electrolytic
C17	10µF, 25V Electrolytic
C_F	0.47µF, 50V Ceramic
C_T	0.002µF, 50V Ceramic
D1, D2, D3, D4, D10	1N5406 (Fairchild)
D5	MUR860 (Fairchild)
D6, D8, D9, D11, D12, D13	1N4148 (Fairchild)
F1	5A, 250V 3AG with clips
IC1	ML4812CP (Fairchild)
L1	2mH, 4A I_{PEAK} (see note)
Q1	FQP9N50 (Fairchild)
Q2	KA7815 (Fairchild)
Q3	PN2222 (Fairchild)
R1A, R1B, R4A, R4B	180kΩ
R2A, R5A	10kΩ TRIMPOT BOURNS 3299 or equivalent
R2B, R5B	3.9kΩ
R3, R13	22kΩ
R6, R7, RPB	150kΩ
R10	39kΩ, 2W
R11	33kΩ
R12	1kΩ
RG	10Ω
RM	27kΩ
RPA, R15	360kΩ
RS	100kΩ
RSC	33kΩ
RT	7.5kΩ
T1	SPANG F41206-TC N_S = 80, N_P = 1 (see note)

Note:

1. All resistors 1/4W unless otherwise specified. Some reference designators are skipped (e.g. C2, C12, etc.) and do not appear on the schematic. These designators were used in previous revisions of the board and are not used on this revision. Additional information on key components is included in the attached appendix.



NOTES:
1. ALL UNSPECIFIED DIODES ARE 1N4148.
2. ALL UNSPECIFIED RESISTORS ARE 1/4 WATT.
3. ALL UNSPECIFIED CAPACITOR VOLTAGE RATINGS ARE 50V.
4. ADJUST R_{2A} AND R_{5A} WITH CAUTION TO AVOID OVER VOLTAGE CONDITIONS.

Q_3 = PN2222

* AT INITIAL TURN-ON TO CHECK THE IC FOR PROPER OPERATION, APPLY ≈ 16VDC.

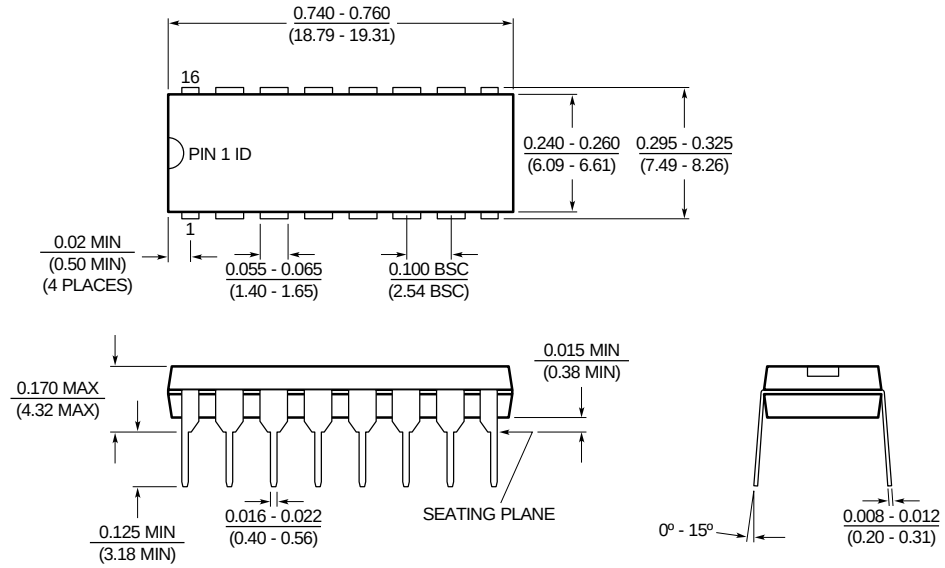
** FIXED RESISTORS CAN BE USED FOR THE SENSING COMPONENTS. BELOW ARE 1% STANDARD RESISTORS THAT WILL FORCE THE CORRECT OUTPUT VOLTAGES R1A, R1B, R4A, R4B = 178kΩ 1%, R2B = 4.75Ω 1%, R5B = 4.53kΩ 1%. USE JUMPERS INSTEAD OF R2A AND R5A (POTS).

*** FOR HIGHER POWER USE MORE V_{CC} DECOUPLING.

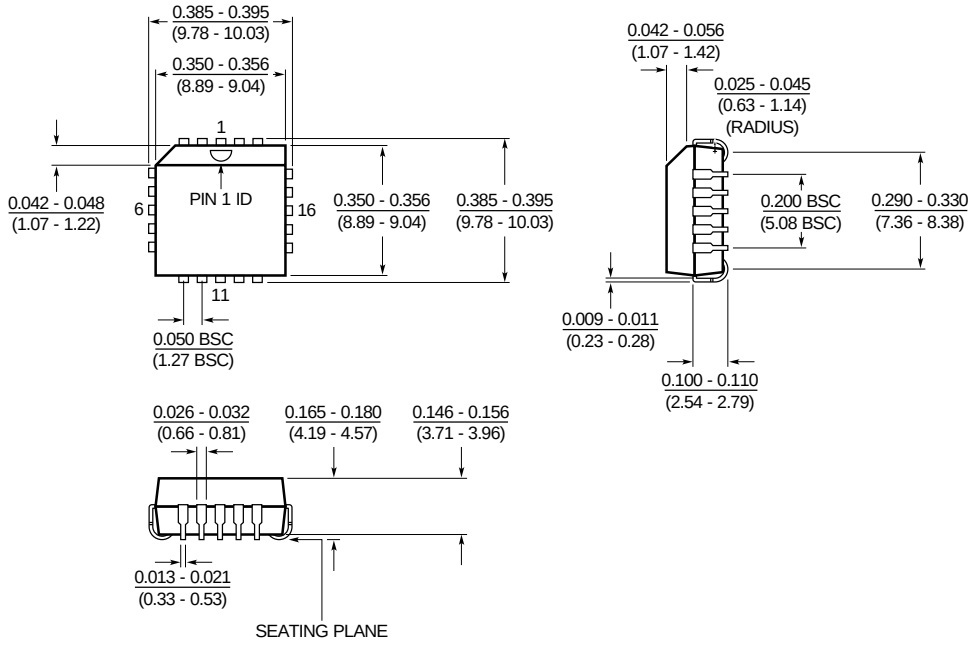
Figure 13. 1kW Input Power, Power Factor Correction Circuit

Mechanical Dimensions

Package: P16
16-Pin PDIP



Package: Q20
20-Pin PLCC



Ordering Information

Part Number	Temperature Range	Package
ML4812CP	0°C to 70°C	Molded PDIP (P16)
ML4812CQ	0°C to 70°C	Molded PLCC (Q20)

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