THE DATASHEET OF

MICRF001BN

MICRF001

QwikRadio[tm] Receiver/Data Demodulator

Advance Information

General Description

The MICRF001 is a single chip OOK (ON-OFF Keyed) Receiver IC for remote wireless applications, employing Micrel's latest QwikRadio[tm] technology. This device is a true "antenna-in, data-out" monolithic device. All RF and IF tuning is accomplished automatically within the IC, which eliminates manual tuning, and reduces production costs. Receiver functions are completely integrated. The result is a highly reliable yet extremely low cost solution for high volume wireless applications. Because the MICRF001 is a true single-chip radio receiver, it is extremely easy to apply, minimizing design and production costs, and improving time to market.

The MICRF001 uses a novel architecture that allows the receiver to demodulate signals over a wide RF band, which eliminates the need for manual tuning. This also significantly relaxes the frequency accuracy and stability requirements of the Transmitter, allowing the MICRF001 to be compatible with both SAW-based and LC-based transmitters. The receiver sensitivity and selectivity are sufficient to provide low bit error rates for decode ranges over 100 meters, equaling the performance of other more expensive solutions.

All tuning and alignment are accomplished on-chip by a low-cost ceramic resonator or with an externally supplied clock reference. Initial tolerance requirements on the ceramic resonator or external clock is a modest ±0.5%. The MICRF001 performance is insensitive to data modulation duty cycle. The MICRF001 may be used with such coding schemes as Manchester or 33/66% PWM.

All post-detection (demodulator) data filtering is provided on the MICRF001, so no external filters need to be designed. Any one of four filter bandwidths may be selected externally by the user. Bandwidths range from 0.6kHz to 4.8kHz in binary steps

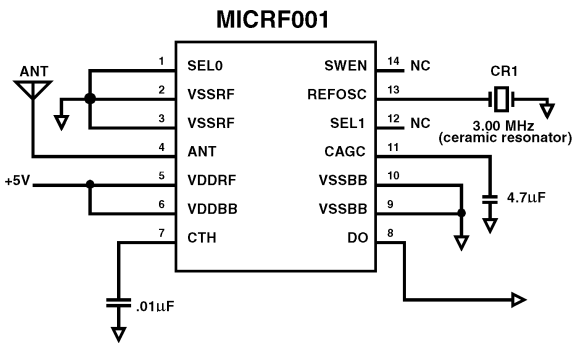
Features

- Complete UHF receiver on a monolithic chip
- Frequency range 300 to 440 MHz
- Typical range over 100 meters with monopole antenna
- Data rates to 4.8kbps
- Automatic tuning, no manual adjustment
- No Filters or Inductors required
- Very low RF re-radiation at the antenna
- Direct CMOS logic interface to standard decoder and microprocessor ICs
- Extremely low external part count

Applications

- Keyless Entry
- Security Systems
- Remote Fan/Light Control
- Garage Door Openers

Typical Operating Circuit



387 MHz, 1200 BAUD OOK RECEIVER

Ordering Information

Part Number	Temperature Range	Package
MICRF001BN	-40°C to +85°C	14-Pin DIP
MICRF001BM	-40°C to +85°C	14-Pin SOIC

Pin Configuration (DIP and SOIC)

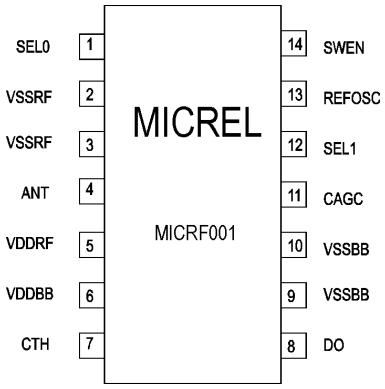


Figure 1

Pin Description

Pin Number	Pin Name	Pin Function
1	SEL0	Programs desired Demodulator Filter Bandwidth. This pin in internally pulled-up to VDD. See Table 1.
2/3	VSSRF	This pin is the ground return for the RF section of the IC. The bypass capacitor connected from VDDRF to VSSRF should have the shortest possible lead length. For best performance, connect VSSRF to VSSBB at the power supply only (i.e., keep VSSBB currents from flowing through VSSRF return path).
4	ANT	This is the receive RF input, internally ac-coupled. Connect this pin to the receive antenna. Input impedance is high (FET gate) with approximately 2pF of shunt (parasitic) capacitance. For applications located in high ambient noise environments, a fixed value band-pass network may be connected between the ANT pin and VSSRF to provide additional receive selectivity and input overload protection. (See *"Application Note 22, MICRF001 Theory of Operation"*.)
5	VDDRF	This pin is the positive supply input for the RF section of the IC. VDDBB and VDDRF should be connected directly at the IC pins. Connect a low ESL, low ESR decoupling capacitor from this pin to VSSRF, as short as possible.
6	VDDBB	This pin is the positive supply input for the baseband section of the IC. VDDBB and VDDRF should be connected directly at the IC pins.
7	CTH	This capacitor extracts the (DC) average value from the demodulated waveform, which becomes the reference for the internal data slicing comparator. Treat this as a low-pass RC filter with source impedance described in Table 1 . (See *"Application Note 22, MICRF001 Theory of Operation"*, section 6.4). A standard ± 20% X7R ceramic capacitor is generally sufficient.
8	DO	Output data pin. CMOS level compatible.
9/10	VSSBB	This is the ground return for the baseband section of the IC. The bypass and output capacitors connected to VSSBB should have the shortest possible lead lengths. For best performance, connect VSSRF to VSSBB at the power supply only (i.e., keep VSSBB currents from flowing through VSSRF return path).
11	CAGC	Integrating capacitor for on-chip receive AGC. The Decay/Attack time-constant (TC) ratio is nominally set as 10:1. CAGC = 10(Attack Time Constant) µF. A standard ± 20% X7R ceramic capacitor is generally sufficient.
12	SEL1	Programs desired Demodulator Filter Bandwidth. This pin in internally pulled-up to VDD. See Table 1.
13	REFOSC	This is the timing reference for on-chip tuning and alignment. Either connect a ceramic resonator between this pin and VSSBB, or drive the input with an AC coupled 0.5Vpp input clock. Use ceramic resonators without integral capacitors. See *"Application Note 22, MICRF001 Theory of Operation"* for details on frequency selection and accuracy.
14	SWEN	This logic pin controls the operating mode of the MICRF001. When SWEN = HIGH, the MICRF001 is in SWP mode. This is the normal (default) mode of the device. When SWEN = LOW, the device operates as a conventional single-conversion superheterodyne receiver. (See *"Application Note 22, MICRF001 Theory of Operation"* for details.) This pin is internally pulled-up to VDD.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VDDRF, VDDBB).....+7V
Voltage on any I/O Pin.....VSS-0.3 to VDD+0.3
Junction Temperature.....+150°C
Storage Temperature Range.....-65°C to + 150°C
Lead Temperature (soldering, 10 seconds).....+ 300°C

Operating Ratings

Supply Voltage (VDDRF, VDDBB).....4.75V to 5.5V
Ambient Operating Temperature (TA).....-40°C to +85°C
Package Thermal Resistance θja (14 Pin DIP).....90°C/W

This device is ESD sensitive: Meets Class 1 ESD test requirements (Human Body Model, HBM), in accordance with MIL-STD-883C, Method 3015. Do not operate or store near strong electrostatic fields. Use appropriate ESD precautions.

Electrical Characteristics

Unless otherwise stated, these specifications apply for Ta=-40°C to 85°C, 4.75<VDD<5.5V. All voltages are with respect to Ground. CAGC = CTH = .047µF, VDDRF= VDDBB = VDD. REFOSC frequency = 2.442MHz.

Parameter	Test Conditions	MIN	TYP	MAX	UNITS
Power Supply					
Operating Current	Ta= 25°C		6.3		mA
Operating Current	Reference Oscillator powered down		2		mA
RF/IF Section					
Receiver Sensitivity	Note 1, 3		-95		dBm
IF Center Frequency			2.25		MHz
IF Bandwidth	Note 3		1.0		MHz
Receive Data Rate		0.1		4.8	kbps
RF Input Range		300		440	MHz
Receive Modulation Duty-Cycle		20		80	%
Maximum Receiver Input	Rs = 50Ω		-20		dBm
Spurious Reverse Isolation	ANT pin, Rs = 50Ω Note 2		30		µVrms
AGC Attack / Decay ratio	T(Attack) / T(Decay)		0.1		
Oscillator Turn-on Time			0.1		s
Demod Section					
CTH Source Impedance	SEL0=SEL1=VDD, See Table 1		200k		Ω
CTH Source Impedance Variation		-15		+15	%
Digital Section					
REFOSC Input Impedance			200k		Ω
Input Pullup Impedance	SEL0, SEL1, SWEN		1000k		Ω
Output Current	DO pin, Push-Pull		10		µA
Output High Voltage	DO pin, Iout = 1µA	0.9VDD			V
Output Low Voltage	DO pin, Iout = 1µA			0.1VDD	V
Output Tr, Tf	DO pin, Cload=15pF			10	µsec

Note 1: Sensitivity is defined as the average signal level measured at the input necessary to achieve 10e-2 Bit Error Rate (BER). The input signal is defined as a return-to-zero (RZ) waveform with 50% average duty cycle at a data rate of 2400bps. The RF input is assumed to be matched into 50Ω.

Note 2: Spurious reverse isolation represents the spurious components which appear on the RF input (ANT) pin measured into 50Ω with an input RF matching network.

Note 3: Sensitivity, a commonly specified Receiver parameter, provides an indication of the Receiver's input referred noise, generally input thermal noise. However, it is possible for a more sensitive receiver to exhibit range performance no better than that of a less sensitive receiver, if the "ether" noise is appreciably higher than the thermal noise. "Ether" noise refers to other interfering "noise" sources, such as FM radio stations, pagers, etc.

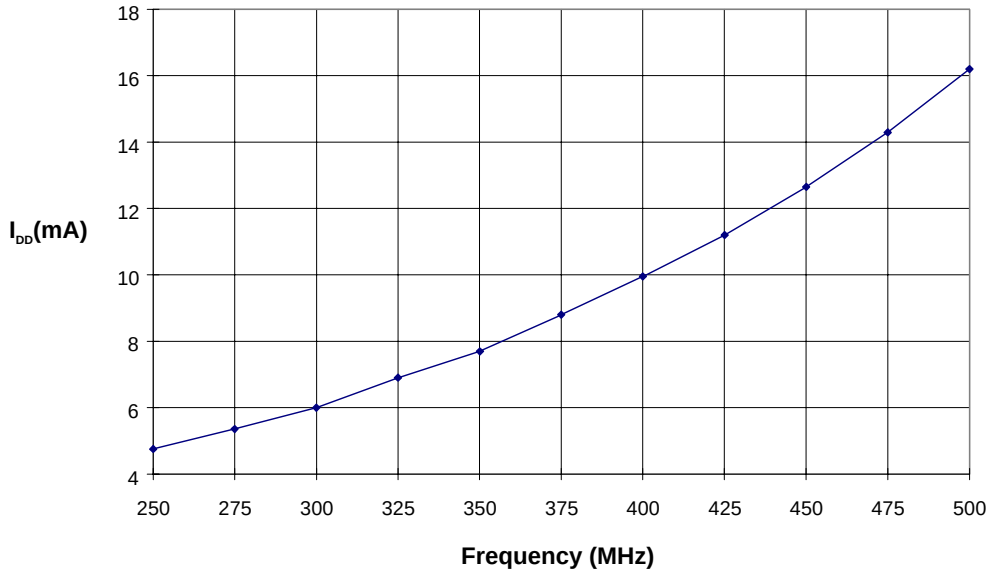
A better indicator of receiver range performance is usually given by its Selectivity, often stated as Intermediate Frequency (IF) or Radio Frequency (RF) bandwidth, depending on receiver topology. Selectivity is a measure of the rejection by the receiver of "ether" noise. More selective receivers will almost invariably provide better range. Only when the receiver selectivity is so high that most of the noise on the receiver input is actually thermal will the receiver demonstrate sensitivity-limited performance.

SEL0	SEL1	PROGRAMMABLE LPF BANDWIDTH (Hz)	CTH SOURCE IMPEDANCE (OHMS)
0	0	600	1600k
1	0	1200	800k
0	1	2400	400k
1	1	4800	200k

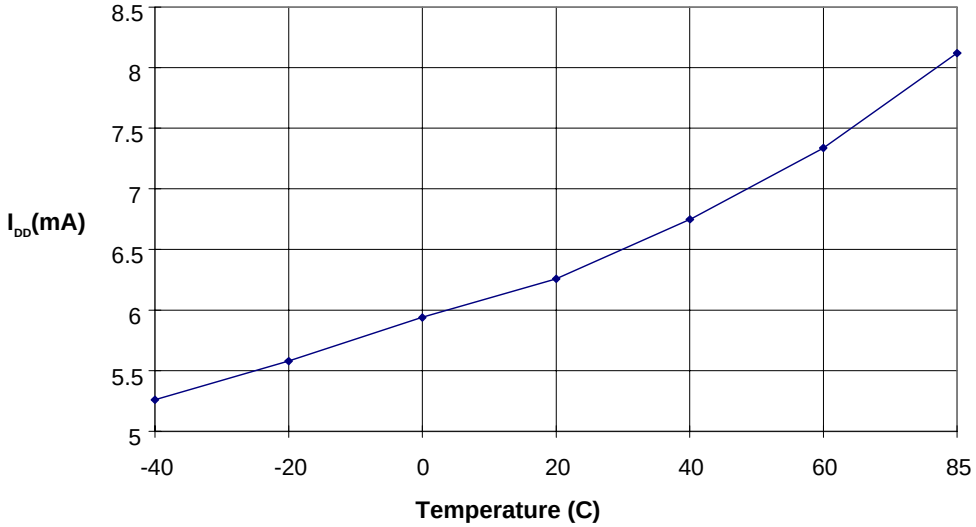
Table 1.
Nominal Characteristics
Programmable LPF Bandwidth and CTH Source Impedance

CTH Source Impedance in Table 1 is represented by (symbolic) resistor RSC in the MICRF001 Simplified Block Diagram. The Programmable LPF (Low Pass Filter) is also illustrated in the MICRF001 Simplified Block Diagram.

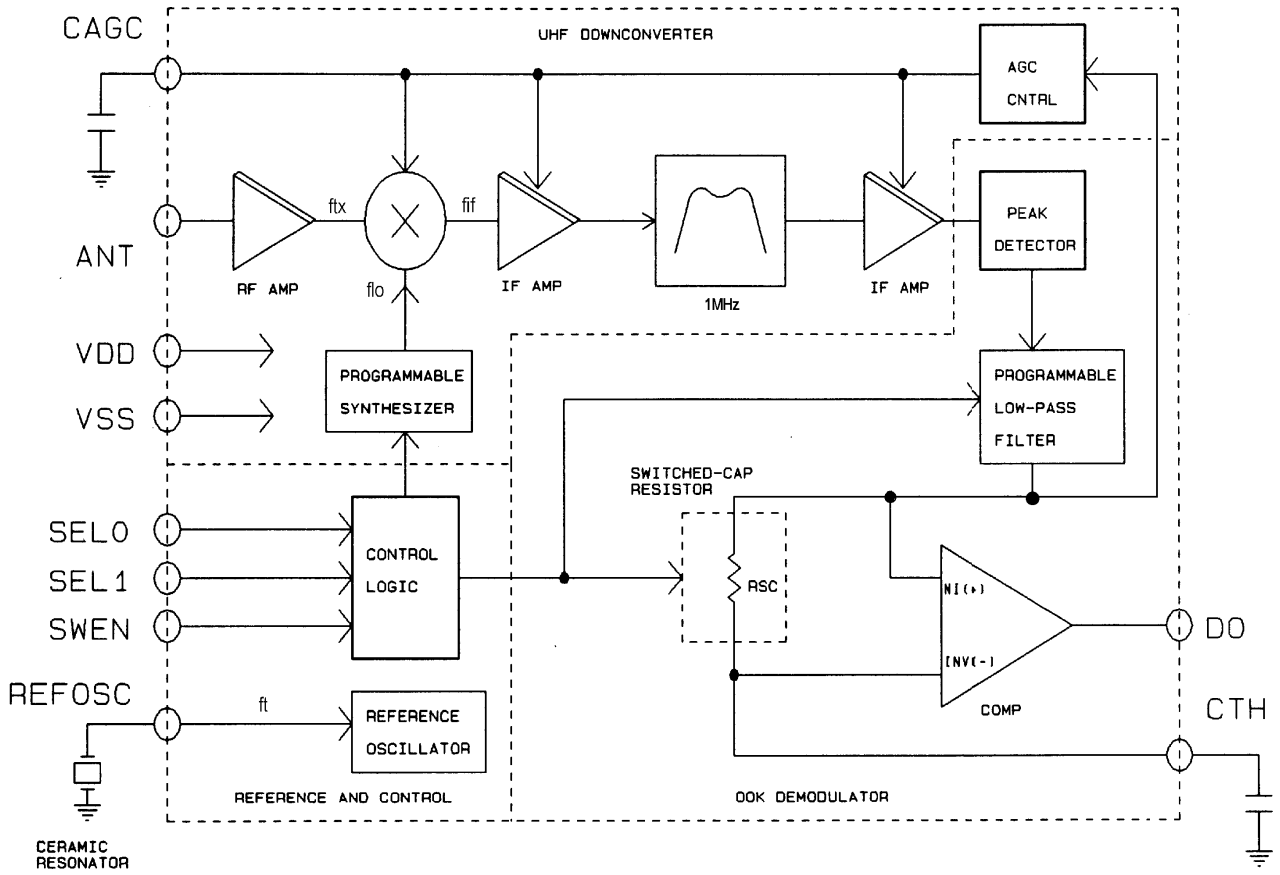
MICRF001 I_{DD} vs Frequency
(Temperature=25°C, V_{DD}=5.25V, SWP Mode)



MICRF001 I_{DD} vs Temperature
(Frequency=315MHz, V_{DD}=5.25V, SWP Mode)



Block Diagram



Functional Description

The block diagram illustrates the basic structure of the MICRF001. Identified in the figure are the three principal functional blocks of the IC, namely (1) UHF Downconverter, (2) OOK Demodulator, and (3) Reference and Control. Also shown in the figure are two capacitors (CTH, CAGC) and one timing component (CR), usually a ceramic resonator. With the exception of a supply decoupling capacitor, these are all the external components needed with the MICRF001 to construct a complete UHF receiver. Three control inputs are shown in the block diagram, SEL0, SEL1 and SWEN. Through these logic inputs the user can control the operating mode and programmable functions of the IC. These inputs are CMOS compatible, and are pulled-up on the IC. The inputs SEL0, SEL1 control the Demodulator filter bandwidth in four binary steps from approximately 0.6kHz to 4.8kHz, and the user must select the bandwidth appropriate to his needs.

The SWEN pin allows the device to be configured in either its normal (SWP) operating mode, or in standard (FIXED) superheterodyne receiver mode. SWP operation is selected when SWEN is HIGH, and is the default mode for the IC. An example of SWP operation would be where the MICRF001 must operate with LC-based transmitters, whose transmit frequency may vary up to ± 0.5% over initial tolerance, aging, and temperature. In this (patent-pending) mode, the LO frequency is varied in a prescribed fashion which results in downconversion of all signals in a band 2-3% around the transmit frequency. So the Transmitter may drift up to ± 0.5% without the need to retune the Receiver, and without impacting system performance. Such performance is not achieved with currently available crystal-based superheterodyne receivers, which can operate only with SAW or crystal based transmitters.

[Note: A range penalty will occur in installations where there exists a competing signal of sufficient strength in this small frequency band of 2-3%. This penalty also exists with super-regenerative type receivers, as their RF bandwidth is also generally 2-3%. So any application for a super-regenerative receiver is also an application for the MICRF001.]

External Control Signals and Mode Selection

For applications where the transmit frequency is accurately set for other reasons (e.g., applications where a SAW transmitter is used for its mechanical stability), the user may choose to configure the MICRF001 as a standard superheterodyne receiver (FIXED mode), mitigating the aforementioned problem of a competing close-in signal. This can be accomplished by tying SWEN to ground. Doing so forces the on-chip LO frequency to a fixed value. In such a case, the ceramic resonator would be replaced with a crystal. Generally, however, the MICRF001 can be operated with a ceramic resonator adequately, no matter whether the transmitter is LC or SAW based.

Slicing Level and the CTH Capacitor

Extraction of the DC value of the demodulated signal for purposes of logic-level data slicing is accomplished by external capacitor CTH and the on-chip switched-cap "resistor" RSC, indicated in the block diagram. The effective resistance of RSC varies in the same way as the Demodulator filter bandwidth, in four binary steps, from approximately 1600kΩ to 200kΩ. Once the filter bandwidth is selected, this "resistance" is determined; then the value of capacitor CTH is easily calculated, once the slicing level time-constant is chosen. Values vary somewhat with decoder type, but typical Slicing Level time constants range 5-50msec. Optimization of the CTH value is required to maximize range, as discussed in *"Application Note 22, MICRF001 Theory of Operation"*, section 6.4.

AGC Function and the CAGC Capacitor

The signal path has automatic gain control (AGC) to increase input dynamic range. An external capacitor, CAGC, must be applied to set the AGC attack and decay time-constants. With the addition of only a capacitor, the ratio of decay-to-attack time-constant is fixed at 10:1 (i.e., the attack time constant is 1/10th the decay time constant), and this ratio cannot be changed by the user. However, the attack time constant is selectable by the user through the value of capacitor CAGC. By adding resistance from the CAGC pin to VDDBB or VSSBB in parallel with the CAGC capacitor, the *ratio* of decay-to-attack time-constant may be varied. See *"Application Note 22, MICRF001 Theory of Operation"*.

Reference Oscillator (REFOSC) and External Timing Element

All timing and tuning operations on the MICRF001 are derived from the REFOSC function. This function is a single-pin Colpitts-type oscillator. The user may handle this pin in one of three possible ways:

(1) connect a ceramic resonator, or
(2) connect a crystal, or
(3) drive this pin with an external timing signal.

The third approach is attractive for further lowering system cost if an accurate reference signal exists elsewhere in the system (e.g., a reference clock from a crystal or ceramic resonator-based microprocessor), and flexibility exists in the choice of system transmit frequency. An externally applied signal should be AC-coupled, and resistively-divided down (or otherwise limited) to approximately 0.5Vpp. The specific reference frequency required is related to the system transmit frequency, and the operating mode of the device as set by the SWEN control pin. See *"Application Note 22, MICRF001 Theory of Operation"* for a discussion of frequency selection and accuracy requirements.

I/O Pin Interface Circuitry

Interface circuitry for the various I/O pins of the MICRF001 is shown in Figures 1 through 6. Specific information regarding each of these circuits is discussed in the following sub-paragraphs. Not shown are ESD protection diodes which are applied to all input pins.

1. ANT Pin

The ANT pin is internally AC-coupled via a 3pF capacitor, to an RF N-channel MOSFET, as shown in Figure 1. Impedance on this pin to VSS is quite high at low frequencies, and decreases as frequency increases. In the UHF frequency range, the device input can be modeled as 6.3kΩ in parallel with 2pF (pin capacitance) shunt to VSSRF.

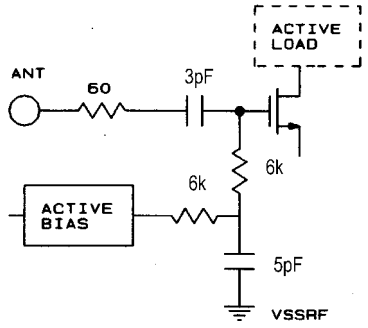


Figure 1 ANT Pin

2. CTH Pin

Figure 2 illustrates the CTH pin interface circuit. CTH pin is driven from a P-channel MOSFET source-follower biased with approximately 20µA of bias current. Transmission gates TG1 and TG2 isolate the 3.3pF capacitor. Internal control signals PHI1/PHI2 are related in a manner such that the impedance across the transmission gates looks like a "resistance". The DC potential on the CTH pin is approximately 2.2V, fundamentally determined by the Vgs of the two P-channel MOSFET source-followers shown.

3. CAGC Pin

Figure 3 illustrates the CAGC pin interface circuit. The AGC control voltage is developed as an integrated current into a capacitor CAGC. The attack current is nominally 15µA, while the decay current is a 1/10th scaling of this, approximately 1.5µA. Signal gain of the RF/IF strip inside the IC diminishes as the voltage on CAGC decreases. By simply adding a capacitor to CAGC pin, the attack/decay time constant ratio is fixed at 1:10. Further discussion on setting the attack time constant is found in *"Application Note 22, MICRF001 Theory of Operation"*, section 6.5. Modification of the attack/decay ratio is possible by adding resistance from CAGC pin either to VDDBB or VSSBB, as desired.

4. DO Pin

The output stage for the Data Comparator (DO pin) is shown in Figure 4. The output is a 10µA push-10µA pull, switched current stage. Such an output stage is capable of driving CMOS-type loads.

5. REFOSC Pin

The REFOSC input circuit is shown in Figure 5. Input impedance is quite high (200kΩ). This is a Colpitts oscillator, with internal 30pF capacitors. This input is intended to work with standard ceramic resonators, connected from this pin to VSSBB. The resonators should not contain integral capacitors, since these capacitors are contained inside the IC. Externally applied signals should be AC-coupled, amplitude limited to approximately 0.5Vpp. The nominal DC bias voltage on this pin is 1.4V.

6. Control Inputs (SEL0, SEL1, SWEN)

Control input circuitry is shown in Figure 6. The standard input is a logic inverter constructed with minimum geometry MOSFETs (Q2, Q3). P-channel MOSFET Q1 is a large channel length device which functions essentially as a "weak" pullup to VDDBB. Typical pullup current is 5µA, leading to an impedance to the VDDBB supply of typically 1MΩ.

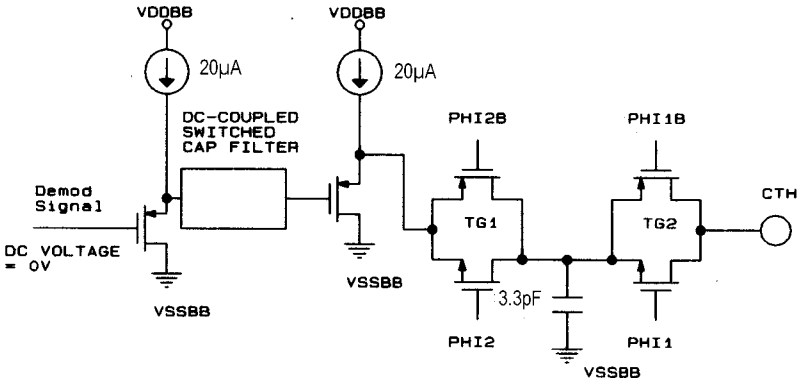


Figure 2 CTH Pin

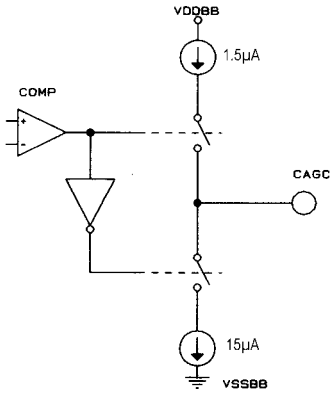


Figure 3 CAGC Pin

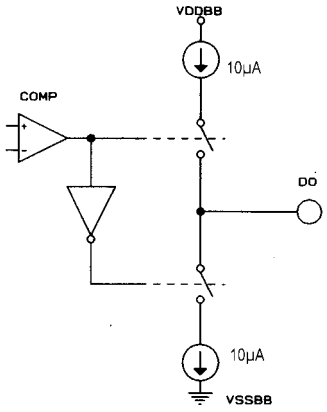


Figure 4 DO Pin

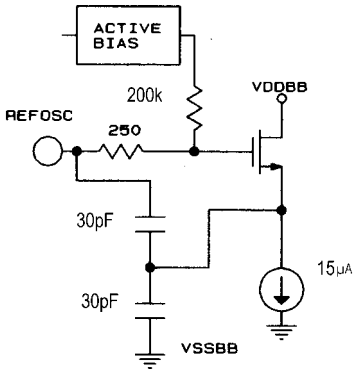


Figure 5 REFOSC Pin

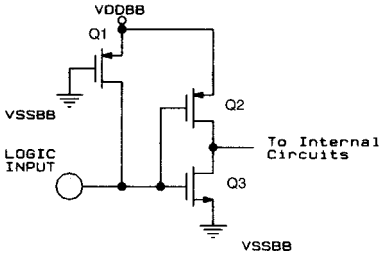
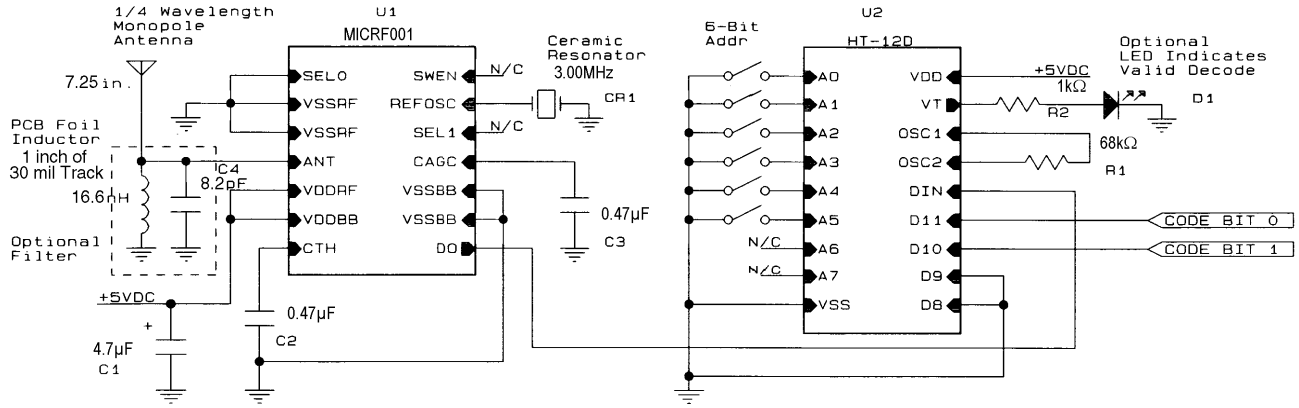


Figure 6 SEL0, SEL1, SWEN

Typical Application

The Figure below illustrates a typical application for the MICRF001 UHF Receiver IC. Operation in this example is at 387MHz, and may be customized by selection of the appropriate reference frequency (CR1), and adjustment of the antenna length. The value of C4 would also change, if the optional input filter is used. Changes from the 1kbps data rate may require a change in the value of R1. The Bill of Materials is shown in the accompanying chart.



Typical MICRF001 Application
387 MHz Operating Frequency
1kbps Operation
6-Bit Address Decode

Bill of Materials

Item	Part Number	Manufacturer	Description
U1	MICRF001	Micrel	UHF Receiver
U2	HT-12D	Holtek	Logic decoder
CR1	CSA3.00MG	Murata	3.00MHz Cer. Res.
D1	SSF-LX100LID	Lumex	RED LED
R1		Bourns	68k, 1/4W ,5%
R2		Bourns	1k,1/4W, 5%
C1		Panasonic	4.7µF, Dip Tant. Cap
C2, C3		Panasonic	0.47µF, Dip Tant. Cap
C4		Panasonic	8.2pF, COG Cer. Cap

Vendor	Telephone	Fax
Bourns	(909) 781-5500	(909) 781-5273
Holtek	(408) 894-9046	(408) 894-0838
Lumex	(800) 278-5666	(847) 359-8904
Murata	(800) 241-6574	(770) 436-3030
Panasonic	(201) 348-7000	(201) 348-8164

MICREL INC. 1849 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL + 1 (408) 944-0800 FAX + 1 (408) 944-0970 WEB http://www.micrel.com

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View MICRF001BN on WIN SOURCE
- Microchip Technology Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management