

4/8-Bit Parallel-Input Latched Drivers

Features

- 4.4 MHz Minimum Data Input Rate
- High-Voltage, High-Current Sink Outputs
- Output Transient Protection
- CMOS, PMOS, NMOS, and TTL Compatible Inputs
- Internal Pull-Down Resistors
- Low-Power CMOS Latches

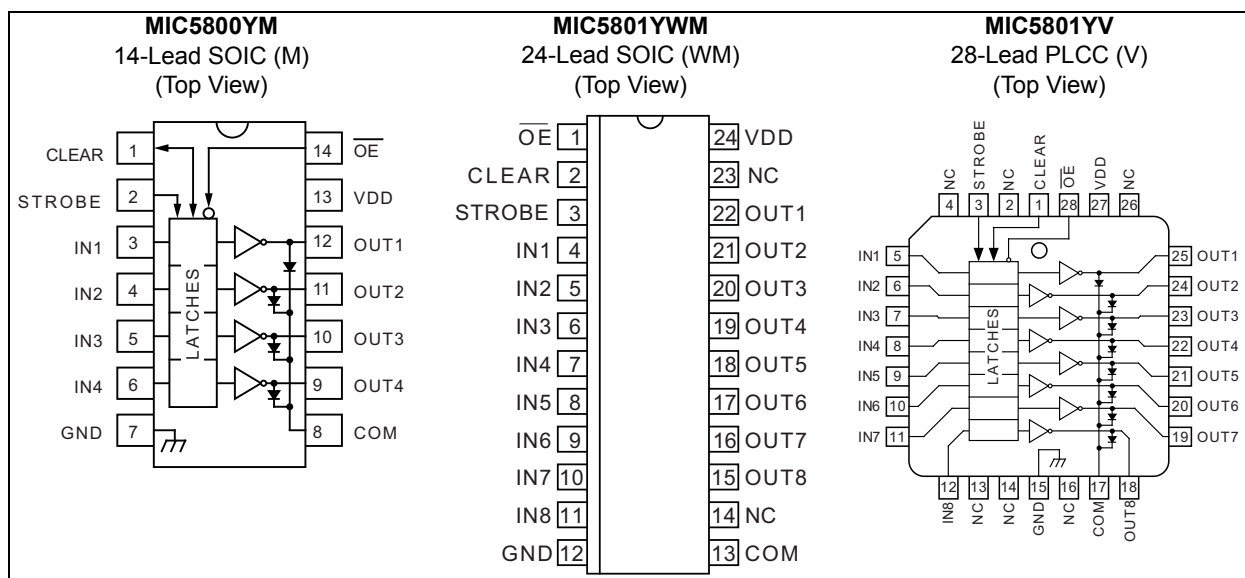
General Description

The MIC5800 and MIC5801 latched drivers are high-voltage, high-current integrated circuits comprised of four or eight CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common CLEAR, STROBE, and OUTPUT ENABLE functions.

The bipolar/MOS combination provides an extremely low-power latch with maximum interface flexibility. MIC5800 contains four latched drivers; MIC5801 contains eight latched drivers.

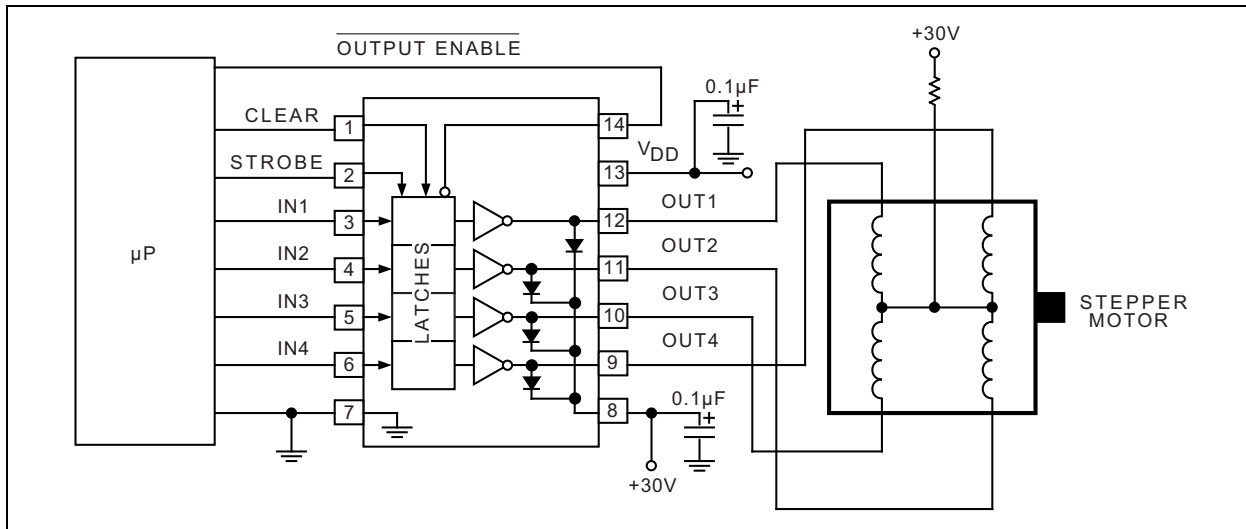
Data input rates are greatly improved in these devices. With a 5V supply, they will typically operate at better than 5 MHz. With a 12V supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors. The bipolar outputs are suitable for use with relays, solenoids, stepping motors, LED or incandescent displays, and other high-power loads. Both units have open-collector outputs and integral diodes for inductive load transient suppression. The output transistors are capable of sinking 500 mA and will sustain at least 50V in the OFF state. Because of limitations on package power dissipation, the simultaneous operation of all drivers at maximum rated current can only be accomplished by a reduction in duty cycle. Outputs may be connected in parallel for higher load current capability.

Package Types

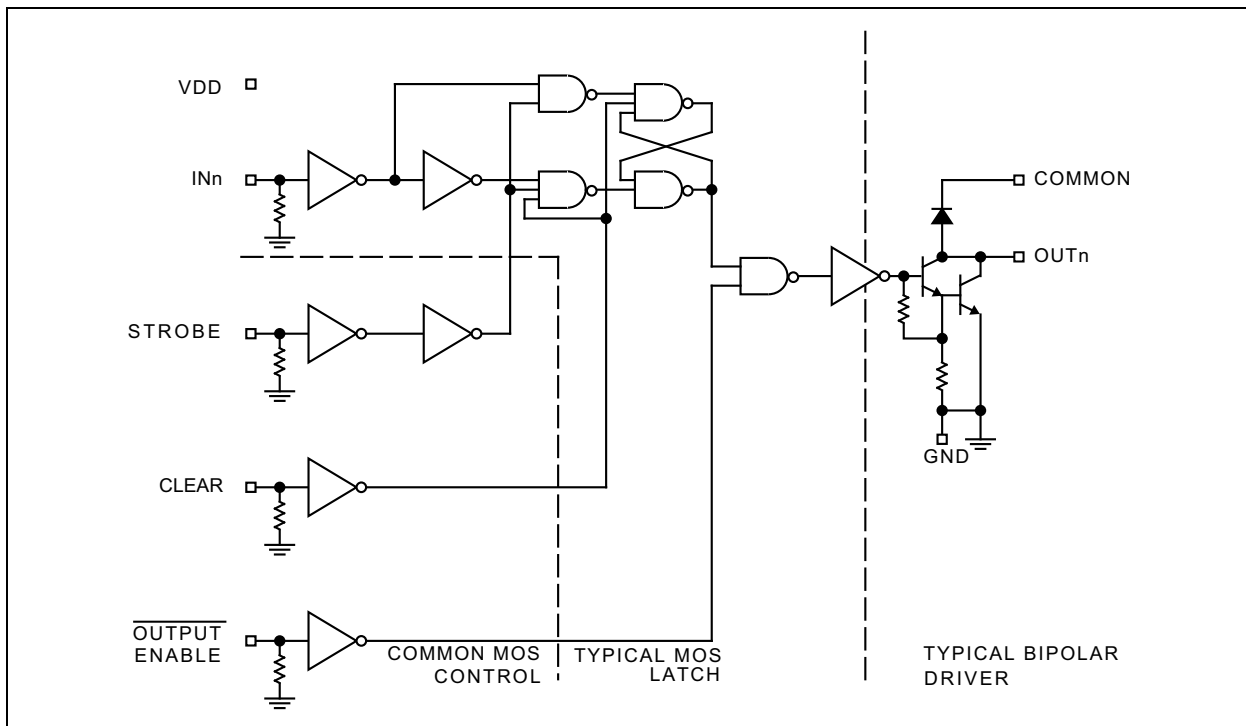


MIC5800/1

Typical Application Circuit



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Output Voltage (V_{CE})	+50V
Supply Voltage (V_{DD})	+15V
Input Voltage Range (V_{IN})	-0.3V to $V_{DD} + 0.3V$
Continuous Collector Current (I_C)	500 mA
ESD Rating (Note 1)	ESD Sensitive

Operating Ratings ††

Package Power Dissipation (P_D)	
MIC5800 SOIC	1.0W
Derate above $T_A = +25^\circ C$	8.5 mW/ $^\circ C$
MIC5801 PLCC	2.25W
Derate above $T_A = +25^\circ C$	18.2 mW/ $^\circ C$
MIC5801 Wide SOIC	1.4W
Derate above $T_A = +25^\circ C$	11 mW/ $^\circ C$

† Notice: Exceeding the absolute maximum ratings may damage the device.

†† Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: Microchip CMOS devices have input-static protection, but are susceptible to damage when exposed to extremely high static electrical charges.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $V_{DD} = 5V$, $T_A = +25^\circ C$, $V_A \leq +85^\circ C$ unless otherwise noted. Note 1						
Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Output Leakage Current	I_{CEX}	—	—	50	μA	$V_{CE} = 50V$, $T_A = +25^\circ C$
		—	—	100		$V_{CE} = 50V$, $T_A = +70^\circ C$
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	—	0.9	1.1	V	$I_C = 100$ mA
		—	1.1	1.3		$I_C = 200$ mA
		—	1.3	1.6		$I_C = 350$ mA, $V_{DD} = 7.0V$
Input Voltage (Low)	$V_{IN(0)}$	—	—	1.0	V	—
Input Voltage (High)	$V_{IN(1)}$	10.5	—	—	V	$V_{DD} = 12V$
		8.5	—	—		$V_{DD} = 10V$
		3.5	—	—		$V_{DD} = 5V$, Note 2
Input Resistance	R_{IN}	50	200	—	k Ω	$V_{DD} = 12V$
		50	300	—		$V_{DD} = 10V$
		50	600	—		$V_{DD} = 5V$
Supply Current ON (Each Stage)	$I_{DD(ON)}$	—	1.0	2.0	mA	$V_{DD} = 12V$, Outputs Open
		—	0.9	1.7		$V_{DD} = 10V$, Outputs Open
		—	0.7	1.0		$V_{DD} = 5V$, Outputs Open
Supply Current OFF (Total)	$I_{DD(OFF)}$	—	—	200	μA	$V_{DD} = 12V$, Outputs Open, Inputs = 0V
		—	50	100		$V_{DD} = 5V$, Outputs Open, Inputs = 0V

Note 1: Specification for packaged product only.

2: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure a minimum logic "1".

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: $V_{DD} = 5V$, $T_A = +25^\circ C$, $V_A \leq +85^\circ C$ unless otherwise noted. Note 1						
Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Clamp Diode Leakage Current	I_R	—	—	50	μA	$V_R = 50V$, $T_A = +25^\circ C$
		—	—	100		$V_R = 50V$, $T_A = +70^\circ C$
Clamp Diode Forward Voltage	V_F	—	1.7	2.0	V	$I_F = 350\text{ mA}$

Note 1: Specification for packaged product only.

2: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure a minimum logic "1".

TRUTH TABLE

IN_N	Strobe	Clear	/OE	OUT_N	
				$t - 1$	t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

Legend: X = Irrelevant; $t - 1$ = Previous output state; t = Present output state.

Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high /OE will set all outputs to the off condition, regardless of any other input conditions. When the /OE is low, the outputs depend on the state of their respective latches.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Storage Temperature Range	T_S	-65	—	+125	$^\circ C$	—
Operating Temperature Range	T_A	-40	—	+85	$^\circ C$	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A , T_J , θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125 $^\circ C$ rating. Sustained junction temperatures above +125 $^\circ C$ can impact the device reliability.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 2-1](#) and [Table 2-2](#).

TABLE 2-1: MIC5800 PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	CLEAR	Resets all latches and turns all outputs OFF (open).
2	STROBE	Input strobe pin. Loads output latches when high.
3, 4, 5, 6	IN _N	Parallel inputs, 1 through 4.
7	GND	Logic and Output Ground pin.
8	COM	Transient suppression diode common cathode pin.
9, 10, 11, 12	OUT _N	Parallel outputs, 4 through 1.
13	VDD	Logic Supply Voltage.
14	/OE	Output Enable. When low, outputs are active. When high, outputs are inactive and device is reset from a fault condition. An undervoltage condition emulates a high OE input.

TABLE 2-2: MIC5801 PIN FUNCTION TABLE

Pin Number SOIC	Pin Number PLCC	Pin Name	Description
1	28	/OE	Output Enable. When low, outputs are active. When high, outputs are inactive and device is reset from a fault condition. An undervoltage condition emulates a high OE input.
2	1	CLEAR	Resets all latches and turns all outputs OFF (open).
3	3	STROBE	Input strobe pin. Loads output latches when high.
4, 5, 6, 7, 8, 9, 10, 11	5, 6, 7, 8, 9, 10, 11, 12	IN _N	Parallel inputs, 1 through 8.
12	15	GND	Logic and Output Ground pin.
13	17	COM	Transient suppression diode common cathode pin.
14, 23	2, 4, 13, 14, 16, 26	NC	No Connection. Leave floating.
15, 16, 17, 18, 19, 20, 21, 22	18, 19, 20, 21, 22, 23, 24, 25	OUT _N	Parallel outputs, 8 through 1.
24	27	VDD	Logic Supply Voltage.

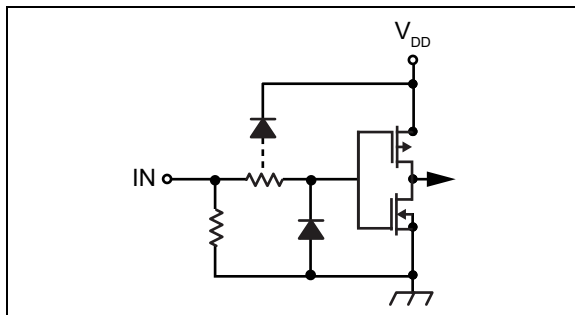


FIGURE 2-1: Typical Input.

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3.0 TIMING

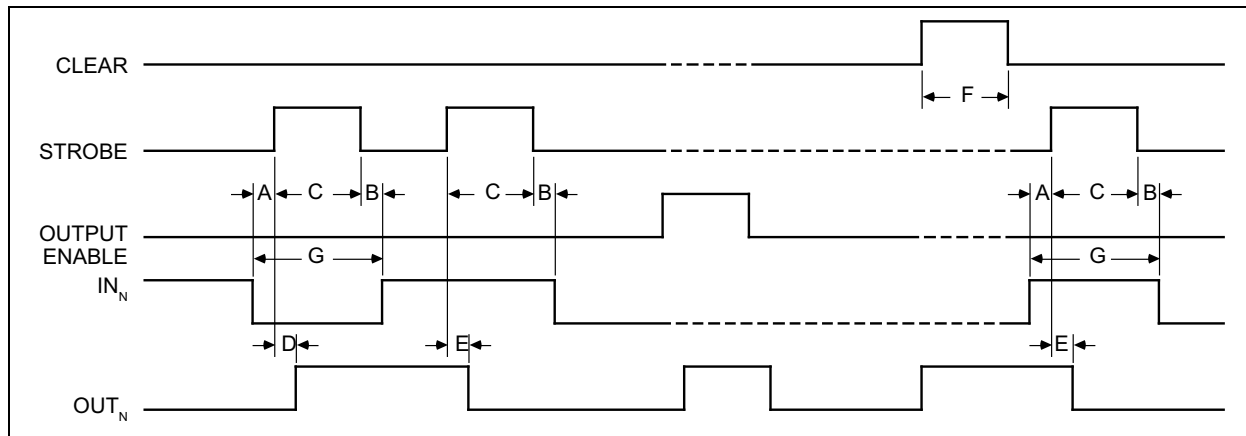


FIGURE 3-1: Timing Diagram.

TABLE 3-1: TIMING CONDITIONS

Characteristics: $T_A = +25^\circ\text{C}$; Logic levels are V_{DD} and Ground; $V_{DD} = 5\text{V}$.

Condition	Min.	Typ.	Max.
A. Minimum data active time before strobe enabled (data set-up time)	50 ns	—	—
B. Minimum data active time after strobe disabled (data hold time)	50 ns	—	—
C. Minimum strobe pulse width	125 ns	—	—
D. Typical time between strobe activation and output on to off transition	—	500 ns	—
E. Typical time between strobe activation and output off to on transition	—	500 ns	—
F. Minimum clear pulse width	300 ns	—	—
G. Minimum data pulse width	225 ns	—	—

4.0 TYPICAL APPLICATIONS

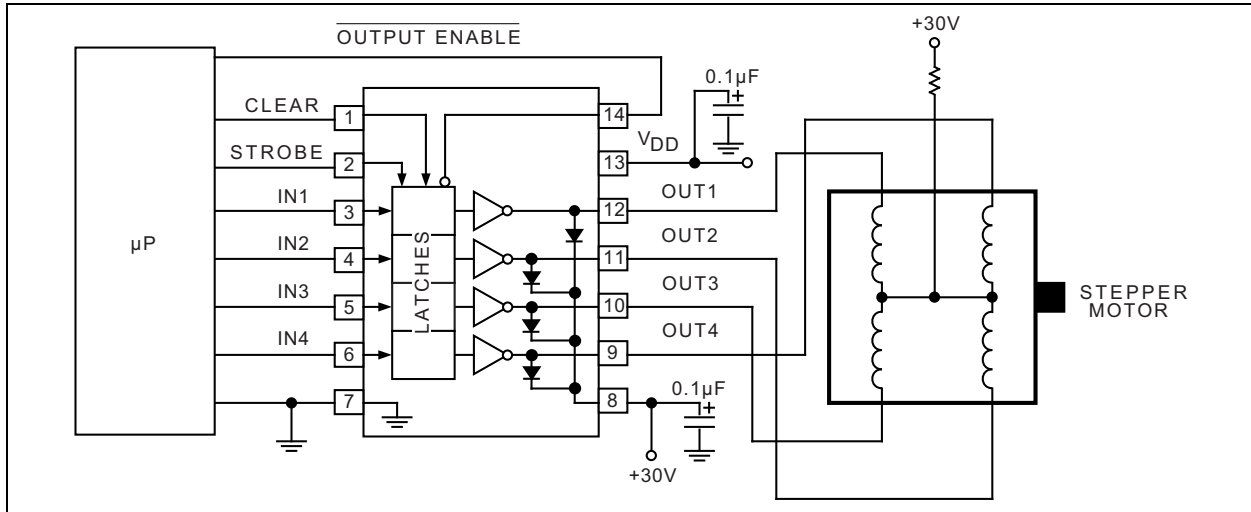


FIGURE 4-1: MIC5800 Unipolar Stepper-Motor Drive.

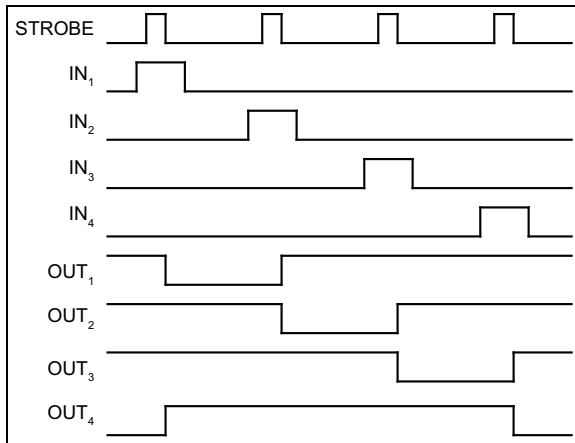


FIGURE 4-2: Unipolar Wave Drive.

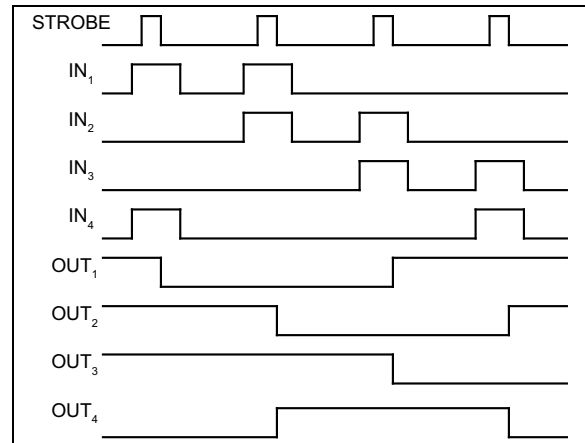


FIGURE 4-3: Unipolar 2-Phase Drive.

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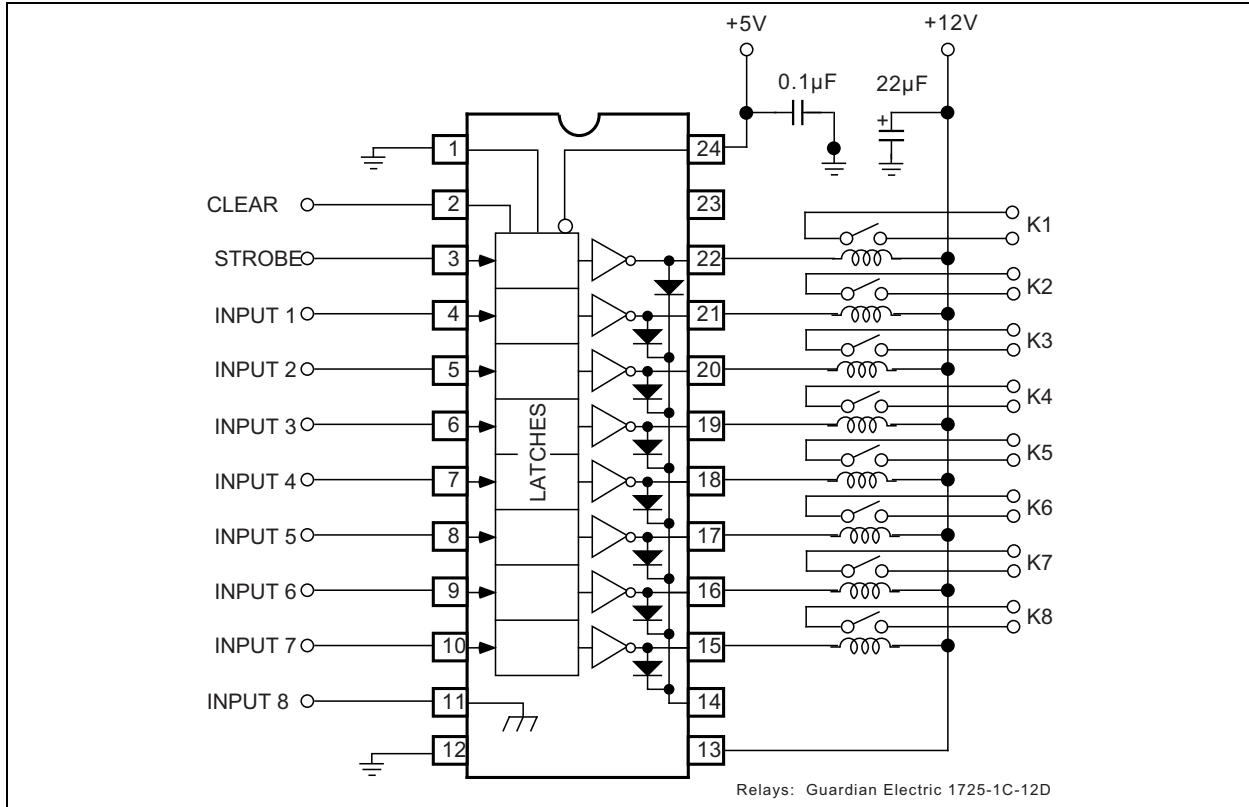


FIGURE 4-4: MIC5801 Relay Driver.

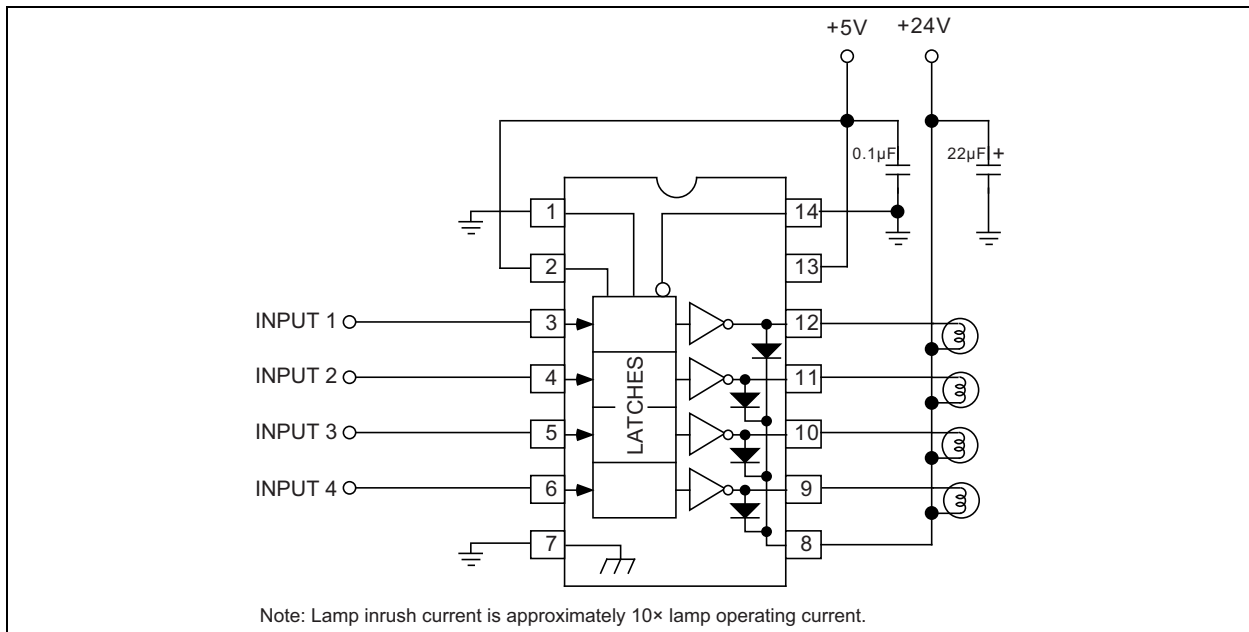


FIGURE 4-5: MIC5800 Incandescent/Halogen Lamp Driver.

5.0 PACKAGING INFORMATION

5.1 Package Marking Information

14-Lead SOIC*	Example
14-Lead PDIP*	Example
28-Lead PLCC*	Example
24-Lead SOICW*	Example

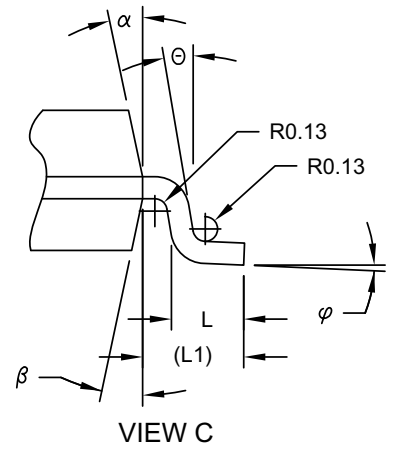
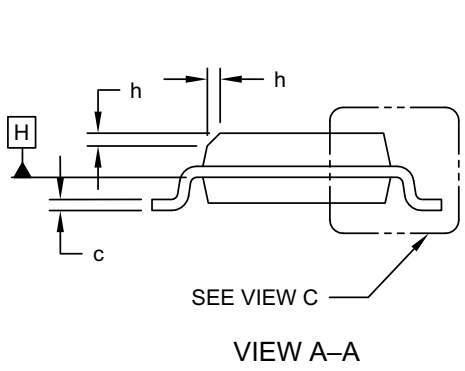
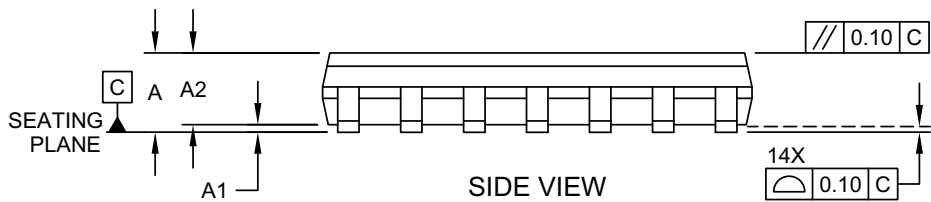
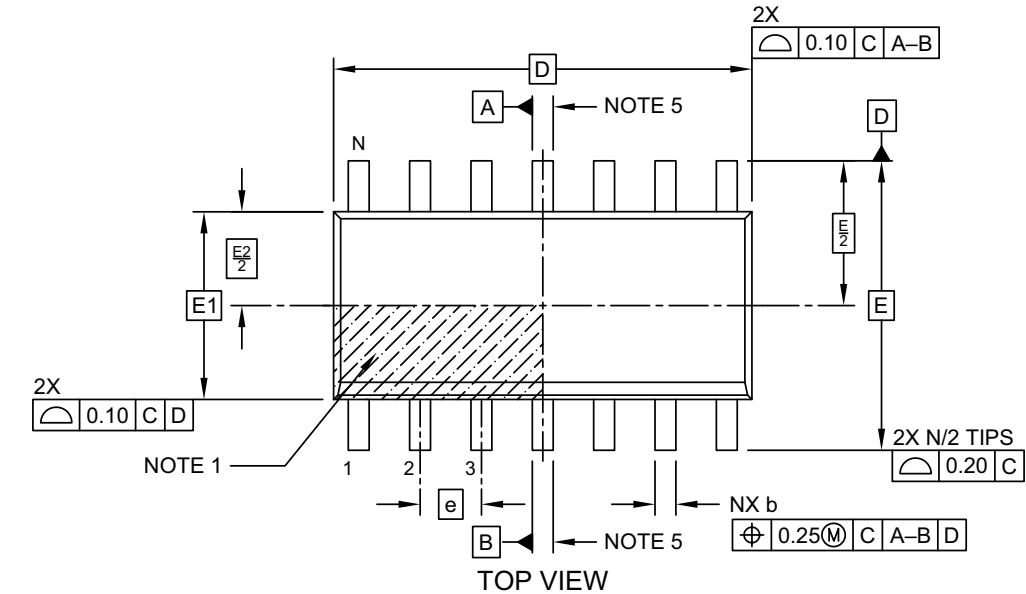
Legend:	<p>XX...X Product code or customer-specific information</p> <p>Y Year code (last digit of calendar year)</p> <p>YY Year code (last 2 digits of calendar year)</p> <p>WW Week code (week of January 1 is week '01')</p> <p>NNN Alphanumeric traceability code</p> <p>(e3) Pb-free JEDEC® designator for Matte Tin (Sn)</p> <p>* This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.</p> <p>•, ▲, ▼ Pin one index is identified by a dot, delta up, or delta down (triangle mark).</p>
Note:	<p>In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.</p> <p>Underbar (_) and/or Overbar (¯) symbol may not be to scale.</p>

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14-Lead Plastic Small Outline SOIC Package Outline and Recommended Land Pattern

14-Lead Plastic Small Outline (D3X, UEB, M5B, UEB) - Narrow, 3.90 mm Body [SOIC] Atmel Legacy Global Package Code SVQ

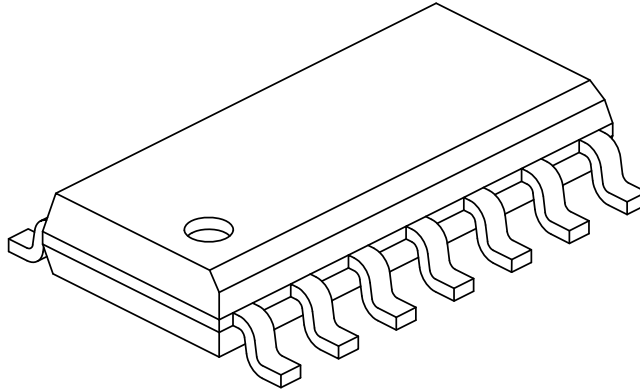
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing No. C04-065-D3X Rev D

14-Lead Plastic Small Outline (D3X, UEB, M5B, UEB) - Narrow, 3.90 mm Body [SOIC] Atmel Legacy Global Package Code SVQ

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	8.65 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

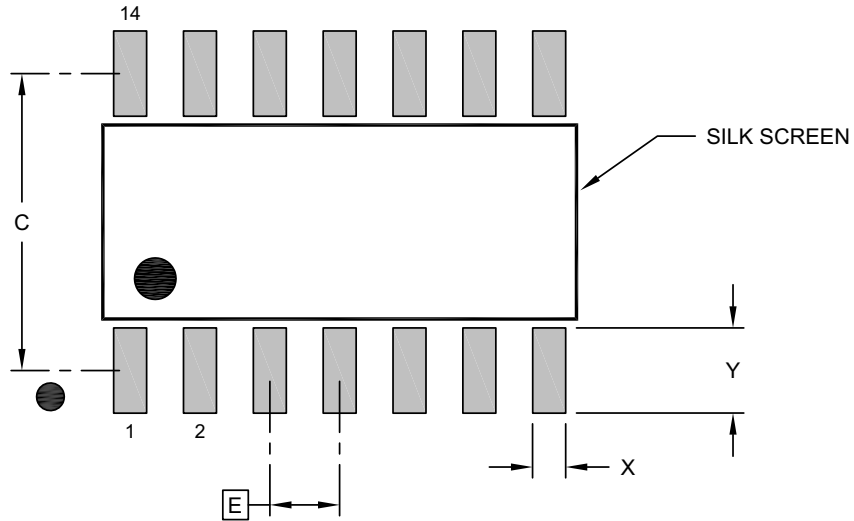
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.
- Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065-D3X Rev D Sheet 2 of 2

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14-Lead Plastic Small Outline (D3X, UEB, M5B, UEB) - Narrow, 3.90 mm Body [SOIC] Atmel Legacy Global Package Code SVQ

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X14)	X			0.60
Contact Pad Length (X14)	Y			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

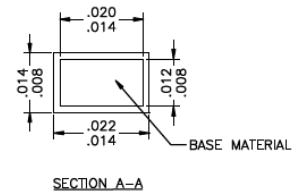
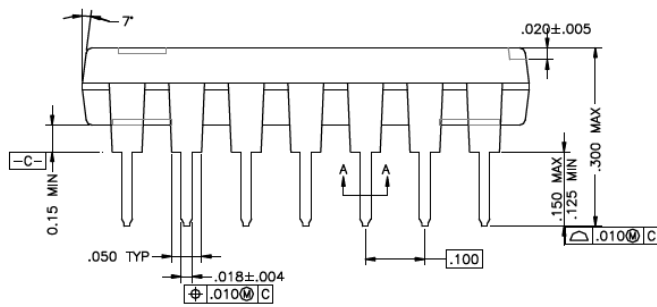
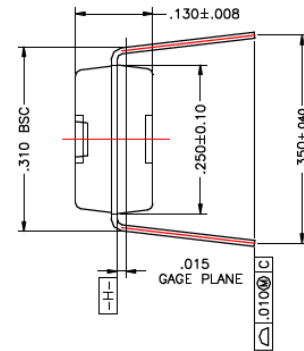
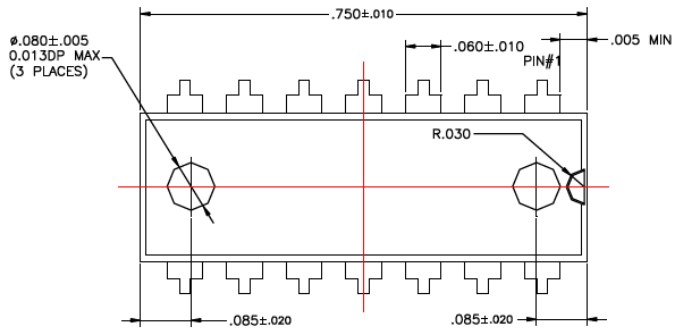
Microchip Technology Drawing No. C04-2065-D3X Rev D

14-Lead PDIP Package Outline and Recommended Land Pattern

TITLE

14 LEAD PDIP PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

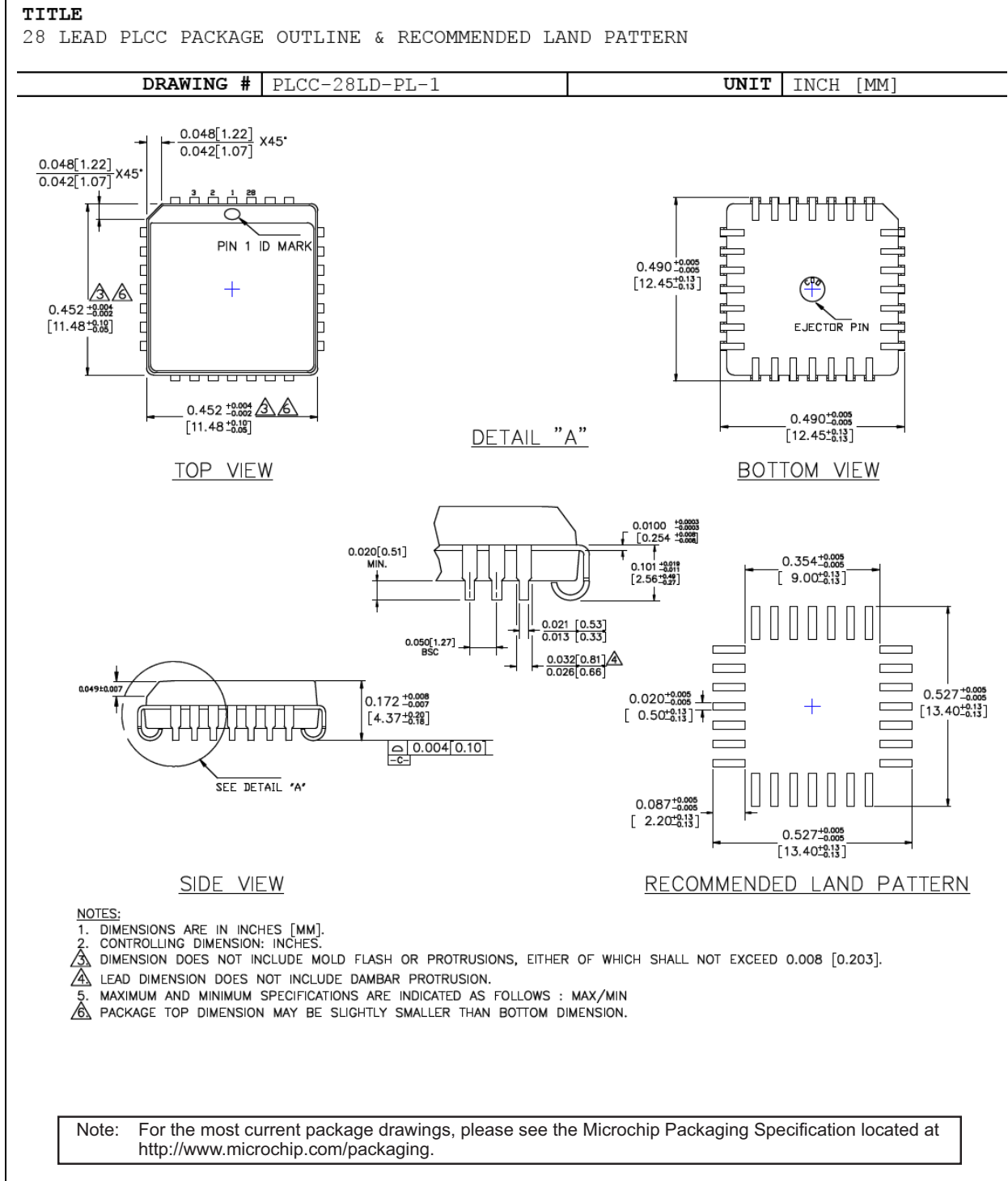
DRAWING #	PDIP-14LD-PL-1	UNIT	INCH
LEAD FRAME	Copper	LEAD FINISH	Matte Tin



Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

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28-Lead PLCC Package Outline and Recommended Land Pattern

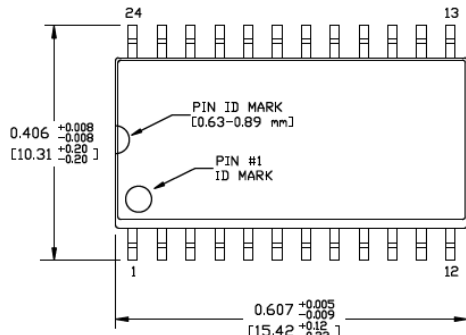


24-Lead SOICW Package Outline and Recommended Land Pattern

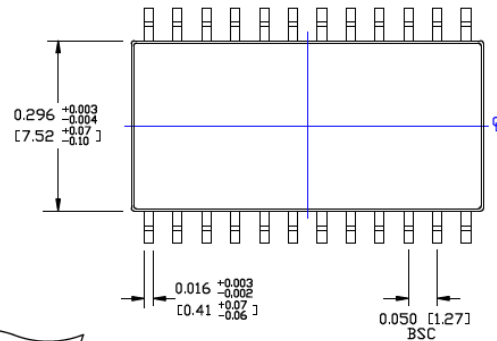
TITLE

24 LEAD SOICW PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

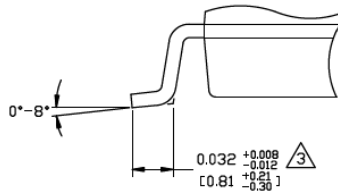
DRAWING #	SOICW-24LD-PL-1	UNIT	INCH [MM]
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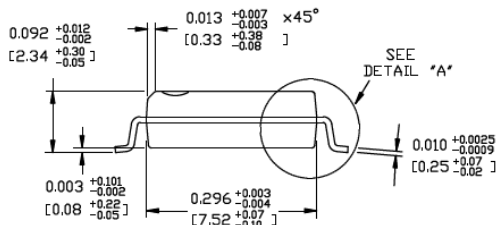
TOP VIEW
NOTE · 1, 2



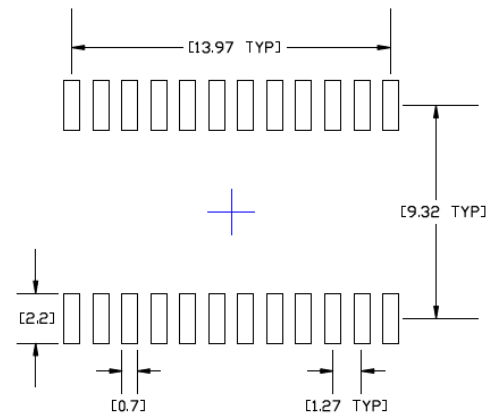
BOTTOM VIEW
NOTE · 1, 2



DETAIL "A"



END VIEW
NOTE · 1, 2, 3



RECOMMENDED LAND PATTERN

NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.006[0.15] PER SIDE.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

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NOTES:

APPENDIX A: REVISION HISTORY

Revision A (April 2019)

- Converted Micrel document MIC5800/1 to Microchip data sheet template DS20006184A.
- Minor grammatical text changes throughout.

MIC5800/1

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Device	<u>X</u>	<u>XX</u>	<u>-XX</u>	
Part No.	Junction Temp. Range	Package	Media Type	
Device:	MIC5800:	4-Bit Parallel-Input, High-Voltage, High-Current Latched Driver		
	MIC5801:	8-Bit Parallel-Input, High-Voltage, High-Current Latched Driver		
Junction Temperature Range:	Y =	-40°C to +85°C, Industrial		
Package:	M =	14-Lead SOIC (MIC5800)		
	N =	14-Lead PDIP (MIC5800)		
	V =	28-Lead PLCC (MIC5801)		
	WM =	24-Lead Wide SOIC (MIC5801)		
Media Type:	<blank>=	54/Tube (M, MIC5800)		
	<blank>=	25/Tube (N, MIC5800)		
	<blank>=	38/Tube (V, MIC5801)		
	<blank>=	31/Tube (WM, MIC5801)		
	TR =	750/Reel (V, MIC5801)		
	TR =	1,000/Reel (WM, MIC5801)		
	TR =	2,500/Reel (M, MIC5800)		
				Examples:
				a) MIC5800YM: MIC5800, -40°C to +85°C Temperature Range, 14-Lead SOIC, 54/Tube
				b) MIC5800YM-TR: MIC5800, -40°C to +85°C Temperature Range, 14-Lead SOIC, 2,500/Reel
				c) MIC5800YN: MIC5800, -40°C to +85°C Temperature Range, 14-Lead PDIP, 25/Tube
				d) MIC5801YV: MIC5801, -40°C to +85°C Temperature Range, 28-Lead PLCC, 38/Tube
				e) MIC5801YV-TR: MIC5801, -40°C to +85°C Temperature Range, 28-Lead PLCC, 750/Reel
				f) MIC5801YWM: MIC5801, -40°C to +85°C Temperature Range, 24-Lead Wide SOIC, 31/Tube
				g) MIC5801YWM-TR: MIC5801, -40°C to +85°C Temperature Range, 24-Lead Wide SOIC, 1,000/Reel
				Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

**QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
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