MIC4123/4/5

Dual 3A Peak Low-Side MOSFET Drivers

Features

- Reliable, Low-Power Bipolar/CMOS/DMOS Construction
- Latch-Up Protected to >200 mA Reverse Current
- Logic Input Withstands Swing to –5V
- High 3A Peak Output Current
- Wide 4.5V to 20V Operating Range
- Drives 1800 pF Capacitance in 25 ns
- Short <50 ns Typical Delay Time
- Delay Times Consistent within Supply Voltage Change
- Matched Rise and Fall Times
- TTL Logic Input Independent of Supply Voltage
- Low Equivalent 6 pF Input Capacitance
- Low Supply Current
  - 3.5 mA with Logic-1 Input
  - 350 µA with Logic-0 Input
- Low 2.3Ω Typical Output Impedance
- Output Voltage Swings within 25 mV of Ground or V_S
- '426/7/8-, '1426/7/8-, '4426/7/8-Compatible Pinout
- Inverting, Non-Inverting, and Differential Configurations
- Exposed Backside Pad Packaging Reduces Heat
  - ePad SOIC-8L (θ_{JA} = 58°C/W)
  - 4 mm x 4 mm VDFN-8L (θ_{JA} = 45°C/W)

General Description

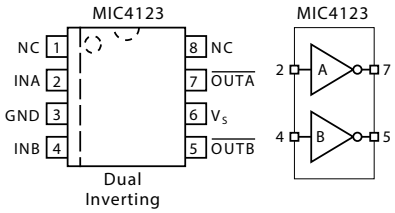
The MIC4123/4124/4125 family are highly reliable BiCMOS/DMOS buffer/driver/MOSFET drivers. They are higher output current versions of the MIC4126/4127/4128, which are improved versions of the MIC4426/4427/4428. All three families are pin-compatible. The MIC4123/4/5 drivers are capable of providing reliable service in more demanding electrical environments than their predecessors. They will not latch under any conditions within their power and voltage ratings. They can survive up to 5V of noise spiking, of either polarity, on the ground pin. They can accept, without either damage or logic upset, up to half an amp of reverse current (either polarity) forced back into their outputs.

The MIC4123/4/5 series drivers are easier to use, more flexible in operation, and more forgiving than other CMOS or bipolar drivers currently available. Their BiCMOS/DMOS construction dissipates minimum power and provides rail-to-rail voltage swings.

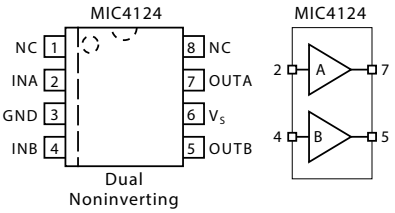
Primarily intended for driving power MOSFETs, the MIC4123/4/5 drivers are suitable for driving other loads (capacitive, resistive, or inductive) that require low-impedance, high peak currents, and fast switching times. Heavily loaded clock lines, coaxial cables, or piezoelectric transducers are some examples. The only known limitation on loading is that total power dissipated in the driver must be kept within the maximum power dissipation limits of the package.

Package Types

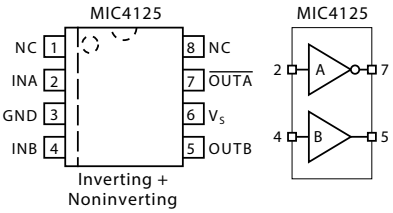
MIC4123
ePad SOIC-8 (ME)
VDFN-8 (ML)
(Top View)



MIC4124
ePad SOIC-8 (ME)
VDFN-8 (ML)
(Top View)



MIC4125
ePad SOIC-8 (ME)
VDFN-8 (ML)
(Top View)



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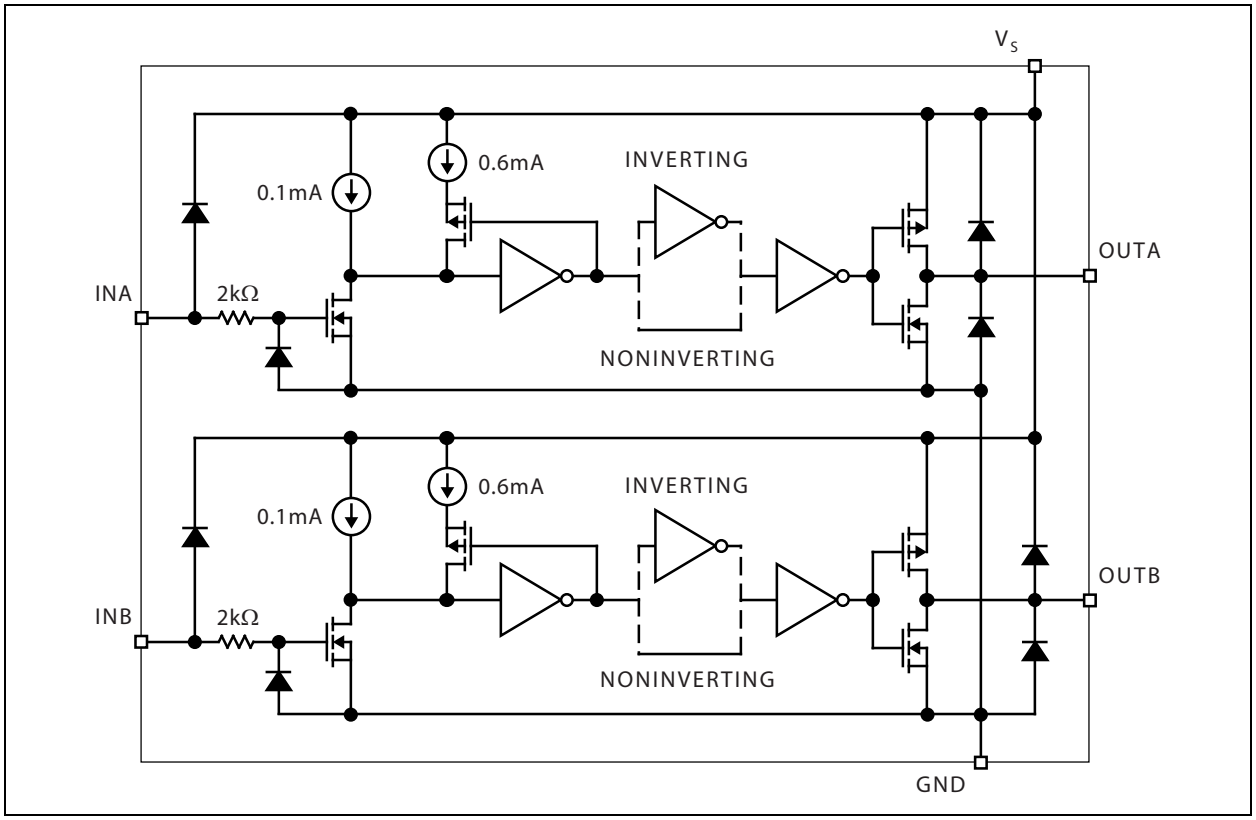
Functional Block Diagram



The function block diagram contains only four resistors, four capacitors, and 52 transistors. Be sure to ground any unused inputs.

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage ..... +24V
Input Voltage ..... V_S + 0.3V to GND – 5V
ESD Susceptibility ..... (Note 1)

Operating Ratings ††

Supply Voltage (V_S) ..... +4.5V to +20V

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† **Notice:** The device is not guaranteed to function outside its operating ratings.

Note 1: Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5 kΩ in series with 100 pF.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: 4.5V ≤ V_S ≤ 20V; T_A = +25°C, **bold** values indicate –40°C ≤ T_J ≤ +125°C; unless noted. Input voltage slew rate >2.5 V/µs. Note 1

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Input						
Logic 1 Input Voltage	V_{IH}	**2.4**	1.5	—	V	—
Logic 0 Input Voltage	V_{IL}	—	1.3	**0.8**	V	—
Input Current	I_{IN}	–1	—	1	µA	0V ≤ V_{IN} ≤ V_S
		–10	—	**10**		—
Output						
High Output Voltage	V_{OH}	**V_S – 0.025**	—	—	V	I_{OUT} = 100 µA
Low Output Voltage	V_{OL}	—	—	**0.025**	V	I_{OUT} = –100 µA
Output Resistance High State	R_O	—	2.3	5	Ω	I_{OUT} = 10 mA, V_S = 20V
		—	—	**8**		—
Output Resistance Low State		—	2.2	5		I_{OUT} = 10 mA, V_S = 20V
		—	—	**8**		—
Peak Output Current	I_{PK}	—	3	—	A	—
Latch-Up Protection Withstand Reverse Current	I	>200	—	—	mA	—
Switching Time						
Rise Time	t_r	—	11	35	ns	Test Figure 1-1, C_L = 1800 pF
		—	—	**60**		—
Fall Time	t_f	—	11	35	ns	Test Figure 1-1, C_L = 1800 pF
		—	—	**60**		—

Note 1: Specification for packaged product only.

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: 4.5V ≤ V_S ≤ 20V; T_A = +25°C, **bold** values indicate –40°C ≤ T_J ≤ +125°C; unless noted. Input voltage slew rate >2.5 V/µs. Note 1

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Delay Time	t_{D1}	—	44	75	ns	Test Figure 1-1, C_L = 1800 pF
		—	—	**100**		—
Delay Time	t_{D2}	—	59	75	ns	Test Figure 1-1, C_L = 1800 pF
		—	—	**100**		—
Power Supply						
Power Supply Current	I_S	—	1.5	2.5	mA	V_{IN} = 3.0V (both inputs)
		—	—	**3.5**		—
Power Supply Current	I_S	—	0.15	0.25	mA	V_{IN} = 0V (both inputs)
		—	—	**0.3**		—

Note 1: Specification for packaged product only.

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TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Maximum Junction Temperature	T_J	—	—	+150	°C	—
Storage Temperature Range	T_S	–65	—	+150	°C	—
Lead Temperature	—	—	—	+300	°C	10 sec.
Junction Operating Temperature Range	T_J	–40	—	+125	°C	—
Package Thermal Resistances						
Thermal Resistance, 4x4 VDFN 8-Ld	θ_{JA}	—	45	—	°C/W	—
Thermal Resistance, EP SOIC-8	θ_{JA}	—	58	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

Test Circuits

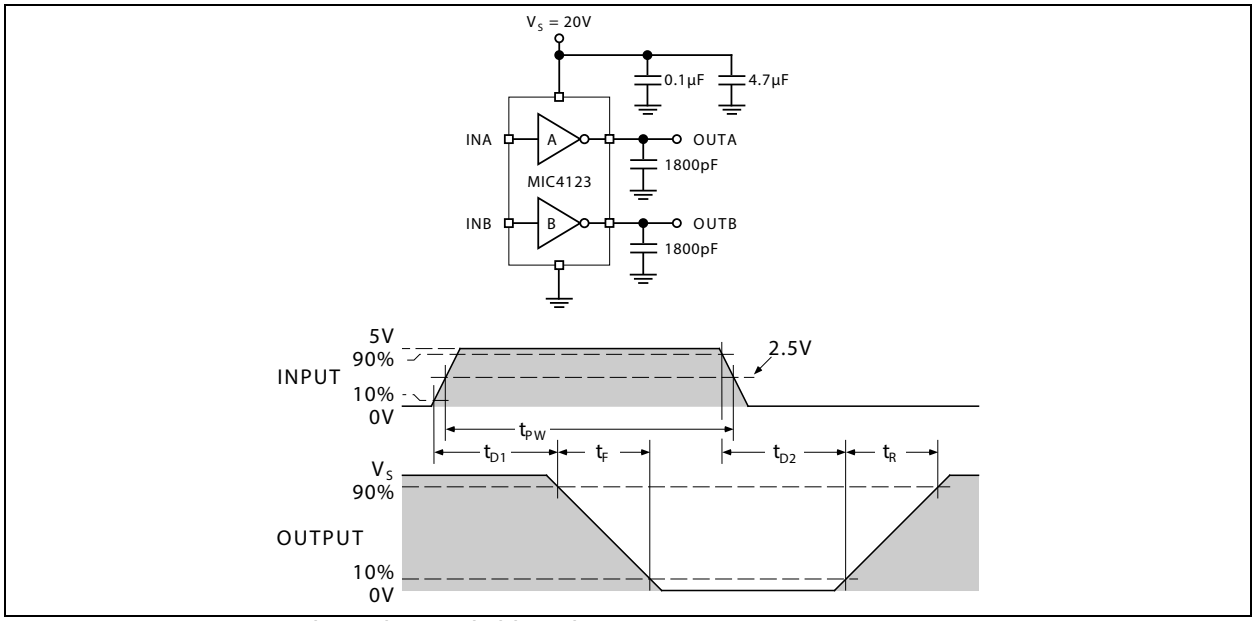

FIGURE 1-1: *Inverting Driver Switching Time.*

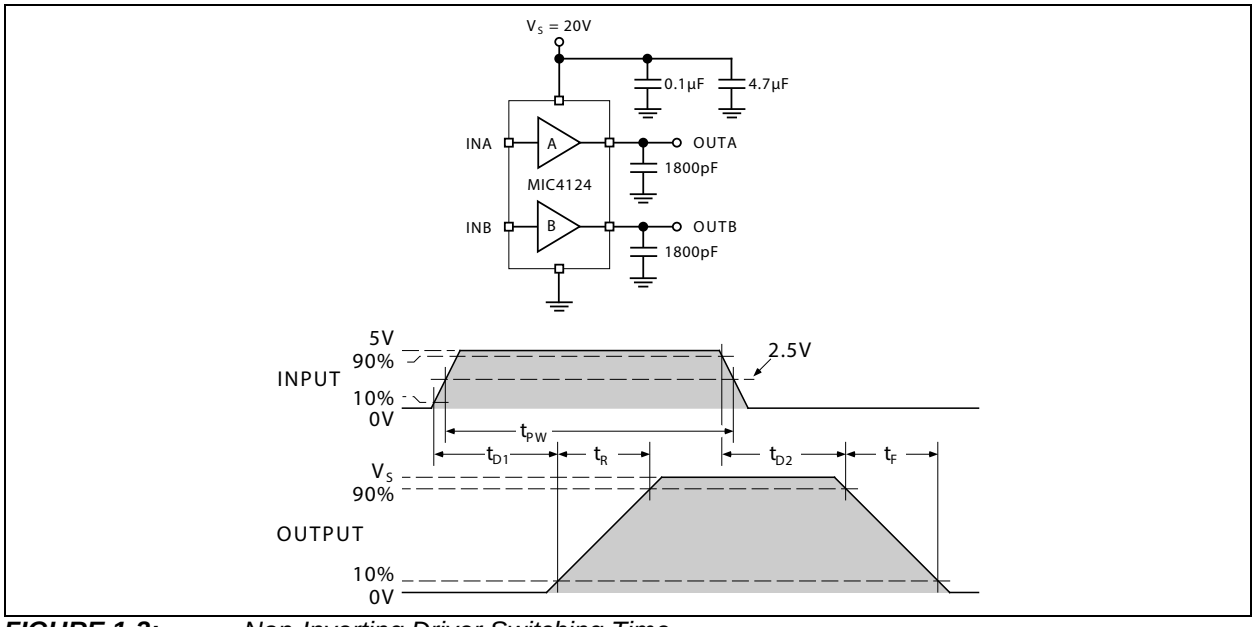

FIGURE 1-2: *Non-Inverting Driver Switching Time.*

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

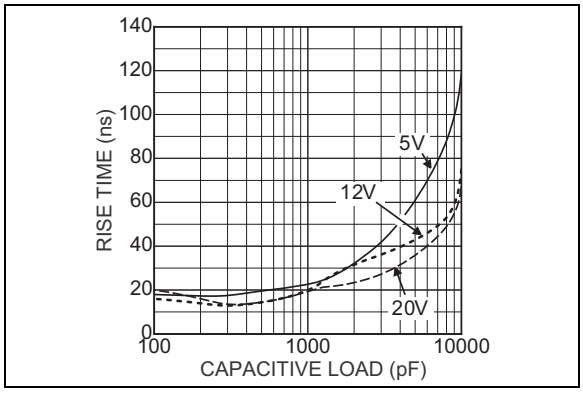

FIGURE 2-1: *Rise Time vs. Capacitive Load.*

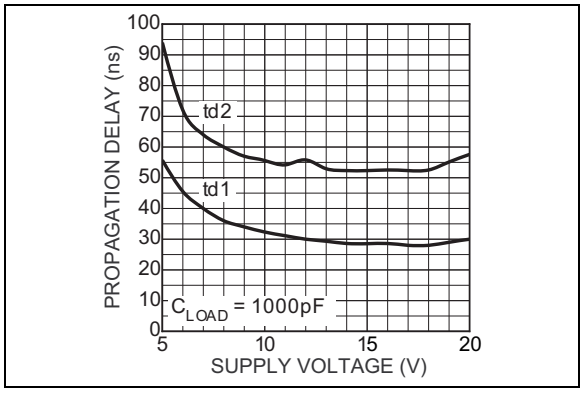

FIGURE 2-4: *Propagation Delay vs. Supply Voltage.*

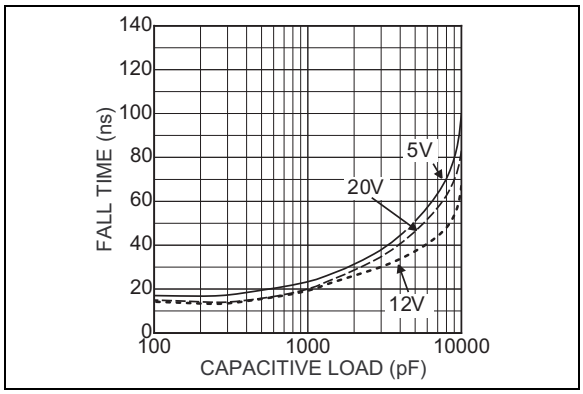

FIGURE 2-2: *Fall Time vs. Capacitive Load.*

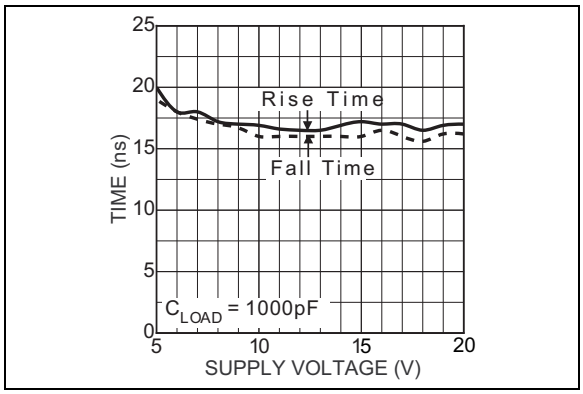

FIGURE 2-5: *Rise and Fall Time vs. Supply Voltage.*

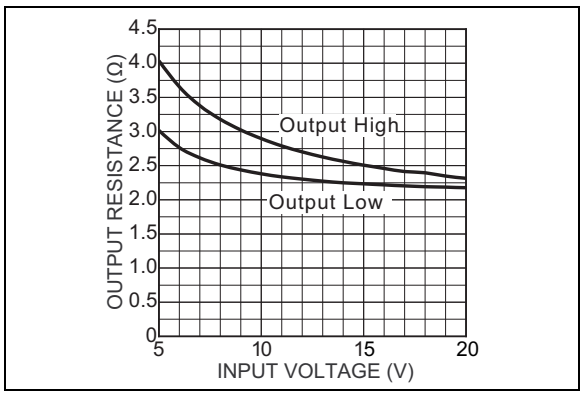

FIGURE 2-3: *Output Resistance vs. Supply Voltage.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
2, 4	INA, INB	Control Input
3	GND	Ground: Duplicate pins must be externally connected together
6	VS	Supply Input: Duplicate pins must be externally connected together
7, 5	OUTA, OUT B	Output: Duplicate pins must be externally connected together
1, 8	NC	Not connected
EP	GND	Ground: Backside Pad

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4.0 APPLICATION INFORMATION

Although the MIC4123/4/5 drivers have been specifically constructed to operate reliably under any practical circumstances, there are nonetheless details of usage that will provide better operation of the device.

4.1 Supply Bypassing

Charging and discharging large capacitive loads quickly requires large currents. For example, charging 2000 pF from 0 to 15 volts in 20 ns requires a constant current of 1.5A. In practice, the charging current is not constant and will usually peak at around 3A. In order to charge the capacitor, the driver must be capable of drawing this much current, this quickly, from the system power supply. In turn, this means that, as far as the driver is concerned, the system power supply, as seen by the driver, must have a very low impedance.

As a practical matter, this means that the power supply bus must be capacitively bypassed at the driver with at least 100 times the load capacitance in order to achieve optimum driving speed. It also implies that the bypassing capacitor must have very low internal inductance and resistance at all frequencies of interest. Generally, this means using two capacitors: one a high-performance low-ESR film, the other a low internal resistance ceramic. Together, the valleys in their two impedance curves allow adequate performance over a broad enough band to get the job done. Please note that many film capacitors can be sufficiently inductive as to be useless for this service. Likewise, many multilayer ceramic capacitors have unacceptably high internal resistance. Use capacitors intended for high pulse current service. The high pulse current demands of capacitive drivers also mean that the bypass capacitors must be mounted very close to the driver in order to prevent the effects of lead inductance or PCB land inductance from nullifying what you are trying to accomplish. For optimum results the sum of the lengths of the leads and the lands from the capacitor body to the driver body should total 2.5 cm or less.

Bypass capacitance, and its close mounting to the driver, serves two purposes. Not only does it allow optimum performance from the driver, it minimizes the amount of lead length radiating at high frequency during switching, (due to the large ΔI) thus minimizing the amount of EMI later available for system disruption and subsequent cleanup. It should also be noted that the actual frequency of the EMI produced by a driver is not the clock frequency at which it is driven, but is related to the highest rate of change of current produced during switching, a frequency generally one or two orders of magnitude higher, and thus more difficult to filter if you let it permeate your system. Good bypassing practice is essential to proper operation of high speed driver ICs.

4.2 Grounding

Both proper bypassing and proper grounding are necessary for optimum driver operation. Bypassing capacitance only allows a driver to turn the load on. Eventually, except in rare circumstances, it is also necessary to turn the load off. This requires attention to the ground path. Two things other than the driver affect the rate at which it is possible to turn a load off: the adequacy of the grounding available for the driver and the inductance of the leads from the driver to the load. The latter will be discussed in a separate section.

The SOIC and VDFN packages have an exposed pad under the package. It's important for good thermal performance that this pad is connected to a ground plane.

Best practice for a ground path is a well laid out ground plane. However, this is not always practical, and a poorly laid out ground plane can be worse than none. Attention to the paths taken by return currents even in a ground plane is essential. In general, the leads from the driver to its load, the driver to the power supply, and the driver to whatever is driving it should all be as low in resistance and inductance as possible. Of the three paths, the ground lead from the driver to the logic driving it is most sensitive to resistance or inductance, and ground current from the load is what is most likely to cause disruption. Thus, these ground paths should be arranged so that they never share a land, or do so for as short a distance as is practical.

To illustrate what can happen, consider the following: the inductance of a 2 cm long land, 1.59 mm (0.062") wide, on a PCB with no ground plane is approximately 45 nH. Assuming a dI/dt of 0.3 A/ns (which will allow a current of 3A to flow after 10 ns, and is thus slightly slow for our purposes) a voltage of 13.5V will develop along this land in response to our postulated ΔI. For a 1 cm land, (approximately 15 nH) 4.5V is developed. Either way, anyone using TTL-level input signals to the driver will find that the response of their driver has been seriously degraded by a common ground path for input to and output from the driver of the given dimensions. Note that this is before accounting for any resistive drops in the circuit. The resistive drop in a 1.59 mm (0.062") land of 2 oz. copper carrying 3A will be about 4 mV/cm (10 mV/in) at DC, and the resistance will increase with frequency as skin effect comes into play.

The problem is most obvious in inverting drivers where the input and output currents are in phase so that any attempt to raise the driver’s input voltage (in order to turn the driver’s load off) is countered by the voltage developed on the common ground path as the driver attempts to do what it was supposed to. It takes very little common ground path under these circumstances to alter circuit operation drastically.

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4.3 Output Lead Inductance

The same descriptions just given for PCB land inductance apply equally well for the output leads from a driver to its load, except that commonly the load is located much further away from the driver than the driver's ground bus.

Generally, the best way to treat the output lead inductance problem, when distances greater than 4 cm (2") are involved, requires treating the output leads as a transmission line. Unfortunately, as both the output impedance of the driver and the input impedance of the MOSFET gate are at least an order of magnitude lower than the impedance of common coax, using coax is seldom a cost-effective solution. A twisted pair works about as well, is generally lower in cost, and allows the use of a wider variety of connectors. The second wire of the twisted pair should carry common from as close as possible to the ground pin of the driver directly to the ground terminal of the load. Do not use a twisted pair where the second wire in the pair is the output of the other driver because this will not provide a complete current path for either driver. Likewise, do not use a twisted triad with two outputs and a common return unless both of the loads to be driver are mounted extremely close to each other and you can guarantee that they will never be switching at the same time.

For output leads on a printed circuit, the general rule is to make them as short and as wide as possible. The lands should also be treated as transmission lines: i.e., minimize sharp bends, or narrowings in the land because these will cause ringing. For a rough estimate on a 1.59 mm (0.062") thick G-10 PCB, a pair of opposing lands each 2.36 mm (0.093") wide translates to a characteristic impedance of about 50Ω. Half that width suffices on a 0.787 mm (0.031") thick board. For accurate impedance matching with a MIC4123/4/5 driver on a 1.59 mm (0.062") board, a land width of 42.75 mm (1.683") would be required, due to the low impedance of the driver and (usually) its load. This is impractical under most circumstances. Generally, the trade off point between lands and wires comes when lands narrower than 3.18 mm (0.125") would be required on a 1.59 mm (0.062") board.

To obtain minimum delay between the driver and the load, it is considered best to locate the driver as close as possible to the load using adequate bypassing. Using matching transformers at both ends of a piece of coax, or several matched lengths of coax between the driver and the load, works in theory, but is not optimal.

4.4 Driving at Controlled Rates

Occasionally there are situations where a controlled rise or fall time, which may be considerably longer than the normal rise or fall time of the driver's output, is desired for a load. In such cases, it is still prudent to employ the best possible practice in terms of bypassing, grounding, and PCB layout, then reduce the switching speed of the load, not the driver, by adding a non-inductive series resistor of an appropriate value between the output of the driver and the load. For situations where only rise or only fall should be slowed, the resistor can be paralleled with a fast diode so that switching in the other direction remains fast. Due to the Schmitt-trigger action of the driver's input, it is not possible to slow the rate of rise or fall of the driver's input signal to achieve slowing of the output.

4.5 Input Signal

The input stage of the MIC4123/4/5 consists of a single-MOSFET class A stage with an input capacitance of <8 pF. This capacitance represents the maximum load from the driver that will be seen by its controlling logic. The drain load on the input MOSFET is a –2 mA current source. Thus, the quiescent current drawn by the driver varies, depending upon the logic state of the input.

Following the input stage is a buffer stage that provides ~400 mV of hysteresis for the input to prevent oscillations when slowly changing input signals are used or when noise is present on the input. Input voltage switching threshold is approximately 1.5V, which makes the driver directly compatible with TTL signals or with CMOS powered from any supply voltage between 3V and 15V.

The MIC4123/4/5 drivers can also be driven directly by the MIC9130, MIC3808, MIC38C42, and similar switch mode power supply ICs. By relocating the main switch drive function into the driver rather than using the somewhat limited drive capabilities of a PWM IC. The PWM IC runs cooler, which generally improves its performance and longevity, and the main switches switch faster, which reduces switching losses and increase system efficiency.

The input protection circuitry of the MIC4123/4/5, in addition to providing 2 kV or more of ESD protection, also works to prevent latch up or logic upset due to ringing or voltage spiking on the logic input terminal. In most CMOS devices when the logic input rises above the power supply terminal, or descends below the ground terminal, the device can be destroyed or rendered inoperable until the power supply is cycled off and on. The MIC4123/4/5 drivers have been designed to prevent this. Input voltages excursions as great as 5V below ground will not alter the operation of the device. Input excursions above the power supply voltage will result in the excess voltage being conducted to the power supply terminal of the IC. Because the excess voltage is simply conducted to the power terminal, if the input to the driver is left in a high state when the power supply to the driver is turned off, currents as high as 30 mA can be conducted through the driver from the input terminal to its power supply terminal. This may overload the output of whatever is driving the driver, and may cause other devices that share the driver's power supply, as well as the driver, to

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operate when they are assumed to be off, but it will not harm the driver itself. Excessive input voltage will also slow the driver down, and result in much longer internal propagation delays within the drivers. t_{D2}, for example, may increase to several hundred nanoseconds. In general, while the driver will accept this sort of misuse without damage, proper termination of the line feeding the driver so that line spiking and ringing are minimized, will always result in faster and more reliable operation of the device, leave less EMI to be filtered elsewhere, be less stressful to other components in the circuit, and leave less chance of unintended modes of operation.

4.6 Power Dissipation

CMOS circuits usually permit the user to ignore power dissipation. Logic families such as 4000 series and 74Cxxx have outputs which can only source or sink a few milliamps of current, and even shorting the output of the device to ground or V_{CC} may not damage the device. CMOS drivers, on the other hand, are intended to source or sink several amps of current. This is necessary in order to drive large capacitive loads at frequencies into the megahertz range. Package power dissipation of driver ICs can easily be exceeded when driving large loads at high frequencies. Care must therefore be paid to device dissipation when operating in this domain. Operating frequency, power supply voltage, and load all affect power dissipation.

Given the power dissipation in the device and the thermal resistance of the package, junction operating temperature for any ambient is easy to calculate. For example, the thermal resistance of the 8-pin ePad SOIC package, from the data sheet, is 58°C/W. In a 25°C ambient, then, using a maximum junction temperature of 150°C, this package will dissipate 2.16W.

Accurate power dissipation numbers can be obtained by summing the three sources of power dissipation in the device:

- Load power dissipation (P_L)
- Quiescent power dissipation (P_Q)
- Transition power dissipation (P_T)

Calculation of load power dissipation differs depending upon whether the load is capacitive, resistive or inductive.

4.6.1 RESISTIVE LOAD POWER DISSIPATION

Dissipation caused by a resistive load can be calculated as:

EQUATION 4-1:

$$P_L = I^2 \times R_O \times D$$

Where:
I = The current drawn by the load.
R_O = The output resistance of the driver when the output is high, at the power supply voltage used.
D = Fraction of time the load is conducting (duty cycle).

4.6.2 CAPACITIVE LOAD POWER DISSIPATION

Dissipation caused by a capacitive load is simply the energy placed in, or removed from, the load capacitance by the driver. The energy stored in a capacitor is described by the equation:

EQUATION 4-2:

$$E = 1/2 \times C \times V^2$$

As this energy is lost in the driver each time the load is charged or discharged, for power dissipation calculations the 1/2 is removed. This equation also shows that it is good practice not to place more voltage in the capacitor than is necessary, as dissipation increases as the square of the voltage applied to the capacitor. For a driver with a capacitive load:

EQUATION 4-3:

$$P_L = f \times C \times V_S^2$$

Where:

f = Operating frequency.
C = Load capacitance.
V_S = Driver supply voltage.

4.6.3 INDUCTIVE LOAD POWER DISSIPATION

For inductive loads, the situation is more complicated. For the part of the cycle in which the driver is actively forcing current into the inductor, the situation is the same as it is in the resistive case:

EQUATION 4-4:

$$P_{L1} = I^2 \times R_O \times D$$

However, in this instance, the R_O required may be either the on resistance of the driver when its output is in the high state; or its on-resistance when the driver is in the low state, depending upon how the inductor is connected. For the part of the cycle when the inductor is forcing current through the driver, dissipation is best described as:

EQUATION 4-5:

$$P_{L2} = I \times V_D \times (1 - D)$$

Where:
V_D = The forward drop of the clamp diode in the driver (generally around 0.7V).

The two parts of the load dissipation must be summed in to produce P_L. Simply $P_{L1} + P_{L2} = P_L$.

4.6.4 QUIESCENT POWER DISSIPATION

Quiescent power dissipation (P_Q, as described in the input section) depends on whether the input is high or low. A low input will result in a maximum current drain (per driver) of ≤0.2 mA; a logic high will result in a current drain of ≤2.0 mA. Quiescent power can therefore be found from:

EQUATION 4-6:

$$P_Q = V_S \times (D \times I_H + (1 - D) \times I_L)$$

Where:

I_H	= Quiescent current with input high.
I_L	= Quiescent current with input low.
D	= Duty cycle.
V_S	= Power supply voltage.

4.6.5 TRANSITION POWER DISSIPATION

Transition power is dissipated in the driver each time its output changes state, because during the transition, for a very brief interval, both the N- and P-channel MOSFETs in the output totem-pole are ON simultaneously, and a current is conducted through them from V_S to ground. The transition power dissipation is approximately:

EQUATION 4-7:

$$P_T = f \times V_S \times (A \bullet s)$$

Where:
A•s = A time-current factor derived from Figure 4-1.

Total power (P_D) then, as previously described, is just:

EQUATION 4-8:

$$P_D = P_L + P_Q + P_T$$

Examples show the relative magnitude for each term.

Example 1:

A MIC4123 operating on a 12V supply driving two capacitive loads of 3000 pF each, operating at 250 kHz, with a duty cycle of 50%, in a maximum ambient of +60°C.

First calculate load power loss:

EQUATION 4-9:

$$P_L = f \times C \times {V_S}^2$$

$$P_L = 250,000 \times (3x10^{-9} + 3x10^{-9}) \times 12^2$$

$$P_L = 0.2160W$$

Then calculate transition power loss:

EQUATION 4-10:

$$P_T = f \times V_S \times (A \bullet s)$$

$$P_T = 250,000 \times 12 \times 2.2x10^{-9} = 6.6mW$$

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Then calculate quiescent power loss:

EQUATION 4-11:

$$P_Q = V_S \times (D \times I_H + (1 - D) \times I_L)$$

$$P_Q = 12 \times ((0.5 \times 0.0035) + (0.5 \times 0.0003))$$

$$P_Q = 0.0228W$$

Total power dissipation, then, is:

EQUATION 4-12:

$$P_D = 0.2160W + 0.0066W + 0.0228W = 0.2454W$$

Assuming an ePad SOIC package, with an θ_{JA} of 58°C/W, this will result in the junction running at:

EQUATION 4-13:

$$0.2454W \times 58°C/\text{W} = 14.2°C$$

14.2°C above ambient, given a maximum ambient temperature of 60°C, results in a maximum junction temperature of 89.4°C.

Example 2:

A MIC4124 operating on a 15V input, with one driver driving a 50Ω resistive load at 1 MHz, with a duty cycle of 67%, and the other driver quiescent, in a maximum ambient temperature of +40°C:

EQUATION 4-14:

$$P_L = I^2 \times R_O \times D$$

First, I_O must be determined.

EQUATION 4-15:

$$I_O = \frac{V_S}{R_O + R_{LOAD}}$$

Given R_O from the characteristic curves:

EQUATION 4-16:

$$I_O = \frac{15V}{3.3\Omega + 50\Omega} = 0.281A$$

EQUATION 4-17:

$$P_L = 0.281A^2 \times 3.3\Omega \times 0.67 = 0.174W$$

But, because only one side is operating:

EQUATION 4-18:

$$P_T = \frac{f \times V_S \times (A \bullet s)}{2}$$

$$P_T = \frac{1,000,000 \times 15 \times 3.3x10^{-9}}{2}$$

$$P_T = 0.025W$$

And then:

EQUATION 4-19:

$$P_Q = 15 + ((0.67 \times 0.00125) + (0.33 \times 0.000125) + (1 \times 0.000125))$$

$$P_Q = 0.015W$$

Now, this assumes that the unused side of the driver has its input grounded, which is more efficient.

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Then:

EQUATION 4-20:

$$P_D = 0.174 + 0.025 + 0.015 = 0.214W$$

In a VDFN with a θ_{JA} of 45°C/W, this amount of power results in a junction temperature given the maximum +40°C ambient of:

EQUATION 4-21:

$$(0.214W \times 45°C/\mathrm{W}) + 40°C = 49.6°C$$

The actual junction temperature will be lower than calculated both because the duty cycle is less than 100% and because the graph lists $R_{DS(ON)}$ at a T_J of 125°C and the $R_{DS(ON)}$ at 49.6°C T_J will be somewhat lower.

4.6.6 DEFINITIONS

C_L = Load Capacitance in Farads.

D = Duty Cycle expressed as the fraction of time the input to the driver is high.

f = Operating Frequency of the driver in Hertz.

I_H = Power supply current drawn by a driver when both inputs are high and neither output is loaded.

I_L = Power supply current drawn by a driver when both inputs are low and neither output is loaded.

I_D = Output current from a driver in Amps.

P_D = Total power dissipated in a driver in Watts.

P_L = Power dissipated in the driver due to the driver's load in Watts.

P_Q = Power dissipated in a quiescent driver in Watts.

P_T = Power dissipated in a driver when the output changes states ("shoot-through current") in Watts.

Note that the shoot-through current from a dual transition (once up, once down) for both drivers is stated in Figure 4-1 in amperenanoseconds. This figure must be multiplied by the number of repetitions per second (frequency to find Watts).

R_O = Output resistance of a driver in Ohms.

V_S = Power supply voltage to the IC in Volts.

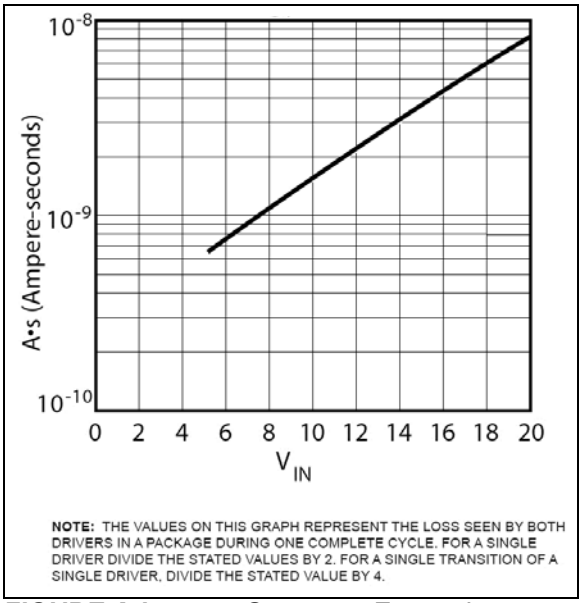

FIGURE 4-1: *Crossover Energy Loss.*

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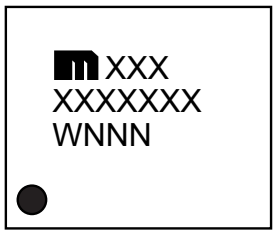
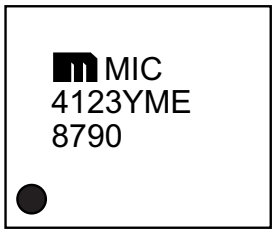
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

8-Lead SOIC*



Example



8-Lead VDFN*

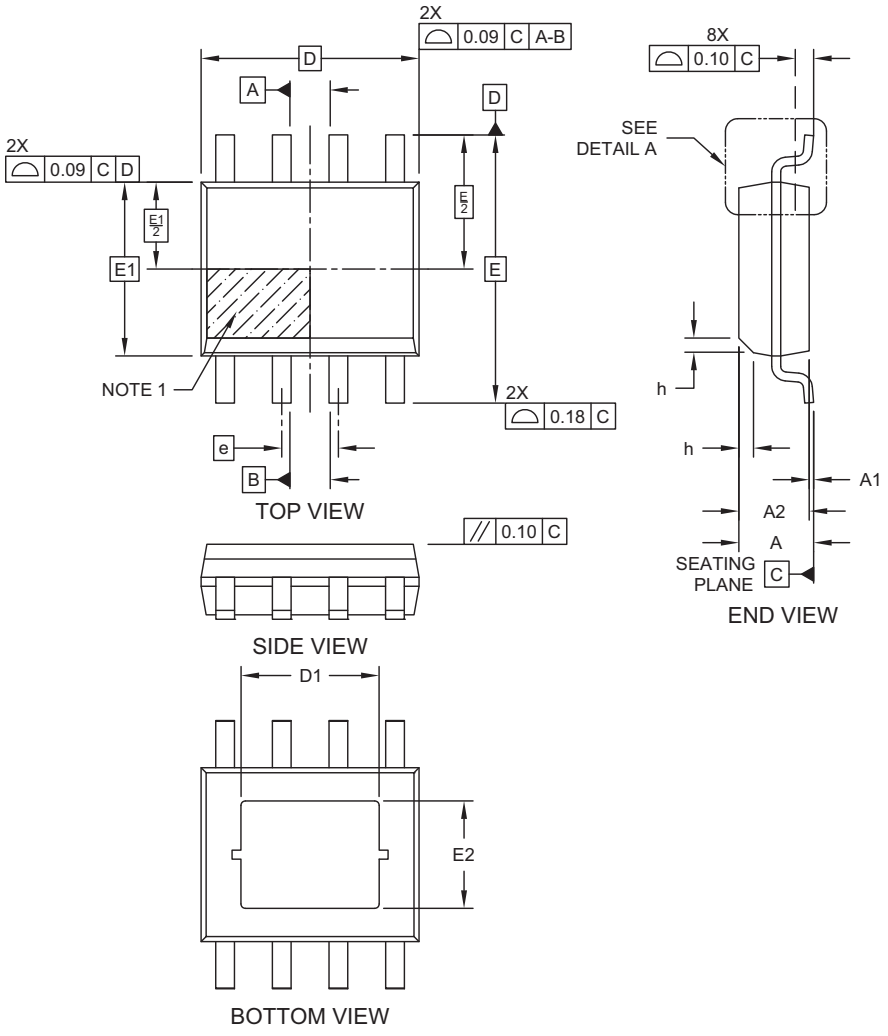
Example

Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

8-Lead SOICN ePad Package Outline & Recommended Land Pattern

8-Lead Small Outline Integrated Circuit Package (EQA) - 3.90 mm (1.50 In) Body [SOIC]
With 3.10x2.41 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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8-Lead Small Outline Integrated Circuit Package (EQA) - 3.90 mm (1.50 In) Body [SOIC] With 3.10x2.41 mm Exposed Pad

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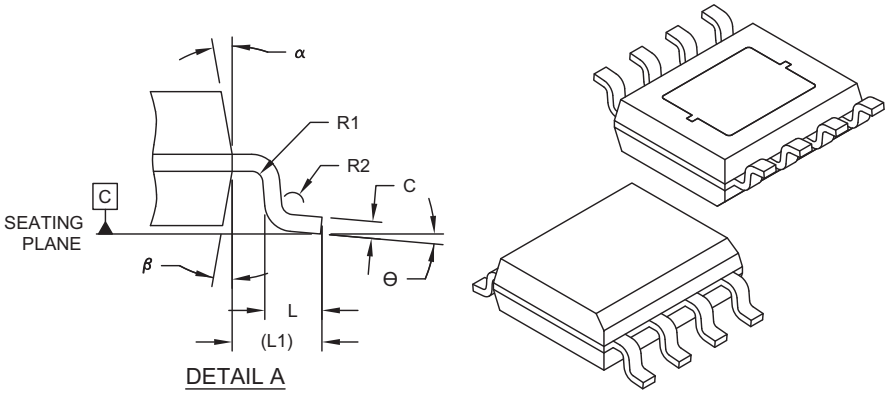

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	1.43	1.55	1.68
Standoff	A1	0.00	0.05	0.10
Molded Package Thickness	A2	1.25	-	-
Overall Length	D		4.89 BSC	
Exposed Pad Length	D1	-	3.10	-
Overall Width	E		6.02 BSC	
Molded Package Width	E1		3.90 BSC	
Exposed Pad Width	E2	-	2.41	-
Terminal Width	b	0.35	0.41	0.49
Lead Thickness	c	0.19	0.20	0.25
Terminal Length	L	0.41	0.64	0.89
Terminal-to-Exposed-Pad	L1		1.04 REF	
Foot Angle	Θ	0°	5°	8°
Lead Bend Radius	R1	0.07	-	-
Terminal Length	R2	0.07	-	-
Mold Draft Angle	α	5°	-	15°
Mold Draft Angle	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

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8-Lead Small Outline Integrated Circuit Package (EQA) - 3.90 mm (1.50 In) Body [SOIC] With 3.10x2.41 mm Exposed Pad

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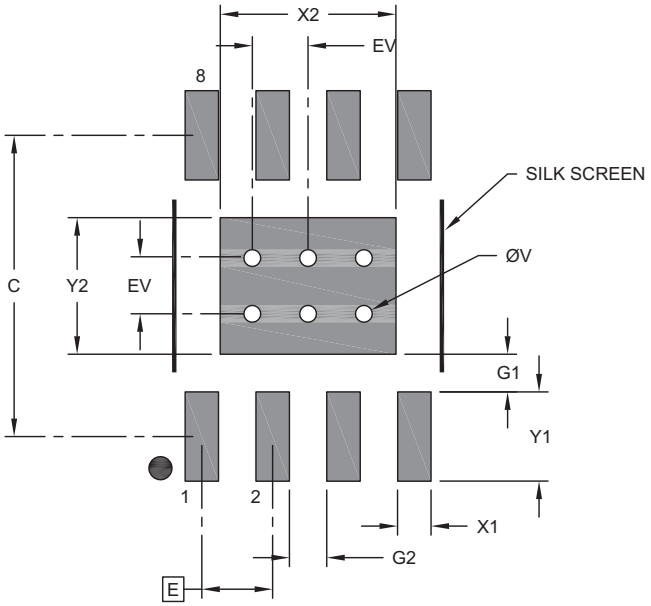

RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Optional Center Pad Width	X2			3.15
Optional Center Pad Length	Y2			2.45
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.60
Contact Pad to Center Pad (X8)	G1	0.68		
Contact Pad to Contact Pad (X6)	G2	0.67		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

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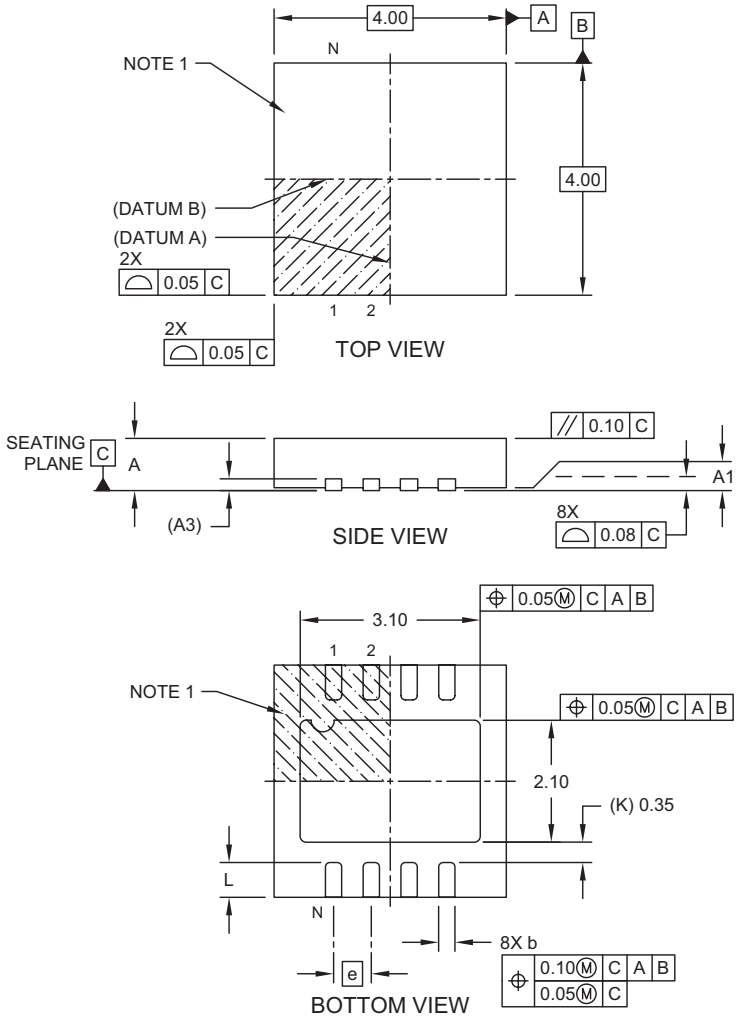
8-Lead 4 mm x 4 mm VDFN Package Outline and Recommended Land Pattern

8-Lead Very Thin Plastic Dual Flat, No Lead Package (JWA) - 4x4 mm Body [VDFN]
Saw Singulated with 3.1x2.1 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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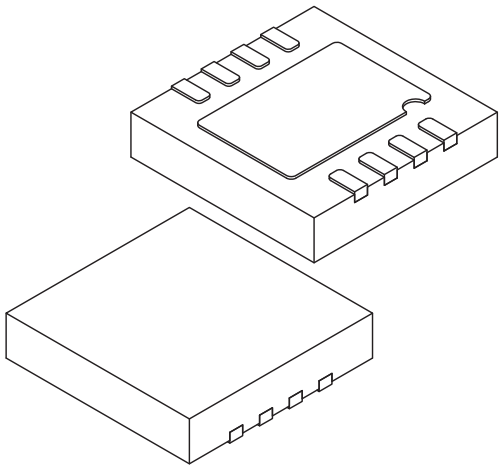
8-Lead Very Thin Plastic Dual Flat, No Lead Package (JWA) - 4x4 mm Body [VDFN]
Saw Singulated with 3.1x2.1 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	3.05	3.10	3.15
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.05	2.10	2.15
Terminal Width	b	0.23	0.28	0.33
Terminal Length	L	0.55	0.60	0.65
Terminal-to-Exposed-Pad	K		0.35 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
4. See Drawing C04-1248 for punch singulated version.

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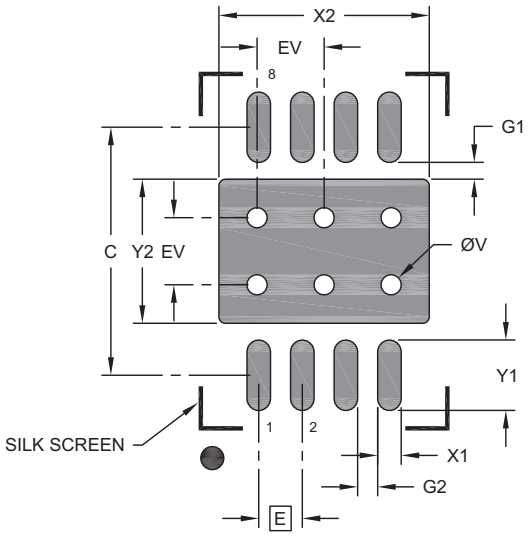
8-Lead Very Thin Plastic Dual Flat, No Lead Package (JWA) - 4x4 mm Body [VDFN]
Saw Singulated with 3.1x2.1 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	X2			3.14
Optional Center Pad Length	Y2			2.15
Contact Pad Spacing	C		3.70	
Contact Pad Width (X8)	X1			0.35
Contact Pad Length (X8)	Y1			1.05
Contact Pad to Center Pad (X8)	G1	0.25		
Contact Pad to Contact Pad (X6)	G2	0.30		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

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NOTES:

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APPENDIX A: REVISION HISTORY

Revision A (June 2018)

- Converted Micrel document MIC4123/4/5 to Microchip data sheet template DS20006035A.
- Minor grammatical text changes throughout.
- Updated Packaging Information to MCHP-standard versions.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Device	X	XX	-XX
Part No.	Junction Temp. Range	Package	Media Type

Device:	MIC4123:	Dual Inverting, Dual 3A-Peak Low-Side MOSFET Driver
	MIC4124:	Dual Non-Inverting, Dual 3A-Peak Low-Side MOSFET Driver
	MIC4125:	Inverting and Non-Inverting, Dual 3A-Peak Low-Side MOSFET Driver
Junction Temperature Range:	Y =	–40°C to +125°C, RoHS-Compliant
Package:	ME =	8-Lead ePad SOIC
	ML =	8-Lead 4 mm x 4 mm VDFN
Media Type:	<blank>=	95/Tube (SOIC only)
	TR =	2,500/Reel (SOIC only)
	TR =	5,000/Reel (VDFN only)

Examples:

a) MIC4123YME:	MIC4123, –40°C to +125°C Temperature Range, 8-Lead ePad SOIC, 95/Tube
b) MIC4124YML-TR:	MIC4124, –40°C to +125°C Temperature Range, 8-Lead VDFN, 5,000/Reel
c) MIC4125YME-TR:	MIC4125, –40°C to +125°C Temperature Range, 8-Lead ePad SOIC, 2,500/Reel
d) MIC4123YML-TR:	MIC4123, –40°C to +125°C Temperature Range, 8-Lead VDFN, 5,000/Reel
e) MIC4124YME:	MIC4124, –40°C to +125°C Temperature Range, 8-Lead ePad SOIC, 95/Tube
f) MIC4125YML-TR:	MIC4125, –40°C to +125°C Temperature Range, 8-Lead VDFN, 5,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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