THE DATASHEET OF

MIC2588-1YM-TR

MIC2588/MIC2594

Single-Channel, Negative High-Voltage Hot Swap Power Controllers

General Description

The MIC2588 and the MIC2594 are single-channel, negative-voltage hot swap controllers designed to address the need for safe insertion and removal of circuit boards into "live" high-voltage system backplanes, while using very few external components. The MIC2588 and the MIC2594 are each available in an 8-pin SOIC package and work in conjunction with an external N-Channel MOSFET for which the gate drive is controlled to provide inrush current limiting and output voltage slew-rate control. Overcurrent fault protection is also provided and includes a programmable overcurrent threshold. During an output overload condition, a constant-current regulation loop is engaged to ensure that the system power supply maintains regulation. If a fault condition exceeds a built-in 400µs nuisance-trip delay, the MIC2588 and the MIC2594 will latch the circuit breaker's output off and will remain in the off state until reset by cycling either the UV/OFF pin or the power to the IC. A master Power-Good signal is provided to indicate that the output voltage of the soft-start circuit is within its valid output range. This signal can be used to enable one or more DC-DC converter modules.

All support documentation can be found on Micrel's web site at www.micrel.com.

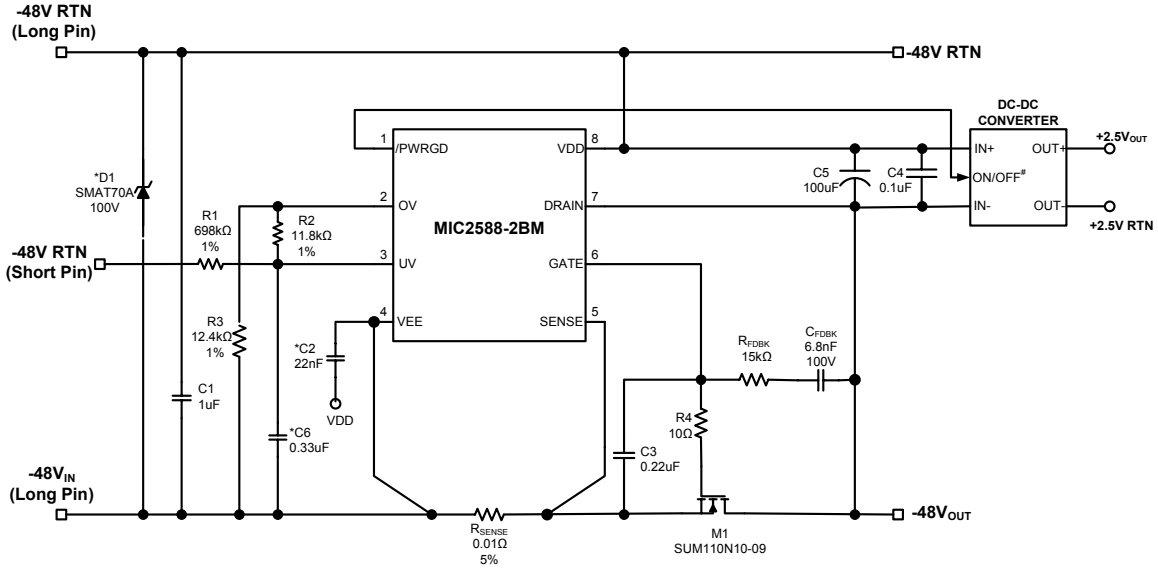
Features

- MIC2588:
  - Pin-for-pin functional equivalent to the LT1640/LT1640A/LT4250
- Provides safe insertion and removal from live –48V (nominal) backplanes
- Operates from –19V to –80V
- Electronic circuit breaker function
- Built-in 400µs "nuisance-trip" delay (t_{FLT})
- Regulated maximum output current into faults
- Programmable inrush current limiting
- Fast response to short circuit conditions (< 1µs)
- Programmable undervoltage and overvoltage lockouts (MIC2588-xBM)
- Programmable UVLO hysteresis (MIC2594-xBM)
- Fault reporting:
  - Active-HIGH (-1BM) and Active-LOW (-2BM) Power-Good output signal

Applications

- Central office switching
- –48V power distribution
- Distributed power systems
- Server Networks

Typical Application



Nominal Undervoltage and Overvoltage Thresholds:
V_{UV} = 36.5V
V_{OV} = 71.2V
* Optional components (See Applications Information for more details)
# An external pull-up resistor for the power-good signal is necessary for DC-DC supplies (and all other load modules) not equipped with internal pull-up impedence

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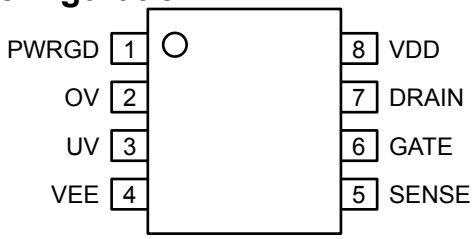
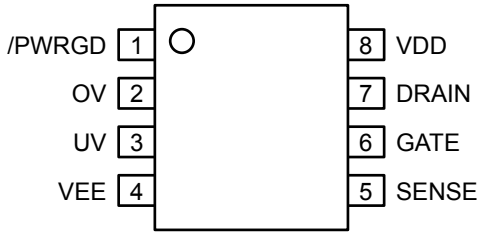
Ordering Information

Part Number		PWRGD Polarity	Lockout Functions	Circuit Breaker Function	Package
Standard	Pb-Free				
MIC2588-1BM	MIC2588-1YM	Active-High	Undervoltage and Overvoltage	Latched Off	8-pin SOIC
MIC2588-2BM	MIC2588-2YM	Active-Low	Undervoltage and Overvoltage	Latched Off	8-pin SOIC
MIC2594-1BM	MIC2594-1YM	Active-High	Programmable UVLO Hysteresis	Latched Off	8-pin SOIC
MIC2594-2BM	MIC2594-2YM	Active-Low	Programmable UVLO Hysteresis	Latched Off	8-pin SOIC

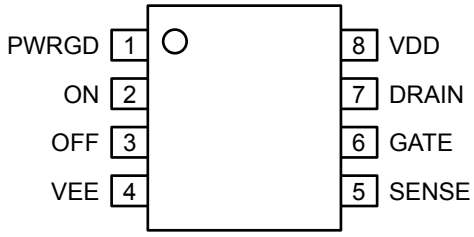
Pin Configuration



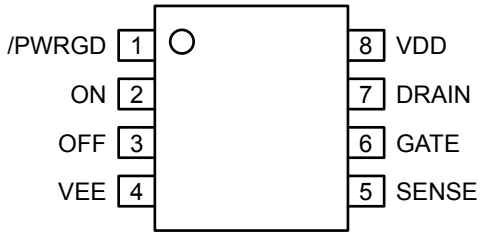
8-Pin SOIC (M)
MIC2588-1BM



8-Pin SOIC (M)
MIC2588-2BM



8-Pin SOIC (M)
MIC2594-1BM



8-Pin SOIC (M)
MIC2594-2BM

Pin Description

Pin Number	Pin Name	Pin Function
1	PWRGD /PWRGD	Power-Good Output: Open-drain. Asserted when the voltage on the DRAIN pin (V_{DRAIN}) is within V_{PGTH} of VEE, indicating that the output voltage is within proper specifications.
1	MIC25XX-1 PWRGD Active-High	MIC2588-1 and MIC2594-1: PWRGD will be high-impedance when V_{DRAIN} is less than V_{PGTH}, and will pull-down to V_{DRAIN} when V_{DRAIN} is greater than V_{PGTH}. Asserted State: Open-Drain.
1	MIC25XX-2 /PWRGD Active-Low	MIC2588-2 and MIC2594-2: /PWRGD will pull-down to V_{DRAIN} when V_{DRAIN} is less than $V_{PGTH,}$ and will be high impedance when V_{DRAIN} is greater than V_{PGTH}. Asserted State: Active-Low.
2	OV Threshold	MIC2588: Overvoltage Threshold Input. When the voltage at the OV pin is greater than the V_{OVH} threshold, the GATE pin is immediately pulled low by an internal 100µA current pull-down.
2	ON Turn-On Threshold	MIC2594: Turn-On Threshold. At initial system power-up or after the device has been shut off by the OFF pin, the voltage on the ON pin must exceed the V_{ONH} threshold in order for the MIC2594 to be enabled.
3	UV Threshold	MIC2588: Undervoltage Threshold Input. When the voltage at the UV pin is less than the V_{UVL} threshold, the GATE pin is immediately pulled low by an internal 100µA current pull-down. The UV pin is also used to cycle the device off and on to reset the circuit breaker. Taken together, the OV and UV pins form a window comparator which defines the limits of V_{EE} within which the load may safely be powered.
3	OFF Turn-Off Threshold	MIC2594: Turn-Off Threshold. When the voltage at the OFF pin is less than the V_{OFFL} threshold, the GATE pin is immediately pulled low by an internal 100µA current pull-down. The OFF pin is also used to cycle the device off and on to reset the circuit breaker. Taken together, the ON and OFF pins provide programmable hysteresis for the turn-on command voltage.
4	VEE	Negative Supply Voltage Input. Connect to the negative, or low side, terminal of the input power supply.
5	SENSE	Circuit Breaker Sense Input: The current-limit threshold is set by connecting a resistor between this pin and V_{EE}. When the current-limit threshold of IR = 50mV is exceeded for an internal delay t_{FLT} (400µs), the circuit breaker is tripped and the GATE pin is immediately pulled low by $I_{GATEOFF}$. Toggling the UV/OFF pin will reset the circuit breaker. To disable the circuit breaker, externally connect SENSE and VEE together.
6	GATE	Gate Drive Output: Connect to the gate of an external N-Channel MOSFET.
7	DRAIN	Drain Sense Input: Connect to the drain of an external N-Channel MOSFET.
8	VDD	Positive Supply Input. Connect to the positive, or high side, terminal of the input power supply.

Absolute Maximum Ratings[1]

(All voltages are referred to V_{EE})

Supply Voltage (V_{DD}–V_{EE}) .....–0.3V to 100V
DRAIN, PWRGD pins.....–0.3V to 100V
GATE pin .....–0.3V to 12.5V
SENSE, OV, UV, ON, OFF pins.....–0.3V to 6V
Lead Temperature (soldering)
Standard package (-xBM)
(IR Reflow, Peak Temperature)..... 240°C +0°C/–5°C
Pb-Free Package-(xYM)
(IR Reflow, Peak Temperature)..... 260°C +0°C/–5°C
ESD Ratings[3]
Human Body Model 2kV
Machine Model 100V

Operating Ratings[2]

Supply Voltage (V_{DD}–V_{EE}) ..... +19V to +80V
Ambient Temperature Range (T_A) ..... –40°C to 85°C
Junction Temperature (T_J)..... 125°C
Package Thermal Resistance
SOIC (θ_{JA}) ..... 152°C/W

DC Electrical Characteristics[4]

V_{DD} = 48V, V_{EE} = 0V, T_A = 25°C, unless otherwise noted. **Bold** indicates specifications apply over the full operating temperature range of –40°C to +85°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{DD} – V_{EE}$	Supply Voltage		**19**		**80**	V
I_{DD}	Supply Current			3	**5**	mA
V_{TRIP}	Circuit Breaker Trip Voltage	$V_{TRIP} = V_{SENSE} – V_{EE}$	**40**	50	**60**	mV
I_{GATEON}	GATE Pin Pull-up Current	$V_{GATE} = V_{EE}$ to 8V 19V ≤ ($V_{DD} – V_{EE}$) ≤ 80V	**30**	45	**60**	µA
$I_{GATEOFF}$	GATE Pin Sink Current	($V_{SENSE} – V_{EE}$) = 100mV V_{GATE} = 2V	100	230		mA
V_{GATE}	GATE Drive Voltage, ($V_{GATE} – V_{EE}$)	15V ≤ ($V_{DD} – V_{EE}$) ≤ 80V	**9**	10	**11**	V
I_{SENSE}	SENSE Pin Current	V_{SENSE} = 50mV		0.2		µA
V_{UVH}	UV Pin High Threshold Voltage	Low-to-High transition	**1.213**	1.243	**1.272**	V
V_{UVL}	UV Pin Low Threshold Voltage	High-to-Low transition	**1.198**	1.223	**1.247**	V
V_{UVHYS}	UV Pin Hysteresis			20		mV
V_{OVH}	OV Pin High Threshold Voltage	Low-to-High transition	**1.198**	1.223	**1.247**	V
V_{OVL}	OV Pin Low Threshold Voltage	High-to-Low transition	**1.165**	1.203	**1.232**	V
V_{OVHYS}	OV Pin Hysteresis			20		mV
V_{ONH}	ANSI ON Pin High Threshold Voltage	Low-to-High transition	**1.198**	1.223	**1.247**	V
V_{OFFH}	ANSI OFF Pin Low Threshold Voltage	High-to-Low transition	**1.198**	1.223	**1.247**	V
I_{CNTRL}	Input Bias Current (OV, UV, ON, OFF Pins)	V_{UV} = 1.25V			**0.5**	µA
V_{PGTH}	Power-Good Threshold	High-to-Low transition ($V_{DRAIN} – V_{EE}$)	**1.1**	1.26	**1.40**	V
V_{OLPG}	PWRGD Output Voltage (relative to voltage at the DRAIN pin)	$V_{OLPG} – V_{DRAIN}$ 0mA ≤ $I_{PG(LOW)}$ ≤ 1mA				
	MIC25XX-1	($V_{DRAIN} – V_{EE}$) < V_{PGTH}	**–0.25**		**0.8**	V
	MIC25XX-2	($V_{DRAIN} – V_{EE}$) > V_{PGTH}	**–0.25**		**0.8**	V
$I_{LKG(PG)}$	PWRGD Output Leakage Current	$V_{PWRGD} = V_{DD}$ = 80V			**1**	µA

Notes:

1. Exceeding the “Absolute Maximum Ratings” may damage the devices.
2. The devices are not guaranteed to function outside the specified operating conditions.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model: 1.5kΩ in series with 100pF. Machine model: 200pF, no series resistance.
4. Specification for packaged product only.

AC Electrical Characteristics[5]

Symbol	Parameter	Condition	Min	Typ	Max	Units
t_{FLT}	Built-in Overcurrent Nuisance Trip Time Delay[6] (Figure 1)			400		µs
$t_{OCSENSE}$	Overcurrent Sense to GATE Low (Figure 2)	$V_{SENSE} - V_{EE}$ = 100mV			3.5	µs
t_{OVPHL}	OV to GATE Low[6] (Figure 3)			1		µs
t_{OVPLH}	OV to GATE High[6] (Figure 3)			1		µs
t_{UVPHL}	UV to GATE Low[6] (Figure 4)			1		µs
t_{UVPLH}	UV to GATE High[6] (Figure 4)			1		µs
$t_{PGL(1)}$	DRAIN High to PWRGD Output Low[6] (-1 Version parts only)	R_{PULLUP} = 100kΩ, C_{LOAD} on PWRGD = 50pF		1		µs
$t_{PGL(2)}$	DRAIN Low to /PWRGD Output Low[6] (-2 Version parts only)	R_{PULLUP} = 100kΩ, C_{LOAD} on /PWRGD = 50pF		1		µs
$t_{PGH(1)}$	DRAIN Low to PWRGD Output High[6] (-1 Version parts only)	R_{PULLUP} = 100kΩ, C_{LOAD} on PWRGD = 50pF		2		µs
$t_{PGH(2)}$	DRAIN High to /PWRGD Output High[6] (-2 Version parts only)	R_{PULLUP} = 100kΩ, C_{LOAD} on /PWRGD = 50pF		2		µs

Notes:

5. Specification for packaged product only.
6. Not 100% production tested. Parameters are guaranteed by design.

Timing Diagrams

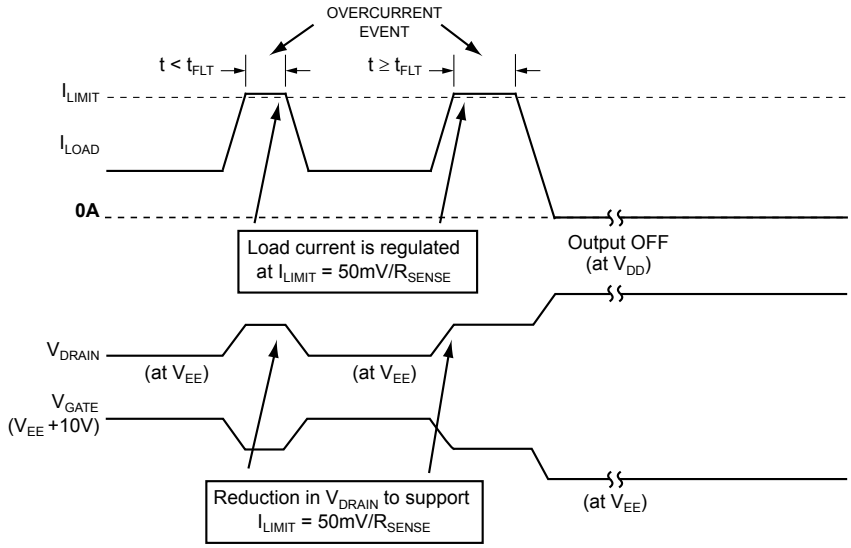


Figure 1. Overcurrent Response

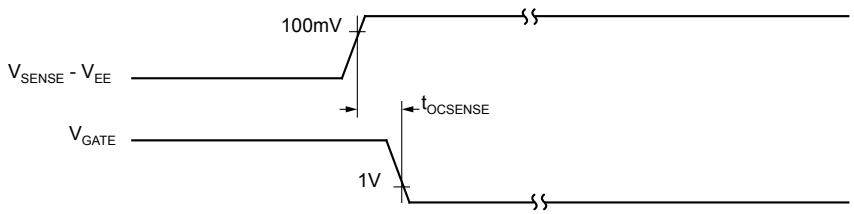


Figure 2. SENSE to GATE LOW Timing Response

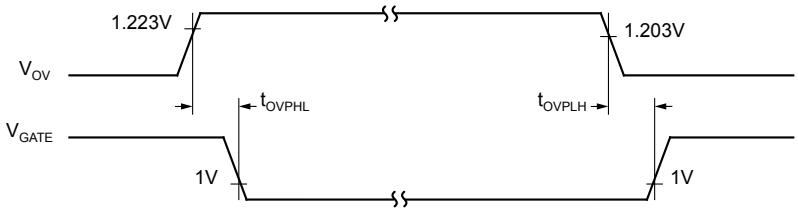


Figure 3. Overvoltage Response

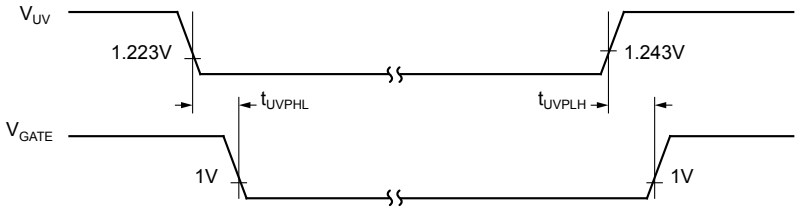


Figure 4. Undervoltage Response

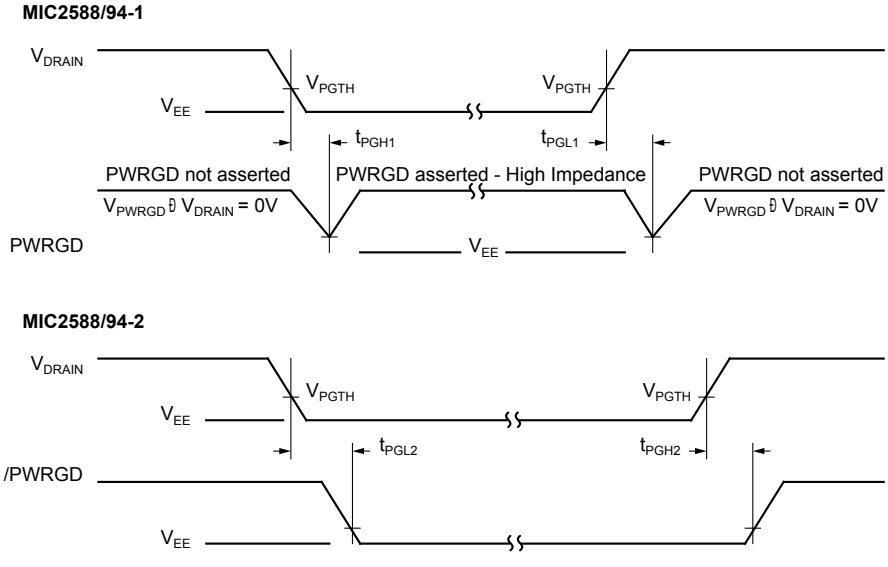
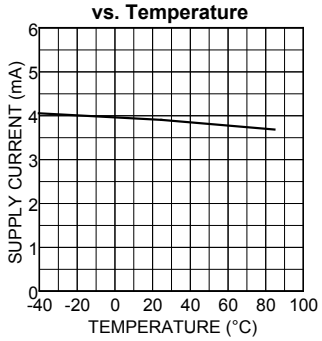


Figure 5. DRAIN to Power-Good Response

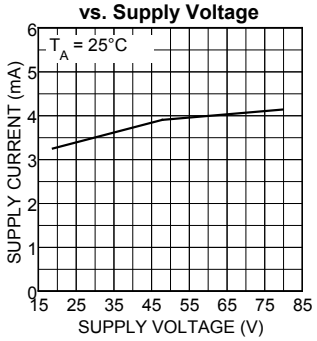
Typical Characteristics

[Section under construction]

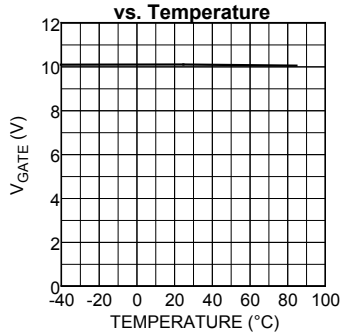
Supply Current vs. Temperature



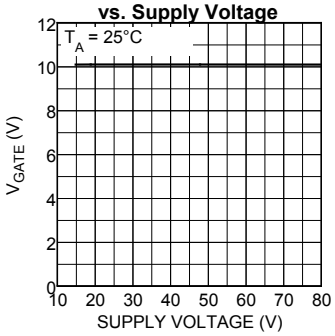
Supply Current vs. Supply Voltage



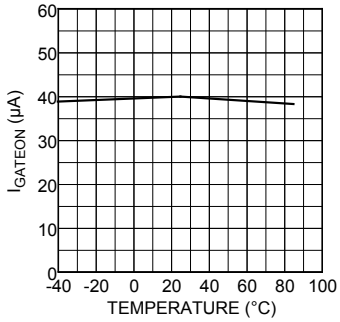
GATE Drive (V_{GATE} - V_{EE}) vs. Temperature



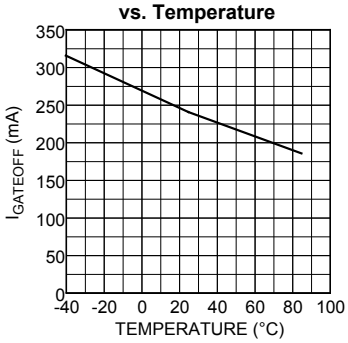
GATE Drive (V_{GATE} - V_{EE}) vs. Supply Voltage



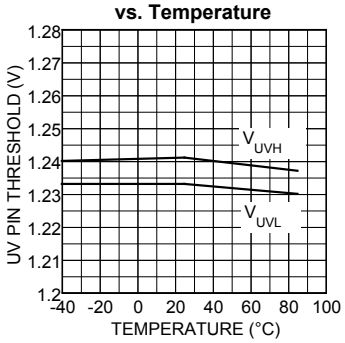
GATE Pull-Up Current vs. Temperature



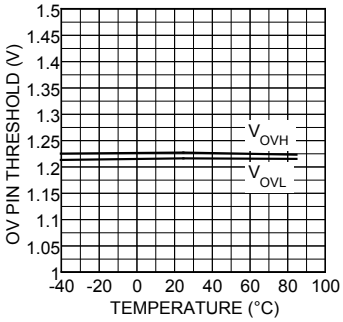
GATE Sink Current vs. Temperature



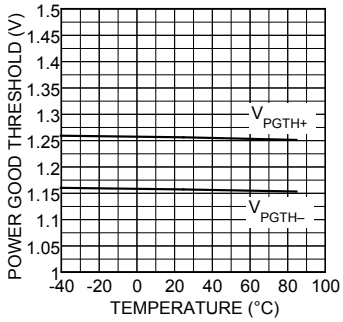
UV Pin Threshold vs. Temperature



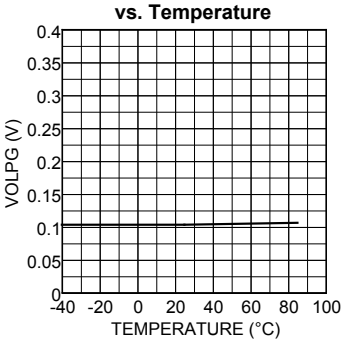
OV Pin Threshold vs. Temperature



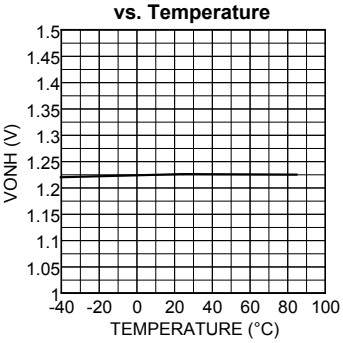
Power Good Threshold vs. Temperature



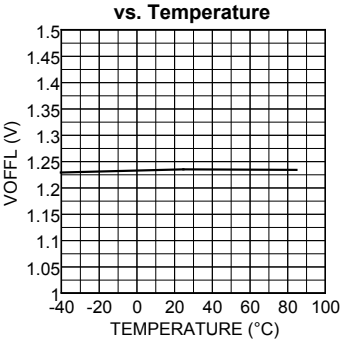
Power-Good Low Voltage vs. Temperature

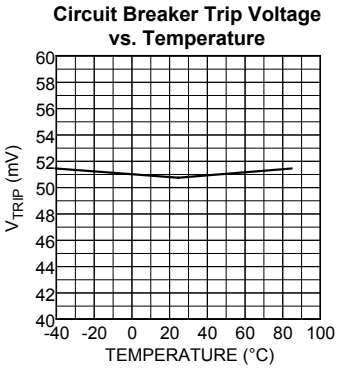


ON Pin Threshold vs. Temperature

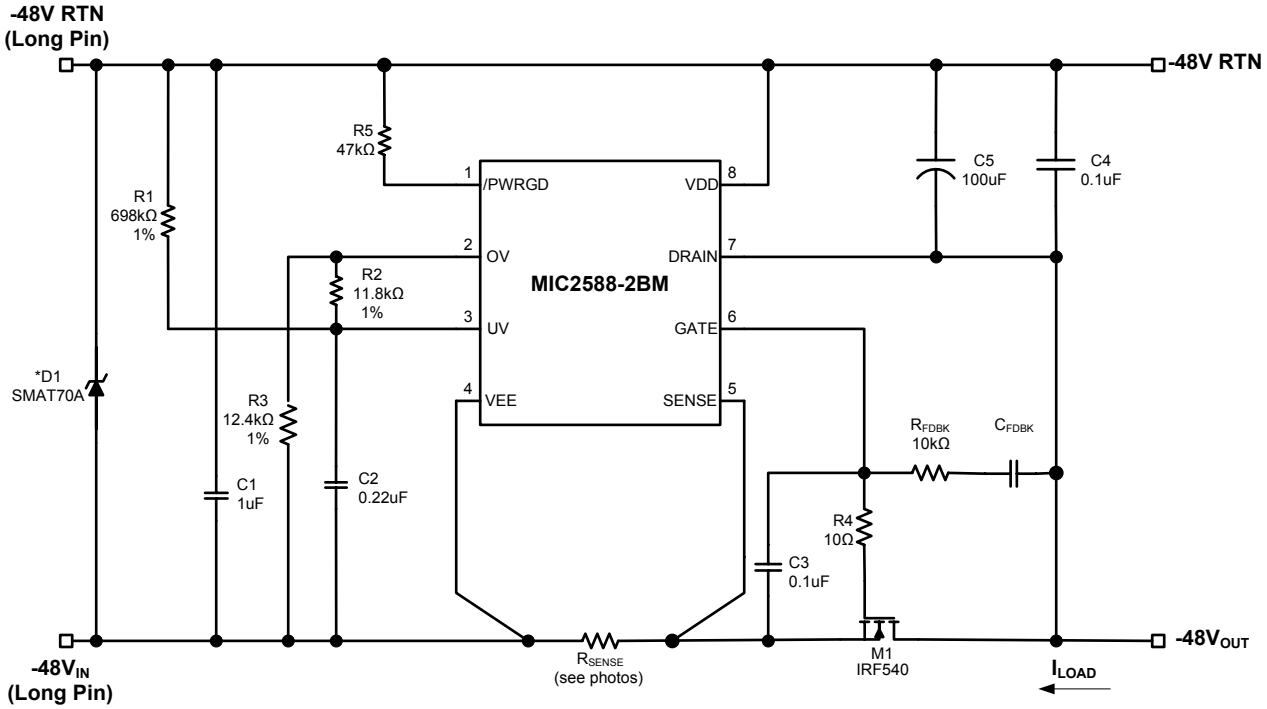


OFF Pin Threshold vs. Temperature





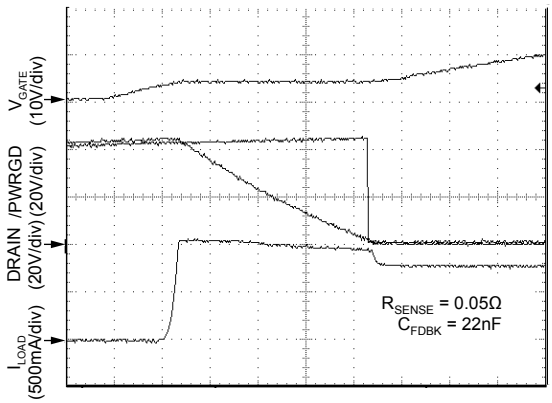
Test Circuit



MIC2588/MIC2594 Test Circuit

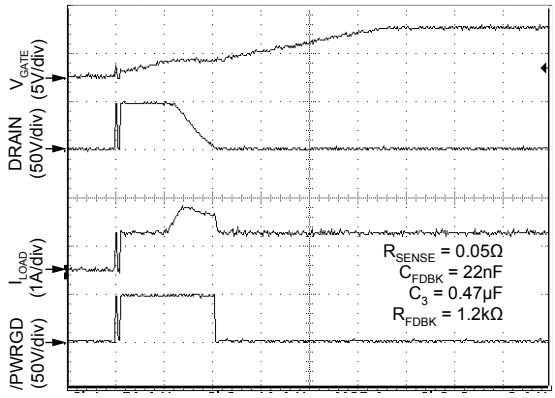
Functional Characteristics

Turn-On Response



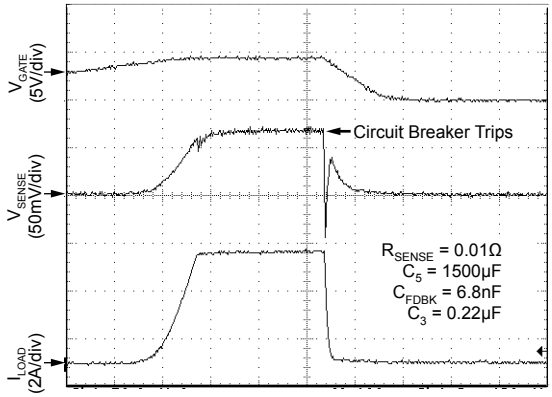
TIME (5ms/div.)

Hot-Plug Turn-On Response



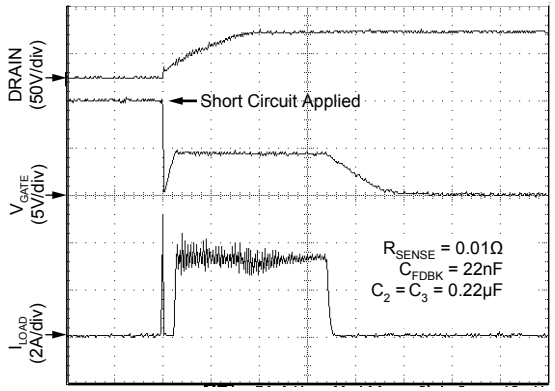
TIME (25ms/div.)

Turn-On (Circuit Breaker Trip) Into Large C_{LOAD}



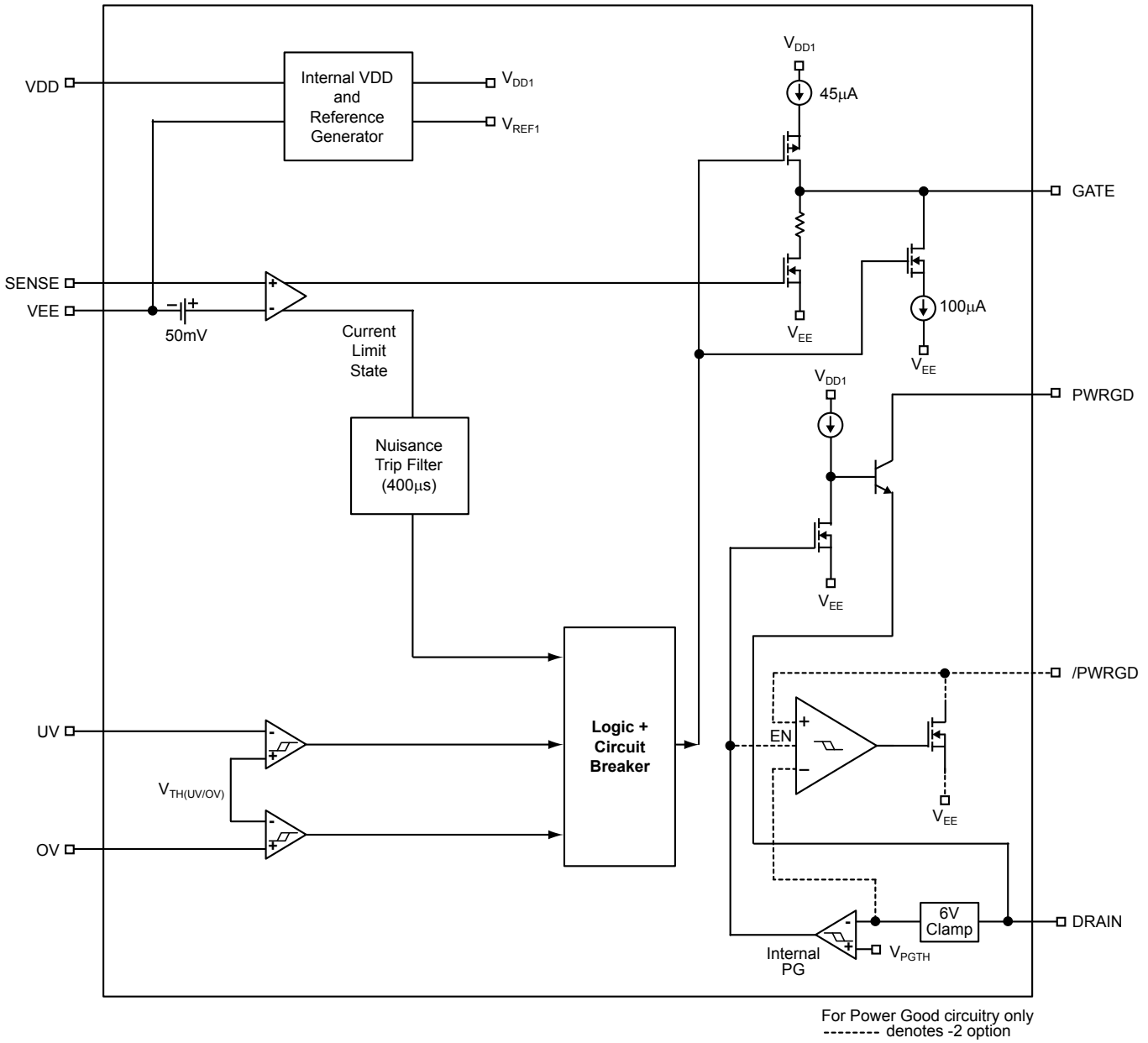
TIME (100µs/div.)

Overcurrent Response (Short Circuit)



TIME (100µs/div.)

Functional Diagram



MIC2588 Block Diagram

Functional Description

Hot Swap Insertion

When circuit boards are inserted into systems carrying live supply voltages ("hot swapped"), high inrush currents often result due to the charging of bulk capacitance that resides across the circuit board's supply pins. These current spikes can cause the system's supply voltages to temporarily go out of regulation, causing data loss or system lock-up. In more extreme cases, the transients occurring during a hot swap event may cause permanent damage to connectors or on-board components.

The MIC2588 and the MIC2594 are designed to address these issues by limiting the magnitude of the transient or inrush current during hot swap events. This is achieved by controlling the rate at which power is applied to the circuit board (di/dt and dv/dt management). Additionally, the MIC2588 and the MIC2594 incorporate input voltage supervisory functions and current limiting, thereby providing robust protection for both the system and the circuit board.

Start-Up Cycle

When the input voltage to the controller is between the overvoltage and undervoltage thresholds (MIC2588) or is greater than V_{ON} (MIC2594), a start cycle is initiated to deliver power to the load. At this time, the GATE pin of the controller applies a constant charging current (I_{GATEON}) to the gate of the external MOSFET (M1). C_{FDBK} creates a Miller integrator out of the MOSFET circuit, which limits the slew-rate of the voltage at the drain of M1. The drain voltage rate-of-change (dv/dt) of M1 is:

$$\frac{dv(M1_{DRAIN})}{dt} = \left(\frac{I_{GATE(-)}}{C_{FDBK}}\right) = -\left(\frac{I_{GATEON}}{C_{FDBK}}\right)$$

where $I_{GATE(+)}$ = Gate Charging Current = I_{GATEON};
$I_{GATE(-)} \cong -I_{GATE(+)}$, due to the extremely high transconductance values of power MOSFETs; and

$$I_{GATE(-)} = C_{FDBK} \times \frac{dv(M1_{DRAIN})}{dt}$$

Relating the above to the maximum transient (or inrush) current charging the load capacitance upon hot swap or power-up involves an extension of the same formula:

$$I_{INRUSH} = \frac{C_{LOAD} \times dv(M1_{DRAIN})}{dt}$$

$$I_{INRUSH} = C_{LOAD} \times -\left(\frac{I_{GATEON}}{C_{FDBK}}\right)$$

$$| I_{INRUSH} | = \frac{C_{LOAD}}{C_{FDBK}} \times I_{GATEON} \qquad (1)$$

The presence of C3 and R_{FDBK} prevent turn-on of the external pass device by limiting the hot swap current surges induced by AC coupled transients from the drain to the gate of M1 (i.e., $C_{FDBK} + C_{GD}(M1)$). An appropriate value for C3 may be determined using the formula for a capacitive voltage divider.

The maximum voltage on C3 at turn-on must be less than $V_{THRESHOLD}$ of M1.

1. For a standard 10V enhancement N-Channel MOSFET, $V_{THRESHOLD}$ is about 4.25V.
2. Choose 2V as the maximum voltage to avoid turn-on transients.

$$V_{GS}(M1) \times [C3 + (C_{FDBK} + C_{GD}(M1))] = V_{IN}(max) \times (C_{FDBK} + C_{GD}(M1))$$

$$V_{GS}(M1) \times C3 = (V_{IN}(max) - V_{GS}(M1))(C_{FDBK} + C_{GD}(M1))$$

$$C3 = (C_{FDBK} + C_{GD}(M1)) \times \frac{V_{IN}(max) - V_{GS}(M1)}{V_{GS}(M1)} \qquad (2)$$

where $V_{IN}(max) = V_{DD} - V_{EE}(min)$.

For example, we can determine appropriate capacitor values given a hot swap controller that is required to maintain the inrush current into a 220µF load capacitance at 2A maximum and an input supply voltage as high as $V_{IN}(max)$ = 75V. One of the suggested MOSFETs to be used with the MIC2588/MIC2594 is an SUM110N10-09,a 100V D^2PAK device which has a typical C_{GD} of 750pF.

Calculating a value for C_{FBDK} using Equation 1 yields:

$$C_{FDBK} = \frac{220\mu F \times 45\mu A}{2A} = 4.95nF$$

Good engineering practice suggests the use of the worst-case parameter values for I_{GATEON} from the "DC Electrical Characteristics" section:

$$C_{FDBK} = \frac{220\mu F \times 60\mu A}{2A} = 6.6nF$$

where the nearest standard 5% value is 6.8nF. Substituting 6.8nF into Equation 2 from above yields:

$$C3 = (6.8nF + 750pF) \times \frac{(75V - 2V)}{2V} = 0.275\mu F$$

For C3, the nearest standard 5% value is 0.22µF.

While the value for R_{FDBK} is not critical, it should be chosen to allow a maximum of a few milliamperes to flow in the gate-drain circuit of M1 during turn-on. While the final value for R_{FDBK} is determined empirically, initial values between R_{FDBK} = 15kΩ to 27kΩ for systems with a maximum value of $V_{IN}(max)$ = 75V are appropriate.

Resistor R4, in series with the MOSFET's gate, minimizes the potential for parasitic high frequency oscillations from occurring in M1. While the exact value of R4 is not critical, commonly used values for R4 range from 10Ω to 33Ω.

Power-Good (PWRGD or /PWRGD) Output

For the MIC2588-1 and the MIC2594-1, the Power-Good output signal (PWRGD) will be high impedance when V_{DRAIN} drops below V_{PGTH}, and will pull down to V_{DRAIN} when V_{DRAIN} is above V_{PGTH}. For the MIC2588-2 and the MIC2594-2, /PWRGD will pull down to the potential of the V_{DRAIN} pin when V_{DRAIN} drops below V_{PGTH}, and will be high impedance when V_{DRAIN} is above V_{PGTH}. Hence, the -1 parts have an active-high PWRGD signal and the -2 parts have an active-low /PWRGD output. Either PWRGD or /PWRGD may be used as an enable signal for one or more

subsequent DC/DC converter modules or for other system uses as desired. When used as an enable signal, the time necessary for the PWRGD (or /PWRGD) signal to pull-up (when in high impedance state) will depend upon the load (RC) that is present on this output.

Circuit Breaker Function

The MIC2588 and the MIC2594 employ an electronic circuit breaker that protects the MOSFET and other system components against faults such as short circuits. The current limit threshold is set via an external resistor, R_{SENSE}, connected between the V_{EE} and SENSE pins and is determined by:

$$I_{LIM} = \frac{V_{TRIP}}{R_{SENSE}} \quad (3)$$

where V_{TRIP} is the circuit breaker trip threshold specified in the Electrical Characteristics Table.

An internal 400µs timer limits the length of time (t_{FLT}) for which the circuit can draw current in excess of its programmed threshold before the circuit breaker is tripped. This short delay prevents nuisance tripping of the circuit breaker due to system transients while providing rapid protection against large-scale transient faults. Whenever the voltage across R_{SENSE} exceeds 50mV, two things happen:

1. A constant-current regulation loop is engaged and is designed to hold the voltage across R_{SENSE} equal to 50mV. This protects both the load and the MIC2588 circuit from excessively high currents. This loop will engage in less than 1µs from the time at which the overvoltage condition on R_{SENSE} occurs.
2. The internal 400µs timer is started. If the 400µs timeout period expires, the circuit breaker trips and the GATE pin is immediately pulled low by an internal current pull-down. This operation turns off the MOSFET quickly and disconnects the input from the load.

Undervoltage/Overvoltage Detection—MIC2588

The MIC2588 has "UV" and "OV" input pins. These pins can be used to detect input supply rail undervoltage and overvoltage conditions. Undervoltage lockout prevents energizing the load until the supply input is stable and within tolerance. In a similar fashion, overvoltage turn-off prevents damage to sensitive circuit components should the input voltage exceed normal operational limits. Each of these pins is internally connected to an analog comparator with 20mV of hysteresis. When the UV pin falls below its V_{UVL} threshold or the OV pin is above its V_{OVH} threshold, the GATE pin is immediately pulled low. The GATE pin will be held low until UV exceeds its V_{UVH} threshold or OV drops below its V_{OVL} threshold. The UV and OV circuits' threshold trip points are programmed using the resistor divider R1, R2, and R3 as shown in the "Typical Application." The equations to set the trip points are shown below. For the following example, the circuit's nominal UV threshold is set to V_{UV} = 37V and the nominal OV threshold is placed at V_{OV} = 72V, values commonly used in Central Office power distribution applications.

$$V_{UV} = V_{UVL}(typ) \times \frac{(R1+R2+R3)}{(R2+R3)} \quad (4)$$

$$V_{OV} = V_{OVH}(typ) \times \frac{(R1+R2+R3)}{R3} \quad (5)$$

Given V_{UV}, V_{OV}, and any one resistor value, the remaining two resistor values can be found. A suggested value for R3 is that which will provide a minimum of 100µA of current through the voltage divider chain at $V_{DD} = V_{UV}$. This yields the following as a starting point:

$$R3 = \frac{V_{OVH}(typ)}{100\mu A} = 12.23k\Omega$$

The closest standard 1% value for R3 = 12.4kΩ. Using Equations 3 and 4 above, solving for R2 and R1 yields:

$$R2 = R3 \times \left[\left(\frac{V_{OV}}{V_{UV}}\right) - 1\right]$$

$$R2 = 12.4k\Omega \times \left[\left(\frac{72V}{37V}\right) - 1\right]$$

$$R2 = 11.729k\Omega$$

The closest standard 1% value for R2 = 11.8kΩ. Next, the value for R1 is calculated:

$$R1 = R3 \times \left(\frac{V_{OV} - 1.223V}{1.223V}\right) - R2$$

$$R1 = 12.4k\Omega \times \left(\frac{72V - 1.223V}{1.223V}\right) - 11.8k\Omega$$

$$R1 = 705.808k\Omega$$

The closest standard 1% value for R1 = 698kΩ.

Using standard 1% resistor values, the circuit's nominal UV and OV thresholds are:

V_{UV} = 36.5V
V_{OV} = 71.2V

Good general engineering design practices must consider the tolerances associated with these parameters, including but not limited to, power supply tolerance, undervoltgae and overvoltage tolerances, and the tolerances of the external passive components.

Programmable UVLO Hysteresis—MIC2594

The MIC2594 has user-programmable hysteresis by means of the ON and OFF pins. This allows setting the part to turn on at a voltage V1, and not turn off until a second voltage V2, where V2 < V1. This can significantly simplify dealing with source impedances in the supply bus while at the same time increasing the amount of available operating time from a loosely regulated power supply (for example, a battery supply). Similarly to the MIC2588, each of these pins is internally connected to an analog comparator with 20mV of hysteresis. The MIC2594 holds the output off until the voltage at the ON pin exceeds its V_{ONH} threshold value given in the "Electrical Characteristics" table. Once the output has been enabled by the ON pin, it will remain on until the voltage at

the OFF pin falls below its V_{OFFL} threshold value, or the part turns off due to a fault. Should either event occur, the GATE pin is immediately pulled low and will remain low until the ON pin once again exceeds its V_{ONH} threshold. The circuit's turn-on and turn-off points are set using the resistor divider R1, R2, and R3 as shown in the "Typical Application." The equations to establish the trip points are shown below. In the following example, the circuit's nominal ON threshold is set to V_{ON} = 40V and the circuit's nominal OFF threshold is V_{OFF} = 35V.

$$V_{ON} = V_{ONH}(typ) \times \frac{(R1 + R2 + R3)}{R3}$$

$$V_{OFF} = V_{OFFL}(typ) \times \frac{(R1 + R2 + R3)}{(R2 + R3)}$$

Given V_{OFF}, V_{ON}, and any one resistor value, the remaining two resistor values can be readily found. A suggested value for R3 is that which will provide a minimum of 100µA of current through the voltage divider chain at V_{DD} = V_{OFF}. This yields the following as a starting point:

$$R3 = \frac{V_{OFFL}(typ)}{100\mu A} = 12.23k\Omega$$

The closest standard 1% value for R3 = 12.4kΩ.

solving for R2 and R1 yields:

$$R2 = R3 \times \left[\left(\frac{V_{ON}}{V_{OFF}}\right) - 1\right]$$

$$R2 = 12.4k\Omega \times \left[\left(\frac{40V}{35V}\right) - 1\right]$$

$$R2 = 1.771k\Omega$$

The closest standard 1% value for R2 = 1.78kΩ.

$$R1 = R3 \times \frac{\left(V_{ON} - 1.223V\right)}{1.223V} - R2$$

$$R1 = 12.4k\Omega \times \frac{(40V - 1.223V)}{1.223V} - 1.78k\Omega$$

$$R1 = 391.380k\Omega$$

The closest standard 1% value for R1 = 392kΩ.

Using standard 1% resistor values, the circuit's nominal ON and OFF thresholds are:

V_{ON} = 40.1V
V_{OFF} = 35V

Good general engineering design practices must consider the tolerances associated with these parameters, including but not limited to, power supply tolerance, undervoltgae and overvoltage tolerances, and the tolerances of the external passive components.

Applications Information

Optional External Circuits for Added Protection/Performance

In many telecom applications, it is very common for circuit boards to encounter large-scale supply-voltage transients in backplane environments. Because backplanes present a complex impedance environment, these transients can be as high as 2.5 times steady-state levels, or 120V in worst-case situations. In addition, a sudden load dump anywhere on the circuit card can generate a very high voltage spike at the drain of the output MOSFET which, in turn, will appear at the DRAIN pin of the MIC2588/MIC2594. In both cases, it is good engineering practice to include protective measures to avoid damaging sensitive ICs or the hot swap controller from these large-scale transients. Two typical scenarios in which large-scale transients occur are described below:

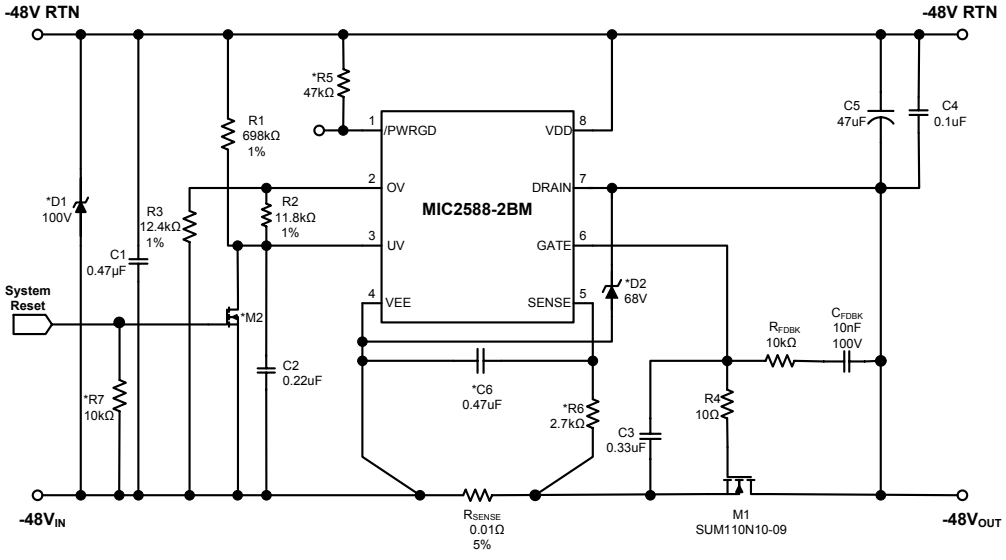
1. An output current load dump with no bypass (charge bucket or bulk) capacitance to V_{EE}. For example, if L_{LOAD} = 5µH, V_{IN} = 56V and t_{OFF} = 0.7µs, the resulting peak short-circuit current prior to the MOSFET turning off would reach:

$$\frac{(56V \times 0.7\mu s)}{5\mu H} = 7.8A$$

   If there is no other path for this current to take when the MOSFET turns off, it will avalanche the drain-source junction of the MOSFET. Since the total energy represented is small relative to the sturdiness of modern power MOSFETs, it's unlikely that this will damage the transistor. However, the actual avalanche voltage is unknown; all that can be guaranteed is that it will be greater than the $V_{BD(D-S)}$ of the MOSFET. The drain of the transistor is connected to the DRAIN pin of the MIC2588/MIC2594, and the resulting transient does have enough voltage and energy to damage this, or any, high-voltage hot swap controller.
2. If the load's bypass capacitance (for example, the input filter capacitors for DC-DC converter module(s)) are on a board from which the board with the MIC2588/MIC2594 and the MOSFET can be unplugged, the same type of inductive transient damage can occur to the MIC2588/MIC2594.

For many applications, the use of additional circuit components can be implemented for optimum system performance and/or protection. The circuit, shown in Figure 6, includes several components to address some the following system (dynamic) responses and/or functions: 1) suppression of transient voltage spikes, 2) elimination of false "tripping" of the circuit breaker due to undervoltage and overcurrent glitches, and 3) the implementation of an external reset circuit.

It is not mandatory that these techniques be utilized, however, the application environment will dictate suitability. For protection against sudden on-card load dumps at the DRAIN pin of the MIC2588/MIC2594 controller, a 68V, 1W, 5% Zener diode clamp (D2) connected from the DRAIN to the VEE of the controller can be implemented, as shown. To protect the controller from large-scale transients at the card input, a 100V clamp diode (D1, SMAT70A or equivalent) can be used. In either case, very short lead lengths and compact layout design is strongly recommended to prevent unwanted transients in the protection circuitry. Power buss inductance often produces localized (plug-in card) high-voltage transients during a turn-off event. Managing these repeated voltage stresses with sufficient input bulk capacitance and/or transient suppressing diode clamps is highly recommended for maximizing the life of the hot swap controller(s).



* Optional components (See Applications Information for more details)
An SOT-363 is recommended for M2.
D2 is a 68V, 1W Zener diode.

Figure 6 Optional Components for Added Performance/Protection

For systems that experience known load current surges exceeding the 400µs internal overcurrent filter (t_{FLT}), the RC circuit consisting of R6 and C6 provides a means for additional overcurrent filtering to eliminate false "tripping" of the circuit breaker due to these transient load current surges. It is highly recommended to limit the increase of the overcurrent filter to approximately 2x the internal filter to allow the MOSFET to operate within its thermal specifications and SOA. R6 and C6 act as a low-pass filter to reduce the slew rate of the SENSE pin voltage. The SENSE pin current is nominally 200nA, resulting in a slight voltage drop across R6 that will combine in series with the voltage across R_{SENSE} to produce an effective circuit breaker trip voltage of $V_{TRIP} – (R6 \times I_{SENSE})$. The following equation can be used to select component values for a given overcurrent filter delay.

$$t_{OCDLY} = – (R \times C) \ln \left[1 – \frac{V_{TRIP} – V(t_O)}{V(t) – V(t_O)} \right] \quad (8)$$

where V_{TRIP} is the typical circuit breaker trip voltage specified in the electrical specifications, V(t0) is the voltage drop across the sense resister before the short or overcurrent condition occurs, and V(t) is the voltage drop across the sense resistor when the short or overcurrent is applied. The following example sets an overcurrent delay of 1ms for a 7.5A load current surge with a 2A steady-state load current and 5A current limit (R_{SENSE} = 10mΩ).

V_{TRIP} = 50mV

$V(t_0)$ = 2A × 10mΩ = 20mV

V(t) = 7.5A × 10mΩ = 75mV

Using Equation 8, for R6 = 2.7kΩ, C6 is 0.47µF.

The capacitor (C2) connected from UV to reference (V_{EE}) is used as a glitch filter for the input undervoltage monitor. C2 combines with the resistive network at the UV pin to form an RC time constant to slow the UV pin voltage fall time whenever the input voltage experiences a negative (magnitude) transient. During start-up, the UV rise time will also be affected by a longer RC time constant due to R1, therefore, the output start cycle will be delayed until the UV pin crosses its threshold.

The circuit in Figure 6 consisting of M2, R7, R8, and a digital control signal, can be used to reset the controller after the GATE (and output) turns off. Once the output has been latched off, applying a low-high-low pulse on the GATE of M2 via the System Enable control can toggle the UV pin. System Enable is a user defined signal referenced to V_{EE}.

Sense Resistor Selection

The sense resistor is nominally valued at:

$$R_{SENSE(nom)} = \frac{V_{TRIP(typ)}}{I_{HOT\_SWAP(nom)}} \quad (9)$$

where $V_{TRIP(TYP)}$ is the typical (or nominal) circuit breaker threshold voltage (50mV) and $I_{HOT\_SWAP(NOM)}$ is the nominal load current level necessary to trip the internal circuit breaker.

To accommodate worse-case tolerances in the sense resistor (for a ±1% initial tolerance, allow ±3% tolerance for variations over time and temperature) and circuit breaker threshold voltages, a slightly more detailed calculation must be used to determine the minimum and maximum hot swap load currents.

As the MIC2588's minimum current limit threshold voltage is 40mV, the minimum hot swap load current is determined where the sense resistor is 3% high:

$$I_{HOT\_SWAP(min)} = \frac{40mV}{(1.03 \times R_{SENSE(nom)})} = \frac{38.8mV}{R_{SENSE(nom)}}$$

Keep in mind that the minimum hot swap load current should be greater than the application circuit's upper steady-state load current boundary. Once the lower value of R_{SENSE} has been calculated, it is good practice to check the maximum hot swap load current ($I_{HOT\_SWAP(MAX)}$) that the circuit may let pass in the case of tolerance build-up in the opposite direction. Here, the worse case maximum is found using a $V_{TRIP(MAX)}$ threshold of 60mV and a sense resistor 3% low in value:

$$I_{HOT\_SWAP(max)} = \frac{60mV}{(0.97 \times R_{SENSE(nom)})} = \frac{61.9mV}{R_{SENSE(nom)}}$$

In this case, the application circuit must be sturdy enough to operate up to approximately 1.5x the steady-state hot swap load current. For example, if an MIC2588 circuit must pass a minimum hot swap load current of 4A without nuisance trips, R_{SENSE} should be set to:

$$R_{SENSE(nom)} = \frac{40mV}{4A} = 10m\Omega$$

where the nearest 1% standard value is 10.0mΩ. At the other tolerance extremes, $I_{HOT\_SWAP(MAX)}$ for the circuit in question is then simply:

$$I_{HOT\_SWAP(max)} = \frac{61.9mV}{10m\Omega} = 6.19A$$

With a knowledge of the application circuit's maximum hot swap load current, the power dissipation rating of the sense resistor can be determined using $P = I^2 \times R$. Here, the current is $I_{HOT\_SWAP(max)}$ = 6.19A and the resistance $R_{SENSE(max)} = (1.03)(R_{SENSE(nom)})$ = 10.3mΩ.

Thus, the sense resistor's maximum power dissipation is:

$P_{MAX} = (6.19A)^2 \times (10.3m\Omega) = 0.395W$

A 0.5W sense resistor is a good choice in this application.

Power MOSFET Selection

Selecting the proper external MOSFET for use with the-MIC2588/MIC2594 involves three straightforward tasks:

- Choice of a MOSFET which meets minimum voltage requirements.
- Selection of a device to handle the maximum continuous current (steady-state thermal issues).
- Verify the selected part's ability to withstand any peak currents (transient thermal issues).

Power MOSFET Operating Voltage Requirements

The first voltage requirement for the MOSFET is easily stated:

the drain-source breakdown voltage of the MOSFET must be greater than $V_{IN(MAX)}$, or $V_{DD} – V_{EE}$(min).

The second breakdown voltage criterion that must be met is the gate-source voltage. For the MIC2588/MIC2594, the gate of the external MOSFET is driven up to a maximum of 11V above VEE. This means that the external MOSFET must be chosen to have a gate-source breakdown voltage of 12V or more; 20V is recommended. Most power MOSFETs with a 20V gate-source voltage rating have a 30V drain-source breakdown rating or higher. For many 48V telecom applications, transient voltage spikes can approach, and sometimes exceed, 100V. The absolute maximum input voltage rating of the MIC2588/MIC2594 is 100V; therefore, a drain-source breakdown voltage of 100V is suggested for the external MOSFET. Additionally, an external input voltage clamp is strongly recommended for applications that do not utilize conditioned power supplies.

Power MOSFET Steady-State Thermal Issues

The selection of a MOSFET to meet the maximum continuous current is a fairly straightforward exercise. First, arm yourself with the following data:

- The value of $I_{LOAD(CONT, MAX.)}$ for the output in question (see Sense Resistor Selection).
- The manufacturer's datasheet for the candidate MOSFET.
- The maximum ambient temperature in which the device will be required to operate.
- Any knowledge you can get about the heat sinking available to the device (e.g., can heat be dissipated into the ground plane or power plane, if using a surface-mount part? Is any airflow available?).

The datasheet will almost always give a value of on resistance for a given MOSFET at a gate-source voltage of 4.5V and 10V. For MIC2588/MIC2594 applications, choose the gate-source ON resistance at 10V and call this value R_{ON}. Since a heavily enhanced MOSFET acts as an ohmic (resistive) device, almost all that's required to determine steady-state power dissipation is to calculate I^2R. The one addendum to this is that MOSFETs have a slight increase in R_{ON} with increasing die temperature. A good approximation for this value is 0.5% increase in R_{ON} per °C rise in junction temperature above the point at which R_{ON} was initially specified by the manufacturer. For instance, if the selected MOSFET has a calculated R_{ON} of 10mΩ at aT_J = 25°C, and the actual junction temperature ends up at 110°C, a good first cut at the operating value for R_{ON} would be:

$$R_{ON} \approx 10m\Omega[1 + (110 – 25)(0.005)] \approx 14.3m\Omega$$

The final step is to make sure that the heat sinking available to the MOSFET is capable of dissipating at least as much power (rated in °C/W) as that with which the MOSFET's performance was specified by the manufacturer. Here are a few practical tips:

1. The heat from a TO-263 power MOSFET flows almost entirely out of the drain tab. If the drain tab can be soldered down to one square inch or more, the copper will act as the heat sink for the part. This copper must be on the same layer of the board as the MOSFET drain.
2. Airflow works. Even a few LFM (linear feet per-minute) of air will cool a MOSFET down substantially. If you can, position the MOSFET(s) near the inlet of a power supply's fan, or the outlet of a processor's cooling fan.
3. The best test of a candidate MOSFET for an application (assuming the above tips show it to be a likely fit) is an empirical one. Check the MOSFET's temperature in the actual layout of the expected final circuit, at full operating current. The use of a thermocouple on the drain leads, or infrared pyrometer on the package, will then give a reasonable idea of the device's junction temperature.

Power MOSFET Transient Thermal Issues

If the prospecitve MOSFET has been shown to withstand the environmental voltage stresses and the worse-case steady-state power dissipation is addressed, the remaining task is to verify if the MOSFET is capable of handling extreme overcurrent load faults, such as a short circuit, without overheating. A power MOSFET can handle a much higher pulsed power without damage than its continuos power dissipation ratings imply due to an inherent trait, thermal inertia. With respect to the specification and use of power MOSFETs, the parameter of interest is the "Transient Thermal Impedence", or Z_θ, which is a real number (variable factor) used as a multiplier of the thermal resistance (R_θ). The multiplier is determined using the given "Transient Thermal Imepedence Graph", normalized to R_θ, that displays curves for the thermal impedence versus power pulse duration and duty cycle. The single-pulse curve is appropriate for most hot swap applications. Z_θ is specified from junction-to-case for power MOSFETs typically used in telecom applications.

The following example provides a method for estimating the peak junction temperature of a power MOSFET in determining if the MOSFET is suitable for a particular application. V_{IN} (VDD – VEE) = 48V, I_{LIM} = 4.2A, and the power MOSFET is SUM110N10-09 (TO-263 package) from Vishay-Siliconix. This MOSFET has an R_{ON} of 9.5mΩ (T_J = 25°C), the junction-to-case thermal resistance ($R_{\theta(J-C)}$) is 0.4°C/W, junction-to-ambient thermal resistance ($R_{\theta(J-A)}$) is 40°C/W, and the Transient Thermal Impedence Curve is shown in Figure 7. Consider, say, the MOSFET is switched on at time t1 and the steady-state load current passing through the MOSFET is 3A. At some point in time after t1, at time t2, there is an unexpected short-circuit applied to the load, causing the MIC2588/MIC2594 controller to adjust the GATE output voltage and regulate the load current for 400µs at the programmed current limit value, 4.2A in this example. During this short-circuit load condition, the dissipation in the MOSFET is calculated by:

$$P_D(short) = V_{DS} \times I_{LIM} \qquad V_{DS} = 0V – (-48V) = 48V$$

$$P_D(short) = 48V \times 4.2A = 201.6W \text{ for } 400\mu s.$$

At first glance, it would appear that a very hefty MOSFET is required to withstand this extreme overload condition. Upon further examination, the calculation to approximate the peak junction temperature is not a difficult task. The first step is to determine the maximum steady-state junction temperature,

then add the rise in temperature due to the maximum power dissipated during a transient overload caused by a short circuit condtion. The equation to estimate the maximum steady-state junction temperature is given by:

$$T_J(\text{steady-state}) \cong T_C(\max) + \Delta T_J \quad (10)$$

T_C(max) is the highest anticipated case temperaure, prior to an overcurrent condition, at which the MOSFET will operate and is estimated from the following equation based on the highest ambient temperature of the system environment.

$$T_C(\max) = T_A(\max) + P_D \times (R_{\theta(J\text{-}A)} - R_{\theta(J\text{-}C)}) \quad (11)$$

Let's assume a maximum ambient of 60°C. The power dissipation of the MOSFET is determined by the current through the MOSFET and the on-resistance (I^2R), which we will estimate at 17mΩ (specification given at T_J = 125°C). Using our example information and substituting into Equation 11,

$$T_C(\max) = 60°C + [((3A)^2 \times 17m\Omega) \times (40 - 0.4)°C/W] = 66.06°C$$

Substituting the variables into Equation 10, T_J is determined by:

$$\begin{aligned} T_J(\text{steady-state}) &\cong T_C(\max)+[R_{ON}+(T_C(\max)-T_C)(0.005) \times (R_{ON})][I^2\times(R_{\theta(J\text{-}A)}-R_{\theta(J\text{-}C)})] \\ &\cong 66.06°C+[17m\Omega+(66.06°C-25°C)(0.005/°C) \times (17m\Omega)][(3A)^2\times(40-0.4)°C/W] \\ &\cong 66.06°C + 7.30°C \\ &\cong 73.36°C \end{aligned}$$

Since this is not a closed-form equation, getting a close apporoximation may take one or two iterations. On the second iteration, start with T_J equal to the value calculated above. Doing so in this example yields;

$$\begin{aligned} T_J(\text{steady-state}) &\cong 66.06°C+[17m\Omega+(73.36°C-25°C)\times(0.005/°C) \times(17m\Omega)][(3A)^2\times(40-0.4)]°C/W \\ &\cong 73.62°C \end{aligned}$$

Another iteration shows that the result (73.63°C) is converging quickly, so we'll estimate the maximum $T_{J(\text{steady-state})}$ at 74°C.

The use of the Transient Thermal Impedence Curves is necessary to determine the increase in junction temperature associated with a worst-case transient condition. From our previous calculation of the maximum power dissipated during a short circuit event for the MIC2588/MIC2594, we calculate the transient junction temperature increase as:

$$T_J(\text{transient}) = P_D(\text{short}) \times R_{\theta(J\text{-}C)} \times \text{Multiplier} \quad (12)$$

Assume the MOSFET has been on for a long time – several minutes or more – and delivering the steady-state load current of 3A to the load when the load is short circuited. The controller will regulate the GATE output voltage to limit the current to the programmed value of 4.2A for approximately 400µs before immediately shutting off the output. For this situation and almost all hot swap applications, this can be considered a single pulse event as there is no significant duty cycle. From Figure 7, find the point on the X-axis ("Square-Wave Pulse Duration") for 1ms, allowing for a healthy margin of the 400µs t_{FLT}, and read up the Y-axis scale to find the intersection of the Single Pulse curve. This point is the normalized transient thermal impedence ($Z_{\theta(J\text{-}C)}$), and the effective transient thermal impedence is the product of $R_{\theta(J\text{-}C)}$ and the multiplier, 0.45 in this example. Solving Equation 12,

$$T_J(\text{transient}) = (201.6W) \times (0.4°C/W) \times 0.45 = 36.3°C$$

Finally, add this result to the maximum steady state junction temperature calculated previously to determine the estimated maximum transient junction temperature of the MOSFET: T_J(max.transient) = 74°C + 36.3°C = 110.3°C, which is safely under the specified maximum junction temperature of 200°C for the SUM110N10-09.

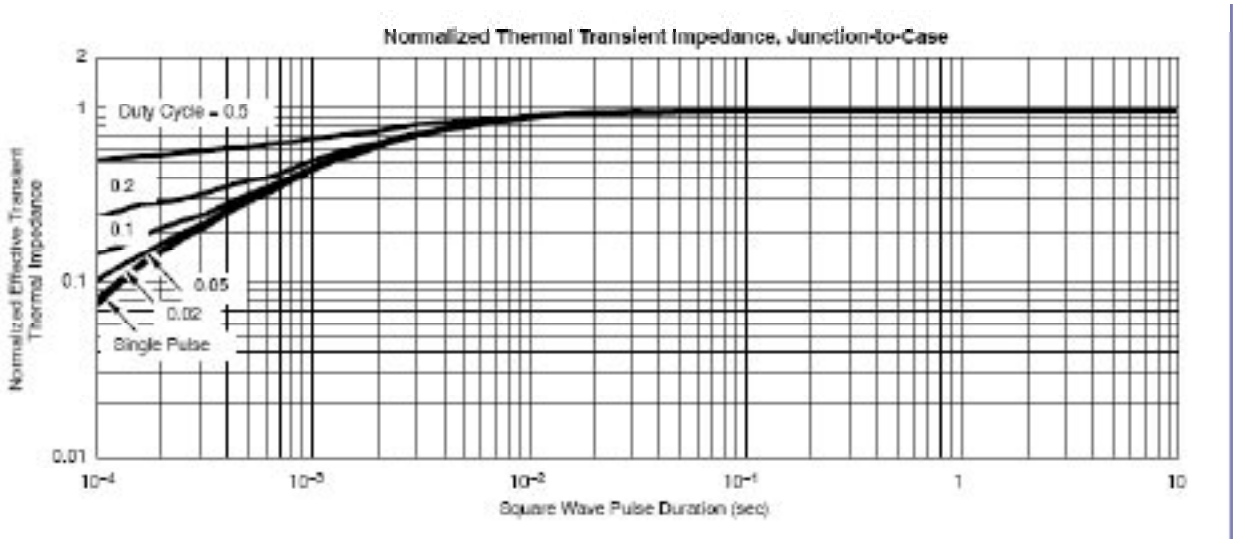


FIgure 7. Transient Thermal Impedance - SUM110N10-09

PCB Layout Considerations

4-Wire Kelvin Sensing

Because of the low value typically required for the sense resistor, special care must be used to measure accurately the voltage drop across it. Specifically, the measurement technique across each R_{SENSE} must employ 4-wire Kelvin sensing. This is simply a means of making sure that any voltage drops in the power traces connecting to the resistors are not picked up by the signal conductors measuring the voltages across the sense resistors.

Figure 8 illustrates how to implement 4-wire Kelvin sensing. As the figure shows, all the high current in the circuit (from V_{EE} through R_{SENSE}, and then to the source of the output MOSFET) flows directly through the power PCB traces and R_{SENSE}. The voltage drop resulting across R_{SENSE} is sampled in such a way that the high currents through the power traces will not introduce any parasitic voltage drops in the sense leads. It is recommended to connect the hot swap controller's sense leads directly to the sense resistor's metalized contact pads.

Other Layout Considerations

Figure 9 is a suggested PCB layout diagram for the MIC2588/MIC2594. Many hot swap applications will require load currents of several amperes. Therefore, the power (V_{EE} and Return) trace widths (W) need to be wide enough to allow the current to flow while the rise in temperature for a given copper plate (e.g., 1oz. or 2oz.) is kept to a maximum of 10°C to 25°C. The return (or power ground) trace should be the same width as the positive voltage power traces (input/load) and isolated from any ground and signal planes so that the controller's power is common mode. Also, these traces should be as short as possible in order to minimize the IR drops between the input and the load.

Finally, the use of plated-through vias will be necessary to make circuit connections to the power, ground and signal planes of multi-layer PCBs.

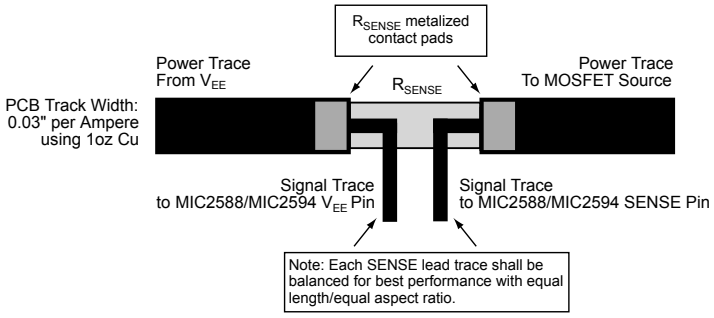


Figure 8. 4-Wire Kelvin Sense Connections for R_{SENSE}

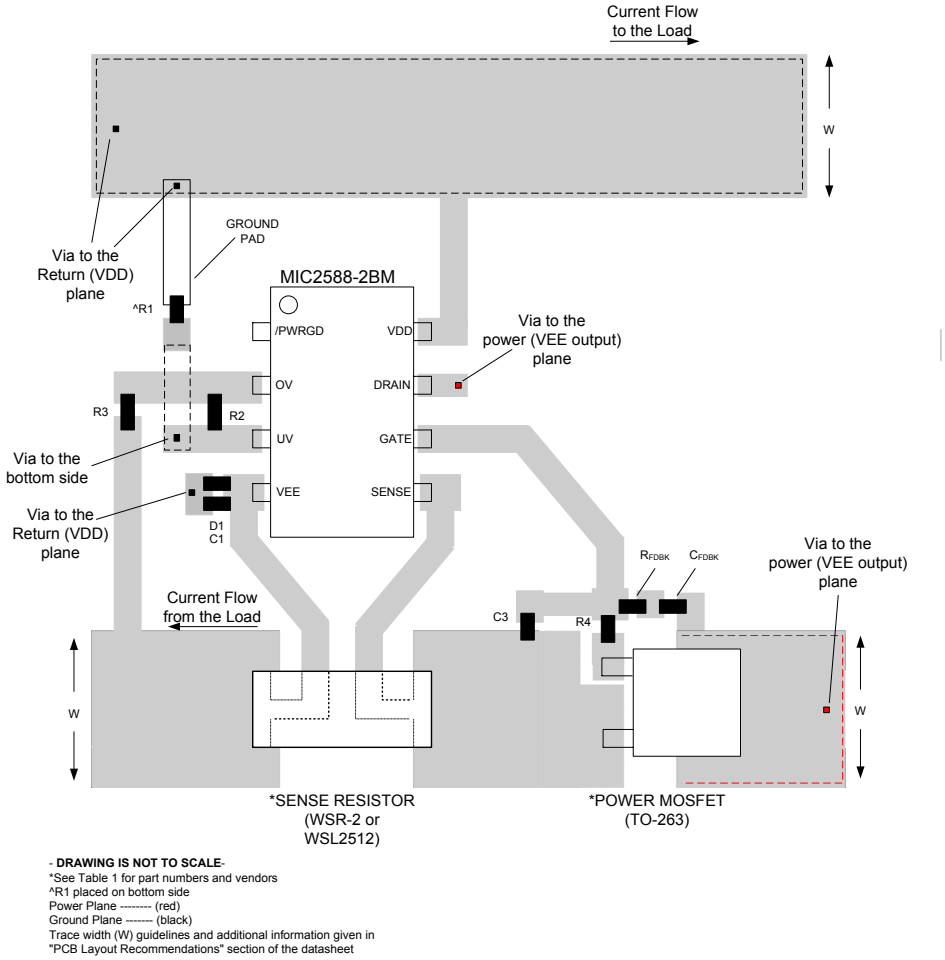


Figure 9. Recommended PCB Layout for Sense Resistor, Power MOSFET, Overvoltage/Undervoltage Resistive Divider Network, and Timer Capacitors

MOSFET and Sense Resistor Vendors

Device types, part numbers, and manufacturer contacts for power MOSFTETS and sense resistors are provided in Table 1.

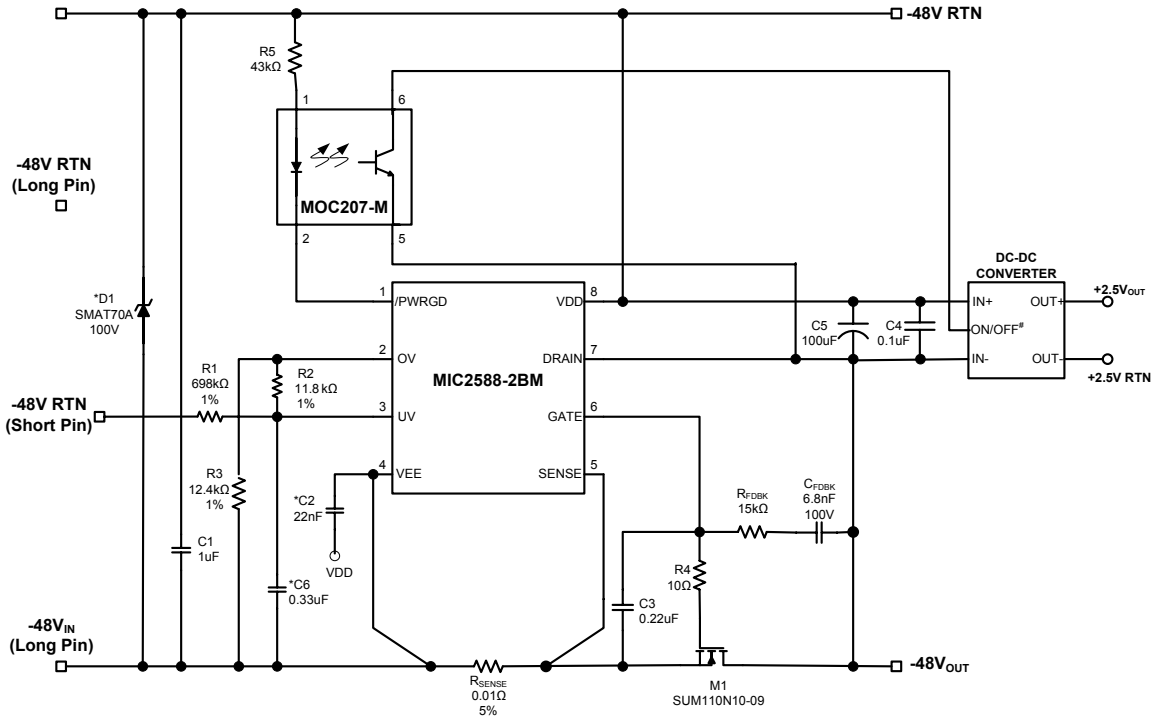
MOSFET Vendors	Key MOSFET Type(s)	Breakdown Voltage (V_{DSS})	Contact Information
Vishay - Siliconix	SUM75N06-09L (TO-263) SUM70N06-11 (TO-263) SUM50N06-16L (TO-263)	60V 60V 60V	www.siliconix.com (203) 452-5664
	SUP85N10-10 (TO-220AB) SUB85N10-10 (TO-263) SUM110N10-09 (TO-263) SUM60N10-17 (TO-263)	100V 100V 100V 100V	www.siliconix.com (203) 452-5664
International Rectifier	IRF530 (TO-220AB) IRF540N (TO-220AB)	100V 100V	www.irf.com (310) 322-3331
Renesas	2SK1298 (TO-3PFM) 2SK1302 (TO-220AB) 2SK1304 (TO-3P)	60V 100V 100V	www.renesas.com (408) 433-1990

Resistor Vendors	Sense Resistors	Contact Information
Vishay - Dale	“WSL” and “WSR” Series	www.vishay.com/docswsl_30100.pdf (203) 452-5664
IRC	“OARS” Series “LR” Series second source to “WSL”	www.irctt.com/pdf_files/OARS.pdf www.irctt.com/pdf_files/LRC.pdf (828) 264-8861

Table 1. MOSFET and Sense Resistor Vendors

/PWRGD Signal Drive Capability

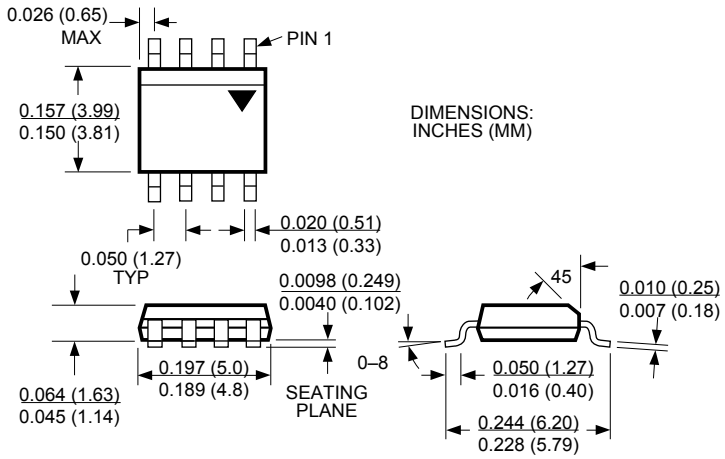
The /PWRGD signal can be used to drive an optoisolator or an LED. The use of an optoisolator is sometimes needed to protect I/O signals (e.g., /PWRGD, RESET, ENABLE) of both the controller and downstream DC-DC converter(s) from damage caused by common mode transients. Such is the case when an EMI filter is utilized to prevent DC-DC converter switching noise from being injected back onto the power supply. The circuit of Figure 10 shows how to configure an optoisolator driven by the /PWRGD signal of the MIC2588 controller.



Nominal Undervoltage and Overvoltage Thresholds:
V_{UV} = 36.5V
V_{OV} = 71.2V
* Optional components (See Applications Information for more details)
# An external pull-up resistor for the power-good signal is necessary for DC-DC supplies (and all other load modules) not equipped with internal pull-up impedence

Figure 10. Optoisolator Driven by /PWRGD Signal

Package Information



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