

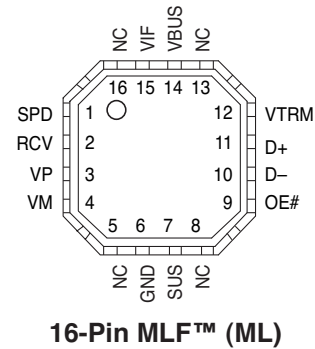
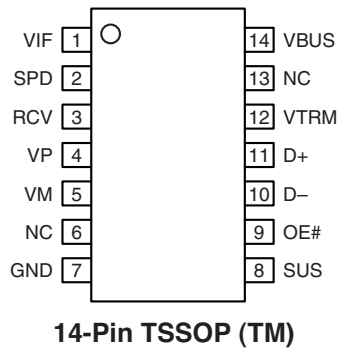


# THE DATASHEET OF MIC2550ABTS





## Pin Configuration



## Pin Description

Pin Name	Pin Number MIC2550ABTS	Pin Number MIC2550ABML	Pin Function
VIF	1	15	System Interface Supply Voltage (Input): Determines logic voltage levels for system interface signaling to logic controller.
SPD	2	1	Speed (Input): Edge rate control. Logic high selects full-speed edge rates. Logic low selects low-speed edge rates.
RCV	3	2	Receive Data (Output): System interface receive data interface to logic controller.
VP	4	3	Plus (Input/Output): System interface signal to logic controller. If OE# is logic 1, VP is a receiver output (+); If OE# is logic 0, VP is a driver input (+).
VM	5	4	Minus (Input/Output): System interface signal to logic controller. If OE# is logic 1, VM is a receiver output (-); If OE# is logic 0, VM is a driver input (-).
NC	6, 13	5, 8, 13 16	Not internally connected
GND	7	6	Ground: Power supply return and signal reference.
SUS	8	7	Suspend (Input): Logic high turns off internal circuits to reduce supply current.
OE#	9	9	Output Enable (Input): Active low system interface input signal from logic controller. Logic low causes transceiver to transmit data onto the bus. Logic high causes the transceiver to receive data from the bus.
D-	10	10	USB Differential Data Line - (Input/Output)
D+	11	11	USB Differential Data Line + (Input/Output)
VTRM	12	12	Termination Supply (Output): 3.3V speed termination resistor supply output.
VBUS	14	14	USB Supply Voltage (Input): Transceiver supply.

**Absolute Maximum Ratings (Note 1)**

Supply Voltage ( $V_{IF}$ )	+6.5V
Input Voltage ( $V_{BUS}$ )	-0.5V(min)/5.5V(max)
Output Current ( $I_{D+}$ , $I_{D-}$ )	$\pm 50$ mA
Output Current (all others)	$\pm 15$ mA
Input Current	$\pm 50$ mA
Storage Temperature ( $T_S$ )	-65° to +150°C

**ESD, Note 3**

$V_{BUS}$ , D+, D-	$\pm 10$ kV
All other pins	$\pm 2$ kV

**Operating Ratings (Note 2)**

Supply Voltage ( $V_{BUS}$ )	4.0V to 5.25V
Temperature Range ( $T_A$ )	-40°C to +85°C
Junction Temperature ( $T_J$ )	160°C
Package Thermal Resistance	
TSSOP ( $\theta_{JA}$ )	100°C/W

**Electrical Characteristics (Note 8)**

$T_A = 25^\circ\text{C}$ , **bold** values indicate  $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ ; typical values at  $V_{BUS} = 5.0\text{V}$ ,  $V_{IF} = 3.0\text{V}$ ; minimum and maximum values at  $V_{BUS} = 4.0\text{V}$  to  $5.25\text{V}$ ,  $V_{IF} = 2.5\text{V}$  to  $3.6\text{V}$ ; unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
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**System and USB Interface DC Characteristics**

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{BUS}$	USB Supply Voltage		4.0		5.25	V
$V_{IF}$	System I/F Supply Voltage		2.5		5.25	V
$V_{IL}$	Low-Level Input Voltage, <b>Note 4</b>				$0.15V_{IF}$	V
$V_{IH}$	High-Level Input Voltage, <b>Note 4</b>		$0.85V_{IF}$			V
$V_{OH}$	High-Level Output Voltage, <b>Note 4</b>	$I_{OH} = 20\mu\text{A}$	$0.9V_{IF}$			V
$V_{OL}$	Low-Level Output Voltage, <b>Note 4</b>	$I_{OL} = 20\mu\text{A}$			0.1	V
$I_{IL}$	Input Leakage Current, <b>Note 4</b>				$\pm 5$	$\mu\text{A}$

Symbol	Parameter	Conditions					Min	Typ	Max	Units
		SPD	SUS	OE#	Voltage	Load				
$I_{IF}$	VIF Supply Current	1	0	1	VBUS = 5.25V VIF = 3.6V		1	<b>5</b>	$\mu\text{A}$	
		1	0	0			1	<b>5</b>	$\mu\text{A}$	
		0	0	1			1	<b>5</b>	$\mu\text{A}$	
		0	0	0			1	<b>5</b>	$\mu\text{A}$	
		0	1	0			1	<b>5</b>	$\mu\text{A}$	
		1	0	0		f = 6MHz CLOAD = 50 pF, <b>Note 7</b>	325	<b>650</b>	$\mu\text{A}$	
		0	0	0		f = 750kHz CLOAD = 600 pF <b>Note 7</b>	40	<b>75</b>	$\mu\text{A}$	
$I_{VBUS}$	VBUS Supply Current	1	0	1	VBUS = 5.25V VIF = 3.6V		800	1100	$\mu\text{A}$	
		1	0	0			3000	<b>5000</b>	$\mu\text{A}$	
		0	0	1			230	<b>350</b>	$\mu\text{A}$	
		0	0	0			400	700	$\mu\text{A}$	
		0	1	0			130	200	$\mu\text{A}$	
		1	0	0		f = 6MHz CLOAD = 50 pF, <b>Note 7</b>	7.3	<b>10</b>	mA	
		0	0	0		f = 750kHz CLOAD = 600 pF <b>Note 7</b>	3.6	<b>5</b>	mA	
$V_{TRM}$	Termination Voltage	$I_{TRM} = 2.5\text{mA}$					3.0		3.6	V

**ESD Protection**

IEC-1000-4-2	Parameter	Condition	Min	Typ	Max	Units
(D+, D-, $V_{BUS}$ only)	Air Discharge	10 pulses		$\pm 6$		kV
	Contact Discharge	10 pulses		$\pm 6$		kV

Symbol	Parameter	Condition	Min	Typ	Max	Units
<b>Transceiver DC Characteristics</b>						
$I_{LO}$	Hi-Z State Data Line Leakage	$0V < V_{BUS} < 3.3V$ , D+, D-, OE# = 1 pins only	-10		+10	$\mu A$
$V_{DI}$	Differential Input Sensitivity	$ I(D+) - I(D-) $ , $V_{IN} = 0.8V - 2.5V$	0.2			V
$V_{CM}$	Differential Common-Mode Range	Includes $V_{DI}$ range	0.8		2.5	V
$V_{SE}$	Single-Ended Receiver Threshold		0.8		2.0	V
	Receiver Hysteresis, <b>Note 6</b>			200		mV
$V_{OL}$	Static Output Low, <b>Note 5</b>	OE# = 0, $R_L = 1.5k\Omega$ to 3.6V			0.3	V
$V_{OH}$	Static Output High, <b>Note 5</b>	OE# = 0, $R_L = 15k\Omega$ to GND	2.8		3.6	V
$V_{CRS}$	Output Signal Crossover Voltage <b>Note 6</b>		1.3		2.0	V
$C_{IN}$	Transceiver Capacitance, <b>Note 6</b>	Pin to GND			20	pF
$Z_{DRV}$	Driver Output Resistance	Steady state drive, <b>Note 6</b>	6		18	$\Omega$

**Low-Speed Driver Characteristics, Note 7**

$t_R$	Transition Rise Time	$C_L = 50pF$ $C_L = 600pF$	75		300	ns ns
$t_F$	Transition Fall Time	$C_L = 50pF$ $C_L = 600pF$	75		300	ns ns
$t_R/t_F$	Rise and Fall Time Matching	$T_R \div T_F$	80		125	%
$V_{CRS}$	Output Signal Crossover Voltage		1.3		2.0	V

**Full-Speed Driver Characteristics, Note 7**

$t_R$	Transition Rise Time	$C_L = 50pF$	4		20	ns
$t_F$	Transition Fall Time	$C_L = 50pF$	4		20	ns
$t_R/t_F$	Rise and Fall Time Matching	$T_R \div T_F$	90		111.11	%
$V_{CRS}$	Output Signal Crossover Voltage		1.3		2.0	V

**Transceiver Timing, Note 7**

$t_{PVZ}$	OE# to RCVR Tri-state Delay	Figure 1			15	ns
$t_{PZD}$	Receiver Tri-state to Transmit Delay	Figure 1	15			ns
$t_{PDZ}$	OE# to DRVR Tri-state Delay	Figure 1			15	ns
$t_{PZV}$	Driver Tri-state to Receiver Delay	Figure 1	15			ns
$t_{PLH}$	V+/V- to D+/D- Propagation Delay	Figure 4			15	ns
$t_{PHL}$	V+/V- to D+/D- Propagation Delay	Figure 4			15	ns
$t_{PLH}$	D+/D- to RCV Propagation Delay	Figure 3			15	ns
$t_{PHL}$	D+/D- to RCV Propagation Delay	Figure 3			15	ns
$t_{PLH}$	D+/D- to V+/D- Propagation Delay	Figure 3			8	ns
$t_{PHL}$	D+/D- to V+/D- Propagation Delay	Figure 3			8	ns

**Note 1.** Exceeding the absolute maximum rating may damage the device.

**Note 2.** The device is not guaranteed to function outside its operating rating.

**Note 3.** Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.

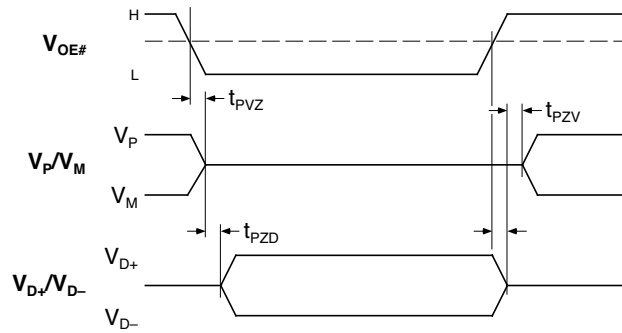
**Note 4.** Applies to the VP, VM, RCV, OE#, SPD, and SUS pins.

**Note 5.** Applies to D+, D-.

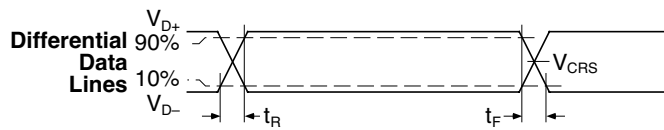
**Note 6.** Not production tested. Guaranteed by design.

**Note 7.** Characterized specification(s), but not production tested.

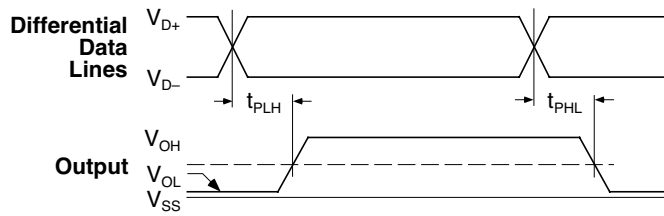
# Timing Diagrams



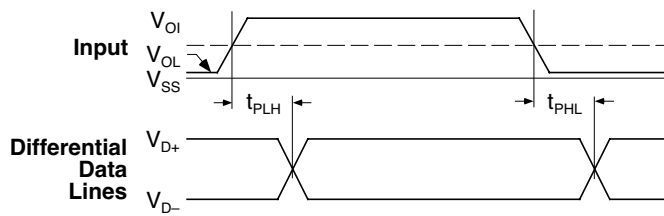
**Figure 1. Enable and Disable Times**



**Figure 2. Rise and Fall Times**



**Figure 3. Receiver Propagation Delay D+/D- to RCV, V<sub>P</sub>, and V<sub>M</sub>**



**Figure 4. Driver Propagation Delay V<sub>P</sub> and V<sub>M</sub> to D+/D-**

OE# = 0 (Transmit):					
Input		Output			Result
VP	VM	D+	D-	RCV	
0	0	0	0	X	SE0
0	1	0	1	0	Logic 0
1	0	1	0	1	Logic 1
1	1	1	1	X	Undefined
OE# = 1 (Receive):					
Input		Output			Result
D+	D-	VP	VM	RCV	
0	0	0	0	X	SE0
0	1	0	1	0	Logic 0
1	0	1	0	1	Logic 1
1	1	1	1	X	Undefined

Note. X = undefined.

Table 1. Truth Table

### Test Circuits

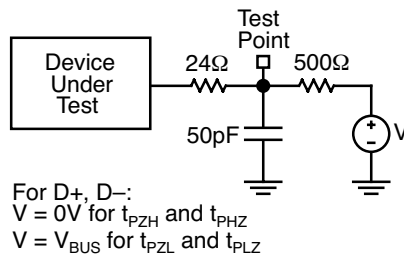


Figure 5. Load for Enable and Disable Time (D+, D-)

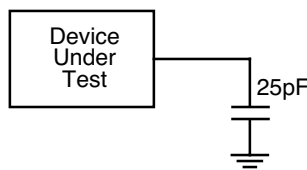
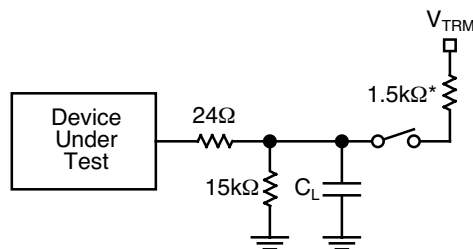


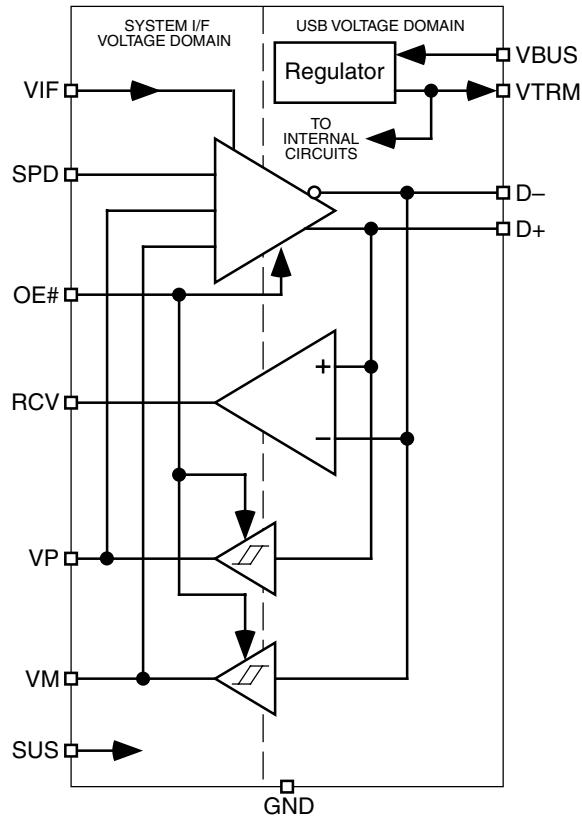
Figure 6.  $V_p$ ,  $V_M$  and RCV Load



$C_L = 50\text{pF}$ , full speed  
 $C_L = 50\text{pF}$ , low speed (minimum timing)  
 $C_L = 600\text{pF}$ , low speed (maximum timing)  
 \*1.5k on D- for low speed or D+ for high speed

Figure 7. D+ and D- Load

# Block Diagram



## Applications Information

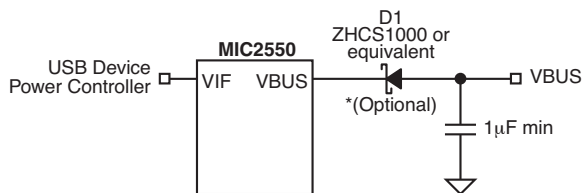
The MIC2550A is designed to provide USB connectivity in mobile systems where system supply voltages are not available to satisfy USB requirements. The MIC2550A can operate down to supply voltages of 2.5V and still meet USB physical layer specifications. As shown in the system diagram, the MIC2550A takes advantage of USB's supply voltage,  $V_{BUS}$ , to operate the transceiver. The system voltage,  $V_{IF}$ , is used to set the reference voltage used by the digital I/O lines (VP, VM, RCV, OE#, SPD, and SUS pins) interfacing to the system. Internal circuitry provides translation between the USB and system voltage domains.  $V_{IF}$  will typically be the main supply voltage rail for the system.

In addition, a 3.3V, 10% termination supply voltage,  $V_{TRM}$ , is provided to support speed selection. A 0.47 $\mu$ F (minimum) capacitor from  $V_{TRM}$  to ground is required to ensure stability. A 1.5K resistor is required between this pin and the D+ or D- lines to respectively specify full-speed or low-speed operation.

### Power Supply Configurations

#### $V_{IF}/V_{BUS}$ Switched

When the  $V_{BUS}$  input pin is pulled to ground a low impedance path between  $V_{IF}$  and  $V_{BUS}$  can cause a high current flow from  $V_{IF}$  to  $V_{BUS}$  thereby damaging the MIC2550A. This issue can arise in systems where  $V_{BUS}$  is driven from a power supply that can be switched off such as in the case of a desktop PC. Adding a Schottky diode, such as the ZHCS1000 by Zetex, in series with  $V_{BUS}$  will prevent any current flow during this condition. A solution is shown in Figure 8 below. If the  $V_{IF}$  source is current limited to less than 50mA, then diode D1 is not necessary.

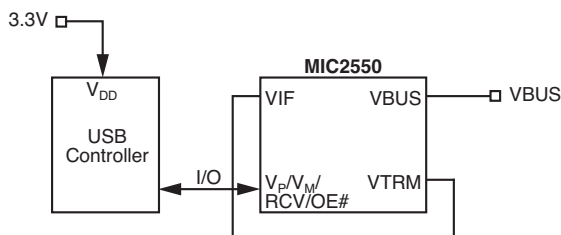


Note: \*(Optional) See Text - Power Supply Configurations

**Figure 8. Solution to  $V_{IF}/V_{BUS}$  Switching**

#### I/O Interface Using 3.3V

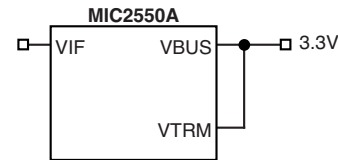
In systems where the I/O interface utilizes a 3.3V USB controller, an alternate solution is shown in Figure 9. This configuration has the advantage over Figure 8, in that no extra components are needed. Ensure that the load on  $V_{TRM}$  does not exceed 1mA total.



**Figure 9. I/O Interface Using 3.3V**

#### Internal 3.3V Source

If the device is self-powered and has 3.3V available, the circuit in Figure 10 is yet another power supply configuration option. In this configuration, the internal regulator is disabled and the 3.3V source and not  $V_{BUS}$  powers the entire chip.



**Figure 10. Powering Chip from Internal 3.3V Source**

#### Suspend

When the suspend pin (SUS) is high, power consumption is reduced to a minimum.  $V_{TRM}$  is not disabled. RCV,  $V_P$  and  $V_M$  are still functional to enable the device to detect USB activity. For minimal current consumption in suspend mode, it is recommended that OE# = 1, and SPD = 0.

#### Speed

The speed pin (SPD) sets D+/D- output edge rates by increasing or decreasing biasing current sources within the output drivers. For low speed, SPD = 0. For full speed, SPD = 1. By setting SPD = 0 during idle periods, in conjunction with suspend (SUS), the lowest quiescent current can be obtained. However, designers must provide a 300ns delay between changing SPD from 0 to 1 and transmission of data at full speed. This delay ensures the output drivers have arrived at their proper operating conditions. Failure to do so can result in leading edge distortion on the first few data bits transmitted.

#### External ESD Protection

The use of ESD transient protection devices is not required for operation, but is recommended. We recommend the following devices or the equivalent:

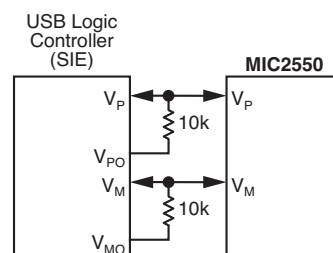
Cooper Electronics Technologies ([www.cooperet.com](http://www.cooperet.com))  
41206ESDA SurgX<sup>®</sup>  
0805ESDA SurgX<sup>®</sup>

Littelfuse ([www.littelfuse.com](http://www.littelfuse.com))

V0402MHS05  
SP0503BAHT

#### Non-multiplexed Bus

To save pin count for the USB logic controller interface, the MIC2550A was designed with  $V_P$  and  $V_M$  as bidirectional pins. To interface the MIC2550A with a non-multiplexed data bus, resistors can be used for low cost isolation as shown in Figure 11.



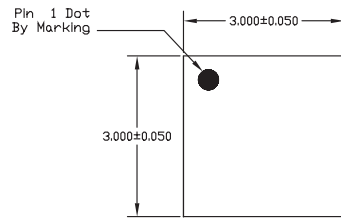
**Figure 11. MIC2550A Interface to Non-multiplexed Data Bus**

## PCB Layout Recommendations

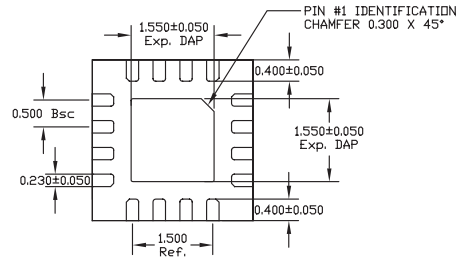
Although the USB standard and applications are not based in an impedance controlled environment, a properly designed PCB layout is recommended for optimal transceiver performance. The suggested PCB layout hints are as follows:

- Match signal line traces (VP/VM, D+, D-) to 40ps, approximately  $\frac{1}{3}$  inch if possible. FR-4 PCB material propagation is about 150ps/inch, so to minimize skew try to keep VP/VM, D+/D- traces as short as possible.
- For every signal line trace width (w), separate the signal lines by 1.5–2 widths. Place all other traces at  $>2w$  from all signal line traces.
- Maintain the same number of vias on each differential trace, keeping traces approximately at same separation distance along the line.
- Control signal line impedances to  $\pm 10\%$ .
- Keep  $R_S$  as close to the IC as possible, with equal distance between  $R_S$  and the IC for both D+ and D-.

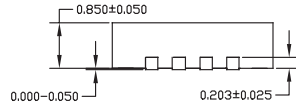




TOP VIEW



BOTTOM VIEW



SIDE VIEW

- NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
  2. MAX. PACKAGE WARPAGE IS 0.05 mm.
  3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
  4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.

**16-Pin MLF™ (ML)**

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