MIC25400

2A Dual Output PWM Synchronous Buck Regulator IC

General Description

The MIC25400 is a synchronous PWM dual output step down converter with internal 2A high-side switches. The MIC25400 has an integrated low-side gate driver for synchronous step-down conversion by connecting an external N-channel MOSFET to achieve high efficiencies in low duty-cycle applications. The IC's switching frequency is 1MHz. A patented control scheme allows the use of a wide range of output capacitance from small ceramic capacitors to large electrolytic types with only one compensation component. A 2% output voltage tolerance over the temperature range allows the maximum level of system performance. The MIC25400 power good signal allows full control for sequencing the output voltages with minimum external components.

An adjustable current limit allows the use of smaller inductors in lower current applications.

The MIC25400 is available in the ePad 24-pin 4mm × 4mm MLF® package, and has an operating junction temperature range of –40°C to +125°C.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

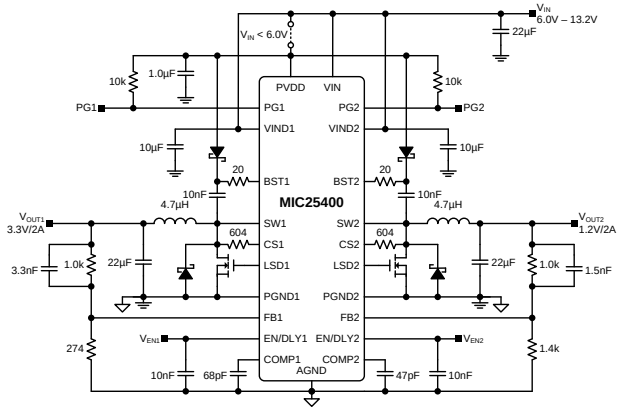
Features

- 4.5V to 13.2V input voltage range
- Adjustable output voltages down to 0.7V
- 2A per channel
- 180° out-of-phase operation
- Low-side driver for synchronous operation
- 2% output voltage accuracy (over temperature)
- 1MHz switching frequency
- Output voltage sequencing
- Programmable maximum current-limit
- Power good output
- Ramp Control™ provides soft-start
- Low-side current sensing allows very low duty-cycle
- Works with ceramic output capacitors
- 24-pin 4mm × 4mm MLF package
- Junction temperature range of –40°C to +125°C

Applications

- Multi-output power supplies with sequencing
- DSP, FPGA, CPU, and ASIC power supplies
- Telecom and networking equipment, servers

Typical Application



MIC25400 Dual Output Buck Converter

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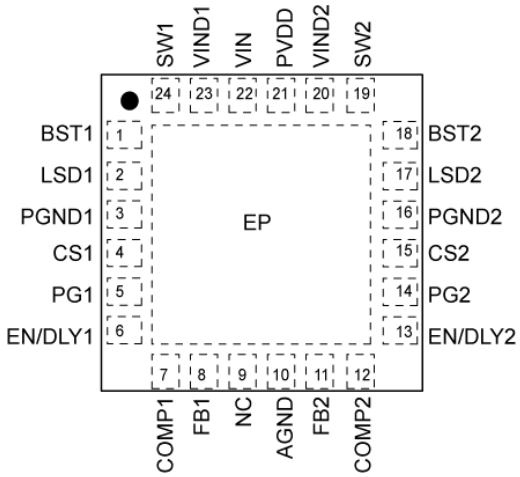
MLF and *Micro*Lead Frame are registered trademarks of Micrel, Inc.

Ordering Information

Part Number	Voltage	Switching Frequency	Temperature Range	Package	Lead Finish
MIC25400YML	Adjustable	1MHz	-40°C to +125°C	24-Pin 4mm × 4mm MLF	Pb-Free

Pin Configuration



24-Pin 4mm × 4mm MLF (ML)
(Top View)

Pin Description

Pin Number	Pin Name	Pin Description
1	BST1	Boost 1 (Input): Provides voltage for high-side internal MOSFET for channel 1. Connect a 0.01µF capacitor from SW1 to BST1 pin and a diode-to-PVDD.
2	LSD1	Low-Side Drive 1 (Output): External low-side N-Channel MOSFET driver. Use 4.5V rated MOSFETs.
3	PGND1	Power Ground 1 (Input).
4	CS1	Current Sense 1 (Input): Place a resistor from SW1 to this pin to program the current limit point from 0.5A to 2.7A.
5	PG1	Power Good 1 (Output): Open drain. Device is in the OFF state. i.e., high when output is within 90% of regulation.
6	EN/DLY1	Enable/Delay 1 (Input): This pin can be used to disable V_{OUT1}. When used to disable V_{OUT1}, this pin must be pulled down to ground in less than 1µs for proper operation. It is also used for soft-start of the output. Soft-start capacitor range is 4.7nF to 22nF (see the *Functional Description* section for additional information).
7	COMP1	Compensation 1 (Input): Pin for external compensation, Channel 1.
8	FB1	Feedback 1 (Input): Input to Ch1 error amplifier. Regulates to 0.7V.
9	NC	No Connect.
10	AGND	Analog Ground (Input): Control section ground. Connect to PGND.

Pin Description (Continued)

Pin Number	Pin Name	Pin Description
11	FB2	Feedback 2 (Input): Input to Channel 2 error amplifier. Regulates to 0.7V.
12	COMP2	Compensation 2 (Input): Pin for external compensation, Channel 2.
13	EN/DLY2	Enable/Delay 2 (Input): This pin can be used to disable V_{OUT2}. When used to disable V_{OUT2}, this pin must be pulled down to ground in less than 1µs for proper operation. It is also used for soft-start of the output. Soft-start capacitor range is 4.7nF to 22nF (see the *Functional Description* section for additional information).
14	PG2	Power Good 2 (Output) Open drain. Device is in the OFF state. i.e., high when output is within 90% of regulation
15	CS2	Current Sense 2 (Input) Place a resistor from SW2 to this pin to program the current-limit point from 0.5A to 2.7A
16	PGND2	Power Ground 2 (Input)
17	LSD2	Low-Side Drive 2 (Output): External low-side N-Channel MOSFET driver. Use 4.5V rated MOSFETs.
18	BST2	Boost 2 (Input): Provides voltage for high-side internal MOSFET for Channel 2. Connect a 0.01µF capacitor from SW2 to BST2 pin and a diode-to-PVDD.
19	SW2	Switch Node 2 (Output): Source of internal high-side power MOSFET.
20	VIND2	Supply voltage (Input): For the drain of internal high-side power MOSFET 4.5V to 13.2V.
21	PVDD	5V Internal Linear Regulator (Output): PVDD is the external MOSFET gate drive for LSD1 and LSD2 and an internal supply bus for the IC. Connect to an external 1µF bypass capacitor. When VIN is <6V, this regulator operates in drop-out mode. Connect VDD to VIN when VIN <6V.
22	VIN	Supply voltage (Input): For the internal 5V linear regulator. 4.5V to 13.2V.
23	VIND1	Supply voltage (Input): For the drain of internal high-side power MOSFET 4.5V to 13.2V.
24	SW1	Switch Node 1 (Output): Source of internal high-side power MOSFET.
EP	GND	Exposed thermal pad for package only. Connect to ground. Must make a full connection to the ground plane to maximize thermal performance of the package.

Absolute Maximum Ratings[1]

V_{IN} to PGND ..... –0.3V to 16V
V_{IND1}, V_{IND2} to PGND..... –0.3V to 16V
V_{PVDD} to PGND ..... –0.3V to 6V
V_{SW1}, V_{SW2} to PGND .....–0.7V to (V_{IN} + 0.3V)
V_{CS1}, V_{CS2} to PGND .....–0.7V to (V_{IN} + 0.3V)
V_{BST1} to V_{SW1}, V_{BST2} to V_{SW2}..... –0.3V to 6.0V
V_{BST1}, V_{BST2} to PGND..... –0.3V to 22V
$V_{EN/DLY1}$, $V_{EN/DLY2}$ to PGND.....–0.7V to (V_{PVDD} + 0.3V)
V_{COMP1}, V_{COMP2} to PGND.....–0.7V to (V_{PVDD} + 0.3V)
V_{FB1}, V_{FB2} to PGND.....–0.7V to (V_{PVDD} + 0.3V)
V_{PG1}, V_{PG2} to PGND .....–0.7V to (V_{PVDD} + 0.3V)
PGND1, PGND2 to AGND ..... –0.3V to +0.3V
Junction Temperature ..... 150°C
Storage Temperature .....–65°C to +150°C
Lead Temperature (soldering,10s)..... 260°C
ESD Rating[3]..... 2kV

Operating Ratings[2]

Supply Voltage (V_{IN})..... +4.5V to +13.2V
Output Voltage Range (V_{OUT})……..0.7V to 0.7*V_{IN}
Maximum Output Current (I_{OUT})…….. .....2A
Junction Temperature (T_J) .....–40°C to +125°C
Junction Thermal Resistance
4mm × 4mm MLF-24L (θ_{JA}) .....35°C/W

Electrical Characteristics[4]

V_{IN} = 12V; V_{EN} = 5V; V_{OUT}=1.8V; I_{LOAD}=10mA; T_A = 25°C, **bold** values indicate –40°C ≤ TJ ≤ +125°C, unless noted.

Parameter	Condition	Min.	Typ.	Max.	Units
Power Input Supply					
Input Voltage Range (V_{IN})		4.5		13.2	V
Quiescent Supply Current	V_{FB} = 0.8V, I_{OUT} = 0A; Both outputs not switching		3.6	**7**	mA
Shutdown Current	V_{EN1} = V_{EN2} = 0V		360	**425**	µA
V_{IN} UVLO Threshold	V_{IN} Rising, P_{VDD} open, for V_{IN}≥6V	**3.6**	4.02	**4.5**	V
V_{IN} UVLO Hysteresis	V_{IN} ≥ 6V		150		mV
V_{IN} UVLO V_{IN} <6V)	V_{IN} Rising, P_{VDD} connected to V_{IN}, for V_{IN}<6V	**3.2**	3.5	**3.9**	V
VDD Supply					
Internal Bias Voltages P_{VDD}	V_{FB} = 0.8V, I_{PVDD} = 75mA	4.7	5.1	5.4	V
Reference (Each Channel)					
Feedback Reference Voltage	±2% over temperature	**686**	700	**714**	mV
FB Bias Current	V_{FB} = 0.7V		5		nA
FB Line Regulation	V_{IN} = 6V to 13.2V, I_{OUT} = 10mA		0.005		%/V
Output Voltage Line Regulation	V_{IN} = 6V to 13.2V , V_{OUT} = 1.8V, I_{OUT} = 1A		0.005		%/V
Output Voltage Load Regulation	V_{OUT} = 1.8V, I_{OUT} = 0A to 2A		0.15		%
Output Voltage Total Regulation	V_{IN} = 6V to 13.2V , I_{OUT} = 0.25A to 2A, V_{OUT} = 1.8V		0.1		%

Notes:

1. Exceeding the absolute maximum ratings may damage the device.
2. The device is not guaranteed to function outside its operating ratings.
3. Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5kΩ in series with 100pF.
4. Specification for packaged product only.

Electrical Characteristics[4] (Continued)

V_{IN} = 12V; V_{EN} = 5V; V_{OUT}=1.8V; I_{LOAD}=10mA; T_A = 25°C, **bold** values indicate –40°C ≤ TJ ≤ +125°C, unless noted.

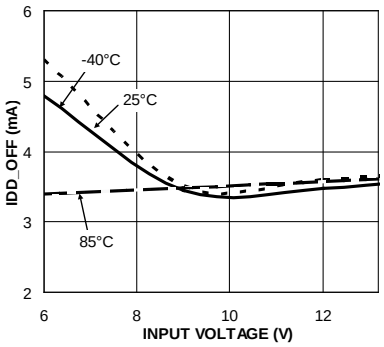
Parameter	Condition	Min.	Typ.	Max.	Units
External Current Sense, Adjustable					
Current-Limit Trip Point Current	Sourcing current	175	200	225	µA
Current-Limit Temperature Coefficient			750		ppm/°C
Current-Limit Comparator Offset		**–10**	0	**10**	mV
Oscillator / PWM					
Switching Frequency		**0.8**	1	**1.2**	MHz
Maximum Duty-cycle		**70**	75		%
Minimum On-Time	I_{LOAD} > 200mA[5]		15		ns
Error Amplifier (each channel)					
DC Gain			68		dB
High-Side Internal MOSFET					
On-Resistance RDS(ON)	I_{FET} = 1A, V_{FB}=0.8V		150		mΩ
Low-Side MOSFET Driver					
DH On-Resistance	Pull Up, I_{SOURCE} = 10mA		4		Ω
	Pull Down; I_{SINK} = 10mA		2.5		Ω
DH Transition Time	Into 1000pF		12		ns
	Into 1000pF		9		ns
Driver Non-Overlap Dead Time	(Adaptive)		25		ns
EN/DLY and Soft-Start Control					
EN/DLY Pull-Up Current	$V_{EN/DLY}$=0V	**5.0**	6.5	**8.0**	µA
P_{VDD} Threshold	P_{VDD} turns on	**0.3**	0.4	**0.6**	V
Soft-Start Begins Threshold	Channel soft-start begins	**1**	1.35	**1.8**	V
Soft-Start Ends Threshold	Channel soft-start ends	**2**	2.4	**2.8**	V
Power Good					
PG Threshold Voltage	V_{OUT} Rising (% of V_{OUT} nominal)	**86**	90	**94**	%Nom
PG Output Low Voltage	V_{FB} = 0V, I_{PG} = 1mA		0.24	**0.3**	V
PG Leakage Current	V_{FB} = 800mV, V_{PG} = 5.5V		5		nA
Thermal Protection					
Overtemperature Shutdown	T_J Rising		172		°C
Overtemperature Shutdown Hysteresis			22		°C

Note:

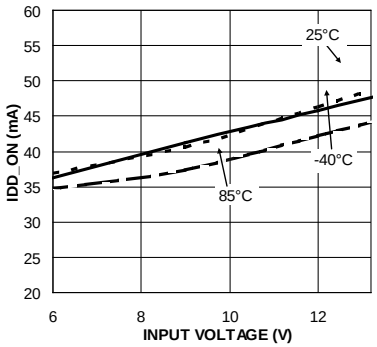
5. Minimum on-time before automatic cycle skipping begins (see *Application Information*).

Typical Characteristics

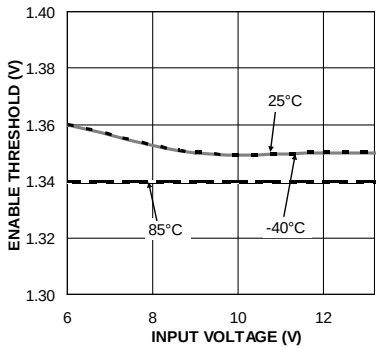
I_{DD_OFF} vs. Input Voltage



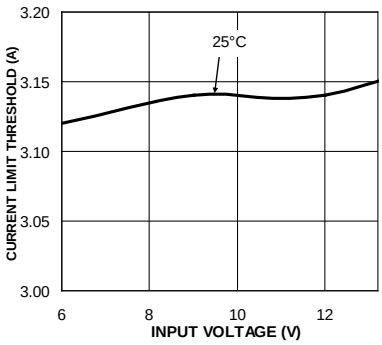
I_{DD_ON} vs. Input Voltage



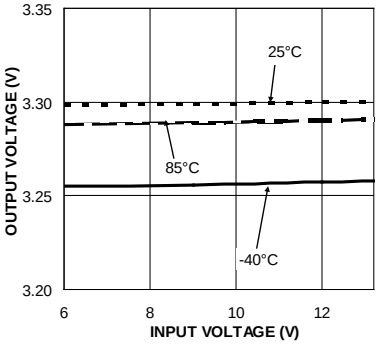
Enable Threshold vs. Input Voltage



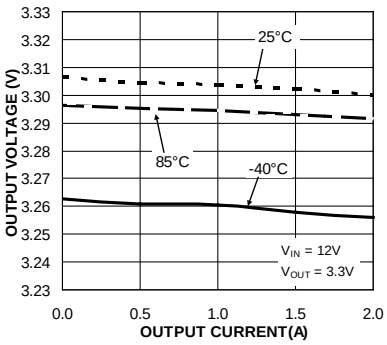
Current Limit Threshold vs. Input Voltage



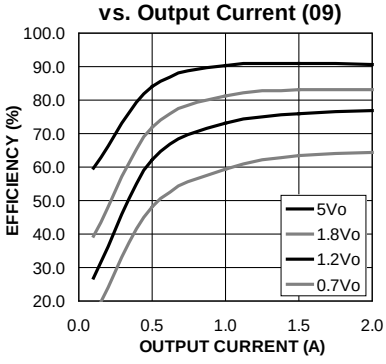
Output Voltage vs. Input Voltage



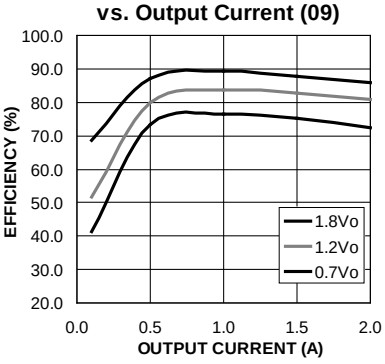
Load Regulation



$12V_{IN}$ Efficiency vs. Output Current (09)

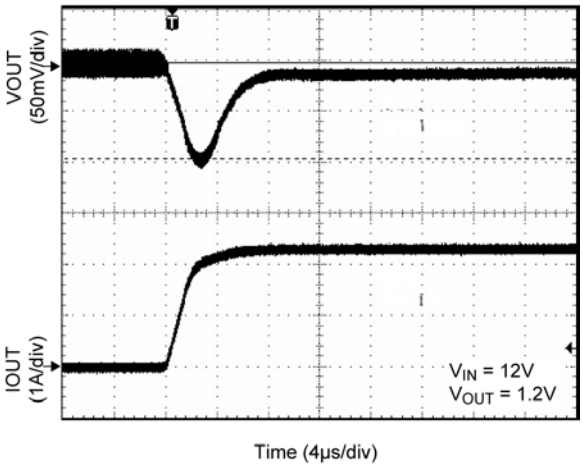


$5V_{IN}$ Efficiency vs. Output Current (09)

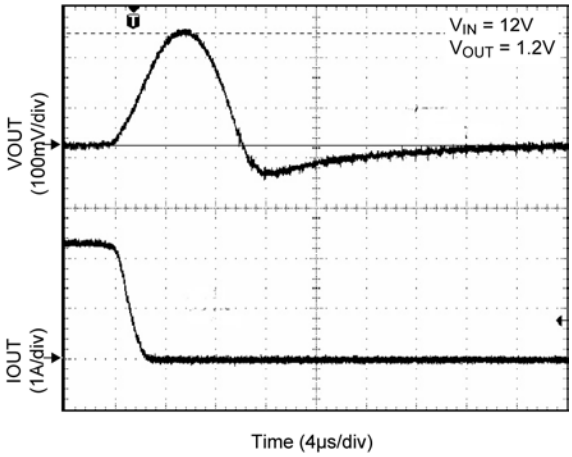


Functional Characteristics

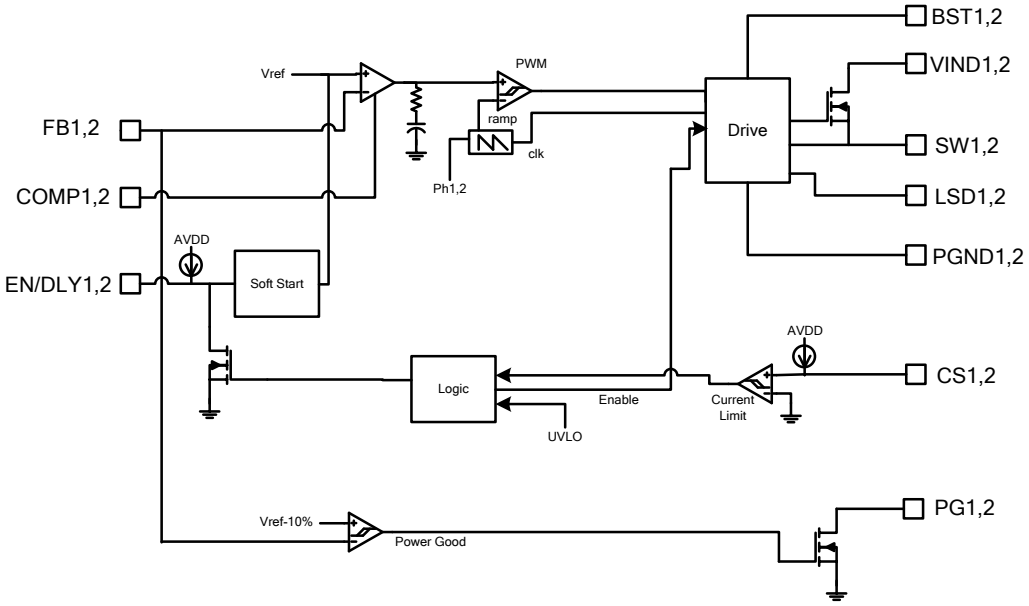
Transient Response



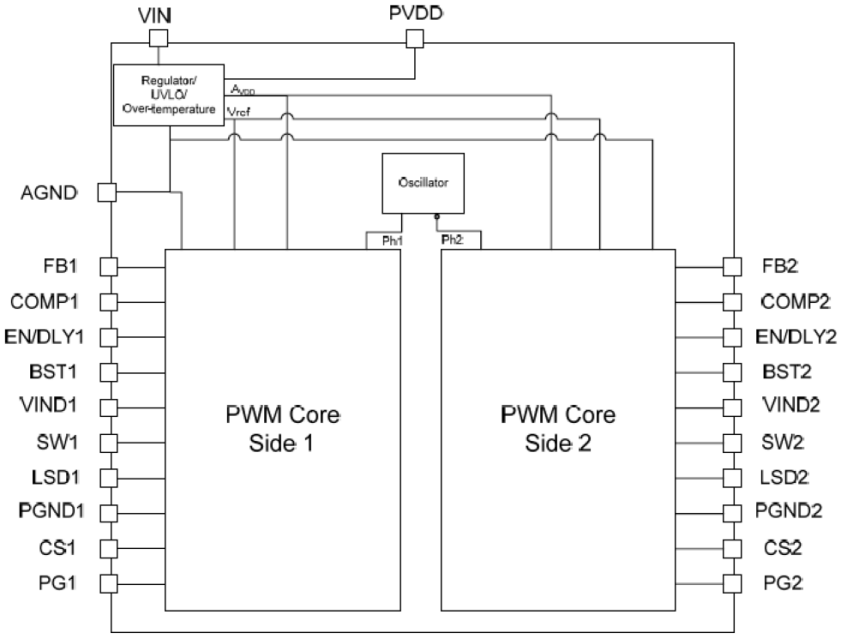
Transient Response



Functional Diagram



PWM Core



MIC25400 Block Diagram

Functional Description

The MIC25400 is a dual output, synchronous buck regulators. Output regulation is performed using a fixed frequency, voltage mode control scheme. The fixed frequency clock drives the two sections 180° out of phase, which reduces input ripple current.

Oscillator

An internal oscillator provides a clock signal to each of the two sides. The clock signals are 180° out of phase with the other. Each phase is used to generate a ramp for the PWM comparator and a clock pulse that terminates the switching cycle. The MIC25400 oscillator frequency is nominally 1MHz.

UVLO

The UVLO monitors voltage on the V_{IN} pin. The circuit controls both regulators (side 1 and side 2). It disables the output drivers and discharges the EN/DLY capacitor when V_{IN} is below the UVLO threshold. As V_{IN} rises above the threshold, the internal high-side FET drivers and external low-side drives are enabled and the EN/DLY pins are released.

A low impedance source should be used to supply input voltage to the MIC25400. When V_{IN} drops below the UVLO threshold and the outputs turn off, the change in input current will cause V_{IN} to slight rise. The output voltage will momentarily turn back on if the rise in V_{IN} is greater than the UVLO hysteresis.

The preferred method is to use the EN/DLY pins, as shown in Figure 1, for startup and shutdown of the outputs. This avoids the possibility of glitching during startup and shutdown. If an external control signal is not available, the circuit in Figure 2 may be used to set a higher turn-on and turn-off threshold than the internal UVLO circuit. Moreover, the hysteresis is adjustable and can accommodate a wider input source impedance range. Refer to the MIC841 datasheet for additional information on selecting the resistor values.

Regulator/Reference

The internal regulator generates a PVDD pin voltage that powers the high-side MOSFET and low-side gate drive circuits. It also generates an internal analog voltage, A_{VDD}, which is used by the low level analog and digital sections. The A_{VDD} voltage is also used by the bandgap to generate a nominal 700mV for the error amplifier reference. The output undervoltage and power good circuits use the bandgap for their references.

The dropout of the internal regulator causes V_{PVDD} to drop when V_{IN} is below 6V. When operating below 6V, the PVDD pin must be jumpered to V_{IN}. This bypasses the internal LDO and prevents V_{PVDD} from dropping out.

A 1µF ceramic capacitor should be used to decouple V_{PVDD}-to-ground.

EN/DLY

The EN/DLY pins are used to turn on, turn off and soft-start the outputs. The pins can be controlled with an open collector or open drain device as shown in Figure 1. It must not be actively driven high or damage will result. When disabling the output with an external device, the enable pin turn-off time must be less than 1µs.

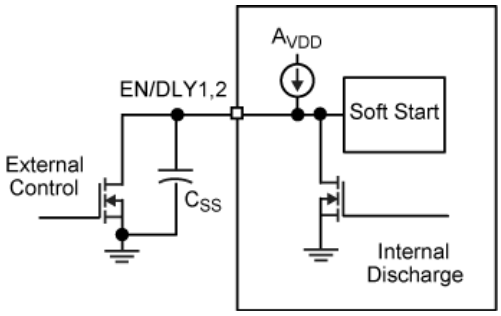


Figure 1. Enable and Soft-Start Circuit

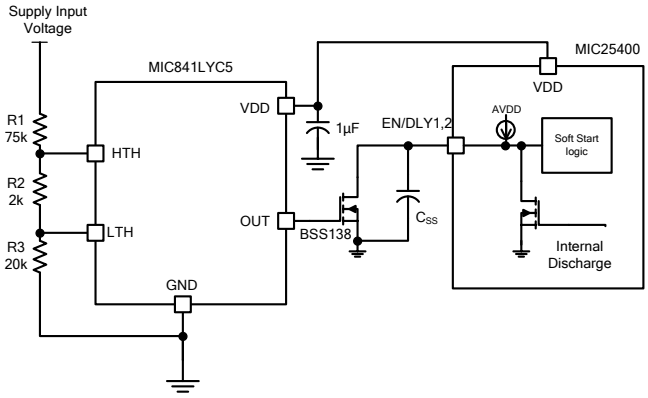


Figure 2. Adjustable UVLO Start-Up Circuit

Minimum Output Load when Disabled

When one output is disabled and the other enabled, then the disabled output requires a minimum output load to prevent its output voltage from rising. Typically, a 2kΩ load on the output will keep the output voltage below 100mV. The output setting voltage divider resistors may be used for the 2kΩ load if the total resistance is set low enough. A separate output resistor should be used for lower output voltages since the voltage divider resistance becomes impractically low.

Soft-Start

Enable and soft-start waveforms are shown in Figure 3.

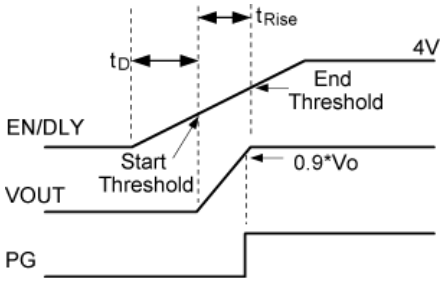


Figure 3. Soft-Start Timing Diagram

A capacitor, C_{SS}, is connected to the EN/DLY pin. The C_{SS} capacitor range is 4.7nF to 22nF. Releasing the pin allows an internal current source to charge the capacitor. The delay between the EN/DLY pin release and when V_{OUT} starts to rise can be calculated by Equation 1.

$$t_D = \frac{C_{SS} \times V_{Threshold\_Start}}{I_{SS}} \quad \text{Eq. 1}$$

where:

- C_{SS} is the soft-start capacitor.
- I_{SS} is the internal soft-start current (200µA nominal).
- $V_{Threshold\_start}$ is the EN/DLY pin voltage where the output starts to rise (1.35V nominal).

The output voltage starts to rise when voltage on the EN/DLY pin reaches the start threshold. The output voltage reaches regulation when the EN/DLY pin voltage reaches the end threshold.

The output voltage rise time can be calculated by Equation 2:

$$t_D = \frac{C_{SS} \times (V_{Threshold\_End} - V_{Threshold\_Start})}{I_{SS}} \quad \text{Eq. 2}$$

where:

- $V_{Threshold\_End}$ is the EN/DLY pin voltage where the output reaches regulation.

Power Good

Power good is an open drain signal that asserts when V_{OUT} exceed the power good threshold. The circuit monitors the FB pin. The internal FET is turned on while the FB voltage is below the FB threshold. When voltage on the FB in exceeds the FB threshold, the FET is turned off. A pull-up resistor can be connected to P_{VDD} or and external source. The external source voltage must not exceed the maximum rating of the pin. The PG pin can be connected to another regulator's EN/DLY pin for sequencing of the outputs. A pull-up resistor is not used when the power good pin is connected to another regulators EN/DLY pin.

Output Sequencing

Sequencing of the outputs is shown in Figure 4. The power good pin is used to disable V_{OUT2} until the V_{OUT1} reaches regulation. Sequencing waveforms are shown in Figure 4.

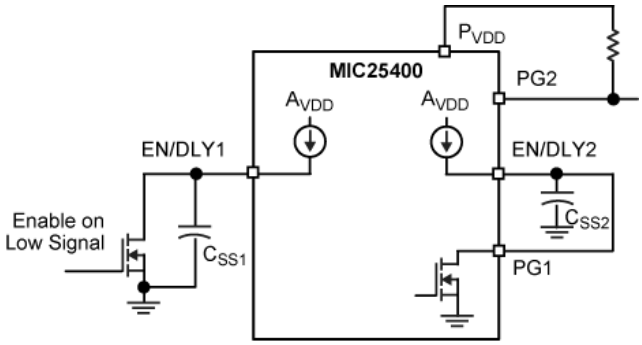


Figure 4. Output Sequencing

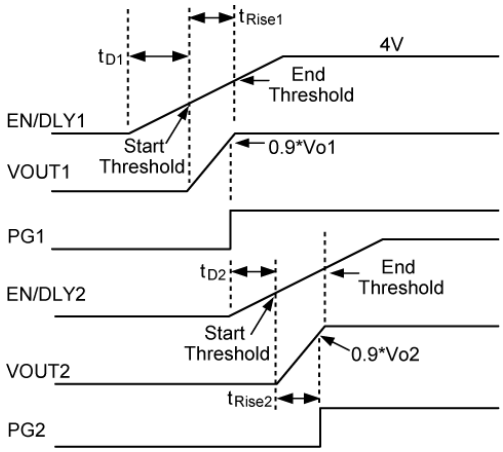


Figure 5. Output Sequencing Waveforms

The MIC25400 must start up without a pre-biased output voltage. During start up, the MIC25400 pulls the output to ground if it is above 0V. This may cause the output to ring below ground and excessive voltage on the VSW node. A pre-bias condition can occur if the output is turned off then immediately turned back on before the output capacitor is discharged to ground. It is also possible that the output of the MIC25400 could be pulled up or pre-biased through parasitic conduction paths from one supply rail to another in multiple voltage level ICs like a FPGA.

High-Side Drive

The internal high-side drive circuit is designed to switch the internal N-channel MOSFET. Figure 6 shows a diagram of the high-side MOSFET, gate drive and bootstrap circuit. D2 and C_{BST} comprise the bootstrap circuit, which supplies drive voltage to the high-side MOSFET. Bootstrap capacitor C_{BST} is charged through diode D2 when the low-side MOSFET turns on and pulls the SW pin voltage-to-ground. When the high-side MOSFET driver is turned on, energy from C_{BST} charges the MOSFET gate, turning it on. Voltage on the SW pin increases to approximately V_{IN}. Diode D2 is reversed biased and C_{BST} flies high while maintaining gate voltage on the high-side MOSFET.

A resistor should be added in series with the BST1 and BST2 pins. This will slow down the turn-on time of the high-side MOSFET while leaving the turn-off time unaffected. Slowing down the MOSFET rise time will reduce the turn-on overshoot at the switch node, which is important when operating with an input voltage close to the maximum operating voltage.

The recommended capacitor for CBST is a 0.01µF ceramic capacitor. The recommended value for RBST is 20Ω.

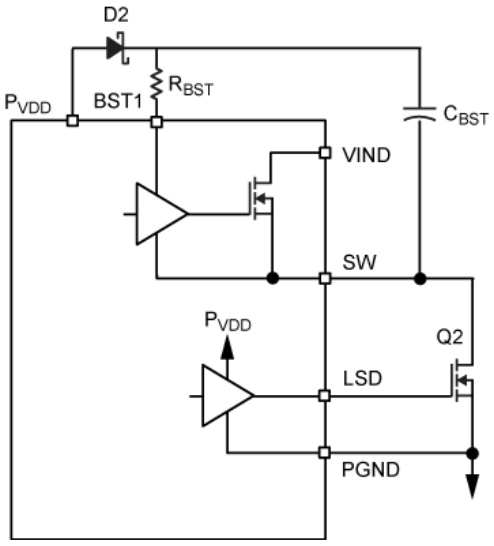


Figure 6. High-Side Drive Circuitry

Low-Side Drive Output

The LSD pin is used to drive an external MOSFET. This MOSFET is driven out of phase with the internal high-side MOSFET to conduct inductor current during the high-side MOSFETs off-time. Circuitry internal to the regulator prevents short circuit "shoot-through" current from flowing by preventing the high-side and low-side MOSFETs from conducting at the same time.

The low-side MOSFET gate voltage is supplied from V_{PVDD}. Turn off of the MOSFET is accomplished by discharging the gate through the LSD pin. The return path is through the PGND pin and back to the MOSFET's source pin. These circuit paths must be kept short to minimize noise. See the layout section of this datasheet for additional information.

Driving the low-side MOSFET on and off dissipates power in the MIC25400 regulator. The power can be calculated by the equation below:

$$P_{DRIVER} = Q_G \times V_{GS} \times f_S \quad \text{Eq. 3}$$

where:

- P_{DRIVER} is the power dissipated in the regulator by switching the MOSFET on and off.
- Q_G is the total Gate charge of the MOSFET at V_{GS}.
- V_{GS} is the MOSFET's Gate to Source voltage which is equal to the voltage on P_{VDD}.
- f_S is the switching frequency of the regulator (1MHz nominal).

dV/dT-Induced Turn-On of the Low-Side MOSFET

As the high-side MOSFET turns on, the rising dv/dt on the switch-node forces current through C_{GD} of the low-side MOSFET causing a glitch on its gate. Figure 7 demonstrates the basic mechanism causing this issue. If the glitch on the gate is greater than the MOSFET's turn-on threshold, it may cause an unwanted turn-on of the low-side MOSFET while the high-side MOSFET is on. A short circuit between input and ground would momentarily occur, which lowers efficiency and increases power dissipation in both FETs. Additionally, turning on the low-side FET during the off-time could interfere with overcurrent sensing.

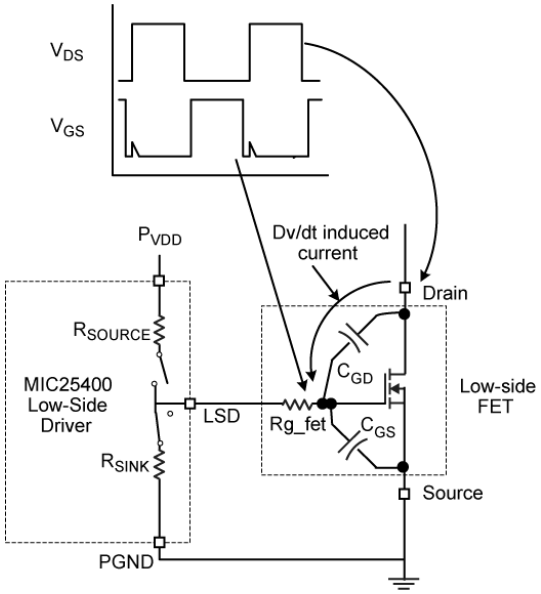


Figure 7. dv/dt-Induced Turn-On of the Low-Side MOSFET

The following steps can be taken to lower the gate drive impedance, minimize the dv/dt-induced current and lower the FET's susceptibility to the induced glitch:

- Chose a low-side MOSFET with a high C_{GS}/C_{GD} ratio and a low internal gate resistance
- Do not put a resistor between the LSD output and the gate.
- Insure both the gate drive and return etch are short, low inductance connections.
- Use a 4.5V V_{GS} rated MOSFET. Its higher gate threshold voltage is more immune to glitches than a 2.5V or 3.3V rated MOSFET. MOSFETs that are rated for operation at less than 4.5 V_{GS} should not be used.
- Add a resistor in series with the BST pin. This will slow down the turn-on time of the high-side MOSFET while leaving the turn-off time unaffected.

Current Limit

The MIC25400 uses the synchronous (low-side) MOSFET's RDS_{ON} to sense an over-current condition. The low-side MOSFET is used because it displays lower parasitic oscillations after switching than the upper MOSFET. Additionally, it improves the accuracy and reduces false tripping at lower voltage outputs and narrow duty cycles since the off-time increases as duty-cycle decreases. Figure 8 shows how over current protection is performed using the low-side MOSFET.

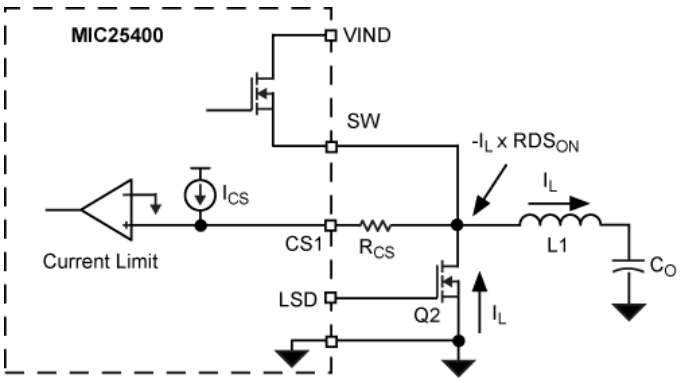


Figure 8. Overcurrent Circuit

Inductor current, I_L, flows from the lower MOSFET source to the drain during the off-time, causing the drain voltage to become negative with respect to ground. This negative voltage is proportional to the instantaneous inductor current times the MOSFET RDS_{ON}. The low-side MOSFET voltage becomes even more negative as the output current increases.

The over-current circuit operates by passing a known fixed current source through a resistor R_{CS}. This sets up an offset voltage (I_{CS} x R_{CS}) that is compared to the V_{DS} of the low-side FET. When I_{SD} (source-to-drain current) x RDS_{ON} is equal to this voltage the soft-start circuit is reset and a hiccup current mode is initiated to protect the power supply and load from excessive current during short circuits.

Current-Limit Calculations and Maximum Peak Limit

The current limit method requires careful selection of the inductor value and saturation current. If a short circuit occurs during the off-time, the overcurrent circuit will take up to a full cycle to detect the overcurrent once it exceeds the overcurrent limit. The worst case occurs if the output current is 0A and a hard short is applied to the output. The short circuit causes the output voltage to fall, which increases the pulse width of the regulator. It may take three or four cycles for the current to build up in the inductor before current limit forces the part into hiccup mode. The wider pulse width generates a larger peak to peak inductor current which can saturate the inductor.

For this reason, the minimum inductor value for the MIC25400 is 4.7µH and the maximum peak current-limit set point is 2.7A. The saturation current for each of these inductors should be at least 1.5A higher than the overcurrent limit setting.

Voltage Setting Components

The regulator requires two external resistors to set the output voltage as shown in Figure 9.

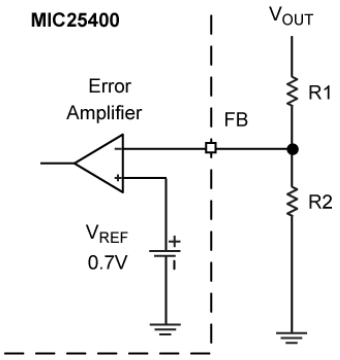


Figure 9. Setting the Output Voltage

The output voltage is determined by Equation 4.

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) \quad \text{Eq. 4}$$

where: V_{REF} is 0.7V nominal.

If the voltage divider resistance is used to provide the minimum load (see "EN/DLY" sub-section) then R1 should be low enough to provide the necessary impedance.

Once R1 is selected, R2 can be calculated with the following formula:

$$R2 = \frac{V_{REF} \times R1}{V_{OUT} - V_{REF}} \quad \text{Eq. 5}$$

Minimum Pulse Width

Output voltage is regulated by adjusting the on-time pulse width of the high-side FET. This is accomplished by comparing the error amplifier output with a sawtooth waveform (see Functional Diagram). The pulse width output of the comparator becomes smaller as the error amplifier voltage decreases. Due to propagation delay and other circuit limitations, there is a minimum pulse width at the output of the comparator. If the error amplifier voltage drops any further, then the output of the comparator will be low.

The PWM circuit will skip pulses if a smaller duty-cycle is required to maintain output voltage regulation. This effectively cuts the output frequency in half.

Thermal Protection

The internal temperature of the regulator is monitored to prevent damage to the device. Both outputs are inhibited from switching if the over-temperature threshold is exceeded. Hysteresis in the circuit allows the regulator to cool before turning back on.

Application Information

Component Selection

Inductor

The value of inductance is determined by the peak to peak inductor current. Higher values of inductance reduce the inductor current ripple at the expense of a larger inductor. Smaller inductance values allow faster response to output current transients but increase the output ripple voltage and require more output capacitance.

The inductor value and saturation current are also controlled by the method of overcurrent limit used (see explanation in the previous section). The minimum value of inductance for the MIC25400 is 4.7µH.

The peak-to-peak ripple current may be calculated using the Equation 6:

$$I_{PP} = \frac{V_{OUT} \cdot (\eta \cdot V_{IN(max)} - V_{OUT})}{\eta \cdot V_{IN(max)} \cdot f_S \cdot L} \quad \text{Eq. 6}$$

where:

- I_{PP} is the peak to peak inductor ripple current
- L is the value of inductance
- f_S is the switching frequency of the regulator
- η is the efficiency of the power supply

Efficiency values from the Functional Characteristics section can be used for these calculations.

The peak inductor current in each channel is equal to the average output current plus one half of the peak-to-peak inductor ripple current:

$$I_{PK} = I_{OUT} + 0.5 \times I_{PP} \quad \text{Eq. 7}$$

The RMS inductor current is used to calculate the I^2R losses in the inductor:

$$I_{INDUCTOR_{RMS}} = I_{OUT} \cdot \sqrt{1 + \frac{1}{3}\left(\frac{I_{PP}}{I_{OUT}}\right)^2} \quad \text{Eq. 8}$$

Maximizing efficiency requires the proper selection of core material and minimizing the winding resistance. The high-frequency operation of the MIC25400 requires the use of ferrite materials. Lower cost iron powder cores may be used but the increase in core loss will reduce the efficiency of the power supply. This is especially noticeable at low output power. The inductor winding resistance decreases efficiency at the higher output current levels. The winding resistance must be minimized although this usually comes at the expense of a larger inductor.

The power dissipated in the inductor equals the sum of the core and copper losses. Core loss information is usually available from the magnetics vendor.

Input Capacitor

A 10µF ceramic is suggested on each of the V_{IN} pins for bypassing. X5R or X7R dielectrics are recommended for the input capacitor. Y5V dielectrics should not be used. Besides losing most of their capacitance over temperature, they also become resistive at high frequencies, which reduce their ability to filter out high frequency noise.

Output Capacitor

The MIC25400 regulator is designed for ceramic output capacitors although tantalum and Aluminum Electrolytic may also be used.

Output ripple voltage is determined by the magnitude of inductor current ripple, the output capacitor's ESR and the value of output capacitance. When using ceramic output capacitors, the primary contributor to output ripple is the value of capacitance. Output ripple using ceramic capacitors may be calculated using Equation 9:

$$C_{OUT} \geq \frac{I_{PP}}{8 \cdot \Delta V_{OUT} \cdot 2 \cdot f_S} \quad \text{Eq. 9}$$

where:

- ΔV_{OUT} is the peak-to-peak output voltage ripple
- I_{PP} is the peak-to-peak ripple current as see by the capacitors
- f_S is the switching frequency (1MHz nominal).

When using tantalum or aluminum electrolytic capacitors, both the capacitance and ESR contribute to output ripple. The total ripple is calculated as shown in Equation 10:

$$\Delta V_{OUT} = \sqrt{\left[\frac{I_{PP}}{8 \cdot C_{OUT} \cdot 2 \cdot f_S}\right]^2 + \left[I_{PP} \cdot R_{ESR}\right]^2} \quad \text{Eq. 10}$$

The output capacitor RMS current is calculated by Equation 11:

$$I_{COUT_{RMS}} = \frac{I_{PP}}{\sqrt{12}} \quad \text{Eq. 11}$$

The power dissipated in the output capacitors can be calculated by Equation 12:

$$P_{DISS_{COUT}} = \left(I_{COUT_{RMS}}\right)^2 \cdot R_{ESR} \quad \text{Eq. 12}$$

Current-Limit Resistor

The current-limit circuit responds to the peak inductor current flowing through the low-side FET. Calculating the current setting resistor R_{CS} should take into account the peak inductor current and the blanking delay of approximately 100ns.

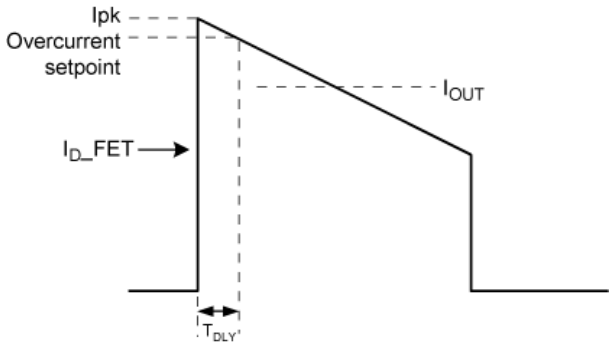


Figure 10. Overcurrent Waveform

Figure 10 shows the low-side MOSFET current waveform. Peak current is measured after a small delay. The equations used to calculate the current limit resistor value are illustrated in Equation 13:

$$I_{PK} = I_{OUT} + \frac{I_{PP}}{2}$$

$$I_{OC} = I_{PK} - \frac{V_{OUT} \cdot T_{DLY}}{L}$$

$$R_{CS} = \frac{I_{OC} \cdot RDS_{ON}}{I_{CS}} \quad \text{Eq. 13}$$

where:

- I_{OC} is the current-limit set point
- L = inductor value
- T_{DLY} = Current-limit blanking time ~ 100ns
- I_{CS} is the overcurrent pin sense current (200µA nominal)
- RDS_{ON} is the on resistance of the low-side MOSFET

Snubber

A snubber is used to damp out high frequency ringing caused by parasitic inductance and capacitance in the buck converter circuit. Figure 11 shows a simplified schematic of one of the buck converter phases. Stray capacitance consists mostly of the two MOSFET's output capacitance (C_{OSS}). The stray inductances are mostly package and etch inductance. The arrows show the resonant current path when the high-side MOSFET turns on. This ringing causes stress on the semiconductors in the circuit as well as increased EMI.

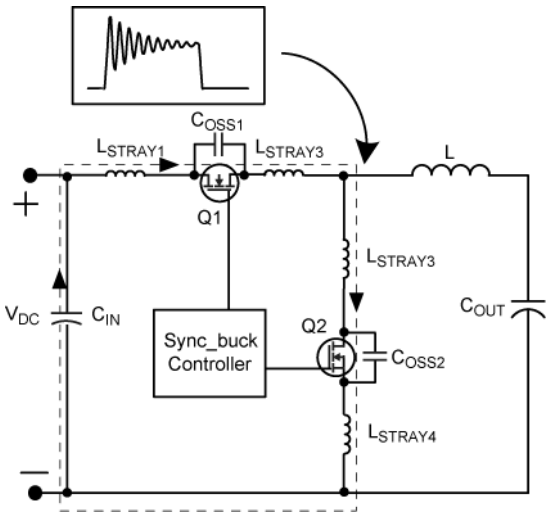


Figure 11. Output Parasitics

One method of reducing the ringing is to use a resistor to lower the Q of the resonant circuit. The circuit in Figure 12 shows an RC network connected between the switch node and ground. Capacitor C_S is used to block DC and minimize the power dissipation in the resistor. This capacitor value should be between five and ten times the parasitic capacitance of the MOSFET C_{OSS}. A capacitor that is too small will have high impedance and prevent the resistor from damping the ringing. A capacitor that is too large causes unnecessary power dissipation in the resistor, which lowers efficiency.

The snubber components should be placed as close as possible to the low-side MOSFET and/or external Schottky diode since in contributes to most of the stray capacitance. Placing the snubber too far from the FET or using an etch that is too long or too thin adds inductance to the snubber and diminishes its effectiveness.

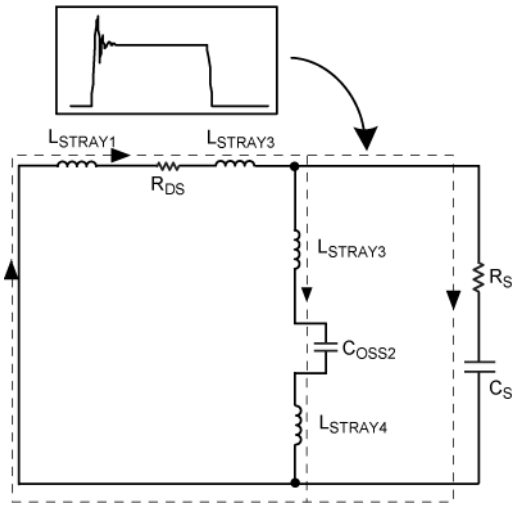


Figure 12. Snubber Circuit

Proper snubber design requires the parasitic inductance and capacitance be known. A method of determining these values and calculating the damping resistor value is outlined below.

1. Measure the ringing frequency at the switch node which is determined by parasitic L_P and C_P. Define this frequency as f_1.
2. Add a capacitor C_S (normally at least 3 times as big as the C_{OSS} of the FET) from the switch node-to-ground and measure the new ringing frequency. Define this new (lower) frequency as f_2. L_P and C_P can now be solved using the values of f_1, f_2 and C_S.
3. Add a resistor R_S in series with C_S to generate critical damping.

Step 1: First measure the ringing frequency on the switch node voltage when the high-side MOSFET turns on. This ringing is characterized by Equation 14:

$$f_1 = \frac{1}{2\pi\sqrt{L_P \cdot C_P}} \quad \text{Eq. 14}$$

where:

- C_P and L_P are the parasitic capacitance and inductance

Step 2: Add a capacitor, C_S, in parallel with the synchronous MOSFET, Q2. The capacitor value should be approximately three times the C_{OSS} of Q2. Measure the frequency of the switch node ringing, f_2:

$$f_2 = \frac{1}{2\pi\sqrt{L_P \cdot (C_S + C_P)}} \quad \text{Eq. 15}$$

Define f' as:

$$f' = \frac{f_1}{f_2} \quad \text{Eq. 16}$$

Combining the equations for f_1, f_2 and f' to derive C_P, the parasitic capacitance:

$$C_P = \frac{C_S}{2 \cdot (f')^2 - 1} \quad \text{Eq. 17}$$

L_P is solved by re-arranging the equation for f_1:

$$L_P = \frac{1}{(2\pi)^2 \cdot C_P \cdot (f_1)^2} \quad \text{Eq. 18}$$

Step 3: Calculate the damping resistor.

Critical damping occurs at Q = 1:

$$Q = \frac{1}{R_S}\sqrt{\frac{L_P}{C_S + C_P}} = 1 \quad \text{Eq. 19}$$

Solving for R_S:

$$R_S = \sqrt{\frac{L_P}{C_S + C_P}} \quad \text{Eq. 20}$$

Figure 12 shows the snubber in the circuit and the damped switch node waveform.

The snubber capacitor, C_S, is charged and discharged each switching cycle. The energy stored in C_S is dissipated by the snubber resistor, R_S, two times per switching period. This power is calculated in Equation 21:

$$P_{snubber} = f_S \cdot C_S \cdot V_{IN}^2 \quad \text{Eq. 21}$$

where:

- f_S is the switching frequency for each phase
- V_{IN} is the DC input voltage

Low-Side MOSFET Selection

An external N-channel logic level power MOSFET must be used for the low-side switch. The MOSFET gate-to-source drive voltage of the MIC25400 is regulated by an internal 5V regulator. Logic level MOSFETs, whose operation is specified at V_{GS} = 4.5V must be used. Use of MOSFETs with a lower specified V_{GS} (such as 3.3V or 2.5V) are not recommended since the low threshold can cause them to turn on when the high-side FET is turning on. When operating the regulator below a 6V input, connect V_{DD} to V_{IN} to prevent the V_{DD} regulator from dropping out.

Total gate charge is the charge required to turn the MOSFET on and off under specified operating conditions (V_{DS} and V_{GS}). The gate charge is supplied by the regulator's gate drive circuit. Gate charge is a source of power dissipation in the regulator due to the high switching frequencies. At low output load this power dissipation is noticeable as a reduction in efficiency.

The average current required to drive the MOSFETs is:

$$I_{DD} = Q_G \cdot f_S \quad \text{Eq. 22}$$

where:

- Q_G is the gate charge for both of the external MOSFETs. This information should be obtained from the manufacturer's data sheet.

Since current from the gate drive is supplied by the input voltage, power dissipated in the MIC25400 due to gate drive is:

$$P_{GATE\_DRIVE} = Q_G \cdot f_S \cdot V_{IN} \quad \text{Eq. 23}$$

Parameters that are important to MOSFET selection are:

- Voltage rating
- On resistance
- Total Gate Charge

The MOSFET is subjected to a V_{DS} equal to the input voltage. A safety factor of 20% should be added to the $V_{DS(max)}$ of the MOSFET to account for voltage spikes due to circuit parasitics. Generally, 30V MOSFETs are recommended for all applications since lower V_{DS} rated MOSFETs tend to have a V_{GS} rating that is lower than the recommended 4.5V.

RMS Current and MOSFET Power Dissipation Calculation

Switching loss in the low-side MOSFET can be neglected since it is turned on and off at a V_{DS} of 0V. The power dissipated in the MOSFET is mostly conduction loss during the on-time ($P_{CONDUCTION}$):

$$P_{CONDUCTION} = I_{SWITCH_{RMS}}^2 \cdot RDS_{ON} \quad \text{Eq. 24}$$

where:

- RDS_{ON} is the on resistance of the MOSFET switch.

The RMS value of the MOSFET current is:

$$I_{SW\_RMS} = \sqrt{(1-D)\cdot(I_{OUT\_MAX}{}^2 + \frac{I_{PP}{}^2}{12})} \quad \text{Eq. 25}$$

where:

- D is the duty-cycle of the converter

I_{PP} is the inductor ripple current:

$$D = \frac{V_{OUT}}{\eta \cdot V_{IN}} \quad \text{Eq. 26}$$

where:

- η is the efficiency of the converter.

External Schottky Diode

A freewheeling diode in parallel with the low-side FET is needed to maintain continuous inductor current flow while both MOSFETs are turned off (dead-time). Dead-time is necessary to prevent current from flowing unimpeded through both MOSFETs. An external Schottky diode is used to bypass the low-side MOSFET's parasitic body diode. An external diode improves efficiency due to its lower forward voltage drop as compared to the internal parasitic diode in the FET. It may also decrease high frequency noise because the Schottky diode junction does not suffer from reverse recovery.

An external Schottky diode conducts at a lower forward voltage preventing the body diode in the MOSFET from turning on. The lower forward voltage drop dissipates less power than the body diode. Depending on the circuit components and operating conditions, an external Schottky diode may give up to 1% improvement in efficiency.

Compensation

The voltage regulation, filter and power stage section is shown in Figure 13. The error amplifier regulates the output voltage and compensates the voltage regulation loop. It is a simplified type III compensator utilizing two compensating zeros and two poles. Figure 12 also shows the transfer function for each section.

Compensation is necessary to insure the control loop has adequate bandwidth and phase margin to properly respond to input voltage and output current transients. High gain at DC and low frequencies is needed for accurate output voltage regulation. Attenuation near the switching frequency prevents switching frequency noise from interfering with the control loop.

The output filter contains a complex double pole formed by the capacitor and inductor and a zero from the output capacitor and it's ESR. The transfer function of the filter is:

$$Gfilter(s) = \frac{1+\frac{s}{\omega z}}{1+\frac{s}{Q\ \omega o}+\frac{s}{\omega o}^2} \quad \text{Eq. 27}$$

where:

$$\omega z = \frac{1}{C_O \cdot R_{ESR}}$$

$$\omega o = \frac{1}{\sqrt{C_O \cdot L_O}}$$

$$Q = R \cdot \sqrt{\frac{C_O}{L}}$$

The modulator gain is proportional to the input voltage and inversely proportional to the internal ramp voltage generated by the oscillator. The peak-peak ramp voltage is 1V:

$$Gmod = \left(\frac{V_{IN}}{V_{RAMP}}\right) \quad \text{Eq. 28}$$

The output voltage divider attenuates V_{OUT} and feeds it back to the error amplifier. The divider gain is:

$$H = \frac{R4}{R1+R4} = \frac{V_{REF}}{V_{OUT}} \quad \text{Eq. 29}$$

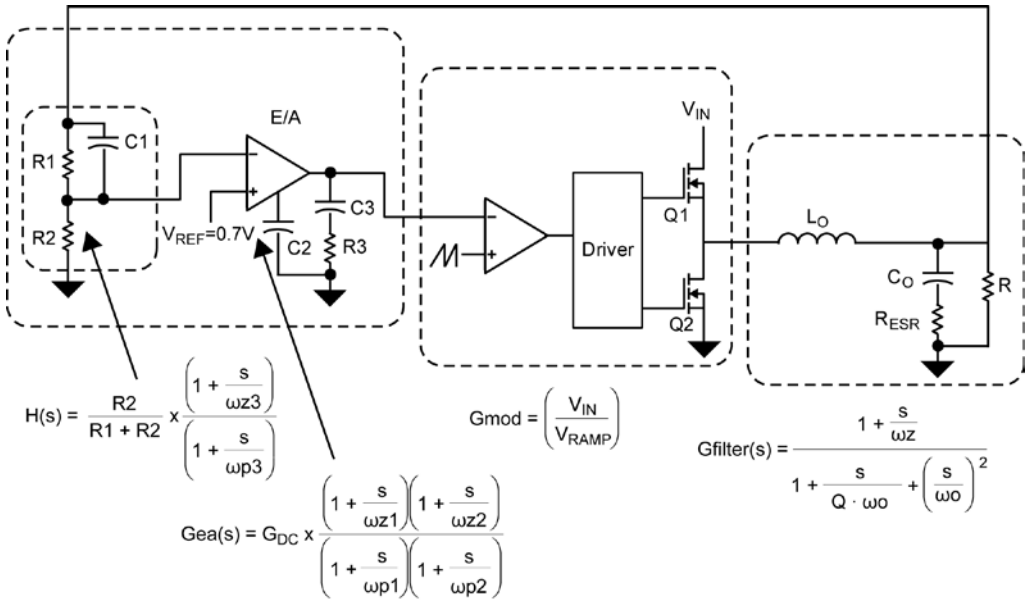


Figure 13. Voltage Loop and Transfer Functions

The modulator, filter and voltage divider gains can be multiplied together to show the open loop gain of these parts.

$$Gvd(s) = Gfilter(s) \cdot H \cdot Gmod \qquad \text{Eq. 30}$$

This transfer function is plotted in Figure 14. At low frequency, the transfer function gain equals the modulator gain times the voltage divider gain. As the frequency increases toward the LC filter resonant frequency, the gain starts to peak. The increase in the gain's amplitude equals Q. Just above the resonant frequency, the gain drops at a -40db/decade rate. The phase quickly drops from 0° to almost 180° before the phase boost of the zero brings it back up to -90°. Higher values of Q will cause the phase to drop quickly. In a well damped, low Q system the phase will change more slowly.

As the frequency approaches the zero frequency (f_Z) formed by C_O and its ESR, then the slope of the gain curve changes from -40db/dec. to -20db/dec and the phase increases. The zero causes a 90° phase boost. Ceramic capacitors, with their smaller values of capacitance and ESR, push the zero and its phase boost out to higher frequencies, which allow the phase lag from the LC filter to drop closer to -180°. The system will be close to being unstable if the overall open loop gain crosses 0dB while the phase is close to −180°.

Gvd Transfer Function

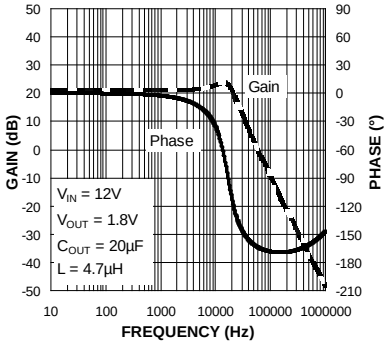


Figure 14. Gvd Transfer Function

If the output capacitance and/or ESR is high, the zero moves lower in frequency and helps to boost the phase, leading to a more stable system.

Error Amplifier Poles and Zeros

The error amplifier has internal poles and zeros that can be shifted in frequency with an external capacitor. The general form of the error amplifier compensation is shown in Equation 31:

$$Gea(s) = G_{DC} \times \frac{\left(1+\frac{s}{\omega z1}\right)\left(1+\frac{s}{\omega z2}\right)}{\left(1+\frac{s}{\omega p1}\right)\left(1+\frac{s}{\omega p2}\right)} \qquad \text{Eq. 31}$$

The G_{DC} is the DC gain of the error amplifier. It is internally set to 2500 (68dB).

As illustrated in Figure 13, there are two compensating zeros. ωz1 is internally set with R3 and C3. The zero frequency is fixed at a nominal 16kHz in the MIC25400. The second zero, ωz2, is set by the external capacitor, C2.

For the MIC25400:

$$R3 = 100k$$

$$C3 = 100pf$$

$$fz1 = \frac{1}{2 \times \pi \times R3 \times C3} = 16kHz$$

$$fz2 = \frac{1}{2 \times \pi \times 21 \cdot 10^3 \times C2}$$

The two compensating pole frequencies are shown below.

$$fp1 = 250Hz$$

$$fp2 = \frac{1}{2 \times \pi \times 12 \cdot 10^3 \times C2}$$

fp2 and fz2 both depend on the value of C2 and are proportionally spaced in frequency with the zero at a lower frequency than the pole. This provides gain and phase boost in the control loop.

Voltage Divider Feed-Forward Capacitor

The capacitor across the upper voltage divider resistor boosts the gain and phase of the control loop by short circuiting the high-side resistor at higher frequencies. The capacitor and upper resistor form a zero at a lower frequency. The capacitor and parallel combination of upper and lower resistors form a pole at a higher frequency. This phase boost circuit is most effective at higher output voltages, where there is a larger attenuation from the voltage divider resistors.

The general form of the feed-forward circuit is illustrated in Equation 32.

$$H(s) = \frac{R2}{R1+R2} \times \frac{\left(1+\frac{s}{\omega z3}\right)}{\left(1+\frac{s}{\omega p3}\right)} \qquad \text{Eq. 32}$$

where:

$$fz3 = \frac{1}{2 \times \pi \times R1 \times C1}$$

$$fp3 = \frac{1}{2 \times \pi \times C1 \times \left(\frac{R1 \times R2}{R1+R2}\right)}$$

The total open loop transfer function is:

$$T(s) = Gea(s) \times Gmod \times Gfilter(s) \times H(s)$$

Table 1 list the recommended values of compensation and filter components for different output voltages. The output capacitors are ceramic.

Table 1. Recommended Compensation Values and Filter Components for MIC25400

VIN	VOUT	R1	R2	C2	C1	Lo	Co
12V	1.0V	1k	2.32k	47pF	1.5nF	4.7µH	22µF
12V	1.2V	1k	1.4k	47pF	1.5nF	4.7µH	22µF
12V	1.4V	1k	1k	47pF	1.5nF	4.7µH	22µF
12V	1.8V	1k	634	47pF	1.5nF	4.7µH	22µF
12V	2.5V	1k	383	47pF	3.3nF	4.7µH	22µF
12V	3.3V	1k	274	68pF	3.3nF	4.7µH	22µF
12V	5.0V	1k	162	68pF	3.3nF	4.7µH	22µF

PCB Layout Guidelines

Warning!!! To minimize EMI and output noise, follow these layout recommendations.

PCB Layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths.

The following guidelines should be followed to insure proper operation of the MIC25400 converter.

IC

- Place the IC and the external Low-side MOSFET close to the point of load (POL).
- Use fat traces to route the input and output power lines.
- The exposed pad (EP) on the bottom of the IC must be connected to the ground.
- Use several vias to connect the EP to the ground plane on layer 2.
- Signal and power grounds should be kept separate and connected at only one location, the EP ground of the package.
- The following signals and their components should be decoupled or referenced to the power ground plane: VIND1, VIND2, PVDD, PGND1, PGND2, LSD1, and LSD2.
- These analog signals should be referenced or decoupled to the analog ground plane: VIN, EN/DLY1, EN/DLY2, COMP1, COMP2, FB1, and FB2.
- Place the overcurrent sense resistor close to the CS1 or CS2 pins. The trace coming from the switch node to this resistor has high dv/dt and should be routed away from other noise sensitive components and traces. Avoid routing this trace under the inductor to prevent noise from coupling into the signal.

Input Capacitor

- Place the input capacitor next. Ceramic capacitors must be placed between VIND1 and PGND1 and between VIND2 and PGND2.
- Place the input capacitors on the same side of the board and as close to the IC and low-side MOSFET as possible.
- Keep both the VIN and PGND connections short.
- Place several vias to the ground plane close to the input capacitor ground terminal, but not between the input capacitors and IC pins.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor.
- If a Tantalum input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage must be derated by 50%.
- In “Hot-Plug” applications, a Tantalum or Electrolytic bypass capacitor must be used to limit the over-voltage spike seen on the input supply with power is suddenly applied. The value must be sufficiently large to prevent this voltage spike from exceeding the maximum voltage rating of the MIC25400.
- An additional Tantalum or Electrolytic bypass input capacitor of 22µF or higher is required at the input power connection.

Inductor

- Keep the inductor connection to the switch node (SW) short.
- Do not route any digital or analog signal lines underneath or close to the inductor.
- Keep the switch node (SW) away from the feedback (FB) pin.
- To minimize noise, place a ground plane underneath the inductor.

Output Capacitor

- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- Phase margin will change as the output capacitor value and ESR changes. Contact the factory if the output capacitor is different from what is shown in the BOM.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high current load trace can degrade the DC load regulation.
- If 0603 package ceramic output capacitors are used, then make sure that it has enough capacitance at the desired output voltage. Please refer to the capacitor datasheet for more details.

Diode

- The external Schottky diode is placed next to the low-side MOSFET.
- The connection from the Schottky diode’s anode to the input capacitors ground terminal must be as short as possible.
- The diode’s cathode connection to the switch node (SW) must be keep as short as possible.

PCB Layout Guidelines (Continued)

RC Snubber

- Place the RC snubber on the same side of the board and as close as possible to the low-side MOSFET.

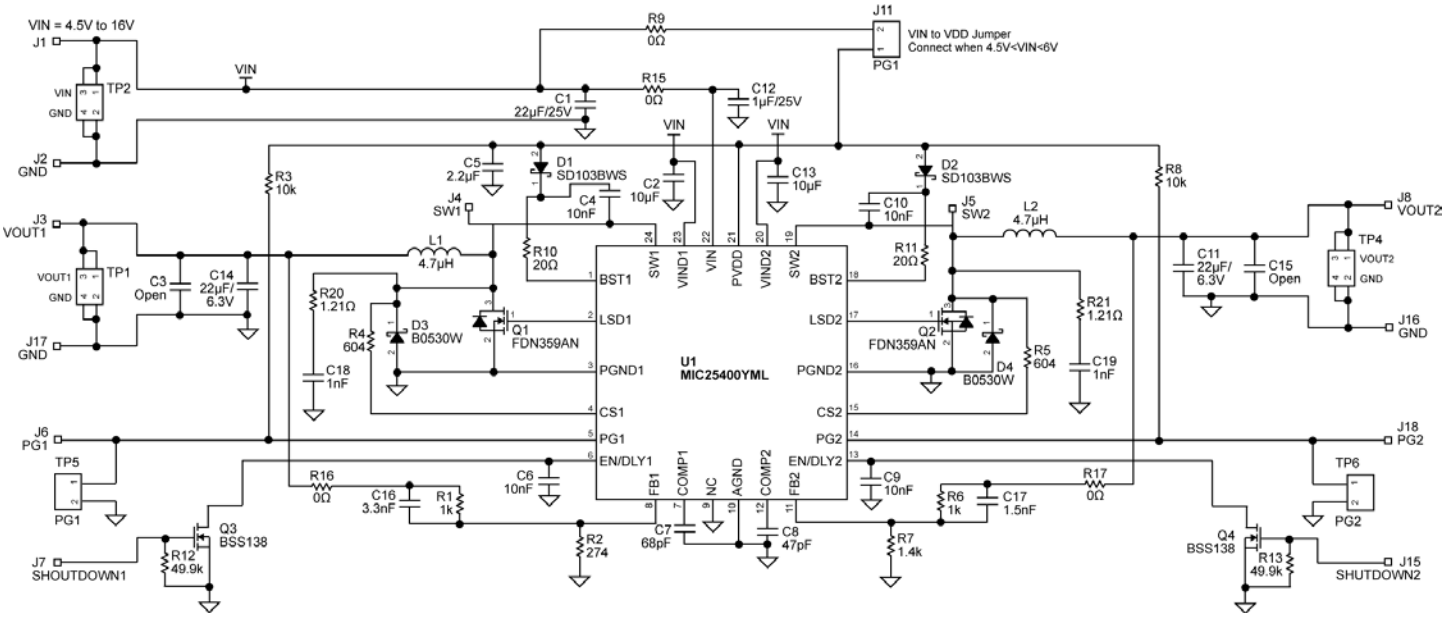
Low-Side MOSFET

- Low-side drive MOSFET traces (LSD pin-to- MOSFET gate pin) must be short and routed over a ground plane. The ground plane should be the connection between the MOSFET source and PGND.
- Chose a low-side MOSFET with a high CGS/CGD ratio and a low internal gate resistance to minimize the effect of dv/dt-inducted turn-on.
- Do not put a resistor between the LSD output and the gate.
- Use a 4.5V Vgs-rated MOSFET. Its higher gate threshold voltage is more immune to glitches than a 2.5V or 3.3V rated MOSFET. MOSFETs that are rated for operation at less than $4.5V_{GS}$ should not be used.

High-Side MOSFET

- Add a 20Ω resistor in series with the boost pin. This will slow down the turn-on time of the high-side MOSFET while leaving the turn-off time unaffected.

MIC25400 Evaluation Board Schematic



Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1	12103D226MAT2A	AVX[6]	Ceramic Capacitor, 22µF, 25V, X5R	1
C2, C13	12063D106MAT2A	AVX	Ceramic Capacitor, 10µF, 25V, X5R	2
C4, C10, C6, C9	06033D103MAT2A	AVX	Ceramic Capacitor, 10nF, 25V	4
C5	08056D225MAT2A	AVX	Ceramic Capacitor, 2.2µF, 6.3V	1
C7	VJ0603Y680KXXMB	Vitramon[7]	Ceramic Capacitor, 68pF, 50V, X7R	1
C8	VJ0603Y470KXXMB	Vitramon	Ceramic Capacitor, 47pF, 50V, X7R	1
C11, C14	08056D226MAT2A	AVX	Ceramic Capacitor, 22µF, 6.3V, X5R	2
C12	06033D105MAT2A	AVX	Ceramic Capacitor, 1µF, 25V	1
C16	VJ0603Y332KXXMB	Vitramon	Ceramic Capacitor, 3.3nF, 50V, X7R	1
C17	VJ0603Y152KXXMB	Vitramon	Ceramic Capacitor, 1.5nF, 50V, X7R	1
C18, C19	VJ0603Y102KXXMB	Vitramon	Ceramic Capacitor, 1nF, 50V, X7R	2

Notes:

6. AVX: www.avx.com.
7. Vishay: www.vishay.com.

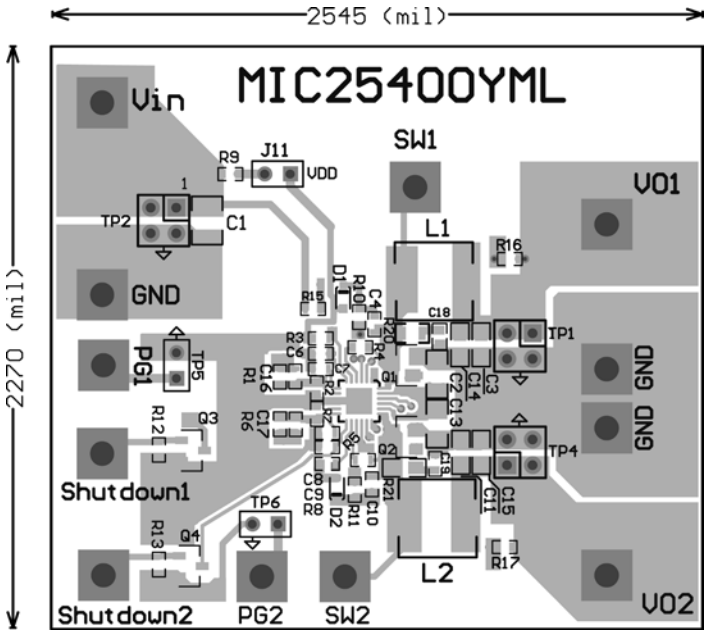
Bill of Materials (Continued)

Item	Part Number	Manufacturer	Description	Qty.
D1, D2	SD103BWS	Vishay[7]	Schottky Diode, 100mA, 30V	2
D3, D4	B0530W	Diodes. Inc[8]	Schottky Diode, 30V, 0.5A	2
L1, L2	DR74-4R7-R	Cooper[9]	Inductor, 4.7µH, 4.3A	2
R1, R6	CRCW06031001FRT1	Vishay Dale[7]	Resistor, 1k (0603 size), 1%	4
R2	CRCW06032740FRT1	Vishay Dale	Resistor, 274 (0603 size), 1%	1
R3, R8	CRCW06031002FRT1	Vishay Dale	Resistor, 10k (0603 size), 1%	4
R4, R5	CRCW06036040FRT1	Vishay Dale	Resistor, 604 (0603 size), 1%	2
R7	CRCW06031401FRT1	Vishay Dale	Resistor, 1.4k (0603 size), 1%	1
R9, R10	CRCW060320R0FRT1	Vishay Dale	Resistor, 20 (0603 size), 1%	2
R12, R13	CRCW06034992FRT1	Vishay Dale	Resistor, 49.9k (0603 size), 1%	2
R15, R16, R17	CRCW06030000FRT1	Vishay Dale	Resistor, 0Ω (0603 size)	3
R20, R21	CRCW08051R21FRT1	Vishay Dale	Resistor, 1.21Ω (0805 size), 1%	2
Q1, Q2	FDN359AN	Fairchild[10]	MOSFET	2
Q3, Q4	BSS138	Fairchild	MOSFET	2
U1	MIC25400YML	**Micrel, Inc.**[11]	**2A Dual Output PWM Synchronous Buck Regulator IC**	**1**

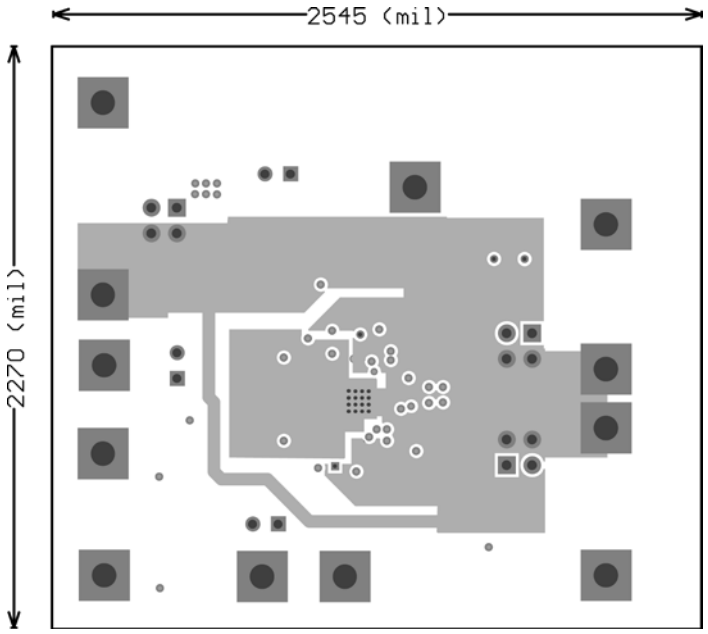
Notes:

8. Diodes, Inc.: www.diodes.com.
9. Cooper Magnetics: www.cooperet.com.
10. Fairchild Semiconductor: www.fairchildsemi.com.
11. Micrel, Inc.: www.micrel.com.

PCB Layout Recommendations

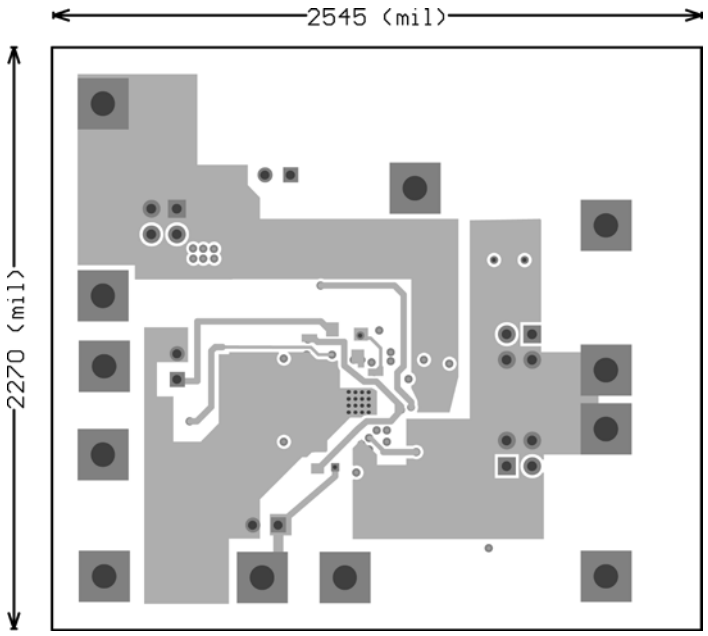


Top Layer

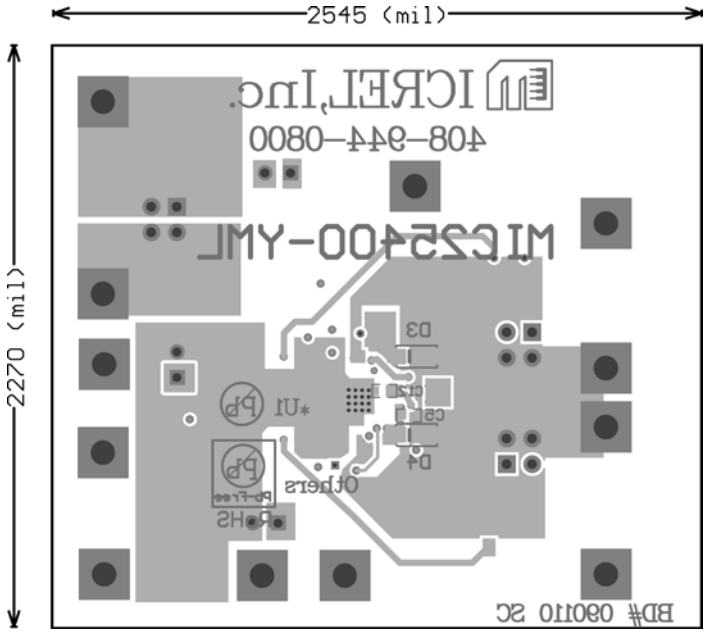


Mid Layer 1

PCB Layout Recommendations (Continued)

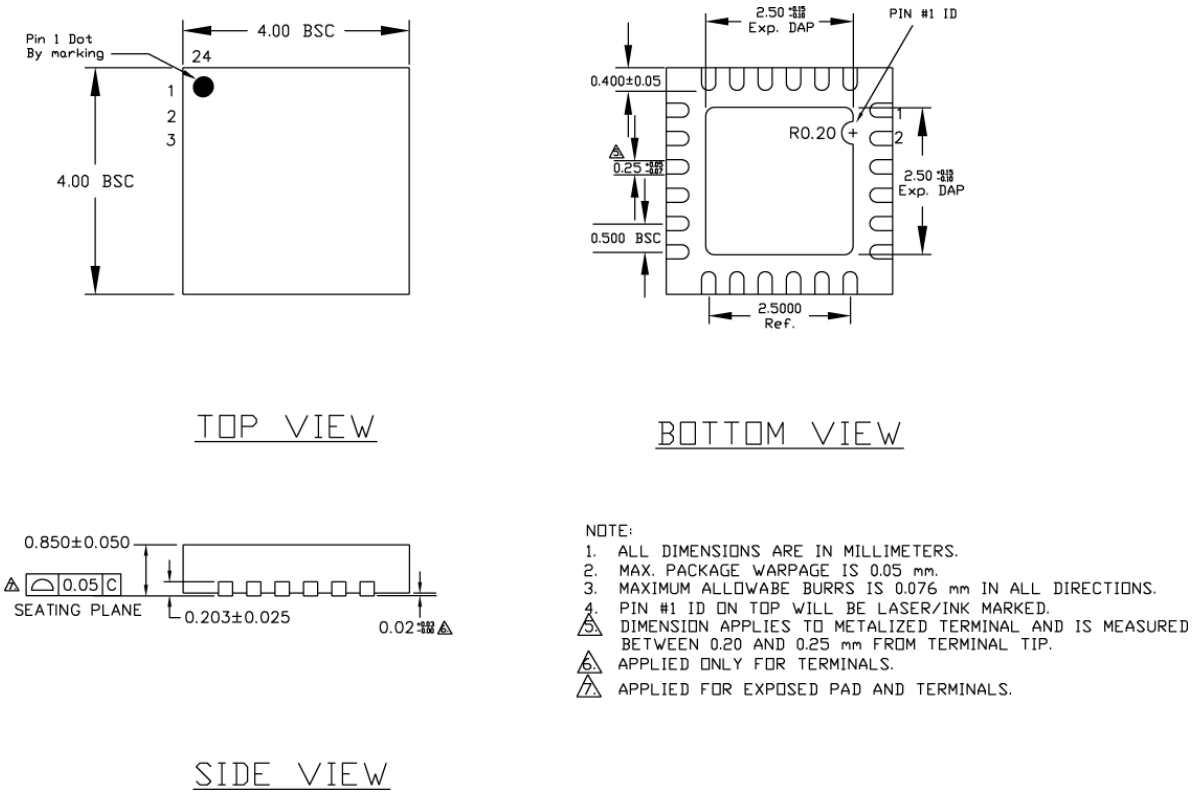


Mid Layer 2



Bottom Layer

Package Information[12]

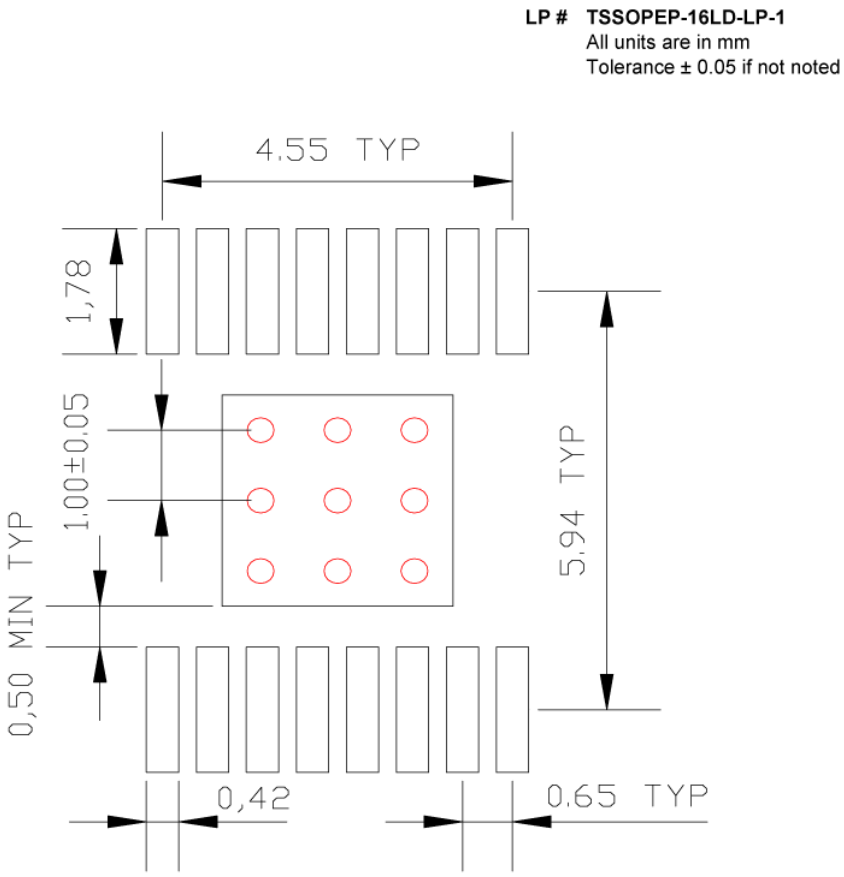


24-Pin 4mm × 4mm MLF (ML)

Note:

12. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

Recommended Landing Pattern



Red circle indicates Thermal Via. Size should be .300-.350 mm in diameter and it should be connected to GND plane for maximum thermal performance.

24-Pin 4mm × 4mm MLF (ML)

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