THE DATASHEET OF

MFRC52302HN1,151

www.win-source.net 0086-755-83957316

MFRC523

Standard performance ISO/IEC 14443 A/B frontend

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115242

Product data sheet
COMPANY PUBLIC

1. Introduction

This document describes the functionality and electrical specifications of the contactless reader/writer MFRC523.

1.1 Different available versions

The MFRC523 is available in two versions:

- MFRC52302 (HVQFN32), hereafter named as version 2.0
- MFRC52301 (HVQFN32), hereafter named as version 1.0

The differences of the version 1.0 to the version 2.0 are summarized in Section 11.

2. General description

The MFRC523 is a highly integrated reader/writer for contactless communication at 13.56 MHz. The MFRC523 reader supports ISO/IEC 14443 A/MIFARE mode.

The MFRC523's internal transmitter is able to drive a reader/writer antenna designed to communicate with ISO/IEC 14443 A/MIFARE cards and transponders without additional active circuitry. The receiver module provides a robust and efficient implementation for demodulating and decoding signals from ISO/IEC 14443 A/MIFARE compatible cards and transponders. The digital module manages the complete ISO/IEC 14443 A framing and error detection (parity and CRC) functionality.

All protocol layers of the ISO/IEC 14443 A and ISO/IEC 14443 B communication standards are supported:

- additional components, such as the oscillator, power supply, coil etc are correctly applied
- standardized protocols, such as ISO/IEC 14443-4 and/or ISO/IEC 14443 B anticollision are correctly implemented

The MFRC523 supports contactless communication using MIFARE higher baud rates (see Section 8.3.4.11 on page 22) at transfer speeds up to 848 kBd in both directions.

The following host interfaces are provided:

- Serial Peripheral Interface (SPI)
- Serial UART (similar to RS232 with voltage levels dependent on pin voltage supply)
- I^2C-bus interface

3. Features and benefits

- Highly integrated analog circuitry to demodulate and decode responses
- Buffered output drivers for connecting an antenna with the minimum number of external components
- Supports ISO/IEC 14443 A/MIFARE
- Supports ISO/IEC 14443 B Read/Write modes
- Typical operating distance in Read/Write mode up to 50 mm depending on the antenna size and tuning
- Supports MIFARE Mini, MIFARE 1K and MIFARE 4K encryption in Read/Write mode
- Supports ISO/IEC 14443 A higher transfer speed communication at 212 kBd, 424 kBd and 848 kBd
- Supports MFIN/MFOUT
- Additional internal power supply to the smart card IC connected via MFIN/MFOUT
- Supported host interfaces
  - SPI up to 10 Mbit/s
  - I^2C-bus interface up to 400 kBd in Fast mode, up to 3400 kBd in High-speed mode
  - RS232 Serial UART up to 1228.8 kBd, with voltage levels dependant on pin voltage supply
- FIFO buffer handles 64 byte send and receive
- Flexible interrupt modes
- Hard reset with low power function
- Power-down by software mode
- Programmable timer
- Internal oscillator for connection to 27.12 MHz quartz crystal
- 2.5 V to 3.3 V power supply
- CRC coprocessor
- Programmable I/O pins
- Internal self-test

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	analog supply voltage	$V_{DD(PVDD)} \leq V_{DDA} = V_{DDD} = V_{DD(TVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V	[1][2]	2.5	3.3	3.6	V
V_{DDD}	digital supply voltage			2.5	3.3	3.6	V
$V_{DD(TVDD)}$	TVDD supply voltage			2.5	3.3	3.6	V
$V_{DD(PVDD)}$	PVDD supply voltage		[3]	1.6	1.8	3.6	V
$V_{DD(SVDD)}$	SVDD supply voltage	$V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V		1.6	-	3.6	V
I_{pd}	power-down current	$V_{DDA} = V_{DDD} = V_{DD(TVDD)} = V_{DD(PVDD)} = 3$ V					
		hard power-down; pin NRSTPD set LOW	[4]	-	-	5	µA
		soft power-down; RF level detector on	[4]	-	-	10	µA
I_{DDD}	digital supply current	pin DVDD; $V_{DDD} = 3$ V		-	6.5	9	mA

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Table 1. Quick reference data *...continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DDA}	analog supply current	pin AVDD; V_{DDA} = 3 V, CommandReg register's RcvOff bit = 0		-	7	10	mA
		pin AVDD; receiver switched off; V_{DDA} = 3 V, CommandReg register's RcvOff bit = 1		-	3	5	mA
$I_{DD(PVDD)}$	PVDD supply current	pin PVDD	[5]	-	-	40	mA
$I_{DD(TVDD)}$	TVDD supply current	pin TVDD; continuous wave	[6][7][8]	-	60	100	mA
T_{amb}	ambient temperature	HVQFN32		−25	-	+85	°C

[1] Supply voltages below 3 V reduce the performance in, for example, the achievable operating distance.

[2] V_{DDA}, V_{DDD} and $V_{DD(TVDD)}$ must always be the same voltage.

[3] $V_{DD(PVDD)}$ must always be the same or lower voltage than V_{DDD}.

[4] I_{pd} is the total current for all supplies.

[5] $I_{DD(PVDD)}$ depends on the overall load at the digital pins.

[6] $I_{DD(TVDD)}$ depends on $V_{DD(TVDD)}$ and the external circuit connected to pins TX1 and TX2.

[7] During typical circuit operation, the overall current is below 100 mA.

[8] Typical value using a complementary driver configuration and an antenna matched to 40 Ω between pins TX1 and TX2 at 13.56 MHz.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
MFRC52302HN1/TRAYB[1]	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminal; body 5 × 5 × 0.85 mm	SOT617-1
MFRC52302HN1/TRAYBM[2]	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminal; body 5 × 5 × 0.85 mm	SOT617-1
MFRC52301HN1/TRAYB[1]	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminal; body 5 × 5 × 0.85 mm	SOT617-1
MFRC52301HN1/TRAYBM[2]	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminal; body 5 × 5 × 0.85 mm	SOT617-1

[1] Delivered in one tray.

[2] Delivered in five trays.

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6. Block diagram

The analog interface manages the modulation and demodulation of the analog signals. The contactless UART manages the protocol requirements for the communication protocols in cooperation with the host. The FIFO buffer ensures fast and convenient data transfers to/from the host and the contactless UART.

Various host interfaces are implemented to meet different customer requirements.

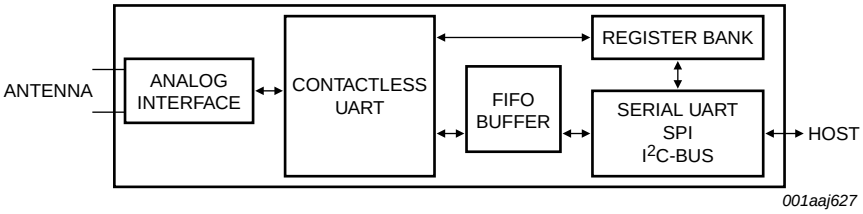

Fig 1. Simplified block diagram of the MFRC523

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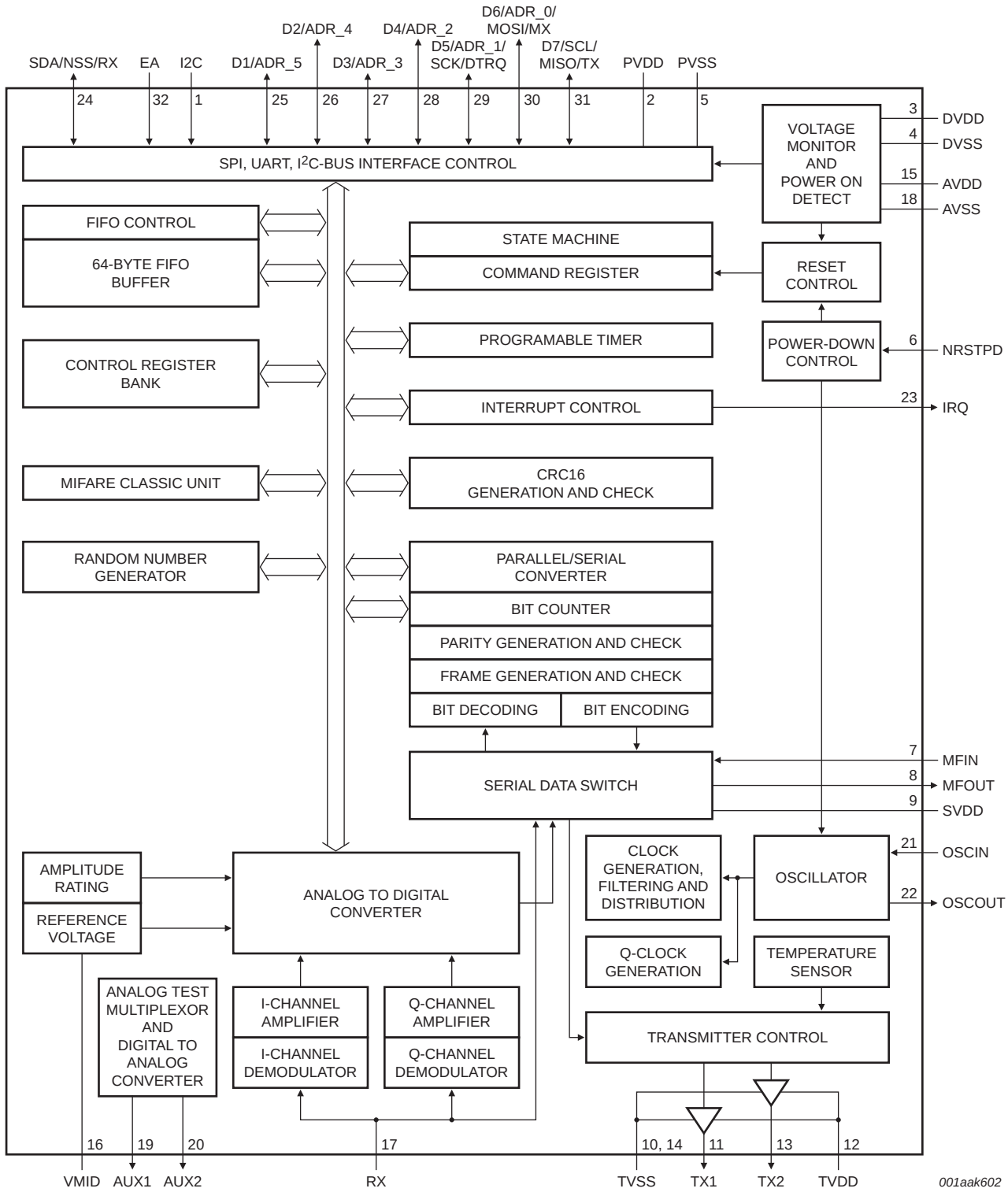

Fig 2. Detailed block diagram of the MFRC523

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7. Pinning information

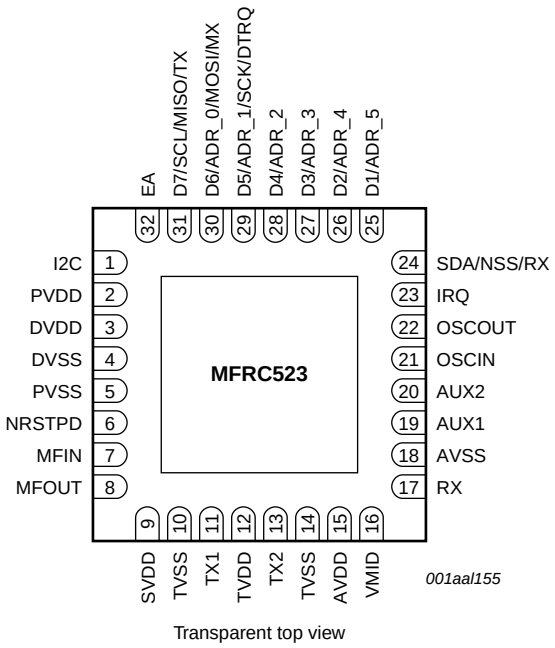

Fig 3. Pinning configuration HVQFN32 (SOT617-1)

7.1 Pin description

Table 3. Pin description

Pin	Symbol	Type[1]	Description
1	I2C	I[2]	I^2C-bus enable input
2	PVDD	P	pin power supply
3	DVDD	P	digital power supply
4	DVSS	G[3]	digital ground
5	PVSS	G	pin power supply ground
6	NRSTPD	I	reset and power-down input: reset: enabled by a positive edge power-down: enabled when LOW; internal current sinks are switched off, the oscillator is inhibited and the input pins are disconnected from the outside world
7	MFIN	I	MIFARE signal input
8	MFOUT	O	MIFARE signal output
9	SVDD	P	MFIN and MFOUT pin power supply
10	TVSS	G	transmitter output stage 1 ground
11	TX1	O	transmitter 1 modulated 13.56 MHz energy carrier output
12	TVDD	P	transmitter power supply: supplies the output stage of transmitters 1 and 2
13	TX2	O	transmitter 2 modulated 13.56 MHz energy carrier output
14	TVSS	G	transmitter output stage 2 ground
15	AVDD	P	analog power supply

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Table 3. Pin description *…continued*

Pin	Symbol	Type[1]	Description
16	VMID	P	internal reference voltage
17	RX	I	RF signal input
18	AVSS	G	analog ground
19	AUX1	O	auxiliary outputs for test purposes
20	AUX2	O	auxiliary outputs for test purposes
21	OSCIN	I	crystal oscillator inverting amplifier input; also the input for an externally generated clock (f_{clk} = 27.12 MHz)
22	OSCOUT	O	crystal oscillator inverting amplifier output
23	IRQ	O	interrupt request output: indicates an interrupt event
24	SDA[2]	I/O	I^2C-bus serial data line input/output
	NSS[2]	I	SPI signal input
	RX[2]	I	UART address input
25	D1[2]	I/O	test port
	ADR_5[2]	I/O	I^2C-bus address 5 input
26	D2	I/O	test port
	ADR_4[2]	I	I^2C-bus address 4 input
27	D3	I/O	test port
	ADR_3[2]	I	I^2C-bus address 3 input
28	D4	I/O	test port
	ADR_2[2]	I	I^2C-bus address 2 input
29	D5	I/O	test port
	ADR_1[2]	I	I^2C-bus address 1 input
	SCK[2]	I	SPI serial clock input
	DTRQ[2]	O	UART request to send output to microcontroller
30	D6	I/O	test port
	ADR_0[2]	I	I^2C-bus address 0 input
	MOSI[2]	I/O	SPI master out, slave in
	MX[2]	O	UART output to microcontroller
31	D7	I/O	test port
	SCL[2]	I/O	I^2C-bus clock input/output
	MISO[2]	I/O	SPI master in, slave out
	TX[2]	O	UART data output to microcontroller
32	EA[2]	I	external address input for coding I^2C-bus address

[1] Pin types: I = Input, O = Output, I/O = Input/Output, P = Power and G = Ground.

[2] The pin functionality of these pins is explained in Section 8.3 “Digital interfaces”.

[3] Connection of heatsink pad on package underside is not necessary. Optional connection to pin DVSS is possible.

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8. Functional description

The MFRC523 transmission module supports ISO/IEC 14443 A and ISO/IEC 14443 B Read/Write mode at various transfer speeds and modulation protocols.

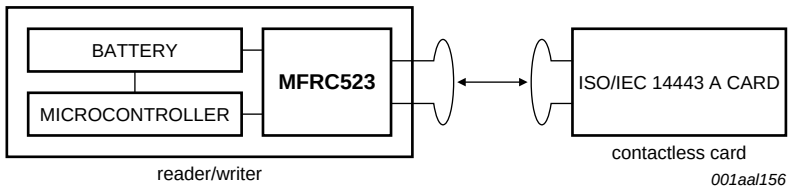
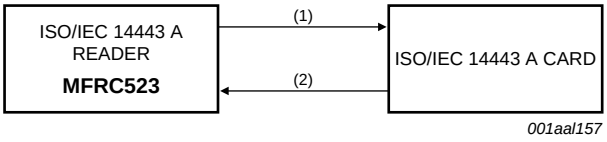


Fig 4. MFRC523 Read/Write mode

8.1 ISO/IEC 14443 A functionality

The physical level communication is shown in Figure 5.



(1) Reader to card (MFRC523 sends data to a card).

(2) Card to reader (card sends data to the MFRC523).

Fig 5. ISO/IEC 14443 A/MIFARE Read/Write mode communication diagram

The physical parameters are described in Table 4.

Table 4. Communication overview for ISO/IEC 14443 A reader/writer

Communication direction	Signal type	Transfer speed			
		106 kBd	212 kBd	424 kBd	848 kBd
Reader to card (MFRC523 sends data to a card)	reader side modulation	100 % ASK	100 % ASK	100 % ASK	100 % ASK
	bit encoding	modified Miller encoding	modified Miller encoding	modified Miller encoding	modified Miller encoding
	bit length	128 (13.56 µs)	64 (13.56 µs)	32 (13.56 µs)	16 (13.56 µs)
Card to reader (card sends data to the MFRC523)	card side modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56 MHz / 16	13.56 MHz / 16	13.56 MHz / 16	13.56 MHz / 16
	bit encoding	Manchester encoding	BPSK	BPSK	BPSK

The MFRC523's contactless UART and dedicated external host must manage the ISO/IEC 14443 A protocol. Figure 6 shows the data coding and framing according to ISO/IEC 14443 A.

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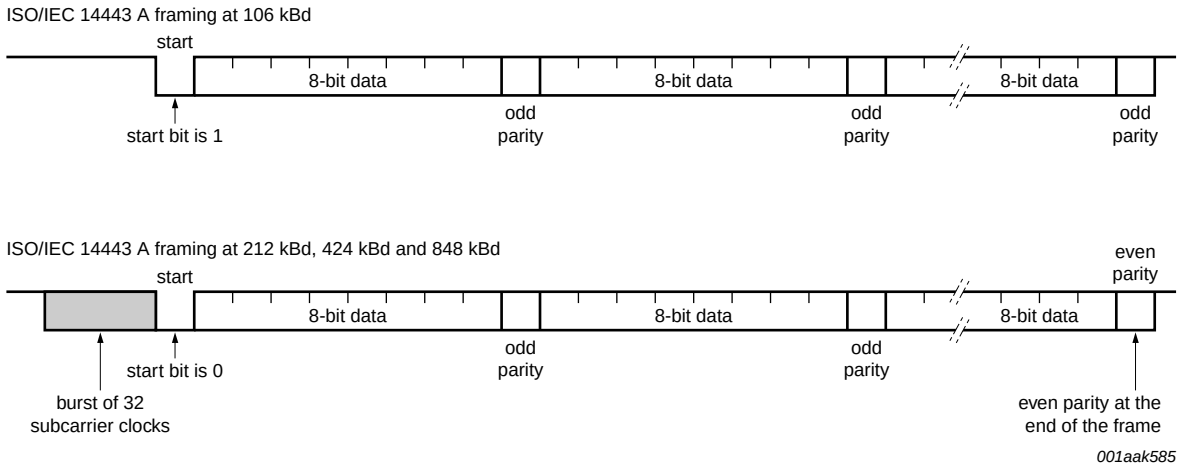

Fig 6. Data coding and framing according to ISO/IEC 14443 A

The internal CRC coprocessor calculates the CRC value based on ISO/IEC 14443 A part 3 and handles parity generation internally based on the transfer speed. Automatic parity generation can be switched off using the ManualRCVReg register's ParityDisable bit.

8.2 ISO/IEC 14443 B functionality

The MFRC523 reader IC fully supports the ISO 14443 international standard which includes the communication schemes ISO 14443 A and ISO 14443 B. Refer to the ISO 14443 reference documents *Identification cards - Contactless integrated circuit cards - Proximity cards* (parts 1 to 4).

8.3 Digital interfaces

8.3.1 Automatic microcontroller interface detection

The MFRC523 supports direct interfacing to hosts using SPI, I^2C-bus or serial UART interfaces. The MFRC523 resets its interface and checks the current host interface type automatically after performing a power-on or hard reset.

The MFRC523 identifies the host interface by sensing the logic levels on the control pins after the reset phase. This is done using a combination of fixed pin connections. Table 5 shows the different pin connection configurations.

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Table 5. Connection protocol for detecting different interface types

Pin	Interface type		
	UART (input)	SPI (output)	I²C-bus (I/O)
SDA	RX	NSS	SDA
I2C	0	0	1
EA	0	1	EA
D7	TX	MISO	SCL
D6	MX	MOSI	ADR_0
D5	DTRQ	SCK	ADR_1
D4	-	-	ADR_2
D3	-	-	ADR_3
D2	-	-	ADR_4
D1	-	-	ADR_5

8.3.2 Serial Peripheral Interface

The 5-wire Serial Peripheral Interface (SPI) is supported and enables high-speed communication with the host. The interface can manage data speeds up to 10 Mbit/s. When communicating with a host, the MFRC523 acts as a slave. As such, it receives data from the external host for register settings, sends and receives data relevant for RF interface communication.

An interface compatible with SPI enables high-speed serial communication between the MFRC523 and a microcontroller. The implemented interface meets with the SPI standard.

The timing specification is given in Section 15.1 on page 78.

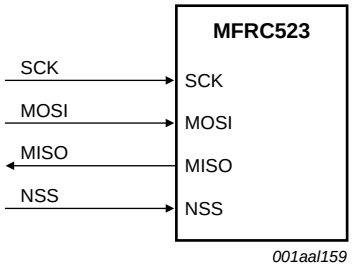

Fig 7. SPI connection to host

The MFRC523 acts as a slave during SPI communication and is timed using the SPI clock signal (SCK) generated by the master. Data communication from the master to the slave uses the MOSI line. The MISO line is used to send data from the MFRC523 to the master.

Data bytes on both MOSI and MISO lines are sent with the MSB first. Data on both MOSI and MISO lines must be stable on the rising edge of the clock and can be changed on the falling edge. Data is sent by the MFRC523 on the falling clock edge and is stable during the rising clock edge.

8.3.2.1 SPI read data

Reading data using SPI requires the byte order shown in Table 6 to be used. It is possible to read out up to n-data bytes.

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The first byte sent defines both the mode and the address.

Table 6. MOSI and MISO byte order

Line	Byte 0	Byte 1	Byte 2	To	Byte n	Byte n + 1
MOSI	address 0	address 1	address 2	...	address n	00
MISO	X[1]	data 0	data 1	...	data n – 1	data n

[1] X = Do not care.

Remark: The MSB must be sent first.

8.3.2.2 SPI write data

To write data to the MFRC523 using SPI requires the byte order shown in Table 7. It is possible to write up to n-data bytes by only sending one address byte.

The first send byte defines both the mode and the address byte.

Table 7. MOSI and MISO byte order

Line	Byte 0	Byte 1	Byte 2	To	Byte n	Byte n + 1
MOSI	address 0	data 0	data 1	...	data n – 1	data n
MISO	X[1]	X[1]	X[1]	...	X[1]	X[1]

[1] X = Do not care.

Remark: The MSB must be sent first.

8.3.2.3 SPI Read and Write address byte

The read address byte must meet the following criteria:

- the Most Significant Bit (MSB) of the first byte sets the mode. To read data from the MFRC523, the MSB is set to logic 1; see Table 8
- bits [6:1] define the address
- the Least Significant Bit (LSB) should be set to logic 0

Table 8. SPI read address

Address (MOSI)	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
byte 0	1	address	address	address	address	address	address	0

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The write address byte must meet the following criteria:

- the MSB of the first byte sets the mode. To write data to the MFRC523, the MSB is set to logic 0; see Table 9
- bits [6:1] define the address
- the LSB should be set to logic 0

Table 9. SPI write address

Address line (MOSI)	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
byte 0	0	address	address	address	address	address	address	0

8.3.3 UART interface

8.3.3.1 Connection to a host

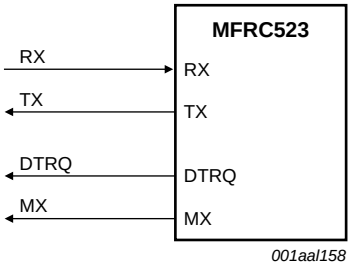

Fig 8. UART connection to microcontrollers

Remark: Signals DTRQ and MX can be disabled by clearing TestPinEnReg register's RS232LineEn bit.

8.3.3.2 Selectable UART transfer speeds

The internal UART interface is compatible with the RS232 serial interface.

The default transfer speed is 9.6 kBd. To change the transfer speed, the host controller must write a value for the new transfer speed to the SerialSpeedReg register. Bits BR_T0[2:0] and BR_T1[4:0] define the factors for setting the transfer speed in the SerialSpeedReg register.

The BR_T0[2:0] and BR_T1[4:0] settings are described in Table 10. Examples of different transfer speeds and the relevant register settings are given in Table 11.

Table 10. BR_T0 and BR_T1 settings

BR_Tn	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
BR_T0 factor	1	1	2	4	8	16	32	64
BR_T1 range	1 to 32	33 to 64	33 to 64	33 to 64	33 to 64	33 to 64	33 to 64	33 to 64

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Table 11. Selectable UART transfer speeds

Transfer speed (kBd)	SerialSpeedReg value		Transfer speed accuracy (%)[1]
	Decimal	Hexadecimal	
7.2	250	FAh	–0.25
9.6	235	EBh	0.32
14.4	218	DAh	–0.25
19.2	203	CBh	0.32
38.4	171	ABh	0.32
57.6	154	9Ah	–0.25
115.2	122	7Ah	–0.25
128	116	74h	–0.06
230.4	90	5Ah	–0.25
460.8	58	3Ah	–0.25
921.6	28	1Ch	1.45
1228.8	21	15h	0.32

[1] The resulting transfer speed error is less than 1.5 % for all described transfer speeds.

The selectable transfer speeds shown in Table 11 are calculated according to the following equations:

If BR_T0[2:0] = 0:

$$transfer\ speed = \frac{27.12 \times 10^6}{(BR_T0 + 1)} \quad (1)$$

If BR_T0[2:0] > 0:

$$transfer\ speed = \left(\frac{27.12 \times 10^6}{(BR_T1 + 33)} \right) \Big/ 2^{(BR_T0 - 1)} \quad (2)$$

Remark: Transfer speeds above 1228.8 kBd are not supported.

8.3.3.3 UART framing

Table 12. UART framing

Bit	Length	Value
Start	1-bit	0
Data	8-bit	data
Stop	1-bit	1

Remark: The LSB for data and address bytes must be sent first. No parity bit is used during transmission.

To read data using the UART interface, the flow shown in Table 13 must be used. The first byte sent defines both the mode and the address.

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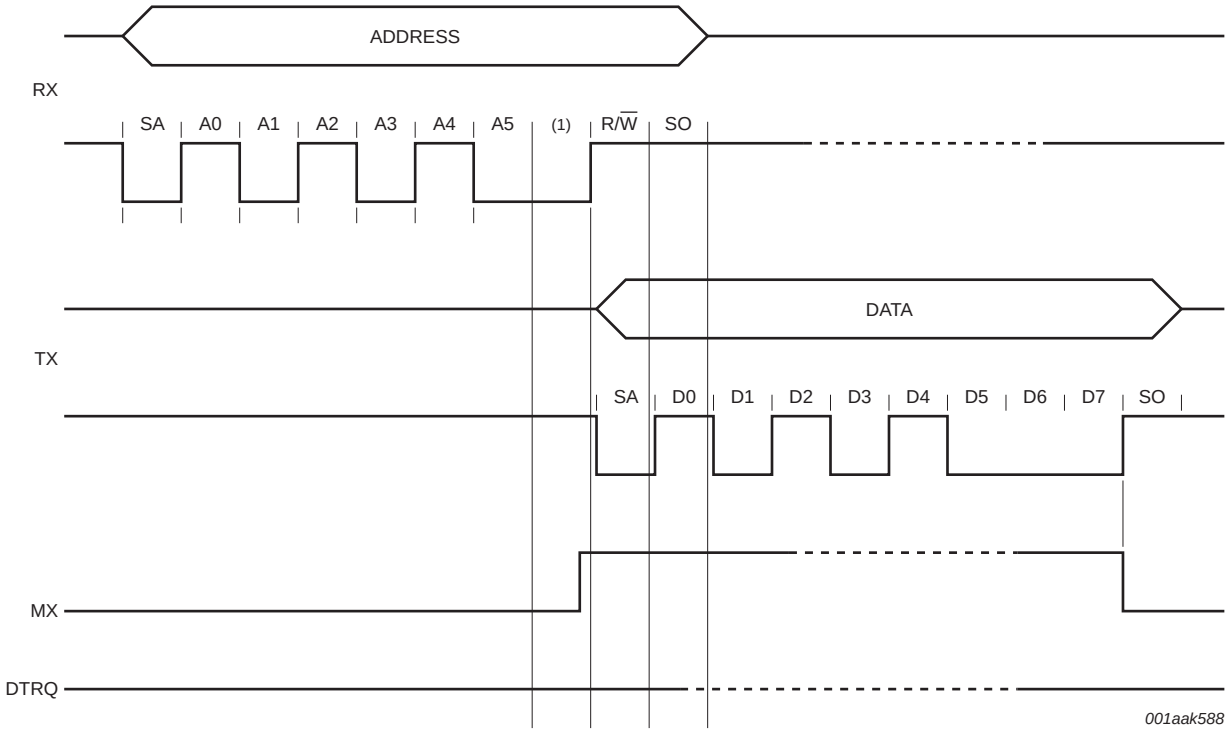
Table 13. Read data byte order

Pin	Byte 0	Byte 1
RX	address	-
TX	-	data 0



(1) Reserved.

Fig 9. UART read data timing diagram

To write data to the MFRC523 using the UART interface, the structure shown in Table 14 must be used.

The first byte sent defines both the mode and the address.

Table 14. Write data byte order

Pin	Byte 0	Byte 1
RX	address 0	data 0
TX	-	address 0

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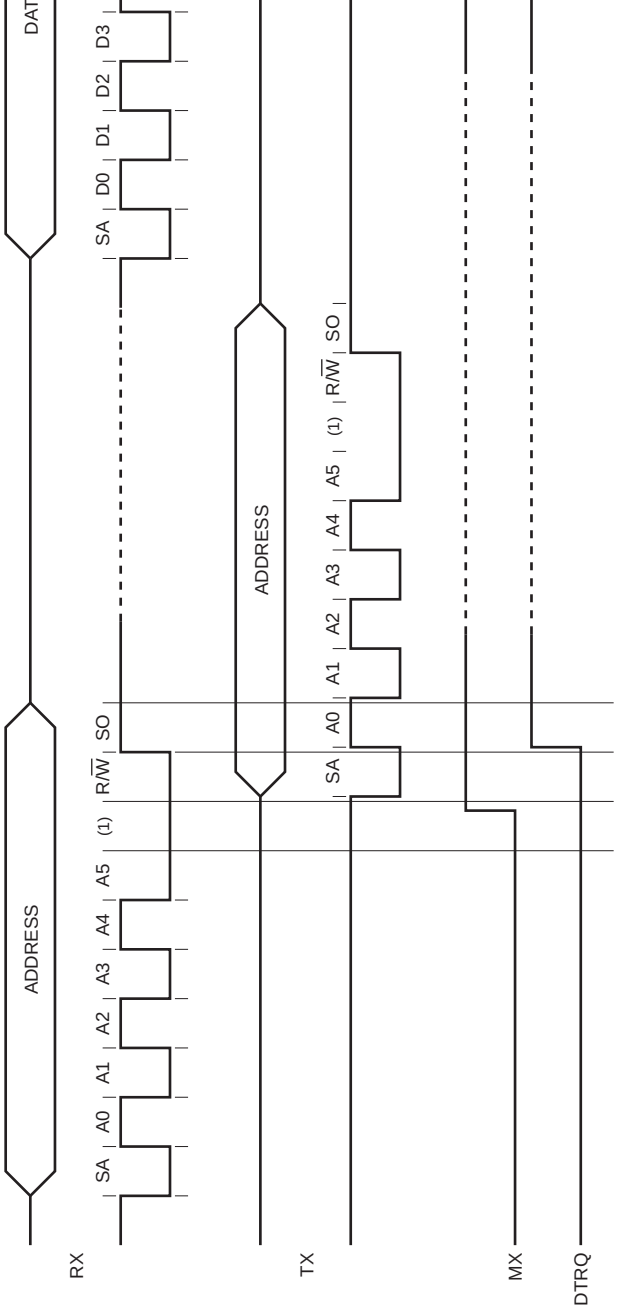

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Remark: The data byte can be sent directly after the address byte on pin RX.

Fig 10. UART write data timing diagram

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The address byte must meet the following formats:

- the MSB of the first byte sets the mode used
  - the MSB is set to logic 0 to write data to the MFRC523
  - the MSB is set to logic 1 to read data from the MFRC523
- bit 6 is reserved for future use
- bits [5:0] define the address; see Table 15

Table 15. Address byte 0 register; address MOSI

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
1 or 0	reserved	address	address	address	address	address	address

8.3.4 I²C Bus Interface

An I²C-bus interface is supported and enables implementation of a low-cost, low pin count serial bus interface to the host. The I²C-bus interface is implemented based on NXP Semiconductors' *I²C-bus interface specification, rev. 2.1, January 2000*. The interface can only act in slave mode. Therefore the MFRC523 does not perform clock generation or access arbitration.

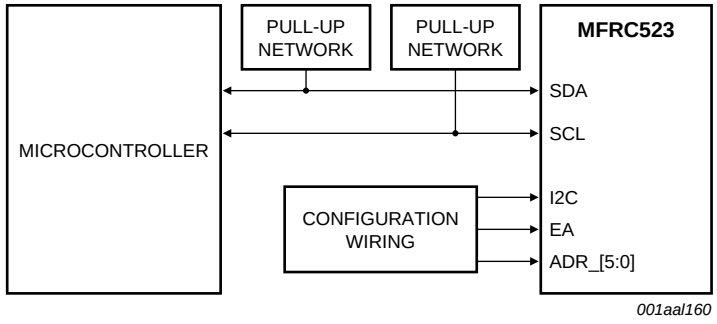

Fig 11. I²C-bus interface

The MFRC523 can act as a slave receiver or slave transmitter in Standard mode, Fast mode and High-speed mode.

SDA is a bidirectional line connected to a positive supply voltage using a current source or a pull-up resistor. Both SDA and SCL lines are set HIGH when data is not transmitted. The MFRC523 has a 3-state output stage to perform the wired-AND function. Data on the I²C-bus can be transferred at data rates of up to 100 kBd in Standard mode, up to 400 kBd in Fast mode or up to 3.4 Mbit/s in High-speed mode.

If the I²C-bus interface is selected, spike suppression is activated on lines SCL and SDA as defined in the I²C-bus interface specification.

See Table 156 on page 79 for timing requirements.

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8.3.4.1 Data validity

Data on the SDA line must be stable during the HIGH clock period. The HIGH or LOW state of the data line must only change when the clock signal on SCL is LOW.

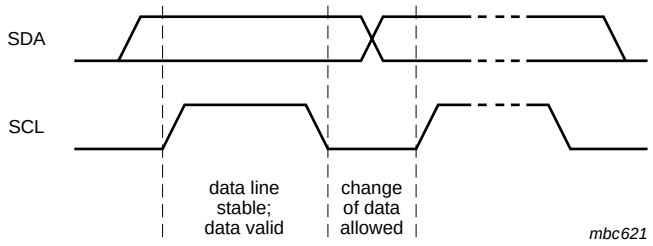

Fig 12. Bit transfer on the I²C-bus

8.3.4.2 START and STOP conditions

To manage the data transfer on the I²C-bus, unique START (S) and STOP (P) conditions are defined.

- A START condition is defined with a HIGH-to-LOW transition on the SDA line while SCL is HIGH.
- A STOP condition is defined with a LOW-to-HIGH transition on the SDA line while SCL is HIGH.

The I²C-bus master always generates the START and STOP conditions. The bus is busy after the START condition. The bus is free again a certain time after the STOP condition.

The bus stays busy if a repeated START (Sr) is generated instead of a STOP condition. The START (S) and repeated START (Sr) conditions are functionally identical. Therefore, S is used as a generic term to represent both the START (S) and repeated START (Sr) conditions.

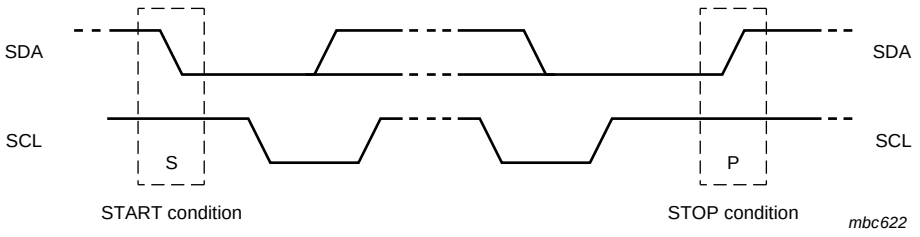

Fig 13. START and STOP conditions

8.3.4.3 Byte format

Each byte must be followed by an acknowledge bit. Data is transferred with the MSB first; see Figure 16. The number of transmitted bytes during one data transfer is unrestricted but must meet the read/write cycle format.

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8.3.4.4 Acknowledge

An acknowledge must be sent at the end of one data byte. The acknowledge-related clock pulse is generated by the master. The transmitter of data, either master or slave, releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver pulls down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse.

The master can then generate either a STOP (P) condition to stop the transfer or a repeated START (Sr) condition to start a new transfer.

A master-receiver indicates the end of data to the slave-transmitter by not generating an acknowledge on the last byte that was clocked out by the slave. The slave-transmitter releases the data line to allow the master to generate a STOP (P) or repeated START (Sr) condition.

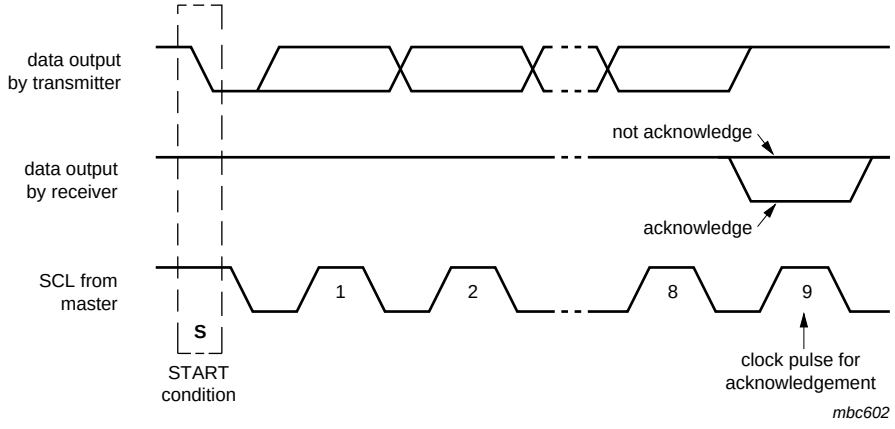

Fig 14. Acknowledge on the I²C-bus

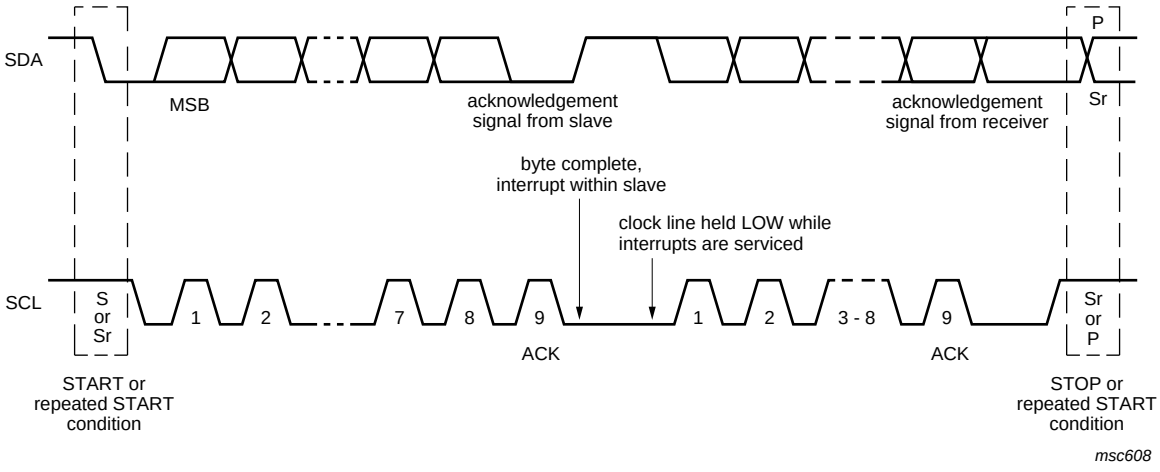

Fig 15. Data transfer on the I²C-bus

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8.3.4.5 7-Bit addressing

During the I²C-bus address procedure, the first byte after the START condition is used to determine which slave will be selected by the master.

Several address numbers are reserved. During device configuration, the designer must ensure that collisions with these reserved addresses cannot occur. Check the *I²C-bus specification* for a complete list of reserved addresses.

The I²C-bus address specification is dependent on the definition of pin EA. Immediately after releasing pin NRSTPD or after a power-on reset, the device defines the I²C-bus address according to pin EA.

If pin EA is set LOW, the upper 4 bits of the device bus address are reserved by NXP Semiconductors and set to 0101b for all MFRC523 devices. The remaining 3 bits (ADR_0, ADR_1, ADR_2) of the slave address can be freely configured by the customer to prevent collisions with other I²C-bus devices.

If pin EA is set HIGH, ADR_0 to ADR_5 can be completely specified at the external pins according to Table 5 on page 10. ADR_6 is always set to logic 0.

In both modes, the external address coding is latched immediately after releasing the reset condition. Further changes at the used pins are not taken into consideration. Depending on the external wiring, the I²C-bus address pins can be used for test signal outputs.

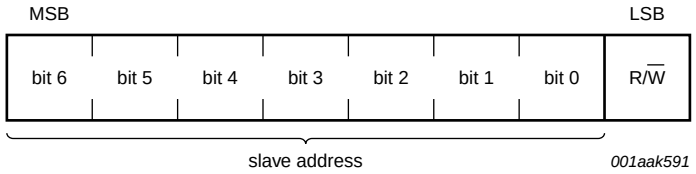

Fig 16. First byte following the START procedure

8.3.4.6 Register write access

To write data from the host controller using the I²C-bus to a specific register in the MFRC523 the following frame format must be used.

- The first byte of a frame indicates the device address according to the I²C-bus rules.
- The second byte indicates the register address followed by up to n-data bytes.

In one frame, all data bytes are written to the same register address. This enables fast FIFO buffer access. The Read/Write (R/$\overline{W}$) bit is set to logic 0.

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8.3.4.7 Register read access

To read out data from a specific register address in the MFRC523, the host controller must use the following procedure:

- Firstly, a write access to the specific register address must be performed as indicated in the frame that follows
- The first byte of a frame indicates the device address according to the I²C-bus rules
- The second byte indicates the register address. No data bytes are added
- The Read/Write bit is 0

After the write access, read access can start. The host sends the device address of the MFRC523. In response, the MFRC523 sends the content of the read access register. In one frame all data bytes can be read from the same register address. This enables fast FIFO buffer access or register polling.

The Read/Write (R/W) bit is set to logic 1.

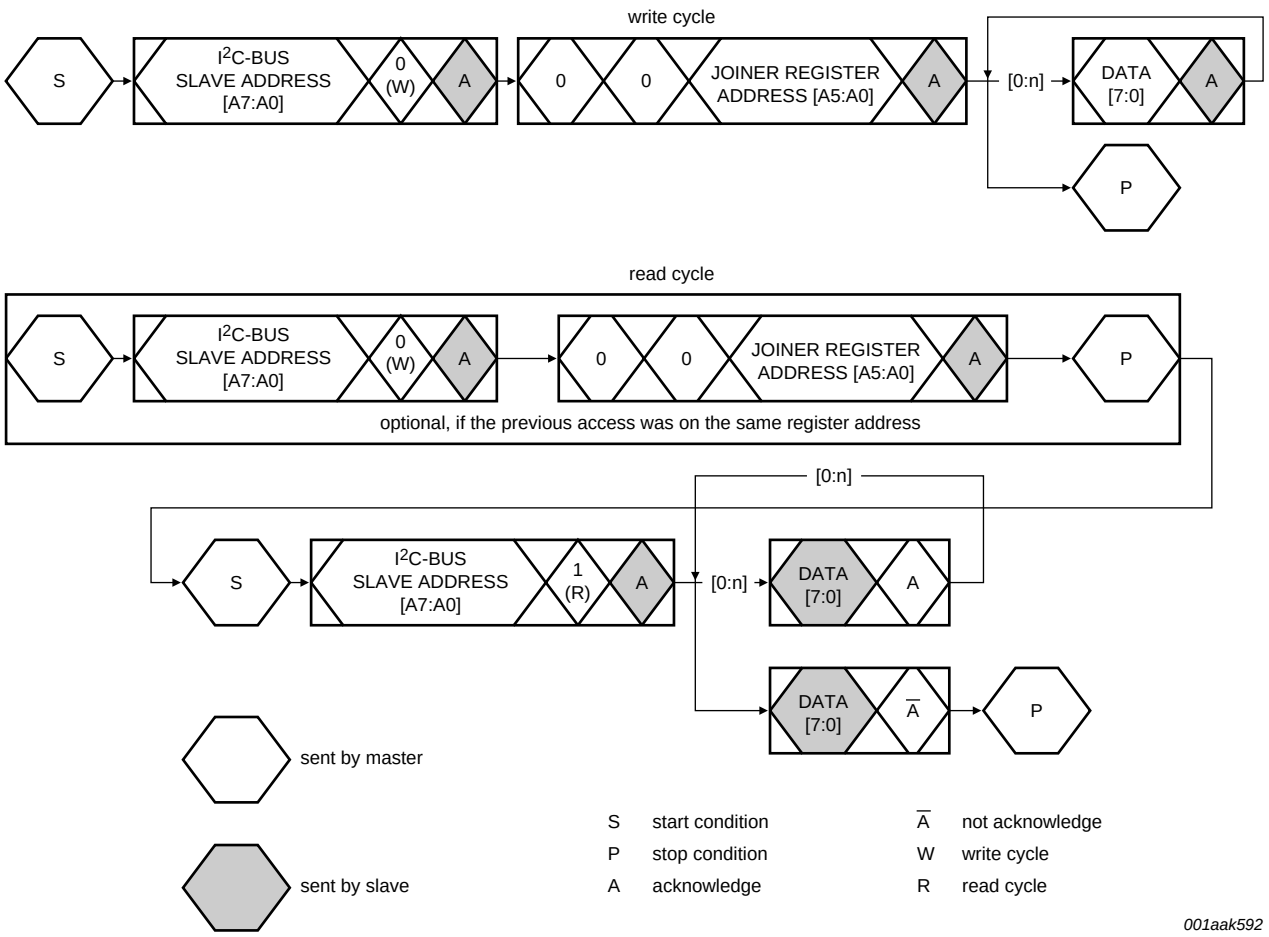

Fig 17. Register read and write access

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8.3.4.8 High-speed mode

In High-speed mode (HS mode), the device can transfer information at data rates of up to 3.4 Mbit/s, while remaining fully downward-compatible with Fast or Standard modes (F/S modes) for bidirectional communication in a mixed-speed bus system.

8.3.4.9 High-speed transfer

To achieve data rates of up to 3.4 Mbit/s the following improvements have been made to I^2C-bus operation.

- The inputs of the device in HS mode incorporate spike suppression, a Schmitt trigger on the SDA and SCL inputs and different timing constants when compared to F/S mode
- The output buffers of the device in HS mode incorporate slope control of the falling edges of the SDA and SCL signals with different fall times compared to F/S mode

8.3.4.10 Serial data transfer format in HS mode

The HS mode serial data transfer format meets the Standard mode I^2C-bus specification. HS mode can only start after all of the following conditions (all of which are in F/S mode):

1. START condition (S)
2. 8-bit master code (00001 XXXb)
3. Not-acknowledge bit ($\overline{A}$)

When HS mode starts, the active master sends a repeated START condition (Sr) followed by a 7-bit slave address with a R/W bit address and receives an acknowledge bit (A) from the selected MFRC523.

Data transfer continues in HS mode after the next repeated START (Sr), only switching back to F/S mode after a STOP condition (P). To reduce the overhead of the master code, a master links a number of HS mode transfers, separated by repeated START conditions (Sr).

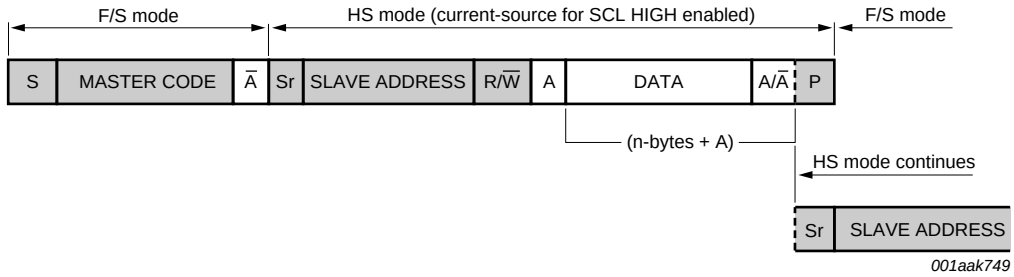

Fig 18. I^2C-bus HS mode protocol switch

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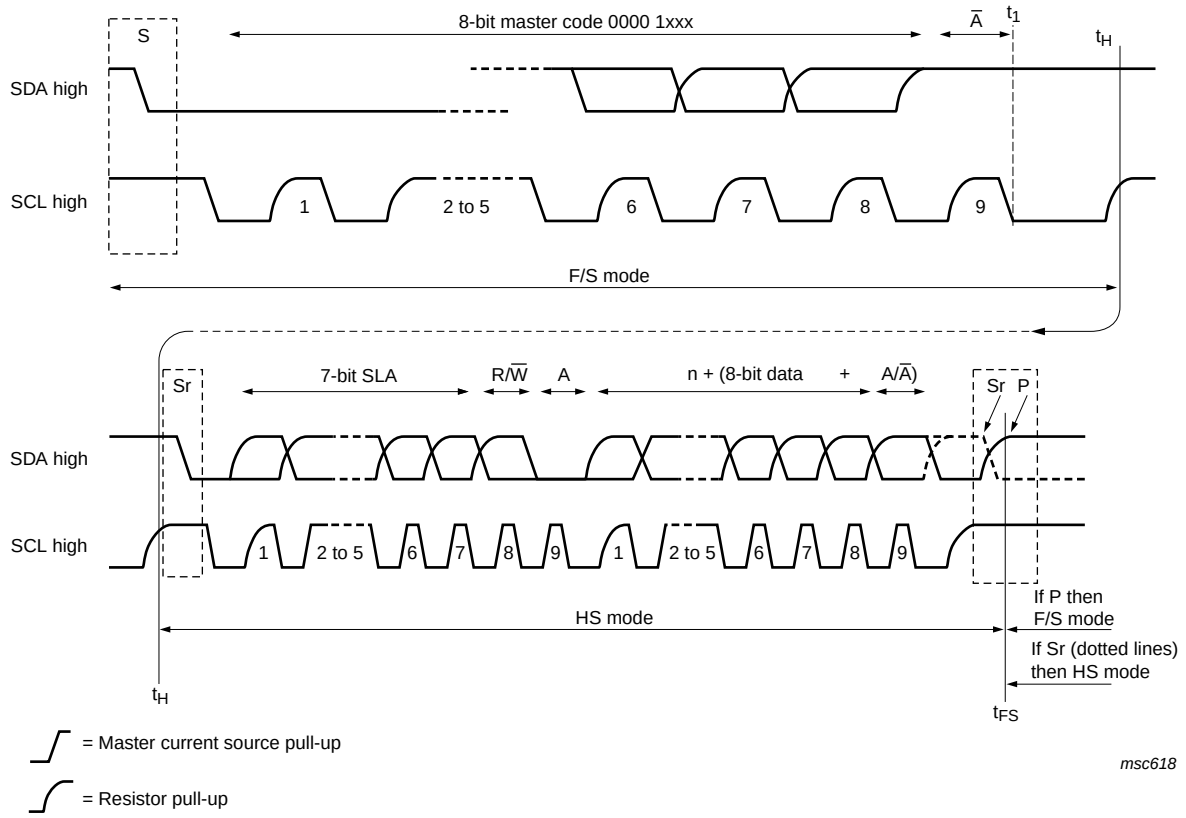

Fig 19. I²C-bus HS mode protocol frame

8.3.4.11 Switching between F/S mode and HS mode

After reset and initialization, the MFRC523 is in Fast mode (which is in effect F/S mode as Fast mode is downward-compatible with Standard mode). The connected MFRC523 recognizes the “S 00001XXX A” sequence and switches its internal circuitry from the Fast mode setting to the HS mode setting.

The following actions are taken:

1. Adapt the SDA and SCL input filters according to the spike suppression requirement in HS mode.
2. Adapt the slope control of the SDA output stages.

It is possible for system configurations that do not have other I²C-bus devices involved in the communication to switch to HS mode permanently. This is implemented by setting Status2Reg register’s I²CForceHS bit to logic 1. In permanent HS mode, the master code is not required to be sent. This is not defined in the specification and must only be used when no other devices are connected on the bus. In addition, spikes on the I²C-bus lines must be avoided because of the reduced spike suppression.

8.3.4.12 MFRC523 in lower speed modes

MFRC523 is fully downward-compatible and can be connected to an F/S mode I²C-bus system. The device stays in F/S mode and communicates at F/S mode speeds because a master code is not transmitted in this configuration.

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8.4 Analog interface and contactless UART

8.4.1 General

The integrated contactless UART supports the external host online with framing and error checking of the protocol requirements up to 848 kBd. An external circuit can be connected to the communication interface pins MFIN and MFOUT to modulate and demodulate the data.

The contactless UART manage the protocol requirements for the communication protocols in cooperation with the host. Protocol handling generates bit and byte-oriented framing. In addition, it manages error detection such as parity and CRC, based on the various supported contactless communication protocols.

Remark: The size and tuning of the antenna and the power supply voltage have an important impact on the achievable operating distance.

8.4.2 TX p-driver

The signal on pins TX1 and TX2 is the 13.56 MHz energy carrier modulated by an envelope signal. It can be used to drive an antenna directly using a few passive components for matching and filtering; see Section 16 on page 81. The signal on pins TX1 and TX2 can be configured using the TxControlReg register; see Section 9.2.2.5 on page 49.

The modulation index can be set by adjusting the impedance of the drivers. The impedance of the p-driver can be configured using registers CWGsPReg and ModGsPReg. The impedance of the n-driver can be configured using the GsNReg register. The modulation index also depends on the antenna design and tuning.

The TxModeReg and TxSelReg registers control the data rate and framing during transmission and the antenna driver setting to support the different requirements at the different modes and transfer speeds.

Table 16. Register and bit settings controlling the signal on pin TX1

Bit Tx1RFEn	Bit Force 100ASK	Bit InvTx1RFOn	Bit InvTx1RFOff	Envelope	Pin TX1	GSPMos	GSNMos	Remarks
0	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	not specified if RF is switched off
1	0	0	X[1]	0	RF	pMod	nMod	100 % ASK: pin TX1 pulled to logic 0, independently of the InvTx1RFOff bit
				1	RF	pCW	nCW	
	0	1	X[1]	0	RF	pMod	nMod	
				1	RF	pCW	nCW	
	1	1	X[1]	0	0	pMod	nMod	
				1	RF_n	pCW	nCW	

[1] X = Do not care.

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Table 17. Register and bit settings controlling the signal on pin TX2

Bit Tx1RFEn	Bit Force 100ASK	Bit Tx2CW	Bit InvTx2RFOn	Bit InvTx2RFOff	Envelope	Pin TX2	GSPMos	GSNMos	Remarks
0	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	not specified if RF is switched off
1	0	0	0	X[1]	0	RF	pMod	nMod	-
					1	RF	pCW	nCW	
			1	X[1]	0	RF_n	pMod	nMod	
					1	RF_n	pCW	nCW	
		1	0	X[1]	X[1]	RF	pCW	nCW	conductance always CW for the Tx2CW bit
			1	X[1]	X[1]	RF_n	pCW	nCW	
	1	0	0	X[1]	0	0	pMod	nMod	100 % ASK: pin TX2 pulled to logic 0 (independent of the InvTx2RFOn/InvTx2RFOff bits)
					1	RF	pCW	nCW	
			1	X[1]	0	0	pMod	nMod	
					1	RF_n	pCW	nCW	
		1	0	X[1]	X[1]	RF	pCW	nCW	
			1	X[1]	X[1]	RF_n	pCW	nCW	

[1] X = Do not care.

The following abbreviations have been used in Table 16 and Table 17:

- RF: 13.56 MHz clock derived from 27.12 MHz quartz crystal oscillator divided by 2
- RF_n: inverted 13.56 MHz clock
- GSPMos: conductance, configuration of the PMOS array
- GSNMos: conductance, configuration of the NMOS array
- pCW: PMOS conductance value for continuous wave defined by the CWGsPReg register
- pMod: PMOS conductance value for modulation defined by the ModGsPReg register
- nCW: NMOS conductance value for continuous wave defined by the GsNReg register's CWGsN[3:0] bits
- nMod: NMOS conductance value for modulation defined by the GsNReg register's ModGsN[3:0] bits
- X = Do not care

Remark: If only one driver is switched on, the values for CWGsPReg, ModGsPReg and GsNReg registers are used for both drivers.

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8.4.3 Serial data switch

Two main blocks are implemented in the MFRC523. The digital block comprises the state machines, encoder/decoder logic. The analog block comprises the modulator and antenna drivers, the receiver and amplifiers. It is possible for the interface between these two blocks to be configured so that the interfacing signals are routed to pins MFIN and MFOUT. This topology allows the analog block of the MFRC523 to be connected to the digital block of another device.

The serial signal switch is controlled by the TxSelReg and RxSelReg registers.

Figure 20 shows the serial data switch for TX1 and TX2.

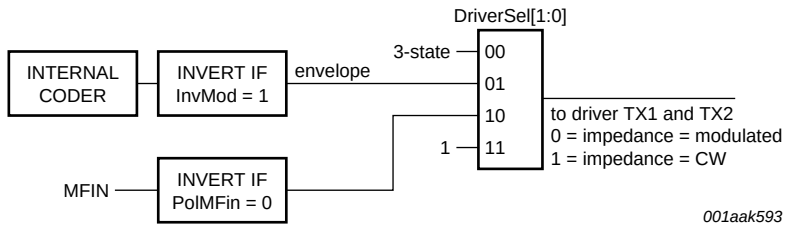

Fig 20. Serial data switch for TX1 and TX2

8.4.4 MFIN and MFOUT interface support

The MFRC523 is divided into a digital circuit block and an analog circuit block. The digital block contains state machines, encoder and decoder logic, etc. The analog block contains the modulator and antenna drivers, receiver and amplifiers. The interface between these two blocks can be configured to enable the interfacing signals to be routed to pins MFIN and MFOUT; see Figure 21 on page 26. This configuration is implemented using TxSelReg register's MFOutSel[3:0]/DriverSel[1:0] bits and RxSelReg register's UARTSel[1:0] bits. This topology allows some parts of the analog block to be connected to the digital block of another device.

Switch MFOutSel in the TxSelReg register can be used to measure MIFARE and ISO/IEC14443 A related signals. This is especially important during the design-in phase or for testing purposes as it enables checking of the transmitted and received data.

The most important use of pins MFIN and MFOUT is found in the active antenna concept. An external active antenna circuit can be connected to the MFRC523's digital block. Switch MFOutSel must be configured so that the internal Miller encoded signal is sent to pin MFOUT (MFOutSel = 100b). UARTSel[1:0] must be configured to receive a Manchester signal with subcarrier from pin MFIN (UARTSel[1:0] = 01).

It is possible to connect a passive antenna to pins TX1, TX2 and RX (using the appropriate filter and matching circuit) and an active antenna to pins MFOUT and MFIN at the same time. In this configuration, two RF circuits can be driven (one after another) by a single host processor.

Remark: Pins MFIN and MFOUT have a dedicated supply on pin SVDD with the ground on pin PVSS.

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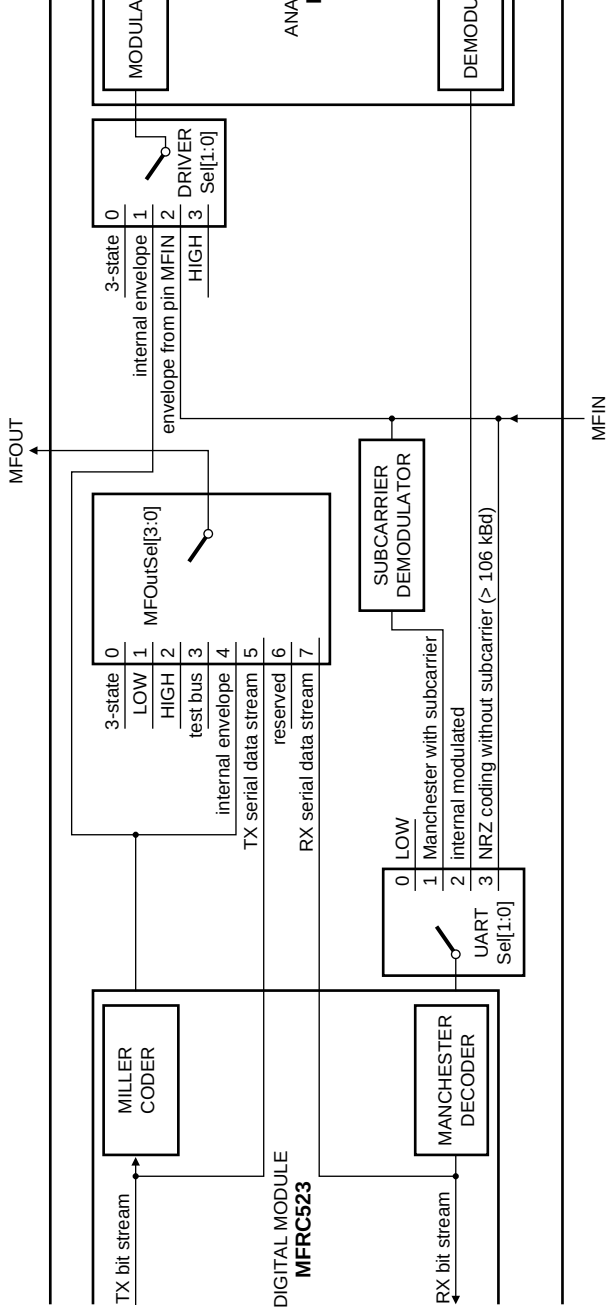

Fig 21. Overview of MFIN and MFOUT signal routing

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8.4.5 CRC coprocessor

The following CRC coprocessor parameters can be configured:

- The CRC preset value can be either 0000h, 6363h, A671h or FFFFh depending on the ModeReg register's CRCPreset[1:0] bits setting
- The CRC polynomial for the 16-bit CRC is fixed to $x^{16} + x^{12} + x^5 + 1$
- The CRCResultReg register indicates the result of the CRC calculation. This register is split into two 8-bit registers representing the higher and lower bytes.
- The ModeReg register's MSB first bit indicates that data will be loaded with the MSB first.

Table 18. CRC coprocessor parameters

Parameter	Value
CRC register length	16-bit CRC
CRC algorithm	algorithm according to ISO/IEC 14443 A and ITU-T
CRC preset value	0000h, 6363h, A671h or FFFFh depending on the setting of the ModeReg register's CRCPreset[1:0] bits

8.5 FIFO buffer

An 8 × 64 bit FIFO buffer is used in the MFRC523. It buffers the input and output data stream between the host and the MFRC523's internal state machine. This makes it possible to manage data streams up to 64 bytes long without the need to take timing constraints into account.

8.5.1 Accessing the FIFO buffer

The FIFO buffer input and output data bus is connected to the FIFODataReg register. Writing to this register stores one byte in the FIFO buffer and increments the internal FIFO buffer write pointer. Reading from this register shows the FIFO buffer contents stored in the FIFO buffer read pointer and decrements the FIFO buffer read pointer. The distance between the write and read pointer can be obtained by reading the FIFOLevelReg register.

When the microcontroller starts a command, the MFRC523 can, while the command is in progress, access the FIFO buffer according to that command. Only one FIFO buffer has been implemented which can be used for input and output. The microcontroller must ensure that there are not any unintentional FIFO buffer accesses.

8.5.2 Controlling the FIFO buffer

The FIFO buffer pointers can be reset by setting FIFOLevelReg register's FlushBuffer bit to logic 1. Consequently, the FIFOLevel[6:0] bits are all set to logic 0 and the ErrorReg register's BufferOvfl bit is cleared. The bytes stored in the FIFO buffer are no longer accessible allowing the FIFO buffer to be filled with another 64 bytes.

8.5.3 FIFO buffer status information

The host can get the following FIFO buffer status information:

- Number of bytes stored in the FIFO buffer: FIFOLevelReg register's FIFOLevel[6:0]
- FIFO buffer almost full warning: Status1Reg register's HiAlert bit

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- FIFO buffer almost empty warning: Status1Reg register's LoAlert bit
- FIFO buffer overflow warning: ErrorReg register's BufferOvfl bit. The BufferOvfl bit can only be cleared by setting the FIFOLevelReg register's FlushBuffer bit.

The MFRC523 can generate an interrupt signal when:

- ComIEnReg register's LoAlertIEn bit is set to logic 1. It activates pin IRQ when Status1Reg register's LoAlert bit changes to logic 1.
- ComIEnReg register's HiAlertIEn bit is set to logic 1. It activates pin IRQ when Status1Reg register's HiAlert bit changes to logic 1.

If the maximum number of WaterLevel[5:0] bits (as set in the WaterLevelReg register) or less are stored in the FIFO buffer, the HiAlert bit is set to logic 1. It is generated according to Equation 3:

$$HiAlert = (64 - FIFOLength) \leq WaterLevel \quad (3)$$

If the number of WaterLevel[5:0] bits (as set in the WaterLevelReg register) or less are stored in the FIFO buffer, the LoAlert bit is set to logic 1. It is generated according to Equation 4:

$$LoAlert = FIFOLength \leq WaterLevel \quad (4)$$

8.6 Interrupt request system

The MFRC523 indicates certain events by setting the Status1Reg register's IRq bit and, if activated, by pin IRQ. The signal on pin IRQ can be used to interrupt the host using its interrupt handling capabilities. This allows the implementation of efficient host software.

8.6.1 Interrupt sources overview

Table 19 shows the available interrupt bits, the corresponding source and the condition for its activation. The ComIrqReg register's TimerIRq interrupt bit indicates an interrupt set by the timer unit which is set when the timer decrements from 1 to 0.

The ComIrqReg register's TxIRq bit indicates that the transmitter has finished. If the state changes from sending data to transmitting the end of the frame pattern, the transmitter unit automatically sets the interrupt bit. The CRC coprocessor sets the DivIrqReg register's CRCIRq bit after processing all the FIFO buffer data which is indicated by CRCReady bit = 1.

The ComIrqReg register's RxIRq bit indicates an interrupt when the end of the received data is detected. The ComIrqReg register's IdleIRq bit is set if a command finishes and the Command[3:0] value in the CommandReg register changes to idle (see Table 150 on page 69).

The ComIrqReg register's HiAlertIRq bit is set to logic 1 when the Status1Reg register's HiAlert bit is set to logic 1 which means that the FIFO buffer has reached the level indicated by the WaterLevel[5:0] bits.

The ComIrqReg register's LoAlertIRq bit is set to logic 1 when the Status1Reg register's LoAlert bit is set to logic 1 which means that the FIFO buffer has reached the level indicated by the WaterLevel[5:0] bits.

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The ComIrqReg register's ErrIRq bit indicates an error detected by the contactless UART during send or receive. This is indicated when any bit is set to logic 1 in register ErrorReg.

Table 19. Interrupt sources

Interrupt flag	Interrupt source	Trigger action
TimerIRq	timer unit	the timer counts from 1 to 0
TxIRq	transmitter	a transmitted data stream ends
CRCIRq	CRC coprocessor	all data from the FIFO buffer has been processed
RxIRq	receiver	a received data stream ends
IdleIRq	ComIrqReg register	command execution finishes
HiAlertIRq	FIFO buffer	the FIFO buffer is almost full
LoAlertIRq	FIFO buffer	the FIFO buffer is almost empty
ErrIRq	contactless UART	an error is detected

8.7 Timer unit

The MFRC523A has a timer unit which the external host can use to manage timing tasks. The timer unit can be used in one of the following timer/counter configurations:

- Timeout counter
- Watchdog counter
- Stop watch
- Programmable one shot
- Periodic trigger

The timer unit can be used to measure the time interval between two events or to indicate that a specific event occurred after a specific time. The timer can be triggered by events explained in the paragraphs below. The timer does not influence any internal events, for example, a time-out during data reception does not automatically influence the reception process. In addition, several timer-related bits can be used to generate an interrupt.

The timer has an input clock of 13.56 MHz derived from the 27.12 MHz quartz crystal oscillator. The timer consists of two stages: prescaler and counter.

The prescaler (TPrescaler) is a 12-bit counter. The reload values (TReloadVal_Hi[7:0] and TReloadVal_Lo[7:0]) for TPrescaler can be set between 0 and 4095 in the TModeReg register's TPrescaler_Hi[3:0] bits and TPrescalerReg register's TPrescaler_Lo[7:0] bits.

The reload value for the counter is defined by 16 bits between 0 and 65535 in the TReloadReg register.

The current value of the timer is indicated in the TCounterValReg register.

When the counter reaches 0, an interrupt is automatically generated, indicated by the ComIrqReg register's TimerIRq bit setting. If enabled, this event can be indicated on pin IRQ. The TimerIRq bit can be set and reset by the host. Depending on the configuration, the timer will stop at 0 or restart with the value set in the TReloadReg register.

The timer status is indicated by the Status1Reg register's TRunning bit.

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The timer can be started manually using the ControlReg register's TStartNow bit and stopped using the ControlReg register's TStopNow bit.

The timer can also be activated automatically to meet any dedicated protocol requirements, by setting the TModeReg register's TAuto bit to logic 1.

The delay time of a timer stage is set by the reload value + 1. The total delay time (t_d) is calculated using Equation 5:

$$t_d = \frac{(TPrescaler \times 2 + 1) \times (TReloadVal + 1)}{13.56\ MHz} \quad (5)$$

or if the TPrescalEven bit is set, using Equation 6:

$$t_d = \frac{(TPrescaler \times 2 + 2) \times (TReloadVal + 1)}{13.56\ MHz} \quad (6)$$

An example of calculating total delay time (t_d) is shown in Equation 7, where the TPrescaler value = 4095 and TReloadVal = 65535:

$$39.59\ s = \frac{(4095 \times 2 + 1) \times (65535 + 1)}{13.56\ MHz} \quad (7)$$

Example: To give a delay time of 25 μs requires 339 clock cycles to be counted and a TPrescaler value of 169. This configures the timer to count up to 65535 time-slots for every 25 μs period.

Available prescaler modes for version 1.0 (B1h) can be seen in Section 11.

8.8 Power reduction modes

8.8.1 Hard power-down

Hard power-down is enabled when pin NRSTPD is LOW. This turns off all internal current sinks including the oscillator. All digital input buffers are separated from the input pins and clamped internally (except pin NRSTPD). The output pins are frozen at either a HIGH or LOW level.

8.8.2 Soft power-down mode

Soft power-down mode is entered immediately after the CommandReg register's PowerDown bit is set to logic 1. All internal current sinks are switched off, including the oscillator buffer. However, the digital input buffers are not separated from the input pins and keep their functionality. The digital output pins do not change their state.

During soft power-down, all register values, the FIFO buffer content and the configuration keep their current contents.

After setting the PowerDown bit to logic 0, it takes 1024 clocks until the Soft power-down mode is exited indicated by the PowerDown bit. Setting it to logic 0 does not immediately clear it. It is automatically cleared by the MFRC523 when Soft power-down mode is exited.

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Remark: When the internal oscillator is used, time (t_{osc}) is required for the oscillator to become stable. This is because the internal oscillator is supplied by V_{DDA} and any clock cycles will not be detected by the internal logic until V_{DDA} is stable. It is recommended for the serial UART, to first send the value 55h to the MFRC523. The oscillator must be stable for further access to the registers. To ensure this, perform a read access to address 0 until the MFRC523 answers to the last read command with the register content of address 0. This indicates that the MFRC523 is ready.

8.8.3 Transmitter Power-down mode

The Transmitter Power-down mode switches off the internal antenna drivers and the RF field. Transmitter Power-down mode is entered by setting either the TxControlReg register's Tx1RFEn bit or Tx2RFEn bit to logic 0.

8.9 Oscillator circuit

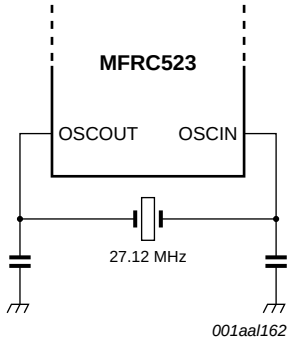

Fig 22. Quartz crystal connection

The clock applied to the MFRC523 provides a time basis for the synchronous system's encoder and decoder. The stability of the clock frequency is an important factor for correct operation. To obtain optimum performance, clock jitter must be reduced as much as possible. This is best achieved using the internal oscillator buffer with the recommended circuitry.

If an external clock source is used, the clock signal must be applied to pin OSCIN. In this case, be very careful in optimizing clock duty cycle and clock jitter. Ensure the clock quality has been verified.

8.10 Reset and oscillator start-up time

8.10.1 Reset timing requirements

The reset signal is filtered by a hysteresis circuit and a spike filter before it enters the digital circuit. The spike filter rejects signals shorter than 10 ns. In order to perform a reset, the signal must be LOW for at least 100 ns.

8.10.2 Oscillator start-up time

If the MFRC523 has been set to a Power-down mode or is powered by a V_{DDX} supply, the start-up time for the MFRC523 depends on the oscillator used and is shown in Figure 23.

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The time ($t_{startup}$) is the start-up time of the crystal oscillator circuit. The crystal oscillator start-up time is defined by the crystal.

The time (t_d) is the internal delay time of the MFRC523 when the clock signal is stable before the MFRC523 can be addressed.

The delay time is calculated by:

$$t_d = \frac{1024}{27\ \mu s} = 37.74\ \mu s \quad (8)$$

The time (t_{osc}) is the sum of t_d and $t_{startup}$.

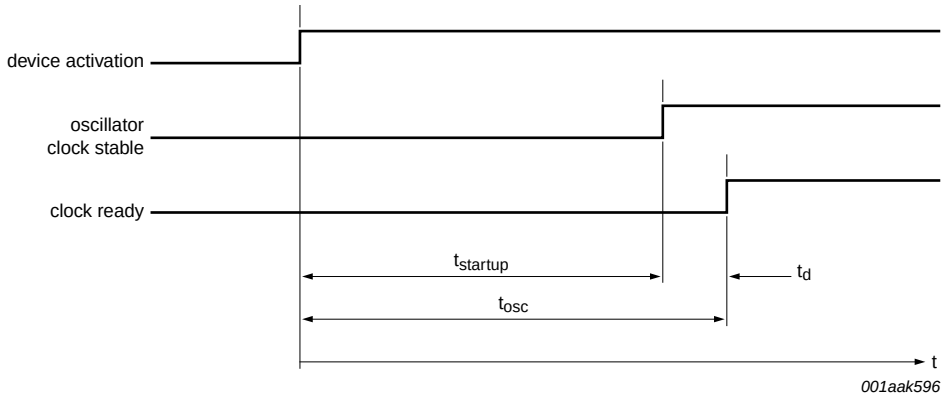

Fig 23. Oscillator start-up time

9. MFRC523 registers

9.1 Register bit behavior

Depending on the functionality of a register, the access conditions to the register can vary. In principle, bits with same behavior are grouped in common registers. The access conditions are described in Table 20.

Table 20. Behavior of register bits and their designation

Abbreviation	Behavior	Description
R/W	read and write	These bits can be written and read by the microcontroller. Since they are used only for control purposes, their content is not influenced by internal state machines, for example the ComIEnReg register can be written and read by the microcontroller. It will also be read by internal state machines but never changed by them.
D	dynamic	These bits can be written and read by the microcontroller. Nevertheless, they can also be written automatically by internal state machines, for example the CommandReg register changes its value automatically after the execution of the command.
R	read only	These register bits hold values which are determined by internal states only, for example the CRCReady bit cannot be written externally but shows internal states.

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Table 20. Behavior of register bits and their designation *...continued*

Abbreviation	Behavior	Description
W	write only	Reading these register bits always returns zero.
reserved	-	Registers which are indicated as being reserved must not be changed. However, in the case of a write access, it is recommended that 0 is always written.
	-	Registers which are indicated as being reserved for future use or are for production tests must not be changed.

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9.1.1 MFRC523 register overview

Table 21. MFRC523 register overview

Subaddress (Hex)	Register name	Function	Refer to
Page 0: Command and status			
00h	Reserved	reserved for future use	Table 22 on page 37
01h	CommandReg	starts and stops command execution	Table 24 on page 37
02h	ComlEnReg	enable and disable interrupt request control bits	Table 26 on page 38
03h	DivlEnReg	enable and disable interrupt request control bits	Table 28 on page 38
04h	ComIrqReg	interrupt request bits	Table 30 on page 39
05h	DivIrqReg	interrupt request bits	Table 32 on page 40
06h	ErrorReg	error bits showing the error status of the last command executed	Table 36 on page 41
07h	Status1Reg	communication status bits	Table 36 on page 41
08h	Status2Reg	receiver and transmitter status bits	Table 38 on page 42
09h	FIFODataReg	input and output of 64 byte FIFO buffer	Table 40 on page 43
0Ah	FIFOLevelReg	number of bytes stored in the FIFO buffer	Table 42 on page 43
0Bh	WaterLevelReg	level for FIFO underflow and overflow warning	Table 44 on page 44
0Ch	ControlReg	miscellaneous control registers	Table 46 on page 44
0Dh	BitFramingReg	adjustments for bit-oriented frames	Table 48 on page 45
0Eh	CollReg	bit position of the first bit-collision detected on the RF interface	Table 50 on page 45
0Fh	Reserved	reserved for future use	Table 52 on page 46
Page 1: Command			
10h	Reserved	reserved for future use	Table 54 on page 46
11h	ModeReg	defines general modes for transmitting and receiving	Table 56 on page 47
12h	TxModeReg	defines transmission data rate and framing	Table 58 on page 48
13h	RxModeReg	defines reception data rate and framing	Table 60 on page 48
14h	TxControlReg	controls the antenna driver pins TX1 and TX2	Table 62 on page 49
15h	TxASKReg	controls the setting of the transmission modulation	Table 64 on page 50
16h	TxSelReg	selects the internal sources for the antenna driver	Table 66 on page 50
17h	RxSelReg	selects internal receiver settings	Table 68 on page 51
18h	RxThresholdReg	selects thresholds for the bit decoder	Table 70 on page 52
19h	DemodReg	defines demodulator settings	Table 72 on page 52
1Ah	Reserved	reserved for future use	Table 74 on page 53
1Bh	Reserved	reserved for future use	Table 76 on page 53
1Ch	MfTxReg	controls MIFARE communication transmit parameters	Table 78 on page 53
1Dh	MfRxReg	controls MIFARE communication receive parameters	Table 80 on page 54
1Eh	TypeBReg	controls the ISO/IEC 14443 B functionality	Table 82 on page 54
1Fh	SerialSpeedReg	selects the speed of the serial UART interface	Table 84 on page 55

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Table 21. MFRC523 register overview *...continued*

Subaddress (Hex)	Register name	Function	Refer to
Page 2: Configuration			
20h	Reserved	reserved for future use	Table 86 on page 56
21h	CRCResultReg	shows the MSB and LSB values of the CRC calculation	Table 88 on page 56
22h	CRCResultReg	shows the MSB and LSB values of the CRC calculation	Table 90 on page 56
23h	Reserved	reserved for future use	Table 92 on page 57
24h	ModWidthReg	controls the ModWidth setting	Table 94 on page 57
25h	Reserved	reserved for future use	Table 96 on page 57
26h	RFCfgReg	configures the receiver gain	Table 98 on page 58
27h	GsNReg	selects the conductance of the antenna driver pins TX1 and TX2 for modulation	Table 100 on page 58
28h	CWGsPReg	defines the conductance of the p-driver output when not active	Table 102 on page 59
29h	ModGsPReg	defines the conductance of the p-driver output during modulation	Table 104 on page 59
2Ah	TModeReg	defines settings for the internal timer	Table 106 on page 59
2Bh	TPrescalerReg		Table 108 on page 60
2Ch	TReloadReg	defines the 16-bit timer reload value	Table 110 on page 61
2Dh	TReloadReg	defines the 16-bit timer reload value	Table 112 on page 61
2Eh	TCounterValReg	shows the 16-bit timer value	Table 114 on page 61
2Fh	TCounterValReg	shows the 16-bit timer value	Table 116 on page 62
Page 3: Test register			
30h	Reserved	reserved for future use	Table 118 on page 62
31h	TestSel1Reg	general test signal configuration	Table 120 on page 62
32h	TestSel2Reg	general test signal configuration and PRBS control	Table 122 on page 63
33h	TestPinEnReg	enables pin output driver on pins D1 to D7	Table 124 on page 63
34h	TestPinValueReg	defines the values for D1 to D7 when it is used as an I/O bus	Table 126 on page 64
35h	TestBusReg	shows the status of the internal test bus	Table 128 on page 64
36h	AutoTestReg	controls the digital self-test	Table 130 on page 64
37h	VersionReg	shows the software version	Table 132 on page 65
38h	AnalogTestReg	controls the pins AUX1 and AUX2	Table 134 on page 65
39h	TestDAC1Reg	defines the test value for TestDAC1	Table 136 on page 67

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Table 21. MFRC523 register overview *…continued*

Subaddress (Hex)	Register name	Function	Refer to
3Ah	TestDAC2Reg	defines the test value for TestDAC2	Table 138 on page 67
3Bh	TestADCReg	shows the value of ADC I-channel and Q-channel	Table 140 on page 67
3Ch to 3Fh	Reserved	reserved for production tests	Table 142 to Table 148 on page 68

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9.2 Register descriptions

9.2.1 Page 0: Command and status

9.2.1.1 Reserved register 00h

Functionality is reserved for future use.

Table 22. Reserved register (address 00h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 23. Reserved register bit descriptions

Bit	Symbol	Value	Description
7 to 0	reserved	-	reserved for future use

9.2.1.2 CommandReg register

Starts and stops command execution.

Table 24. CommandReg register (address 01h); reset value: 20h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol:	00		RcvOff	PowerDown	Command[3:0]			
Access:	-		R/W	D	D			

Table 25. CommandReg register bit descriptions

Bit	Symbol	Value	Description
7 to 6	00	0	reserved
5	RcvOff	1	analog part of the receiver is switched off
4	PowerDown	1	Soft Power-down mode entered
		0	MFRC523 starts the wake up procedure during which this bit is read as a logic 1; it is read as a logic 0 when the MFRC523 is ready; see Section 8.8.2 on page 30 **Remark:** The PowerDown bit cannot be set when the SoftReset command is activated
3 to 0	Command[3:0]	-	activates a command based on the Command value; reading this register shows which command is executed; see Section 10.3 on page 69

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9.2.1.3 ComIEnReg register

Control bits to enable and disable the passing of interrupt requests.

Table 26. ComIEnReg register (address 02h); reset value: 80h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	IRqInv	TxIEn	RxIEn	IdleIEn	HiAlertIEn	LoAlertIEn	ErrIEn	TimerIEn
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 27. ComIEnReg register bit descriptions

Bit	Symbol	Value	Description
7	IRqInv	1	signal on pin IRQ is inverted with respect to the Status1Reg register's IRq bit
		0	signal on pin IRQ is equal to the IRq bit; in combination with the DivIEnReg register's IRqPushPull bit, the default value of logic 1 ensures that the output level on pin IRQ is 3-state
6	TxIEn	-	allows the transmitter interrupt request (TxIRq bit) to be propagated to pin IRQ
5	RxIEn	-	allows the receiver interrupt request (RxIRq bit) to be propagated to pin IRQ
4	IdleIEn	-	allows the idle interrupt request (IdleIRq bit) to be propagated to pin IRQ
3	HiAlertIEn	-	allows the high alert interrupt request (HiAlertIRq bit) to be propagated to pin IRQ
2	LoAlertIEn	-	allows the low alert interrupt request (LoAlertIRq bit) to be propagated to pin IRQ
1	ErrIEn	-	allows the error interrupt request (ErrIRq bit) to be propagated to pin IRQ
0	TimerIEn	-	allows the timer interrupt request (TimerIRq bit) to be propagated to pin IRQ

9.2.1.4 DivIEnReg register

Control bits to enable and disable the passing of interrupt requests.

Table 28. DivIEnReg register (address 03h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	IRQPushPull	reserved		MfinActIEn	reserved	CRCIEn	reserved	
Access	R/W	-		R/W	-	R/W	-	

Table 29. DivIEnReg register bit descriptions

Bit	Symbol	Value	Description
7	IRQPushPull	1	pin IRQ is a standard CMOS output pin
		0	pin IRQ is an open-drain output pin
6 to 5	reserved	-	reserved for future use
4	MfinActIEn	-	allows the MFIN active interrupt request to be propagated to pin IRQ
3	reserved	-	reserved for future use
2	CRCIEn	-	allows the CRC interrupt request, indicated by the DivIrqReg register's CRCIRq bit, to be propagated to pin IRQ
1 to 0	reserved	-	reserved for future use

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9.2.1.5 ComIrqReg register

Interrupt request bits.

Table 30. ComIrqReg register (address 04h); reset value: 14h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	Set1	TxIRq	RxIRq	IdleIRq	HiAlertIRq	LoAlertIRq	ErrIRq	TimerIRq
Access	W	D	D	D	D	D	D	D

Table 31. ComIrqReg register bit descriptions

All bits in the ComIrqReg register are cleared by software.

Bit	Symbol	Value	Description
7	Set1	1	indicates that the marked bits in the ComIrqReg register are set
		0	indicates that the marked bits in the ComIrqReg register are cleared
6	TxIRq	1	set immediately after the last bit of the transmitted data was sent out
5	RxIRq	1	receiver has detected the end of a valid data stream if the RxModeReg register's RxNoErr bit is set to logic 1, the RxIRq bit is only set to logic 1 when data bytes are available in the FIFO
4	IdleIRq	1	if a command terminates, for example, when the CommandReg changes its value from any command to the Idle command (see Table 150 on page 69) if an unknown command is started, the CommandReg register Command[3:0] value changes to the idle state and the IdleIRq bit is set the microcontroller starting the Idle command does not set the IdleIRq bit
3	HiAlertIRq	1	the Status1Reg register's HiAlert bit is set the HiAlertIRq bit stores this event and can only be reset as indicated by the Set1 bit in this register
2	LoAlertIRq	1	Status1Reg register's LoAlert bit is set the LoAlertIRq bit stores this event and can only be reset as indicated by the Set1 bit in this register
1	ErrIRq	1	any error bit in the ErrorReg register is set
0	TimerIRq	1	the timer decrements the timer value in register TCounterValReg to zero

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9.2.1.6 DivIrqReg register

Interrupt request bits.

Table 32. DivIrqReg register (address 05h); reset value: x0h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	Set2	reserved		MfinActIRq	reserved	CRCIRq	reserved	
Access	W	-		D	-	D	-	

Table 33. DivIrqReg register bit descriptions

All bits in the DivIrqReg register are cleared by software.

Bit	Symbol	Value	Description
7	Set2	1	indicates that the marked bits in the DivIrqReg register are set
		0	indicates that the marked bits in the DivIrqReg register are cleared
6 to 5	reserved	-	reserved for future use
4	MfinActIRq	1	MFIN is active; this interrupt is set when either a rising or falling signal edge is detected
3	reserved	-	reserved for future use
2	CRCIRq	1	the CalcCRC command is active and all data is processed
1 to 0	reserved	-	reserved for future use

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9.2.1.7 ErrorReg register

Error bit register showing the error status of the last command executed.

Table 34. ErrorReg register (address 06h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	WrErr	TempErr	reserved	BufferOvfl	CollErr	CRCErr	ParityErr	ProtocolErr
Access	R	R	-	R	R	R	R	R

Table 35. ErrorReg register bit descriptions

Bit	Symbol	Value	Description
7	WrErr	1	data is written into the FIFO buffer by the host during the MFAuthent command or if data is written into the FIFO buffer by the host during the time between sending the last bit on the RF interface and receiving the last bit on the RF interface
6	TempErr[1]	1	internal temperature sensor detects overheating, in which case the antenna drivers are automatically switched off
5	reserved	-	reserved for future use
4	BufferOvfl	1	the host or a MFRC523's internal state machine (e.g. receiver) tries to write data to the FIFO buffer even though it is already full
3	CollErr	1	a bit-collision is detected cleared automatically at receiver start-up phase only valid during the bitwise anticollision at 106 kBd always set to logic 0 during communication protocols at 212 kBd, 424 kBd and 848 kBd
2	CRCErr	1	the RxModeReg register's RxCRCEn bit is set and the CRC calculation fails automatically cleared to logic 0 during receiver start-up phase
1	ParityErr	1	parity check failed automatically cleared during receiver start-up phase only valid for ISO/IEC 14443 A/MIFARE communication at 106 kBd
0	ProtocolErr	1	set to logic 1 if the SOF is incorrect automatically cleared during receiver start-up phase bit is only valid for 106 kBd during the MFAuthent command, the ProtocolErr bit is set to logic 1 if the number of bytes received in one data stream is incorrect

[1] Command execution clears all error bits except the TempErr bit. Cannot be set by software.

9.2.1.8 Status1Reg register

Contains status bits of the CRC, interrupt and FIFO buffer.

Table 36. Status1Reg register (address 07h); reset value: 21h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	CRCOk	CRCReady	IRq	TRunning	reserved	HiAlert	LoAlert
Access	-	R	R	R	R	-	R	R

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Table 37. Status1Reg register bit descriptions

Bit	Symbol	Value	Description
7	reserved	-	reserved for future use
6	CRCOk	1	the CRC result is zero the CRCOk bit is undefined for data transmission and reception: use the ErrorReg register's CRCErr bit indicates the status of the CRC coprocessor, during calculation the value changes to logic 0, when the calculation is done correctly the value changes to logic 1
5	CRCReady	1	the CRC calculation has finished; only valid for the CRC coprocessor calculation using the CalcCRC command
4	IRq	-	indicates if any interrupt source requests attention with respect to the setting of the interrupt enable bits: see the ComIEnReg and DivIEnReg registers
3	TRunning	1	MFRC523's timer unit is running, i.e. the timer will decrement the TCounterValReg register with the next timer clock **Remark:** in gated mode, the TRunning bit is set to logic 1 when the timer is enabled by TModeReg register's TGated[1:0] bits; this bit is not influenced by the gated signal
2	reserved	-	reserved for future use
1	HiAlert	1	the alert level for the number of bytes in the FIFO buffer (FIFOLength[6:0]) is: $HiAlert = (64 - FIFOLength) \leq WaterLevel$ otherwise value = logic 0 Example: FIFOLength = 60, WaterLevel = 4 then HiAlert = logic 1 FIFOLength = 59, WaterLevel = 4 then HiAlert = logic 0
0	LoAlert	1	the alert level for number of bytes in the FIFO buffer (FIFOLength[6:0]) is: $LoAlert = FIFOLength \leq WaterLevel$ otherwise value = logic 0 Example: FIFOLength = 4, WaterLevel = 4 then LoAlert = logic 1 FIFOLength = 5, WaterLevel = 4 then LoAlert = logic 0

9.2.1.9 Status2Reg register

Contains status bits of the receiver, transmitter and data mode detector.

Table 38. Status2Reg register (address 08h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TempSensClear	I^2CForceHS	reserved		MFCrypto1On	ModemState[2:0]		
Access	R/W	R/W	-		D	R		

Table 39. Status2Reg register bit descriptions

Bit	Symbol	Value	Description
7	TempSensClear	1	clears the temperature error if the temperature is below the alarm limit of 125 °C

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Table 39. Status2Reg register bit descriptions *...continued*

Bit	Symbol	Value	Description
6	I^2CForceHS		I^2C-bus input filter settings:
		1	the I^2C-bus input filter is set to the High-speed mode independent of the I^2C-bus protocol
		0	the I^2C-bus input filter is set to the I^2C-bus protocol used
5 to 4	reserved	-	reserved
3	MFCrypto1On	-	indicates that the MIFARE Crypto1 unit is switched on and all data communication with the card is encrypted; this bit is cleared by software; can only be set to logic 1 by a successful execution of the MFAuthent command only valid in Read/Write mode for MIFARE standard cards
2 to 0	ModemState[2:0]	-	shows the state of the transmitter and receiver state machines:
		000	idle
		001	wait for the BitFramingReg register's StartSend bit
		010	TxWait: wait until RF field is present if the TModeReg register's TxWaitRF bit is set to logic 1. The minimum time for TxWait is defined by the TxWaitReg register
		011	transmitting
		100	RxWait: wait until RF field is present if the TModeReg register's TxWaitRF bit is set to logic 1. The minimum time for RxWait is defined by the RxWaitReg register
		101	wait for data
		110	receiving

9.2.1.10 FIFODataReg register

Input and output of 64 byte FIFO buffer.

Table 40. FIFODataReg register (address 09h); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	FIFOData[7:0]							
Access	D							

Table 41. FIFODataReg register bit descriptions

Bit	Symbol	Description
7 to 0	FIFOData[7:0]	data input and output port for the internal 64-byte FIFO buffer. FIFO buffer acts as parallel in/parallel out converter for all serial data stream inputs and outputs

9.2.1.11 FIFOLevelReg register

Indicates the number of bytes stored in the FIFO.

Table 42. FIFOLevelReg register (address 0Ah); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	FlushBuffer	FIFOLevel[6:0]						
Access	W	R						

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Table 43. FIFOLevelReg register bit descriptions

Bit	Symbol	Value	Description
7	FlushBuffer	1	immediately clears the internal FIFO buffer's read and write pointer and ErrorReg register's BufferOvfl bit. Reading this bit always returns 0
6 to 0	FIFOLevel[6:0]	-	indicates the number of bytes stored in the FIFO buffer. Writing to the FIFODataReg register increments and reading decrements the FIFOLevel value

9.2.1.12 WaterLevelReg register

Defines the level for FIFO under- and overflow warning.

Table 44. WaterLevelReg register (address 0Bh); reset value: 08h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved		WaterLevel[5:0]					
Access	-		R/W					

Table 45. WaterLevelReg register bit descriptions

Bit	Symbol	Description
7 to 6	reserved	reserved for future use
5 to 0	WaterLevel[5:0]	defines a warning level to indicate a FIFO buffer overflow or underflow: Status1Reg register's HiAlert bit is set to logic 1 if the remaining number of bytes in the FIFO buffer space is equal to, or less than the defined number of WaterLevel[5:0] bits Status1Reg register's LoAlert bit is set to logic 1 if equal to, or less than the WaterLevel[5:0] bits in the FIFO buffer **Remark:** to calculate values for HiAlert and LoAlert, see Section 9.2.1.9 on page 42.

9.2.1.13 ControlReg register

Miscellaneous control bits.

Table 46. ControlReg register (address 0Ch); reset value: 10h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TStopNow	TStartNow	reserved			RxLastBits[2:0]		
Access	W	W	-			R		

Table 47. ControlReg register bit descriptions

Bit	Symbol	Value	Description
7	TStopNow	1	timer stops immediately
6	TStartNow	1	timer starts immediately. Reading this bit always returns it to 0
5 to 3	reserved	-	reserved for future use
2 to 0	RxLastBits[2:0]	-	indicates the number of valid bits in the last received byte. If this value is zero, the whole byte is valid

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9.2.1.14 BitFramingReg register

Adjustments for bit-oriented frames.

Table 48. BitFramingReg register (address 0Dh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	StartSend	RxAlign[2:0]			reserved	TxLastBits[2:0]		
Access	W	R/W			-	R/W		

Table 49. BitFramingReg register bit descriptions

Bit	Symbol	Value	Description
7	StartSend	1	starts the transmission of data only valid in combination with the Transceive command
6 to 4	RxAlign[2:0]		used for reception of bit-oriented frames: defines the bit position for the first bit received to be stored in the FIFO buffer example:
		0	LSB of the received bit is stored at bit position 0, the second received bit is stored at bit position 1
		1	LSB of the received bit is stored at bit position 1, the second received bit is stored at bit position 2
		7	LSB of the received bit is stored at bit position 7, the second received bit is stored in the next byte that follows at bit position 0 These bits are only to be used for bitwise anticollision at 106 kBd, for all other modes they are set to 0
3	reserved	-	reserved for future use
2 to 0	TxLastBits[2:0]	-	used for transmission of bit oriented frames: defines the number of bits of the last byte that will be transmitted. 000b indicates that all bits of the last byte will be transmitted

9.2.1.15 CollReg register

Defines the first bit-collision detected on the RF interface.

Table 50. CollReg register (address 0Eh); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	ValuesAfterColl	reserved	CollPosNotValid	CollPos[4:0]				
Access	R/W	-	R	R				

Table 51. CollReg register bit descriptions

Bit	Symbol	Value	Description
7	ValuesAfterColl	0	all received bits will be cleared after a collision only used during bitwise anticollision at 106 kBd, otherwise it is set to logic 1
6	reserved	-	reserved for future use
5	CollPosNotValid	1	no collision detected or the position of the collision is out of the range of CollPos[4:0]

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Table 51. CollReg register bit descriptions *...continued*

Bit	Symbol	Value	Description
4 to 0	CollPos[4:0]	-	shows the bit position of the first detected collision in a received frame only data bits are interpreted example:
		00h	indicates a bit-collision in the 32nd bit
		01h	indicates a bit-collision in the 1st bit
		08h	indicates a bit-collision in the 8th bit these bits will only be interpreted if the CollPosNotValid bit is set to logic 0

9.2.1.16 Reserved register 0Fh

Functionality is reserved for future use.

Table 52. Reserved register (address 0Fh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 53. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

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9.2.2.1 Reserved register 10h

Functionality is reserved for future use.

Table 54. Reserved register (address 10h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 55. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

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9.2.2.2 ModeReg register

Defines general mode settings for transmitting and receiving.

Table 56. ModeReg register (address 11h); reset value: 3Fh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	MSBFirst	reserved	TxWaitRF	reserved	PolMFin	reserved	CRCPreset[1:0]	
Access	R/W	-	R/W	-	R/W	-	R/W	

Table 57. ModeReg register bit descriptions

Bit	Symbol	Value	Description
7	MSBFirst	1	CRC coprocessor calculates the CRC with MSB first. In the CRCResultReg register the values for the CRCResultMSB[7:0] bits and the CRCResultLSB[7:0] bits are bit reversed **Remark:** during RF communication this bit is ignored
6	reserved	-	reserved for future use
5	TxWaitRF	1	transmitter can only be started if an RF field is generated
4	reserved	-	reserved for future use
3	PolMFin		defines the polarity of pin MFIN **Remark:** the internal envelope signal is encoded active LOW, changing this bit generates a MFinActIRq event
		1	polarity of pin MFIN is active HIGH
		0	polarity of pin MFIN is active LOW
2	reserved	-	reserved for future use
1 to 0	CRCPreset [1:0]		defines the preset value for the CRC coprocessor for the CalcCRC command **Remark:** during any communication, the preset values are selected automatically according to the definition of bits in the RxModeReg and TxModeReg registers
		00	0000h
		01	6363h
		10	A671h
		11	FFFFh

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9.2.2.3 TxModeReg register

Defines the data rate during transmission.

Table 58. TxModeReg register (address 12h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TxCRCEn	TxSpeed[2:0]			InvMod	TxFraming		
Access	R/W	D			R/W	D		

Table 59. TxModeReg register bit descriptions

Bit	Symbol	Value	Description
7	TxCRCEn	1	enables CRC generation during data transmission **Remark:** can only be set to logic 0 at 106 kBd
6 to 4	TxSpeed[2:0]		defines the bit rate during data transmission the MFRC523 handles transfer speeds up to 848 kBd
		000	106 kBd
		001	212 kBd
		010	424 kBd
		011	848 kBd
		100	reserved
		101	reserved
		110	reserved
		111	reserved
3	InvMod	1	modulation of transmitted data is inverted
2 to 0	TxFraming[1:0]		defines the framing used for data transmission
		00	ISO/IEC 14443 A/MIFARE
		01	reserved
		10	reserved
		11	ISO/IEC 14443 B

9.2.2.4 RxModeReg register

Defines the data rate during reception.

Table 60. RxModeReg register (address 13h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RxCRCEn	RxSpeed[2:0]			RxNoErr	RxMultiple	RxFraming	
Access	R/W	D			R/W	R/W	D	

Table 61. RxModeReg register bit descriptions

Bit	Symbol	Value	Description
7	RxCRCEn	1	enables the CRC calculation during reception **Remark:** can only be set to logic 0 at 106 kBd

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Table 61. RxModeReg register bit descriptions *...continued*

Bit	Symbol	Value	Description
6 to 4	RxSpeed[2:0]		defines the bit rate while receiving data. The MFRC523 manages transfer speeds up to 848 kBd
		000	106 kBd
		001	212 kBd
		010	424 kBd
		011	848 kBd
		100	reserved
		101	reserved
		110	reserved
		111	reserved
3	RxNoErr	1	an invalid received data stream (less than 4 bits received) will be ignored and the receiver remains active
2	RxMultiple	0	receiver is deactivated after receiving a data frame
		1	able to receive more than one data frame only valid for data rates above 106 kBd in order to handle the polling command after setting this bit, the Receive and Transceive commands will not terminate automatically. Multiple reception can only be deactivated by writing any command (except the Receive command) to the CommandReg register, or by the host clearing the bit if set to logic 1, an error byte is added to the FIFO buffer at the end of a received data stream which is a copy of the ErrorReg register value For version 1.0 please see Section 11.
1 to 0	RxFraming		defines the expected framing for data reception
		00	ISO/IEC 14443 A/MIFARE
		01	reserved
		10	reserved
		11	ISO/IEC 14443 B

9.2.2.5 TxControlReg register

Controls the logical behavior of the antenna driver pins TX1 and TX2.

Table 62. TxControlReg register (address 14h); reset value: 80h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	InvTx2RFOn	InvTx1RFOn	InvTx2RFOff	InvTx1RFOff	Tx2CW	reserved	Tx2RFEn	Tx1RFEn
Access	R/W	R/W	R/W	R/W	R/W	-	R/W	R/W

Table 63. TxControlReg register bit descriptions

Bit	Symbol	Value	Description
7	InvTx2RFOn	1	output signal on pin TX2 inverted when driver TX2 is enabled
6	InvTx1RFOn	1	output signal on pin TX1 inverted when driver TX1 is enabled
5	InvTx2RFOff	1	output signal on pin TX2 inverted when driver TX2 is disabled

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Table 63. TxControlReg register bit descriptions *...continued*

Bit	Symbol	Value	Description
4	InvTx1RFOff	1	output signal on pin TX1 inverted when driver TX1 is disabled
3	Tx2CW	1	output signal on pin TX2 continuously delivers the unmodulated 13.56 MHz energy carrier
		0	Tx2CW bit is enabled to modulate the 13.56 MHz energy carrier
2	reserved	-	reserved for future use
1	Tx2RFEn	1	output signal on pin TX2 delivers the 13.56 MHz energy carrier modulated by the transmission data
0	Tx1RFEn	1	output signal on pin TX1 delivers the 13.56 MHz energy carrier modulated by the transmission data

9.2.2.6 TxASKReg register

Controls transmit modulation settings.

Table 64. TxASKReg register (address 15h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	Force100ASK	reserved					
Access	-	R/W	-					

Table 65. TxASKReg register bit descriptions

Bit	Symbol	Value	Description
7	reserved	-	reserved for future use
6	Force100ASK	1	forces 100 % ASK modulation independently of the ModGsPReg register setting
5 to 0	reserved	-	reserved for future use

9.2.2.7 TxSelReg register

Selects the internal sources for the analog module.

Table 66. TxSelReg register (address 16h); reset value: 10h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol:	reserved		DriverSel[1:0]		MFOutSel[3:0]			
Access:	-		R/W		R/W			

Table 67. TxSelReg register bit descriptions

Bit	Symbol	Value	Description
7 to 6	reserved	-	reserved for future use
5 to 4	DriverSel[1:0]	-	selects the input of drivers TX1 and TX2
		00	3-state; in soft power-down the drivers are only in 3-state mode if the DriverSel[1:0] value is set to 3-state mode
		01	modulation signal (envelope) from the internal encoder, Miller pulse encoded
		10	modulation signal (envelope) from pin MFIN
		11	HIGH; the HIGH level depends on the setting of bits InvTx1RFOn/InvTx1RFOff and InvTx2RFOn/InvTx2RFOff

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Table 67. TxSelReg register bit descriptions *...continued*

Bit	Symbol	Value	Description
3 to 0	MFOutSel[3:0]		selects the input for pin MFOUT
		0000	3-state
		0001	LOW
		0010	HIGH
		0011	test bus signal as defined by the TestSel1Reg register's TstBusBitSel[2:0] value
		0100	modulation signal (envelope) from the internal encoder, Miller pulse encoded
		0101	serial data stream to be transmitted, data stream before Miller encoder
		0110	reserved
		0111	serial data stream received, data stream after Manchester decoder
		1000 to 1111	reserved

9.2.2.8 RxSelReg register

Selects internal receiver settings.

Table 68. RxSelReg register (address 17h); reset value: 84h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	UARTSel[1:0]		RxWait[5:0]					
Access	R/W		R/W					

Table 69. RxSelReg register bit descriptions

Bit	Symbol	Value	Description
7 to 6	UARTSel[1:0]		selects the input of the contactless UART
		00	constant LOW
		01	Manchester with subcarrier from pin MFIN
		10	modulated signal from the internal analog module, default
		11	NRZ coding without subcarrier from pin MFIN which is only valid for transfer speeds above 106 kBd
5 to 0	RxWait[5:0]	-	after data transmission the activation of the receiver is delayed for RxWait bit-clocks, during this 'frame guard time' any signal on pin RX is ignored this parameter is ignored by the Receive command all other commands, such as Transceive, MFAuthent use this parameter the counter starts immediately after the external RF field is switched on

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9.2.2.9 RxThresholdReg register

Selects thresholds for the bit decoder.

Table 70. RxThresholdReg register (address 18h); reset value: 84h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	MinLevel[3:0]				reserved	CollLevel[2:0]		
Access	R/W				-	R/W		

Table 71. RxThresholdReg register bit descriptions

Bit	Symbol	Description
7 to 4	MinLevel[3:0]	defines the minimum signal strength at the decoder input that will be accepted. If the signal strength is below this level it is not evaluated
3	reserved	reserved for future use
2 to 0	CollLevel[2:0]	defines the minimum signal strength at the decoder input that must be reached by the weaker half-bit of the Manchester encoded signal to generate a bit-collision relative to the amplitude of the stronger half-bit

9.2.2.10 DemodReg register

Defines demodulator settings.

Table 72. DemodReg register (address 19h); reset value: 4Dh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	AddIQ[1:0]		FixIQ	TPrescal Even	TauRcv[1:0]		TauSync[1:0]	
Access	R/W		R/W	-	R/W		R/W	

Table 73. DemodReg register bit descriptions

Bit	Symbol	Value	Description
7 to 6	AddIQ[1:0]	-	defines the use of I-channel and Q-channel during reception **Remark:** the FixIQ bit must be set to logic 0 to enable the following settings:
		00	selects the stronger channel
		01	selects the stronger channel and freezes the selected channel during communication
		10	reserved
		11	reserved
5	FixIQ	1	if the bits of AddIQ are set to X0, the reception is fixed to I-channel if the bits of AddIQ are set to X1, the reception is fixed to Q-channel

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Table 73. DemodReg register bit descriptions *…continued*

Bit	Symbol	Value	Description
4	TPrescalEven	0	the following formula is used to calculate f_{Timer} of the prescaler: f_{Timer} = 13.56 MHz / (2 * TPreScaler + 1).
		1	the following formula is used to calculate f_{Timer} of the prescaler: f_{Timer} = 13.56 MHz / (2 * TPreScaler + 2). (Default TPrescalEven is logic 0) This cannot be used in version, see Section 11 “Errata sheet”
3 to 2	TauRcv[1:0]	-	changes the time-constant of the internal PLL during data reception **Remark:** if set to 00b the PLL is frozen during data reception
1 to 0	TauSync[1:0]	-	changes the time constant of the internal PLL during burst

9.2.2.11 Reserved register 1Ah

Functionality is reserved for future use.

Table 74. Reserved register (address 1Ah); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 75. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

9.2.2.12 Reserved register 1Bh

Functionality is reserved for future use.

Table 76. Reserved register (address 1Bh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 77. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

9.2.2.13 MfTxReg register

Controls some MIFARE communication transmit parameters.

Table 78. MfTxReg register (address 1Ch); reset value: 62h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved						TxWait[1:0]	
Access	-						R/W	

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Table 79. MfTxReg register bit descriptions

Bit	Symbol	Description
7 to 2	reserved	reserved for future use
1 to 0	TxWait	defines the additional response time. 7 bits are added to the value of the register bit by default

9.2.2.14 MfRxReg register

Table 80. MfRxReg register (address 1Dh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved			ParityDisable	reserved			
Access	-			R/W	-			

Table 81. MfRxReg register bit descriptions

Bit	Symbol	Value	Description
7 to 5	reserved	-	reserved for future use
4	ParityDisable	1	generation of the parity bit for transmission and the parity check for receiving is switched off. The received parity bit is handled like a data bit
3 to 0	reserved	-	reserved for future use

9.2.2.15 TypeBReg register

Configures the ISO/IEC 14443 B functionality.

Table 82. TypeBReg register (address 1Eh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RxSOFReq	RxEOFReq	reserved	EOFSOF Width	NoTxSOF	NoTxEOF	TxEGT[1:0]	
Access	R/W	R/W	-	R/W	R/W	R/W	R/W	

Table 83. TypeBReg register bit descriptions

Bit	Symbol	Value	Description
7	RxSOFReq	1	requires SOF; a datastream starting without SOF is ignored
		0	accepts a datastream starting with or without SOF; an SOF is removed and not written into the FIFO
6	RxEOFReq	1	requires EOF; a datastream ending without EOF generates a protocol error
		0	accepts a datastream ending with or without EOF; an EOF is removed and not written into the FIFO
5	reserved	-	reserved for future use

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Table 83. TypeBReg register bit descriptions *...continued*

Bit	Symbol	Value	Description
4	EOFSOFWidth	1	if this bit is set to logic 1 and EOFSOFAdjust bit (AutoTestReg register) is logic 0, the SOF and EOF will have the maximum length defined in ISO/IEC 14443 B. if this bit is set to logic 1 and the EOFSOFAadjust bit is logic 1: then SOF low = (11 ETU − 8 cycles) / f_{clk} SOF high = (2 ETU + 8 cycles) / f_{clk} EOF low = (11 ETU − 8 cycles) / f_{clk}
		0	if this bit is cleared and EOFSOFAdjust bit is logic 0, the SOF and EOF will have the minimum length defined in ISO/IEC 14443 B. if this bit is set to logic 0 and the EOFSOFAdjust bit is logic 1 results in an incorrect system behavior in respect to ISO specification
3	NoTxSOF	1	SOF is suppressed
2	NoTxEOF	1	EOF is suppressed
1 to 0	TxEGT		defines EGT bit length
		00	no bits
		01	1 bit
		10	2 bits
		11	3 bits

For the available configuration on version 1.0, please see Section 11.

9.2.2.16 SerialSpeedReg register

Selects the speed of the serial UART interface.

Table 84. SerialSpeedReg register (address 1Fh); reset value: EBh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	BR_T0[2:0]			BR_T1[4:0]				
Access	R/W			R/W				

Table 85. SerialSpeedReg register bit descriptions

Bit	Symbol	Description
7 to 5	BR_T0[2:0]	factor BR_T0 adjusts the transfer speed: for description, see Section 8.3.3.2 on page 12
4 to 0	BR_T1[4:0]	factor BR_T1 adjusts the transfer speed: for description, see Section 8.3.3.2 on page 12

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9.2.3 Page 2: Configuration

9.2.3.1 Reserved register 20h

Functionality is reserved for future use.

Table 86. Reserved register (address 20h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 87. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

9.2.3.2 CRCResultReg registers

Shows the MSB and LSB values of the CRC calculation.

Remark: The CRC is split into two 8-bit registers.

Table 88. CRCResultReg (higher bits) register (address 21h); reset value: FFh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CRCResultMSB[7:0]							
Access	R							

Table 89. CRCResultReg register higher bit descriptions

Bit	Symbol	Description
7 to 0	CRCResultMSB[7:0]	shows the value of the CRCResultReg register's most significant byte. Only valid if Status1Reg register's CRCReady bit is set to logic 1

Table 90. CRCResultReg (lower bits) register (address 22h); reset value: FFh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CRCResultLSB[7:0]							
Access	R							

Table 91. CRCResultReg register lower bit descriptions

Bit	Symbol	Description
7 to 0	CRCResultLSB[7:0]	shows the value of the least significant byte of the CRCResultReg register. Only valid if Status1Reg register's CRCReady bit is set to logic 1

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9.2.3.3 Reserved register 23h

Functionality is reserved for future use.

Table 92. Reserved register (address 23h); reset value: 88h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 93. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

9.2.3.4 ModWidthReg register

Sets the modulation width.

Table 94. ModWidthReg register (address 24h); reset value: 26h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	ModWidth[7:0]							
Access	R/W							

Table 95. ModWidthReg register bit descriptions

Bit	Symbol	Description
7 to 0	ModWidth[7:0]	defines the width of the Miller modulation as multiples of the carrier frequency (ModWidth + 1 / f_{clk}). The maximum value is half the bit period

9.2.3.5 Reserved register 25h

Functionality is reserved for future use.

Table 96. Reserved register (address 25h); reset value: 87h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 97. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

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9.2.3.6 RFCfgReg register

Configures the receiver gain.

Table 98. RFCfgReg register (address 26h); reset value: 48h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	RxGain[2:0]			reserved			
Access	-	R/W			-			

Table 99. RFCfgReg register bit descriptions

Bit	Symbol	Value	Description
7	reserved	-	reserved for future use
6 to 4	RxGain[2:0]		defines the receiver's signal voltage gain factor:
		000	18 dB
		001	23 dB
		010	18 dB
		011	23 dB
		100	33 dB
		101	38 dB
		110	43 dB
		111	48 dB
3 to 0	reserved	-	reserved for future use

9.2.3.7 GsNReg register

Defines the conductance of the antenna driver pins TX1 and TX2 for the n-driver when the driver is switched on.

Table 100. GsNReg register (address 27h); reset value: 88h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CWGsN[3:0]				ModGsN[3:0]			
Access	R/W				R/W			

Table 101. GsNReg register bit descriptions

Bit	Symbol	Description
7 to 4	CWGsN[3:0]	defines the conductance of the output n-driver during periods without modulation which can be used to regulate the output power and subsequently current consumption and operating distance. The value is only used if driver TX1 or TX2 is switched on during Soft power-down mode the highest bit is forced to logic 1 **Remark:** the conductance value is binary-weighted
3 to 0	ModGsN[3:0]	defines the conductance of the output n-driver during periods without modulation which can be used to regulate the modulation index. The value is only used if driver TX1 or TX2 is switched on during Soft power-down mode the highest bit is forced to logic 1 **Remark:** the conductance value is binary weighted

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9.2.3.8 CWGsPReg register

Defines the conductance of the p-driver output during periods of no modulation.

Table 102. CWGsPReg register (address 28h); reset value: 20h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved		CWGsP[5:0]					
Access	-		R/W					

Table 103. CWGsPReg register bit descriptions

Bit	Symbol	Description
7 to 6	reserved	reserved for future use
5 to 0	CWGsP[5:0]	defines the conductance of the p-driver output which can be used to regulate the output power and subsequently current consumption and operating distance during Soft power-down mode the highest bit is forced to logic 1 **Remark:** the conductance value is binary weighted

9.2.3.9 ModGsPReg register

Defines the conductance of the p-driver output during modulation.

Table 104. ModGsPReg register (address 29h); reset value: 20h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved		ModGsP[5:0]					
Access	-		R/W					

Table 105. ModGsPReg register bit descriptions

Bit	Symbol	Description
7 to 6	reserved	reserved for future use
5 to 0	ModGsP[5:0]	defines the conductance of the p-driver output during modulation which can be used to regulate the modulation index. If the TxASKReg register's Force100ASK bit is set to logic 1 the value of ModGsP has no effect during Soft power-down mode the highest bit is forced to logic 1 **Remark:** the conductance value is binary weighted

9.2.3.10 TModeReg and TPrescalerReg registers

These registers define the timer settings.

Remark: The TPrescaler setting higher 4 bits are in the TModeReg register and the lower 8 bits are in the TPrescalerReg register.

Table 106. TModeReg register (address 2Ah); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TAuto	TGated[1:0]		TAutoRestart	TPrescaler_Hi[3:0]			
Access	R/W	R/W		R/W	R/W			

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Table 107. TModeReg register bit descriptions

Bit	Symbol	Value	Description
7	TAuto	1	the timer starts automatically at the end of the transmission in all communication modes at all speeds or when InvTxnRFOn bits are set to logic 1 and the RF field is switched on when RxMultiple bit in register RxModeReg is logic 0: in MIFARE mode and ISO/IEC 14443 B at 106 kBd, the timer stops after the 5th bit (1 start bit, 4 data bits). In all other modes, the timer stops after the 4th bit if the RxMultiple bit is set to logic 1, the timer never stops. In this case the timer can be stopped by setting the TStopNow bit in register ControlReg to logic 1
		0	indicates that the timer is not influenced by the protocol
6 to 5	TGated[1:0]		internal timer is runs in gated or non-gated mode **Remark:** in gated mode, the Status1Reg register's TRunning bit is logic 1 when the timer is enabled by the TModeReg register bits these bits do not influence the gating signal
		00	non-gated mode
		01	gated by pin MFIN
		10	gated by pin AUX1
		11	-
4	TAutoRestart	1	timer automatically restarts its count-down from the 16-bit timer reload value instead of counting down to zero
		0	timer decrements to 0 and the ComIrqReg register's TimerIRq bit is set to logic 1
3 to 0	TPrescaler_Hi[3:0]	-	defines the higher 4 bits of the TPrescaler value the following formula is used to calculate f_{Timer} if TPrescalEven bit in Demod Reg is set to logic 0: f_{Timer} = 13.56 MHz / (2 * TPreScaler + 1). where TPreScaler = [TPrescaler_Hi:TPrescaler_Lo] (TPrescaler value on 12 bits). The default TPrescalEven is logic 0 the following formula is used to calculate f_{Timer} if TPrescalEven bit in Demod Reg is set to logic 1: f_{Timer} = 13.56 MHz / (2 * TPreScaler + 2); see Section 8.7 "Timer unit" For the value applicable for version 1.0, see Section 11.

Table 108. TPrescalerReg register (address 2Bh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TPrescaler_Lo[7:0]							
Access	R/W							

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Table 109. TPrescalerReg register bit descriptions

Bit	Symbol	Description
7 to 0	TPrescaler_Lo[7:0]	defines the lower 8 bits of the TPrescaler value the following formula is used to calculate f_{Timer} if TPrescalEven bit in Demot Reg is set to logic 0: f_{Timer} = 13.56 MHz / (2 * TPreScaler + 1) where TPreScaler = [TPrescaler_Hi:TPrescaler_Lo] (TPrescaler value on 12 bits). The default TPrescalEven is logic 0; f_{Timer} = 13.56 MHz / (2 * TPreScaler + 2); see Section 8.7 “Timer unit” The value applicable for version 1.0 can be seen at Section 11.

9.2.3.11 TReloadReg register

Defines the 16-bit timer reload value.

Remark: The reload value bits are contained in two 8-bit registers.

Table 110. TReloadReg (higher bits) register (address 2Ch); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TReloadVal_Hi[7:0]							
Access	R/W							

Table 111. TReloadReg register higher bit descriptions

Bit	Symbol	Description
7 to 0	TReloadVal_Hi[7:0]	defines the higher 8 bits of the 16-bit timer reload value. On a start event, the timer loads the timer reload value. Changing this register affects the timer only at the next start event

Table 112. TReloadReg (lower bits) register (address 2Dh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TReloadVal_Lo[7:0]							
Access	R/W							

Table 113. TReloadReg register lower bit descriptions

Bit	Symbol	Description
7 to 0	TReloadVal_Lo[7:0]	defines the lower 8 bits of the 16-bit timer reload value. On a start event, the timer loads the timer reload value. Changing this register affects the timer only at the next start event

9.2.3.12 TCounterValReg register

Contains the timer value.

Remark: The timer value bits are contained in two 8-bit registers.

Table 114. TCounterValReg (higher bits) register (address 2Eh); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TCounterVal_Hi[7:0]							
Access	R							

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Table 115. TCounterValReg register higher bit descriptions

Bit	Symbol	Description
7 to 0	TCounterVal_Hi[7:0]	timer value higher 8 bits

Table 116. TCounterValReg (lower bits) register (address 2Fh); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TCounterVal_Lo[7:0]							
Access	R							

Table 117. TCounterValReg register lower bit descriptions

Bit	Symbol	Description
7 to 0	TCounterVal_Lo[7:0]	timer value lower 8 bits

9.2.4 Page 3: Test

9.2.4.1 Reserved register 30h

Functionality is reserved for future use.

Table 118. Reserved register (address 30h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 119. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

9.2.4.2 TestSel1Reg register

General test signal configuration.

Table 120. TestSel1Reg register (address 31h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved					TstBusBitSel[2:0]		
Access	-					R/W		

Table 121. TestSel1Reg register bit descriptions

Bit	Symbol	Description
7 to 3	reserved	reserved for future use
2 to 0	TstBusBitSel[2:0]	selects a test bus signal which is output at pin MFOUT. If AnalogSelAux2[3:0] = FFh in AnalogTestReg register, test bus signal is also output at pins AUX1 or AUX2

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9.2.4.3 TestSel2Reg register

General test signal configuration and PRBS control.

Table 122. TestSel2Reg register (address 32h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TstBusFlip	PRBS9	PRBS15	TestBusSel[4:0]				
Access	R/W	R/W	R/W	R/W				

Table 123. TestSel2Reg register bit descriptions

Bit	Symbol	Value	Description
7	TstBusFlip	1	test bus is mapped to the parallel port in the following order: TstBusBit4,TstBusBit3, TstBusBit2, TstBusBit6, TstBusBit5, TstBusBit0; see Section 17.1 on page 82
6	PRBS9	-	starts and enables the PRBS9 sequence according to ITU-TO150; the data transmission of the defined sequence is started by the Transmit command **Remark:** all relevant registers to transmit data must be configured before entering PRBS9 mode
5	PRBS15	-	starts and enables the PRBS15 sequence according to ITU-TO150; the data transmission of the defined sequence is started by the Transmit command **Remark:** all relevant registers to transmit data must be configured before entering PRBS15 mode
4 to 0	TestBusSel[4:0]	-	selects the test bus; see Section 17.1 “Test signals” on page 82

9.2.4.4 TestPinEnReg register

Enables the test bus pin output driver.

Table 124. TestPinEnReg register (address 33h); reset value: 80h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RS232LineEn	TestPinEn[5:0]						reserved
Access	R/W	R/W						-

Table 125. TestPinEnReg register bit descriptions

Bit	Symbol	Value	Description
7	RS232LineEn	0	serial UART lines MX and DTRQ are disabled
6 to 1	TestPinEn[5:0]	-	enables the output driver on one of the data pins D1 to D7 which outputs a test signal **Example:** setting bit 1 to logic 1 enables pin D1 output setting bit 5 to logic 1 enables pin D5 output **Remark:** If the SPI is used, only pins D1 to D4 can be used. If the serial UART interface is used and the RS232LineEn bit is set to logic 1 only pins D1 to D4 can be used.
0	reserved	-	reserved for future use

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9.2.4.5 TestPinValueReg register

Defines the high and low values for the test port D1 to D7 when it is used as I/O.

Table 126. TestPinValueReg register (address 34h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	UseIO	TestPinValue[5:0]						reserved
Access	R/W	R/W						-

Table 127. TestPinValueReg register bit descriptions

Bit	Symbol	Value	Description
7	UseIO	1	enables the I/O functionality for the test port when one of the serial interfaces is used. The input/output behavior is defined by value TestPinEn[5:0] in the TestPinEnReg register
6 to 1	TestPinValue[5:0]	-	defines the value of the test port when it is used as I/O and each output must be enabled by TestPinEn[5:0] in the TestPinEnReg register **Remark:** Reading the register indicates the status of pins D6 to D1 if the UseIO bit is set to logic 1. If the UseIO bit is set to logic 0, the value of the TestPinValueReg register is read back.
0	reserved	-	reserved for future use

9.2.4.6 TestBusReg register

Shows the status of the internal test bus.

Table 128. TestBusReg register (address 35h); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TestBus[7:0]							
Access	R							

Table 129. TestBusReg register bit descriptions

Bit	Symbol	Description
7 to 0	TestBus[7:0]	shows the status of the internal test bus. The test bus is selected using the TestSel2Reg register; see Section 17.1 on page 82

9.2.4.7 AutoTestReg register

Controls the digital self-test.

Table 130. AutoTestReg register (address 36h); reset value: 40h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	AmpRcv	reserved	EOFSOF Adjust	SelfTest[3:0]			
Access	-	R/W	-	R/W	R/W			

For the configuration on version 1.0, please see Section 11.

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Table 131. AutoTestReg register bit descriptions

Bit	Symbol	Value	Description
7	reserved	-	reserved for production tests
6	AmpRcv	1	internal signal processing in the receiver chain is performed non-linearly which increases the operating distance in communication modes at 106 kBd **Remark:** due to non-linearity, the effect of the RxThresholdReg register's MinLevel[3:0] and the CollLevel[2:0] values is also non-linear
5	reserved	-	reserved for production tests
4	EOFSOFAdjust	0	If set to logic 0 and the EOFSOFwidth bit is set to logic 1 it results in the maximum length of SOF and EOF according to ISO/IEC 14443 B If set to logic 0 and the EOFSOFwidth bit is set to logic 0 it results in the minimum length of SOF and EOF according to ISO/IEC 14443 B
		1	If this bit is set to logic 1 and the EOFSOFwidth bit is logic 1, it results in SOF high = (2 ETU + 8 cycles) / f_{clk} SOF low = (11 ETU – 8 cycles) / f_{clk} EOF low = (11 ETU – 8 cycles) / f_{clk}
3 to 0	SelfTest[3:0]	-	enables the digital self-test. The self-test can also be started by the CalcCRC command; see Section 10.3.1.4 "CalcCRC command" on page 70. Self-test is enabled by 1001b. **Remark:** for default operation the self-test must be disabled by 0000b

9.2.4.8 VersionReg register

Shows the MFRC523 software version.

Table 132. VersionReg register (address 37h); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	Version[7:0]							
Access	R							

Table 133. VersionReg register bit descriptions

Bit	Symbol	Description
7 to 0	Version[7:0]	indicates current MFRC523 software version. The value for the version 1.0 is B1h (see Section 11) and the value for the version 2.0 is B2h.

9.2.4.9 AnalogTestReg register

Determines the analog output test signal at, and status of, pins AUX1 and AUX2.

Table 134. AnalogTestReg register (address 38h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	AnalogSelAux1[3:0]				AnalogSelAux2[3:0]			
Access	R/W				R/W			

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Table 135. AnalogTestReg register bit descriptions

Bit	Symbol	Value	Description
7 to 4	AnalogSelAux1[3:0]		controls pin AUX1
		0000	3-state
		0001	output of TestDAC1 (AUX1), output of TestDAC2 (AUX2)[1]
		0010	test signal Corr1[1]
		0011	reserved
		0100	DAC: test signal MinLevel[1]
		0101	DAC: test signal ADC_I[1]
		0110	DAC: test signal ADC_Q[1]
		0111	reserved
		1000	reserved, test signal for production test[1]
		1001	reserved
		1010	HIGH
		1011	LOW
		1100	TxActive: 106 kBd: HIGH during start bit, data bit, parity and CRC 212 kBd, 424 kBd and 848 kBd: HIGH during data and CRC
		1101	RxActive: 106 kBd: HIGH during data bit, parity and CRC 212 kBd, 424 kBd and 848 kBd: HIGH during data and CRC
		1110	subcarrier detected: 106 kBd: not applicable 212 kBd: 424 kBd and 848 kBd: HIGH during last part of data and CRC
		1111	test bus bit as defined by the TestSel1Reg register's TstBusBitSel[2:0] bits **Remark:** all test signals are described in Section 17.1 "Test signals" on page 82
3 to 0	AnalogSelAux2[3:0]	-	controls pin AUX2 (see bit descriptions for AUX1)

[1] **Remark:** Current source output; the use of 1 kΩ pull-down resistor on AUXn is recommended.

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9.2.4.10 TestDAC1Reg register

Defines the test value for TestDAC1.

Table 136. TestDAC1Reg register (address 39h); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved		TestDAC1[5:0]					
Access	-		R/W					

Table 137. TestDAC1Reg register bit descriptions

Bit	Symbol	Description
7	reserved	reserved for production tests
6	reserved	reserved for future use
5 to 0	TestDAC1[5:0]	defines the test value for TestDAC1. Output of DAC1 can be routed to AUX1 by setting value AnalogSelAux1[3:0] to 0001b in the AnalogTestReg register

9.2.4.11 TestDAC2Reg register

Defines the test value for TestDAC2.

Table 138. TestDAC2Reg register (address 3Ah); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved		TestDAC2[5:0]					
Access	-		R/W					

Table 139. TestDAC2Reg register bit descriptions

Bit	Symbol	Description
7 to 6	reserved	reserved for future use
5 to 0	TestDAC2[5:0]	defines the test value for TestDAC2. DAC2 output can be routed to AUX2 by setting value AnalogSelAux2[3:0] to 0001b in the AnalogTestReg register

9.2.4.12 TestADCReg register

Shows the values of ADC I-channel and Q-channel.

Table 140. TestADCReg register (address 3Bh); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	ADC_I[3:0]				ADC_Q[3:0]			
Access	R				R			

Table 141. TestADCReg register bit descriptions

Bit	Symbol	Description
7 to 4	ADC_I[3:0]	ADC I-channel value
3 to 0	ADC_Q[3:0]	ADC Q-channel value

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9.2.4.13 Reserved register 3Ch

Functionality reserved for production test.

Table 142. Reserved register (address 3Ch); reset value: FFh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 143. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for production tests

Table 144. Reserved register (address 3Dh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 145. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for production tests

Table 146. Reserved register (address 3Eh); reset value: 03h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 147. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for production tests

Table 148. Reserved register (address 3Fh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 149. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for production tests

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10. MFRC523 command set

The MFRC523 operation is determined by a state machine capable of performing a set of commands. A command is executed by writing a command code (see Table 150) to the CommandReg register.

Arguments and data necessary to process a command are exchanged using the FIFO buffer.

10.1 General description

The MFRC523 operation is determined by a state machine capable of performing a set of commands. A command is executed by writing a command code (see Table 150) to the CommandReg register.

Arguments and/or data necessary to process a command are exchanged via the FIFO buffer.

10.2 General behavior

- Each command that needs a data bit stream (or data byte stream) as an input immediately processes any data in the FIFO buffer. An exception to this rule is the Transceive command. Using this command, transmission is started with the BitFramingReg register's StartSend bit.
- Each command that needs a certain number of arguments, starts processing only when it has received the correct number of arguments from the FIFO buffer.
- The FIFO buffer is not automatically cleared when commands start. This makes it possible to write command arguments and/or the data bytes to the FIFO buffer and then start the command.
- Each command can be interrupted by the host writing a new command code to the CommandReg register, for example, the Idle command.

10.3 MFRC523 command overview

Table 150. Command overview

Command	Command code	Action
Idle	0000	no action, cancels current command execution
Mem	0001	stores 25 bytes into the internal buffer
Generate RandomID	0010	generates a 10-byte random ID number
CalcCRC	0011	activates the CRC coprocessor or performs a self-test
Transmit	0100	transmits data from the FIFO buffer
NoCmdChange	0111	no command change, can be used to modify the CommandReg register bits without affecting the command, for example, the PowerDown bit
Receive	1000	activates the receiver circuits
Transceive	1100	transmits data from FIFO buffer to antenna and automatically activates the receiver after transmission

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Table 150. Command overview *...continued*

Command	Command code	Action
-	1101	reserved for future use
MFAuthent	1110	performs the MIFARE standard authentication as a reader
SoftReset	1111	resets the MFRC523

10.3.1 MFRC523 command descriptions

10.3.1.1 Idle mode

Places the MFRC523 in Idle mode. The Idle command also terminates itself.

10.3.1.2 Mem command

Transfers 25 bytes from the FIFO buffer to the internal buffer. To read out the 25 bytes from the internal buffer the Mem command must be started with an empty FIFO buffer. In this case, the 25 bytes are transferred from the internal buffer to the FIFO.

During a hard power-down (using pin NRSTPD), the 25 bytes in the internal buffer remain unchanged and are only lost if the power supply is removed from the MFRC523.

This command automatically terminates when finished and the Idle command becomes active.

10.3.1.3 Generate RandomID

This command generates a 10-byte random number which is initially stored in the internal buffer. This then overwrites the 10 bytes in the internal 25-byte buffer. This command automatically terminates when finished and the MFRC523 returns to Idle mode.

10.3.1.4 CalcCRC command

The FIFO buffer content is transferred to the CRC coprocessor and the CRC calculation is started. The calculation result is stored in the CRCResultReg register. The CRC calculation is not limited to a dedicated number of bytes. The calculation is not stopped when the FIFO buffer is empty during the data stream. The next byte written to the FIFO buffer is added to the calculation.

The CRC preset value is controlled by the ModeReg register's CRCPreset[1:0] bits. The value is loaded in to the CRC coprocessor when the command starts. This command must be terminated by writing a command to the CommandReg register, such as, the Idle command.

If the AutoTestReg register's SelfTest[3:0] bits are set correctly, the MFRC523 enters Self-test mode. Starting the CalcCRC command initiates a digital self-test. The result of the self-test is written to the FIFO buffer.

10.3.1.5 Transmit command

The FIFO buffer content is immediately transmitted after starting this command. Before transmitting the FIFO buffer content, all relevant registers must be set for data transmission.

This command automatically terminates when the FIFO buffer is empty. It can be terminated by another command written to the CommandReg register.

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10.3.1.6 NoCmdChange command

This command does not influence any running command in the CommandReg register. It can be used to manipulate any bit except the CommandReg register Command[3:0] bits, for example, the RcvOff bit or the PowerDown bit.

10.3.1.7 Receive command

The MFRC523 activates the receiver path and waits for a data stream to be received. The correct settings must be chosen before starting this command.

This command automatically terminates when the data stream ends. This is indicated either by the end of frame pattern or by the length byte depending on the selected frame type and speed.

Remark: If the RxModeReg register's RxMultiple bit is set to logic 1, the Receive command does not automatically terminate. It must be terminated by starting another command in the CommandReg register.

10.3.1.8 Transceive command

This command continuously repeats the transmission of data from the FIFO buffer and the reception of data from the RF field. The first action is transmit and after transmission the command is changed to receive a data stream.

Each transmit process must be started by setting the BitFramingReg register's StartSend bit to logic 1. This command must be cleared by writing any command to the CommandReg register.

Remark: If the RxModeReg register's RxMultiple bit is set to logic 1, the Transceive command never leaves the receive state because this state cannot be cancelled automatically.

10.3.1.9 MFAuthent command

This command manages MIFARE authentication to enable a secure communication to any MIFARE card. The following data is written to the FIFO buffer before the command can be activated:

- Authentication command code (60h, 61h)
- Block address
- Sector key byte 0
- Sector key byte 1
- Sector key byte 2
- Sector key byte 3
- Sector key byte 4
- Sector key byte 5
- Card serial number byte 0
- Card serial number byte 1
- Card serial number byte 2
- Card serial number byte 3

12 bytes in total are written to the FIFO.

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Remark: When the MFAuthent command is active all access to the FIFO buffer is blocked. However, if there is access to the FIFO buffer, the ErrorReg register's WrErr bit is set.

This command automatically terminates when the MIFARE card is authenticated and the Status2Reg register's MFCrypto1On bit is set to logic 1.

This command does not terminate automatically if the card does not answer, so the timer must be initialized to automatic mode. In this case, in addition to the IdleIRq bit, the TimerIRq bit can be used as the termination criteria. During authentication processing, the RxIRq bit and TxIRq bit are blocked. The Crypto1On bit is only valid after termination of the MFAuthent command, either after processing the protocol or writing Idle to the CommandReg register.

If an error occurs during authentication, the ErrorReg register's ProtocolErr bit is set to logic 1 and the Status2Reg register's Crypto1On bit is set to logic 0.

10.3.1.10 SoftReset command

This command performs a reset of the device. The configuration data of the internal buffer remains unchanged. All registers are set to the reset values. This command automatically terminates when finished.

Remark: The SerialSpeedReg register is reset and therefore the serial data rate is set to 9.6 kBd.

11. Errata sheet

This chapter lists all differences from version 1.0 to version 2.0:

The value of the version in Section 9.2.4.8 on page 65 is set to B1h.

The answer to the Selftest (see Section 17.1 on page 82) for version 1.0 (VersionReg equal to B1h):

00h, C6h, 37h, D5h, 32h, B7h, 57h, 5Ch
C2h, D8h, 7Ch, 4Dh, D9h, 70h, C7h, 73h
10h, E6h, D2h, AAh, 5Eh, A1h, 3Eh, 5Ah
14h, AFh, 30h, 61h, C9h, 70h, DBh, 2Eh
64h, 22h, 72h, B5h, BDh, 65h, F4h, ECh
22h, BCh, D3h, 72h, 35h, CDh, AAh, 41h
1Fh, A7h, F3h, 53h, 14h, DEh, 7Eh, 02h
D9h, 0Fh, B5h, 5Eh, 25h, 1Dh, 29h, 79h

Only the default setting for the prescaler (see Section 8.7 "Timer unit" on page 29): t = ((TPreScaler*2+1)*TReload+1)/13,56 MHz is supported. As such only the formula f_{Timer} = 13,56 MHz/(2*PreScaler+1) is applicable for the TPrescalerHigh in Table 108 "TPrescalerReg register (address 2Bh); reset value: 00h bit allocation" on page 60 and TPrescalerLo in Table 109 "TPrescalerReg register bit descriptions" on page 61. As there is no option for the prescaler, also the TPrescalEven (see Table 73 "DemodReg register bit descriptions") shall be set to 0, see also Section 9.2.3.10 "TModeReg and TPrescalerReg registers" on page 59.

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Especially when using time slot protocols, it is needed that the error flag is copied into the status information of the frame. When using the RxMultiple feature (see Section 9.2.2.4 on page 48) within version 1.0 the protocol error flag is not included in the status information for the frame. In addition the CRCOk is copied instead of the CRCErr. This can be a problem in frames without length information e.g. ISO/IEC 14443-B.

The version 1.0 does not accept a Type B EOF if there is no 1 bit after the series of 0 bits, as such the configuration within Section 9.2.2.15 “TypeBReg register” on page 54 bit 4 for RxEOFReq does not exist. In addition the IC only has the possibility to select the minimum or maximum timings for SOF/EOF generation defined in ISO/IEC14443B. As such the configuration possible in version 2.0 through the EOFSOFAdjust bit (see Section 9.2.4.7 “AutoTestReg register” on page 64) does not exist and the configuration is limited to only setting minimum and maximum length according ISO/IEC 14443-B, see Section 9.2.2.15 “TypeBReg register” on page 54, bit 4.

The available NXP NFC library is only tested with version 2.0.

12. Limiting values

Table 151. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DDA}	analog supply voltage		–0.5	+4.0	V
V_{DDD}	digital supply voltage		–0.5	+4.0	V
$V_{DD(PVDD)}$	PVDD supply voltage		–0.5	+4.0	V
$V_{DD(TVDD)}$	TVDD supply voltage		–0.5	+4.0	V
$V_{DD(SVDD)}$	SVDD supply voltage		–0.5	+4.0	V
V_I	input voltage	all input pins except pins MFIN and RX	$V_{SS(PVSS)}$ − 0.5	$V_{DD(PVDD)}$ + 0.5	V
		pin MFIN	$V_{SS(PVSS)}$ − 0.5	$V_{DD(SVDD)}$ + 0.5	V
P_{tot}	total power dissipation	per package; V_{DDD} in shortcut mode	-	200	mW
T_j	junction temperature		-	100	°C
V_{ESD}	electrostatic discharge voltage	HBM; 1500 Ω, 100 pF; JESD22-A114-B	-	2000	V
		MM; 0.75 μH, 200 pF; JESD22-A114-A	-	200	V
		Charged device model; JESD22-C101-A			
		on all pins	-	200	V
		on all pins except SVDD in TFBGA64 package	-	500	V

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13. Recommended operating conditions

Table 152. Operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	analog supply voltage	$V_{DD(PVDD)} \leq V_{DDA} = V_{DDD} = V_{DD(TVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V	[1][2]	2.5	3.3	3.6	V
V_{DDD}	digital supply voltage	$V_{DD(PVDD)} \leq V_{DDA} = V_{DDD} = V_{DD(TVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V	[1][2]	2.5	3.3	3.6	V
$V_{DD(TVDD)}$	TVDD supply voltage	$V_{DD(PVDD)} \leq V_{DDA} = V_{DDD} = V_{DD(TVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V	[1][2]	2.5	3.3	3.6	V
$V_{DD(PVDD)}$	PVDD supply voltage	$V_{DD(PVDD)} \leq V_{DDA} = V_{DDD} = V_{DD(TVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V	[3]	1.6	1.8	3.6	V
$V_{DD(SVDD)}$	SVDD supply voltage	$V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V		1.6	-	3.6	V
T_{amb}	ambient temperature	HVQFN32		–25	-	+85	°C

[1] Supply voltages below 3 V reduce the performance in, for example, the achievable operating distance.

[2] V_{DDA}, V_{DDD} and $V_{DD(TVDD)}$ must always be the same voltage.

[3] $V_{DD(PVDD)}$ must always be the same or lower voltage than V_{DDD}.

14. Thermal characteristics

Table 153. Thermal characteristics

Symbol	Parameter	Conditions		Package	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in still air with exposed pin soldered on a 4 layer JEDEC PCB		HVQFN32	40	K/W

15. Characteristics

Table 154. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Input characteristics							
Pins EA, I2C and NRSTPD							
I_{LI}	input leakage current			–1	-	+1	µA
V_{IH}	HIGH-level input voltage			$0.7V_{DD(PVDD)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(PVDD)}$	V
Pin MFIN							
I_{LI}	input leakage current			–1	-	+1	µA
V_{IH}	HIGH-level input voltage			$0.7V_{DD(SVDD)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(SVDD)}$	V

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Table 154. Characteristics *…continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Pin SDA							
I_{LI}	input leakage current			–1	-	+1	µA
V_{IH}	HIGH-level input voltage			$0.7V_{DD(PVDD)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(PVDD)}$	V
Pin RX[1]							
V_i	input voltage			–1	-	V_{DDA} +1	V
C_i	input capacitance	V_{DDA} = 3 V; receiver active; $V_{RX(p-p)}$ = 1 V; 1.5 V (DC) offset		-	10	-	pF
R_i	input resistance	V_{DDA} = 3 V; receiver active; $V_{RX(p-p)}$ = 1 V; 1.5 V (DC) offset		-	350	-	Ω
Input voltage range; see Figure 24							
$V_{i(p-p)(min)}$	minimum peak-to-peak input voltage	Manchester encoded; V_{DDA} = 3 V		-	100	-	mV
$V_{i(p-p)(max)}$	maximum peak-to-peak input voltage	Manchester encoded; V_{DDA} = 3 V		-	4	-	V
Input sensitivity; see Figure 24							
V_{mod}	modulation voltage	minimum Manchester encoded; V_{DDA} = 3 V; RxGain[2:0] = 111b (48 dB)		-	5	-	mV
Pin OSCIN							
I_{LI}	input leakage current			–1	-	+1	µA
V_{IH}	HIGH-level input voltage			$0.7V_{DDA}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DDA}$	V
C_i	input capacitance	V_{DDA} = 2.8 V; DC = 0.65 V; AC = 1 V (p-p)		-	2	-	pF
Input/output characteristics							
pins D1, D2, D3, D4, D5, D6 and D7							
I_{LI}	input leakage current			–1	-	+1	µA
V_{IH}	HIGH-level input voltage			$0.7V_{DD(PVDD)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD(PVDD)}$	V
V_{OH}	HIGH-level output voltage	$V_{DD(PVDD)}$ = 3 V; I_O = 4 mA		$V_{DD(PVDD)}$ – 0.4	-	$V_{DD(PVDD)}$	V
V_{OL}	LOW-level output voltage	$V_{DD(PVDD)}$ = 3 V; I_O = 4 mA		$V_{SS(PVSS)}$	-	$V_{SS(PVSS)}$ + 0.4	V

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Table 154. Characteristics *…continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{OH}	HIGH-level output current	$V_{DD(PVDD)}$ = 3 V		-	-	4	mA
I_{OL}	LOW-level output current	$V_{DD(PVDD)}$ = 3 V		-	-	4	mA
Output characteristics							
Pin MFOUT							
V_{OH}	HIGH-level output voltage	$V_{DD(SVDD)}$ = 3 V; I_O = 4 mA		$V_{DD(SVDD)}$ − 0.4	-	$V_{DD(SVDD)}$	V
V_{OL}	LOW-level output voltage	$V_{DD(SVDD)}$ = 3 V; I_O = 4 mA		$V_{SS(PVSS)}$	-	$V_{SS(PVSS)}$ + 0.4	V
I_{OL}	LOW-level output current	$V_{DD(SVDD)}$ = 3 V		-	-	4	mA
I_{OH}	HIGH-level output current	$V_{DD(SVDD)}$ = 3 V		-	-	4	mA
Pin IRQ							
V_{OH}	HIGH-level output voltage	$V_{DD(PVDD)}$ = 3 V; I_O = 4 mA		$V_{DD(PVDD)}$ − 0.4	-	$V_{DD(PVDD)}$	V
V_{OL}	LOW-level output voltage	$V_{DD(PVDD)}$ = 3 V; I_O = 4 mA		$V_{SS(PVSS)}$	-	$V_{SS(PVSS)}$ + 0.4	V
I_{OL}	LOW-level output current	$V_{DD(PVDD)}$ = 3 V		-	-	4	mA
I_{OH}	HIGH-level output current	$V_{DD(PVDD)}$ = 3 V		-	-	4	mA
Pins AUX1 and AUX2							
V_{OH}	HIGH-level output voltage	V_{DDD} = 3 V; I_O = 4 mA		V_{DDD} − 0.4	-	V_{DDD}	V
V_{OL}	LOW-level output voltage	V_{DDD} = 3 V; I_O = 4 mA		$V_{SS(PVSS)}$	-	$V_{SS(PVSS)}$ + 0.4	V
I_{OL}	LOW-level output current	V_{DDD} = 3 V		-	-	4	mA
I_{OH}	HIGH-level output current	V_{DDD} = 3 V		-	-	4	mA
Pins TX1 and TX2							
V_{OH}	HIGH-level output voltage	$V_{DD(TVDD)}$ = 3 V; $I_{DD(TVDD)}$ = 32 mA; CWGsP[5:0] = 3Fh		$V_{DD(TVDD)}$ − 0.15	-	-	V
		$V_{DD(TVDD)}$ = 3 V; $I_{DD(TVDD)}$ = 80 mA; CWGsP[5:0] = 3Fh		$V_{DD(TVDD)}$ − 0.4	-	-	V
		$V_{DD(TVDD)}$ = 2.5 V; $I_{DD(TVDD)}$ = 32 mA; CWGsP[5:0] = 3Fh		$V_{DD(TVDD)}$ − 0.24	-	-	V
		$V_{DD(TVDD)}$ = 2.5 V; $I_{DD(TVDD)}$ = 80 mA; CWGsP[5:0] = 3Fh		$V_{DD(TVDD)}$ − 0.64	-	-	V

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Table 154. Characteristics *…continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage	$V_{DD(TVDD)}$ = 3 V; $I_{DD(TVDD)}$ = 32 mA; CWGsP[5:0] = 0Fh		-	-	0.15	V
		$V_{DD(TVDD)}$ = 3 V; $I_{DD(TVDD)}$ = 80 mA; CWGsP[5:0] = 0Fh		-	-	0.4	V
		$V_{DD(TVDD)}$ = 2.5 V; $I_{DD(TVDD)}$ = 32 mA; CWGsP[5:0] = 0Fh		-	-	0.24	V
		$V_{DD(TVDD)}$ = 2.5 V; $I_{DD(TVDD)}$ = 80 mA; CWGsP[5:0] = 0Fh		-	-	0.64	V
Current consumption							
I_{pd}	power-down current	V_{DDA} = V_{DDD} = $V_{DD(TVDD)}$ = $V_{DD(PVDD)}$ = 3 V					
		hard power-down; pin NRSTPD set LOW	[2]	-	-	5	µA
		soft power-down; RF level detector on	[2]	-	-	10	µA
I_{DDD}	digital supply current	pin DVDD; V_{DDD} = 3 V		-	6.5	9	mA
I_{DDA}	analog supply current	pin AVDD; V_{DDA} = 3 V; CommandReg register's bit RcvOff = 0		-	7	10	mA
		pin AVDD; receiver switched off; V_{DDA} = 3 V; CommandReg register's bit RcvOff = 1		-	3	5	mA
$I_{DD(PVDD)}$	PVDD supply current	pin PVDD	[3]	-	-	40	mA
$I_{DD(TVDD)}$	TVDD supply current	pin TVDD; continuous wave	[4][5][6]	-	60	100	mA
$I_{DD(SVDD)}$	SVDD supply current	pin SVDD	[7]	-	-	4	mA
Clock frequency							
f_{clk}	clock frequency			-	27.12	-	MHz
δ_{clk}	clock duty cycle			40	50	60	%
t_{jit}	jitter time	RMS		-	-	10	ps
Crystal oscillator							
V_{OH}	HIGH-level output voltage	pin OSCOUT		-	1.1	-	V
V_{OL}	LOW-level output voltage	pin OSCOUT		-	0.2	-	V
C_i	input capacitance	pin OSCOUT		-	2	-	pF
		pin OSCIN		-	2	-	pF

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Table 154. Characteristics *...continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Typical input requirements							
f_{xtal}	crystal frequency			-	27.12	-	MHz
ESR	equivalent series resistance			-	-	100	Ω
C_L	load capacitance			-	10	-	pF
P_{xtal}	crystal power dissipation			-	50	100	μW

[1] The voltage on pin RX is clamped by internal diodes to pins AVSS and AVDD.

[2] I_{pd} is the total current for all supplies.

[3] $I_{DD(PVDD)}$ depends on the overall load at the digital pins.

[4] $I_{DD(TVDD)}$ depends on $V_{DD(TVDD)}$ and the external circuit connected to pins TX1 and TX2.

[5] During typical circuit operation, the overall current is below 100 mA.

[6] Typical value using a complementary driver configuration and an antenna matched to 40 Ω between pins TX1 and TX2 at 13.56 MHz.

[7] $I_{DD(SVDD)}$ depends on the load at pin MFOUT.

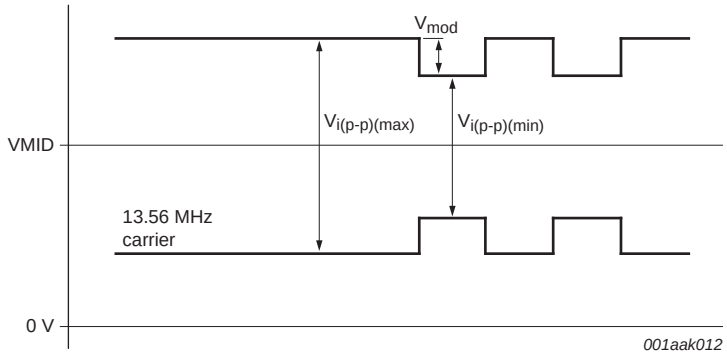

Fig 24. Pin RX input voltage range

15.1 Timing characteristics

Table 155. SPI timing characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{WL}	pulse width LOW	line SCK		50	-	-	ns
t_{WH}	pulse width HIGH	line SCK		50	-	-	ns
$t_{h(SCKH-D)}$	SCK HIGH to data input hold time	SCK to changing MOSI		25	-	-	ns
$t_{su(D-SCKH)}$	data input to SCK HIGH set-up time	changing MOSI to SCK		25	-	-	ns

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Table 155. SPI timing characteristics *...continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{h(SCKL-Q)}$	SCK LOW to data output hold time	SCK to changing MISO		-	-	25	ns
$t_{(SCKL-NSSH)}$	SCK LOW to NSS HIGH time			0	-	-	ns
t_{NSSH}	NSS HIGH time	before communication		50	-	-	ns

Table 156. I^2C-bus timing in Fast mode

Symbol	Parameter	Conditions	Fast mode		High-speed mode		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	400	0	3400	kHz
$t_{HD;STA}$	hold time (repeated) START condition	after this period, the first clock pulse is generated	600	-	160	-	ns
$t_{SU;STA}$	set-up time for a repeated START condition		600	-	160	-	ns
$t_{SU;STO}$	set-up time for STOP condition		600	-	160	-	ns
t_{LOW}	LOW period of the SCL clock		1300	-	160	-	ns
t_{HIGH}	HIGH period of the SCL clock		600	-	60	-	ns
$t_{HD;DAT}$	data hold time		0	900	0	70	ns
$t_{SU;DAT}$	data set-up time		100	-	10	-	ns
t_r	rise time	SCL signal	20	300	10	40	ns
t_f	fall time	SCL signal	20	300	10	40	ns
t_r	rise time	SDA and SCL signals	20	300	10	80	ns
t_f	fall time	SDA and SCL signals	20	300	10	80	ns
t_{BUF}	bus free time between a STOP and START condition		1.3	-	1.3	-	µs

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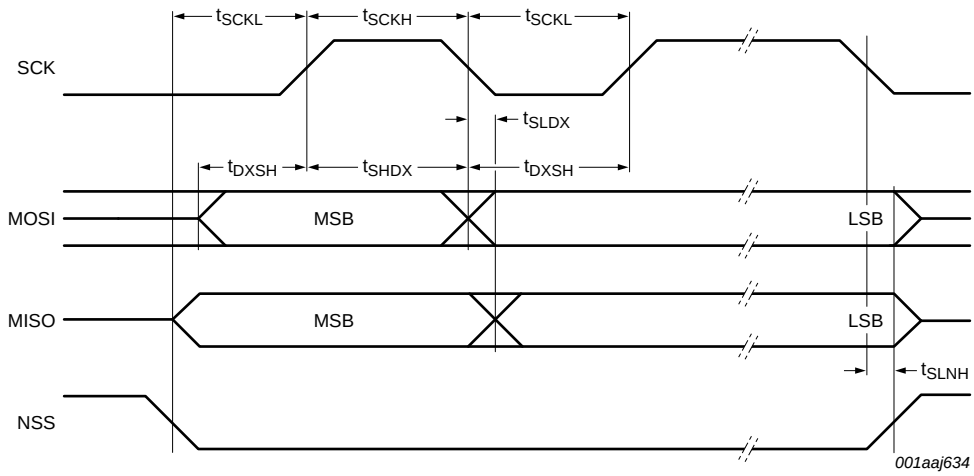

Remark: The signal NSS must be LOW to be able to send several bytes in one data stream. To send more than one data stream NSS must be set HIGH between the data streams.

Fig 25. Timing diagram for SPI

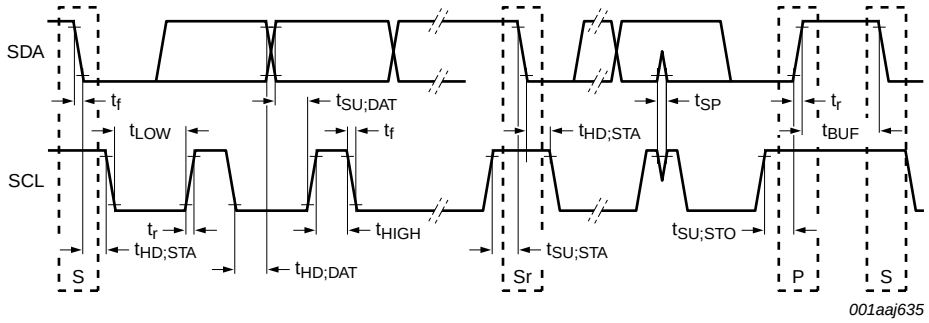

Fig 26. Timing for Fast and Standard mode devices on the I^2C-bus

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16. Application information

A typical application diagram using a complementary antenna connection to the MFRC523 is shown in Figure 27.

The antenna tuning and RF part matching is described in the application note Ref. 1 and Ref. 2.

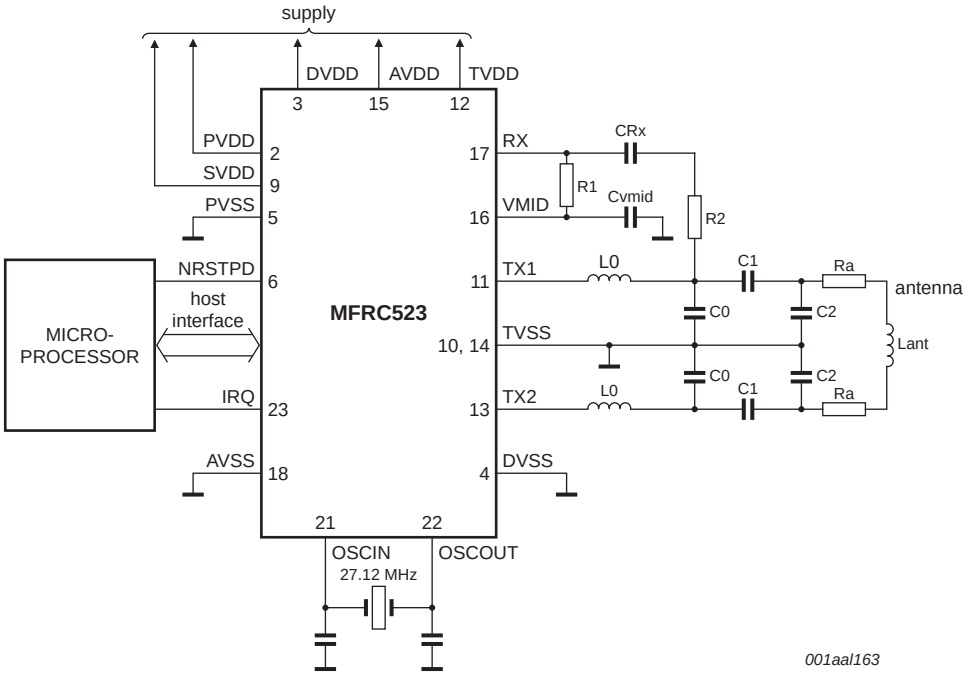

Fig 27. Typical application diagram

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17. Test information

17.1 Test signals

17.1.1 Self-test

The MFRC523 has the capability to perform a digital self-test. The self-test is started by using the following procedure:

1. Perform a soft reset.
2. Clear the internal buffer by writing 25 bytes of 00h and implement the Config command.
3. Enable the self-test by writing 09h to the AutoTestReg register.
4. Write 00h to the FIFO buffer.
5. Start the self-test with the CalcCRC command.
6. The self-test is initiated.
7. When the self-test has completed, the FIFO buffer contains the following 64 bytes:

FIFO buffer byte values for version B2h:

```
00h, EBh, 66h, BAh, 57h, BFh, 23h, 95h, D0h, E3h, 0Dh, 3Dh, 27h, 89h, 5Ch, DEh, 9Dh,
     3Bh, A7h, 00h, 21h, 5Bh, 89h, 82h, 51h, 3Ah, EBh, 02h, 0Ch, A5h, 00h, 49h, 7Ch,
     84h, 4Dh, B3h, CCh, D2h, 1Bh, 81h, 5Dh, 48h, 76h, D5h, 71h, 61h, 21h, A9h, 86h,
     96h, 83h, 38h, CFh, 9Dh, 5Bh, 6Dh, DCh, 15h, BAh, 3Eh, 7Dh, 95h, 3Bh, 2Fh
```

The FIFO buffer byte values for version B1h are available at Section 11.

17.1.2 Test bus

The test bus is used for production tests. The following configuration can be used to improve the design of a system using the MFRC523. The test bus allows internal signals to be routed to the digital interface. The test bus comprises two sets of test signals which are selected using their subaddress specified in the TestSel2Reg register's TestBusSel[4:0] bits. The test signals and their related digital output pins are described in Table 157 and Table 158.

Table 157. Test bus signals: TestBusSel[4:0] = 07h

Pins	Internal signal name	Description
D6	s_data	received data stream
D5	s_coll	bit-collision detected (106 kBd only)
D4	s_valid	s_data and s_coll signals are valid
D3	s_over	receiver has detected a stop condition
D2	RCV_reset	receiver is reset
D1	-	reserved

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Table 158. Test bus signals: TestBusSel[4:0] = 0Dh

Pins	Internal test signal name	Description
D6	clkstable	oscillator output signal
D5	clk27/8	oscillator output signal divided by 8
D4 to D3	-	reserved
D2	clk27	oscillator output signal
D1	-	reserved

17.1.3 Test signals on pins AUX1 or AUX2

The MFRC523 allows the user to select internal signals for measurement on pins AUX1 or AUX2. These measurements can be helpful during the design-in phase to optimize the design or used for test purposes.

Table 159 shows the signals that can be switched to pin AUX1 or AUX2 by setting AnalogSelAux1[3:0] or AnalogSelAux2[3:0] in the AnalogTestReg register.

Remark: The DAC has a current output, therefore it is recommended that a 1 kΩ pull-down resistor is connected to pin AUX1 or pin AUX2.

Table 159. Test signal descriptions

AnalogSelAuxn[3:0]	Signal on pin AUXn
0000	3-state
0001	DAC: register TestDAC1 or TestDAC2
0010	DAC: test signal Corr1
0011	reserved
0100	DAC: test signal MinLevel
0101	DAC: test signal ADC_I
0110	DAC: test signal ADC_Q
0111 to 1001	reserved
1010	HIGH
1011	LOW
1100	TxActive
1101	RxActive
1110	subcarrier detected
1111	TstBusBit

17.1.3.1 Example: Output test signals TestDAC1 and TestDAC2

The AnalogTestReg register is set to 11h. The output on pin AUX1 has the test signal TestDAC1 and the output on pin AUX2 has the test signal TestDAC2. The signal values of TestDAC1 and TestDAC2 are controlled by the TestDAC1Reg and TestDAC2Reg registers.

Figure 28 shows test signal TestDAC1 on pin AUX1 and TestDAC2 on pin AUX2 when the TestDAC1Reg register is programmed with a slope defined by values 00h to 3Fh and the TestDAC2Reg register is programmed with a rectangular signal defined by values 00h and 3Fh.

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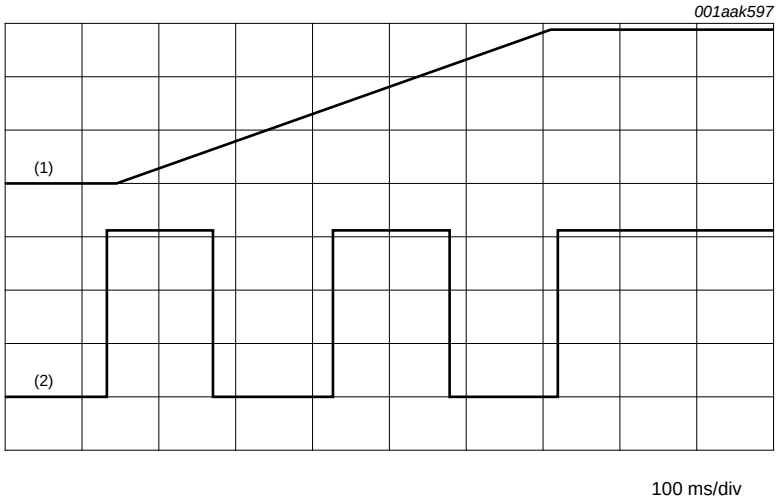
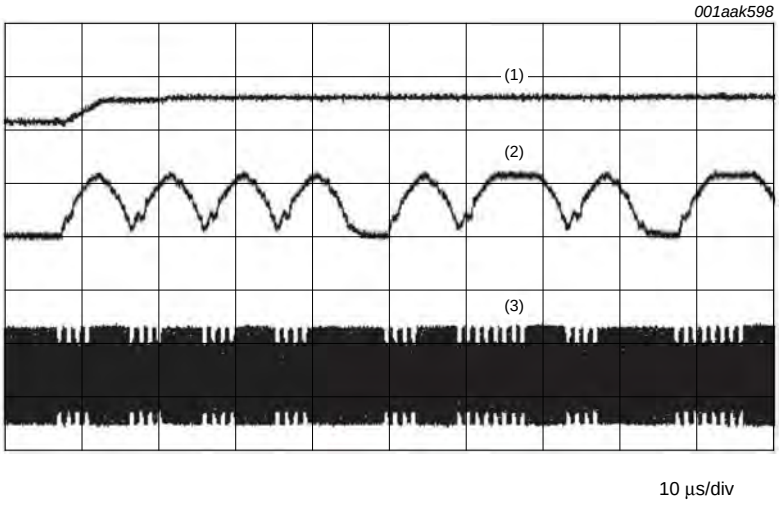


(1) TestDAC1 (500 mV/div) on pin AUX1.
(2) TestDAC2 (500 mV/div) on pin AUX2.

Fig 28. Output test signals TestDAC1 on pin AUX1 and TestDAC2 on pin AUX2

17.1.3.2 Example: Output test signals Corr1 and MinLevel

Figure 29 shows test signals Corr1 and MinLevel on pins AUX1 and AUX2, respectively. The AnalogTestReg register is set to 24h.



(1) MinLevel (1 V/div) on pin AUX2.
(2) Corr1 (1 V/div) on pin AUX1.
(3) RF field.

Fig 29. Output test signals Corr1 on pin AUX1 and MinLevel on pin AUX2

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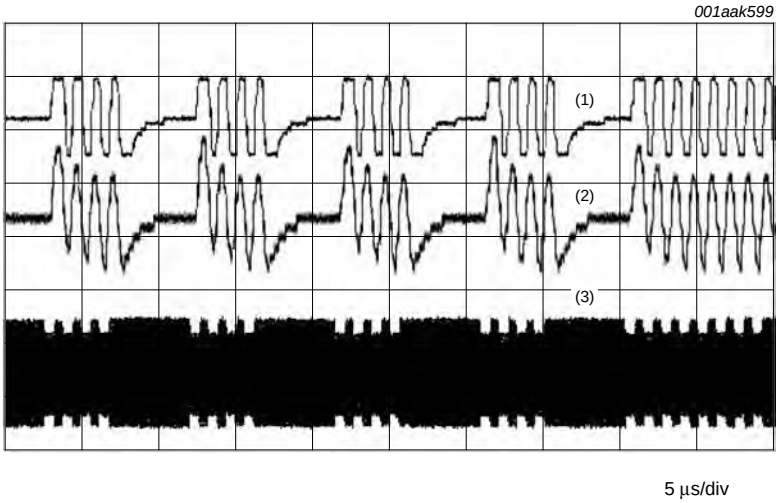
17.1.3.3 Example: Output test signals ADC I-channel and ADC Q-channel

Figure 30 shows the channel behavior test signals ADC_I and ADC_Q on pins AUX1 and AUX2, respectively. The AnalogTestReg register is set to 56h.



(1) ADC_I (1 V/div) on pin AUX1.
(2) ADC_Q (500 mV/div) on pin AUX2.
(3) RF field.

Fig 30. Output ADC I-channel on pin AUX1 and ADC Q-channel on pin AUX2

17.1.3.4 Example: Output test signals RxActive and TxActive

Figure 31 shows the RxActive and TxActive test signals relating to RF communication. The AnalogTestReg register is set to CDh.

- At 106 kBd, RxActive is HIGH during data bits, parity and CRC reception. Start bits are not included
- At 106 kBd, TxActive is HIGH during start bits, data bits, parity and CRC transmission
- At 212 kBd, 424 kBd and 848 kBd, RxActive is HIGH during data bits and CRC reception. Start bits are not included
- At 212 kBd, 424 kBd and 848 kBd, TxActive is HIGH during data bits and CRC transmission

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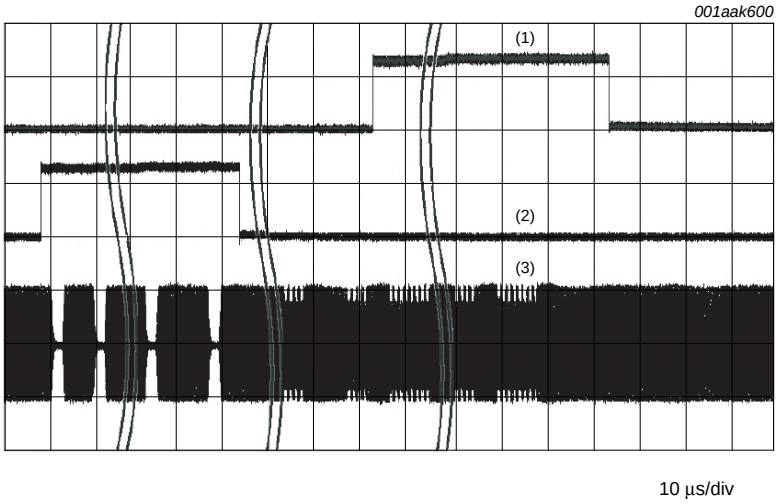
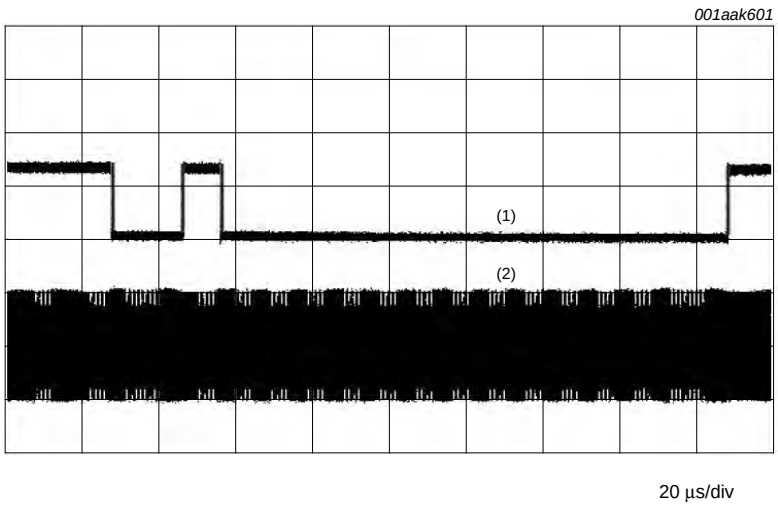


(1) RxActive (2 V/div) on pin AUX1.
(2) TxActive (2 V/div) on pin AUX2.
(3) RF field.

Fig 31. Output RxActive on pin AUX1 and TxActive on pin AUX2

17.1.3.5 Example: Output test signal RX data stream

Figure 32 shows the data stream that is currently being received. The TestSel2Reg register's TestBusSel[4:0] bits are set to 07h to enable test bus signals on pins D1 to D6; see Section 17.1.2 "Test bus" on page 82. The TestSel1Reg register's TstBusBitSel[2:0] bits are set 06h (pin D6 = s_data) and AnalogTestReg register is set to FFh (TstBusBit) which outputs the received data stream on pins AUX1 and AUX2.



(1) s_data (received data stream) (2 V/div).
(2) RF field.

Fig 32. Received data stream on pins AUX1 and AUX2

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17.1.3.6 Pseudo-Random Binary Sequences (PRBS)

The pseudo-random binary sequences PRBS9 and PRBS15 are based on ITU-TO150 and are defined with the TestSel2Reg register. Transmission of either data stream is started by the Transmit command. The preamble/sync byte/start bit/parity bit are automatically generated depending on the mode selected.

Remark: All relevant registers for transmitting data must be configured in accordance with ITU-TO150 before selecting PRBS transmission.

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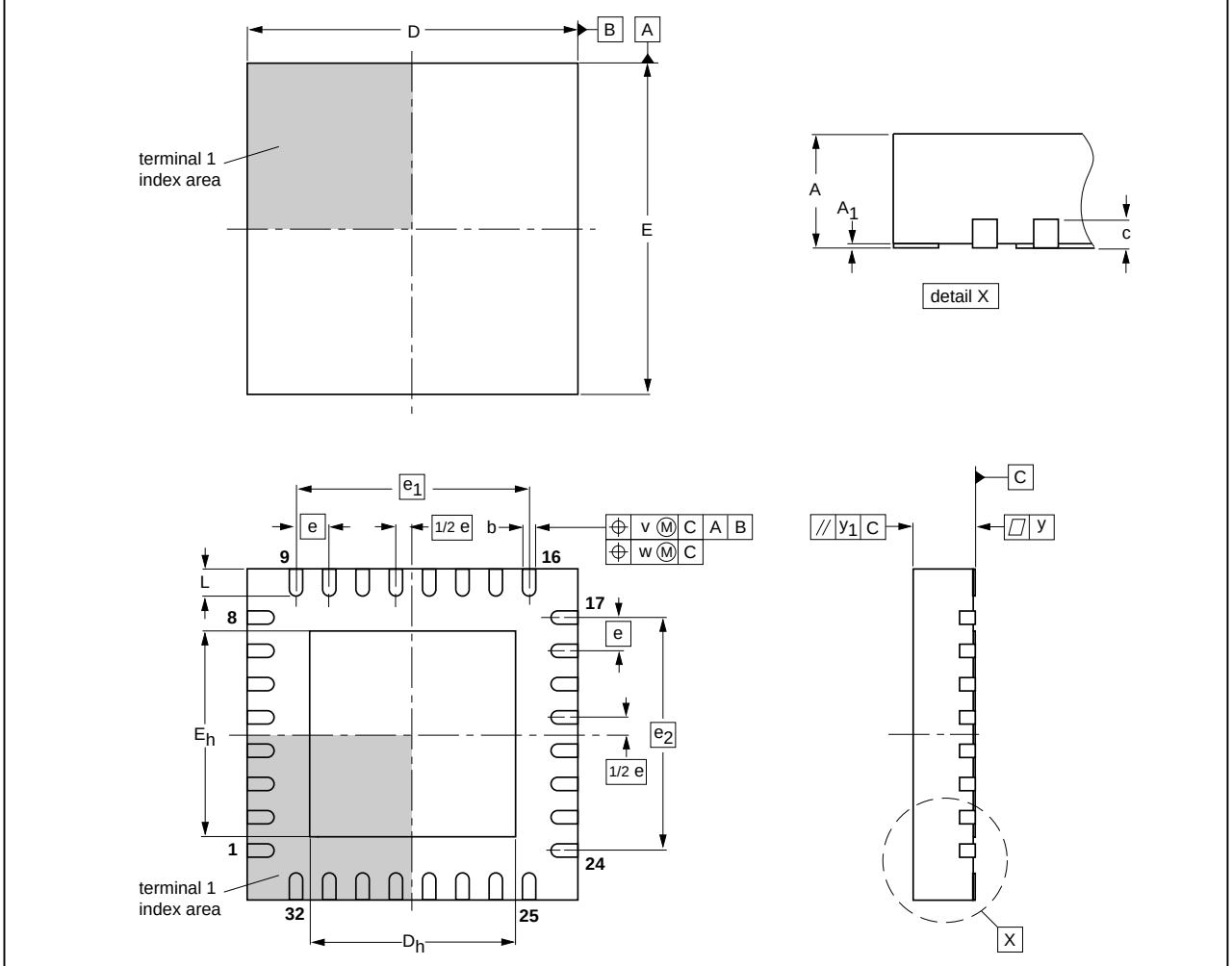
18. Package outline

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm **SOT617-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.1 4.9	3.25 2.95	5.1 4.9	3.25 2.95	0.5	3.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT617-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-18

Fig 33. Package outline SOT617-1 (HVQFN32)

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Detailed package information can be found at: www.nxp.com/package/SOT617-1.html

19. Handling information

Moisture Sensitivity Level (MSL) evaluation has been performed according to *SNW-FQ-225B rev.04/07/07 (JEDEC J-STD-020C)*. MSL for this package is level 1 which means 260 °C convection reflow temperature.

Dry pack is not required.

Unlimited out-of-pack floor life at maximum ambient 30 °C/85 % RH.

20. Packing information

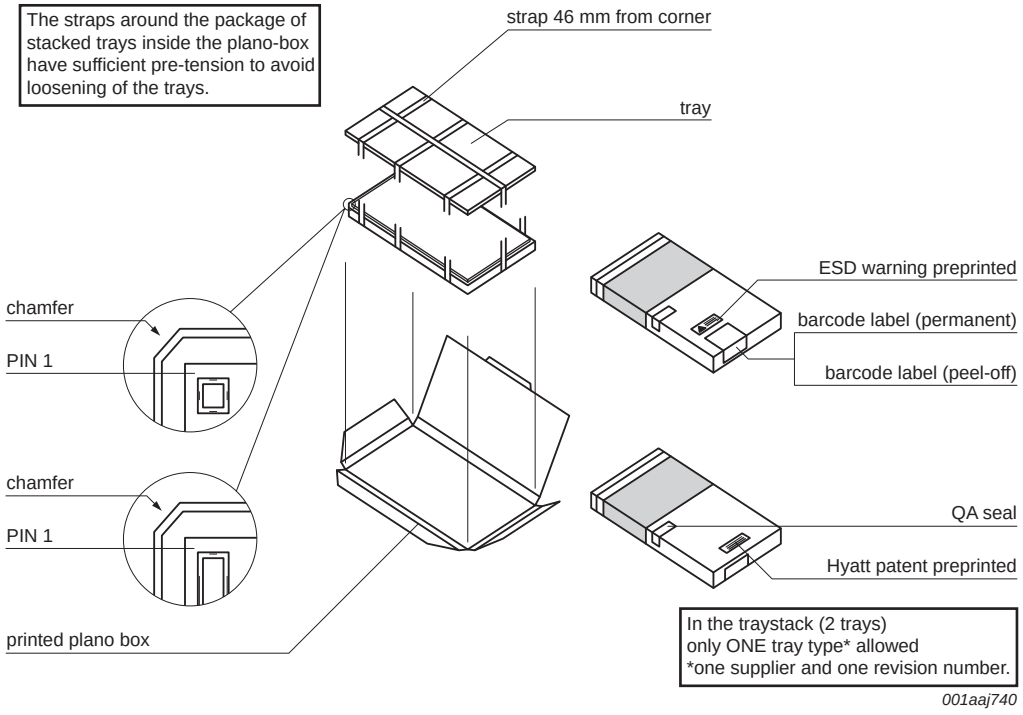

Fig 34. Packing information 1 tray

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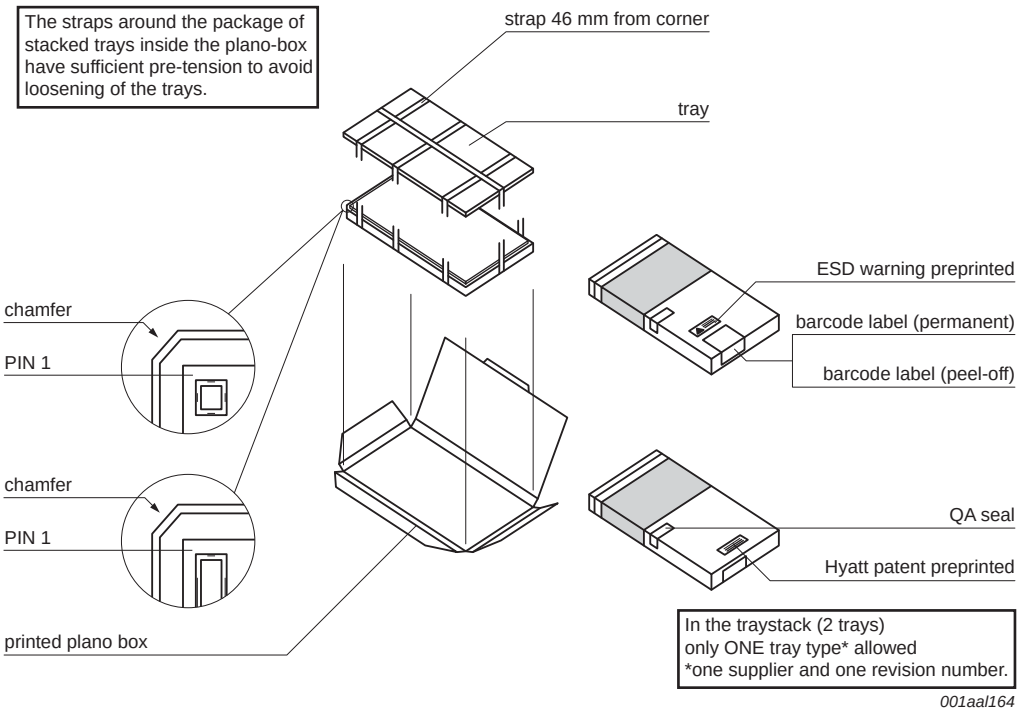

Fig 35. Packing information 5 trays

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21. Abbreviations

Table 160. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
ASK	Amplitude Shift Keying
BPSK	Binary Phase Shift Keying
CRC	Cyclic Redundancy Check
CW	Continuous Wave
DAC	Digital-to-Analog Converter
EOF	End Of Frame
ETU	Elementary Time Unit
HBM	Human Body Model
I^2C	Inter-integrated Circuit
LSB	Least Significant Bit
MISO	Master In Slave Out
MM	Machine Model
MOSI	Master Out Slave In
MSB	Most Significant Bit
NRZ	Not Return to Zero
NSS	Not Slave Select
PCB	Printed-Circuit Board
PLL	Phase-Locked Loop
PRBS	Pseudo-Random Bit Sequence
RX	Receiver
SOF	Start Of Frame
SPI	Serial Peripheral Interface
TX	Transmitter
UART	Universal Asynchronous Receiver Transmitter

22. Glossary

Modulation index — Defined as the voltage ratio $(V_{max} - V_{min}) / (V_{max} + V_{min})$.

Load modulation index — Defined as the voltage ratio for the card $(V_{max} - V_{min}) / (V_{max} + V_{min})$ measured at the card's coil.

23. References

[1] **Application note —** *MFRC52x Reader IC Family Directly Matched Antenna Design*

[2] **Application note —** *MIFARE (ISO/IEC 14443 A) 13.56 MHz RFID Proximity Antennas*

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24. Revision history

Table 161. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
MFRC523 v. 4.2	20160427	Product data sheet	-	MFRC523 v. 4.1
Modifications:	• Descriptive title updated			
MFRC523 v. 4.1	20150506	Product data sheet	-	MFRC523 v. 4.0
Modifications:	• Figure 27 “Typical application diagram”: SVDD symbol corrected			
MFRC523 v. 4.0	20141202	Product data sheet	-	MFRC523 v. 3.9
Modifications:	• Section 8.2 “ISO/IEC 14443 B functionality”: Remark removed			
MFRC523 v. 3.9	20140917	Product data sheet	-	MFRC523 v. 3.8
Modifications:	• Table 151 “Limiting values”: updated			
MFRC523 v. 3.8	20140312	Product data sheet	-	MFRC523 v. 3.7
Modifications:	• Section 2 “General description”: updated • Section 11 “Errata sheet”: section added • Descriptive title changed			
MFRC523 v. 3.7	20111108	Product data sheet	-	MFRC523 v. 3.6
Modifications:	• Table 2 “Ordering information”: updated • Table 154 “Characteristics”: unit of P_{xtal} corrected			
MFRC523 v. 3.6	20110628	Product data sheet	-	MFRC523_35
Modifications:	• Section 9.2.1.7 “ErrorReg register” on page 40 added			
MFRC523_35	20100924	Product data sheet	-	MFRC523_34
Modifications:	• Table 131 “VersionReg register bit descripitons” on page 63 changed			
MFRC523_34	20100715	Product data sheet	-	MFRC523_33
Modifications:	• Section 9.2.2.10 “DemodReg register”: register updated. • Section 9.2.2.15 “TypeBReg register”: register updated. • Section 9.2.3.10 “TModeReg and TPrescalerReg registers”: register updated. • Section 9.2.4.7 “AutoTestReg register”: register updated. • Section 8.7 “Timer unit”: timer calculation updated. • Section 9.2.4.8 “VersionReg register”: version: B2h updated. • Section 16.1 “Test signals”: selftest result updated.			
MFRC523_33	20100305	Product data sheet	-	MFRC523_32
Modifications:	• Table 106 “TModeReg register bit descriptions” and Table 108 “TPrescalerReg register bit descriptions”: text updated. • Section 8.7 “Timer unit”: input clock frequency changed to 13.56 MHz and text updated. • Table 154 “SPI timing characteristics”: NSS HIGH time, t_{NSSH} added.			
MFRC523_32	20100112	Product data sheet	-	115231

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Table 161. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • General re-wording of MIFARE designation and commercial conditions. • Table 106 “TModeReg register bit descriptions” and Table 108 “TPrescalerReg register bit descriptions”: changed value "f_{Timer} = 13.56 MHz / (TPreScaler + 1)". • Graphics: updated to latest standard. • Descriptive text: updated. • Register and bit names: updated. • Register tables: presentation updated. • Parameter symbols: updated. • Section 9 “MFRC523 registers” now follows Section 8 “Functional description”. • Section 16 “Test information” added, incorporating Section 16.1 “Test signals”.			
115231	May 2007	Product data sheet	-	115230
115230	September 2006	Product data sheet	-	115220
115220	August 2006	Preliminary data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
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[2] The term 'short data sheet' is explained in section "Definitions".

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