THE DATASHEET OF

MF10CCWMX/NOPB

www.win-source.net 0086-755-83957316

MF10-N Universal Monolithic Dual Switched Capacitor Filter

Check for Samples: MF10-N

FEATURES

- **Easy to Use**
- **Clock to Center Frequency Ratio Accuracy ±0.6%**
- **Filter Cutoff Frequency Stability Directly Dependent on External Clock Quality**
- **Low Sensitivity to External Component Variation**
- **Separate Highpass (or Notch or Allpass), Bandpass, Lowpass Outputs**
- **$f_O \times Q$ Range up to 200 kHz**
- **Operation up to 30 kHz**
- **20-pin 0.3″ Wide PDIP Package**
- **20-pin Surface Mount (SOIC) Wide-Body Package**

DESCRIPTION

The MF10-N consists of 2 independent and extremely easy to use, general purpose CMOS active filter building blocks. Each block, together with an external clock and 3 to 4 resistors, can produce various 2nd order functions. Each building block has 3 output pins. One of the outputs can be configured to perform either an allpass, highpass or a notch function; the remaining 2 output pins perform lowpass and bandpass functions. The center frequency of the lowpass and bandpass 2nd order functions can be either directly dependent on the clock frequency, or they can depend on both clock frequency and external resistor ratios. The center frequency of the notch and allpass functions is directly dependent on the clock frequency, while the highpass center frequency depends on both resistor ratio and clock. Up to 4th order functions can be performed by cascading the two 2nd order building blocks of the MF10-N; higher than 4th order functions can be obtained by cascading MF10-N packages. Any of the classical filter configurations (such as Butterworth, Bessel, Cauer and Chebyshev) can be formed.

For pin-compatible device with improved performance refer to LMF100 datasheet.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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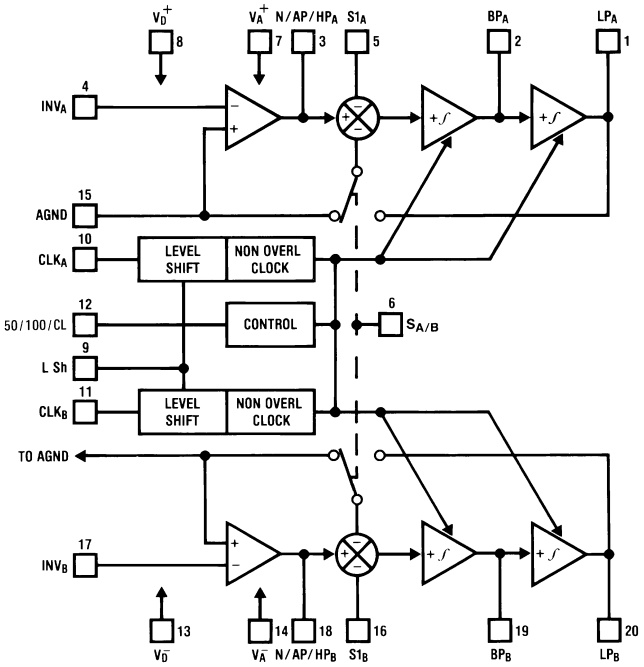
System Block Diagram



Package in 20 pin molded wide body SOIC and 20 pin PDIP.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Supply Voltage ($V^+ - V^-$)		14V
Voltage at Any Pin		$V^+ + 0.3V$
		$V^- - 0.3V$
Input Current at Any Pin[3]		5 mA
Package Input Current[3]		20 mA
Power Dissipation[4]		500 mW
Storage Temperature		150°C
ESD Susceptability[5]		2000V
Soldering Information	N Package: 10 sec	260°C
SO Package	Vapor Phase (60 Sec.)	215°C
	Infrared (15 Sec.)	220°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply boundaries with a 5 mA current limit to four.
(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{JMAX} = 125°C$, and the typical junction-to-ambient thermal resistance of the MF10ACN/CCN when board mounted is 55°C/W. For the MF10AJ/CCJ, this number increases to 95°C/W and for the MF10ACWM/CCWM this number is 66°C/W.
(5) Human body model, 100 pF discharged through a 1.5 kΩ resistor.

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Operating Ratings(1)

Temperature Range ($T_{MIN} \le T_A \le T_{MAX}$)	MF10ACN, MF10CCN, MF10CCWM	$0°C \le T_A \le 70°C$

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Electrical Characteristics

$V^+ = +5.00V$ and $V^- = -5.00V$ unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter		Conditions		MF10ACN, MF10CCN, MF10CCWM			Units
					Typical(1)	Tested Limit(2)	Design Limit(3)	
$V^+ - V^-$	Supply Voltage	Min					**9**	V
		Max					**14**	
I_S	Maximum Supply Current		Clock Applied to Pins 10 & 11 No Input Signal		8	12	**12**	mA
f_O	Center Frequency Range	Min	$f_O \times Q < 200$ kHz		0.1		**0.2**	Hz
		Max			30		**20**	kHz
f_{CLK}	Clock Frequency Range	Min			5.0		**10**	Hz
		Max			1.5		**1.0**	MHz
f_{CLK}/f_O	50:1 Clock to Center Frequency Ratio Deviation	MF10A	Q = 10, Mode 1	V_{pin12} = 5V f_{CLK} = 250 KHz	±0.2	±0.6	**±0.6**	%
		MF10C			±0.2	±1.5	**±1.5**	
f_{CLK}/f_O	100:1 Clock to Center Frequency Ratio Deviation	MF10A	Q = 10, Mode 1	V_{pin12} = 0V f_{CLK} = 500 kHz	±0.2	±0.6	**±0.6**	
		MF10C			±0.2	±1.5	**±1.5**	
	Clock Feedthrough		Q = 10, Mode 1		10			mV
	Q Error (MAX)(4)		Q = 10, Mode 1	V_{pin12} = 5V f_{CLK} = 250 kHz	±2	±6	**±6**	%
				V_{pin12} = 0V f_{CLK} = 500 kHz	±2	±6	**±6**	
H_{OLP}	DC Lowpass Gain		Mode 1 R1 = R2 = 10k		0	±0.2	**±0.2**	dB
V_{OS1}	DC Offset Voltage(5)				±5.0	±20	**±20**	mV
V_{OS2}	DC Offset Voltage(5)	Min	V_{pin12} = +5V (f_{CLK}/f_O = 50)	$S_{A/B} = V^+$	−150	−185	**−185**	mV
		Max				−85	**−85**	
		Min	V_{pin12} = +5V (f_{CLK}/f_O = 50)	$S_{A/B} = V^-$	−70			mV
		Max						
V_{OS3}	DC Offset Voltage(5)	Min	V_{pin12} = +5V (f_{CLK}/f_O = 50)	All Modes	−70	−100	**−100**	mV
		Max				−20	**−20**	
V_{OS2}	DC Offset Voltage (5)		V_{pin12} = 0V (f_{CLK}/f_O = 100)	$S_{A/B} = V^+$	−300			mV
			V_{pin12} = 0V (f_{CLK}/f_O = 100)	$S_{A/B} = V^-$	−140			mV
V_{OS3}	DC Offset Voltage(5)		V_{pin12} = 0V (f_{CLK}/f_O = 100)	All Modes	−140			mV
V_{OUT}	Minimum Output	BP, LP Pins	R_L = 5k		±4.25	±3.8	**±3.8**	V
	Voltage Swing	N/AP/HP Pin	R_L = 3.5k		±4.25	±3.8	**±3.8**	V
GBW	Op Amp Gain BW Product				2.5			MHz
SR	Op Amp Slew Rate				7			V/µs

(1) Typicals are at 25°C and represent most likely parametric norm.
(2) Tested limits are ensured to AOQL (Average Outgoing Quality Level).
(3) Design limits are specified but not 100% tested. These limits are not used to calculate outgoing quality levels.
(4) The accuracy of the Q value is a function of the center frequency (f_O). This is illustrated in the curves under the heading "Typical Performance Characteristics".
(5) V_{OS1}, V_{OS2}, and V_{OS3} refer to the internal offsets as discussed in OFFSET VOLTAGE.

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Electrical Characteristics (continued)

V^+ = +5.00V and V^- = −5.00V unless otherwise specified. **Boldface limits apply for T_{MIN} to T_{MAX};** all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter		Conditions	MF10ACN, MF10CCN, MF10CCWM			Units
				Typical (1)	Tested Limit (2)	Design Limit (3)	
	Dynamic Range (6)		V_{pin12} = +5V, (f_{CLK}/f_O = 50)	83			dB
			V_{pin12} = 0V, (f_{CLK}/f_O = 100)	80			dB
I_{SC}	Maximum Output Short Circuit Current (7)	Source		20			mA
		Sink		3.0			mA

(6) For ±5V supplies the dynamic range is referenced to 2.82V rms (4V peak) where the wideband noise over a 20 kHz bandwidth is typically 200 µV rms for the MF10-N with a 50:1 CLK ratio and 280 µV rms for the MF10-N with a 100:1 CLK ratio.

(7) The short circuit source current is measured by forcing the output that is being tested to its maximum positive voltage swing and then shorting that output to the negative supply. The short circuit sink current is measured by forcing the output that is being tested to its maximum negative voltage swing and then shorting that output to the positive supply. These are the worst case conditions.

Logic Input Characteristics

Boldface limits apply for T_{MIN} to T_{MAX}; all other limits $T_A = T_J$ = 25°C

Parameter		Conditions	MF10ACN, MF10CCN, MF10CCWM			Units
			Typical (1)	Tested Limit (2)	Design Limit (3)	
CMOS Clock Input Voltage	Min Logical “1”	V^+ = +5V, V^- = −5V, V_{LSh} = 0V		+3.0	**+3.0**	V
	Max Logical “0”			−3.0	**−3.0**	V
	Min Logical “1”	V^+ = +10V, V^- = 0V, V_{LSh} = +5V		+8.0	**+8.0**	V
	Max Logical “0”			+2.0	**+2.0**	V
TTL Clock Input Voltage	Min Logical “1”	V^+ = +5V, V^- = −5V, V_{LSh} = 0V		+2.0	**+2.0**	V
	Max Logical “0”			+0.8	**+0.8**	V
	Min Logical “1”	V^+ = +10V, V^- = 0V, V_{LSh} = 0V		+2.0	**+2.0**	V
	Max Logical “0”			+0.8	**+0.8**	V

(1) Typicals are at 25°C and represent most likely parametric norm.

(2) Tested limits are ensured to AOQL (Average Outgoing Quality Level).

(3) Design limits are specified but not 100% tested. These limits are not used to calculate outgoing quality levels.

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Typical Performance Characteristics

Power Supply Current vs. Power Supply Voltage

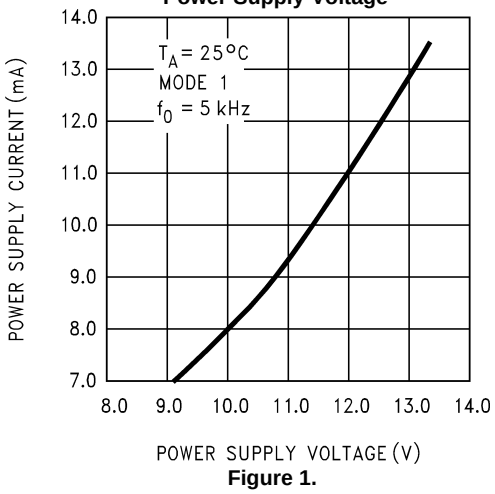

Figure 1.

Positive Output Voltage Swing vs. Load Resistance (N/AP/HP Output)

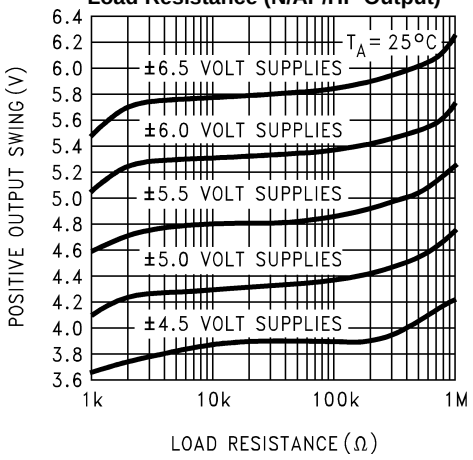

Figure 2.

Negative Output Voltage Swing vs. Load Resistance (N/AP/HP Output)

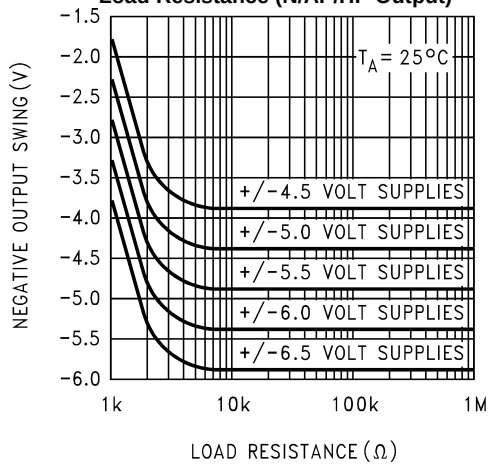

Figure 3.

Negative Output Swing vs. Temperature

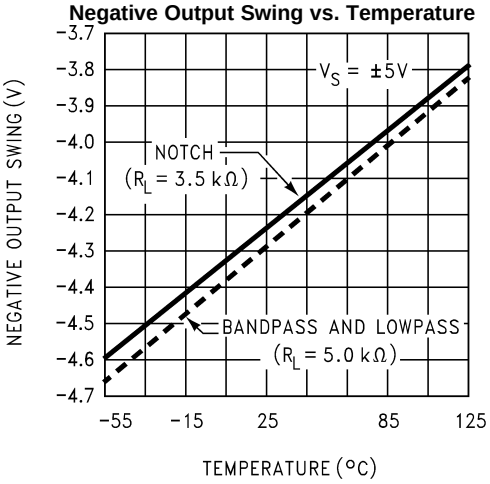

Figure 4.

Positive Output Swing vs. Temperature

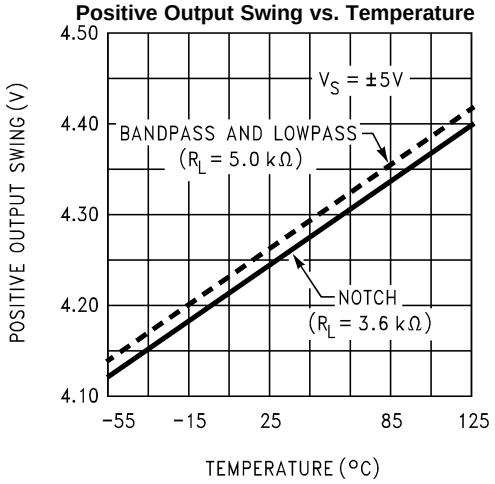

Figure 5.

Crosstalk vs. Clock Frequency

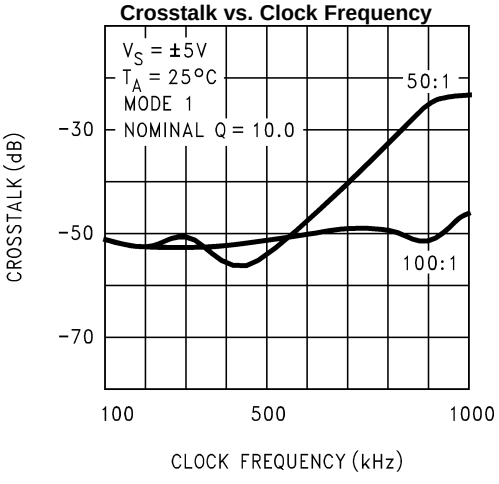

Figure 6.

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Typical Performance Characteristics (continued)

Q Deviation vs. Temperature

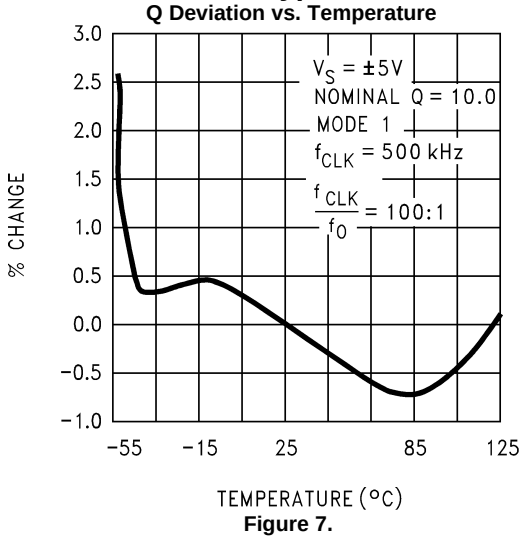

Figure 7.

Q Deviation vs. Temperature

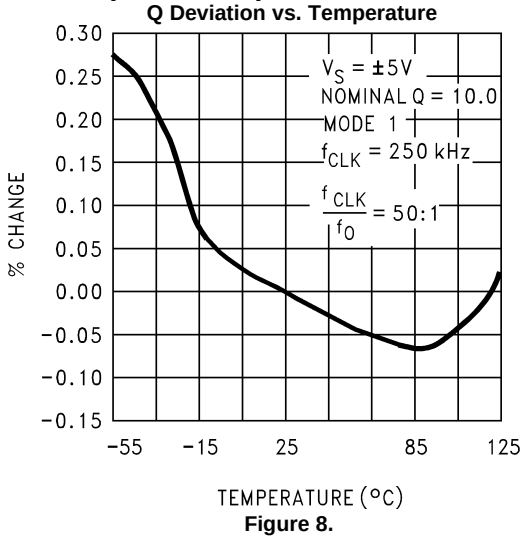

Figure 8.

Q Deviation vs. Clock Frequency

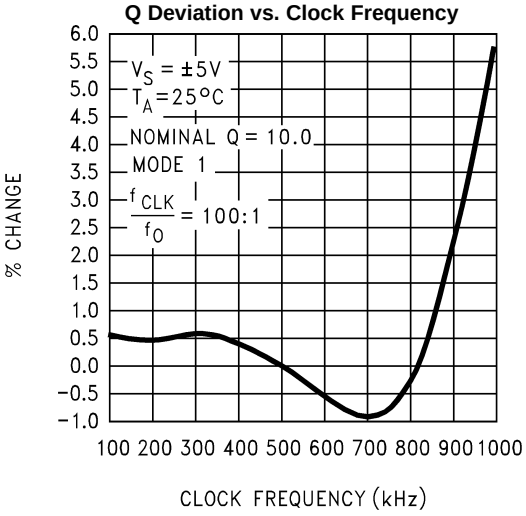

Figure 9.

Q Deviation vs. Clock Frequency

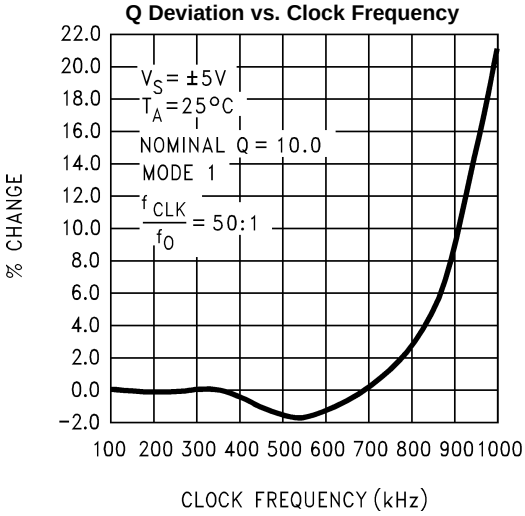

Figure 10.

f_{CLK}/f_O Deviation vs. Temperature

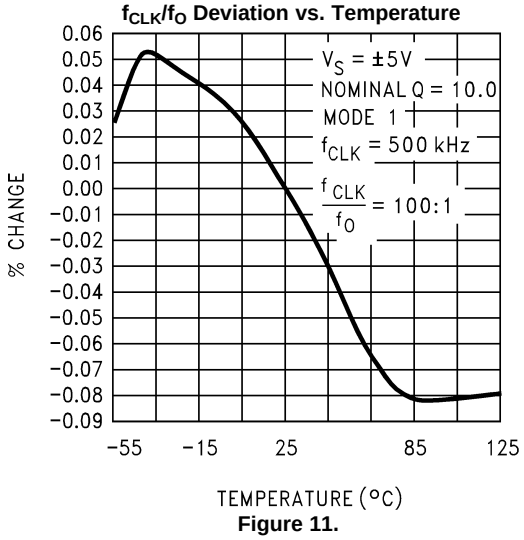

Figure 11.

f_{CLK}/f_O Deviation vs. Temperature

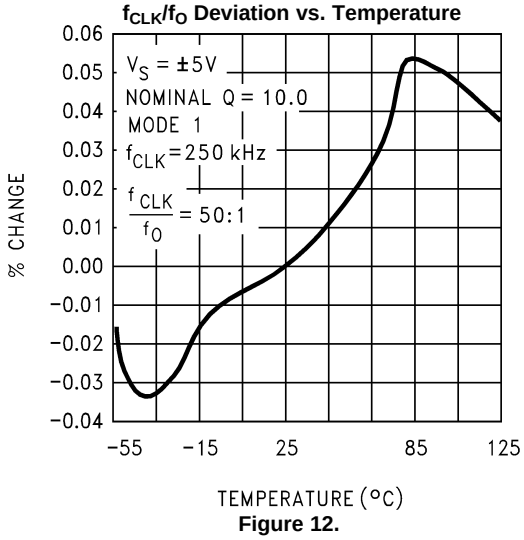

Figure 12.

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Typical Performance Characteristics (continued)

f_{CLK}/f_O Deviation vs. lock Frequency

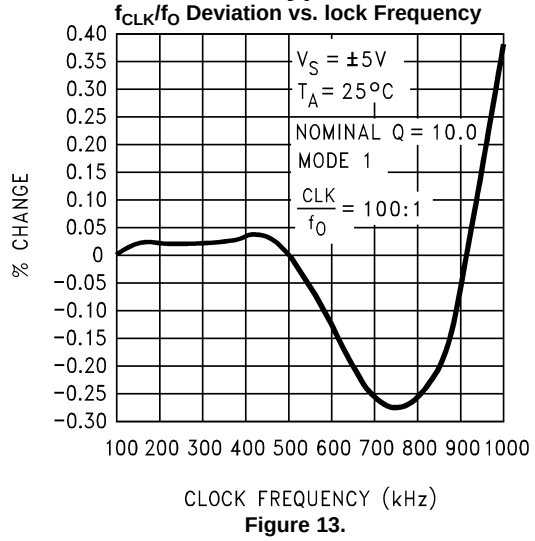

Figure 13.

f_{CLK}/f_O Deviation vs. Clock Frequency

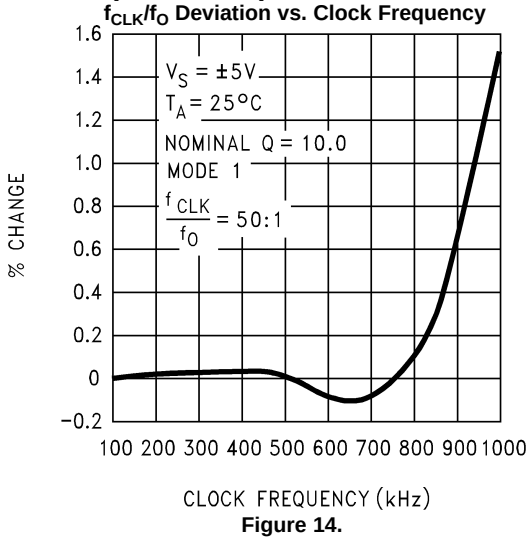

Figure 14.

Deviation of f_{CLK}/f_O vs. Nominal Q

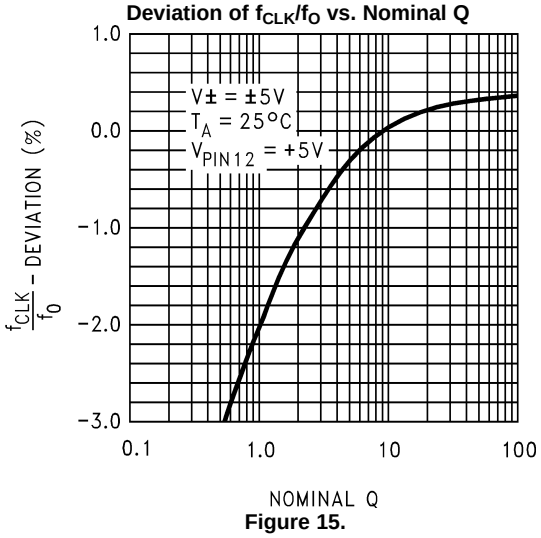

Figure 15.

Deviation of f_{CLK}/f_O vs. Nominal Q

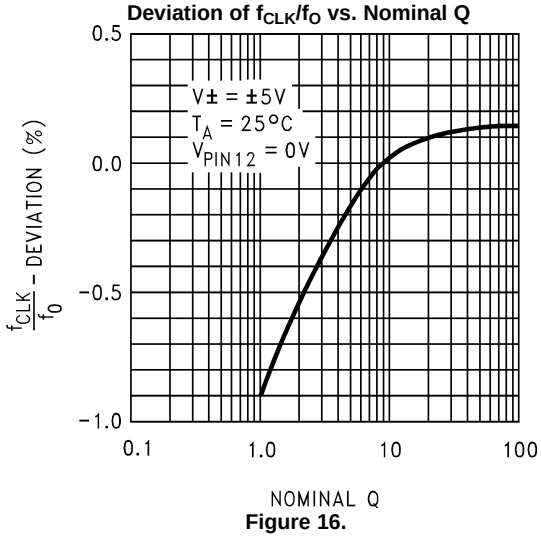

Figure 16.

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PIN DESCRIPTIONS

LP(1,20), BP(2,19), N/AP/HP(3,18) The second order lowpass, bandpass and notch/allpass/highpass outputs. These outputs can typically sink 1.5 mA and source 3 mA. Each output typically swings to within 1V of each supply.

INV(4,17) The inverting input of the summing op-amp of each filter. These are high impedance inputs, but the non-inverting input is internally tied to AGND, making INV_A and INV_B behave like summing junctions (low impedance, current inputs).

S1(5,16) S1 is a signal input pin used in the allpass filter configurations (see modes 4 and 5). The pin should be driven with a source impedance of less than 1 kΩ. If S1 is not driven with a signal it should be tied to AGND (mid-supply).

$S_{A/B}$(6) This pin activates a switch that connects one of the inputs of each filter's second summer to either AGND ($S_{A/B}$ tied to V^-) or to the lowpass (LP) output ($S_{A/B}$ tied to V^+). This offers the flexibility needed for configuring the filter in its various modes of operation.

V_A^+(7),V_D^+(8) Analog positive supply and digital positive supply. These pins are internally connected through the IC substrate and therefore V_A^+ and V_D^+ should be derived from the same power supply source. They have been brought out separately so they can be bypassed by separate capacitors, if desired. They can be externally tied together and bypassed by a single capacitor.

V_A^-(14), V_D^-(13) Analog and digital negative supplies. The same comments as for V_A^+ and V_D^+ apply here.

LSh(9) Level shift pin; it accommodates various clock levels with dual or single supply operation. With dual ±5V supplies, the MF10-N can be driven with CMOS clock levels (±5V) and the LSh pin should be tied to the system ground. If the same supplies as above are used but only TTL clock levels, derived from 0V to +5V supply, are available, the LSh pin should be tied to the system ground. For single supply operation (0V and +10V) the V_A^-, V_D^-pins should be connected to the system ground, the AGND pin should be biased at +5V and the LSh pin should also be tied to the system ground for TTL clock levels. LSh should be biased at +5V for CMOS clock levels in 10V single-supply applications.

CLKA(10), CLKB(11) Clock inputs for each switched capacitor filter building block. They should both be of the same level (TTL or CMOS). The level shift (LSh) pin description discusses how to accommodate their levels. The duty cycle of the clock should be close to 50% especially when clock frequencies above 200 kHz are used. This allows the maximum time for the internal op-amps to settle, which yields optimum filter operation.

50/100/CL(12) By tying this pin high a 50:1 clock-to-filter-center-frequency ratio is obtained. Tying this pin at mid-supplies (i.e. analog ground with dual supplies) allows the filter to operate at a 100:1 clock-to-center-frequency ratio. When the pin is tied low (i.e., negative supply with dual supplies), a simple current limiting circuit is triggered to limit the overall supply current down to about 2.5 mA. The filtering action is then aborted.

AGND(15) This is the analog ground pin. This pin should be connected to the system ground for dual supply operation or biased to mid-supply for single supply operation. For a further discussion of mid-supply biasing techniques see the Applications Information. For optimum filter performance a “clean” ground must be provided.

Definition of Terms

f_{CLK}: the frequency of the external clock signal applied to pin 10 or 11.

f_O: center frequency of the second order function complex pole pair. f_O is measured at the bandpass outputs of the MF10-N, and is the frequency of maximum bandpass gain (Figure 17).

f_{notch}: the frequency of minimum (ideally zero) gain at the notch outputs.

f_Z: the center frequency of the second order complex zero pair, if any. If f_z is different from f_O and if Q_Z is high, it can be observed as the frequency of a notch at the allpass output (Figure 26).

Q: “quality factor” of the 2nd order filter. Q is measured at the bandpass outputs of the MF10-N and is equal to f_O divided by the −3 dB bandwidth of the 2nd order bandpass filter (Figure 17). The value of Q determines the shape of the 2nd order filter responses as shown in Figure 22.

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Q_Z: the quality factor of the second order complex zero pair, if any. Q_Z is related to the allpass characteristic, which is written:

$$H_{AP}(s) = \frac{H_{OAP}\left(s^2 - \frac{s\omega_O}{Q_Z} + \omega_O^2\right)}{s^2 + \frac{s\omega_O}{Q} + \omega_O^2} \quad (1)$$

where $Q_Z = Q$ for an all-pass response.

H_{OBP}: the gain (in V/V) of the bandpass output at $f = f_O$.

H_{OLP}: the gain (in V/V) of the lowpass output as $f \rightarrow 0$ Hz (Figure 18).

H_{OHP}: the gain (in V/V) of the highpass output as $f \rightarrow f_{CLK}/2$ (Figure 19).

H_{ON}: the gain (in V/V) of the notch output as $f \rightarrow 0$ Hz and as $f \rightarrow f_{CLK}/2$, when the notch filter has equal gain above and below the center frequency (Figure 20). When the low-frequency gain differs from the high-frequency gain, as in modes 2 and 3a (Figure 27 and Figure 24), the two quantities below are used in place of H_{ON}.

H_{ON1}: the gain (in V/V) of the notch output as $f \rightarrow 0$ Hz.

H_{ON2}: the gain (in V/V) of the notch output as $f \rightarrow f_{CLK}/2$.

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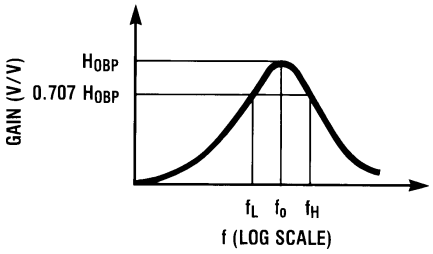
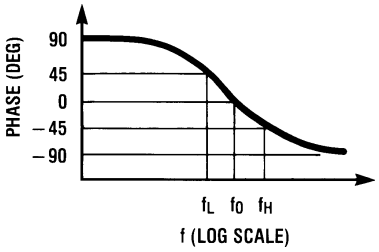


(a)



(b)

$$H_{BP}(s) = \frac{H_{OBP}\frac{\omega O}{Q}S}{s^2 + \frac{s\omega_O}{Q} + \omega_O{}^2}$$

$$Q = \frac{f_O}{f_H - f_L};\ f_O = \sqrt{f_L f_H}$$

$$f_L = f_O\left(\frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

$$f_H = f_O\left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

$$\omega_O = 2\pi f_O$$

Figure 17. 2nd-Order Bandpass Response

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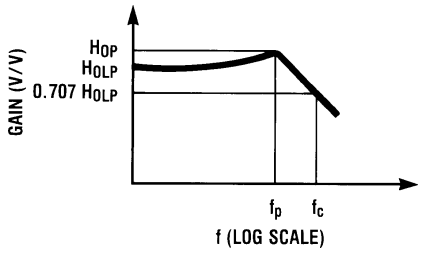
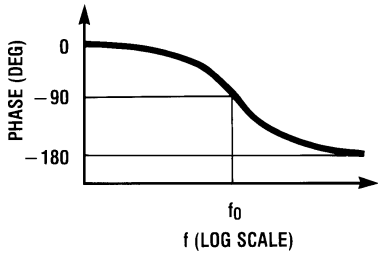


(a)



(b)

$$H_{LP}(s) = \frac{H_{OLP}\omega_O^2}{s^2 + \frac{s\omega_O}{Q} + \omega_O^2}$$

$$f_C = f_O \times \sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}$$

$$f_p = f_O \sqrt{1 - \frac{1}{2Q^2}}$$

$$H_{OP} = H_{OLP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

Figure 18. 2nd-Order Low-Pass Response

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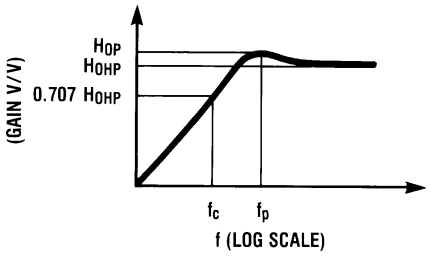
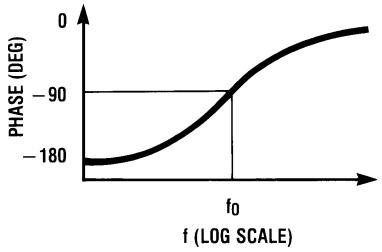


(a)



(b)

$$H_{HP}(s) = \frac{H_{OHP}s^2}{s^2 + \frac{s\omega_O}{Q} + \omega_O^2}$$

$$f_C = f_O \times \left[\sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}\right]^{-1}$$

$$f_p = f_O \times \left[\sqrt{1 - \frac{1}{2Q^2}}\right]^{-1}$$

$$H_{OP} = H_{OHP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

Figure 19. 2nd-Order High-Pass Response

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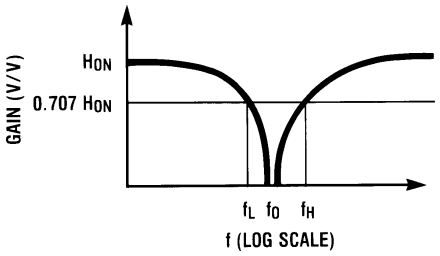
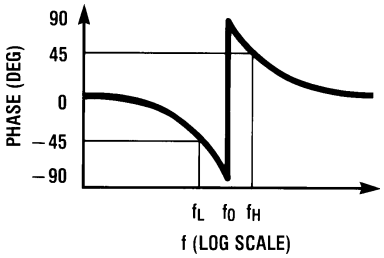


(a)



(b)

$$H_N(s) = \frac{H_{ON}(s^2 + \omega_O^2)}{s^2 + \frac{s\omega_O}{Q} + \omega_O^2}$$

$$Q = \frac{f_O}{f_H - f_L};\ f_O = \sqrt{f_L f_H}$$

$$f_L = f_O \left(\frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1} \right)$$

$$f_H = f_O \left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1} \right)$$

Figure 20. 2nd-Order Notch Response

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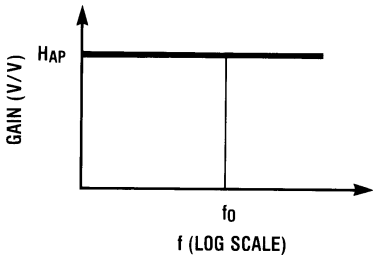
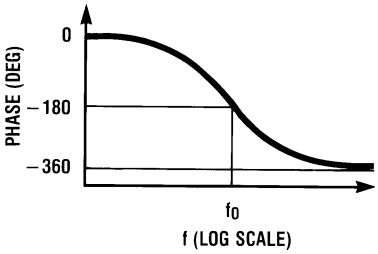


(a)



(b)

$$H_{AP}(s) = \frac{H_{OAP}\left(s^2 - \frac{s\omega_O}{Q} + \omega_O^2\right)}{s^2 + \frac{s\omega_O}{Q} + \omega_O^2}$$

Figure 21. 2nd-Order All-Pass Response

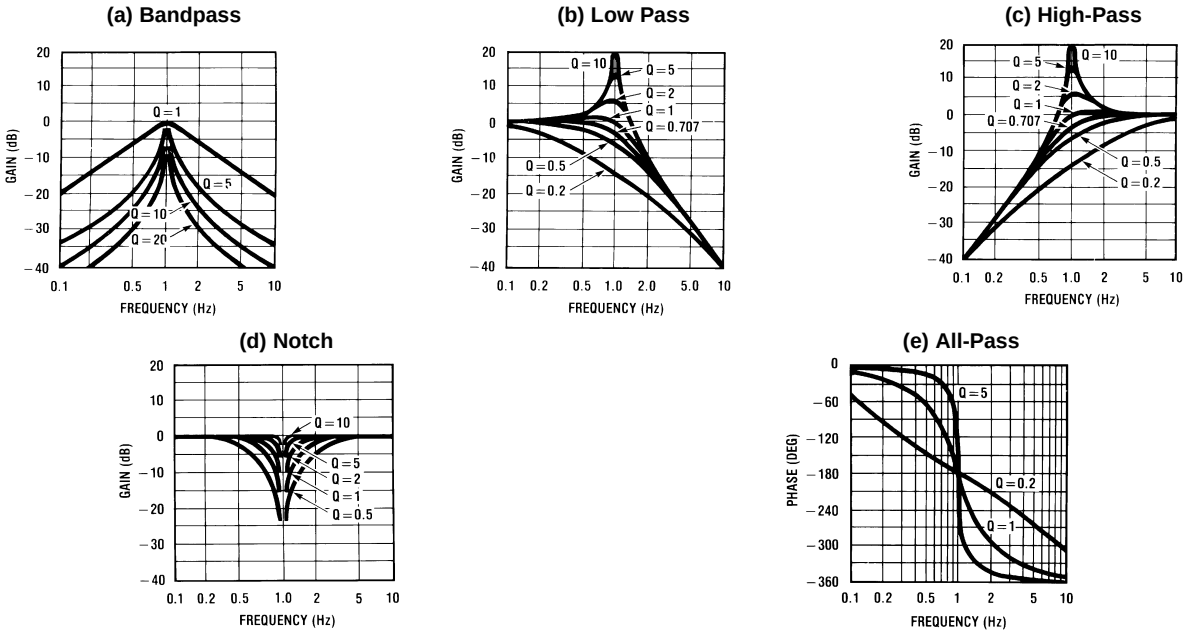


Figure 22. Response of various 2nd-order filters as a function of Q. Gains and center frequencies are normalized to unity.

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Modes of Operation

The MF10-N is a switched capacitor (sampled data) filter. To fully describe its transfer functions, a time domain approach is appropriate. Since this is cumbersome, and since the MF10-N closely approximates continuous filters, the following discussion is based on the well known frequency domain. Each MF10-N can produce a full 2nd order function. See Table 1 for a summary of the characteristics of the various modes.

MODE 1: Notch 1, Bandpass, Lowpass Outputs:

$$f_{notch} = f_O \text{ (See Figure 23)} \tag{2}$$

f_O= center frequency of the complex pole pair

$$= \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50} \tag{3}$$

f_{notch}= center frequency of the imaginary zero pair = f_O.

$$H_{OLP} = \text{Lowpass gain (as } f \rightarrow 0) = -\frac{R2}{R1}$$

$$H_{OBP} = \text{Bandpass gain (at } f = f_O) = -\frac{R3}{R1}$$

$$H_{ON} = \text{Notch output gain as } \left.\begin{matrix} f \rightarrow 0 \\ f \rightarrow f_{CLK}/2 \end{matrix}\right\} = \frac{-R_2}{R_1} \tag{4}$$

$$Q = \frac{f_O}{BW} = \frac{R3}{R2} \tag{5}$$

= quality factor of the complex pole pair

BW = the −3 dB bandwidth of the bandpass output.

Circuit dynamics:

$$H_{OLP} = \frac{H_{OBP}}{Q} \text{ or } H_{OBP} = H_{OLP} \times Q$$

$$= H_{ON} \times Q.$$

$$H_{OLP(peak)} \cong Q \times H_{OLP} \text{ (for high Q's)} \tag{6}$$

MODE 1a: Non-Inverting BP, LP (See Figure 24)

$$f_O = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

$$Q = \frac{R3}{R2}$$

$$H_{OLP} = -1;\ H_{OLP(peak)} \cong Q \times H_{OLP} \text{ (for high Q's)}$$

$$H_{OBP_1} = -\frac{R3}{R2}$$

$$H_{OBP_2} = 1 \text{ (Non-Inverting)}$$

Circuit Dynamics: $H_{OBP1} = Q$ (7)

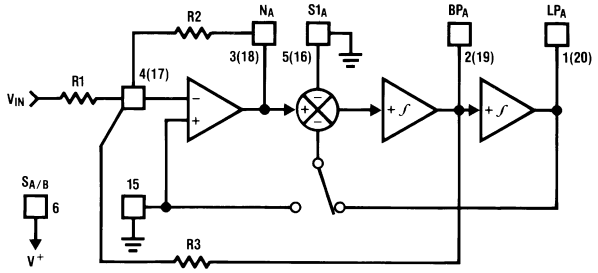

Figure 23. MODE 1

V_{IN} should be driven from a low impedance (<1 kΩ) source.

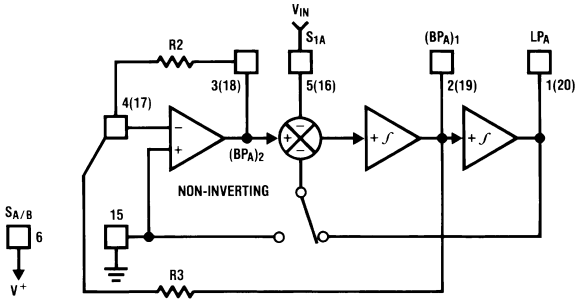

Figure 24. MODE 1a

MODE 2: Notch 2, Bandpass, Lowpass: $f_{notch} < f_O$ (See Figure 25)

$$f_O = \text{center frequency} = \frac{f_{CLK}}{100}\sqrt{\frac{R2}{R4}+1} \text{ or } \frac{f_{CLK}}{50}\sqrt{\frac{R2}{R4}+1}$$

$$f_{notch} = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

$$Q = \text{quality factor of the complex pole pair} = \frac{\sqrt{R2/R4+1}}{R2/R3}$$

$$H_{OLP} = \text{Lowpass output gain (as } f \longrightarrow 0) = -\frac{R2/R1}{R2/R4+1}$$

$$H_{OBP} = \text{Bandpass output gain (at } f = f_O) = -R3/R1$$

$$H_{ON_1} = \text{Notch output gain (as } f \longrightarrow 0) = -\frac{R2/R1}{R2/R4+1}$$

$$H_{ON_2} = \text{Notch output gain}\left(\text{as } f \longrightarrow \frac{f_{CLK}}{2}\right) = -R2/R1$$

$$\text{Filter dynamics: } H_{OBP} = Q\sqrt{H_{OLP}\,H_{ON_2}} = \sqrt{H_{ON1}\,H_{ON2}} \tag{8}$$

MODE 3: Highpass, Bandpass, Lowpass Outputs (See Figure 26)

$$f_O = \frac{f_{CLK}}{100}\times\sqrt{\frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50}\times\sqrt{\frac{R2}{R4}}$$

$$Q = \text{quality factor of the complex pole pair} = \sqrt{\frac{R2}{R4}}\times\frac{R3}{R2}$$

$$H_{OHP} = \text{Highpass Gain}\left(\text{as } f \longrightarrow \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1}$$

$$H_{OBP} = \text{Lowpass Gain}\left(\text{at } f = f_O\right) = -\frac{R3}{R1}$$

$$H_{OLP} = \text{Lowpass Gain}\left(\text{as } f \longrightarrow 0\right) = -\frac{R4}{R1}$$

$$\text{Circuit dynamics: } \frac{R2}{R4} = \frac{H_{OHP}}{H_{OLP}};\quad H_{OBP} = \sqrt{H_{OHP}\times H_{OLP}}\times Q$$

$$H_{OLP(peak)} \cong Q \times H_{OLP} \text{ (for high Q's)}$$

$$H_{OHP(peak)} \cong Q \times H_{OHP} \text{ (for high Q's)} \tag{9}$$

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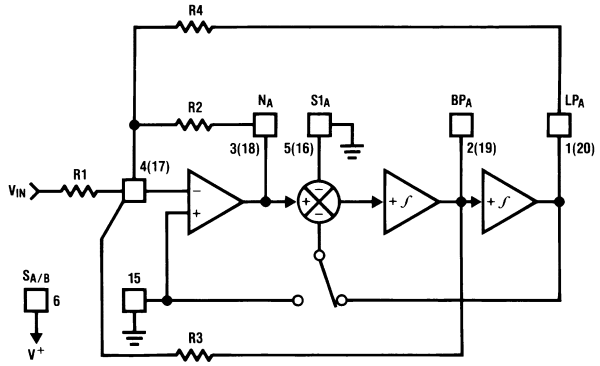
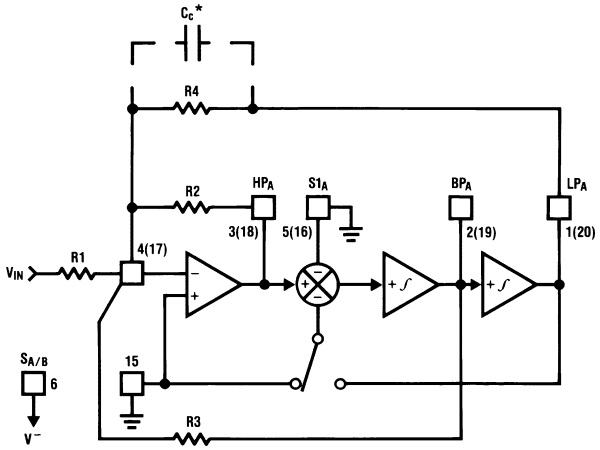


Figure 25. MODE 2



*In Mode 3, the feedback loop is closed around the input summing amplifier; the finite GBW product of this op amp causes a slight Q enhancement. If this is a problem, connect a small capacitor (10 pF − 100 pF) across R4 to provide some phase lead.

Figure 26. MODE 3

MODE 3a: HP, BP, LP and Notch with External Op Amp (See Figure 27)

$$f_O = \frac{f_{CLK}}{100} \times \sqrt{\frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{\frac{R2}{R4}}$$

$$Q = \sqrt{\frac{R2}{R4}} \times \frac{R3}{R2}$$

$$H_{OHP} = -\frac{R2}{R1}$$

$$H_{OBP} = -\frac{R3}{R1}$$

$$H_{OLP} = -\frac{R4}{R1}$$

$$f_n = \text{notch frequency} = \frac{f_{CLK}}{100}\sqrt{\frac{R_h}{R_l}} \text{ or } \frac{f_{CLK}}{50}\sqrt{\frac{R_h}{R_l}}$$

$$H_{ON} = \text{gain of notch at } f = f_O = \left\| Q\left(\frac{R_g}{R_l} H_{OLP} - \frac{R_g}{R_h} H_{OHP}\right)\right\|$$

$$H_{n1} = \text{gain of notch (as } f \rightarrow 0) = \frac{R_g}{R_l} \times H_{OLP}$$

$$H_{n2} = \text{gain of notch}\left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = -\frac{R_g}{R_h} \times H_{OHP} \quad (10)$$

MODE 4: Allpass, Bandpass, Lowpass Outputs (See Figure 28)

f_O = center frequency

$$= \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50};$$

f_z* = center frequency of the complex zero $\approx f_O$

$$Q = \frac{f_O}{BW} = \frac{R3}{R2};$$

Q_Z = quality factor of complex zero pair $= \frac{R3}{R1}$

For AP output make R1 = R2

$$H_{OAP}* = \text{Allpass gain}\left(\text{at } 0 < f < \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1} = -1$$

$$H_{OLP} = \text{Lowpass gain (as } f \rightarrow 0) = -\left(\frac{R2}{R1} + 1\right) = -2$$

$$H_{OBP} = \text{Bandpass gain (at } f = f_O) = -\frac{R3}{R2}\left(1 + \frac{R2}{R1}\right) = -2\left(\frac{R3}{R2}\right)$$

Circuit Dynamics: $H_{OBP} = (H_{OLP}) \times Q = (H_{OAP} + 1)Q$ (11)

*Due to the sampled data nature of the filter, a slight mismatch of f_z and f_O occurs causing a 0.4 dB peaking around f_O of the allpass filter amplitude response (which theoretically should be a straight line). If this is unacceptable, Mode 5 is recommended.

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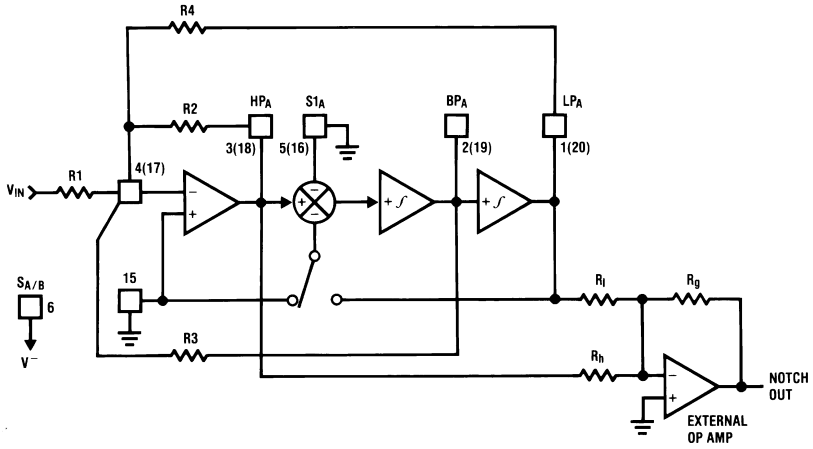

Figure 27. MODE 3a

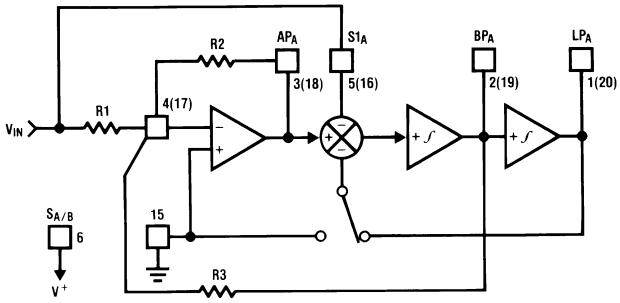

Figure 28. MODE 4

MODE 5: Numerator Complex Zeros, BP, LP (See Figure 29)

$$f_O = \sqrt{1 + \frac{R2}{R4}} \times \frac{f_{CLK}}{100} \text{ or } \sqrt{1 + \frac{R2}{R4}} \times \frac{f_{CLK}}{50}$$

$$f_z = \sqrt{1 - \frac{R2}{R4}} \times \frac{f_{CLK}}{100} \text{ or } \sqrt{1 - \frac{R1}{R4}} \times \frac{f_{CLK}}{50}$$

$$Q = \sqrt{1 + R2/R4} \times \frac{R3}{R2}$$

$$Q_Z = \sqrt{1 - R1/R4} \times \frac{R3}{R1}$$

$$H_{0_{z1}} = \text{gain at C.Z. output (as } f \rightarrow 0 \text{ Hz)} = \frac{-R2(R4 - R1)}{R1(R2 + R4)}$$

$$H_{0_{z2}} = \text{gain at C.Z. output} \left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = \frac{-R2}{R1}$$

$$H_{OBP} = -\left(\frac{R2}{R1} + 1\right) \times \frac{R3}{R2}$$

$$H_{OLP} = -\left(\frac{R2 + R1}{R2 + R4}\right) \times \frac{R4}{R1} \quad (12)$$

MODE 6a: Single Pole, HP, LP Filter (See Figure 30)

$$
\begin{aligned}
f_c &= \text{cutoff frequency of LP or HP output} \\
&= \frac{R2}{R3}\,\frac{f_{CLK}}{100} \text{ or } \frac{R2}{R3}\,\frac{f_{CLK}}{50} \\
H_{OLP} &= -\frac{R3}{R1} \\
H_{OHP} &= -\frac{R2}{R1}
\end{aligned}
\tag{13}
$$

MODE 6b: Single Pole LP Filter (Inverting and Non-Inverting) (See Figure 31)

$$
\begin{aligned}
f_c &= \text{cutoff frequency of LP outputs} \\
&\cong \frac{R2}{R3}\,\frac{f_{CLK}}{100} \text{ or } \frac{R2}{R3}\,\frac{f_{CLK}}{50} \\
H_{OLP1} &= 1 \text{ (non-inverting)} \\
H_{OLP2} &= -\frac{R3}{R2}
\end{aligned}
\tag{14}
$$

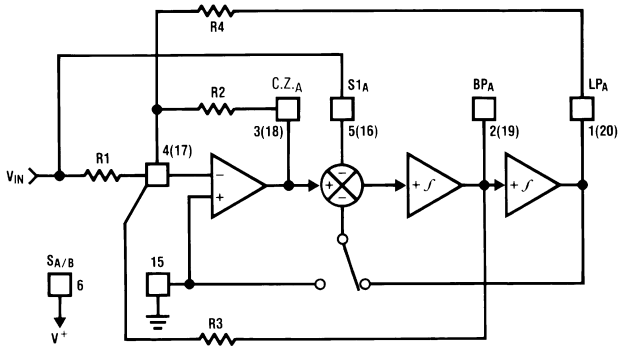

Figure 29. MODE 5

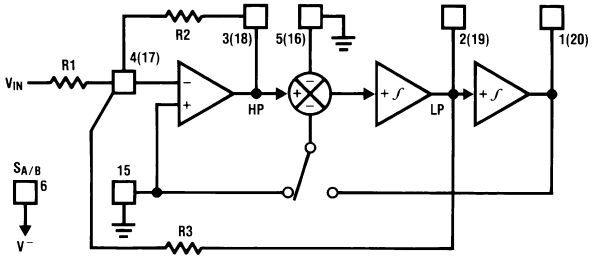

Figure 30. MODE 6a

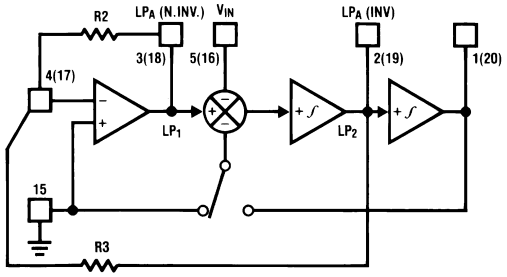

Figure 31. MODE 6b

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Table 1. Summary of Modes. Realizable filter types (e.g. low-pass) denoted by asterisks. Unless otherwise noted, gains of various filter outputs are inverting and adjustable by resistor ratios.

Mode	BP	LP	HP	N	AP	Number of Resistors	Adjustable f_{CLK}/f_O	Notes
1	*	*		*		3	No	
1a	$H_{OBP1} = -Q$ $H_{OBP2} = +1$	$H_{OLP} + 1$				2	No	May need input buffer. Poor dynamics for high Q.
2	*	*		*		3	Yes (above $f_{CLK}/50$ or $f_{CLK}/100$)	
3	*	*	*			4	Yes	Universal State-Variable Filter. Best general-purpose mode.
3a	*	*	*	*		7	Yes	As above, but also includes resistor-tuneable notch.
4	*	*			*	3	No	Gives Allpass response with $H_{OAP} = -1$ and $H_{OLP} = -2$.
5	*	*			*	4		Gives flatter allpass response than above if $R_1 = R_2 = 0.02R_4$.
6a		*	*			3		Single pole.
6b		HOLP1 = +1 HOLP2 = -R3/R2				2		Single pole.

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APPLICATIONS INFORMATION

The MF10-N is a general-purpose dual second-order state variable filter whose center frequency is proportional to the frequency of the square wave applied to the clock input (f_{CLK}). By connecting pin 12 to the appropriate DC voltage, the filter center frequency f_O can be made equal to either $f_{CLK}/100$ or $f_{CLK}/50$. f_O can be very accurately set (within ±6%) by using a crystal clock oscillator, or can be easily varied over a wide frequency range by adjusting the clock frequency. If desired, the f_{CLK}/f_O ratio can be altered by external resistors as in Figure 25, Figure 26, Figure 27, Figure 29, Figure 30, and Figure 31. The filter Q and gain are determined by external resistors.

All of the five second-order filter types can be built using either section of the MF10-N. These are illustrated in Figure 17 through Figure 21 along with their transfer functions and some related equations. Figure 22 shows the effect of Q on the shapes of these curves. When filter orders greater than two are desired, two or more MF10-N sections can be cascaded.

DESIGN EXAMPLE

In order to design a second-order filter section using the MF10-N, we must define the necessary values of three parameters: f_0, the filter section's center frequency; H_0, the passband gain; and the filter's Q. These are determined by the characteristics required of the filter being designed.

As an example, let's assume that a system requires a fourth-order Chebyshev low-pass filter with 1 dB ripple, unity gain at DC, and 1000 Hz cutoff frequency. As the system order is four, it is realizable using both second-order sections of an MF10-N. Many filter design texts include tables that list the characteristics (f_O and Q) of each of the second-order filter sections needed to synthesize a given higher-order filter. For the Chebyshev filter defined above, such a table yields the following characteristics:

f_{0A} = 529 Hz $Q_A = 0.785$

f_{0B} = 993 Hz $Q_B = 3.559$

For unity gain at DC, we also specify:

$H_{0A} = 1$

$H_{0B} = 1$

The desired clock-to-cutoff-frequency ratio for the overall filter of this example is 100 and a 100 kHz clock signal is available. Note that the required center frequencies for the two second-order sections will not be obtainable with clock-to-center-frequency ratios of 50 or 100. It will be necessary to adjust

$$\frac{f_{CLK}}{f_0} \tag{15}$$

externally. From Table 1, we see that Mode 3 can be used to produce a low-pass filter with resistor-adjustable center frequency.

In most filter designs involving multiple second-order stages, it is best to place the stages with lower Q values ahead of stages with higher Q, especially when the higher Q is greater than 0.707. This is due to the higher relative gain at the center frequency of a higher-Q stage. Placing a stage with lower Q ahead of a higher-Q stage will provide some attenuation at the center frequency and thus help avoid clipping of signals near this frequency. For this example, stage A has the lower Q (0.785) so it will be placed ahead of the other stage.

For the first section, we begin the design by choosing a convenient value for the input resistance: R_{1A} = 20k. The absolute value of the passband gain H_{OLPA} is made equal to 1 by choosing R_{4A} such that: $R_{4A} = -H_{OLPA}R_{1A} = R_{1A}$ = 20k. If the 50/100/CL pin is connected to mid-supply for nominal 100:1 clock-to-center-frequency ratio, we find R_{2A} by:

$$R_{2A} = R_{4A}\frac{f_{0A}^2}{(f_{CLK}/100)^2} = 2 \times 10^4 \times \frac{(529)^2}{(1000)^2} = 5.6\text{k and}$$

$$R_{3A} = Q_A\sqrt{R_{2A}R_{4A}} = 0.785\sqrt{5.6 \times 10^3 \times 2 \times 10^4} = 8.3\text{k} \tag{16}$$

The resistors for the second section are found in a similar fashion:

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$$R_{1B} = 20k$$
$$R_{4B} = R_{1B} = 20k$$
$$R_{2B} = R_{4B}\frac{f_{0B}^2}{(f_{CLK}/100)^2} = 20k\frac{(993)^2}{(1000)^2} = 19.7k$$
$$R_{3B} = Q_B\sqrt{R_{2B}R_{4B}} = 3.559\sqrt{1.97\times10^4\times2\times10^4} = 70.6k \quad (17)$$

The complete circuit is shown in Figure 32 for split ±5V power supplies. Supply bypass capacitors are highly recommended.

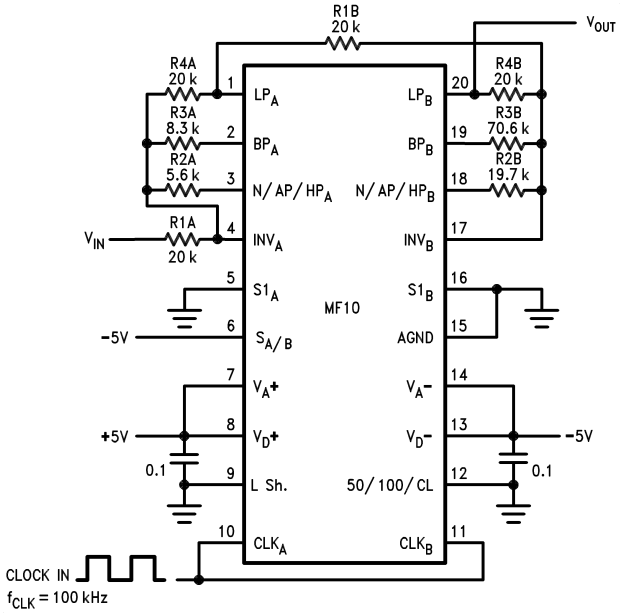

Figure 32. Fourth-Order Chebyshev Low-Pass Filter from Example in 3.1. ±5V Power Supply. 0V–5V TTL or −5V ±5V CMOS Logic Levels.

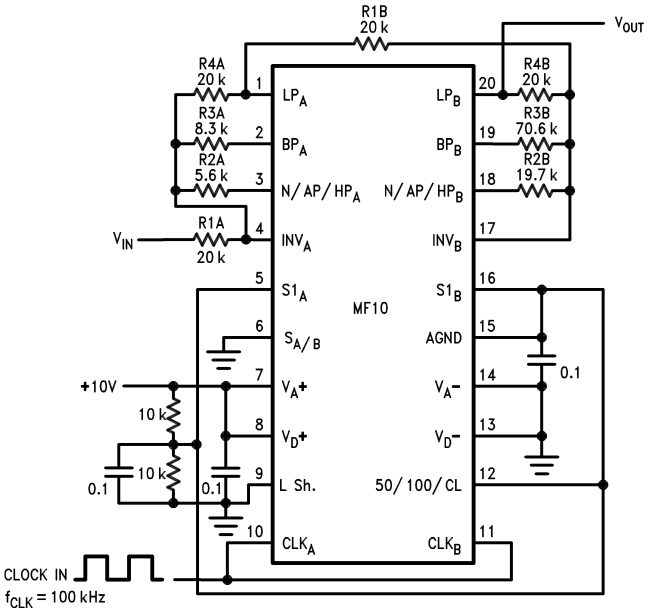

Figure 33. Fourth-Order Chebyshev Low-Pass Filter from Example in 3.1. Single +10V Power Supply. 0V–5V TTL Logic Levels. Input Signals Should be Referred to Half-Supply or Applied through a Coupling Capacitor.

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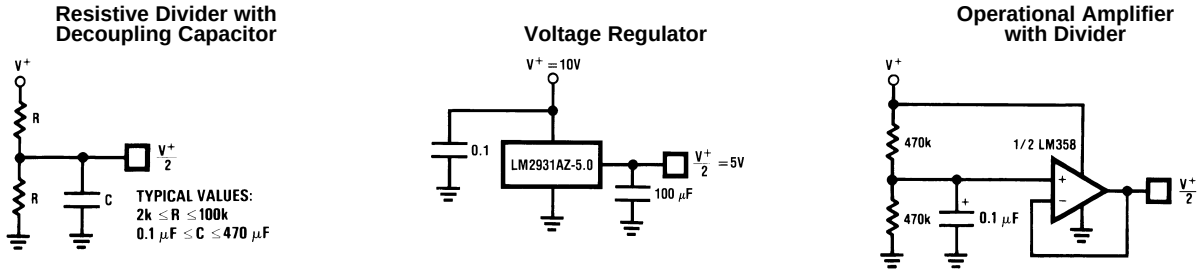

Figure 34. Three Ways of Generating $V^+/2$ for Single-Supply Operation

SINGLE SUPPLY OPERATION

The MF10-N can also operate with a single-ended power supply. Figure 33 shows the example filter with a single-ended power supply. V_A^+ and V_D^+ are again connected to the positive power supply (8V to 14V), and V_A^- and V_D^- are connected to ground. The A_{GND} pin must be tied to $V^+/2$ for single supply operation. This half-supply point should be very “clean”, as any noise appearing on it will be treated as an input to the filter. It can be derived from the supply voltage with a pair of resistors and a bypass capacitor (See Figure 34), or a low-impedance half-supply voltage can be made using a three-terminal voltage regulator or an operational amplifier (See Figure 34 and Figure 34). The passive resistor divider with a bypass capacitor is sufficient for many applications, provided that the time constant is long enough to reject any power supply noise. It is also important that the half-supply reference present a low impedance to the clock frequency, so at very low clock frequencies the regulator or op-amp approaches may be preferable because they will require smaller capacitors to filter the clock frequency. The main power supply voltage should be clean (preferably regulated) and bypassed with 0.1 µF.

DYNAMIC CONSIDERATIONS

The maximum signal handling capability of the MF10-N, like that of any active filter, is limited by the power supply voltages used. The amplifiers in the MF10-N are able to swing to within about 1V of the supplies, so the input signals must be kept small enough that none of the outputs will exceed these limits. If the MF10-N is operating on ±5V, for example, the outputs will clip at about 8 V_{p-p}. The maximum input voltage multiplied by the filter gain should therefore be less than 8 V_{p-p}.

Note that if the filter Q is high, the gain at the lowpass or highpass outputs will be much greater than the nominal filter gain (Figure 22). As an example, a lowpass filter with a Q of 10 will have a 20 dB peak in its amplitude response at f_O. If the nominal gain of the filter H_{OLP} is equal to 1, the gain at f_O will be 10. The maximum input signal at f_O must therefore be less than 800 mV_{p-p} when the circuit is operated on ±5V supplies.

Also note that one output can have a reasonable small voltage on it while another is saturated. This is most likely for a circuit such as the notch in Mode 1 (Figure 23). The notch output will be very small at f_O, so it might appear safe to apply a large signal to the input. However, the bandpass will have its maximum gain at f_O and can clip if overdriven. If one output clips, the performance at the other outputs will be degraded, so avoid overdriving any filter section, even ones whose outputs are not being directly used. Accompanying Figure 23 through Figure 31 are equations labeled “circuit dynamics”, which relate the Q and the gains at the various outputs. These should be consulted to determine peak circuit gains and maximum allowable signals for a given application.

OFFSET VOLTAGE

The MF10-N's switched capacitor integrators have a higher equivalent input offset voltage than would be found in a typical continuous-time active filter integrator. Figure 35 shows an equivalent circuit of the MF10-N from which the output DC offsets can be calculated. Typical values for these offsets with $S_{A/B}$ tied to V^+ are:

V_{os1} = opamp offset = ±5 mV	
V_{os2} = −150 mV @ 50:1	−300 mV @ 100:1
V_{os3} = −70 mV @ 50:1	−140 mV @ 100:1

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When $S_{A/B}$ is tied to V^-, V_{os2} will approximately halve. The DC offset at the BP output is equal to the input offset of the lowpass integrator (V_{os3}). The offsets at the other outputs depend on the mode of operation and the resistor ratios, as described in the following expressions.

Mode 1 and Mode 4

$$V_{OS(N)} = V_{OS1}\left(\frac{1}{Q} + 1\left\|H_{OLP}\right\|\right) - \frac{V_{OS3}}{Q}$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N)} - V_{OS2}$$

Mode 1a

$$V_{OS(N.INV.BP)} = \left(1 + \frac{1}{Q}\right)V_{OS1} - \frac{V_{OS3}}{Q}$$

$$V_{OS(INV.BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N.INV.BP)} - V_{OS2} \quad (18)$$

Mode 2 and Mode 5

$$V_{OS(N)} = \left(\frac{R2}{R_p} + 1\right)V_{OS1} \times \frac{1}{1 + R2/R4} + V_{OS2}\frac{1}{1 + R4/R2} - \frac{V_{OS3}}{Q\sqrt{1 + R2/R4}}$$

$$R_p = R1//R3//R4$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N)} - V_{OS2}$$

Mode 3

$$V_{OS(HP)} = V_{OS2}$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS1}\left[1 + \frac{R4}{R_p}\right] - V_{OS2}\left(\frac{R4}{R2}\right) - V_{OS3}\left(\frac{R4}{R3}\right)$$

$$Rp = R1//R2//R3 \quad (19)$$

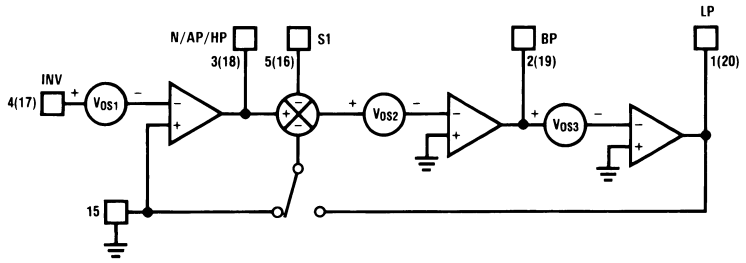

Figure 35. MF10-N Offset Voltage Sources

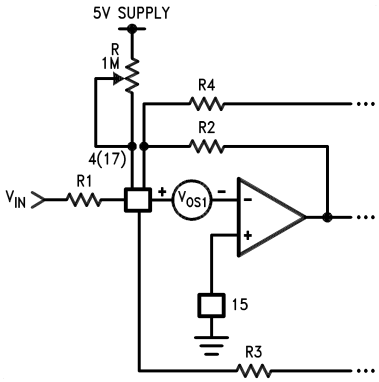

Figure 36. Method for Trimming V_{OS}

For most applications, the outputs are AC coupled and DC offsets are not bothersome unless large signals are applied to the filter input. However, larger offset voltages will cause clipping to occur at lower AC signal levels, and clipping at any of the outputs will cause gain nonlinearities and will change f_O and Q. When operating in Mode 3, offsets can become excessively large if R2 and R4 are used to make f_{CLK}/f_O significantly higher than the nominal value, especially if Q is also high. An extreme example is a bandpass filter having unity gain, a Q of 20, and f_{CLK}/f_O = 250 with pin 12 tied to ground (100:1 nominal). R4/R2 will therefore be equal to 6.25 and the offset voltage at the lowpass output will be about +1V. Where necessary, the offset voltage can be adjusted by using the circuit of Figure 36. This allows adjustment of V_{OS1}, which will have varying effects on the different outputs as described in the above equations. Some outputs cannot be adjusted this way in some modes, however ($V_{OS(BP)}$ in modes 1a and 3, for example).

SAMPLED DATA SYSTEM CONSIDERATIONS

The MF10-N is a sampled data filter, and as such, differs in many ways from conventional continuous-time filters. An important characteristic of sampled-data systems is their effect on signals at frequencies greater than one-half the sampling frequency. (The MF10-N's sampling frequency is the same as its clock frequency.) If a signal with a frequency greater than one-half the sampling frequency is applied to the input of a sampled data system, it will be “reflected” to a frequency less than one-half the sampling frequency. Thus, an input signal whose frequency is $f_s/2$ + 100 Hz will cause the system to respond as though the input frequency was $f_s/2$ − 100 Hz. This phenomenon is known as “aliasing”, and can be reduced or eliminated by limiting the input signal spectrum to less than $f_s/2$. This may in some cases require the use of a bandwidth-limiting filter ahead of the MF10-N to limit the input spectrum. However, since the clock frequency is much higher than the center frequency, this will often not be necessary.

Another characteristic of sampled-data circuits is that the output signal changes amplitude once every sampling period, resulting in “steps” in the output voltage which occur at the clock rate (Figure 37). If necessary, these can be “smoothed” with a simple R–C low-pass filter at the MF10-N output.

The ratio of f_{CLK} to f_C (normally either 50:1 or 100:1) will also affect performance. A ratio of 100:1 will reduce any aliasing problems and is usually recommended for wideband input signals. In noise sensitive applications, however, a ratio of 50:1 may be better as it will result in 3 dB lower output noise. The 50:1 ratio also results in lower DC offset voltages, as discussed in OFFSET VOLTAGE.

The accuracy of the f_{CLK}/f_O ratio is dependent on the value of Q. This is illustrated in Typical Performance Characteristics. As Q is changed, the true value of the ratio changes as well. Unless the Q is low, the error in f_{CLK}/f_O will be small. If the error is too large for a specific application, use a mode that allows adjustment of the ratio with external resistors.

It should also be noted that the product of Q and f_O should be limited to 300 kHz when f_O < 5 kHz, and to 200 kHz for f_O > 5 kHz.

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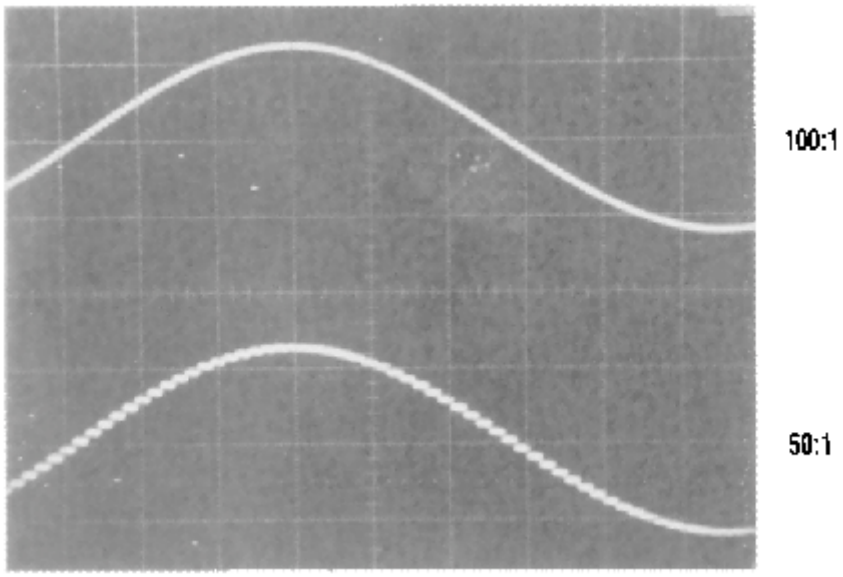

Figure 37. The Sampled-Data Output Waveform

Connection Diagram

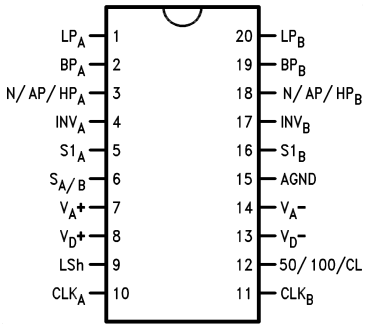

Figure 38. SOIC and PDIP Packages (Top View)
See Package Numbers DW and NFH0020A

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REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	27

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MF100CCM	NRND	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70	MF10CCWM	
MF100CCWM	NRND	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70	MF10CCWM	
MF10CCN	NRND	PDIP	NFH	20	18	TBD	Call TI	Call TI	0 to 70	MF10CCN	
MF10CCN/NOPB	ACTIVE	PDIP	NFH	20	18	Pb-Free (RoHS)	CU SN	Level-1-NA-UNLIM	0 to 70	MF10CCN	Samples
MF10CCWM/NOPB	ACTIVE	SOIC	DW	20	36	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 70	MF10CCWM	Samples
MF10CCWMX	NRND	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70	MF10CCWM	
MF10CCWMX/NOPB	ACTIVE	SOIC	DW	20	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 70	MF10CCWM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

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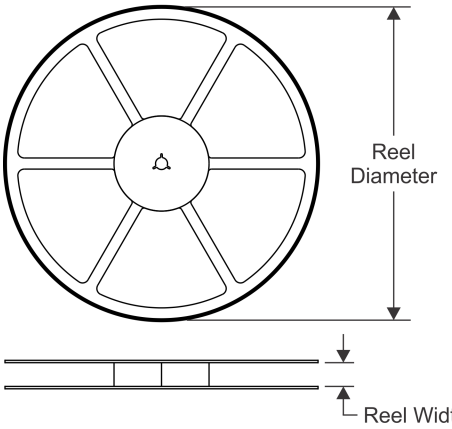
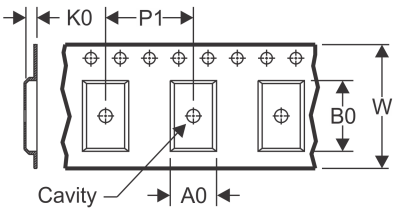
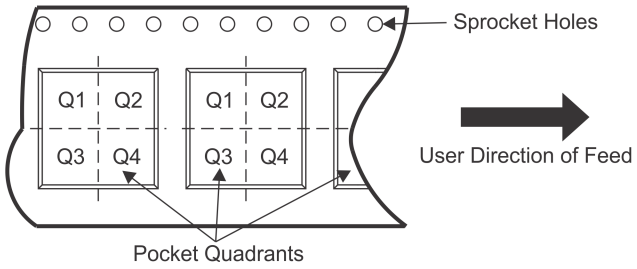


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

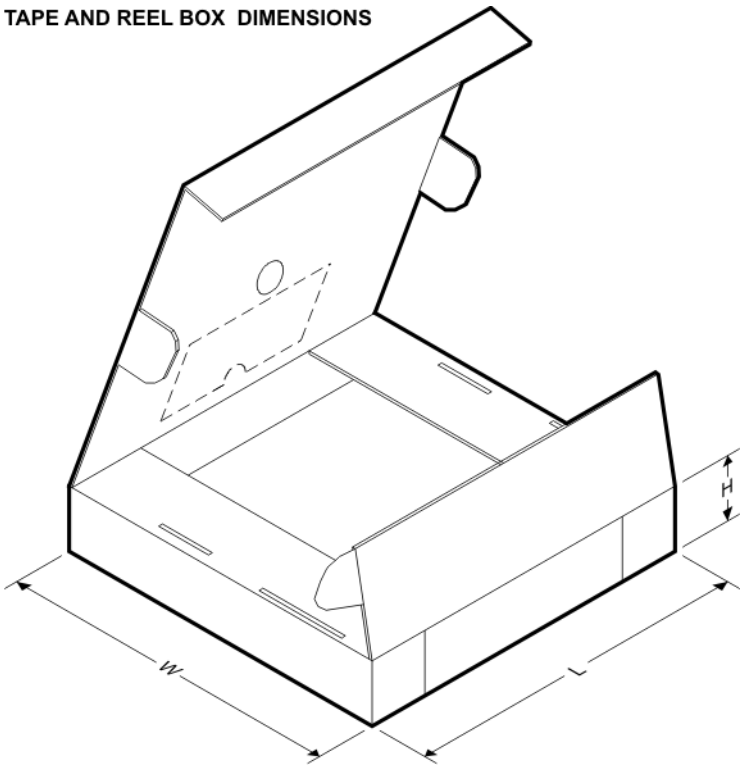
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MF10CCWMX/NOPB	SOIC	DW	20	1000	330.0	24.4	10.9	13.3	3.25	12.0	24.0	Q1

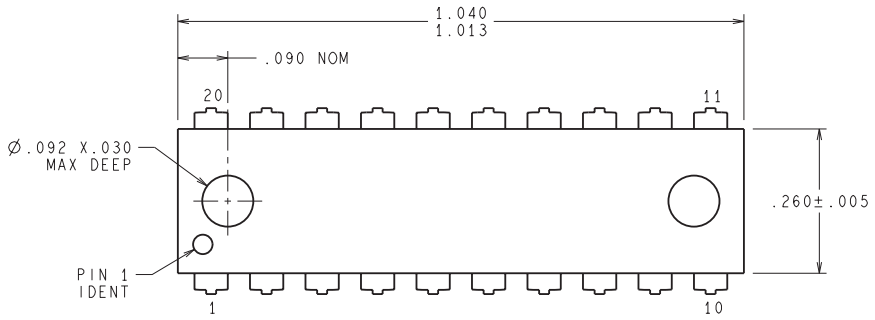
TAPE AND REEL BOX DIMENSIONS



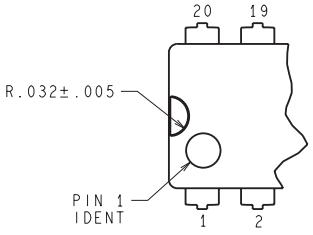
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MF10CCWMX/NOPB	SOIC	DW	20	1000	367.0	367.0	45.0

N0020A



OPTION 1



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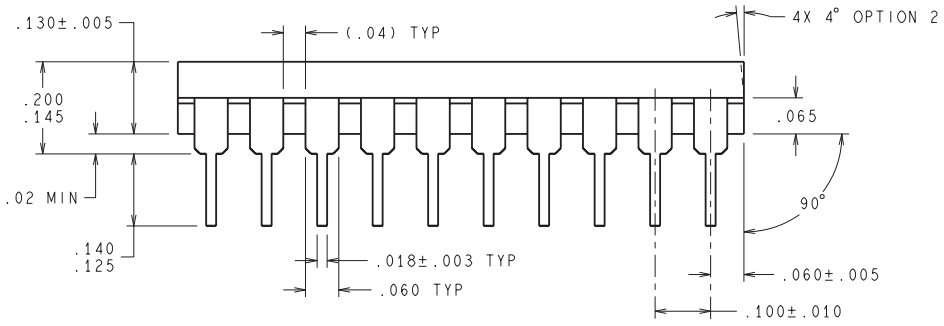
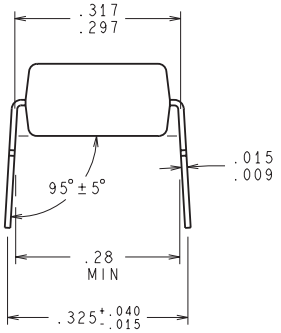
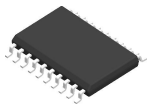




N20A (Rev G)

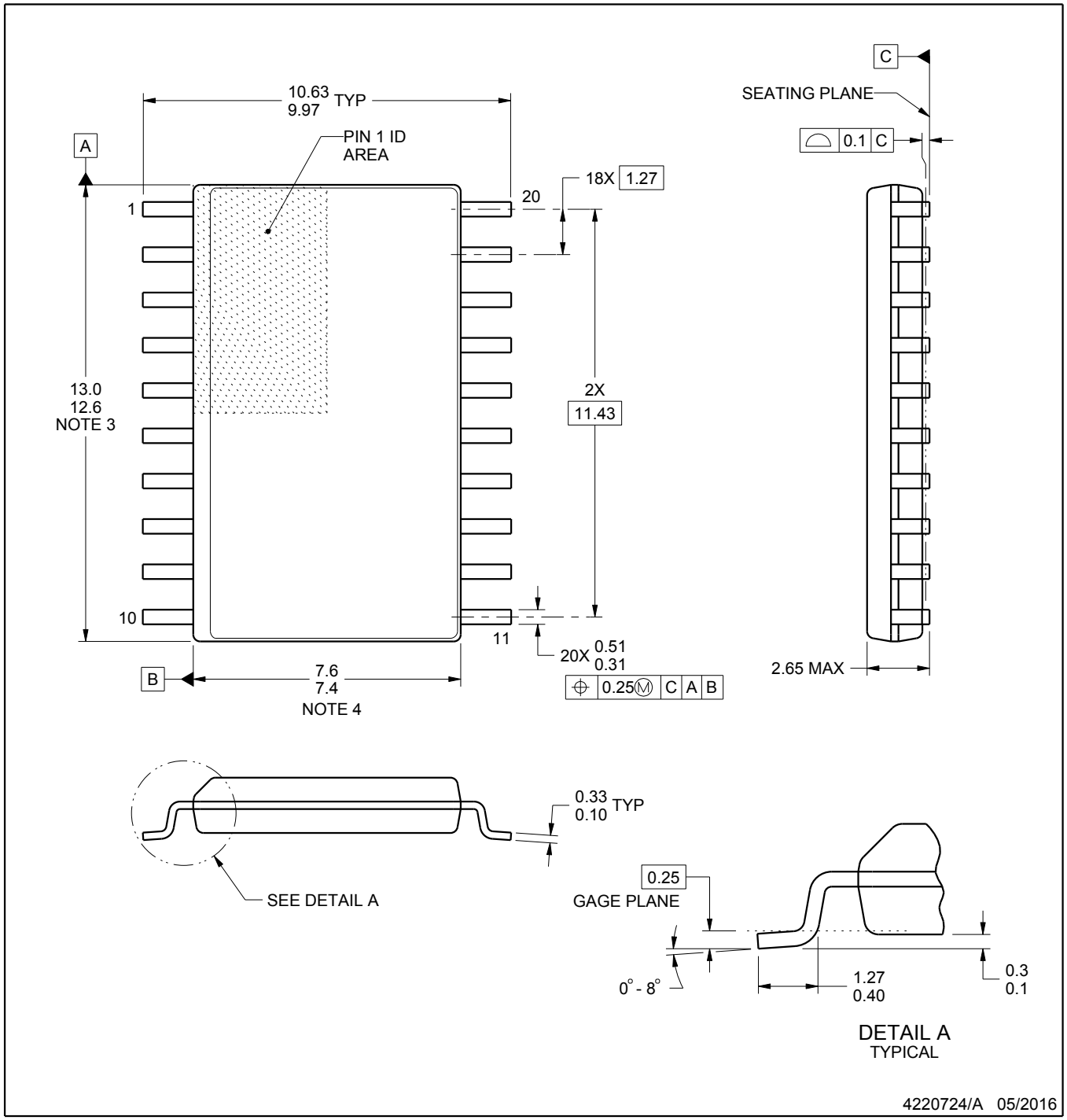


PACKAGE OUTLINE

DW0020A

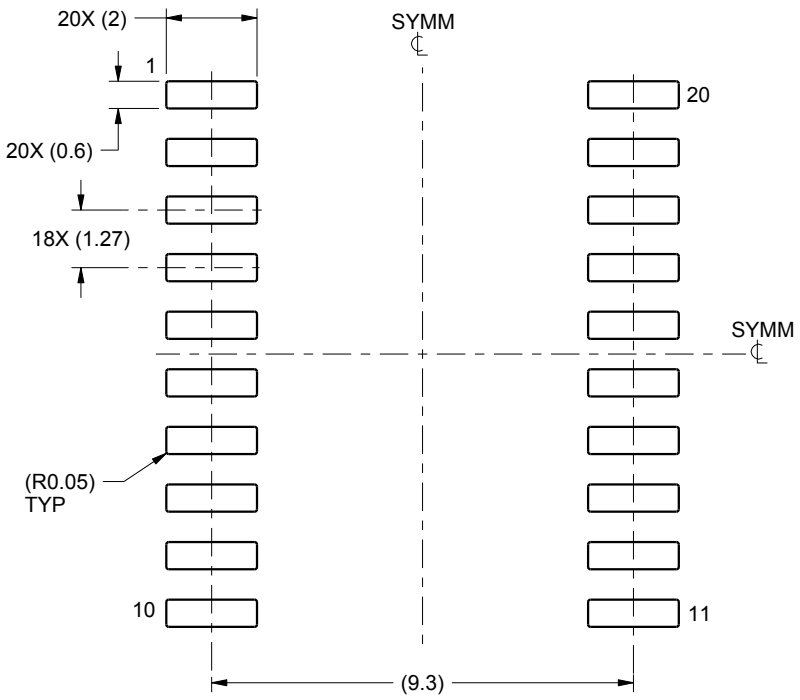
SOIC - 2.65 mm max height

SOIC



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
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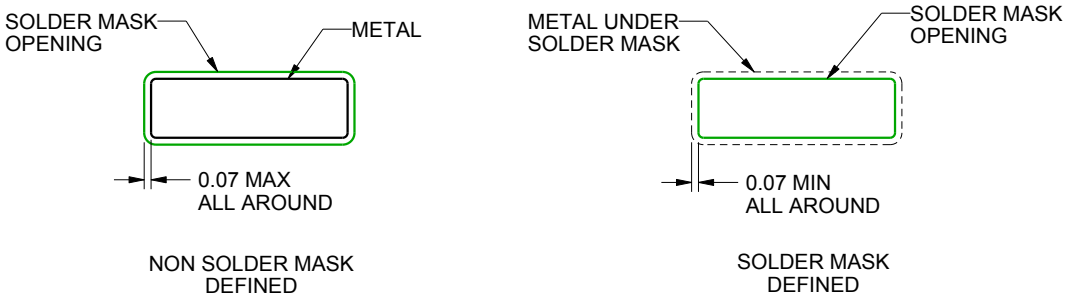
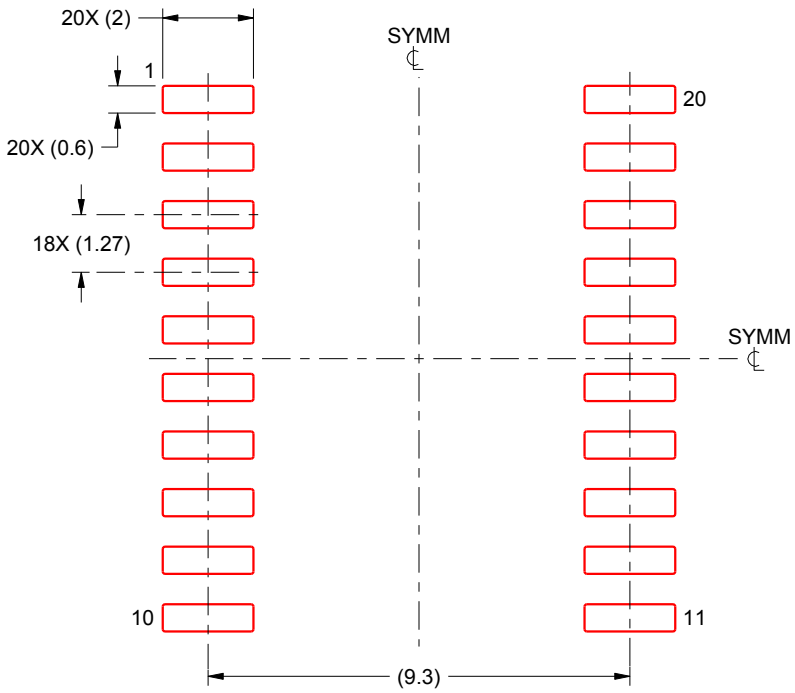


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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