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MC9S12H256VPV

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MC9S12H256
Device User Guide
V01.20
Covers also MC9S12H128

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Freescale Semiconductor Inc.

Revision History

Version Number	Revision Date	Effective Date	Author	Description of Changes
V01.00	07 MAR 2001	03 APR 2001		Initial version.
V01.01	10 MAI 2001	10 MAY 2001		- Minor formal corrections - Changed ATD coupling ratio to10^{-2} - Changed V_{DD5} to 4.5V
V01.02	14 MAY 2001	14 MAY 2001		- Removed 112-pin package references - Changed ATD Electrical Characteristics separate coupling ratio for positive and negative bulk current injection
V01.03	30 MAY 2001	30 MAY 2001		- Reinserted 112-pin package information.
V01.04	11 JUN 2001	11 JUN 2001		- Removed SRSv2 comment from preface - Corrected RESET pin to active low in table 2-1
V01.05	18 JUN 2001	18 JUN 2001		- Adapted style and wording to 9DP256 device user guide - Minor format and wording improvements - Added SRAM data retention disclaimer
V01.06	28 JUN 2001	28 JUN 2001		- Changed Oscillator Characteristics t_{CQOUT} max 2.5s and replaced Clock Monitor Time-out by Clock Monitor Failure Assert Frequency - Changed Self Clock Mode Frequency min 1MHz and max 5.5MHz - Changed I_{DDPS} (RTI and COP disabled) to 400µA - Corrected typo in Figure 2-1 pin 76: PK3 -> PK2
V01.07	12 JUL 2001	12 JUL 2001		- Added t_{EXTR} and t_{EXTF} to Oscillator Characteristics - Added typ value for t_{UPOSC} - Corrected t_{EXTL} and t_{EXTH} values - Updated thermal resistances as per Thermal Simulation Report, July 10, 2001
V01.08	16 JUL 2001	16 JUL 2001		- updated EEPROM size - added DC cutoff capacitor into layout proposals
V01.09	03 AUG 2001	03 AUG 2001		- minor updates
V01.10	29 AUG 2001	29 AUG 2001		- updated electrical spec

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Version Number	Revision Date	Effective Date	Author	Description of Changes
V01.11	11 OCT 2001	11 OCT 2001		- Replaced references w.r.t. new family name HCS12. - Corrected XCLKS reference in CRG electrical spec.
V01.12	07 NOV 2001	07 NOV 2001		- added ‘powered by’ column in pin list table
V01.13	08 MAR 2002	08 MAR 2002		- new document numbering - removed document order number except from cover sheet - updated min VDD, VDDPLL - updated currents on V_{OH},V_{OL} for standard pins - updated C_{IN}, I_{DDS}, I_{REF}, C_{INS}, T_{EXTL}, T_{EXTH} - included missing lcd electrical spec - updated NVM spec
V01.14	16 DEC 2002	16 DEC 2002		- updated input leakage - updated slew rate spec on PU,PV, PW - updated supply currents - included 1K78X - added detailed register map
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V01.17	04 AUG 2004	04 AUG 2004		- added MC9S12H128
V01.18	13 AUG 2004	13 AUG 2004		- added Internal Pull Resistor columns to signal properties table
V01.19	05 NOV 2004	05 NOV 2004		- changed SPI0 to SPI, ATD0 to ATD
V01.20	28 JUL 2008	28 JUL 2008		- changed PU,PV,PW rise/fall times in EPP package at cold.

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Preface

The Device User Guide provides information about the MC9S12H256 and MC9S12H128 device made up of standard HCS12 blocks and the HCS12 processor core.

This document is part of the customer documentation. A complete set of device manuals also includes the HCS12 Core User Guide and all the individual Block User Guides of the implemented modules. In an effort to reduce redundancy all module specific information is located only in the respective Block User Guide. If applicable, special implementation details of the module are given in the block description sections of this document.

See **Table 0-1** for names and versions of the referenced documents throughout the Device User Guide.

Table 0-1 Document References

User Guide	Version	Document Order Number
HCS12 V1.5 Core User Guide	1.2	HCS12COREUG
CRG Block User Guide	V02	S12CRGV2/D
TIM_16B8C Block User Guide	V01	S12TIM16B8CV1/D
ATD_10B16C Block User Guide	V02	S12ATD10B16CV2/D
IIC Block User Guide	V02	S12IICV2/D
SCI Block User Guide	V02	S12SCIV2/D
SPI Block User Guide	V02	S12SPIV2/D
PWM_8B6C Block User Guide	V01	S12PWM8B6CV1/D
FTS256K Block User Guide	V02	S12FTS256KV2/D
EETS4K Block User Guide	V02	S12EETS4KV2/D
LCD_32F4B Block User Guide	V01	S12LCD32F4BV1/D
MSCAN Block User Guide	V02	S12MSCANV2/D
MC_10B12C Block User Guide	V02	S12MC10B12CV2/D
PIM_9H256 Block User Guide	V01	S12PIMH256V1/D
VREG Block User Guide	V01	S12VREGV1/D

Section 1 Introduction

1.1 Overview

The MC9S12H256 microcontroller unit (MCU) is a 16-bit device composed of standard on-chip peripherals including a 16-bit central processing unit (HCS12 CPU), 256K bytes of Flash EEPROM, 12K bytes of RAM, 4K bytes of EEPROM, two asynchronous serial communications interfaces (SCI), a serial peripheral interface (SPI), an IIC-bus interface (IIC), an 8-channel 16-bit timer (TIM), a 16-channel, 10-bit analog-to-digital converter (ATD), a six-channel pulse width modulator (PWM), and two CAN 2.0 A, B software compatible modules (MSCAN).

The MC9S12H128 microcontroller unit (MCU) is a 16-bit device composed of standard on-chip peripherals including a 16-bit central processing unit (HCS12 CPU), 128K bytes of Flash EEPROM, 6K bytes of RAM, 2K bytes of EEPROM, one asynchronous serial communications interface (SCI), a serial peripheral interface (SPI), an IIC-bus interface (IIC), an 8-channel 16-bit timer (TIM), a 8-channel, 10-bit analog-to-digital converter (ATD), a two-channel pulse width modulator (PWM), and two CAN 2.0 A, B software compatible modules (MSCAN).

In addition, it features a 32x4 liquid crystal display (LCD) controller/driver and a motor pulse width modulator (MC) consisting of 24 high current outputs suited to drive up to 6 stepper motors. System resource mapping, clock generation, interrupt control, and bus interfacing are managed by the HCS12 Core.

The MC9S12H256 has full 16-bit data paths throughout. The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements. In addition to the I/O ports available in each module, 12 general purpose I/O pins are available with interrupt and wake-up capability from STOP or WAIT mode.

1.2 Features

- HCS12 Core
  - 16-bit HCS12 CPU
    i. Upward compatible with M68HC11 instruction set
    ii. Interrupt stacking and programmer’s model identical to M68HC11
    iii. 20-bit ALU
    iv. Instruction queue
    v. Enhanced indexed addressing
  - MEBI (Multiplexed External Bus Interface)
  - MMC (Module Mapping Control)
  - INT (Interrupt control)
  - BKP (Breakpoints)

  - BDM (Background Debug Mode)
- CRG (low current oscillator, PLL, reset, clocks, COP watchdog, real time interrupt, clock monitor)
- 8-bit and 4-bit ports with interrupt functionality
  - Digital filtering
  - Programmable rising or falling edge trigger
- Memory
  - 128K, 256K Flash EEPROM
  - 2K, 4K byte EEPROM
  - 6K, 12K byte RAM
- Analog-to-Digital Converter
  - 8, 16 channels, 10-bit resolution
  - External conversion trigger capability
- Two 1M bit per second, CAN 2.0 A, B software compatible modules
  - Five receive and three transmit buffers
  - Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit or 8 x 8 bit
  - Four separate interrupt channels for Rx, Tx, error and wake-up
  - Low-pass filter wake-up function
  - Loop-back for self test operation
- Timer
  - 16-bit main counter with 7-bit prescaler
  - 8 programmable input capture or output compare channels
  - Two 8-bit or one 16-bit pulse accumulators
- 2, 6 PWM channels
  - Programmable period and duty cycle
  - 8-bit 2, 6-channel or 16-bit 1, 3-channel
  - Separate control for each pulse width and duty cycle
  - Center-aligned or left-aligned outputs
  - Programmable clock select logic with a wide range of frequencies
  - Fast emergency shutdown input
- Serial interfaces
  - Two asynchronous Serial Communications Interfaces (SCI)
  - Synchronous Serial Peripheral Interface (SPI)

  - Inter-Integrated Circuit interface (IIC)
- Liquid Crystal Display driver with variable input voltage
  - Configurable for up to 32 frontplanes and 4 backplanes or general purpose input or output
  - 5 modes of operation allow for different display sizes to meet application requirements
  - Unused frontplane and backplane pins can be used as general purpose I/O
- 16, 24 high current drivers suited for PWM motor control
  - Each PWM channel switchable between two drivers in an H-bridge configuration
  - Left, right and center aligned outputs
  - Support for sine and cosine drive
  - Dithering
  - Output slew rate control
- 144-Pin or 112-Pin LQFP package
  - I/O lines with 5V input and drive capability
  - 5V A/D converter inputs
  - Operation at 32MHz equivalent to 16MHz Bus Speed
  - Development support
  - Single-wire background debug™ mode (BDM)
  - On-chip hardware breakpoints

1.3 Modes of Operation

User modes

- Normal and Emulation Operating Modes
  - Normal Single-Chip Mode
  - Normal Expanded Wide Mode
  - Normal Expanded Narrow Mode
  - Emulation Expanded Wide Mode
  - Emulation Expanded Narrow Mode
- Special Operating Modes
  - Special Single-Chip Mode with active Background Debug Mode
  - Special Test Mode (**Freescale Use Only**)
  - Special Peripheral Mode (**Freescale Use Only**)

Low power modes

- Stop Mode
- Pseudo Stop Mode
- Wait Mode

1.4 Block Diagram

Figure 1-1 is a block diagram of the MC9S12H256 device.

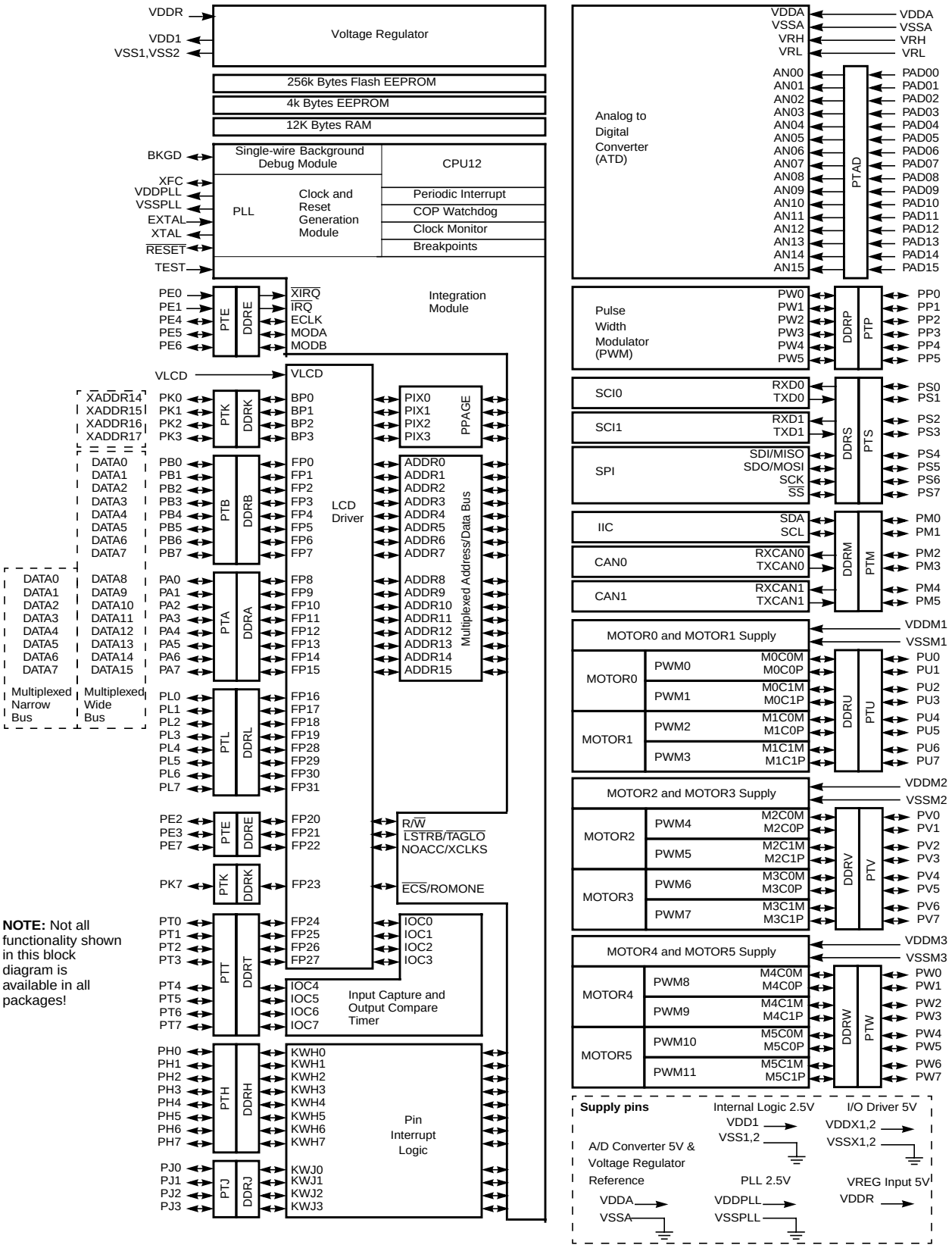


Figure 1-1 MC9S12H256 Block Diagram

Figure 1-2 is a block diagram of the MC9S12H128 device.

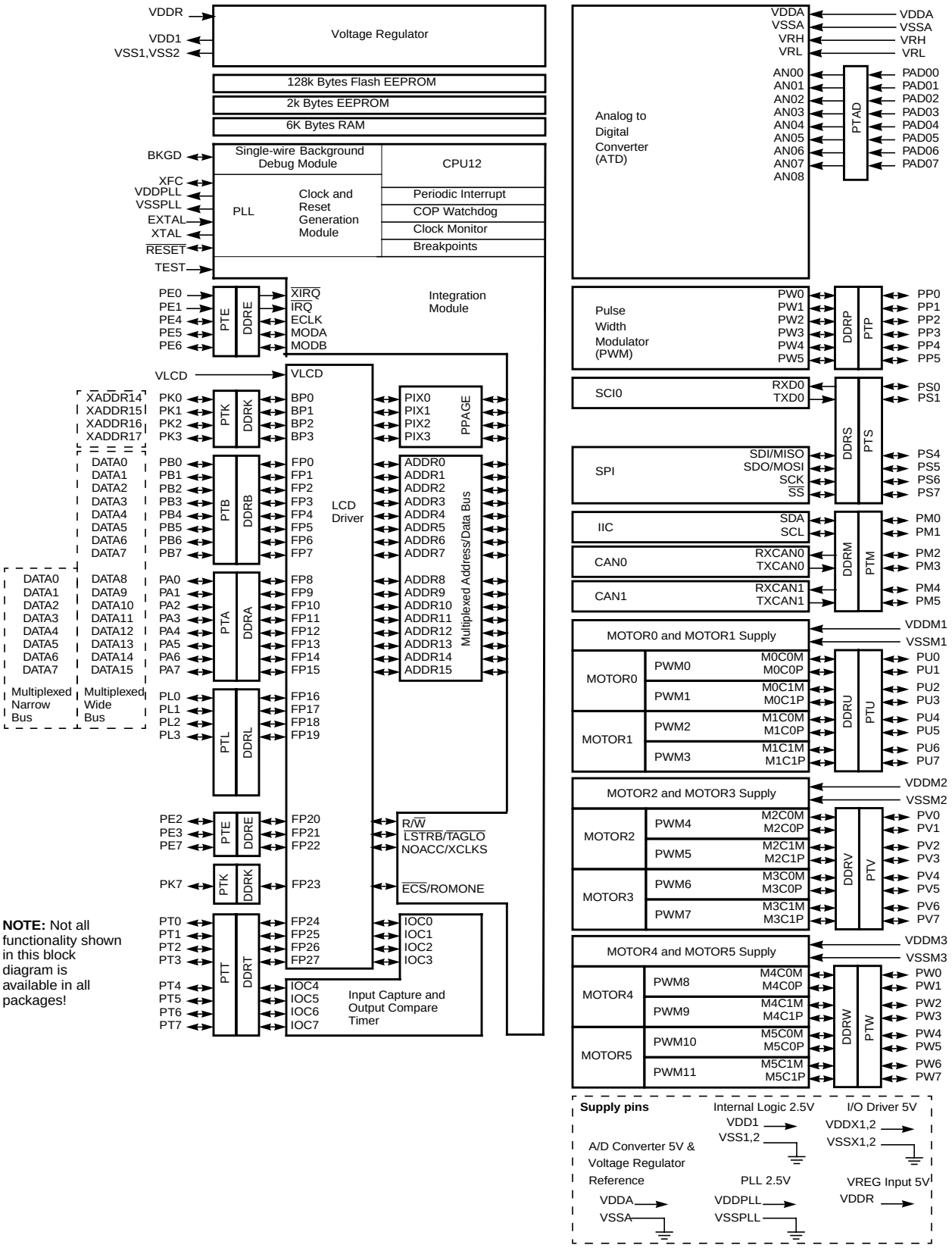


Figure 1-2 MC9S12H128 Block Diagram

1.5 Device Memory Map

Table 1-1 and **Figure 1-3** show the device memory map of the MC9S12H256.

Table 1-1 Device Memory Map MC9S12H256

Address	Module	Size (Bytes)
$0000 – $0017	CORE (Ports A, B, E, Modes, Inits, Test)	24
$0018 – $0019	Reserved	2
$001A – $001B	Device ID register (PARTID)	2
$001C – $001F	CORE (MEMSIZ, IRQ, HPRIO)	4
$0020 – $0027	Reserved	8
$0028 – $002F	CORE (Background Debug Mode)	8
$0030 – $0033	CORE (PPAGE, Port K)	4
$0034 – $003F	Clock and Reset Generator (PLL, RTI, COP)	12
$0040 – $006F	Standard Timer Module 16-bit 8 channels (TIM)	48
$0070 – $007F	Reserved	16
$0080 – $00AF	Analog to Digital Converter 10-bit 16 channels (ATD)	48
$00B0 – $00BF	Reserved	16
$00C0 – $00C7	Inter Integrated Circuit (IIC)	8
$00C8 – $00CF	Serial Communications Interface 0 (SCI0)	8
$00D0 – $00D7	Serial Communications Interface 1 (SCI1)	8
$00D8 – $00DF	Serial Peripheral Interface (SPI)	8
$00E0 – $00FF	Pulse Width Modulator 8-bit 6 channels (PWM)	32
$0100 – $010F	Flash control registers	16
$0110 – $011B	EEPROM control registers	12
$011C – $011F	Reserved	4
$0120 – $0137	Liquid Crystal Display Driver 32x4 (LCD)	24
$0140 – $017F	Freescale Scalable Controller Area Network 0 (MSCAN0)	64
$0180 – $01BF	Freescale Scalable Controller Area Network 1 (MSCAN1)	64
$01C0 – $01FF	Motor Control Module (MC)	64
$0200 – $027F	Port Integration Module (PIM)	128
$0280 – $03FF	Reserved	384
$0000 – $0FFF	EEPROM array	4096
$1000 – $3FFF	RAM array	12288
$4000 – $7FFF	Fixed Flash EEPROM array incl. 0.5K, 1K, 2K or 4K Protected Sector at start	16384
$8000 – $BFFF	Flash EEPROM Page Window	16384
$C000 – $FFFF	Fixed Flash EEPROM array incl. 0.5K, 1K, 2K or 4K Protected Sector at end and 256 bytes of Vector Space at $FF80 – $FFFF	16384

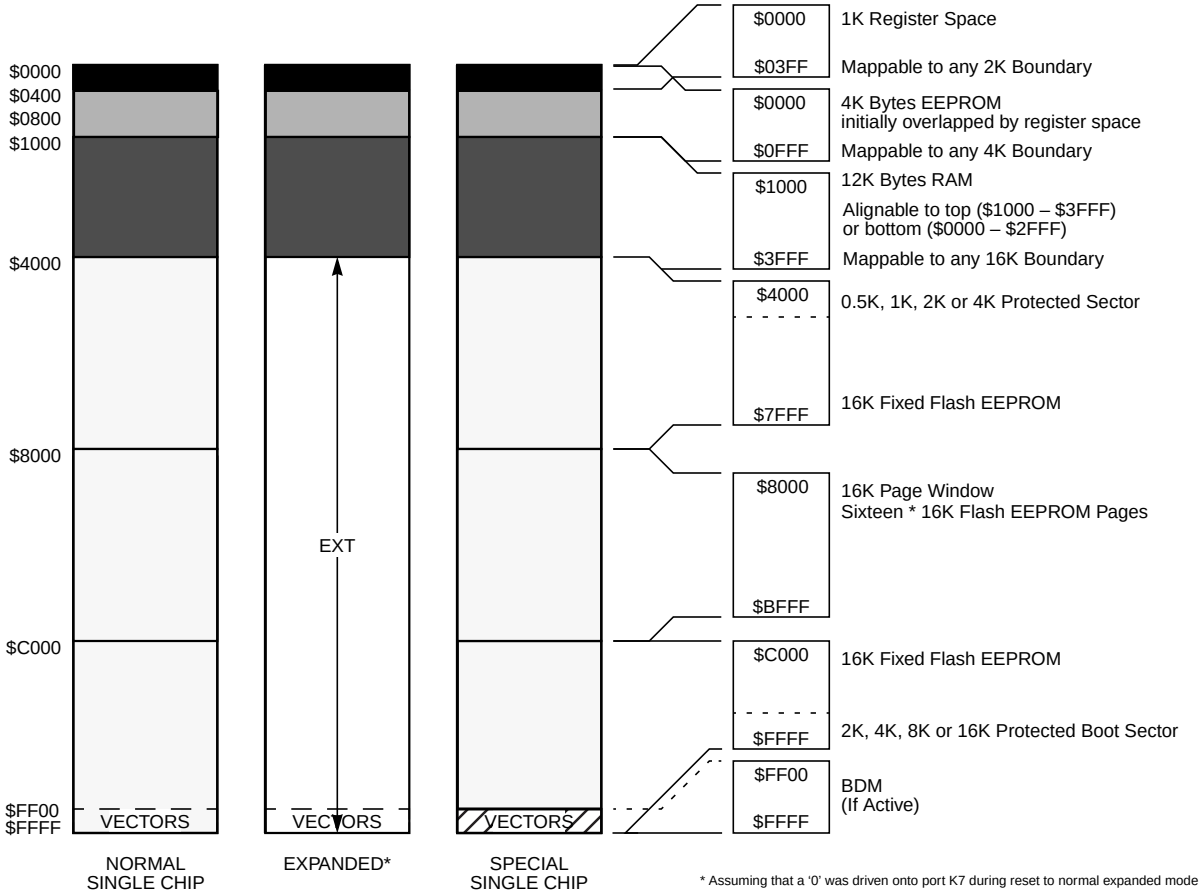


Figure 1-3 MC9S12H256 Memory Map

Table 1-2 and **Figure 1-4** show the device memory map of the MC9S12H128.

Table 1-2 Device Memory Map MC9S12H128

Address	Module	Size (Bytes)
$0000 – $0017	CORE (Ports A, B, E, Modes, Inits, Test)	24
$0018 – $0019	Reserved	2
$001A – $001B	Device ID register (PARTID)	2
$001C – $001F	CORE (MEMSIZ, IRQ, HPRIO)	4
$0020 – $0027	Reserved	8
$0028 – $002F	CORE (Background Debug Mode)	8
$0030 – $0033	CORE (PPAGE, Port K)	4
$0034 – $003F	Clock and Reset Generator (PLL, RTI, COP)	12
$0040 – $006F	Standard Timer Module 16-bit 8 channels (TIM)	48
$0070 – $007F	Reserved	16
$0080 – $00AF	Analog to Digital Converter 10-bit 16 channels (ATD)	48
$00B0 – $00BF	Reserved	16
$00C0 – $00C7	Inter Integrated Circuit (IIC)	8

Table 1-2 Device Memory Map MC9S12H128

Address	Module	Size (Bytes)
$00C8 – $00CF	Serial Communications Interface 0 (SCI0)	8
$00D0 – $00D7	Reserved	8
$00D8 – $00DF	Serial Peripheral Interface (SPI)	8
$00E0 – $00FF	Pulse Width Modulator 8-bit 6 channels (PWM)	32
$0100 – $010F	Flash control registers	16
$0110 – $011B	EEPROM control registers	12
$011C – $011F	Reserved	4
$0120 – $0137	Liquid Crystal Display Driver 32x4 (LCD)	24
$0140 – $017F	Freescale Scalable Controller Area Network 0 (MSCAN0)	64
$0180 – $01BF	Freescale Scalable Controller Area Network 1 (MSCAN1)	64
$01C0 – $01FF	Motor Control Module (MC)	64
$0200 – $027F	Port Integration Module (PIM)	128
$0280 – $03FF	Reserved	384
$0000 – $07FF	EEPROM array	2048
$1000 – $3FFF	RAM array	12288
$4000 – $7FFF	Fixed Flash EEPROM array incl. 0.5K, 1K, 2K or 4K Protected Sector at start	16384
$8000 – $BFFF	Flash EEPROM Page Window	16384
$C000 – $FFFF	Fixed Flash EEPROM array incl. 0.5K, 1K, 2K or 4K Protected Sector at end and 256 bytes of Vector Space at $FF80 – $FFFF	16384

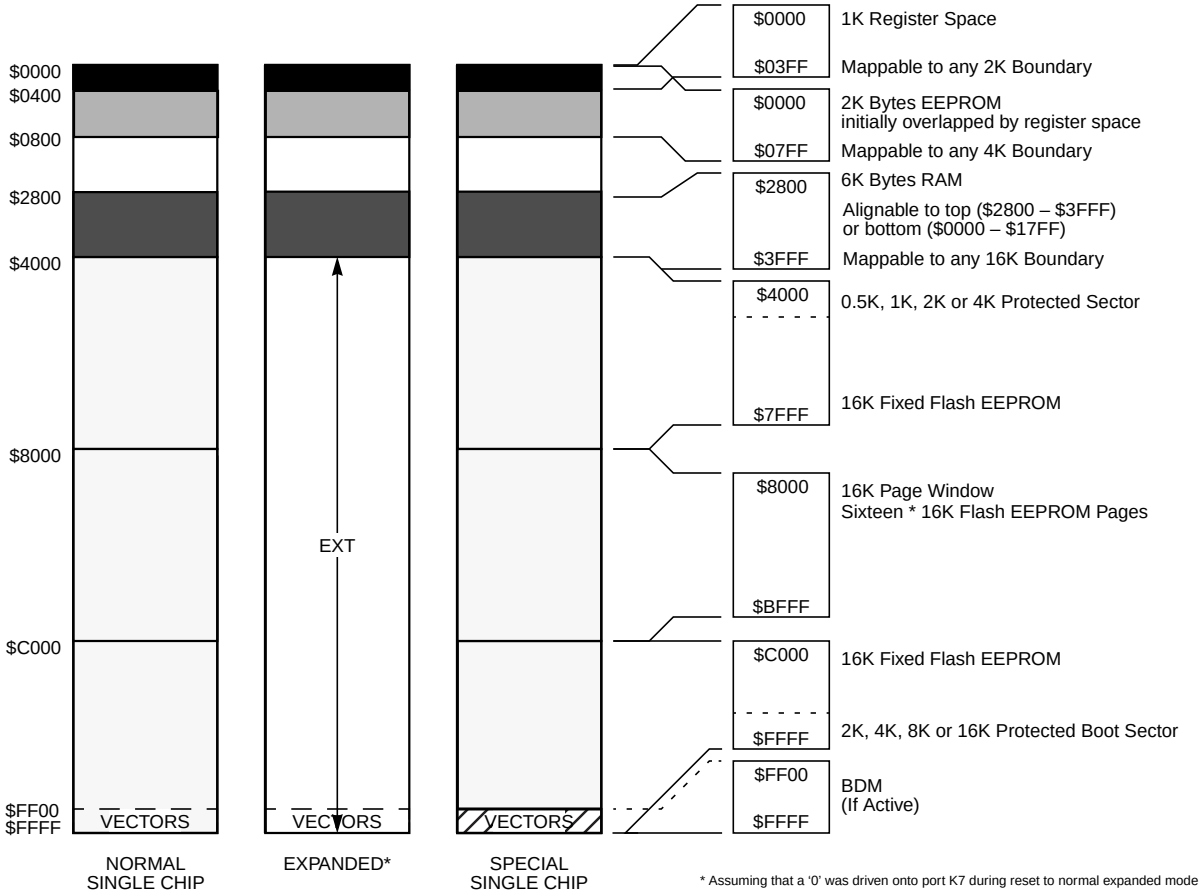


Figure 1-4 MC9S12H128 Memory Map

1.5.1 Detailed Register Map

$0000 - $000F MEBI map 1 of 3 (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0000	PORTA	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0001	PORTB	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0002	DDRA	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0003	DDRB	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0004	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0005	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0006	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0007	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0008	PORTE	Read: Write:	Bit 7	6	5	4	3	2	Bit 1	Bit 0
$0009	DDRE	Read: Write:	Bit 7	6	5	4	3	Bit 2	0	0
$000A	PEAR	Read:	NOACCE	0	PIPOE	NECLK	LSTRE	RDWE	0	0
		Write:								
$000B	MODE	Read: Write:	MODC	MODB	MODA	0	IVIS	0	EMK	EME
$000C	PUCR	Read: Write:	PUPKE	0	0	PUPEE	0	0	PUPBE	PUPAE
$000D	RDRIV	Read: Write:	RDPK	0	0	RDPE	0	0	RDPB	RDPA
$000E	EBICTL	Read:	0	0	0	0	0	0	0	ESTR
		Write:								
$000F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0010 - $0014 MMC map 1 of 4 (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0010	INITRM	Read: Write:	RAM15	RAM14	RAM13	RAM12	RAM11	0	0	RAMHAL
$0011	INITRG	Read:	0	REG14	REG13	REG12	REG11	0	0	0
		Write:								
$0012	INITEE	Read: Write:	EE15	EE14	EE13	EE12	0	0	0	EEON
$0013	MISC	Read:	0	0	0	0	EXSTR1	EXSTR0	ROMHM	ROMON
		Write:								
$0014	MTST0 Test Only	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

$0015 - $0016 INT map 1 of 2 (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0015	ITCR	Read:	0	0	0	WRINT	ADR3	ADR2	ADR1	ADR0
		Write:								
$0016	ITEST	Read: Write:	INTE	INTC	INTA	INT8	INT6	INT4	INT2	INT0

$0017 - $0017 MMC map 2 of 4 (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0017	MTST1 Test Only	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

$0018 - $001B Miscellaneous Peripherals (Device User Guide, Table 1-5)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0018	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0019	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$001A	PARTIDH	Read:	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8
		Write:								
$001B	PARTIDL	Read:	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
		Write:								

$001C - $001D MMC map 3 of 4 (Core and Device User Guide, Table 1-6)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$001C	MEMSIZ0	Read:	reg_sw0	0	eep_sw1	eep_sw0	0	ram_sw2	ram_sw1	ram_sw0
		Write:								
$001D	MEMSIZ1	Read:	rom_sw1	rom_sw0	0	0	0	0	pag_sw1	pag_sw0
		Write:								

$001E - $001E MEBI map 2 of 3 (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$001E	INTCR	Read:	IRQE	IRQEN	0	0	0	0	0	0
		Write:								

$001F - $001F INT map 2 of 2 (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$001F	HPRIO	Read:	PSEL7	PSEL6	PSEL5	PSEL4	PSEL3	PSEL2	PSEL1	0
		Write:								

$0020 - $0027 Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0020 - $0027	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0028 - $002F BKP (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0028	BKPCT0	Read:	BKEN	BKFULL	BKBDM	BKTAG	0	0	0	0
		Write:								
$0029	BKPCT1	Read:	BK0MBH	BK0MBL	BK1MBH	BK1MBL	BK0RWE	BK0RW	BK1RWE	BK1RW
		Write:								
$002A	BKP0X	Read:	0	0	BK0V5	BK0V4	BK0V3	BK0V2	BK0V1	BK0V0
		Write:								
$002B	BKP0H	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$002C	BKP0L	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$002D	BKP1X	Read:	0	0	BK1V5	BK1V4	BK1V3	BK1V2	BK1V1	BK1V0
		Write:								
$002E	BKP1H	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$002F	BKP1L	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

$0030 - $0031 MMC map 4 of 4 (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0030	PPAGE	Read:	0	0	PIX5	PIX4	PIX3	PIX2	PIX1	PIX0
		Write:								
$0031	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0032 - $0033 MEBI map 3 of 3 (Core User Guide)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0032	PORTK	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0033	DDRK	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								

$0034 - $003F CRG (Clock and Reset Generator)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0034	SYNR	Read:	0	0	SYN5	SYN4	SYN3	SYN2	SYN1	SYN0
		Write:								
$0035	REFDV	Read:	0	0	0	0	REFDV3	REFDV2	REFDV1	REFDV0
		Write:								
$0036	CTFLG TEST ONLY	Read:	0	0	0	0	0	0	0	0
		Write:								
$0037	CRGFLG	Read:	RTIF	PORF	0	LOCKIF	LOCK	TRACK	SCMIF	SCM
		Write:								
$0038	CRGINT	Read:	RTIE	0	0	LOCKIE	0	0	SCMIE	0
		Write:								
$0039	CLKSEL	Read:	PLLSEL	PSTP	SYSWAI	ROAWAI	PLLWAI	CWAI	RTIWAI	COPWAI
		Write:								
$003A	PLLCTL	Read:	CME	PLLON	AUTO	ACQ	0	PRE	PCE	SCME
		Write:								
$003B	RTICTL	Read:	0	RTR6	RTR5	RTR4	RTR3	RTR2	RTR1	RTR0
		Write:								
$003C	COPCTL	Read:	WCOP	RSBCK	0	0	0	CR2	CR1	CR0
		Write:								
$003D	FORBYP TEST ONLY	Read:	0	0	0	0	0	0	0	0
		Write:								
$003E	CTCTL TEST ONLY	Read:	0	0	0	0	0	0	0	0
		Write:								
$003F	ARMCOP	Read:	0	0	0	0	0	0	0	0
		Write:	Bit 7	6	5	4	3	2	1	Bit 0

$0040 - $006F TIM (Timer 16 Bit 8 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0040	TIOS	Read:	IOS7	IOS6	IOS5	IOS4	IOS3	IOS2	IOS1	IOS0
		Write:								
$0041	CFORC	Read:	0	0	0	0	0	0	0	0
		Write:	FOC7	FOC6	FOC5	FOC4	FOC3	FOC2	FOC1	FOC0
$0042	OC7M	Read:	OC7M7	OC7M6	OC7M5	OC7M4	OC7M3	OC7M2	OC7M1	OC7M0
		Write:								
$0043	OC7D	Read:	OC7D7	OC7D6	OC7D5	OC7D4	OC7D3	OC7D2	OC7D1	OC7D0
		Write:								
$0044	TCNT (hi)	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$0045	TCNT (lo)	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$0046	TSCR1	Read:	TEN	TSWAI	TSFRZ	TFFCA	0	0	0	0
		Write:								
$0047	TTOV	Read:	TOV7	TOV6	TOV5	TOV4	TOV3	TOV2	TOV1	TOV0
		Write:								
$0048	TCTL1	Read:	OM7	OL7	OM6	OL6	OM5	OL5	OM4	OL4
		Write:								
$0049	TCTL2	Read:	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0
		Write:								

$0040 - $006F TIM (Timer 16 Bit 8 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$004A	TCTL3	Read: Write:	EDG7B	EDG7A	EDG6B	EDG6A	EDG5B	EDG5A	EDG4B	EDG4A
$004B	TCTL4	Read: Write:	EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG0A
$004C	TIE	Read: Write:	C7I	C6I	C5I	C4I	C3I	C2I	C1I	C0I
$004D	TSCR2	Read: Write:	TOI	0	0	0	TCRE	PR2	PR1	PR0
$004E	TFLG1	Read: Write:	C7F	C6F	C5F	C4F	C3F	C2F	C1F	C0F
$004F	TFLG2	Read: Write:	TOF	0	0	0	0	0	0	0
$0050	TC0 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$0051	TC0 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0052	TC1 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$0053	TC1 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0054	TC2 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$0055	TC2 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0056	TC3 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$0057	TC3 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0058	TC4 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$0059	TC4 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$005A	TC5 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$005B	TC5 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$005C	TC6 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$005D	TC6 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$005E	TC7 (hi)	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$005F	TC7 (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0060	PACTL	Read: Write:	0	PAEN	PAMOD	PEDGE	CLK1	CLK0	PAOVI	PAI
$0061	PAFLG	Read: Write:	0	0	0	0	0	0	PAOVF	PAIF
$0062	PACNT (hi)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0

$0040 - $006F TIM (Timer 16 Bit 8 Channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0063	PACNT (lo)	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$0064	Reserved	Read: Write:								
$0065	Reserved	Read: Write:								
$0066	Reserved	Read: Write:								
$0067	Reserved	Read: Write:								
$0068	Reserved	Read: Write:								
$0069	Reserved	Read: Write:								
$006A	Reserved	Read: Write:								
$006B	Reserved	Read: Write:								
$006C	Reserved	Read: Write:								
$006D	TIMTST Test Only	Read: Write:	0	0	0	0	0	0	TCBYP	PCBYP
$006E	Reserved	Read: Write:								
$006F	Reserved	Read: Write:								

$0070 - $007F Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0070 - $007F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0080 - $00AF ATD (Analog to Digital Converter 10 Bit 16 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0080	ATDCTL0	Read:	0	0	0	0	0	0	0	0
		Write:								
$0081	ATDCTL1	Read:	0	0	0	0	0	0	0	0
		Write:								
$0082	ATDCTL2	Read:	ADPU	AFFC	AWAI	ETRIGLE	ETRIGP	ETRIG	ASCIE	ASCIF
		Write:								
$0083	ATDCTL3	Read:	0	S8C	S4C	S2C	S1C	FIFO	FRZ1	FRZ0
		Write:								
$0084	ATDCTL4	Read:	SRES8	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0
		Write:								
$0085	ATDCTL5	Read:	DJM	DSGN	SCAN	MULT	CD	CC	CB	CA
		Write:								

$0080 - $00AF ATD (Analog to Digital Converter 10 Bit 16 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0086	ATDSTAT0	Read:	SCF	0	ETORF	FIFOR	CC3	CC2	CC1	CC0
		Write:								
$0087	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0088	ATDTEST0	Read:	SAR9	SAR8	SAR7	SAR6	SAR5	SAR4	SAR3	SAR2
		Write:								
$0089	ATDTEST1	Read:	SAR1	SAR0	0	0	0	RST	ATDCLK	SC
		Write:								
$008A	ATDSTAT2	Read:	CCF15	CCF14	CCF13	CCF12	CCF11	CCF10	CCF9	CCF8
		Write:								
$008B	ATDSTAT1	Read:	CCF7	CCF6	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
		Write:								
$008C	ATDDIEN0	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$008D	ATDDIEN1	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$008E	PORTAD0	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$008F	PORTAD1	Read:	Bit7	6	5	4	3	2	1	BIT 0
		Write:								
$0090	ATDDR0H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0091	ATDDR0L	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								
$0092	ATDDR1H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0093	ATDDR1L	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								
$0094	ATDDR2H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0095	ATDDR2L	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								
$0096	ATDDR3H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0097	ATDDR3L	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								
$0098	ATDDR4H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$0099	ATDDR4L	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								
$009A	ATDDR5H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$009B	ATDDR5L	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								
$009C	ATDDR6H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$009D	ATDDR6L	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								
$009E	ATDDR7H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								

$0080 - $00AF ATD (Analog to Digital Converter 10 Bit 16 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$009F	ATDDR7L	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								
$00A0	ATDDR8H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00A1	ATDDR8L	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								
$00A2	ATDDR9H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00A3	ATDDR9L	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								
$00A4	ATDDR10H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00A5	ATDDR10L	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								
$00A6	ATDDR11H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00A7	ATDDR11L	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								
$00A8	ATDDR12H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00A9	ATDDR12L	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								
$00AA	ATDDR13H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00AB	ATDDR13L	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								
$00AC	ATDDR14H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00AD	ATDDR14L	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								
$00aE	ATDDR15H	Read:	Bit15	14	13	12	11	10	9	Bit8
		Write:								
$00AF	ATDDR15L	Read:	Bit7	6	5	4	3	2	1	Bit0
		Write:								

$00B0 - $00BF Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00B0 - $00BF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$00C0 - $00C7 IIC (Inter IC Bus)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00C0	IBAD	Read: Write:	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	0
$00E1	IBFD	Read: Write:	IBC7	IBC6	IBC5	IBC4	IBC3	IBC2	IBC1	IBC0

$00C0 - $00C7 IIC (Inter IC Bus)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00C2	IBCR	Read:	IBEN	IBIE	MS/$\overline{SL}$	TX/$\overline{RX}$	TXAK	0	0	IBSWAI
		Write:						RSTA		
$00C3	IBSR	Read:	TCF	IAAS	IBB	IBAL	0	SRW	IBIF	RXAK
		Write:								
$00C4	IBDR	Read: Write:	D7	D6	D5	D4	D3	D2	D1	D 0
$00C5	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00C6	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00C7	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$00C8 - $00CF SCI0 (Asynchronous Serial Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00C8	SCI0BDH	Read:	0	0	0	SBR12	SBR11	SBR10	SBR9	SBR8
		Write:								
$00C9	SCI0BDL	Read: Write:	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
$00CA	SCI0CR1	Read: Write:	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
$00CB	SCI0CR2	Read: Write:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
$00CC	SCI0SR1	Read:	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
		Write:								
$00CD	SCI0SR2	Read:	0	0	0	0	0	BRK13	TXDIR	RAF
		Write:								
$00CE	SCI0DRH	Read:	R8	T8	0	0	0	0	0	0
		Write:								
$00CF	SCI0DRL	Read:	R7	R6	R5	R4	R3	R2	R1	R0
		Write:	T7	T6	T5	T4	T3	T2	T1	T0

$00D0 - $00D7 SCI1 (Asynchronous Serial Interface) only on MC9S12H256

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00D0	SCI1BDH	Read:	0	0	0	SBR12	SBR11	SBR10	SBR9	SBR8
		Write:								
$00D1	SCI1BDL	Read: Write:	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
$00D2	SCI1CR1	Read: Write:	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
$00D3	SCI1CR2	Read: Write:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
$00D4	SCI1SR1	Read:	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
		Write:								

$00D0 - $00D7 SCI1 (Asynchronous Serial Interface) only on MC9S12H256

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00D5	SCI1SR2	Read:	0	0	0	0	0	BRK13	TXDIR	RAF
		Write:								
$00D6	SCI1DRH	Read:	R8	T8	0	0	0	0	0	0
		Write:								
$00D7	SCI1DRL	Read:	R7	R6	R5	R4	R3	R2	R1	R0
		Write:	T7	T6	T5	T4	T3	T2	T1	T0

$00D8 - $00DF SPI (Serial Peripheral Interface)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00D8	SPICR1	Read: Write:	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
$00D9	SPICR2	Read:	0	0	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
		Write:								
$00DA	SPIBR	Read:	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
		Write:								
$00DB	SPISR	Read:	SPIF	0	SPTEF	MODF	0	0	0	0
		Write:								
$00DC	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00DD	SPIDR	Read: Write:	Bit7	6	5	4	3	2	1	Bit0
$00DE	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$00DF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$00E0 - $00FF PWM (Pulse Width Modulator 8 Bit 6 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00E0	PWME	Read:	0	0	PWME5	PWME4	PWME3	PWME2	PWME1	PWME0
		Write:								
$00E1	PWMPOL	Read:	0	0	PPOL5	PPOL4	PPOL3	PPOL2	PPOL1	PPOL0
		Write:								
$00E2	PWMCLK	Read:	0	0	PCLK5	PCLK4	PCLK3	PCLK2	PCLK1	PCLK0
		Write:								
$00E3	PWMPRCLK	Read:	0	PCKB2	PCKB1	PCKB0	0	PCKA2	PCKA1	PCKA0
		Write:								
$00E4	PWMCAE	Read:	0	0	CAE5	CAE4	CAE3	CAE2	CAE1	CAE0
		Write:								
$00E5	PWMCTL	Read:	0	CON45	CON23	CON01	PSWAI	PFRZ	0	0
		Write:								
$00E6	PWMTST Test Only	Read:	0	0	0	0	0	0	0	0
		Write:								
$00E7	PWMPRSC Test Only	Read:	0	0	0	0	0	0	0	0
		Write:								
$00E8	PWMSCLA	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0

$00E0 - $00FF PWM (Pulse Width Modulator 8 Bit 6 Channel)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00E9	PWMSCLB	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00EA	PWMSCNTA Test Only	Read:	0	0	0	0	0	0	0	0
		Write:								
$00EB	PWMSCNTB Test Only	Read:	0	0	0	0	0	0	0	0
		Write:								
$00EC	PWMCNT0	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00ED	PWMCNT1	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00EE	PWMCNT2	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00EF	PWMCNT3	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00F0	PWMCNT4	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00F1	PWMCNT5	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:	0	0	0	0	0	0	0	0
$00F2	PWMPER0	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00F3	PWMPER1	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00F4	PWMPER2	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00F5	PWMPER3	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00F6	PWMPER4	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00F7	PWMPER5	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00F8	PWMDTY0	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00F9	PWMDTY1	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00FA	PWMDTY2	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00FB	PWMDTY3	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00FC	PWMDTY4	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00FD	PWMDTY5	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$00FE	PWMSDN	Read:	PWMIF	PWMIE	PWMRSTRT	PWMLVL	0	PWM5IN	PWM5INL	PWM5ENA
		Write:								
$00FF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0100 - $010F Flash Control Register (fts256k)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0100	FCLKDIV	Read:	FDIVLD	PRDIV8	FDIV5	FDIV4	FDIV3	FDIV2	FDIV1	FDIV0
		Write:								
$0101	FSEC	Read:	KEYEN	NV6	NV5	NV4	NV3	NV2	SEC1	SEC0
		Write:								
$0102	Reserved	Read:	0	0	0	WRALL	0	0	0	0
		Write:								
$0103	FCNFG	Read:	CBEIE	CCIE	KEYACC	0	0	0	BKSEL1	BKSEL0
		Write:								
$0104	FPROT	Read:	FPOPEN	NV6	FPHDIS	FPHS1	FPHS0	FPLDIS	FPLS1	FPLS0
		Write:								
$0105	FSTAT	Read:	CBEIF	CCIF	PVIOL	ACCERR	0	BLANK	0	0
		Write:								
$0106	FCMD	Read:	0	CMDB6	CMDB5	0	0	CMDB2	0	CMDB0
		Write:								
$0107	Reserved for Factory Test	Read:	0	0	0	0	0	0	0	0
		Write:								
$0108	FADDRHI	Read:	0	Bit 14	13	12	11	10	9	Bit 8
		Write:								
$0109	FADDRLO	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$010A	FDATAHI	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
$010B	FDATALO	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
$010C - $010F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0110 - $011B EEPROM Control Register (eets4k)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0110	ECLKDIV	Read:	EDIVLD	PRDIV8	EDIV5	EDIV4	EDIV3	EDIV2	EDIV1	EDIV0
		Write:								
$0111	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0112	Reserved for Factory Test	Read:	0	0	0	0	0	0	0	0
		Write:								
$0113	ECNFG	Read:	CBEIE	CCIE	0	0	0	0	0	0
		Write:								
$0114	EPROT	Read:	EPOPEN	NV6	NV5	NV4	EPDIS	EP2	EP1	EP0
		Write:								
$0115	ESTAT	Read:	CBEIF	CCIF	PVIOL	ACCERR	0	BLANK	0	0
		Write:								
$0116	ECMD	Read:	0	CMDB6	CMDB5	0	0	CMDB2	0	CMDB0
		Write:								
$0117	Reserved for Factory Test	Read:	0	0	0	0	0	0	0	0
		Write:								
$0118	EADDRHI	Read:	0	0	0	0	0	10	9	Bit 8
		Write:								

$0110 - $011B EEPROM Control Register (eets4k)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0119	EADDRLO	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
$011A	EDATAHI	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
$011B	EDATALO	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0

$011C - $011F Reserved for RAM Control Register

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$011C - $011F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0120 - $0137 LCD (Liquid Crystal Display 32 frontplanes, 4 backplanes)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0120	LCDCR0	Read:	LCDEN	0	LCLK2	LCLK1	LCLK0	BIAS	DUTY1	DUTY0
		Write:								
$0121	LCDCR1	Read:	0	0	0	0	0	0	LCDSWAI	LCDRPSTP
		Write:								
$0122	FPENR0	Read: Write:	FPEN7	FPEN6	FPEN5	FPEN4	FPEN3	FPEN2	FPEN1	FPEN0
$0123	FPENR1	Read: Write:	FPEN15	FPEN14	FPEN13	FPEN12	FPEN11	FPEN10	FPEN9	FPEN8
$0124	FPENR2	Read: Write:	FPEN23	FPEN22	FPEN21	FPEN20	FPEN19	FPEN18	FPEN17	FPEN16
$0125	FPENR3	Read: Write:	FPEN31	FPEN30	FPEN29	FPEN28	FPEN27	FPEN26	FPEN25	FPEN24
$0126	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0127	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0128	LCDRAM0	Read: Write:	FP1BP3	FP1BP2	FP1BP1	FP1BP0	FP0BP3	FP0BP2	FP0BP1	FP0BP0
$0129	LCDRAM1	Read: Write:	FP3BP3	FP3BP2	FP3BP1	FP3BP0	FP2BP3	FP2BP2	FP2BP1	FP2BP0
$012A	LCDRAM2	Read: Write:	FP5BP3	FP5BP2	FP5BP1	FP5BP0	FP4BP3	FP4BP2	FP4BP1	FP4BP0
$012B	LCDRAM3	Read: Write:	FP7BP3	FP7BP2	FP7BP1	FP7BP0	FP6BP3	FP6BP2	FP6BP1	FP6BP0
$012C	LCDRAM4	Read: Write:	FP9BP3	FP9BP2	FP9BP1	FP9BP0	FP8BP3	FP8BP2	FP8BP1	FP8BP0
$012D	LCDRAM5	Read: Write:	FP11BP3	FP11BP2	FP11BP1	FP11BP0	FP10BP3	FP10BP2	FP10BP1	FP10BP0
$012E	LCDRAM6	Read: Write:	FP13BP3	FP13BP2	FP13BP1	FP13BP0	FP12BP3	FP12BP2	FP12BP1	FP12BP0
$012F	LCDRAM7	Read: Write:	FP15BP3	FP15BP2	FP15BP1	FP15BP0	FP14BP3	FP14BP2	FP14BP1	FP14BP0

$0120 - $0137 LCD (Liquid Crystal Display 32 frontplanes, 4 backplanes)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0130	LCDRAM8	Read: Write:	FP17BP3	FP17BP2	FP17BP1	FP17BP0	FP16BP3	FP16BP2	FP16BP1	FP16BP0
$0131	LCDRAM9	Read: Write:	FP19BP3	FP19BP2	FP19BP1	FP19BP0	FP18BP3	FP18BP2	FP18BP1	FP18BP0
$0132	LCDRAM10	Read: Write:	FP21BP3	FP21BP2	FP21BP1	FP21BP0	FP20BP3	FP20BP2	FP20BP1	FP20BP0
$0133	LCDRAM11	Read: Write:	FP23BP3	FP23BP2	FP23BP1	FP23BP0	FP22BP3	FP22BP2	FP22BP1	FP22BP0
$0134	LCDRAM12	Read: Write:	FP25BP3	FP25BP2	FP25BP1	FP25BP0	FP24BP3	FP24BP2	FP24BP1	FP24BP0
$0135	LCDRAM13	Read: Write:	FP27BP3	FP27BP2	FP27BP1	FP27BP0	FP26BP3	FP26BP2	FP26BP1	FP26BP0
$0136	LCDRAM14	Read: Write:	FP29BP3	FP29BP2	FP29BP1	FP29BP0	FP28BP3	FP28BP2	FP28BP1	FP28BP0
$0137	LCDRAM15	Read: Write:	FP31BP3	FP31BP2	FP31BP1	FP31BP0	FP30BP3	FP30BP2	FP30BP1	FP30BP0

$0140 - $017F CAN0 (Freescale Scalable CAN - MSCAN)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0140	CAN0CTL0	Read: Write:	RXFRM	RXACT —	CSWAI	SYNCH —	TIME	WUPE	SLPRQ	INITRQ
$0141	CAN0CTL1	Read: Write:	CANE	CLKSRC	LOOPB	LISTEN	0 —	WUPM	SLPAK —	INITAK —
$0142	CAN0BTR0	Read: Write:	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
$0143	CAN0BTR1	Read: Write:	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
$0144	CAN0RFLG	Read: Write:	WUPIF	CSCIF	RSTAT1 —	RSTAT0 —	TSTAT1 —	TSTAT0 —	OVRIF	RXF
$0145	CAN0RIER	Read: Write:	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
$0146	CAN0TFLG	Read: Write:	0 —	0 —	0 —	0 —	0 —	TXE2	TXE1	TXE0
$0147	CAN0TIER	Read: Write:	0 —	0 —	0 —	0 —	0 —	TXEIE2	TXEIE1	TXEIE0
$0148	CAN0TARQ	Read: Write:	0 —	0 —	0 —	0 —	0 —	ABTRQ2	ABTRQ1	ABTRQ0
$0149	CAN0TAAK	Read: Write:	0 —	0 —	0 —	0 —	0 —	ABTAK2 —	ABTAK1 —	ABTAK0 —
$014A	CAN0TBSEL	Read: Write:	0 —	0 —	0 —	0 —	0 —	TX2	TX1	TX0
$014B	CAN0IDAC	Read: Write:	0 —	0 —	IDAM1	IDAM0	0 —	IDHIT2 —	IDHIT1 —	IDHIT0 —
$014C	Reserved	Read: Write:	0 —	0 —	0 —	0 —	0 —	0 —	0 —	0 —
$014D	Reserved	Read: Write:	0 —	0 —	0 —	0 —	0 —	0 —	0 —	0 —
$014E	CAN0RXERR	Read: Write:	RXERR7 —	RXERR6 —	RXERR5 —	RXERR4 —	RXERR3 —	RXERR2 —	RXERR1 —	RXERR0 —

$0140 - $017F CAN0 (Freescale Scalable CAN - MSCAN)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$014F	CAN0TXERR	Read:	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
		Write:								
$0150 - $0153	CAN0IDAR0 - CAN0IDAR3	Read: Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$0154 - $0157	CAN0IDMR0 - CAN0IDMR3	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$0158 - $015B	CAN0IDAR4 - CAN0IDAR7	Read: Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$015C - $015F	CAN0IDMR4 - CAN0IDMR7	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$0160 - $016F	CAN0RXFG	Read:	FOREGROUND RECEIVE BUFFER see **Table 1-3**							
		Write:								
$0170 - $017F	CAN0TXFG	Read: Write:	FOREGROUND TRANSMIT BUFFER see **Table 1-3**							

Table 1-3 Detailed MSCAN Foreground Receive and Transmit Buffer Layout

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Extended ID	Read:	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
$0160	Standard ID	Read:	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3
	CAN0RIDR0	Write:								
	Extended ID	Read:	ID20	ID19	ID18	SRR=1	IDE=1	ID17	ID16	ID15
$0161	Standard ID	Read:	ID2	ID1	ID0	RTR	IDE=0			
	CAN0RIDR1	Write:								
	Extended ID	Read:	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7
$0162	Standard ID	Read:								
	CAN0RIDR2	Write:								
	Extended ID	Read:	ID6	ID5	ID4	ID3	ID2	ID1	ID0	RTR
$0163	Standard ID	Read:								
	CAN0RIDR3	Write:								
$0164-	CAN0RDSR0 -	Read:	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
$016B	CAN0RDSR7	Write:								
$016C	CAN0RDLR	Read:					DLC3	DLC2	DLC1	DLC0
		Write:								
$016D	Reserved	Read: Write:								
$016E	CAN0RTSRH	Read:	TSR15	TSR14	TSR13	TSR12	TSR11	TSR10	TSR9	TSR8
		Write:								
$016F	CAN0RTSRL	Read:	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0
		Write:								
$0170	Extended ID CAN0TIDR0	Read: Write:	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
	Standard ID	Read: Write:	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3
$0171	Extended ID CAN0TIDR1	Read: Write:	ID20	ID19	ID18	SRR=1	IDE=1	ID17	ID16	ID15
	Standard ID	Read: Write:	ID2	ID1	ID0	RTR	IDE=0			

Table 1-3 Detailed MSCAN Foreground Receive and Transmit Buffer Layout

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0172	Extended ID CAN0TIDR2	Read: Write:	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7
	Standard ID	Read: Write:								
$0173	Extended ID CAN0TIDR3	Read: Write:	ID6	ID5	ID4	ID3	ID2	ID1	ID0	RTR
	Standard ID	Read: Write:								
$0174- $017B	CAN0TDSR0 - CAN0TDSR7	Read: Write:	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
$017C	CAN0TDLR	Read: Write:					DLC3	DLC2	DLC1	DLC0
$017D	CON0TTBPR	Read: Write:	PRIO7	PRIO6	PRIO5	PRIO4	PRIO3	PRIO2	PRIO1	PRIO0
$017E	CAN0TTSRH	Read:	TSR15	TSR14	TSR13	TSR12	TSR11	TSR10	TSR9	TSR8
		Write:								
$017F	CAN0TTSRL	Read:	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0
		Write:								

$0180 - $01BF CAN1 (Freescale Scalable CAN - MSCAN)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0180	CAN1CTL0	Read:	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
		Write:								
$0181	CAN1CTL1	Read:	CANE	CLKSRC	LOOPB	LISTEN	0	WUPM	SLPAK	INITAK
		Write:								
$0182	CAN1BTR0	Read: Write:	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
$0183	CAN1BTR1	Read: Write:	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
$0184	CAN1RFLG	Read:	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
		Write:								
$0185	CAN1RIER	Read: Write:	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
$0186	CAN1TFLG	Read:	0	0	0	0	0	TXE2	TXE1	TXE0
		Write:								
$0187	CAN1TIER	Read:	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
		Write:								
$0188	CAN1TARQ	Read:	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
		Write:								
$0189	CAN1TAAK	Read:	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
		Write:								
$018A	CAN1TBSEL	Read:	0	0	0	0	0	TX2	TX1	TX0
		Write:								
$018B	CAN1IDAC	Read:	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHIT0
		Write:								
$018C	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$018D	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0180 - $01BF CAN1 (Freescale Scalable CAN - MSCAN)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$018E	CAN1RXERR	Read:	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
		Write:								
$018F	CAN1TXERR	Read:	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
		Write:								
$0190 - $0193	CAN1IDAR0 - CAN1IDAR3	Read: Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$0194 - $0197	CAN1IDMR0 - CAN1IDMR3	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$0198 - $019B	CAN1IDAR4 - CAN1IDAR7	Read: Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
$019C - $019F	CAN1IDMR4 - CAN1IDMR7	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
$01A0 - $01AF	CAN1RXFG	Read:	FOREGROUND RECEIVE BUFFER see **Table 1-3**							
		Write:								
$01B0 - $01BF	CAN1TXFG	Read: Write:	FOREGROUND TRANSMIT BUFFER see **Table 1-3**							

Table 1-4 Detailed MSCAN Foreground Receive and Transmit Buffer Layout

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Extended ID	Read:	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
$01A0	Standard ID	Read:	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3
	CAN1RIDR0	Write:								
	Extended ID	Read:	ID20	ID19	ID18	SRR=1	IDE=1	ID17	ID16	ID15
$01A1	Standard ID	Read:	ID2	ID1	ID0	RTR	IDE=0			
	CAN1RIDR1	Write:								
	Extended ID	Read:	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7
$01A2	Standard ID	Read:								
	CAN1RIDR2	Write:								
	Extended ID	Read:	ID6	ID5	ID4	ID3	ID2	ID1	ID0	RTR
$01A3	Standard ID	Read:								
	CAN1RIDR3	Write:								
$01A4- $01AB	CAN1RDSR0 - CAN1RDSR7	Read:	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		Write:								
$01AC	CAN1RDLR	Read:					DLC3	DLC2	DLC1	DLC0
		Write:								
$01AD	Reserved	Read: Write:								
$01AE	CAN1RTSRH	Read:	TSR15	TSR14	TSR13	TSR12	TSR11	TSR10	TSR9	TSR8
		Write:								
$01AF	CAN1RTSRL	Read:	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0
		Write:								
$01B0	Extended ID CAN1TIDR0	Read: Write:	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
	Standard ID	Read: Write:	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3

Table 1-4 Detailed MSCAN Foreground Receive and Transmit Buffer Layout

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$01B1	Extended ID CAN1TIDR1	Read: Write:	ID20	ID19	ID18	SRR=1	IDE=1	ID17	ID16	ID15
	Standard ID	Read: Write:	ID2	ID1	ID0	RTR	IDE=0			
$01B2	Extended ID CAN1TIDR2	Read: Write:	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7
	Standard ID	Read: Write:								
$01B3	Extended ID CAN1TIDR3	Read: Write:	ID6	ID5	ID4	ID3	ID2	ID1	ID0	RTR
	Standard ID	Read: Write:								
$01B4- $01BB	CAN1TDSR0 - CAN1TDSR7	Read: Write:	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
$01BC	CAN1TDLR	Read: Write:					DLC3	DLC2	DLC1	DLC0
$01BD	CON1TTBPR	Read: Write:	PRIO7	PRIO6	PRIO5	PRIO4	PRIO3	PRIO2	PRIO1	PRIO0
$01BE	CAN1TTSRH	Read:	TSR15	TSR14	TSR13	TSR12	TSR11	TSR10	TSR9	TSR8
		Write:								
$01BF	CAN1TTSRL	Read:	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0
		Write:								

$01C0 - $01FF MC (Motor Controller 10bit 12 channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$01C0	MCCTL0	Read:	0	MCPRE1	MCPRE0	MCSWAI	FAST	DITH	0	MCTOIF
		Write:								
$01C1	MCCTL1	Read:	RECIRC	0	0	0	0	0	0	MCTOIE
		Write:								
$01C2	MCPER (hi)	Read:	0	0	0	0	0	P10	P9	P8
		Write:								
$01C3	MCPER (lo)	Read: Write:	P7	P6	P5	P4	P3	P2	P1	P0
$01C4	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01C5	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01C6	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01C7	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01C8	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01C9	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01CA	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01CB	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$01C0 - $01FF MC (Motor Controller 10bit 12 channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$01CC	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01CD	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01CE	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01CF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01D0	MCCC0	Read:	OM1	OM0	AM1	AM0	0	0	CD1	CD0
		Write:								
$01D1	MCCC1	Read:	OM1	OM0	AM1	AM0	0	0	CD1	CD0
		Write:								
$01D2	MCCC2	Read:	OM1	OM0	AM1	AM0	0	0	CD1	CD0
		Write:								
$01D3	MCCC3	Read:	OM1	OM0	AM1	AM0	0	0	CD1	CD0
		Write:								
$01D4	MCCC4	Read:	OM1	OM0	AM1	AM0	0	0	CD1	CD0
		Write:								
$01D5	MCCC5	Read:	OM1	OM0	AM1	AM0	0	0	CD1	CD0
		Write:								
$01D6	MCCC6	Read:	OM1	OM0	AM1	AM0	0	0	CD1	CD0
		Write:								
$01D7	MCCC7	Read:	OM1	OM0	AM1	AM0	0	0	CD1	CD0
		Write:								
$01D8	MCCC8	Read:	OM1	OM0	AM1	AM0	0	0	CD1	CD0
		Write:								
$01D9	MCCC9	Read:	OM1	OM0	AM1	AM0	0	0	CD1	CD0
		Write:								
$01DA	MCCC10	Read:	OM1	OM0	AM1	AM0	0	0	CD1	CD0
		Write:								
$01DB	MCCC11	Read:	OM1	OM0	AM1	AM0	0	0	CD1	CD0
		Write:								
$01DC	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01DD	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01DE	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01DF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01E0	MCDC0 (hi)	Read:	S	S	S	S	S	D10	D9	D8
		Write:								
$01E1	MCDC0 (lo)	Read:	D7	D6	D5	D4	D3	D2	D1	D0
		Write:								
$01E2	MCDC1 (hi)	Read:	S	S	S	S	S	D10	D9	D8
		Write:								
$01E3	MCDC1 (lo)	Read:	D7	D6	D5	D4	D3	D2	D1	D0
		Write:								
$01E4	MCDC2 (hi)	Read:	S	S	S	S	S	D10	D9	D8
		Write:								

$01C0 - $01FF MC (Motor Controller 10bit 12 channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$01E5	MCDC2 (lo)	Read:	D7	D6	D5	D4	D3	D2	D1	D0
		Write:								
$01E6	MCDC3 (hi)	Read:	S	S	S	S	S	D10	D9	D8
		Write:								
$01E7	MCDC3 (lo)	Read:	D7	D6	D5	D4	D3	D2	D1	D0
		Write:								
$01E8	MCDC4 (hi)	Read:	S	S	S	S	S	D10	D9	D8
		Write:								
$01E9	MCDC4 (lo)	Read:	D7	D6	D5	D4	D3	D2	D1	D0
		Write:								
$01EA	MCDC5 (hi)	Read:	S	S	S	S	S	D10	D9	D8
		Write:								
$01EB	MCDC5 (lo)	Read:	D7	D6	D5	D4	D3	D2	D1	D0
		Write:								
$01EC	MCDC6 (hi)	Read:	S	S	S	S	S	D10	D9	D8
		Write:								
$01ED	MCDC6 (lo)	Read:	D7	D6	D5	D4	D3	D2	D1	D0
		Write:								
$01EE	MCDC7 (hi)	Read:	S	S	S	S	S	D10	D9	D8
		Write:								
$01EF	MCDC7 (lo)	Read:	D7	D6	D5	D4	D3	D2	D1	D0
		Write:								
$01F0	MCDC8 (hi)	Read:	S	S	S	S	S	D10	D9	D8
		Write:								
$01F1	MCDC8 (lo)	Read:	D7	D6	D5	D4	D3	D2	D1	D0
		Write:								
$01F2	MCDC9 (hi)	Read:	S	S	S	S	S	D10	D9	D8
		Write:								
$01F3	MCDC9 (lo)	Read:	D7	D6	D5	D4	D3	D2	D1	D0
		Write:								
$01F4	MCDC10 (hi)	Read:	S	S	S	S	S	D10	D9	D8
		Write:								
$01F5	MCDC10 (lo)	Read:	D7	D6	D5	D4	D3	D2	D1	D0
		Write:								
$01F6	MCDC11 (hi)	Read:	S	S	S	S	S	D10	D9	D8
		Write:								
$01F7	MCDC11 (lo)	Read:	D7	D6	D5	D4	D3	D2	D1	D0
		Write:								
$01F8	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01F9	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01FA	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01FB	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01FC	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$01C0 - $01FF MC (Motor Controller 10bit 12 channels)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$01FD	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01FE	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$01FF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0200 - $027F PIM (Port Integration Module)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0200	PTT	Read: Write:	PTT7	PTT6	PTT5	PTT4	PTT3	PTT2	PTT1	PTT0
$0201	PTIT	Read:	PTIT7	PTIT6	PTIT5	PTIT4	PTIT3	PTIT2	PTIT1	PTIT0
		Write:								
$0202	DDRT	Read: Write:	DDRT7	DDRT7	DDRT5	DDRT4	DDRT3	DDRT2	DDRT1	DDRT0
$0203	RDRT	Read: Write:	RDRT7	RDRT6	RDRT5	RDRT4	RDRT3	RDRT2	RDRT1	RDRT0
$0204	PERT	Read: Write:	PERT7	PERT6	PERT5	PERT4	PERT3	PERT2	PERT1	PERT0
$0205	PPST	Read: Write:	PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0
$0206	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0207	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0208	PTS	Read: Write:	PTS7	PTS6	PTS5	PTS4	PTS3	PTS2	PTS1	PTS0
$0209	PTIS	Read:	PTIS7	PTIS6	PTIS5	PTIS4	PTIS3	PTIS2	PTIS1	PTIS0
		Write:								
$020A	DDRS	Read: Write:	DDRS7	DDRS7	DDRS5	DDRS4	DDRS3	DDRS2	DDRS1	DDRS0
$020B	RDRS	Read: Write:	RDRS7	RDRS6	RDRS5	RDRS4	RDRS3	RDRS2	RDRS1	RDRS0
$020C	PERS	Read: Write:	PERS7	PERS6	PERS5	PERS4	PERS3	PERS2	PERS1	PERS0
$020D	PPSS	Read: Write:	PPSS7	PPSS6	PPSS5	PPSS4	PPSS3	PPSS2	PPSS1	PPSS0
$020E	WOMS	Read: Write:	WOMS7	WOMS6	WOMS5	WOMS4	WOMS3	WOMS2	WOMS1	WOMS0
$020F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0210	PTM	Read:	0	0	PTM5	PTM4	PTM3	PTM2	PTM1	PTM0
		Write:								
$0211	PTIM	Read:	0	0	PTIM5	PTIM4	PTIM3	PTIM2	PTIM1	PTIM0
		Write:								
$0212	DDRM	Read:	0	0	DDRM5	DDRM4	DDRM3	DDRM2	DDRM1	DDRM0
		Write:								

$0200 - $027F PIM (Port Integration Module)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0213	RDRM	Read:	0	0	RDRM5	RDRM4	RDRM3	RDRM2	RDRM1	RDRM0
		Write:								
$0214	PERM	Read:	0	0	PERM5	PERM4	PERM3	PERM2	PERM1	PERM0
		Write:								
$0215	PPSM	Read:	0	0	PPSM5	PPSM4	PPSM3	PPSM2	PPSM1	PPSM0
		Write:								
$0216	WOMM	Read:	0	0	WOMM5	WOMM4	WOMM3	WOMM2	WOMM1	WOMM0
		Write:								
$0217	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0218	PTP	Read:	0	0	PTP5	PTP4	PTP3	PTP2	PTP1	PTP0
		Write:								
$0219	PTIP	Read:	0	0	PTIP5	PTIP4	PTIP3	PTIP2	PTIP1	PTIP0
		Write:								
$021A	DDRP	Read:	0	0	DDRP5	DDRP4	DDRP3	DDRP2	DDRP1	DDRP0
		Write:								
$021B	RDRP	Read:	0	0	RDRP5	RDRP4	RDRP3	RDRP2	RDRP1	RDRP0
		Write:								
$021C	PERP	Read:	0	0	PERP5	PERP4	PERP3	PERP2	PERP1	PERP0
		Write:								
$021D	PPSP	Read:	0	0	PPSP5	PPSP4	PPSP3	PPSP2	PPSP1	PPSS0
		Write:								
$021E	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$021F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0220	PTH	Read:	PTH7	PTH6	PTH5	PTH4	PTH3	PTH2	PTH1	PTH0
		Write:								
$0221	PTIH	Read:	PTIH7	PTIH6	PTIH5	PTIH4	PTIH3	PTIH2	PTIH1	PTIH0
		Write:								
$0222	DDRH	Read:	DDRH7	DDRH7	DDRH5	DDRH4	DDRH3	DDRH2	DDRH1	DDRH0
		Write:								
$0223	RDRH	Read:	RDRH7	RDRH6	RDRH5	RDRH4	RDRH3	RDRH2	RDRH1	RDRH0
		Write:								
$0224	PERH	Read:	PERH7	PERH6	PERH5	PERH4	PERH3	PERH2	PERH1	PERH0
		Write:								
$0225	PPSH	Read:	PPSH7	PPSH6	PPSH5	PPSH4	PPSH3	PPSH2	PPSH1	PPSH0
		Write:								
$0226	PIEH	Read:	PIEH7	PIEH6	PIEH5	PIEH4	PIEH3	PIEH2	PIEH1	PIEH0
		Write:								
$0227	PIFH	Read:	PIFH7	PIFH6	PIFH5	PIFH4	PIFH3	PIFH2	PIFH1	PIFH0
		Write:								
$0228	PTJ	Read:	0	0	0	0	PTJ3	PTJ2	PTJ1	PTJ0
		Write:								
$0229	PTIJ	Read:	0	0	0	0	PTIJ3	PTIJ2	PTIJ1	PTIJ0
		Write:								
$022A	DDRJ	Read:	0	0	0	0	DDRJ3	DDRJ2	DDRJ1	DDRJ0
		Write:								
$022B	RDRJ	Read:	0	0	0	0	RDRJ3	RDRJ2	RDRJ1	RDRJ0
		Write:								

$0200 - $027F PIM (Port Integration Module)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$022C	PERJ	Read:	0	0	0	0	PERJ3	PERJ2	PERJ1	PERJ0
		Write:								
$022D	PPSJ	Read:	0	0	0	0	PPSJ3	PPSJ2	PPSJ1	PPSJ0
		Write:								
$022E	PIEJ	Read:	0	0	0	0	PIEJ3	PIEJ2	PIEJ1	PIEJ0
		Write:								
$022F	PIFJ	Read:	0	0	0	0	PIFJ3	PIFJ2	PIFJ1	PIFJ0
		Write:								
$0230	PTL	Read:	PTL7	PTL6	PTL5	PTL4	PTL3	PTL2	PTL1	PTL0
		Write:								
$0231	PTIL	Read:	PTIL7	PTIL6	PTIL5	PTIL4	PTIL3	PTIL2	PTIL1	PTIL0
		Write:								
$0232	DDRL	Read:	DDRL7	DDRL7	DDRL5	DDRL4	DDRL3	DDRL2	DDRL1	DDRL0
		Write:								
$0233	RDRL	Read:	RDRL7	RDRL6	RDRL5	RDRL4	RDRL3	RDRL2	RDRL1	RDRL0
		Write:								
$0234	PERL	Read:	PERL7	PERL6	PERL5	PERL4	PERL3	PERL2	PERL1	PERL0
		Write:								
$0235	PPSL	Read:	PPSL7	PPSL6	PPSL5	PPSL4	PPSL3	PPSL2	PPSL1	PPSL0
		Write:								
$0236	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0237	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0238	PTU	Read:	PTU7	PTU6	PTU5	PTU4	PTU3	PTU2	PTU1	PTU0
		Write:								
$0239	PTIU	Read:	PTIU7	PTIU6	PTIU5	PTIU4	PTIU3	PTIU2	PTIU1	PTIU0
		Write:								
$023A	DDRU	Read:	DDRU7	DDRU7	DDRU5	DDRU4	DDRU3	DDRU2	DDRU1	DDRU0
		Write:								
$023B	SRRU	Read:	SRRU7	SRRU6	SRRU5	SRRU4	SRRU3	SRRU2	SRRU1	SRRU0
		Write:								
$023C	PERU	Read:	PERU7	PERU6	PERU5	PERU4	PERU3	PERU2	PERU1	PERU0
		Write:								
$023D	PPSU	Read:	PPSU7	PPSU6	PPSU5	PPSU4	PPSU3	PPSU2	PPSU1	PPSU0
		Write:								
$023E	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$023F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0240	PTV	Read:	PTV7	PTV6	PTV5	PTV4	PTV3	PTV2	PTV1	PTV0
		Write:								
$0241	PTIV	Read:	PTIV7	PTIV6	PTIV5	PTIV4	PTIV3	PTIV2	PTIV1	PTIV0
		Write:								
$0242	DDRV	Read:	DDRV7	DDRV7	DDRV5	DDRV4	DDRV3	DDRV2	DDRV1	DDRV0
		Write:								
$0243	SRRV	Read:	SRRV7	SRRV6	SRRV5	SRRV4	SRRV3	SRRV2	SRRV1	SRRV0
		Write:								
$0244	PERV	Read:	PERV7	PERV6	PERV5	PERV4	PERV3	PERV2	PERV1	PERV0
		Write:								

$0200 - $027F PIM (Port Integration Module)

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0245	PPSV	Read: Write:	PPSV7	PPSV6	PPSV5	PPSV4	PPSV3	PPSV2	PPSV1	PPSV0
$0246	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0247	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0248	PTW	Read: Write:	PTW7	PTW6	PTW5	PTW4	PTW3	PTW2	PTW1	PTW0
$0249	PTIW	Read:	PTIW7	PTIW6	PTIW5	PTIW4	PTIW3	PTIW2	PTIW1	PTIW0
		Write:								
$024A	DDRW	Read: Write:	DDRW7	DDRW7	DDRW5	DDRW4	DDRW3	DDRW2	DDRW1	DDRW0
$024B	SRRW	Read: Write:	SRRW7	SRRW6	SRRW5	SRRW4	SRRW3	SRRW2	SRRW1	SRRW0
$024C	PERW	Read: Write:	PERW7	PERW6	PERW5	PERW4	PERW3	PERW2	PERW1	PERW0
$024D	PPSW	Read: Write:	PPSW7	PPSW6	PPSW5	PPSW4	PPSW3	PPSW2	PPSW1	PPSW0
$024E	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$024F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								
$0250 - $027F	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

$0280 - $03FF Reserved

Address	Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0280 - $03FF	Reserved	Read:	0	0	0	0	0	0	0	0
		Write:								

1.6 Part ID Assignments

The part ID is located in two 8-bit registers PARTIDH and PARTIDL at addresses $001A,$001B, respectively. The read-only value is a unique part ID for each revision of the chip. **Table 1-5** shows the assigned part ID numbers.

Table 1-5 Assigned Part ID Numbers

Device	Mask Set Number	Part ID[1]
MC9S12H256	0K78X	$1000
MC9S12H256	1K78X	$1001

NOTES:
1. The coding is as follows:
Bit 15-12: Major family identifier
Bit 11-8: Minor family identifier
Bit 7-4: Major mask set revision number including FAB transfers
Bit 3-0: Minor - non full - mask set revision

The device memory sizes are located in two 8-bit registers MEMSIZ0 and MEMSIZ1 (addresses $001C and $001D after reset). **Table 1-6** shows the read-only values of these registers. Refer to section Module Mapping and Control (MMC) of HCS12 Core User Guide for further details.

Table 1-6 Memory size registers

Register name	Value
MEMSIZ0	$25
MEMSIZ1	$81

Section 2 Signal Description

This section describes signals that connect off-chip. It includes a pinout diagram, a table of signal properties, and detailed discussion of signals. It is built from the signal description sections of the Block User Guides of the individual IP blocks on the device.

2.1 Device Pinout

The MC9S12H256 is available in a 112-pin and 144-pin quad flat pack (LQFP), the MC9S12H128 is available in a 112-pin quad flat pack (LQFP). Most pins perform two or more functions, as described in the Signal Descriptions. **Figure 2-1** and **Figure 2-2** show the pin assignments.

NOTE: *In expanded narrow modes the lower byte data is multiplexed with higher byte data through pins 64-71 on the 112-pin LQFP or through pins 111-118 on the 144-pin LQFP version.*

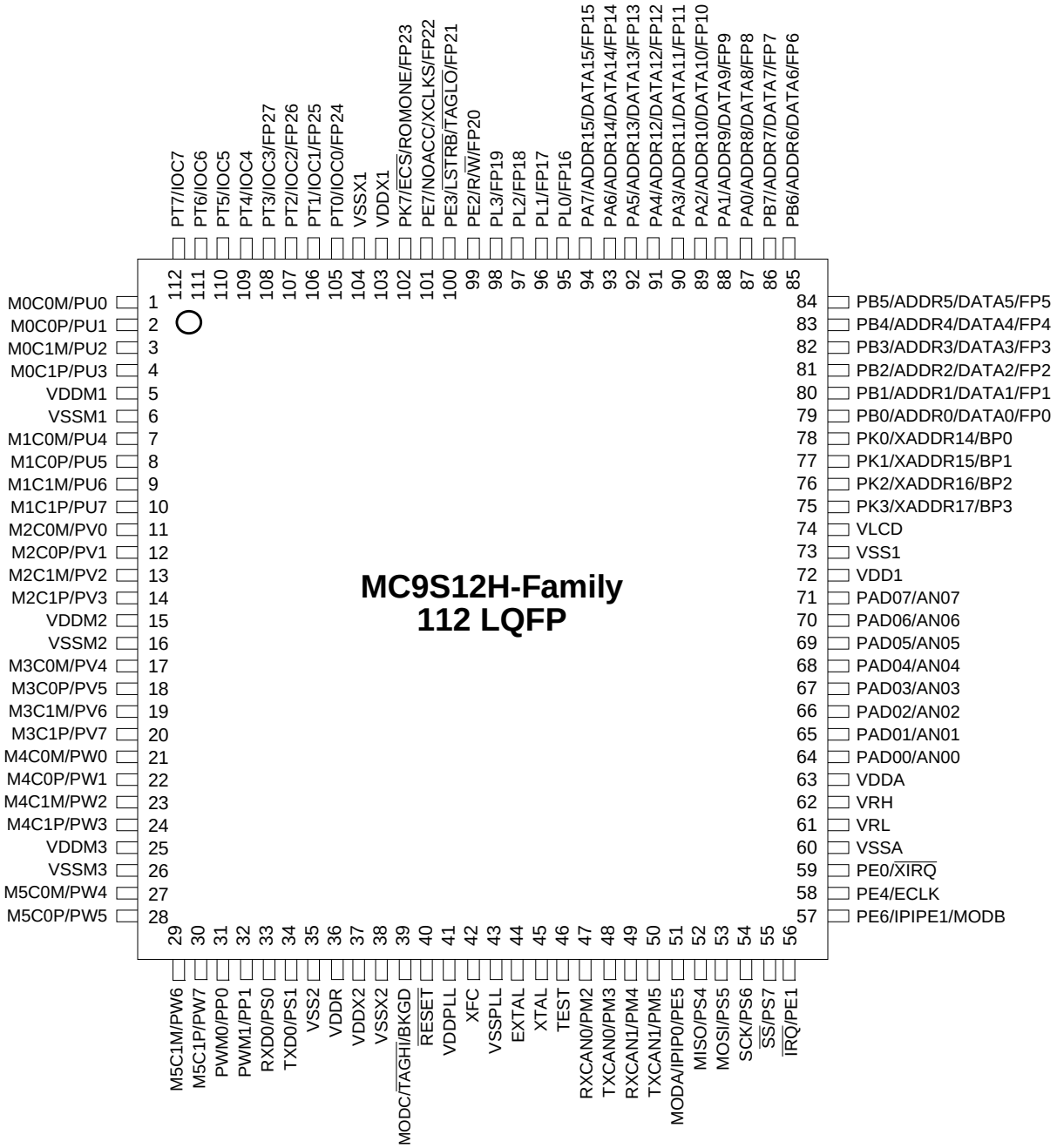


Figure 2-1 Pin Assignments in 112-pin LQFP for MC9S12H256 and MC9S12H128

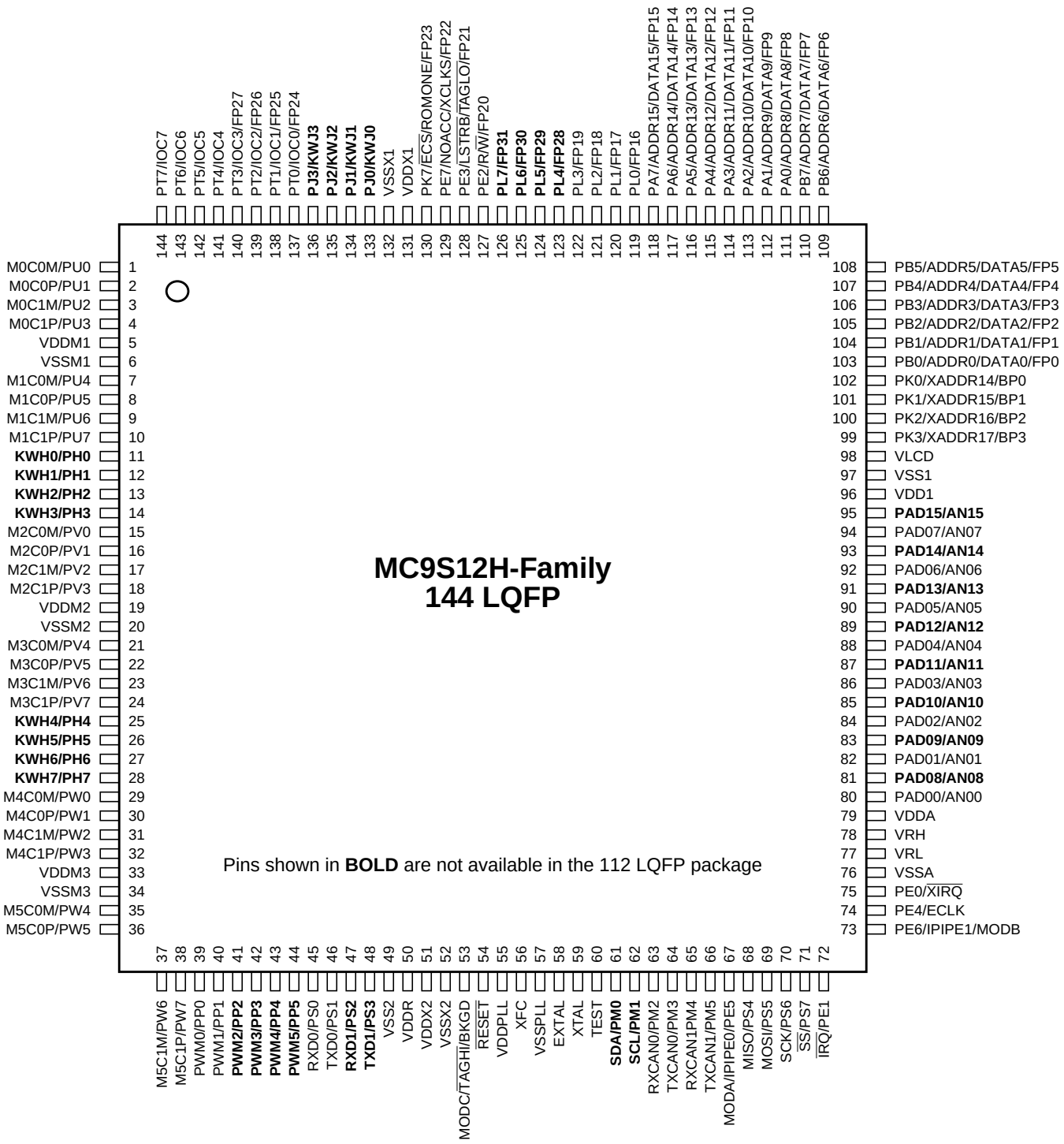


Figure 2-2 Pin Assignments in 144-pin LQFP for MC9S12H256

2.2 Signal Properties Summary

Table 2-1 summarizes all pin functions.

NOTE: *Bold entries determine pins not available on 112-pin LQFP.*

Table 2-1 Signal Properties

Pin Name Function 1	Pin Name Function 2	Pin Name Function 3	Pin Name Function 4	Powered by	Internal Pull Resistor		Description
					CTRL	Reset State	
EXTAL	—	—	—	VDDPLL	None	None	Oscillator Pins
XTAL	—	—	—	VDDPLL			
$\overline{\text{RESET}}$	—	—	—	VDDX2			External Reset Pin
TEST	—	—	—	VDDX2			Test Input
XFC	—	—	—	VDDPLL			PLL Loop Filter
BKGD	$\overline{\text{TAGHI}}$	MODC	—	VDDX2	Always Up	Up	Background Debug, Tag High, Mode Pin
PAD[7:0]	AN[7:0]	—	—	VDDA	None	None	Port AD Inputs, Analog Inputs (ATD)
PAD[15:8]	**AN[15:8]**	**—**	—	VDDA			**Port AD Inputs, Analog Inputs (ATD)**
PA[7:0]	FP[15:8]	ADDR[15:8]/ DATA[15:8]	—	VDDX1	PUCR/ PUPAE	Down	Port A I/O, Multiplexed Address/Data
PB[7:0]	FP[7:0]	ADDR[7:0]/ DATA[7:0]	—	VDDX1	PUCR/ PUPBE	Down	Port B I/O, Multiplexed Address/Data
PE7	FP22	XCLKS	NOACC	VDDX1	PUCR/ PUPEE	Down	Port E I/O, Access, Clock Select, LCD driver
PE6	IPIPE1	MODB	—	VDDX2	While $\overline{\text{RESET}}$ pin is low: Down		Port E I/O, Pipe Status, Mode Input
PE5	IPIPE0	MODA	—	VDDX2			Port E I/O, Pipe Status, Mode Input
PE4	ECLK	—	—	VDDX2	PUCR/ PUPEE	Mode de-pendent	Port E I/O, Bus Clock Output
PE3	FP21	$\overline{\text{LSTRB}}$	$\overline{\text{TAGLO}}$	VDDX1			Port E I/O, LCD driver, Byte Strobe, Tag Low
PE2	FP20	R/$\overline{\text{W}}$	—	VDDX1			Port E I/O, R/$\overline{\text{W}}$ in expanded modes
PE1	$\overline{\text{IRQ}}$	—	—	VDDX2		Up	Port E Input, Maskable Interrupt
PE0	$\overline{\text{XIRQ}}$	—	—	VDDX2			Port E Input, Non Maskable Interrupt
PH[7:0]	**KWH[7:0]**	**—**	—	VDDM	PERH/ PPSH	Disabled	**Port H I/O, Interrupts**
PJ[3:0]	**KWJ[3:0]**	**—**	—	VDDX1	PERJ/ PPSJ	Disabled	**Port J I/O, Interrupts**
PK7	FP23	$\overline{\text{ECS}}$	ROMONE	VDDX1	PUCR/ PUPKE	Down	Port K I/O, Emulation Chip Select, ROM On Enable
PK[3:0]	BP[3:0]	XADDR[17:14]	—	VDDX1			Port K I/O, LCD driver, Extended Addresses
PL[3:0]	FP[19:16]	—	—	VDDX1	PERL/ PPSL	Down	Port L I/O, LCD drivers
PL[7:4]	**FP[31:28]**	**—**	—	VDDX1			**Port L I/O, LCD drivers**

Pin Name Function 1	Pin Name Function 2	Pin Name Function 3	Pin Name Function 4	Powered by	Internal Pull Resistor		Description
					CTRL	Reset State	
PM5	TXCAN1	—	—	VDDX2	PERM/ PPSM	Disabled	Port M I/O, TX of CAN1
PM4	RXCAN1	—	—	VDDX2			Port M I/O, RX of CAN1
PM3	TXCAN0	—	—	VDDX2			Port M I/O, TX of CAN0
PM2	RXCAN0	—	—	VDDX2			Port M I/O, RX of CAN0
PM1	**SCL**	**—**	—	VDDX2			**Port M I/O, SCL of IIC**
PM0	**SDA**	**—**	—	VDDX2			**Port M I/O, SDA of IIC**
PP[5:2]	**PWM[5:2]**	**—**	—	VDDX2	PERP/ PPSP	Disabled	**Port P I/O, PWM channels**
PP[1:0]	PWM[1:0]	—	—	VDDX2			Port P I/O, PWM channels
PS7	$\overline{SS}$	—	—	VDDX2	PERS/ PPSS	Disabled	Port S I/O, $\overline{SS}$ of SPI
PS6	SCK	—	—	VDDX2			Port S I/O, SCK of SPI
PS5	MOSI	—	—	VDDX2			Port S I/O, MOSI of SPI
PS4	MISO	—	—	VDDX2			Port S I/O, MISO of SPI
PS3	**TXD1**	**—**	—	VDDX2			**Port S I/O, TXD of SCI1**
PS2	**RXD1**	**—**	—	VDDX2			**Port S I/O, RXD of SCI1**
PS1	TXD0	—	—	VDDX2			Port S I/O, TXD of SCI0
PS0	RXD0	—	—	VDDX2			Port S I/O, RXD of SCI0
PT[7:4]	IOC[7:4]	—	—	VDDX1	PERT/ PPST	Down	Port T I/O, Timer channels
PT[3:0]	IOC[3:0]	FP[27:24]	—	VDDX1			Port T I/O, Timer channels, LCD driver
PU[3:0]	M0C0M M0C0P M0C1M M0C1P	—	—	VDDM	PERU/ PPSU	Disabled	Port U I/O, Motor0 of MC
PU[7:4]	M1C0M M1C0P M1C1M M1C1P	—	—	VDDM			Port U I/O, Motor1 of MC
PV[3:0]	M2C0M M2C0P M2C1M M2C1P	—	—	VDDM	PERV/ PPSV	Disabled	Port V I/O, Motor2 of MC
PV[7:4]	M3C0M M3C0P M3C1M M3C1P	—	—	VDDM			Port V I/O, Motor3 of MC
PW[3:0]	M4C0M M4C0P M4C1M M4C1P	—	—	VDDM	PERW/ PPSW	Disabled	Port W I/O, Motor4 of MC
PW[7:4]	M5C0M M5C0P, M5C1M M5C1P	—	—	VDDM			Port W I/O, Motor5 of MC

2.3 Detailed Signal Descriptions

2.3.1 EXTAL, XTAL — Oscillator Pins

EXTAL and XTAL are the crystal driver and external clock pins. On reset all the device clocks are derived from the EXTAL input frequency. XTAL is the crystal output.

2.3.2 $\overline{\text{RESET}}$ — External Reset Pin

An active low bidirectional control signal, it acts as an input to initialize the MCU to a known start-up state, and an output when an internal MCU function causes a reset.

2.3.3 TEST — Test Pin

This pin is reserved for test.

NOTE: *The TEST pin must be tied to VSS in all applications.*

2.3.4 XFC — PLL Loop Filter Pin

Dedicated pin used to create the PLL loop filter.

2.3.5 BKGD / $\overline{\text{TAGHI}}$ / MODC — Background Debug, Tag High, and Mode Pin

The BKGD/$\overline{\text{TAGHI}}$/MODC pin is used as a pseudo-open-drain pin for the background debug communication. In MCU expanded modes of operation when instruction tagging is on, an input low on this pin during the falling edge of E-clock tags the high half of the instruction word being read into the instruction queue. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODC bit at the rising edge of $\overline{\text{RESET}}$.

2.3.6 PAD[15:8] / AN[15:8] — Port AD Input Pins [15:8]

PAD15-PAD8 are general purpose input pins and analog inputs for the analog to digital converter.

NOTE: *These pins are not available in the 112-pin LQFP version.*

2.3.7 PAD[7:0] / AN[7:0] — Port AD Input Pins [7:0]

PAD7-PAD0 are general purpose input pins and analog inputs for the analog to digital converter.

2.3.8 PA[7:0] / FP[15:8] / ADDR[15:8] / DATA[15:8] — Port A I/O Pins

PA7-PA0 are general purpose input or output pins. They can be configured as frontplane segment driver outputs FP15-FP8 of the LCD. In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus.

2.3.9 PB[7:0] / FP[7:0] / ADDR[7:0] / DATA[7:0] — Port B I/O Pins

PB7-PB0 are general purpose input or output pins. They can be configured as frontplane segment driver outputs FP7-FP0 of the LCD. In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus.

2.3.10 PE7 / FP22 / XCLKS / NOACC — Port E I/O Pin 7

PE7 is a general purpose input or output pin. It can be configured as frontplane segment driver output FP22 of the LCD module. The XCLKS signal selects between an external clock or oscillator configuration during reset.
The XCLKS input selects between an external clock or oscillator configuration. The state of this pin is latched at the rising edge of $\overline{\text{RESET}}$. If the input is a logic high the EXTAL pin is configured for an external clock drive. If input is a logic low an oscillator circuit is configured on EXTAL and XTAL. Since this pin is an input with a pull-down device during reset, if the pin is left floating, the default configuration is an oscillator circuit on EXTAL and XTAL.
During MCU expanded modes of operation, the NOACC signal, when enabled, is used to indicate that the current bus cycle is an unused or “free” cycle. This signal will assert when the CPU is not using the bus.

2.3.11 PE6 / MODB / IPIPE1 — Port E I/O Pin 6

PE6 is a general purpose input or output pin. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODB bit at the rising edge of $\overline{\text{RESET}}$. This pin is shared with the instruction queue tracking signal IPIPE1. This pin is an input with a pull-down device which is only active when $\overline{\text{RESET}}$ is low.

2.3.12 PE5 / MODA / IPIPE0 — Port E I/O Pin 5

PE5 is a general purpose input or output pin. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODA bit at the rising edge of $\overline{\text{RESET}}$. This pin is shared with the instruction queue tracking signal IPIPE0. This pin is an input with a pull-down device which is only active when $\overline{\text{RESET}}$ is low.

2.3.13 PE4 / ECLK — Port E I/O Pin 4

PE4 is a general purpose input or output pin. It can be configured to drive the internal bus clock ECLK. ECLK can be used as a timing reference.

2.3.14 PE3 / FP21 / $\overline{\text{LSTRB}}$ / $\overline{\text{TAGLO}}$ — Port E I/O Pin 3

PE3 is a general purpose input or output pin. It can be configured as frontplane segment driver output FP21 of the LCD module. In MCU expanded modes of operation, $\overline{\text{LSTRB}}$ is used for the low-byte strobe function to indicate the type of bus access and when instruction tagging is on, $\overline{\text{TAGLO}}$ is used to tag the low half of the instruction word being read into the instruction queue.

2.3.15 PE2 / FP20 / R/$\overline{W}$ — Port E I/O Pin 2

PE2 is a general purpose input or output pin. It can be configured as frontplane segment driver output FP20 of the LCD module. In MCU expanded modes of operations, this pin performs the read/write output signal for the external bus. It indicates the direction of data on the external bus.

2.3.16 PE1 / $\overline{IRQ}$ — Port E Input Pin 1

PE1 is a general purpose input pin and also the maskable interrupt request input that provides a means of applying asynchronous interrupt requests. This will wake up the MCU from STOP or WAIT mode.

2.3.17 PE0 / $\overline{XIRQ}$ — Port E Input Pin 0

PE0 is a general purpose input pin and also the non-maskable interrupt request input that provides a means of applying asynchronous interrupt requests. This will wake up the MCU from STOP or WAIT mode.

2.3.18 PH[7:0] / KWH[7:0] — Port H I/O Pins [7:0]

PH7-PH0 are general purpose input or output pins. They can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode.

NOTE: *These pins are not available in the 112-pin LQFP version.*

2.3.19 PJ[3:0] / KWJ[3:0] — Port J I/O Pins [3:0]

PJ3-PJ0 are general purpose input or output pins. They can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode.and are shared with the interrupt function.

NOTE: *These pins are not available in the 112-pin LQFP version.*

2.3.20 PK7 / FP23 / $\overline{ECS}$ / ROMONE — Port K I/O Pin 7

PK7 is a general purpose input or output pin. It can be configured as frontplane segment driver output FP23 of the LCD module. During MCU expanded modes of operation, this pin is used as the emulation chip select signal ($\overline{ECS}$). During reset of the MCU to normal expanded modes of operation, this pin is used to enable the Flash EEPROM memory in the memory map (ROMONE). At the rising edge of $\overline{RESET}$, the state of this pin is latched to the ROMON bit.

2.3.21 PK[3:0] / BP[3:0] / XADDR[17:14] — Port K I/O Pins [3:0]

PK3-PK0 are general purpose input or output pins. They can be configured as backplane segment driver outputs BP3-BP0 of the LCD module. In MCU expanded modes of operation, these pins provide the expanded address XADDR[17:14] for the external bus.

2.3.22 FreescalePL[7:4] / FP[31:28] — Port L I/O Pins [7:4]

PL7-PL4 are general purpose input or output pins. They can be configured as frontplane segment driver outputs FP31-FP28 of the LCD module.

NOTE: *These pins are not available in the 112-pin LQFP version.*

2.3.23 PL[3:0] / FP[19:16] — Port L I/O Pins [3:0]

PL3-PL0 are general purpose input or output pins. They can be configured as frontplane segment driver outputs FP19-FP16 of the LCD module.

2.3.24 PM5 / TXCAN1 — Port M I/O Pin 5

PM5 is a general purpose input or output pin. It can be configured as the transmit pin TXCAN1 of the Freescale Scalable Controller Area Network controller 1 (CAN1)

2.3.25 PM4 / RXCAN1 — Port M I/O Pin 4

PM4 is a general purpose input or output pin. It can be configured as the receive pin RXCAN1 of the Freescale Scalable Controller Area Network controller 1 (CAN1)

2.3.26 PM3 / TXCAN0 — Port M I/O Pin 3

PM3 is a general purpose input or output pin. It can be configured as the transmit pin TXCAN0 of the Freescale Scalable Controller Area Network controller 0 (CAN0)

2.3.27 PM2 / RXCAN0 — Port M I/O Pin 2

PM2 is a general purpose input or output pin. It can be configured as the receive pin RXCAN0 of the Freescale Scalable Controller Area Network controller 0 (CAN0)

2.3.28 PM1 / SCL — Port M I/O Pin 1

PM1 is a general purpose input or output pin. It can be configured as the serial clock pin SCL of the Inter-IC Bus Interface (IIC).

NOTE: *This pin is not available in the 112-pin LQFP version.*

2.3.29 PM0 / SDA — Port M I/O Pin 0

PM0 is a general purpose input or output pin. It can be configured as the serial data pin SDA of the Inter-IC Bus Interface (IIC).

NOTE: *This pin is not available in the 112-pin LQFP version.*

2.3.30 PP[5:2] / PWM[5:2] — Port P I/O Pins [5:2]

PP5-PP2 are general purpose input or output pins. They can be configured as Pulse Width Modulator (PWM) channel outputs PWM5-PWM2.

NOTE: *These pins are not available in the 112-pin LQFP version.*

2.3.31 PP[1:0] / PWM[1:0] — Port P I/O Pins [1:0]

PP1-PP0 are general purpose input or output pins. They can be configured as Pulse Width Modulator (PWM) channel outputs PWM1-PWM0.

2.3.32 PS7 / $\overline{SS}$ — Port S I/O Pin 7

PS7 is a general purpose input or output pin. It can be configured as slave select pin $\overline{SS}$ of the Serial Peripheral Interface (SPI).

2.3.33 PS6 / SCK — Port S I/O Pin 6

PS6 is a general purpose input or output pin. It can be configured as serial clock pin SCK of the Serial Peripheral Interface (SPI).

2.3.34 PS5 / MOSI — Port S I/O Pin 5

PS5 is a general purpose input or output pin. It can be configured as the master output (during master mode) or slave input (during slave mode) pin MOSI of the Serial Peripheral Interface (SPI).

2.3.35 PS4 / MISO — Port S I/O Pin 4

PS4 is a general purpose input or output pin. It can be configured as master input (during master mode) or slave output (during slave mode) pin MISO for the Serial Peripheral Interface (SPI).

2.3.36 PS3 / TXD1 — Port S I/O Pin 3

PS3 is a general purpose input or output pin. It can be configured as transmit pin TXD1 of the Serial Communication Interface 1 (SCI1).

NOTE: *This pin is not available in the 112-pin LQFP version.*

2.3.37 PS2 / RXD1 — Port S I/O Pin 2

PS2 is a general purpose input or output pin. It can be configured as receive pin RXD1 of the Serial Communication Interface 1 (SCI1).

NOTE: *This pin is not available in the 112-pin LQFP version.*

2.3.38 PS1 / TXD0 — Port S I/O Pin 1

PS1 is a general purpose input or output pin. It can be configured as transmit pin TXD0 of the Serial Communication Interface 0 (SCI0).

2.3.39 PS0 / RXD0 — Port S I/O Pin 0

PS0 is a general purpose input or output pin. It can be configured as receive pin RXD0 of the Serial Communication Interface 0 (SCI0).

2.3.40 PT[7:4] / IOC[7:4] — Port T I/O Pins [7:4]

PT7-PT4 are general purpose input or output pins. They can be configured as input capture or output compare pins IOC7-IOC4 of the Timer (TIM).

2.3.41 PT[3:0] / IOC[3:0] / FP[27:24] — Port T I/O Pins [3:0]

PT3-PT0 are general purpose input or output pins. They can be configured as input capture or output compare pins IOC3-IOC0 of the Timer (TIM). They can be configured as frontplane segment driver outputs FP27-FP24 of the LCD module.

2.3.42 PU[7:4] / M1C1P, M1C1M, M1C0P, M1C0M — Port U I/O Pins [7:4]

PU7-PU4 are general purpose input or output pins. They can be configured as high current PWM output pins which can be used for motor drive. These pins interface to the coils of motor 1. PWM output on M1C0M results in a positive current flow through coil 0 when M1C0P is driven to a logic high state. PWM output on M1C1M results in a positive current flow through coil 1 when M1C1P is driven to a logic high state.

2.3.43 PU[3:0] / M0C1P, M0C1M, M0C0P, M0C0M — Port U I/O Pins [3:0]

PU3-PU0 are general purpose input or output pins. They can be configured as high current PWM output pins which can be used for motor drive. These pins interface to the coils of motor 0. PWM output on M0C0M results in a positive current flow through coil 0 when M0C0P is driven to a logic high state. PWM output on M0C1M results in a positive current flow through coil 1 when M0C1P is driven to a logic high state.

2.3.44 PV[7:4] / M3C1P, M3C1M, M3C0P, M3C0M — Port V I/O Pins [7:4]

PV7-PV4 are general purpose input or output pins. They can be configured as high current PWM output pins which can be used for motor drive. These pins interface to the coils of motor 3. PWM output on M3C0M results in a positive current flow through coil 0 when M3C0P is driven to a logic high state. PWM output on M3C1M results in a positive current flow through coil 1 when M3C1P is driven to a logic high state.

2.3.45 PV[3:0] / M2C1P, M2C1M, M2C0P, M2C0M — Port V I/O Pins [3:0]

PV3-PV0 are general purpose input or output pins. They can be configured as high current PWM output pins which can be used for motor drive. These pins interface to the coils of motor 2. PWM output on M2C0M results in a positive current flow through coil 0 when M2C0P is driven to a logic high state. PWM output on M2C1M results in a positive current flow through coil 1 when M2C1P is driven to a logic high state.

2.3.46 PW[7:4] / M5C1P, M5C1M, M5C0P, M5C0M — Port W I/O Pins [7:4]

PW7-PW4 are general purpose input or output pins. They can be configured as high current PWM output pins which can be used for motor drive. These pins interface to the coils of motor 5. PWM output on M5C0M results in a positive current flow through coil 0 when M5C0P is driven to a logic high state. PWM output on M5C1M results in a positive current flow through coil 1 when M5C1P is driven to a logic high state.

2.3.47 PW[3:0] / M4C1P, M4C1M, M4C0P, M4C0M — Port W I/O Pins [3:0]

PW3-PW0 are general purpose input or output pins. They can be configured as high current PWM output pins which can be used for motor drive. These pins interface to the coils of motor 4. PWM output on M4C0M results in a positive current flow through coil 0 when M4C0P is driven to a logic high state. PWM output on M4C1M results in a positive current flow through coil 1 when M4C1P is driven to a logic high state.

2.4 Power Supply Pins

MC9S12H256 power and ground pins are described below.

NOTE: *All VSS pins must be connected together in the application (**21.2 Recommended PCB layout**).*

*Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded (**Table 21-1**).*

2.4.1 VDDR — External Power Pin

VDDR is the power supply pin for the internal voltage regulator.

2.4.2 VDDX1, VDDX2, VSSX1, VSSX2 — External Power and Ground Pins

VDDX1, VDDX2, VSSX1 and VSSX2 are the power supply and ground pins for input/output drivers.VDDX1 and VDDX2 as well as VSSX1 and VSSX2 are not internally connected.

2.4.3 VDD1, VSS1, VSS2 — Core Power Pins

VDD1, VSS1 and VSS2 are the core power and ground pins and related to the voltage regulator output. These pins serve as connection points for filter capacitors. VSS1 and VSS2 are internally connected.

NOTE: *No load allowed except for bypass capacitors.*

2.4.4 VDDA, VSSA — Power Supply Pins for ATD and VREG

VDDA, VSSA are the power supply and ground pins for the voltage regulator and the analog to digital converter.

2.4.5 VDDM1, VDDM2, VDDM3 — Power Supply Pins for Motor 0 to 5

VDDM1, VDDM2 and VDDM3 are the supply pins for the ports U,V and W. VDDM1, VDDM2 and VDDM3 are internally connected.

2.4.6 VSSM1, VSSM2, VSSM3 — Ground Pins for Motor 0 to 5

VSSM1, VSSM2 and VSSM3 are the ground pins for the ports U,V and W. VSSM1, VSSM2 and VSSM3 are internally connected.

2.4.7 VLCD — Power Supply Reference Pin for LCD driver

VLCD is the voltage reference pin for the LCD driver. Adjusting the voltage on this pin will change the display contrast.

2.4.8 VRH, VRL — ATD Reference Voltage Input Pins

VRH and VRL are the voltage reference pins for the analog to digital converter.

2.4.9 VDDPLL, VSSPLL — Power Supply Pins for PLL

VDDPLL and VSSPLL are the PLL supply pins and serve as connection points for external loop filter components.

NOTE: *No load allowed except for bypass capacitors.*

Section 3 System Clock Description

3.1 Overview

The Clock and Reset Generator provides the internal clock signals for the core and all peripheral modules. **Figure 3-1** shows the clock connections from the CRG to all modules.

Consult the CRG Block User Guide for details on clock generation.

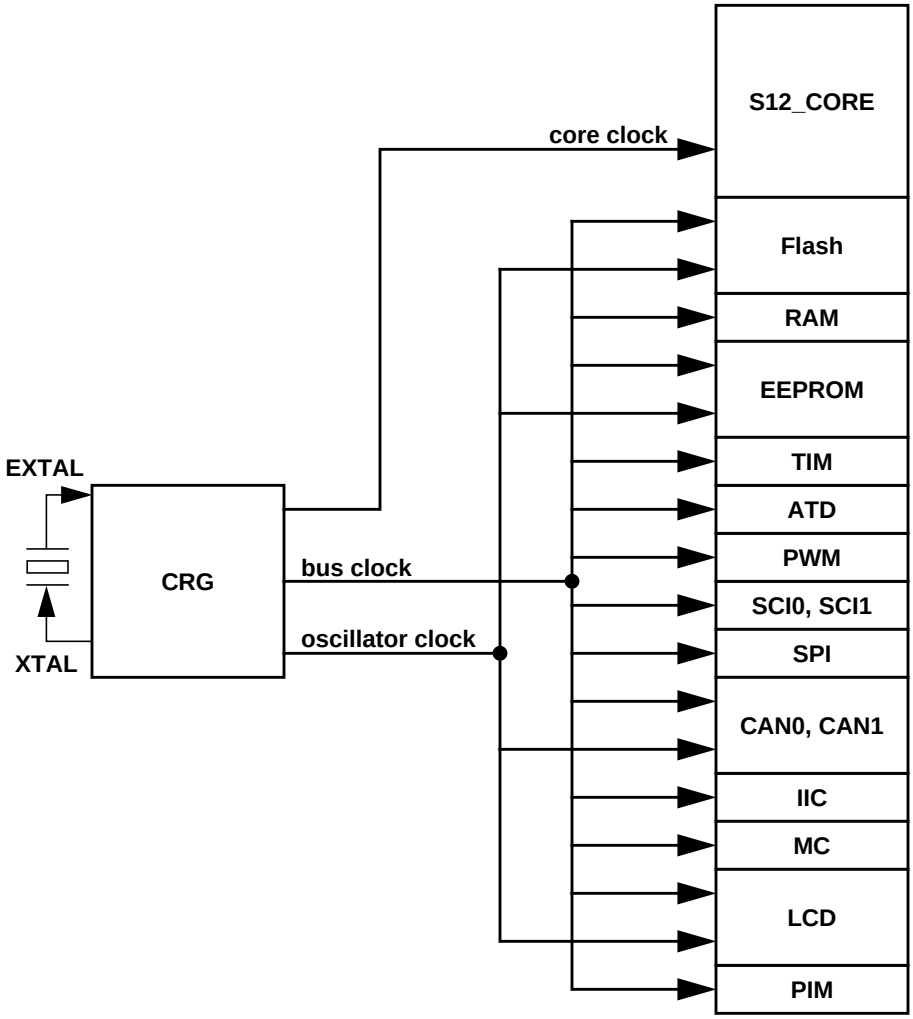


Figure 3-1 Clock Connections

Section 4 Modes of Operation

4.1 Overview

Eight possible modes determine the operating configuration of the MC9S12H256. Each mode has an associated default memory map and external bus configuration.

Three low power modes exist for the device.

4.2 Modes of Operation

The operating mode out of reset is determined by the states of the MODC, MODB, and MODA pins during reset (**Table 4-1**). The MODC, MODB, and MODA bits in the MODE register show the current operating mode and provide limited mode switching during operation. The states of the MODC, MODB, and MODA pins are latched into these bits on the rising edge of the reset signal.

Table 4-1 Mode Selection

MODC	MODB	MODA	Mode Description
0	0	0	Special Single Chip, BDM allowed and ACTIVE. BDM is allowed in all other modes but a serial command is required to make BDM active.
0	0	1	Emulation Expanded Narrow, BDM allowed
0	1	0	Special Test (Expanded Wide) (**Freescale Use Only**), BDM allowed
0	1	1	Emulation Expanded Wide, BDM allowed
1	0	0	Normal Single Chip, BDM allowed
1	0	1	Normal Expanded Narrow, BDM allowed
1	1	0	Peripheral (**Freescale Use Only**); BDM allowed but bus operations would cause bus conflicts (must not be used)
1	1	1	Normal Expanded Wide, BDM allowed

There are two basic types of operating modes:

1. Normal modes: Some registers and bits are protected against accidental changes.
2. Special modes: Allow greater access to protected control registers and bits for special purposes such as testing.

A system development and debug feature, background debug mode (BDM), is available in all modes. In special single-chip mode, BDM is active immediately after reset.

Some aspects of Port E are not mode dependent. Bit 1 of Port E is a general purpose input or the $\overline{IRQ}$ interrupt input. $\overline{IRQ}$ can be enabled by bits in the CPU's condition codes register but it is inhibited at reset so this pin is initially configured as a simple input with a pull-up. Bit 0 of Port E is a general purpose input or the $\overline{XIRQ}$ interrupt input. $\overline{XIRQ}$ can be enabled by bits in the CPU's condition codes register but it is inhibited at reset so this pin is initially configured as a simple input with a pull-up. The ESTR bit in the EBICTL register is set to one by reset in any user mode. This assures that the reset vector can be fetched

even if it is located in an external slow memory device. The PE6/MODB/IPIPE1 and PE5/MODA/IPIPE0 pins act as high-impedance mode select inputs during reset.

The following paragraphs discuss the default bus setup and describe which aspects of the bus can be changed after reset on a per mode basis.

4.2.1 Normal Operating Modes

These modes provide three operating configurations. Background debug is available in all three modes, but must first be enabled for some operations by means of a BDM background command, then activated.

4.2.1.1 Normal Single-Chip Mode

There is no external expansion bus in this mode. All pins of Ports A, B and E are configured as general purpose I/O pins Port E bits 1 and 0 are available as general purpose input only pins with internal pull-ups enabled. All other pins of Port E are bidirectional I/O pins that are initially configured as high-impedance inputs with internal pull-ups enabled. Ports A and B are configured as high-impedance inputs with their internal pull-ups disabled.

The pins associated with Port E bits 6, 5, 3, and 2 cannot be configured for their alternate functions IPIPE1, IPIPE0, $\overline{\text{LSTRB}}$, and R/$\overline{\text{W}}$ while the MCU is in single chip modes. In single chip modes, the associated control bits PIPOE, LSTRE, and RDWE are reset to zero. Writing the opposite state into them in single chip mode does not change the operation of the associated Port E pins.

In normal single chip mode, the MODE register is writable one time. This allows a user program to change the bus mode to narrow or wide expanded mode and/or turn on visibility of internal accesses.

Port E, bit 4 can be configured for a free-running E clock output by clearing NECLK=0. Typically the only use for an E clock output while the MCU is in single chip modes would be to get a constant speed clock for use in the external application system.

4.2.1.2 Normal Expanded Wide Mode

In expanded wide modes, Ports A and B are configured as a 16-bit multiplexed address and data bus and Port E bit 4 is configured as the E clock output signal. These signals allow external memory and peripheral devices to be interfaced to the MCU.

Port E pins other than PE4/ECLK are configured as general purpose I/O pins (initially high-impedance inputs with internal pull-up resistors enabled). Control bits PIPOE, NECLK, LSTRE, and RDWE in the PEAR register can be used to configure Port E pins to act as bus control outputs instead of general purpose I/O pins.

It is possible to enable the pipe status signals on Port E bits 6 and 5 by setting the PIPOE bit in PEAR, but it would be unusual to do so in this mode. Development systems where pipe status signals are monitored would typically use the special variation of this mode.

The Port E bit 2 pin can be reconfigured as the R/$\overline{\text{W}}$ bus control signal by writing “1” to the RDWE bit in PEAR. If the expanded system includes external devices that can be written, such as RAM, the RDWE bit

would need to be set before any attempt to write to an external location. If there are no writable resources in the external system, PE2 can be left as a general purpose I/O pin. The

Port E bit 3 pin can be reconfigured as the $\overline{\text{LSTRB}}$ bus control signal by writing “1” to the LSTRE bit in PEAR. The default condition of this pin is a general purpose input because the $\overline{\text{LSTRB}}$ function is not needed in all expanded wide applications.

The Port E bit 4 pin is initially configured as ECLK output with stretch. The E clock output function depends upon the settings of the NECLK bit in the PEAR register, the IVIS bit in the MODE register and the ESTR bit in the EBICTL register. The E clock is available for use in external select decode logic or as a constant speed clock for use in the external application system.

4.2.1.3 Normal Expanded Narrow Mode

This mode is used for lower cost production systems that use 8-bit wide external EPROMs or RAMs. Such systems take extra bus cycles to access 16-bit locations but this may be preferred over the extra cost of additional external memory devices.

Ports A and B are configured as a 16-bit address bus and Port A is multiplexed with data. Internal visibility is not available in this mode because the internal cycles would need to be split into two 8-bit cycles.

Since the PEAR register can only be written one time in this mode, use care to set all bits to the desired states during the single allowed write.

The PE3/$\overline{\text{LSTRB}}$ pin is always a general purpose I/O pin in normal expanded narrow mode. Although it is possible to write the LSTRE bit in PEAR to “1” in this mode, the state of LSTRE is overridden and Port E bit 3 cannot be reconfigured as the $\overline{\text{LSTRB}}$ output.

It is possible to enable the pipe status signals on Port E bits 6 and 5 by setting the PIPOE bit in PEAR, but it would be unusual to do so in this mode. LSTRB would also be needed to fully understand system activity. Development systems where pipe status signals are monitored would typically use special expanded wide mode or occasionally special expanded narrow mode.

The PE4/ECLK pin is initially configured as ECLK output with stretch. The E clock output function depends upon the settings of the NECLK bit in the PEAR register, the IVIS bit in the MODE register and the ESTR bit in the EBICTL register. In normal expanded narrow mode, the E clock is available for use in external select decode logic or as a constant speed clock for use in the external application system.

The PE2/R/W pin is initially configured as a general purpose input with a pull-up but this pin can be reconfigured as the R/$\overline{\text{W}}$ bus control signal by writing “1” to the RDWE bit in PEAR. If the expanded narrow system includes external devices that can be written such as RAM, the RDWE bit would need to be set before any attempt to write to an external location. If there are no writable resources in the external system, PE2 can be left as a general purpose I/O pin.

4.2.1.4 Internal Visibility

Internal visibility is available when the MCU is operating in expanded wide modes or special narrow mode. It is not available in single-chip, peripheral or normal expanded narrow modes. Internal visibility is enabled by setting the IVIS bit in the MODE register.

If an internal access is made while E, R/$\overline{W}$, and $\overline{LSTRB}$ are configured as bus control outputs and internal visibility is off (IVIS=0), E will remain low for the cycle, R/$\overline{W}$ will remain high, and address, data and the $\overline{LSTRB}$ pins will remain at their previous state.

When internal visibility is enabled (IVIS=1), certain internal cycles will be blocked from going external. During cycles when the BDM is selected, R/$\overline{W}$ will remain high, data will maintain its previous state, and address and $\overline{LSTRB}$ pins will be updated with the internal value. During CPU no access cycles when the BDM is not driving, R/$\overline{W}$ will remain high, and address, data and the $\overline{LSTRB}$ pins will remain at their previous state.

4.2.1.5 Emulation Expanded Wide Mode

In expanded wide modes, Ports A and B are configured as a 16-bit multiplexed address and data bus and Port E provides bus control and status signals. These signals allow external memory and peripheral devices to be interfaced to the MCU. These signals can also be used by a logic analyzer to monitor the progress of application programs.

The bus control related pins in Port E (PE7/NOACC, PE6/MODB/IPIPE1, PE5/MODA/IPIPE0, PE4/ECLK, PE3/$\overline{LSTRB}$/$\overline{TAGLO}$, and PE2/R/$\overline{W}$) are all configured to serve their bus control output functions rather than general purpose I/O. Notice that writes to the bus control enable bits in the PEAR register in special mode are restricted.

4.2.1.6 Emulation Expanded Narrow Mode

Expanded narrow modes are intended to allow connection of single 8-bit external memory devices for lower cost systems that do not need the performance of a full 16-bit external data bus. Accesses to internal resources that have been mapped external (i.e. PORTA, PORTB, DDRA, DDRB, PORTE, DDRE, PEAR, PUCR, RDRIV) will be accessed with a 16-bit data bus on Ports A and B. Accesses of 16-bit external words to addresses which are normally mapped external will be broken into two separate 8-bit accesses using Port A as an 8-bit data bus. Internal operations continue to use full 16-bit data paths. They are only visible externally as 16-bit information if IVIS=1.

Ports A and B are configured as multiplexed address and data output ports. During external accesses, address A15, data D15 and D7 are associated with PA7, address A0 is associated with PB0 and data D8 and D0 are associated with PA0. During internal visible accesses and accesses to internal resources that have been mapped external, address A15 and data D15 is associated with PA7 and address A0 and data D0 is associated with PB0.

The bus control related pins in Port E (PE7/NOACC, PE6/MODB/IPIPE1, PE5/MODA/IPIPE0, PE4/ECLK, PE3/$\overline{LSTRB}$/$\overline{TAGLO}$, and PE2/R/$\overline{W}$) are all configured to serve their bus control output functions rather than general purpose I/O. Notice that writes to the bus control enable bits in the PEAR register in special mode are restricted.

4.2.2 Special Operating Modes

There are two special operating modes that correspond to normal operating modes. These operating modes are commonly used in factory testing and system development.

4.2.2.1 Special Single-Chip Mode

When the MCU is reset in this mode, the background debug mode is enabled and active. The MCU does not fetch the reset vector and execute application code as it would in other modes. Instead the active background mode is in control of CPU execution and BDM firmware is waiting for additional serial commands through the BKGD pin. When a serial command instructs the MCU to return to normal execution, the system will be configured as described below unless the reset states of internal control registers have been changed through background commands after the MCU was reset.

There is no external expansion bus after reset in this mode. Ports A and B are initially simple bidirectional I/O pins that are configured as high-impedance inputs with internal pull-ups disabled; however, writing to the mode select bits in the MODE register (which is allowed in special modes) can change this after reset. All of the Port E pins (except PE4/ECLK) are initially configured as general purpose high-impedance inputs with pull-ups enabled. PE4/ECLK is configured as the E clock output in this mode.

The pins associated with Port E bits 6, 5, 3, and 2 cannot be configured for their alternate functions IPIPE1, IPIPE0, $\overline{\text{LSTRB}}$, and R/$\overline{\text{W}}$ while the MCU is in single chip modes. In single chip modes, the associated control bits PIPOE, LSTRE and RDWE are reset to zero. Writing the opposite value into these bits in single chip mode does not change the operation of the associated Port E pins.

Port E, bit 4 can be configured for a free-running E clock output by clearing NECLK=0. Typically the only use for an E clock output while the MCU is in single chip modes would be to get a constant speed clock for use in the external application system.

4.2.2.2 Special Test Mode (Freescale Use Only)

In expanded wide modes, Ports A and B are configured as a 16-bit multiplexed address and data bus and Port E provides bus control and status signals. In special test mode, the write protection of many control bits is lifted so that they can be thoroughly tested without needing to go through reset.

4.2.3 Test Operating Mode (Freescale Use Only)

There is a test operating mode in which an external master, such as an I.C. tester, can control the on-chip peripherals.

4.2.3.1 Peripheral Mode

This mode is intended for Freescale factory testing of the MCU. In this mode, the CPU is inactive and an external (tester) bus master drives address, data and bus control signals in through Ports A, B and E. In effect, the whole MCU acts as if it was a peripheral under control of an external CPU. This allows faster testing of on-chip memory and peripherals than previous testing methods. Since the mode control register is not accessible in peripheral mode, the only way to change to another mode is to reset the MCU into a different mode. Background debugging should not be used while the MCU is in special peripheral mode as internal bus conflicts between BDM and the external master can cause improper operation of both functions.

4.3 Security

The device will make available a security feature preventing the unauthorized read and write of the memory contents. This feature allows:

- Protection of the contents of FLASH,
- Protection of the contents of EEPROM,
- Operation in single-chip mode,
- Operation from external memory with internal FLASH and EEPROM disabled.

The user must be reminded that part of the security must lie with the user's code. An extreme example would be user's code that dumps the contents of the internal program. This code would defeat the purpose of security. At the same time the user may also wish to put a back door in the user's program. An example of this is the user downloads a key through the SCI which allows access to a programming routine that updates parameters stored in EEPROM.

4.3.1 Securing the Microcontroller

Once the user has programmed the FLASH and EEPROM (if desired), the part can be secured by programming the security bits located in the FLASH module. These non-volatile bits will keep the part secured through resetting the part and through powering down the part.

The security byte resides in a portion of the Flash array.

Check the Flash Block User Guide for more details on the security configuration.

4.3.2 Operation of the Secured Microcontroller

4.3.2.1 Normal Single Chip Mode

This will be the most common usage of the secured part. Everything will appear the same as if the part was not secured with the exception of BDM operation. The BDM operation will be blocked.

4.3.2.2 Executing from External Memory

The user may wish to execute from external space with a secured microcontroller. This is accomplished by resetting directly into expanded mode. The internal FLASH and EEPROM will be disabled. BDM operations will be blocked.

4.3.3 Unsecuring the Microcontroller

In order to unsecure the microcontroller, the internal FLASH and EEPROM must be erased. This can be done through an external program in expanded mode.

Once the user has erased the FLASH and EEPROM, the part can be reset into special single chip mode. This invokes a program that verifies the erasure of the internal FLASH and EEPROM. Once this program

completes, the user can erase and program the FLASH security bits to the unsecured state. This is generally done through the BDM, but the user could also change to expanded mode (by writing the mode bits through the BDM) and jumping to an external program (again through BDM commands). Note that if the part goes through a reset before the security bits are reprogrammed to the unsecure state, the part will be secured again.

4.4 Low Power Modes

Consult the respective Block User Guide for information on the module behavior in Stop, Pseudo Stop, and Wait Mode.

Section 5 Resets and Interrupts

5.1 Overview

Consult the Exception Processing section of the HCS12 Core User Guide for information on resets and interrupts.

5.2 Vectors

5.2.1 Vector Table

Table 5-1 lists interrupt sources and vectors in default order of priority.

Table 5-1 Reset and Interrupt Vector Table

Vector Address	Interrupt Source	CCR Mask	Local Enable	HPRIO Value to Elevate
$FFFE, $FFFF	External or Power On Reset	None	None	-
$FFFC, $FFFD	Clock Monitor fail reset	None	COPCTL (CME, FCME)	-
$FFFA, $FFFB	COP failure reset	None	COP rate select	-
$FFF8, $FFF9	Unimplemented instruction trap	None	None	-
$FFF6, $FFF7	SWI	None	None	-
$FFF4, $FFF5	$\overline{\text{XIRQ}}$	X-Bit	None	-
$FFF2, $FFF3	$\overline{\text{IRQ}}$	I-Bit	INTCR (IRQEN)	$F2
$FFF0, $FFF1	Real Time Interrupt	I-Bit	RTICTL (RTIE)	$F0
$FFEE, $FFEF	Timer channel 0	I-Bit	TIE (C0I)	$EE
$FFEC, $FFED	Timer channel 1	I-Bit	TIE (C1I)	$EC
$FFEA, $FFEB	Timer channel 2	I-Bit	TIE (C2I)	$EA
$FFE8, $FFE9	Timer channel 3	I-Bit	TIE (C3I)	$E8
$FFE6, $FFE7	Timer channel 4	I-Bit	TIE (C4I)	$E6
$FFE4, $FFE5	Timer channel 5	I-Bit	TIE (C5I)	$E4
$FFE2, $FFE3	Timer channel 6	I-Bit	TIE (C6I)	$E2
$FFE0, $FFE1	Timer channel 7	I-Bit	TIE (C7I)	$E0
$FFDE, $FFDF	Timer overflow	I-Bit	TSCR2 (TOI)	$DE
$FFDC, $FFDD	Pulse accumulator A overflow	I-Bit	PACTL (PAOVI)	$DC
$FFDA, $FFDB	Pulse accumulator input edge	I-Bit	PACTL (PAI)	$DA
$FFD8, $FFD9	SPI	I-Bit	SPICR1 (SPIE)	$D8
$FFD6, $FFD7	SCI0	I-Bit	SC0CR2 (TIE, TCIE, RIE, ILIE)	$D6
$FFD4, $FFD5	SCI1	I-Bit	SC1CR2 (TIE, TCIE, RIE, ILIE)	$D4
$FFD2, $FFD3	ATD	I-Bit	ATDCTL2 (ASCIE)	$D2
$FFD0, $FFD1	Reserved			
$FFCE, $FFCF	Port J	I-Bit	PTJIF (PTJIE)	$CE
$FFCC, $FFCD	Port H	I-Bit	PTHIF (PTHIE)	$CC
$FFCA, $FFCB	Reserved			

Table 5-1 Reset and Interrupt Vector Table

Vector Address	Interrupt Source	CCR Mask	Local Enable	HPRIO Value to Elevate
$FFC8, $FFC9	Reserved			
$FFC6, $FFC7	CRG PLL lock	I-Bit	CRGINT (LOCKIE)	$C6
$FFC4, $FFC5	CRG Self Clock Mode	I-Bit	CRGINT (SCMIE)	$C4
$FFC2, $FFC3	Reserved			
$FFC0, $FFC1	IIC Bus	I-Bit	IBCR (IBIE)	$C0
$FFBE, $FFBF	Reserved			
$FFBC, $FFBD	Reserved			
$FFBA, $FFBB	EEPROM	I-Bit	EECTL (CCIE, CBEIE)	$BA
$FFB8, $FFB9	FLASH	I-Bit	FCTL (CCIE, CBEIE)	$B8
$FFB6, $FFB7	CAN0 wake-up	I-Bit	CAN0RIER (WUPIE)	$B6
$FFB4, $FFB5	CAN0 errors	I-Bit	CAN0RIER (CSCIE, OVRIE)	$B4
$FFB2, $FFB3	CAN0 receive	I-Bit	CAN0RIER (RXFIE)	$B2
$FFB0, $FFB1	CAN0 transmit	I-Bit	CAN0TIER (TXEIE[2:0])	$B0
$FFAE, $FFAF	CAN1 wake-up	I-Bit	CAN0RIER (WUPIE)	$AE
$FFAC, $FFAD	CAN1 errors	I-Bit	CAN1RIER (CSCIE, OVRIE)	$AC
$FFAA, $FFAB	CAN1 receive	I-Bit	CAN1RIER (RXFIE)	$AA
$FFA8, $FFA9	CAN1 transmit	I-Bit	CAN1TIER (TXEIE[2:0])	$A8
$FF98 to $FFA7	Reserved			
$FF96, $FF97	Motor Control Timer Overflow	I-Bit	MCCTL1 (MCOCIE)	$96
$FF9E to $FF95	Reserved			
$FF8C, $FF8D	PWM Emergency Shutdown	I-Bit	PWMSDN(PWMIE)	$8C
$FF80 to $FF8B	Reserved			

5.3 Effects of Reset

When a reset occurs, MCU registers and control bits are changed to known start-up states. Refer to the respective module Block User Guides for register reset states.

5.3.1 I/O pins

Refer to the HCS12 Core User Guides for mode dependent pin configuration of port A, B, E and K out of reset.

Refer to the PIM Block User Guide for reset configurations of all peripheral module ports.

NOTE: *For devices assembled in 112-pin LQFP packages all non-bonded out pins should be configured as outputs after reset in order to avoid current drawn from floating inputs. Refer to* ***Table 2-1*** *for affected pins.*

5.3.2 Memory

Refer to **Table 1-1** for locations of the memories depending on the operating mode after reset

The RAM array is not automatically initialized out of reset.

Section 6 HCS12 Core Block Description

Consult the HCS12 Core User Guide for information about the HCS12 core modules, i.e. central processing unit (CPU), interrupt module (INT), module mapping control module (MMC), multiplexed external bus interface (MEBI), breakpoint module (BKP) and background debug mode module (BDM).

Section 7 Clock and Reset Generator (CRG) Block Description

Consult the CRG Block User Guide for information about the Clock and Reset Generator module.

7.1 Device-specific information

7.1.1 XCLKS

The XCLKS input signal is active high (see **2.3.10 PE7 / FP22 / XCLKS / NOACC — Port E I/O Pin 7**).

Section 8 Timer (TIM) Block Description

Consult the TIM_16B8C Block User Guide for information about the Timer module.

Section 9 Analog to Digital Converter (ATD) Block Description

Consult the ATD_10B16C Block User Guide for information about the Analog to Digital Converter module.

Section 10 Inter-IC Bus (IIC) Block Description

Consult the IIC Block User Guide for information about the Inter-IC Bus module.

Section 11 Serial Communications Interface (SCI) Block Description

There are two Serial Communications Interfaces (SCI0 and SCI1) implemented on the MC9S12H256 device and one SCI (SCI0) on MC9S12H128. Consult the SCI Block User Guide for information about each Serial Communications Interface module.

Section 12 Serial Peripheral Interface (SPI) Block Description

Consult the SPI Block User Guide for information about the Serial Peripheral Interface module.

Section 13 Pulse Width Modulator (PWM) Block Description

Consult the PWM_8B6C Block User Guide for information about the Pulse Width Modulator module.

Section 14 Flash EEPROM 256K Block Description

Consult the FTS256K Block User Guide for information about the flash module.

Section 15 EEPROM 4K Block Description

Consult the EETS4K Block User Guide for information about the EEPROM module.

Section 16 RAM Block Description

The RAM module does not contain any control registers. Thus no Block User Guide is available.

This module supports single-cycle misaligned word accesses without wait states.

Section 17 Liquid Crystal Display Driver (LCD) Block Description

Consult the LCD_32F4B Block User Guide for information about the Liquid Crystal Display Driver module.

Section 18 MSCAN Block Description

There are two MSCAN modules (CAN0 and CAN1) implemented on the MC9S12H256 device. Consult the MSCAN Block User Guide for information on each MSCAN.

Section 19 PWM Motor Control (MC) Block Description

Consult the MC_10B12C Block User Guide for information about the PWM Motor Control module.

Section 20 Port Integration Module (PIM) Block Description

Consult the PIM_9H256 Block User Guide for information about the Port Integration Module.

Section 21 Voltage Regulator (VREG) Block Description

Consult the VREG Block User Guide for information about the dual output linear voltage regulator.

21.1 Device-specific information

21.1.1 VREGEN

There is no VREGEN pin implemented on this device.

21.1.2 Modes of Operation

21.1.2.1 Run Mode

VREG enters run mode whenever the CPU is neither in Stop nor in Pseudo Stop mode. Both regulating loops operate in Run mode with full performance.

21.1.2.2 Standby Mode

VREG enters Standby mode when the CPU operates either in Stop or in Pseudo Stop mode. The supply of the core logic as well as the oscillators are derived from two voltage clamps. Standby mode minimizes quiescent current drawn by the voltage regulator block.

21.1.2.3 Shutdown Mode

VREG Shutdown mode is not available on MC9S12H family devices.

21.2 Recommended PCB layout

Figure 21-1 LQFP112 recommended PCB layout

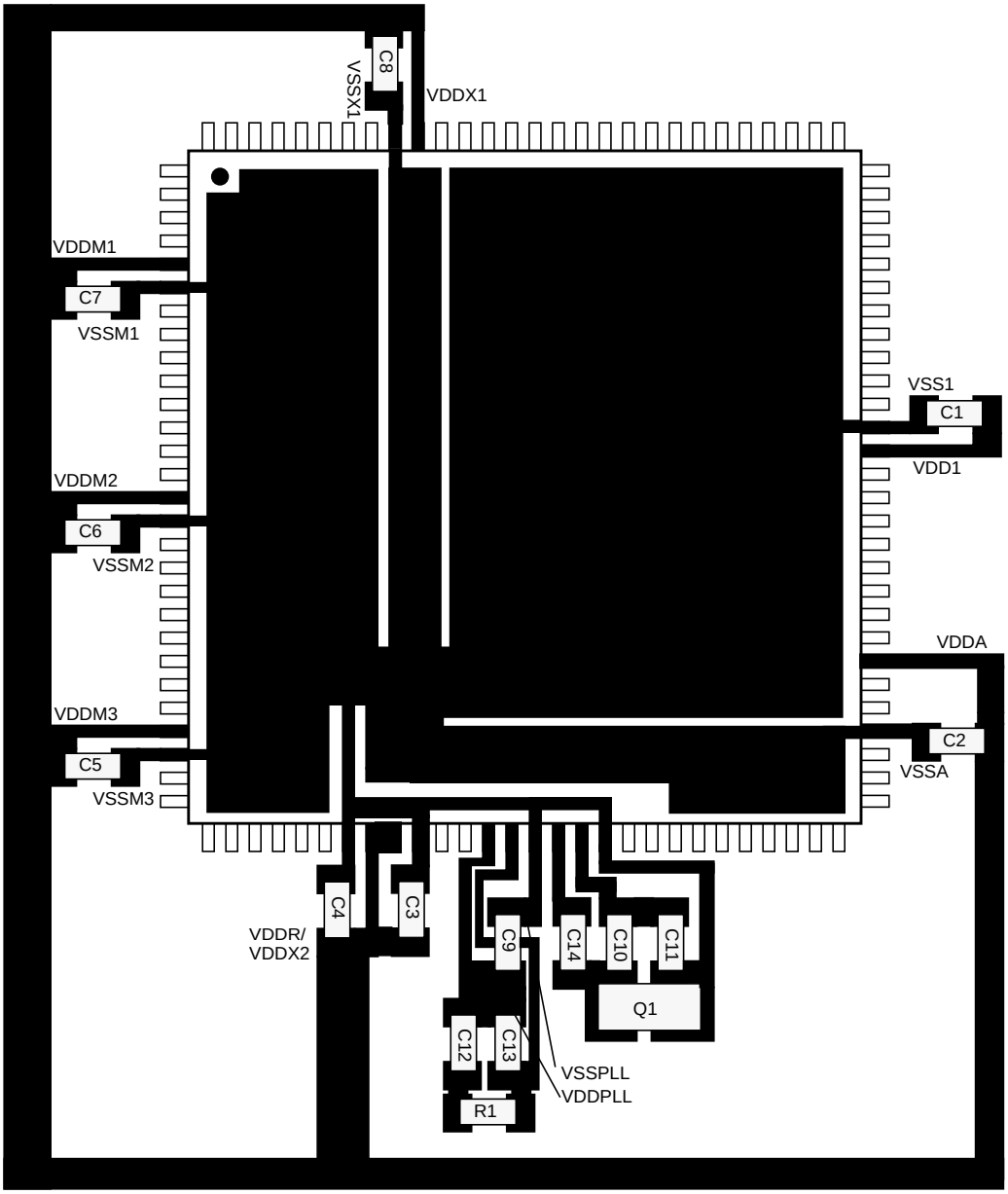


Figure 21-2 LQFP144 recommended PCB layout

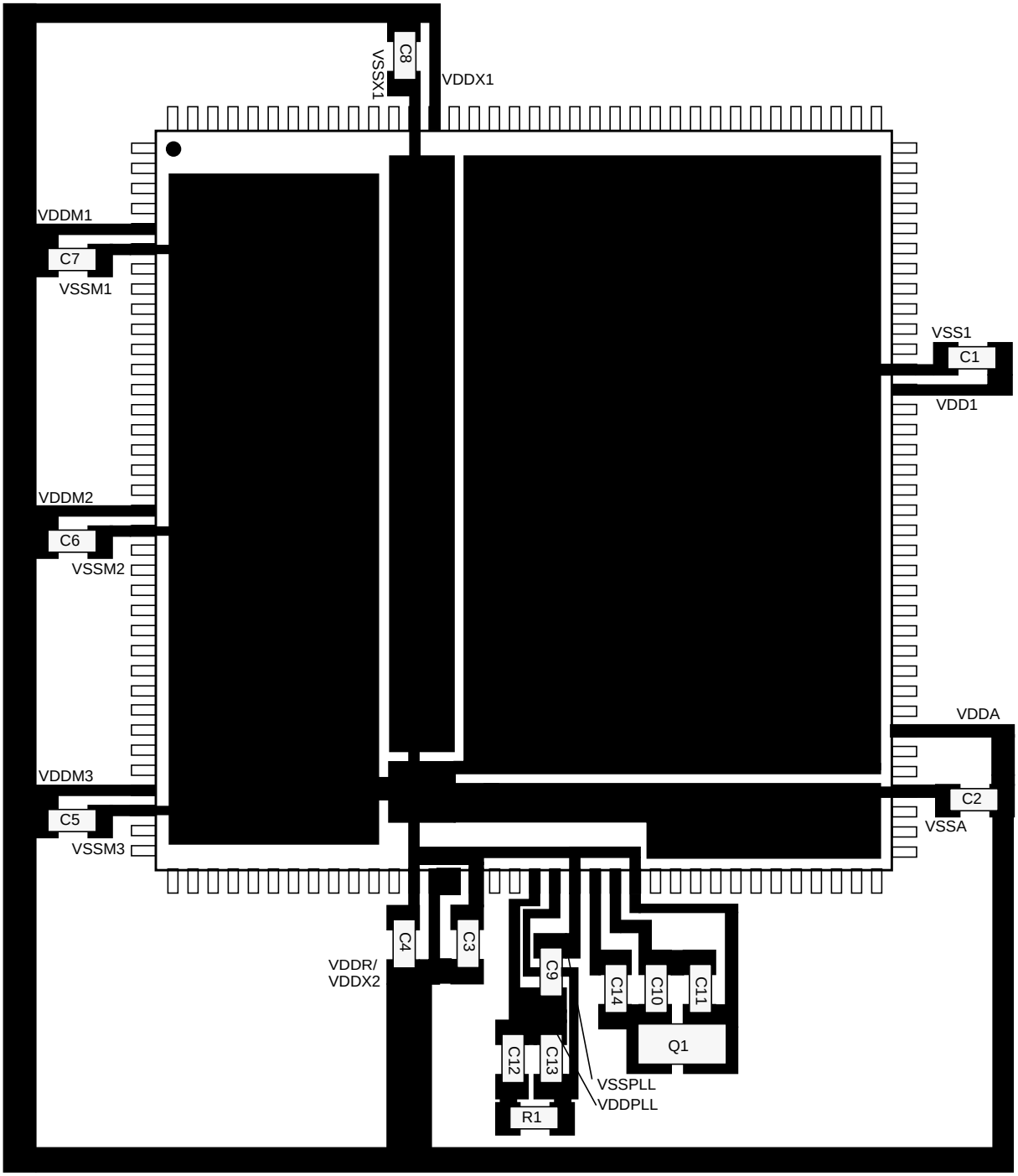


Table 21-1 Recommended Components

Component	Purpose	Type	Value
C1	VDD1 filter cap	ceramic X7R	100 .. 220nF
C2	VDDA filter cap	X7R/tantalum	>=100nF
C3	VDDX2 filter cap	X7R/tantalum	>=100nF
C4	VDDR filter cap	X7R/tantalum	>=100nF
C5	VDDM3 filter cap	X7R/tantalum	>=100nF
C6	VDDM2 filter cap	X7R/tantalum	>=100nF
C7	VDDM1 filter cap	X7R/tantalum	>=100nF
C8	VDDX1 filter cap	X7R/tantalum	>=100nF
C9	VDDPLL filter cap	ceramic X7R	100nF .. 220nF
C10	OSC load cap	See CRG Block User Guide	
C11	OSC load cap		
C12	PLL loop filter cap		
C13	PLL loop filter cap		
C14	DC cutoff cap		
R1	PLL loop filter res		
Q1	Quartz/Resonator		

The PCB must be carefully laid out to ensure proper operation of the voltage regulator as well as of the MCU itself. The following rules must be observed:

- Every supply pair must be decoupled by a ceramic/tantalum capacitor connected as near as possible to the corresponding pins(C1 – C9).
- Central point of the ground star should be the VSS1 pin.
- Use low ohmic low inductance connections between VSS1, VSS2, VSSA, VSSX1,2 and VSSM1,2,3.
- VSSPLL must be directly connected to VSS1.
- Keep traces of VSSPLL, EXTAL and XTAL as short as possible and occupied board area for C10, C11, C14 and Q1 as small as possible.
- Do not place other signals or supplies underneath area occupied by C10, C11, C14 and Q1 and the connection area to the MCU.
- Central power input should be fed in at the VDDA/VSSA pins.

Appendix A Electrical Characteristics

A.1 General

This supplement contains the most accurate electrical information for the MC9S12H256 and MC9S12H128 microcontroller available at the time of publication.

This introduction is intended to give an overview on several common topics like power supply, current injection etc.

A.1.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate.

NOTE: *This classification is shown in the column labeled "C" in the parameter tables where appropriate.*

P:

Those parameters are guaranteed during production testing on each individual device.

C:

Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.

T:

Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.

D:

Those parameters are derived mainly from simulations.

A.1.2 Power Supply

The MC9S12H256 utilizes several pins to supply power to the I/O ports, A/D converter, oscillator and PLL as well as the digital core.

The VDDA, VSSA pair supplies the A/D converter and the resistor ladder of the internal voltage regulator.

The VDDX1/VSSX1 and VDDX2/VSSX2 pairs supply the I/O pins except PH, PU, PV and PW. VDDR supplies the internal voltage regulator.

VDDM1/VSSM1, VDDM2/VSSM2 and VDDM3/VSSM3 pairs supply the ports PH, PU, PV and PW.

VDD1, VSS1 and VSS2 are the supply pins for the digital logic, VDDPLL, VSSPLL supply the oscillator and the PLL.

VSS1 and VSS2 are internally connected by metal.

VDDA, VDDX1, VDDX2, VDDM as well as VSSA, VSSX1, VSSX2 and VSSM are connected by anti-parallel diodes for ESD protection.

NOTE: *In the following context VDD5 is used for either VDDA, VDDM, VDDR and VDDX1/2; VSS5 is used for either VSSA, VSSR and VSSX unless otherwise noted. IDD5 denotes the sum of the currents flowing into the VDDA, VDDX1/2, VDDM and VDDR pins.*
VDD is used for VDD1 and VDDPLL, VSS is used for VSS1, VSS2 and VSSPLL. IDD is used for the sum of the currents flowing into VDD1 and VDDPLL.

A.1.3 Pins

There are four groups of functional pins.

A.1.3.1 5V I/O pins

Those I/O pins have a nominal level of 5V. This class of pins is comprised of all port I/O pins, the analog inputs, BKGD and the RESET pins.The internal structure of all those pins is identical, however some of the functionality may be disabled. E.g. for the analog inputs the output drivers, pull-up and pull-down resistors are disabled permanently.

A.1.3.2 Analog Reference

This group is made up by the VRH and VRL pins.

A.1.3.3 Oscillator

The pins XFC, EXTAL, XTAL dedicated to the oscillator have a nominal 2.5V level. They are supplied by VDDPLL.

A.1.3.4 TEST

This pin is used for production testing only.

A.1.4 Current Injection

Power supply must maintain regulation within operating V_{DD5} or V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD5}$) is greater than I_{DD5}, the injection current may flow out of VDD5 and could result in external power supply going out of regulation. Ensure external VDD5 load will shunt current greater than maximum injection current. This will be the

greatest risk when the MCU is not consuming power; e.g. if no system clock is present, or if clock rate is very low which would reduce overall power consumption.

A.1.5 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only. A functional operation under or outside those maxima is not guaranteed. Stress beyond those limits may affect the reliability or cause permanent damage of the device.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS5} or V_{DD5}).

Table A-1 Absolute Maximum Ratings[1]

Num	Rating	Symbol	Min	Max	Unit
1	I/O, Regulator and Analog Supply Voltage	V_{DD5}	–0.3	6.0	V
2	Digital Logic Supply Voltage [2]	V_{DD}	–0.3	3.0	V
3	PLL Supply Voltage [2]	V_{DDPLL}	–0.3	3.0	V
4	Voltage difference VDDX1 to VDDX2 to VDDM and VDDA	Δ_{VDDX}	–0.3	0.3	V
5	Voltage difference VSSX to VSSR and VSSA	Δ_{VSSX}	–0.3	0.3	V
6	Digital I/O Input Voltage	V_{IN}	–0.3	6.0	V
7	Analog Reference	V_{RH}, V_{RL}	–0.3	6.0	V
8	XFC, EXTAL, XTAL inputs	V_{ILV}	–0.3	3.0	V
9	TEST input	V_{TEST}	–0.3	10.0	V
10	Instantaneous Maximum Current Single pin limit for all digital I/O pins except PU, PV and PW [3]	I_D	–25	+25	mA
11	Instantaneous Maximum Current Single pin limit for Port PU, PV and PW [4]	I_D	–55	+55	mA
12	Instantaneous Maximum Current Single pin limit for XFC, EXTAL, XTAL[5]	I_{DL}	–25	+25	mA
13	Instantaneous Maximum Current Single pin limit for TEST [6]	I_{DT}	–0.25	0	mA
14	Storage Temperature Range	T_{stg}	– 65	155	°C

NOTES:
1. Beyond absolute maximum ratings device might be damaged.
2. The device contains an internal voltage regulator to generate the logic and PLL supply out of the I/O supply. The absolute maximum ratings apply when the device is powered from an external source.
3. All digital I/O pins are internally clamped to $V_{SSX1/2}$ and $V_{DDX1/2}$, V_{SSM} and V_{DDM} or V_{SSA} and V_{DDA}.
4. Ports PU, PV, PW are internally clamped to V_{SSM} and V_{DDM}.

5. Those pins are internally clamped to V_{SSPLL} and V_{DDPLL}.
6. This pin is clamped low to V_{SSPLL}, but not clamped high. This pin must be tied low in applications.

A.1.6 ESD Protection and Latch-up Immunity

All ESD testing is in conformity with CDF-AEC-Q100 Stress test qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the Human Body Model (HBM), the Machine Model (MM) and the Charge Device Model.

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table A-2 ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ω
	Storage Capacitance	C	100	pF
	Number of Pulse per pin positive negative	–	– 3 3	
Machine	Series Resistance	R1	0	Ω
	Storage Capacitance	C	200	pF
	Number of Pulse per pin positive negative	–	– 3 3	
Latch-up	Minimum input voltage limit		–2.5	V
	Maximum input voltage limit		7.5	V

Table A-3 ESD and Latch-Up Protection Characteristics

Num	C	Rating	Symbol	Min	Max	Unit
1	C	Human Body Model (HBM)	V_{HBM}	2000	–	V
2	C	Machine Model (MM)	V_{MM}	200	–	V
3	C	Charge Device Model (CDM)	V_{CDM}	500	–	V
4	C	Latch-up Current at T_A = 125°C positive negative	I_{LAT}	+100 –100	–	mA
5	C	Latch-up Current at T_A = 27°C positive negative	I_{LAT}	+200 –200	–	mA

A.1.7 Operating Conditions

This chapter describes the operating conditions of the device. Unless otherwise noted those conditions apply to all the following data.

NOTE: *Please refer to the temperature rating of the device (C, V, M) with regards to the ambient temperature T_A and the junction temperature T_J. For power dissipation calculations refer to* ***Section A.1.8 Power Dissipation and Thermal Characteristics****.*

Table A-4 Operating Conditions

Rating	Symbol	Min	Typ	Max	Unit
I/O, Regulator and Analog Supply Voltage	V_{DD5}	4.5	5	5.25	V
Digital Logic Supply Voltage [1]	V_{DD}	2.35	2.5	2.75	V
PLL Supply Voltage [2]	V_{DDPLL}	2.35	2.5	2.75	V
Voltage Difference VDDX to VDDR and VDDA	Δ_{VDDX}	–0.1	0	0.1	V
Voltage Difference VSSX to VSSR and VSSA	Δ_{VSSX}	–0.1	0	0.1	V
Oscillator	f_{osc}	0.5	–	16	MHz
Bus Frequency	f_{bus}	0.5	–	16	MHz
MC9S12H256**C**, MC9S12H128**C**					
Operating Junction Temperature Range	T_J	–40	–	100	°C
Operating Ambient Temperature Range [2]	T_A	–40	27	85	°C
MC9S12H256**V**, MC9S12H128**V**					
Operating Junction Temperature Range	T_J	–40	–	120	°C
Operating Ambient Temperature Range [2]	T_A	–40	27	105	°C
MC9S12H256**M**, MC9S12H128**M**					
Operating Junction Temperature Range	T_J	–40	–	140	°C
Operating Ambient Temperature Range [2]	T_A	–40	27	125	°C

NOTES:
1. The device contains an internal voltage regulator to generate the logic and PLL supply out of the I/O supply. The absolute maximum ratings apply when this regulator is disabled and the device is powered from an external source.
2. Please refer to **Section A.1.8 Power Dissipation and Thermal Characteristics** for more details about the relation between ambient temperature T_A and device junction temperature T_J.

A.1.8 Power Dissipation and Thermal Characteristics

Power dissipation and thermal characteristics are closely related. The user must assure that the maximum operating junction temperature is not exceeded. The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \Theta_{JA})$$

T_J = Junction Temperature, [°C]

T_A = Ambient Temperature, [°C]

P_D = Total Chip Power Dissipation, [W]

Θ_{JA} = Package Thermal Resistance, [°C/W]

The total power dissipation can be calculated from:

$$P_D = P_{INT} + P_{IO}$$

P_{INT} = Chip Internal Power Dissipation, [W]

$$P_{INT} = I_{DDR} \cdot V_{DDR} + I_{DDA} \cdot V_{DDA}$$

$$P_{IO} = \sum_i R_{DSON} \cdot I_{IO_i}^{2}$$

P_{IO} is the sum of all output currents on I/O ports associated with VDDX1,2 and VDDM1,2,3.

Table A-5 Thermal Package Characteristics[1]

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	T	Thermal Resistance LQFP112, single sided PCB[2]	θ_{JA}	–	–	54	^{o}C/W
2	T	Thermal Resistance LQFP112, double sided PCB with 2 internal planes[3]	θ_{JA}	–	–	41	^{o}C/W
3	T	Thermal Resistance LQFP 144, single sided PCB	θ_{JA}	–	–	45	^{o}C/W
4	T	Thermal Resistance LQFP 144, double sided PCB with 2 internal planes	θ_{JA}	–	–	37	^{o}C/W

NOTES:
1. The values for thermal resistance are achieved by package simulations
2. PC Board according to EIA/JEDEC Standard 51-2
3. PC Board according to EIA/JEDEC Standard 51-7

A.1.9 I/O Characteristics

This section describes the characteristics of all 5V I/O pins. All parameters are not always applicable, e.g. not all pins feature pull up/down resistances.

Table A-6 5V I/O Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Input High Voltage	V_{IH}	$0.65*V_{DD5}$	–	$V_{DD5} + 0.3$	V
2	P	Input Low Voltage	V_{IL}	$V_{SS5} – 0.3$	–	$0.35*V_{DD5}$	V
3	C	Input Hysteresis	V_{HYS}		250		mV
4	P	Input Leakage Current except PU, PV, PW (pins in high impedance input mode)[1] $V_{in} = V_{DD5}$ or V_{SS5}	I_{in}	–1.0	–	1.0	µA
5	P	Input Leakage Current PU, PV, PW (pins in high impedance input mode)[2] $V_{in} = V_{DD5}$ or V_{SS5}	I_{in}	–2.5	–	2.5	µA
6	P	Output High Voltage (pins in output mode, except PU, PV and PW) Partial Drive I_{OH} = –1.0mA Full Drive I_{OH} = –10mA	V_{OH}	$V_{DD5} – 0.8$	–	–	V
7	P	Output Low Voltage (pins in output mode except PU, PV and PW) Partial Drive I_{OL} = +1.0mA Full Drive I_{OL} = +10mA	V_{OL}	–	–	0.8	V
8	P	Output High Voltage (pins PU, PV and PW in output mode) I_{OH} = –20mA	V_{OH}	$V_{DD5} – 0.32$	$V_{DD5} – 0.2$	–	V
9	P	Output Low Voltage (pins PU, PV and PW in output mode) I_{OL} = +20mA	V_{OL}	–	.2	0.32	V
10	P	Output Rise Time (pins PU, PV and PW in output mode with slew control enabled) V_{DD5}=5V, R_{load}=1KΩ, 10% to 90% of V_{OH} -40°C, EPP package 25°C, 140°C	t_r	60 60	120[3] 100	180[3] 130	ns
11	P	Output Fall Time (pins PU, PV and PW in output mode with slew control enabled) V_{DD5}=5V, R_{load}=1KΩ, 10% to 90% of V_{OH} -40°C, EPP package 25°C, 140°C	t_f	60 60	120[3] 100	180[3] 130	ns
12	P	Internal Pull Up Device Current, tested at V_{IL} Max.	I_{PUL}	–	–	–130	µA
13	P	Internal Pull Up Device Current, tested at V_{IH} Min.	I_{PUH}	–10	–	–	µA
14	P	Internal Pull Down Device Current, tested at V_{IH} Min.	I_{PDH}	–	–	130	µA
15	P	Internal Pull Down Device Current, tested at V_{IL} Max.	I_{PDL}	10	–	–	µA

Table A-6 5V I/O Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
16	D	Input Capacitance	C_{in}		6	–	pF
17	T	Injection current[4] Single Pin limit Total Device Limit. Sum of all injected currents	 I_{ICS} I_{ICP}	 –2.5 –25	–	 2.5 25	mA
18	P	Port H, J Interrupt Input Pulse filtered[5]	t_{PULSE}			3	µs
19	P	Port H, J Interrupt Input Pulse passed[5]	t_{PULSE}	10			µs

NOTES:
1. Maximum leakage current occurs at maximum operating temperature. Current decreases by approximately one-half for each 8 C to 12 C in the temperature range from 50 C to 125 C.
2. Maximum leakage current occurs at maximum operating temperature. Current decreases by approximately one-half for each 8 C to 12 C in the temperature range from 50 C to 125 C.
3. This only applies to the EPP package, non-EPP packages retain the 100ns typ and 130ns max spec.
4. Refer to **Section A.1.4 Current Injection**, for more details
5. Parameter only applies in STOP or Pseudo STOP mode.

A.1.10 Supply Currents

This section describes the current consumption characteristics of the device as well as the conditions for the measurements.

A.1.10.1 Measurement Conditions

All measurements are without output loads. Unless otherwise noted the currents are measured in single chip mode, internal voltage regulator enabled and at 16MHz bus frequency using a 4MHz oscillator in Colpitts mode. Production testing is performed using a square wave signal at the EXTAL input.

A.1.10.2 Additional Remarks

In expanded modes the currents flowing in the system are highly dependent on the load at the address, data and control signals as well as on the duty cycle of those signals. No generally applicable numbers can be

given. A very good estimate is to take the single chip currents and add the currents due to the external loads.

Table A-7 Supply Current Characteristics

Conditions are shown in **Table A-4** unless otherwise noted

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	P	Run supply currents Single Chip, Internal regulator enabled	I_{DD5}			65	mA
2	P P	Wait Supply current All modules enabled, PLL on only RTI enabled [1]	I_{DDW}			40 5	mA
3		Pseudo Stop Current (RTI and COP disabled) [1, 2]	I_{DDPS}				µA
	C	–40°C			360		
	P	27°C			420	520	
	C	70°C			760		
	C	85°C			800		
	P	C Temp Option 100°C			950	2000	
	C	105°C			1000		
	P	V Temp Option 120°C			1500	3300	
	C	125°C			1700		
	P	M Temp Option 140° C			2500	4800	
4		Pseudo Stop Current (RTI and COP enabled) [1, 2]	I_{DDPS}				µA
	C	–40°C			420		
	C	27°C			480		
	C	70°C			820		
	C	85°C			860		
	C	105°C			1050		
	C	125°C			1700		
	C	140°C			2500		
5		Stop Current [2]	I_{DDS}				µA
	C	–40°C			20		
	P	27°C			40	100	
	C	70°C			200		
	C	85°C			300		
	P	C Temp Option 100°C			550	1500	
	C	105°C			700		
	P	V Temp Option 120°C			1200	2900	
	C	125°C			1400		
	P	M Temp Option 140°C			2200	4500	

NOTES:
1. PLL off
2. At those low power dissipation levels $T_J = T_A$ can be assumed

A.2 ATD Characteristics

This section describes the characteristics of the analog to digital converter.

A.2.1 ATD Operating Characteristics

The **Table A-8** shows conditions under which the ATD operates.

The following constraints exist to obtain full-scale, full range results:
$V_{SSA} \le V_{RL} \le V_{IN} \le V_{RH} \le V_{DDA}$. This constraint exists since the sample buffer amplifier can not drive beyond the power supply levels that it ties to. If the input level goes outside of this range it will effectively be clipped.

Table A-8 ATD Operating Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	Reference Potential Low High	 V_{RL} V_{RH}	 V_{SSA} $V_{DDA}/2$		 $V_{DDA}/2$ V_{DDA}	 V V
2	C	Differential Reference Voltage[1]	$V_{RH}–V_{RL}$	4.50	5.00	5.25	V
3	D	ATD Clock Frequency	f_{ATDCLK}	0.5		2.0	MHz
4	D	ATD 10-Bit Conversion Period Clock Cycles[2] Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	 N_{CONV10} T_{CONV10}	 14 7		 28 14	 Cycles µs
5	D	ATD 8-Bit Conversion Period Clock Cycles[2] Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	 N_{CONV8} T_{CONV8}	 12 6		 26 13	 Cycles µs
6	D	Stop Recovery Time (V_{DDA}=5.0 Volts)	t_{SR}			20	µs
7	P	Reference Supply current	I_{REF}			0.375	mA

NOTES:
1. Full accuracy is not guaranteed when differential voltage is less than 4.50V
2. The minimum time assumes a final sample period of 2 ATD clocks cycles while the maximum time assumes a final sample period of 16 ATD clocks.

A.2.2 Factors influencing accuracy

Three factors – source resistance, source capacitance and current injection – have an influence on the accuracy of the ATD.

A.2.2.1 Source Resistance:

Due to the input pin leakage current as specified in **Table A-6** in conjunction with the source resistance there will be a voltage drop from the signal source to the ATD input. The maximum source resistance R_S specifies results in an error of less than 1/2 LSB (2.5mV) at the maximum leakage current. If device or

operating conditions are less than worst case or leakage-induced error is acceptable, larger values of source resistance is allowed.

A.2.2.2 Source Capacitance

When sampling an additional internal capacitor is switched to the input. This can cause a voltage drop due to charge sharing with the external and the pin capacitance. For a maximum sampling error of the input voltage ≤ 1LSB, then the external filter capacitor, $C_f \geq 1024 * (C_{INS} - C_{INN})$.

A.2.2.3 Current Injection

There are two cases to consider.

1. A current is injected into the channel being converted. The channel being stressed has conversion values of $3FF ($FF in 8-bit mode) for analog inputs greater than V_{RH} and $000 for values less than V_{RL} unless the current is higher than specified as disruptive condition.
2. Current is injected into pins in the neighborhood of the channel being converted. A portion of this current is picked up by the channel (coupling ratio K), This additional current impacts the accuracy of the conversion depending on the source resistance.
   The additional input voltage error on the converted channel can be calculated as $V_{ERR} = K * R_S * I_{INJ}$, with I_{INJ} being the sum of the currents injected into the two pins adjacent to the converted channel.

Table A-9 ATD Electrical Characteristics

Conditions are shown in **Table A-4** unless otherwise noted

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	C	Max input Source Resistance	R_S	–	–	1	KΩ
2	T	Total Input Capacitance Non Sampling Sampling	 C_{INN} C_{INS}			 10 22	pF
3	C	Disruptive Analog Input Current	I_{NA}	–2.5		2.5	mA
4	C	Coupling Ratio positive current injection	K_p			10^{-4}	A/A
5	C	Coupling Ratio negative current injection	K_n			10^{-2}	A/A

A.2.3 ATD accuracy

Table A-10 specifies the ATD conversion performance excluding any errors due to current injection, input capacitance and source resistance.

Table A-10 ATD Conversion Performance

Conditions are shown in **Table A-4** unless otherwise noted
$V_{REF} = V_{RH} – V_{RL}$ = 5.12V. Resulting to one 8 bit count = 20mV and one 10 bit count = 5mV
f_{ATDCLK} = 2.0MHz

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	P	10-Bit Resolution	LSB		5		mV
2	P	10-Bit Differential Nonlinearity	DNL	–1		1	Counts
3	P	10-Bit Integral Nonlinearity	INL	–2.5	±1.5	2.5	Counts
4	P	10-Bit Absolute Error[1]	AE	–3	±2.0	3	Counts
5	P	8-Bit Resolution	LSB		20		mV
6	P	8-Bit Differential Nonlinearity	DNL	–0.5		0.5	Counts
7	P	8-Bit Integral Nonlinearity	INL	–1.0	±0.5	1.0	Counts
8	P	8-Bit Absolute Error[1]	AE	–1.5	±1.0	1.5	Counts

NOTES:
1. These values include the quantization error which is inherently 1/2 count for any A/D converter.

For the following definitions see also **Figure A-1**.

Differential Non-Linearity (DNL) is defined as the difference between two adjacent switching steps.

$$DNL(i) = \frac{V_i - V_{i-1}}{1LSB} - 1$$

The Integral Non-Linearity (INL) is defined as the sum of all DNLs:

$$INL(n) = \sum_{i=1}^{n} DNL(i) = \frac{V_n - V_0}{1LSB} - n$$

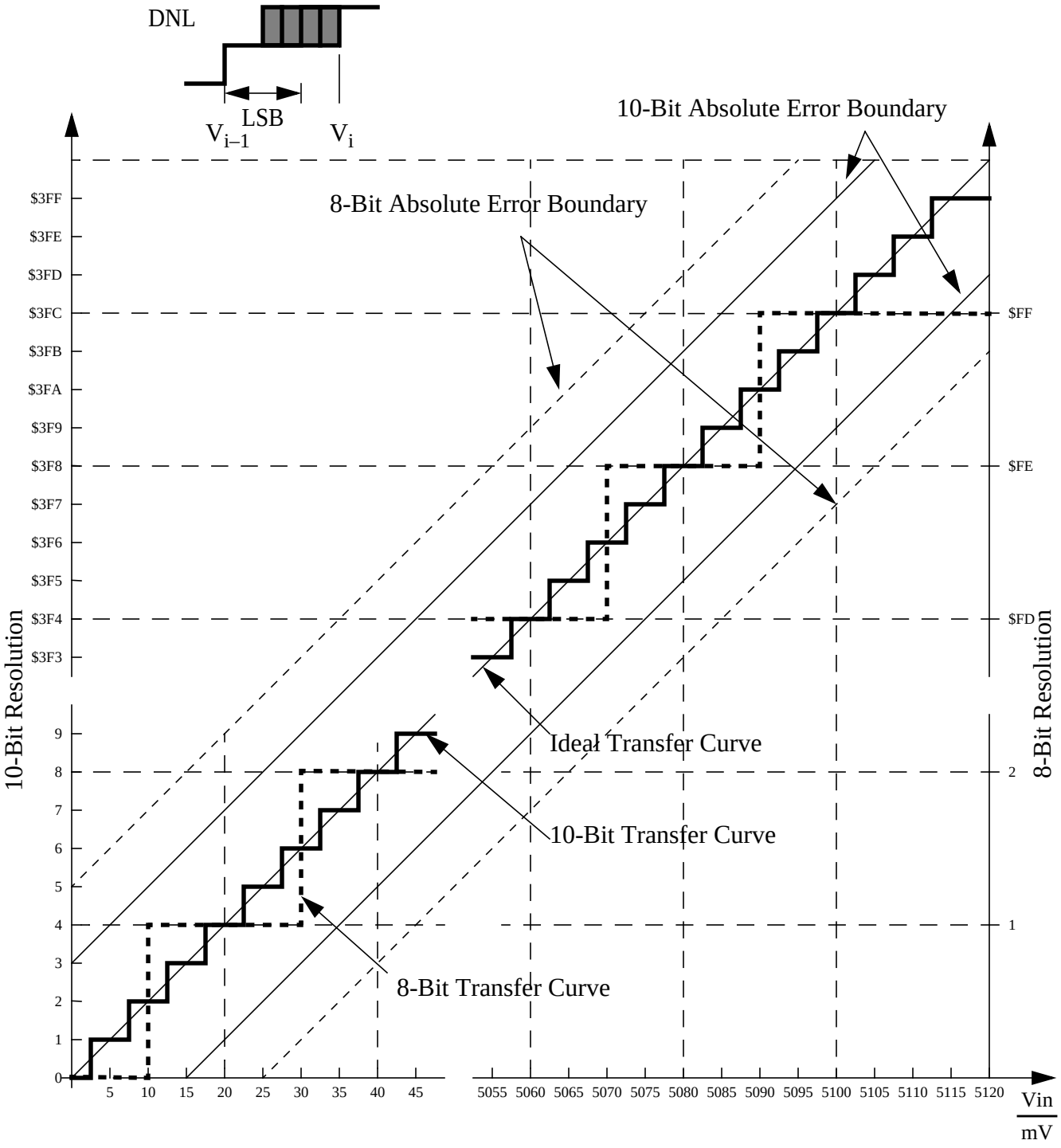


Figure A-1 ATD Accuracy Definitions

NOTE: ***Figure A-1*** *shows only definitions, for specification values refer to* ***Table A-10****.*

A.3 NVM, Flash and EEPROM

NOTE: *Unless otherwise noted the abbreviation NVM (Non Volatile Memory) is used for both Flash and EEPROM.*

A.3.1 NVM timing

The time base for all NVM program or erase operations is derived from the oscillator. A minimum oscillator frequency f_{NVMOSC} is required for performing program or erase operations. The NVM modules do not have any means to monitor the frequency and will not prevent program or erase operation at frequencies above or below the specified minimum. Attempting to program or erase the NVM modules at a lower frequency a full program or erase transition is not assured.

The Flash and EEPROM program and erase operations are timed using a clock derived from the oscillator using the FCLKDIV and ECLKDIV registers respectively. The frequency of this clock must be set within the limits specified as f_{NVMOP}.

The minimum program and erase times shown in **Table A-11** are calculated for maximum f_{NVMOP} and maximum f_{bus}. The maximum times are calculated for minimum f_{NVMOP} and a f_{bus} of 2MHz.

A.3.1.1 Single Word Programming

The programming time for single word programming is dependant on the bus frequency as a well as on the frequency f_{NVMOP} and can be calculated according to the following formula.

$$t_{swpgm} = 9 \cdot \frac{1}{f_{NVMOP}} + 25 \cdot \frac{1}{f_{bus}}$$

A.3.1.2 Burst Programming

This applies only to the Flash where up to 32 words in a row can be programmed consecutively using burst programming by keeping the command pipeline filled. The time to program a consecutive word can be calculated as:

$$t_{bwpgm} = 4 \cdot \frac{1}{f_{NVMOP}} + 9 \cdot \frac{1}{f_{bus}}$$

The time to program a whole row is:

$$t_{brpgm} = t_{swpgm} + 31 \cdot t_{bwpgm}$$

Burst programming is more than 2 times faster than single word programming.

A.3.1.3 Sector Erase

Erasing a 512 byte Flash sector or a 4 byte EEPROM sector takes:

$$t_{era} \approx 4000 \cdot \frac{1}{f_{NVMOP}}$$

The setup time can be ignored for this operation.

A.3.1.4 Mass Erase

Erasing a NVM block takes:

$$t_{mass} \approx 20000 \cdot \frac{1}{f_{NVMOP}}$$

The setup time can be ignored for this operation.

Table A-11 NVM Timing Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	External Oscillator Clock	f_{NVMOSC}	0.5		32 [1]	MHz
2	D	Bus frequency for Programming or Erase Operations	f_{NVMBUS}	1			MHz
3	D	Operating Frequency	f_{NVMOP}	150		200	kHz
4	P	Single Word Programming Time	t_{swpgm}	46 [2]		74.5 [3]	µs
5	D	Flash Burst Programming consecutive word [4]	t_{bwpgm}	20.4 [2]		31 [3]	µs
6	D	Flash Burst Programming Time for 32 Words [4]	t_{brpgm}	678.4 [2]		1035.5 [3]	µs
7	P	Sector Erase Time	t_{era}	20 [5]		26.7 [3]	ms
8	P	Mass Erase Time	t_{mass}	100 [5]		133 [3]	ms

NOTES:
1. Restrictions for oscillator in crystal mode apply!
2. Minimum Programming times are achieved under maximum NVM operating frequency f_{NVMOP} and maximum bus frequency f_{bus}.
3. Maximum Erase and Programming times are achieved under particular combinations of f_{NVMOP} and bus frequency f_{bus}. Refer to formulae in Sections **A.3.1.1 - A.3.1.4** for guidance.
4. urst Programming operations are not applicable to EEPROM
5. Minimum Erase times are achieved under maximum NVM operating frequency f_{NVMOP}.

A.3.2 NVM Reliability

The reliability of the NVM blocks is guaranteed by stress test during qualification, constant process monitors and burn-in to screen early life failures.

The failure rates for data retention and program/erase cycling are specified at the operating conditions noted.

The program/erase cycle count on the sector is incremented every time a sector or mass erase event is executed.

Table A-12 NVM Reliability Characteristics

Conditions are shown in **Table A-4** unless otherwise noted					
Num	**C**	**Rating**	**Cycles**	**Data Retention Lifetime**	**Unit**
1	C	Flash/EEPROM (-40˚C to +125˚C)	10	15	Years
2	C	EEPROM (-40˚C to +125˚C)	10,000	5	Years

NOTE: *Flash cycling performance is 10 cycles at -40˚C to +125˚C. Data retention is specified for 15 years.*

NOTE: *EEPROM cycling performance is 10K cycles at -40˚C to 125˚C. Data retention is specified for 5 years on words after cycling 10K times. However if only 10 cycles are executed on a word the data retention is specified for 15 years.*

A.4 Reset, Oscillator and PLL

This section summarizes the electrical characteristics of the various startup scenarios for Oscillator and Phase-Locked-Loop (PLL).

A.4.1 Startup

Table A-13 summarizes several startup characteristics explained in this section. Detailed description of the startup behavior can be found in the Clock and Reset Generator (CRG) Block User Guide.

Table A-13 Startup Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	T	POR release level	V_{PORR}			2.07	V
2	T	POR assert level	V_{PORA}	0.97			V
3	D	Reset input pulse width, minimum input time	PW_{RSTL}	2			t_{osc}
4	D	Startup from Reset	n_{RST}	192		196	n_{osc}
5	D	Interrupt pulse width, $\overline{IRQ}$ edge-sensitive mode	PW_{IRQ}	20			ns
6	D	Wait recovery startup time	t_{WRS}			14	t_{cyc}

A.4.1.1 POR

The release level V_{PORR} and the assert level V_{PORA} are derived from the VDD supply. They are also valid if the device is powered externally. After releasing the POR reset the oscillator and the clock quality check are started. If after a time t_{CQOUT} no valid oscillation is detected, the MCU will start using the internal self clock. The fastest startup time possible is given by n_{uposc}.

A.4.1.2 SRAM Data Retention

Provided an appropriate external reset signal is applied to the MCU, preventing the CPU from executing code when VDD5 is out of specification limits, the SRAM contents integrity is guaranteed if after the reset the PORF bit in the CRG Flags Register has not been set.

A.4.1.3 External Reset

When external reset is asserted for a time greater than PW_{RSTL} the CRG module generates an internal reset, and the CPU starts fetching the reset vector without doing a clock quality check, if there was an oscillation before reset.

A.4.1.4 Stop Recovery

Out of STOP the controller can be woken up by an external interrupt. A clock quality check as after POR is performed before releasing the clocks to the system.

A.4.1.5 Pseudo Stop and Wait Recovery

The recovery from Pseudo STOP and Wait are essentially the same since the oscillator was not stopped in both modes. The controller can be woken up by internal or external interrupts. After t_{wrs} the CPU starts fetching the interrupt vector.

A.4.2 Oscillator

The device features an internal Colpitts oscillator. By asserting the XCLKS input during reset this oscillator can be bypassed allowing the input of a square wave. Before asserting the oscillator to the internal system clocks the quality of the oscillation is checked for each start from either power-on, STOP or oscillator fail. t_{CQOUT} specifies the maximum time before switching to the internal self clock mode after POR or STOP if a proper oscillation is not detected. The quality check also determines the minimum oscillator start-up time t_{UPOSC}. The device also features a clock monitor. A Clock Monitor Failure is asserted if the frequency of the incoming clock signal is below the Assert Frequency f_{CMFA}.

Table A-14 Oscillator Characteristics

Conditions are shown in **Table A-4** unless otherwise noted

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	C	Crystal oscillator range	f_{OSC}	0.5		16	MHz
2	P	Startup Current	i_{OSC}	100			µA
3	D	Oscillator start-up time from POR or STOP	n_{UPOSC}	4100			cyc_{OSC}
4	C	Oscillator start-up time	t_{UPOSC}		8[1]	100[2]	ms
5	D	Clock Quality check time-out	t_{CQOUT}	0.45		2.5	s
6	P	Clock Monitor Failure Assert Frequency	f_{CMFA}	50	100	200	KHz
7	P	External square wave input frequency[3]	f_{EXT}	0.5		32	MHz
8	D	External square wave pulse width low	t_{EXTL}	15			ns
9	D	External square wave pulse width high	t_{EXTH}	15			ns
10	D	External square wave rise time	t_{EXTR}			1	ns
11	D	External square wave fall time	t_{EXTF}			1	ns
12	D	Input Capacitance EXTAL pin	C_{IN}		9		pF
13	D	Input Capacitance XTAL pin	C_{IN}		13		pF
14	C	DC Operating Bias in Colpitts Configuration on EXTAL Pin	V_{DCBIAS}		1.1		V

NOTES:
1. f_{osc} = 4MHz, C = 22pF.
2. Maximum value is for extreme cases using high Q, low frequency crystals

3. XCLKS =1 during reset

A.4.3 Phase Locked Loop

The oscillator provides the reference clock for the PLL. The PLL´s Voltage Controlled Oscillator (VCO) is also the system clock source in self clock mode.

A.4.3.1 XFC Component Selection

This section describes the selection of the XFC components to achieve a good filter characteristics.

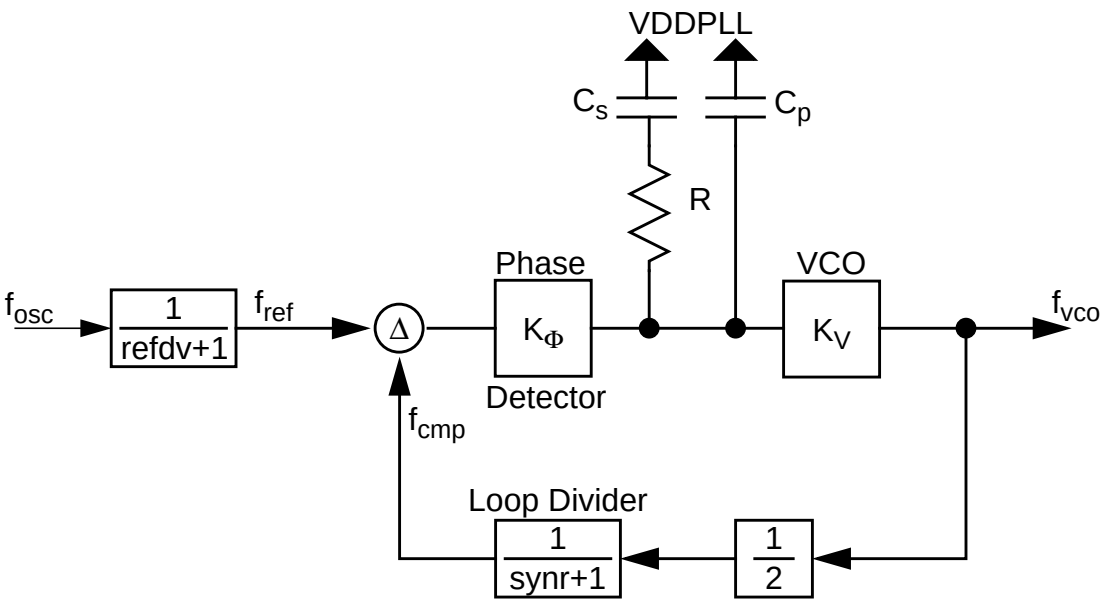


Figure A-2 Basic PLL functional diagram

The following procedure can be used to calculate the resistance and capacitance values using typical values for K_1, f_1 and i_{ch} from **Table A-15**.

The VCO Gain at the desired VCO output frequency is approximated by:

$$K_V = K_1 \cdot e^{\frac{(f_1 - f_{vco})}{K_1 \cdot 1V}}$$

The phase detector relationship is given by:

$$K_\Phi = i_{ch} \cdot K_V$$

i_{ch} is the current in tracking mode.

The loop bandwidth f_C should be chosen to fulfill the Gardner's stability criteria by at least a factor of 10, typical values are 50. $\zeta = 0.9$ ensures a good transient response.

$$f_C < \frac{2 \cdot \zeta \cdot f_{ref}}{\pi \cdot \left(\zeta + \sqrt{1 + \zeta^2}\right)} \frac{1}{50} \rightarrow f_C < \frac{f_{ref}}{4 \cdot 50}; (\zeta = 0.9)$$

And finally the frequency relationship is defined as

$$n = \frac{f_{VCO}}{f_{ref}} = 2 \cdot (synr + 1)$$

With the above inputs the resistance can be calculated as:

$$R = \frac{2 \cdot \pi \cdot n \cdot f_C}{K_\Phi}$$

The capacitance C_s can now be calculated as:

$$C_s = \frac{2 \cdot \zeta^2}{\pi \cdot f_C \cdot R} \approx \frac{0.516}{f_C \cdot R}; (\zeta = 0.9)$$

The capacitance C_p should be chosen in the range of:

$$C_s / 20 \leq C_p \leq C_s / 10$$

The stabilization delays shown in **Table A-15** are dependant on PLL operational settings and external component selection (e.g. crystal, XFC filter).

A.4.3.2 Jitter Information

The basic functionality of the PLL is shown in **Figure A-2**. With each transition of the clock f_{cmp}, the deviation from the reference clock f_{ref} is measured and input voltage to the VCO is adjusted accordingly.The adjustment is done continuously with no abrupt changes in the clock output frequency. Noise, voltage, temperature and other factors cause slight variations in the control loop resulting in a clock jitter. This jitter affects the real minimum and maximum clock periods as illustrated in **Figure A-3**.

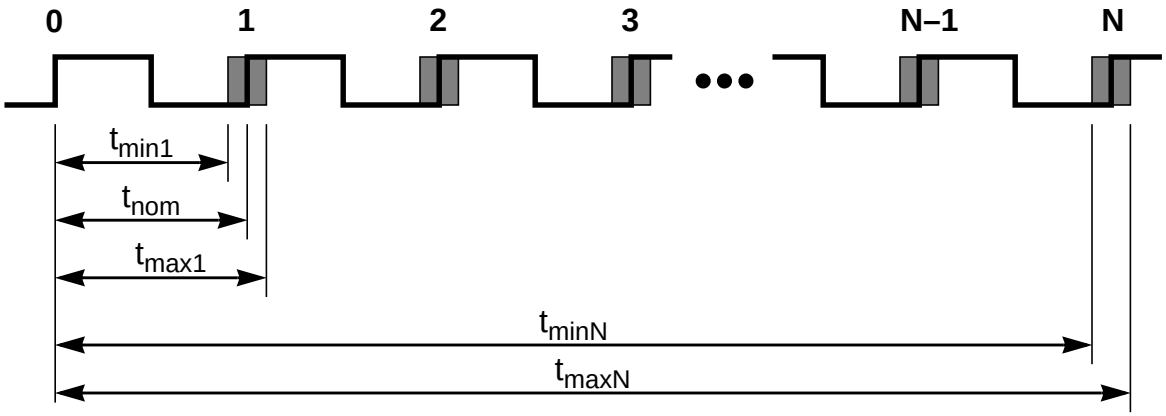


Figure A-3 Jitter Definitions

The relative deviation of t_{nom} is at its maximum for one clock period, and decreases towards zero for larger number of clock periods (N).

Defining the jitter as:

$$J(N) = \max\left(\left|1 - \frac{t_{max}(N)}{N \cdot t_{nom}}\right|, \left|1 - \frac{t_{min}(N)}{N \cdot t_{nom}}\right|\right)$$

For N < 100, the following equation is a good fit for the maximum jitter:

$$J(N) = \frac{j_1}{\sqrt{N}} + j_2$$

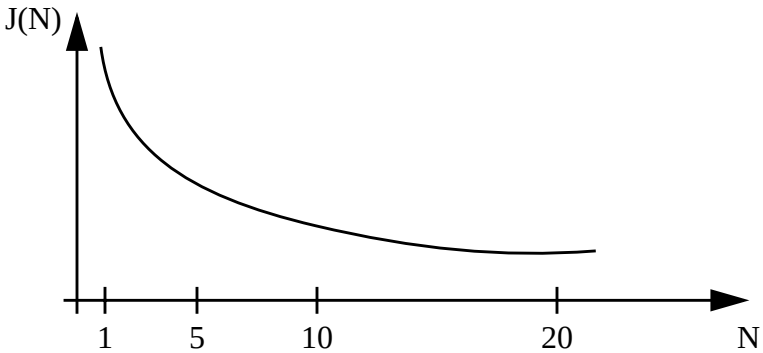


Figure A-4 Maximum bus clock jitter approximation

This is very important to notice with respect to timers, serial modules where a pre-scaler will eliminate the effect of the jitter to a large extent.

Table A-15 PLL Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Self Clock Mode frequency	f_{SCM}	1		5.5	MHz
2	D	VCO locking range	f_{VCO}	8		32	MHz
3	D	Lock Detector transition from Acquisition to Tracking mode	$\|\Delta_{trk}\|$	3		4	%[1]
4	D	Lock Detection	$\|\Delta_{Lock}\|$	0		1.5	%[1]
5	D	Un-Lock Detection	$\|\Delta_{unl}\|$	0.5		2.5	%[1]
6	D	Lock Detector transition from Tracking to Acquisition mode	$\|\Delta_{unt}\|$	6		8	%[1]
7	C	PLLON Total Stabilization delay (Auto Mode) [2]	t_{stab}		0.5		ms
8	D	PLLON Acquisition mode stabilization delay [2]	t_{acq}		0.3		ms
9	D	PLLON Tracking mode stabilization delay [2]	t_{al}		0.2		ms
10	P	Fitting parameter VCO loop gain[3]	K_1		–120	-224	MHz/V
11	D	Fitting parameter VCO loop frequency	f_1		75		MHz
12	P	Charge pump current acquisition mode	$\| i_{ch} \|$	20	38.5	60	µA
13	P	Charge pump current tracking mode	$\| i_{ch} \|$	2	3.5	6	µA
14	C	Jitter fit parameter 1[2]	j_1			1.1	%
15	C	Jitter fit parameter 2[2]	j_2			0.13	%

NOTES:
1. % deviation from target frequency
2. f_{REF} = 4MHz, f_{BUS} = 16MHz equivalent f_{VCO} = 32MHz: REFDV = #$03, SYNR = #$0F, Cs = 4.7nF, Cp = 470pF, Rs = 10KΩ.
3. K_1 is measured with V_{XFC} = 1.4V and V_{XFC} = 1.7V @ VDD5 = 5.25V

A.5 MSCAN

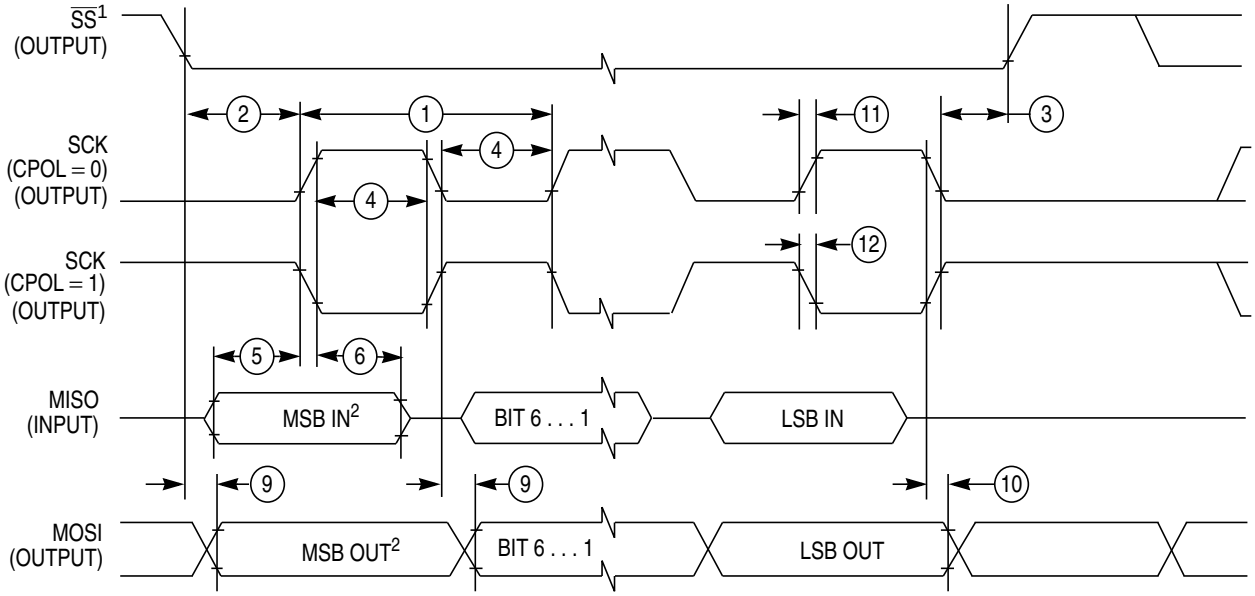
Table A-16 MSCAN Wake-up Pulse Characteristics

Conditions are shown in **Table A-4** unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	MSCAN Wake-up dominant pulse filtered	t_{WUP}			2	µs
2	P	MSCAN Wake-up dominant pulse pass	t_{WUP}	5			µs

A.6 SPI

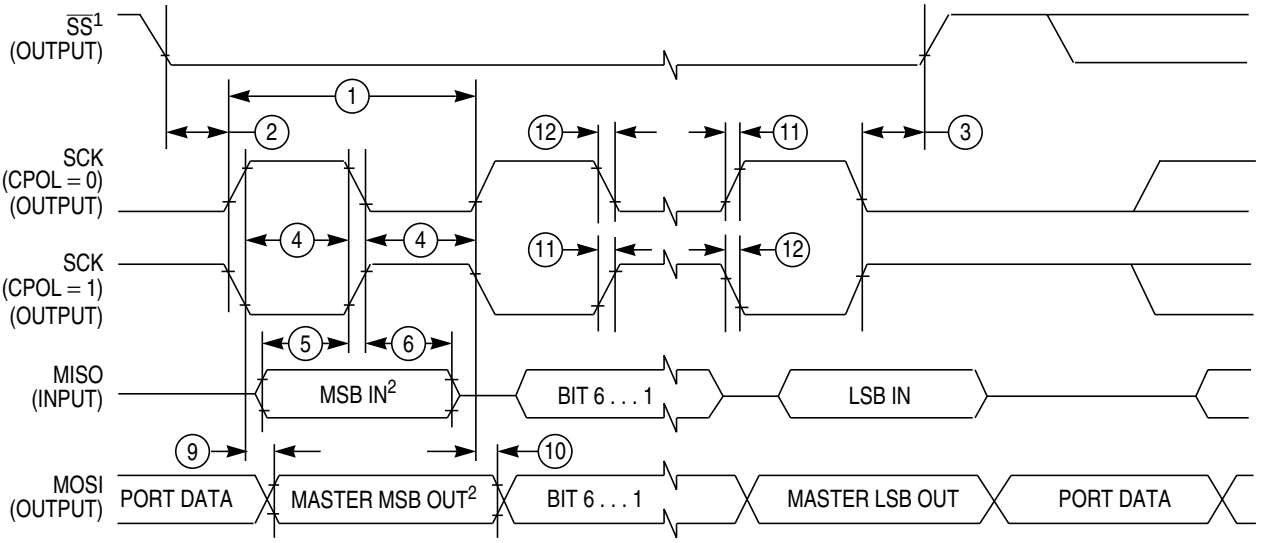
A.6.1 Master Mode

Figure A-5 and **Figure A-6** illustrate the master mode timing. Timing values are shown in **Table A-17**.



1. If configured as output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure A-5 SPI Master Timing (CPHA = 0)



1. If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure A-6 SPI Master Timing (CPHA =1)

Table A-17 SPI Master Mode Timing Characteristics[1]

Conditions are shown in **Table A-4** unless otherwise noted, C_{LOAD} = 200pF on all outputs							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Operating Frequency	f_{op}	DC		1/4	f_{bus}
1	P	SCK Period $t_{sck} = 1./f_{op}$	t_{sck}	4		2048	t_{bus}
2	D	Enable Lead Time	t_{lead}	1/2		—	t_{sck}
3	D	Enable Lag Time	t_{lag}	1/2			t_{sck}
4	D	Clock (SCK) High or Low Time	t_{wsck}	t_{bus} – 30		1024 t_{bus}	ns
5	D	Data Setup Time (Inputs)	t_{su}	25			ns
6	D	Data Hold Time (Inputs)	t_{hi}	0			ns
9	D	Data Valid (after SCK Edge)	t_v			25	ns
10	D	Data Hold Time (Outputs)	t_{ho}	0			ns
11	D	Rise Time Inputs and Outputs	t_r			25	ns
12	D	Fall Time Inputs and Outputs	t_f			25	ns

NOTES:
1. The numbers 7, 8 in the column labeled “Num” are missing. This has been done on purpose to be consistent between the Master and the Slave timing shown in **Table A-18**.

A.6.2 Slave Mode

Figure A-7 and **Figure A-8** illustrate the slave mode timing. Timing values are shown in **Table A-18**.

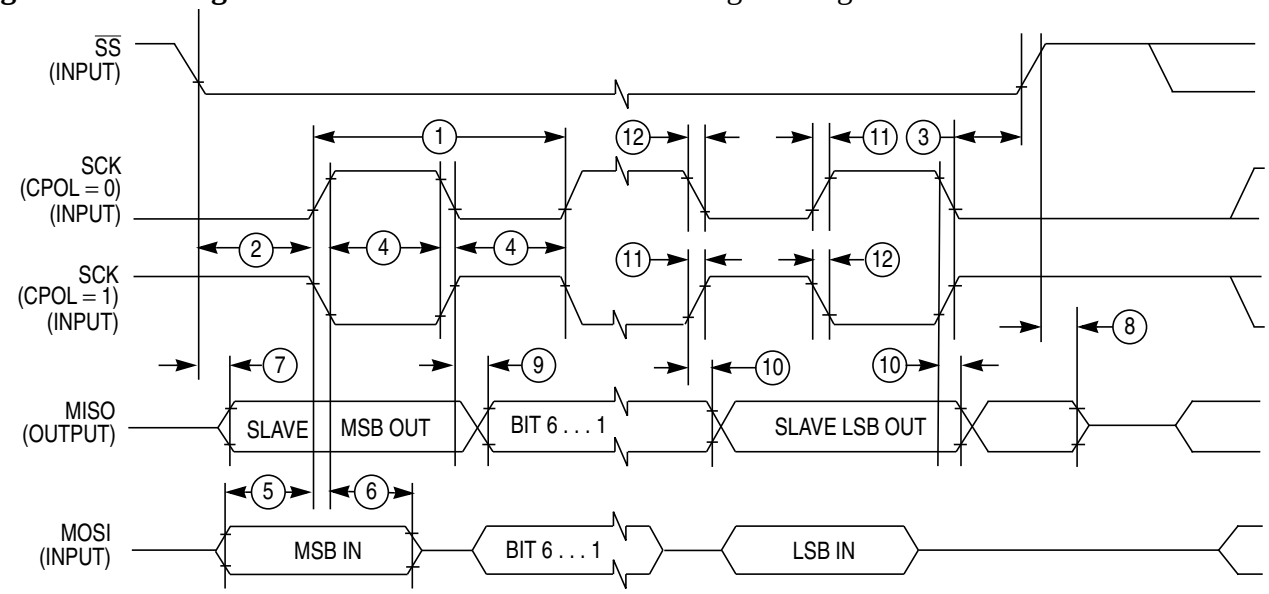


Figure A-7 SPI Slave Timing (CPHA = 0)

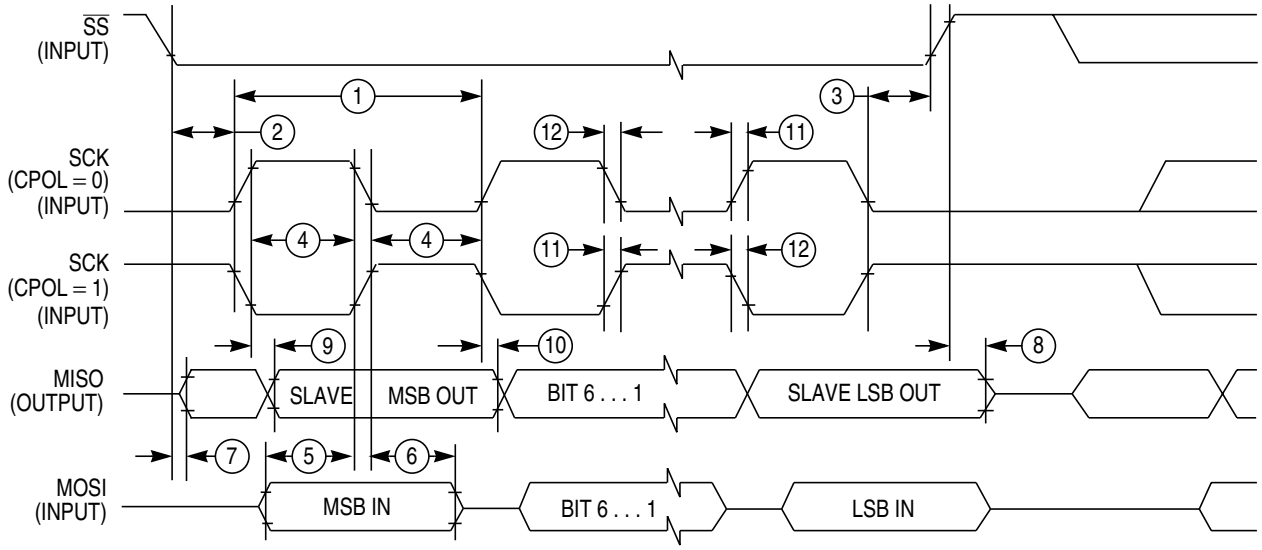


Figure A-8 SPI Slave Timing (CPHA =1)

Table A-18 SPI Slave Mode Timing Characteristics

Conditions are shown in **Table A-4** unless otherwise noted, CLOAD = 200pF on all outputs							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Operating Frequency	f_{op}	DC		1/4	f_{bus}
1	P	SCK Period $t_{sck} = 1./f_{op}$	t_{sck}	4		2048	t_{bus}
2	D	Enable Lead Time	t_{lead}	1			t_{cyc}
3	D	Enable Lag Time	t_{lag}	1			t_{cyc}
4	D	Clock (SCK) High or Low Time	t_{wsck}	$t_{cyc} – 30$			ns
5	D	Data Setup Time (Inputs)	t_{su}	25			ns
6	D	Data Hold Time (Inputs)	t_{hi}	25			ns
7	D	Slave Access Time	t_a			1	t_{cyc}
8	D	Slave MISO Disable Time	t_{dis}			1	t_{cyc}
9	D	Data Valid (after SCK Edge)	t_v			25	ns
10	D	Data Hold Time (Outputs)	t_{ho}	0			ns
11	D	Rise Time Inputs and Outputs	t_r			25	ns
12	D	Fall Time Inputs and Outputs	t_f			25	ns

A.7 LCD_32F4B

Table A.7-19 LCD_32F4B Driver Electrical Characteristics

Characteristic	Symbol	Min.	Typ.	Max.	Unit
LCD Supply Voltage	VLCD	-0.25	-	VDDX + 0.25	V
LCD Output Impedance(BP[3:0],FP[31:0]) for outputs to charge to higher voltage level or to GND [1]	$Z_{BP/FP}$	-	-	5.0	kOhm
LCD Output Current (BP[3:0],FP[31:0]) for outputs to discharge to lower voltage level except GND [2]	$I_{BP/FP}$	50	-	-	uA

NOTES:
1. Outputs measured one at a time, low impedance voltage source connected to the VLCD pin.
2. Outputs measured one at a time, low impedance voltage source connected to the VLCD pin.

A.8 External Bus Timing

A timing diagram of the external multiplexed-bus is illustrated in **Figure A-9** with the actual timing values shown on table **Table A-20**. All major bus signals are included in the diagram. While both a data write and data read cycle are shown, only one or the other would occur on a particular bus cycle.

A.8.1 General Muxed Bus Timing

The expanded bus timings are highly dependent on the load conditions. The timing parameters shown assume a balanced load across all outputs.

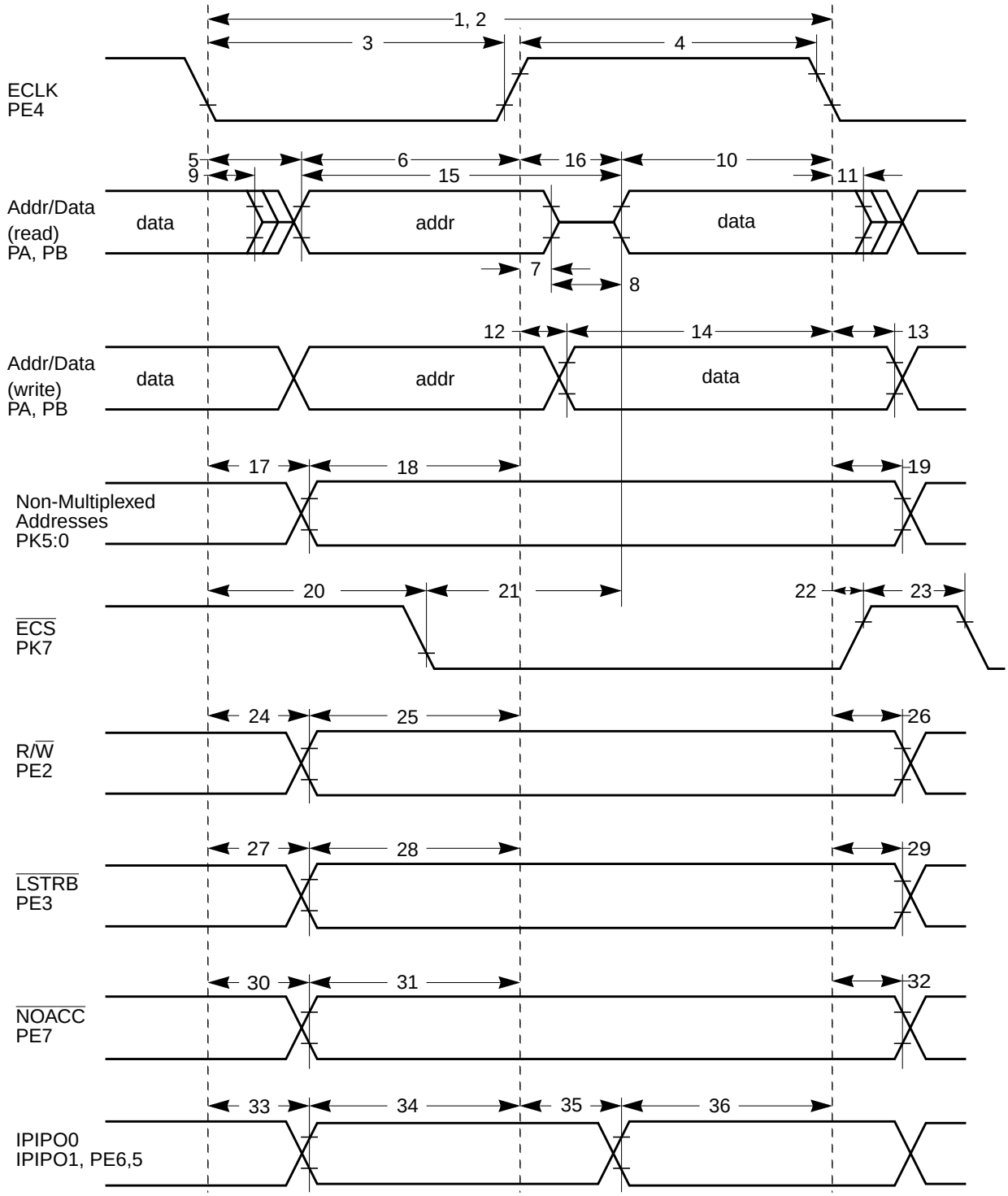


Figure A-9 General External Bus Timing

Table A-20 Expanded Bus Timing Characteristics

Conditions are shown in **Table A-4** unless otherwise noted, C_{LOAD} = 50pF

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	P	Frequency of operation (E-clock)	f_o	0		16.0	MHz
2	P	Cycle time	t_{cyc}	62.5			ns
3	D	Pulse width, E low	PW_{EL}	30			ns
4	D	Pulse width, E high[1]	PW_{EH}	30			ns
5	D	Address delay time	t_{AD}			8	ns
6	D	Address valid time to E rise (PW_{EL}–t_{AD})	t_{AV}	22			ns
7	D	Muxed address hold time	t_{MAH}	2			ns
8	D	Address hold to data valid	t_{AHDS}	7			ns
9	D	Data hold to address	t_{DHA}	2			ns
10	D	Read data setup time	t_{DSR}	24			ns
11	D	Read data hold time	t_{DHR}	0			ns
12	D	Write data delay time	t_{DDW}			7	ns
13	D	Write data hold time	t_{DHW}	2			ns
14	D	Write data setup time[1] (PW_{EH}–t_{DDW})	t_{DSW}	23			ns
15	D	Address access time[1] (t_{cyc}–t_{AD}–t_{DSR})	t_{ACCA}	30			ns
16	D	E high access time[1] (PW_{EH}–t_{DSR})	t_{ACCE}	6			ns
17	D	Non-multiplexed address delay time	t_{NAD}			6	ns
18	D	Non-muxed address valid to E rise (PW_{EL}–t_{NAD})	t_{NAV}	26			ns
19	D	Non-multiplexed address hold time	t_{NAH}	2			ns
20	D	Chip select delay time	t_{CSD}			6 + t_{cyc}/4	ns
21	D	Chip select access time[1] (t_{cyc}–t_{CSD}–t_{DSR})	t_{ACCS}	t_{cyc}/4 – 2			ns
22	D	Chip select hold time	t_{CSH}	2			ns
23	D	Chip select negated time	t_{CSN}	8			ns
24	D	Read/write delay time	t_{RWD}			7	ns
25	D	Read/write valid time to E rise (PW_{EL}–t_{RWD})	t_{RWV}	25			ns
26	D	Read/write hold time	t_{RWH}	2			ns
27	D	Low strobe delay time	t_{LSD}			7	ns
28	D	Low strobe valid time to E rise (PW_{EL}–t_{LSD})	t_{LSV}	25			ns
29	D	Low strobe hold time	t_{LSH}	2			ns
30	D	NOACC strobe delay time	t_{NOD}			7	ns
31	D	NOACC valid time to E rise (PW_{EL}–t_{NOD})	t_{NOV}	25			ns

Table A-20 Expanded Bus Timing Characteristics

Conditions are shown in **Table A-4** unless otherwise noted, C_{LOAD} = 50pF							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
32	D	NOACC hold time	t_{NOH}	2			ns
33	D	IPIPO[1:0] delay time	t_{P0D}	2		7	ns
34	D	IPIPO[1:0] valid time to E rise (PW_{EL}–t_{P0D})	t_{P0V}	22			ns
35	D	IPIPO[1:0] delay time[1] (PW_{EH}–t_{P1V})	t_{P1D}	2		25	ns
36	D	IPIPO[1:0] valid time to E fall	t_{P1V}	22			ns

NOTES:

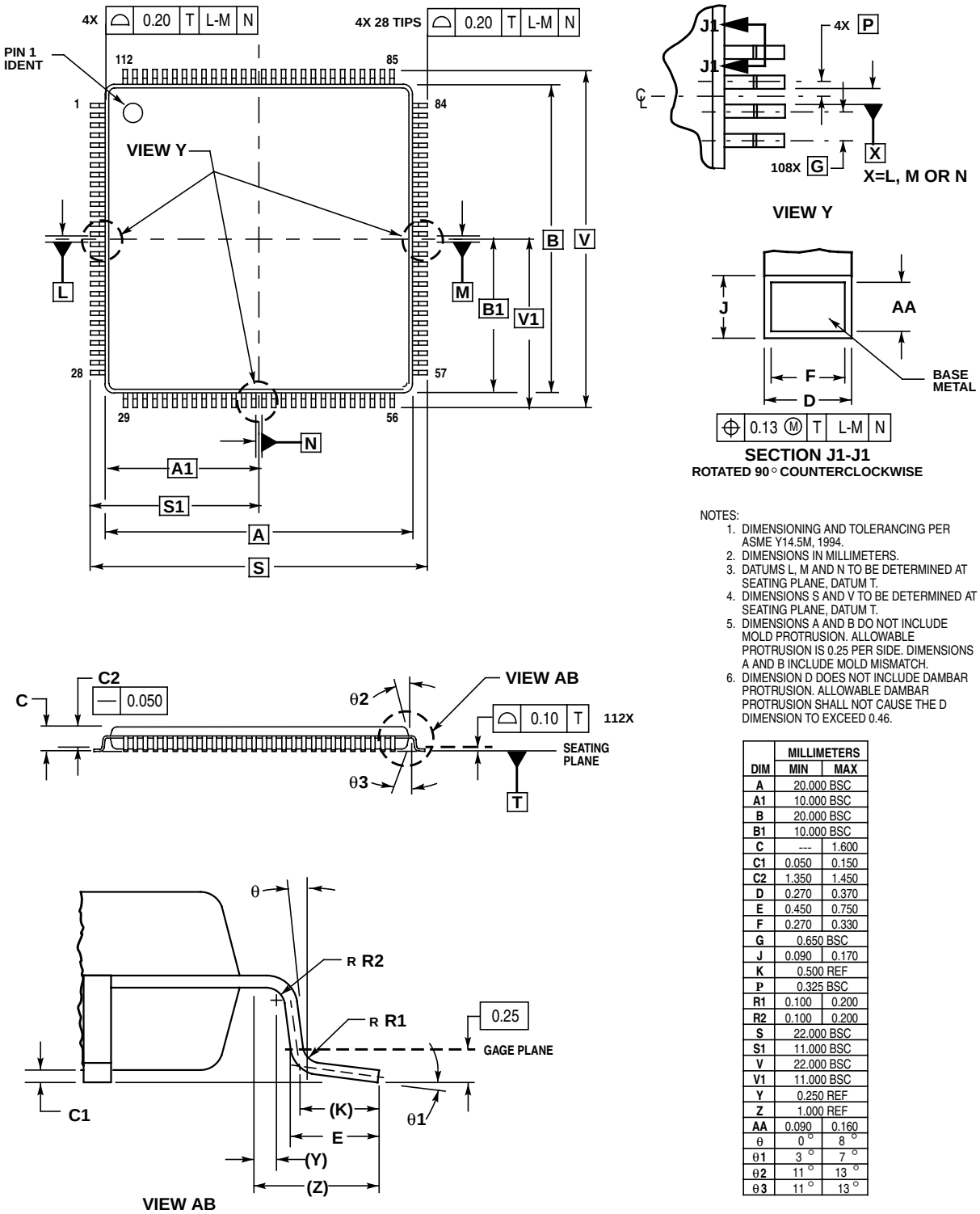
1. Affected by clock stretch: add N x t_{cyc} where N=0,1,2 or 3, depending on the number of clock stretches.

Appendix B Package Information

B.1 General

This section provides the physical dimensions of the MC9S12H256 and MC9S12H128 packages.

B.2 112-pin LQFP package

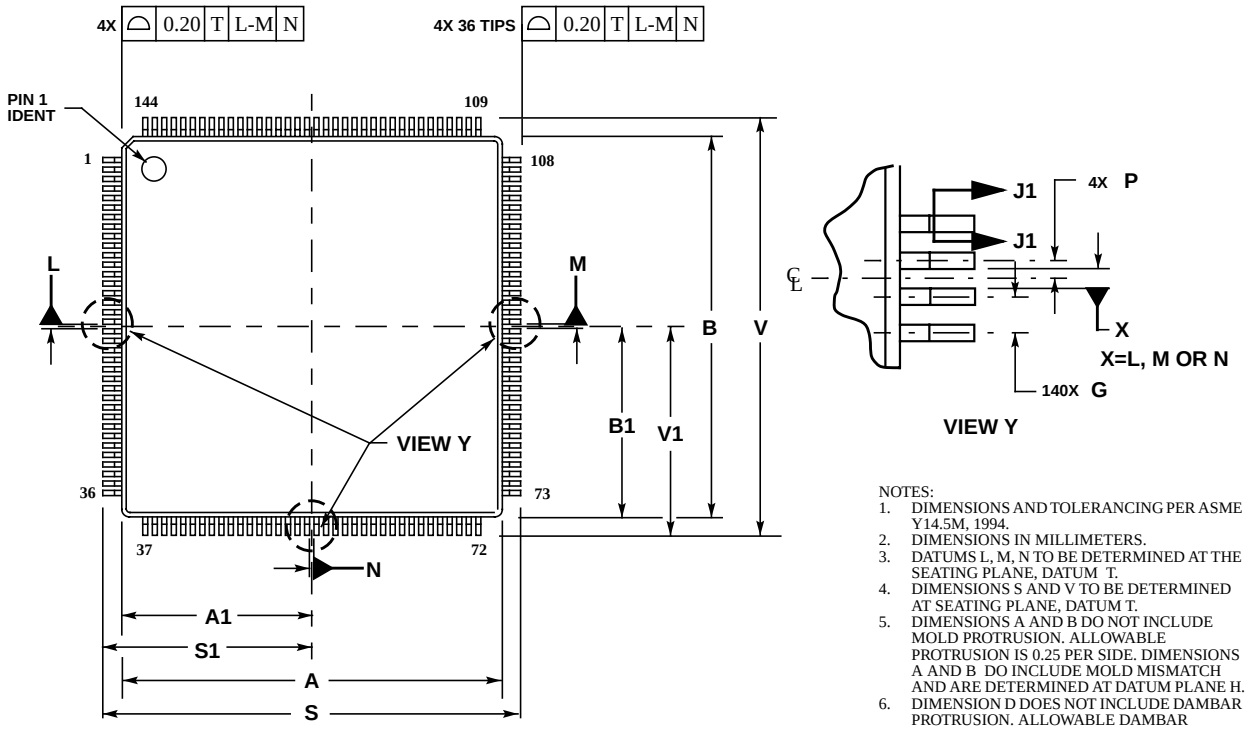


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DATUMS L, M AND N TO BE DETERMINED AT SEATING PLANE, DATUM T.
4. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM T.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B INCLUDE MOLD MISMATCH.
6. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.46.

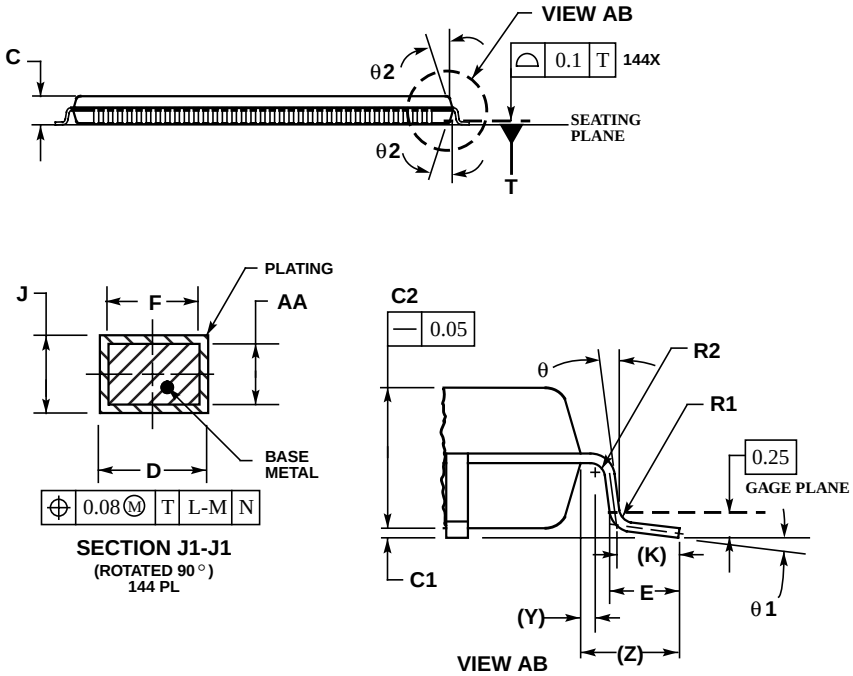
	MILLIMETERS	
DIM	MIN	MAX
A	20.000 BSC	
A1	10.000 BSC	
B	20.000 BSC	
B1	10.000 BSC	
C	---	1.600
C1	0.050	0.150
C2	1.350	1.450
D	0.270	0.370
E	0.450	0.750
F	0.270	0.330
G	0.650 BSC	
J	0.090	0.170
K	0.500 REF	
P	0.325 BSC	
R1	0.100	0.200
R2	0.100	0.200
S	22.000 BSC	
S1	11.000 BSC	
V	22.000 BSC	
V1	11.000 BSC	
Y	0.250 REF	
Z	1.000 REF	
AA	0.090	0.160
θ	0°	8°
θ1	3°	7°
θ2	11°	13°
θ3	11°	13°

Figure B-1 112-pin LQFP mechanical dimensions (case no. 987)

B.3 144-pin LQFP package



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DATUMS L, M, N TO BE DETERMINED AT THE SEATING PLANE, DATUM T.
4. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM T.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.35.



DIM	MILLIMETERS MIN	MAX
A	20.00 BSC	
A1	10.00 BSC	
B	20.00 BSC	
B1	10.00 BSC	
C	1.40	1.60
C1	0.05	0.15
C2	1.35	1.45
D	0.17	0.27
E	0.45	0.75
F	0.17	0.23
G	0.50 BSC	
J	0.09	0.20
K	0.50 REF	
P	0.25 BSC	
R1	0.13	0.20
R2	0.13	0.20
S	22.00 BSC	
S1	11.00 BSC	
V	22.00 BSC	
V1	11.00 BSC	
Y	0.25 REF	
Z	1.00 REF	
AA	0.09	0.16
θ	0 °	
θ1	0 °	7 °
θ2	11°	13 °

CASE 918-03
ISSUE C

Figure B-2 144-pin LQFP mechanical dimensions (case no. 918-03)

User Guide End Sheet

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