# THE DATASHEET OF

# MC94MX21DVKN3

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**Freescale Semiconductor**
Data Sheet: Technical Data

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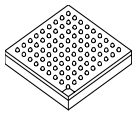
# MC94MX21



**Package Information**

(MAPBGA–289)

**Ordering Information: See Table 1 on page 3**

# MC94MX21

333 and 350 MHz

## 1 Introduction

Freescale's i.MX family of microprocessors has demonstrated leadership in the portable handheld market. Building on the success of the MX (Media Extensions) series, the i.MX21 (MC94MX21) provides a leap in performance with an ARM926EJ-S™ microprocessor core that provides accelerated Java support in addition to highly integrated system functions. The i.MX21 device specifically addresses the needs of the smartphone and portable product markets with intelligent integrated peripherals, advanced processor core, and power management capabilities.

Thei.MX21 features the advanced and power-efficient ARM926EJ-S core operating at speeds up to 350 MHz and is part of a growing family of *Smart Speed* products that offer high performance processing optimized for lowest power consumption. On-chip modules such as a video accelerator module, LCD controller, USB On-The-Go, 1-Wire® interface, CMOS sensor interface, and synchronous serial interfaces offer designers a rich suite of peripherals that can enhance many products seeking to provide a rich multimedia experience.

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This document contains information on a new product. Specifications and information herein are subject to change without notice.
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For cost sensitive applications, the NAND Flash controller allows the use of low-cost NAND Flash devices to be used as primary or secondary non-volatile storage. The on-chip error correction code (ECC) and parity checking circuitry of the NAND Flash controller frees the CPU for other tasks. WLAN, Bluetooth and expansion options are provided through PCMCIA/CF, USB, and MMC/SD host controllers.

The device is packaged in a 289-pin MAPBGA.

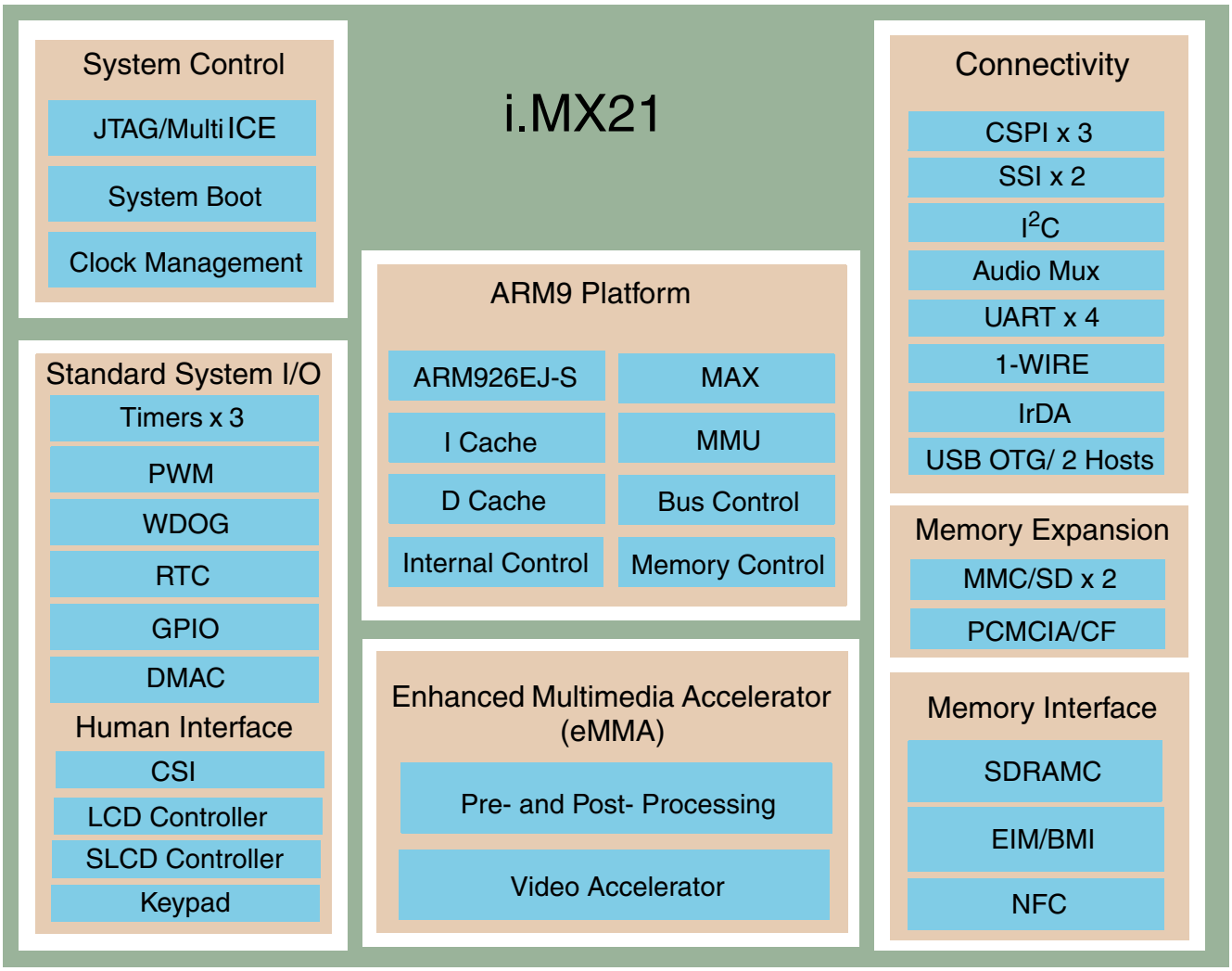



**Figure 1. i.MX21 Functional Block Diagram**

## 1.1 Conventions

This document uses the following conventions:

- $\overline{\text{OVERBAR}}$ is used to indicate a signal that is active when pulled low: for example, $\overline{\text{RESET}}$.
- *Logic level one* is a voltage that corresponds to Boolean true (1) state.
- *Logic level zero* is a voltage that corresponds to Boolean false (0) state.
- To *set* a bit or bits means to establish logic level one.
- To *clear* a bit or bits means to establish logic level zero.
- A *signal* is an electronic construct whose state conveys or changes in state convey information.

- A *pin* is an external physical connection. The same pin can be used to connect a number of signals.
- *Asserted* means that a discrete signal is in active logic state.
  - *Active low* signals change from logic level one to logic level zero.
  - *Active high* signals change from logic level zero to logic level one.
- *Negated* means that an asserted discrete signal changes logic state.
  - *Active low* signals change from logic level zero to logic level one.
  - *Active high* signals change from logic level one to logic level zero.
- LSB means *least significant bit* or *bits*, and MSB means *most significant bit* or *bits*. References to low and high bytes or words are spelled out.
- Numbers preceded by a percent sign (%) are binary. Numbers preceded by a dollar sign ($) or *0x* are hexadecimal.

## 1.2 Target Applications

The i.MX21 is targeted for advanced information appliances, smart phones, Web browsers, digital MP3 audio players, handheld computers based on the popular Palm OS platform, and messaging applications.

## 1.3 Reference Documentation

The following documents are required for a complete description of the i.MX21 and are necessary to design properly with the device. Especially for those not familiar with the ARM926EJ-S processor the following documents are helpful when used in conjunction with this manual.

*ARM Architecture Reference Manual* (ARM Ltd., order number ARM DDI 0100)

*ARM7TDMI Data Sheet* (ARM Ltd., order number ARM DDI 0029)

*ARM920T Technical Reference Manual* (ARM Ltd., order number ARM DDI 0151C)

*MC9328MX21 Product Brief* (order number MC9328MX21P)

*MC9328MX21 Reference Manual* (order number MC9328MX21RM)

The Freescale manuals are available on the Freescale Semiconductor Web site at http://www.freescale.com. These documents may be downloaded directly from the Freescale Web site, or printed versions may be ordered. The ARM Ltd. documentation is available from http://www.arm.com.

## 1.4 Ordering Information

Table 1 provides ordering information for the device. See Table 4 on page 14 for core frequency and supply voltage requirements.

**Table 1. Ordering Information**

| Part Order Number | Package Size | Package Type | Operating Range |
|---|---|---|---|
| MC94MX21DVKN3 | 289-lead MAPBGA<br>0.65mm, 14mm x 14mm | Lead-free | -30°C–70°C |

## 1.5 Features

The i.MX21 boasts a robust array of features that can support a wide variety of applications. Below is a brief description of i.MX21 features.

- ARM926EJ-S Core Complex
- enhanced Multimedia Accelerator (eMMA)
- Display and Video Modules
  - LCD Controller (LCDC)
  - Smart LCD Controller (SLCDC)
  - CMOS Sensor Interface (CSI)
- Bus Master Interface (BMI)
- Wireless Connectivity
  - Fast Infra-Red Interface (FIRI)
- Wired Connectivity
  - USB On-The-Go (USBOTG) Controller
  - Four Universal Asynchronous Receiver/Transmitters (UART*x*)
  - Three Configurable Serial Peripheral Interfaces (CSPI*x*) for High Speed Data Transfer
  - Inter-IC ($I^2C$) Bus Module
  - Two Synchronous Serial Interfaces (SSI) with Inter-IC Sound ($I^2S$)
  - Digital Audio Mux
  - One-Wire Controller
  - Keypad Interface
- Memory Expansion and I/O Card Support
  - Two Multimedia Card and Secure Digital (MMC/SD) Host Controller Modules
- Memory Interface
  - External Interface Module (EIM)
  - SDRAM Controller (SDRAMC)
  - NAND Flash Controller (NFC)
  - PCMCIA/CF Interface
- Standard System Resources
  - Clock Generation Module (CGM) and Power Control Module
  - Three General-Purpose 32-Bit Counters/Timers
  - Watchdog Timer
  - Real-Time Clock/Sampling Timer (RTC)
  - Pulse-Width Modulator (PWM) Module
  - Direct Memory Access Controller (DMAC)
  - General-Purpose I/O (GPIO) Ports
  - Debug Capability

# 2 Signal Descriptions

Table 2 identifies and describes the i.MX21 signals. Pin assignment is provided in Section 4, “Pin Assignment and Package Information” and in the “Signal Multiplexing Scheme” table within the reference manual.

The connections of the pins in Table 2 depends solely upon the user application, however there are a few factory test signals that are not used in a normal application. Following is a list of these signals and how they are to be terminated for proper operation of the i.MX21 processor:

- CLKMODE[1:0]: To ensure proper operation, leave these signals as no connects.
- OSC26M_TEST: To ensure proper operation, leave this signal as no connect.
- EXT_48M: To ensure proper operation, connect this signal to ground.
- EXT_266M: To ensure proper operation, connect this signal to ground.
- TEST_WB[2:0]: These signals are also multiplexed with GPIO PORT E as well as alternate keypad signals. If not utilizing these signals for GPIO functionality or for their other multiplexed function, then configure as GPIO input with pull up enabled, and leave as a no connect.
- TEST_WB[4:3]: To ensure proper operation, leave these signals as no connects.

**Table 2. i.MX21 Signal Descriptions**

| Signal Name | Function/Notes |
|---|---|
| **External Bus/Chip Select (EIM)** | |
| A [25:0] | Address bus signals |
| D [31:0] | Data bus signals |
| $\overline{EB0}$ | MSB Byte Strobe—Active low external enable byte signal that controls D [31:24], shared with SDRAM DQM0. |
| $\overline{EB1}$ | Byte Strobe—Active low external enable byte signal that controls D [23:16], shared with SDRAM DQM1. |
| $\overline{EB2}$ | Byte Strobe—Active low external enable byte signal that controls D [15:8], shared with SDRAM DQM2 and PCMCIA $\overline{PC_REG}$. |
| $\overline{EB3}$ | LSB Byte Strobe—Active low external enable byte signal that controls D [7:0], shared with SDRAM DQM3 and PCMCIA $\overline{PC_IORD}$. |
| $\overline{OE}$ | Memory Output Enable—Active low output enables external data bus, shared with PCMCIA $\overline{PC_IOWR}$. |
| $\overline{CS}$ [5:0] | Chip Select—The chip select signals $\overline{CS}$ [3:2] are multiplexed with $\overline{CSD}$ [1:0] and are selected by the Function Multiplexing Control Register (FMCR) in the System Control chapter. By default $\overline{CSD}$ [1:0] is selected. DTACK is multiplexed with $\overline{CS4}$. |
| $\overline{ECB}$ | Active low input signal sent by flash device to the EIM whenever the flash device must terminate an on-going burst sequence and initiate a new (long first access) burst sequence. |
| $\overline{LBA}$ | Active low signal sent by flash device causing the external burst device to latch the starting burst address. |
| BCLK | Clock signal sent to external synchronous memories (such as burst flash) during burst mode. |
| $\overline{RW}$ | $\overline{RW}$ signal—Indicates whether external access is a read (high) or write (low) cycle. This signal is also shared with the PCMCIA $\overline{PC_WE}$. |
| DTACK | DTACK signal—External input data acknowledge signal, multiplexed with $\overline{CS4}$. |
| **Bootstrap** | |
| BOOT [3:0] | System Boot Mode Select—The operational system boot mode upon system reset is determined by the settings of these pins. To hardwire these inputs low, terminate with a 1 KΩ resister to ground. For a logic high, terminate with a 1 KΩ resistor to VDDA. Do not change the state of these inputs after power-up. Boot 3 should always be tied to logic low. |

**Table 2. i.MX21 Signal Descriptions (Continued)**

| Signal Name | Function/Notes |
|---|---|
| **SDRAM Controller** | |
| SDBA [4:0] | SDRAM non-interleave mode bank address signals. These signals are multiplexed with address signals A[20:16]. |
| SDIBA [3:0] | SDRAM interleave addressing mode bank address signals. These signals are multiplexed with address signals A[24:21]. |
| MA [11:0] | SDRAM address signals. MA[9:0] are multiplexed with address signals A[10:1]. |
| DQM [3:0] | SDRAM data qualifier mask multiplexed with $\overline{EB}$[3:0]. DQM3 corresponds to D[31:24], DQM2 corresponds to D[23:16], DQM1 corresponds to D[15:8], and DQM0 corresponds to D[7:0]. |
| $\overline{CSD0}$ | SDRAM Chip Select signal. This signal is multiplexed with the $\overline{CS2}$ signal. This signal is selectable by programming the Function Multiplexing Control Register in the System Control chapter. |
| $\overline{CSD1}$ | SDRAM Chip Select signal. This signal is multiplexed with the $\overline{CS3}$ signal. This signal is selectable by programming the Function Multiplexing Control Register in the System Control chapter. |
| $\overline{RAS}$ | SDRAM Row Address Select signal. |
| $\overline{CAS}$ | SDRAM Column Address Select signal |
| $\overline{SDWE}$ | SDRAM Write Enable signal |
| SDCKE0 | SDRAM Clock Enable 0 |
| SDCKE1 | SDRAM Clock Enable 1 |
| SDCLK | SDRAM Clock |
| **Clocks and Resets** | |
| EXTAL26M | Crystal input (26MHz), or a 16 MHz to 32 MHz oscillator (or square-wave) input when the internal oscillator circuit is shut down. When using an external signal source, feed this input with a square wave signal switching from GND to VDDA. |
| XTAL26M | Oscillator output to external crystal. When using an external signal source, float this output. |
| EXTAL32K | 32 kHz or 32.768 kHz crystal input. When using an external signal source, feed this input with a square wave signal switching from GND to QVDD5. |
| XTAL32K | Oscillator output to external crystal. When using an external signal source, float this output. |
| CLKO | Clock Out signal selected from internal clock signals. Please refer to clock controller for internal clock selection. |
| EXT_48M | This is a special factory test signal. To ensure proper operation, connect this signal to ground. |
| EXT_266M | This is a special factory test signal. To ensure proper operation, connect this signal to ground. |
| $\overline{RESET_IN}$ | Master Reset—External active low Schmitt trigger input signal. When this signal goes active, all modules (except the reset module, SDRAMC module, and the clock control module) are reset. |
| $\overline{RESET_OUT}$ | Reset Out—Internal active low output signal from the Watchdog Timer module and is asserted from the following sources: Power-on reset, External reset ($\overline{RESET_IN}$), and Watchdog time-out. |
| $\overline{POR}$ | Power On Reset—Active low Schmitt trigger input signal. The $\overline{POR}$ signal is normally generated by an external RC circuit designed to detect a power-up event. |
| CLKMODE[1:0] | These are special factory test signals. To ensure proper operation, leave these signals as no connects. |
| OSC26M_TEST | This is a special factory test signal. To ensure proper operation, leave this signal as a no connect. |
| TEST_WB[2:0] | These are special factory test signals. However, these signals are also multiplexed with GPIO PORT E as well as alternate keypad signals. If not using these signals for GPIO functions or for other multiplexed functions, then configure as GPIO input with pull-up enabled, and leave as a no connect. |

**Table 2. i.MX21 Signal Descriptions (Continued)**

| Signal Name | Function/Notes |
|---|---|
| TEST_WB[4:3] | These are special factory test signals. To ensure proper operation, leave these signals as no connects. |
| WKGD | Battery indicator input used to qualify the walk-up process. Also multiplexed with TIN. |
| **JTAG**<br>For termination recommendations, see the Table "*JTAG pinouts*" in the *Multi-ICE® User Guide* from ARM® Limited. | |
| $\overline{\text{TRST}}$ | Test Reset Pin—External active low signal used to asynchronously initialize the JTAG controller. |
| TDO | Serial Output for test instructions and data. Changes on the falling edge of TCK. |
| TDI | Serial Input for test instructions and data. Sampled on the rising edge of TCK. |
| TCK | Test Clock to synchronize test logic and control register access through the JTAG port. |
| TMS | Test Mode Select to sequence the JTAG test controller's state machine. Sampled on the rising edge of TCK. |
| JTAG_CTRL | JTAG Controller select signal—JTAG_CTRL is sampled during the rising edge of TRST. Must be pulled to logic high for proper JTAG interface to debugger. Pulling JTAG_CRTL low is for internal test purposes only. |
| RTCK | JTAG Return Clock used to enhance stability of JTAG debug interface devices. This signal is multiplexed with 1-Wire, therefore using 1-Wire renders RTCK unusable and vice versa. |
| **CMOS Sensor Interface** | |
| CSI_D [7:0] | Sensor port data |
| CSI_MCLK | Sensor port master clock |
| CSI_VSYNC | Sensor port vertical sync |
| CSI_HSYNC | Sensor port horizontal sync |
| CSI_PIXCLK | Sensor port data latch clock |
| **LCD Controller** | |
| LD [17:0] | LCD Data Bus—All LCD signals are driven low after reset and when LCD is off. LD[15:0] signals are multiplexed with SLCDC1_DAT[15:0] from SLCDC1 and BMI_D[15:0]. LD[17] signal is multiplexed with $\overline{\text{BMI_WRITE}}$ of BMI. LD[16] is multiplexed with BMI_READ_REQ of BMI and $\overline{\text{EXT_DMAGRANT}}$. |
| FLM_VSYNC (or simply referred to as VSYNC) | Frame Sync or Vsync—This signal also serves as the clock signal output for gate driver (dedicated signal SPS for Sharp panel HR-TFT). This signal is multiplexed with BMI_RXF_FULL and $\overline{\text{BMI_WAIT}}$ of the BMI. |
| LP_HSYNC (or simply referred to as HSYNC) | Line Pulse or HSync |
| LSCLK | Shift Clock. This signal is multiplexed with the BMI_CLK_CS from BMI. |
| OE_ACD | Alternate Crystal Direction/Output Enable. |
| CONTRAST | This signal is used to control the LCD bias voltage as contrast control. This signal is multiplexed with the $\overline{\text{BMI_READ}}$ from BMI. |
| SPL_SPR | Sampling start signal for left and right scanning. This signal is multiplexed with the SLCDC1_CLK. |
| PS | Control signal output for source driver (Sharp panel dedicated signal). This signal is multiplexed with the SLCDC1_CS. |
| CLS | Start signal output for gate driver. This signal is invert version of PS (Sharp panel dedicated signal). This signal is multiplexed with the SLCDC1_RS. |
| REV | Signal for common electrode driving signal preparation (Sharp panel dedicated signal). This signal is multiplexed with SLCDC1_D0. |

**Table 2. i.MX21 Signal Descriptions (Continued)**

| Signal Name | Function/Notes |
|---|---|
| **Smart LCD Controller** | |
| SLCDC1_CLK | SLCDC Clock output signal. This signal is multiplexed and available at 2 alternate locations. These are SPL_SPR and SD2_CLK signals of LCDC and SD2, respectively. |
| SLCDC1_CS | SLCDC Chip Select output signal. This signal is multiplexed and available at 2 alternate signal locations. These are PS and SD2_CMD signals of LCDC and SD2, respectively. |
| SLCDC1_RS | SLCDC Register Select output signal. This signal is multiplexed and available at 2 alternate signal locations. These are CLS and SD2_D3 signals of LCDC and SD2, respectively. |
| SLCDC1_D0 | SLCDC serial data output signal. This signal is multiplexed and available at 2 alternate signal locations. These are and REV and SD2_D2 signals of LCDC and SD2, respectively. This signal is inactive when a parallel data interface is used. |
| SLCDC1_DAT[15:0] | SLCDC Data output signals for connection to a parallel SLCD panel interface. These signals are multiplexed with LD[15:0] while an alternate 8-bit SLCD muxing is available on LD[15:8]. Further alternate muxing of these signals are available on some of the USB OTG and USBH1 signals. |
| SLCDC2_CLK | SLCDC Clock input signal for pass through to SLCD device. This signal is multiplexed with SSI3_CLK signal from SSI3. |
| SLCDC2_CS | SLCDC Chip Select input signal for pass through to SLCD device. This signal is multiplexed with SSI3_TXD signal from SSI3. |
| SLCDC2_RS | SLCDC Register Select input signal for pass through to SLCD device. This signal is multiplexed with SSI3_RXD signal from SSI3. |
| SLCDC2_D0 | SLCD Data input signal for pass through to SLCD device. This signal is multiplexed with SSI3_FS signal from SSI3. |
| **Bus Master Interface (BMI)** | |
| BMI_D[15:0] | BMI bidirectional data bus. Bus width is programmable between 8-bit or 16-bit.These signals are multiplexed with LD[15:0] and SLCDC_DAT[15:0]. |
| BMI_CLK_CS | BMI bidirectional clock or chip select signal.This signal is multiplexed with LSCLK of LCDC. |
| $\overline{\text{BMI_WRITE}}$ | BMI bidirectional signal to indicate read or write access. This is an input signal when the BMI is a slave and an output signal when BMI is the master of the interface. $\overline{\text{BMI_WRITE}}$ is asserted for write and negated for read.This signal is muxed with LD[17] of LCDC. |
| $\overline{\text{BMI_READ}}$ | BMI output signal to enable data read from external slave device. This signal is not used and driven high when BMI is slave.This signal is multiplexed with CONTRAST signal of LCDC. |
| BMI_READ_REQ | BMI Read request output signal to external bus master. This signal is active when the data in the TXFIFO is larger or equal to the data transfer size of a single external BMI access.This signal is muxed with LD[16] of LCDC. |
| BMI_RXF_FULL | BMI Receive FIFO full active high output signal to reflect if the RxFIFO reaches water mark value.This signal is muxed with VSYNC of the LCDC. |
| $\overline{\text{BMI_WAIT}}$ | BMI Wait—Active low signal to wait for data ready (read cycle) or accepted (write_cycle). Also multiplexed with VSYNC. |
| **External DMA** | |
| $\overline{\text{EXT_DMAREQ}}$ | External DMA Request input signal. This signal is multiplexed with CSPI1_$\overline{\text{RDY}}$. |
| $\overline{\text{EXT_DMAGRANT}}$ | External DMA Grant output signal. This signal is multiplexed with LD[16] of LCDC and CSPI1_SS1 of CSPI1. |

**Table 2. i.MX21 Signal Descriptions (Continued)**

| Signal Name | Function/Notes |
|---|---|
| **NAND Flash Controller** | |
| NF_CLE | NAND Flash Command Latch Enable output signal. Multiplexed with PC_POE of PCMCIA. |
| $\overline{\text{NF_CE}}$ | NAND Flash Chip Enable output signal. This signal is multiplexed with PC_CE1 of PCMCIA. |
| $\overline{\text{NF_WP}}$ | NAND Flash Write Protect output signal. This signal is multiplexed with PC_CE2 of PCMCIA. |
| NF_ALE | NAND Flash Address Latch Enable output signal. This signal is multiplexed with $\overline{\text{PC_OE}}$ of PCMCIA. |
| $\overline{\text{NF_RE}}$ | NAND Flash Read Enable output signal. This signal is multiplexed with $\overline{\text{PC_RW}}$ of PCMCIA. |
| $\overline{\text{NF_WE}}$ | NAND Flash Write Enable output signal. This signal is multiplexed with and PC_BVD2 of PCMCIA. |
| NF_RB | NAND Flash Ready Busy input signal. This signal is multiplexed with PC_RST of PCMCIA. |
| NF_IO[15:0] | NAND Flash Data input and output signals. NF_IO[15:7] signals are multiplexed with A[25:21] and A[15:13]. NF_IO[7:0] signals are multiplexed with several PCMCIA signals. |
| **PCMCIA Controller** | |
| PC_A[25:0] | PCMCIA Address signals. These signals are multiplexed with A[25:0]. |
| PC_D[15:0] | PCMCIA Data input and output signals. These signals are multiplexed with D[15:0]. |
| $\overline{\text{PC_CD1}}$ | PCMCIA Card Detect1 input signal. This signal is multiplexed with NFIO[7] signal of NF. |
| $\overline{\text{PC_CD2}}$ | PCMCIA Card Detect2 input signal. This signal is multiplexed with NFIO[6] signal of NF. |
| $\overline{\text{PC_WAIT}}$ | PCMCIA Wait input signal to extend current access. This signal is multiplexed with NFIO[5] signal of NF. |
| PC_READY | PCMCIA Ready input signal indicates card is ready for access. Multiplexed with NFIO[4] signal of NF. |
| PC_RST | PCMCIA Reset output signal. This signal is multiplexed with NFRB signal of NF. |
| $\overline{\text{PC_OE}}$ | PCMCIA Memory Read Enable output signal asserted during common or attribute memory read cycles. This signal is multiplexed with NFALE signal of NF. |
| $\overline{\text{PC_WE}}$ | PCMCIA Memory Write Enable output signal asserted during common or attribute memory cycles. This signal is shared with $\overline{\text{RW}}$ of the EIM. |
| PC_VS1 | PCMCIA Voltage Sense1 input signal. This signal is multiplexed with NFIO[2] signal of NF. |
| PC_VS2 | PCMCIA Voltage Sense2 input signal. This signal is multiplexed with NFIO[1] signal of NF. |
| PC_BVD1 | PCMCIA Battery Voltage Detect1 input signal. This signal is multiplexed with NFIO[0] signal of NF. |
| PC_BVD2 | PCMCIA Battery Voltage Detect2 input signal. This signal is multiplexed with $\overline{\text{NF_WE}}$ signal of NF. |
| PC_SPKOUT | PCMCIA Speaker Out output signal. This signal is multiplexed with PWMO signal. |
| $\overline{\text{PC_REG}}$ | PCMCIA Register Select output signal. This signal is shared with $\overline{\text{EB2}}$ of EIM. |
| PC_CE1 | PCMCIA Card Enable1 output signal. This signal is multiplexed with $\overline{\text{NFCE}}$ signal of NF. |
| PC_CE2 | PCMCIA Card Enable2 output signal. This signal is multiplexed with $\overline{\text{NFWP}}$ signal of NF. |
| $\overline{\text{PC_IORD}}$ | PCMCIA IO Read output signal. This signal is shared with $\overline{\text{EB3}}$ of EIM. |
| $\overline{\text{PC_IOWR}}$ | PCMCIA IO Write output signal. This signal is shared with $\overline{\text{OE}}$ signal of EIM. |
| PC_WP | PCMCIA Write Protect input signal. This signal is multiplexed with NFIO[3] signal of NF. |
| PC_POE | PCMCIA Output Enable signal to enable voltage translation buffers and transceivers. This signal is multiplexed with NFCLE signal of NF. |
| $\overline{\text{PC_RW}}$ | PCMCIA Read Write output signal to control external transceiver direction. Asserted high for read access and negated low for write access. This signal is multiplexed with $\overline{\text{NFRE}}$ signal of NF. |
| PC_PWRON | PCMCIA input signal to indicate that the card power has been applied and stabilized. |

**Table 2. i.MX21 Signal Descriptions (Continued)**

| Signal Name | Function/Notes |
|---|---|
| **CSPI** | |
| CSPI1_MOSI | Master Out/Slave In signal |
| CSPI1_MISO | Master In/Slave Out signal |
| CSPI1_SS[2:0] | Slave Select (Selectable polarity) signal. CSPI1_SS2 is also multiplexed with USBG_RXDAT and CSPI1_SS1 is multiplexed with $\overline{\text{EXT_DMAGRANT}}$. |
| CSPI1_SCLK | Serial Clock signal |
| CSPI1_$\overline{\text{RDY}}$ | Serial Data Ready signal. Also multiplexed with $\overline{\text{EXT_DMAREQ}}$. |
| CSPI2_MOSI | Master Out/Slave In signal. This signal is multiplexed with USBH2_TXDP signal of USB OTG. |
| CSPI2_MISO | Master In/Slave Out signal. This signal is multiplexed with USBH2_TXDM signal of USB OTG. |
| CSPI2_SS[2:0] | Slave Select (Selectable polarity) signals. These signals are multiplexed with USBH2_FS, USBH2_RXDP and USBH2_RXDM signal of USB OTG |
| CSPI2_SCLK | Serial Clock signal. This signal is multiplexed with $\overline{\text{USBH2_OE}}$ signal of USB OTG |
| CSPI3_MOSI | Master Out/Slave In signal. This signal is multiplexed with SD1_CMD. |
| CSPI3_MISO | Master In/Slave Out signal. This signal is multiplexed with SD1_D0. |
| CSPI3_SS | Slave Select (Selectable polarity) signal multiplexed with SD1_D3. |
| CSPI3_SCLK | Serial Clock signal. This signal is multiplexed with SD1_CLK. |
| **General Purpose Timers** | |
| TIN | Timer Input Capture or Timer Input Clock—The signal on this input is applied to all 3 timers simultaneously. This signal is muxed with the Walk-up Guard Mode $\overline{\text{WKGD}}$ signal in the PLL, Clock, and Reset Controller module. |
| TOUT1 (or simply TOUT) | Timer Output signal from General Purpose Timer1 (GPT1). This signal is multiplexed with SYS_CLK1 and SYS_CLK2 signal of SSI1 and SSI2. The pin name of this signal is simply TOUT. |
| TOUT2 | Timer Output signal from General Purpose Timer1 (GPT2). This signal is multiplexed with PWMO. |
| TOUT3 | Timer Output signal from General Purpose Timer1 (GPT3). This signal is multiplexed with PWMO. |
| **USB On-The-Go** | |
| $\overline{\text{USB_BYP}}$ | USB Bypass input active low signal. This signal can only be used for USB function, not for GPIO. |
| USB_PWR | USB Power output signal |
| $\overline{\text{USB_OC}}$ | USB Over current input signal. This signal can only be used for USB function, not for GPIO. |
| USBG_RXDP | USB OTG Receive Data Plus input signal. This signal is muxed with SLCDC1_DAT15. |
| USBG_RXDM | USB OTG Receive Data Minus input signal. This signal is muxed with SLCDC1_DAT14. |
| USBG_TXDP | USB OTG Transmit Data Plus output signal. This signal is muxed with SLCDC1_DAT13. |
| USBG_TXDM | USB OTG Transmit Data Minus output signal. This signal is muxed with SLCDC1_DAT12. |
| USBG_RXDAT | USB OTG Transceiver differential data receive signal. Multiplexed with CSPI1_SS2. |
| $\overline{\text{USBG_OE}}$ | USB OTG Output Enable signal. This signal is muxed with SLCDC1_DAT11. |
| $\overline{\text{USBG_ON}}$ | USB OTG Transceiver ON output signal. This signal is muxed with SLCDC1_DAT9. |
| USBG_FS | USB OTG Full Speed output signal. This signal is multiplexed with external transceiver $\overline{\text{USBG_TXR_INT}}$ signal of USB OTG. This signal is muxed with SLCDC1_DAT10. |

**Table 2. i.MX21 Signal Descriptions (Continued)**

| Signal Name | Function/Notes |
|---|---|
| USBH1_RXDP | USB Host1 Receive Data Plus input signal. This signal is multiplexed with UART4_RXD and SLCDC1_DAT6. It also provides an alternative multiplex for $\overline{\text{UART4_RTS}}$, where this signal is selectable by programming the Function Multiplexing Control Register in the System Control chapter. |
| USBH1_RXDM | USB Host1 Receive Data Minus input signal. This signal is muxed with SLCDC1_DAT5. It also provides an alternative multiplex for $\overline{\text{UART4_CTS}}$. |
| USBH1_TXDP | USB Host1 Transmit Data Plus output signal. This signal is multiplexed with $\overline{\text{UART4_CTS}}$ and SLCDC1_DAT4. It also provides an alternative multiplex for UART4_RXD, where this signal is selectable by programming the Function Multiplexing Control Register in the System Control chapter. |
| USBH1_TXDM | USB Host1 Transmit Data Minus output signal. Multiplexed with UART4_TXD and SLCDC1_DAT3. |
| USBH1_RXDAT | USB Host1 Transceiver differential data receive signal. Multiplexed with USBH1_FS. |
| $\overline{\text{USBH1_OE}}$ | USB Host1 Output Enable signal. This signal is muxed with SLCDC1_DAT2. |
| USBH1_FS | USB Host1 Full Speed output signal. Multiplexed with $\overline{\text{UART4_RTS}}$ and SLCDC1_DAT1 and USBH1_RXDAT. |
| $\overline{\text{USBH_ON}}$ | USB Host transceiver ON output signal. This signal is muxed with SLCDC1_DAT0. |
| USBH2_RXDP | USB Host2 Receive Data Plus input signal. This signal is multiplexed with CSPI2_SS[1] of CSPI2. |
| USBH2_RXDM | USB Host2 Receive Data Minus input signal. This signal is multiplexed with CSPI2_SS[2] of CSPI2. |
| USBH2_TXDP | USB Host2 Transmit Data Plus output signal. This signal is multiplexed with CSPI2_MOSI of CSPI2. |
| USBH2_TXDM | USB Host2 Transmit Data Minus output signal. This signal is multiplexed with CSPI2_MISO of CSPI2. |
| $\overline{\text{USBH2_OE}}$ | USB Host2 Output Enable signal. This signal is multiplexed with CSPI2_SCLK of CSPI2. |
| USBH2_FS | USB Host2 Full Speed output signal. This signal is multiplexed with CSPI2_SS[0] of CSPI2. |
| USBG_SCL | USB OTG $I^2C$ Clock input/output signal. This signal is multiplexed with SLCDC1_DAT8. |
| USBG_SDA | USB OTG $I^2C$ Data input/output signal. This signal is multiplexed with SLCDC1_DAT7. |
| $\overline{\text{USBG_TXR_INT}}$ | USB OTG transceiver interrupt input. Multiplexed with USBG_FS. |
| **Secure Digital Interface** | |
| SD1_CMD | SD Command bidirectional signal—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 4.7k–69k external pull-up resistor must be added. This signal is multiplexed with CSPI3_MOSI. |
| SD1_CLK | SD Output Clock. This signal is multiplexed with CSPI3_SCLK. |
| SD1_D[3:0] | SD Data bidirectional signals—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 50k–69k external pull-up resistor must be added. SD1_D[3] is muxed with CSPI3_SS while SD1_D[0] is muxed with CSPI3_MISO. |
| SD2_CMD | SD Command bidirectional signal. This signal is multiplexed with SLCDC1_CS signal from SLCDC1. |
| SD2_CLK | SD Output Clock signal. This signal is multiplexed with SLCDC1_CLK signal from SLCDC1. |
| SD2_D[3:0] | SD Data bidirectional signals. SD2_D[3:2] are multiplexed with SLCDC1_RS and SLCDC_D0 signals from SLCDC1. |
| **UARTs – IrDA/Auto-Bauding** | |
| UART1_RXD | Receive Data input signal |
| UART1_TXD | Transmit Data output signal |
| $\overline{\text{UART1_RTS}}$ | Request to Send input signal |
| $\overline{\text{UART1_CTS}}$ | Clear to Send output signal |

**Table 2. i.MX21 Signal Descriptions (Continued)**

| Signal Name | Function/Notes |
|---|---|
| UART2_RXD | Receive Data input signal. This signal is multiplexed with KP_ROW6 signal from KPP. |
| UART2_TXD | Transmit Data output signal. This signal is multiplexed with KP_COL6 signal from KPP. |
| $\overline{\text{UART2_RTS}}$ | Request to Send input signal. This signal is multiplexed with KP_ROW7 signal from KPP. |
| $\overline{\text{UART2_CTS}}$ | Clear to Send output signal. This signal is multiplexed with KP_COL7 signal from KPP. |
| UART3_RXD | Receive Data input signal. This signal is multiplexed with IR_RXD from FIRI. |
| UART3_TXD | Transmit Data output signal. This signal is multiplexed with IR_TXD from FIRI. |
| $\overline{\text{UART3_RTS}}$ | Request to Send input signal |
| $\overline{\text{UART3_CTS}}$ | Clear to Send output signal |
| UART4_RXD | Receive Data input signal which is multiplexed with USBH1_RXDP and USBH1_TXDP. |
| UART4_TXD | Transmit Data output signal which is multiplexed with USBH1_TXDM. |
| $\overline{\text{UART4_RTS}}$ | Request to Send input signal which is multiplexed with USBH1_FS and USBH1_RXDP. |
| $\overline{\text{UART4_CTS}}$ | Clear to Send output signal which is multiplexed with USBH1_TXDP and USBH1_RXDM. |
| **Serial Audio Port – SSI (configurable to $I^2S$ protocol and AC97)** | |
| SSI1_CLK | Serial clock signal which is output in master or input in slave |
| SSI1_TXD | Transmit serial data |
| SSI1_RXD | Receive serial data |
| SSI1_FS | Frame Sync signal which is output in master and input in slave |
| SYS_CLK1 | SSI1 master clock. Multiplexed with TOUT. |
| SSI2_CLK | Serial clock signal which is output in master or input in slave. |
| SSI2_TXD | Transmit serial data signal |
| SSI2_RXD | Receive serial data |
| SSI2_FS | Frame Sync signal which is output in master and input in slave. |
| SYS_CLK2 | SSI2 master clock. Multiplexed with TOUT. |
| SSI3_CLK | Serial clock signal which is output in master or input in slave. Multiplexed with SLCDC2_CLK |
| SSI3_TXD | Transmit serial data signal which is multiplexed with SLCDC2_CS |
| SSI3_RXD | Receive serial data which is multiplexed with SLCDC2_RS |
| SSI3_FS | Frame Sync signal which is output in master and input in slave. Multiplexed with SLCDC2_D0. |
| SAP_CLK | Serial clock signal which is output in master or input in slave. |
| SAP_TXD | Transmit serial data |
| SAP_RXD | Receive serial data |
| SAP_FS | Frame Sync signal which is output in master and input in slave. |
| **$I^2C$** | |
| I2C_CLK | $I^2C$ Clock |
| I2C_DATA | $I^2C$ Data |
| **1-Wire** | |
| OWIRE | 1-Wire input and output signal. This signal is multiplexed with JTAG RTCK. |

**Table 2. i.MX21 Signal Descriptions (Continued)**

| Signal Name | Function/Notes |
|---|---|
| **PWM** | |
| PWMO | PWM Output. This signal is multiplexed with PC_SPKOUT of PCMCIA, as well as TOUT2 and TOUT3 of the General Purpose Timer module. |
| **General Purpose Input/Output** | |
| PF[16] | Dedicated GPIO. When unused, program this signal as an input with the on-chip pull-up resistor enabled. |
| **Keypad** | |
| KP_COL[7:0] | Keypad Column selection signals. KP_COL[7:6] are multiplexed with $\overline{\text{UART2_CTS}}$ and UART2_TXD respectively. Alternatively, KP_COL6 is also available on the internal factory test signal TEST_WB2. The Function Multiplexing Control Register in the System Control chapter must be used in conjunction with programming the GPIO multiplexing (to select the alternate signal multiplexing) to choose which signal KP_COL6 is available. |
| KP_ROW[7:0] | Keypad Row selection signals. KP_ROW[7:6] are multiplexed with $\overline{\text{UART2_RTS}}$ and UART2_RXD signals respectively. Alternatively, KP_ROW7 and KP_ROW6 are available on the internal factory test signals TEST_WB0 and TEST_WB1 respectively. The Function Multiplexing Control Register in the System Control chapter must be used in conjunction with programming the GPIO multiplexing (to select the alternate signal multiplexing) to choose which signals KP_ROW6 and KP_ROW7 are available. |
| **Noisy Supply Pins** | |
| NVDD | Noisy Supply for the I/O pins. There are six (6) I/O voltages, NVDD1 through NVDD6. |
| NVSS | Noisy Ground for the I/O pins |
| **Supply Pins – Analog Modules** | |
| VDDA | Supply for analog blocks |
| QVSS (internally connected to AVSS) | Quiet GND for analog blocks (QVSS and AVSS are synonymous) |
| **Internal Power Supplies** | |
| QVDD | Power supply pins for silicon internal circuitry |
| QVSS | Quiet GND pins for silicon internal circuitry |
| QVDDX | Power supply pin for the ARM core. Externally connect directly to QVDD |

# 3 Specifications

This section contains the electrical specifications and timing diagrams for the i.MX21 processor.

## 3.1 Maximum Ratings

Table 3 provides the maximum ratings.

**CAUTION**

Stresses beyond those listed under "Maximum Ratings," (Table 3) may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "333/350 MHz Recommended Operating Range" (Table 4) is not implied. Exposure to maximum-rated conditions for extended periods may affect device reliability.

**Table 3. Maximum Ratings**

| Ref. Num | Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|---|
| 1 | Supply Voltage | $QVDD_{max}$, $QVDDX_{max}$ | -0.3 | 2.1 | V |
| | | $NVDD_{max}$, $VDDA_{max}$ | -0.3 | 3.3 | V |
| 2 | Input Voltage Range | $V_{Imax}$ | -0.3 | VDD + 0.3[1] | V |
| 3 | Storage Temperature Range | $T_{storage}$ | -55 | 150 | °C |

1. VDD is the supply voltage associated with the input. See *Signal Multiplexing Scheme* table in the reference manual.

## 3.2 Recommended Operating Range

Table 4 provides the recommended operating ranges. The device has multiple pairs of VDD and VSS power supply and return pins. QVDD, QVDDx, and QVSS pins are used for internal logic. All other VDD and VSS pins are for the I/O pads voltage supply, and each pair of VDD and VSS provides power to the enclosed I/O pads. This design allows different peripheral supply voltage levels in a system.

Because VDDA pins are supply voltages to the analog pads, it is recommended to isolate and noise-filter the VDDA pins from other VDD pins.

For more information about I/O pads grouping per VDD, please refer to Table 4.

**Table 4. 333/350 MHz Recommended Operating Range**

| Rating | | Symbol | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| Operating temperature range | **Part No. Suffix** | | | | |
| | DVKN | $T_A$ | -30 | 70 | °C |
| I/O supply voltage NVDD 1–6 | | NVDDx | 1.70 | 3.30 | V |
| Internal supply voltage (Core = 333 MHz) | | QVDD, QVDDx | 1.65 | 1.80 | V |
| Internal supply voltage (Core = 350 MHz) | | QVDD, QVDDx | 1.70 | 1.80 | V |
| Analog supply voltage | | VDDA | 1.70 | 3.30 | V |

## 3.3 DC Electrical Characteristics

Table 5 contains the DC characteristics of the i.MX21.

**Table 5. DC Characteristics**

| Parameter | Symbol | Test Conditions | Min | Typ[1] | Max | Units |
|---|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | – | 0.7NVDD | – | NVDD | |
| Low-level Input voltage | $V_{IL}$ | – | O | – | 0.3NVDD | |
| High-level output voltage | $V_{OH}$ | $I_{OH}$ = spec'ed Drive | 0.8NVDD | – | – | V |
| Low-level output voltage | $V_{OL}$ | $I_{OL}$ = spec'ed Drive | – | – | 0.2NVDD | V |
| High-level output current, slow I/O | $I_{OH_S}$ | $V_{out}$=0.8NVDD<br>DSCR[2] = 000<br>DSCR = 001<br>DSCR = 011<br>DSCR = 111 | <br>-2<br>-4<br>-8<br>-12 | – | – | mA |
| High-level output current, fast I/O | $I_{OH_F}$ | $V_{out}$=0.8NVDD1<br>DSCR[2] = 000<br>DSCR = 001<br>DSCR = 011<br>DSCR = 111 | <br>-3.5<br>-4.5<br>-5.5<br>-6.5 | – | – | mA |
| Low-level output current, slow I/O | $I_{OL_S}$ | $V_{out}$=0.2NVDD<br>DSCR[2] = 000<br>DSCR = 001<br>DSCR = 011<br>DSCR = 111 | <br>2<br>4<br>8<br>12 | – | – | mA |
| Low-level output current, fast I/O | $I_{OL_F}$ | $V_{out}$=0.2NVDD1<br>DSCR[2] = 000<br>DSCR = 001<br>DSCR = 011<br>DSCR = 111 | <br>3.5<br>4.5<br>5.5<br>6.5 | – | – | mA |
| Schmitt trigger Positive–input threshold | $V_T$ + | – | – | – | 2.15 | V |
| Schmitt trigger Negative–input threshold | $V_T$ - | | 0.75 | – | – | V |
| Hysteresis | $V_{HYS}$ | – | – | 0.3 | – | V |
| Input leakage current (no pull-up or pull-down) | $I_{in}$ | $V_{in}$ = 0 or NVDD | – | – | ±1 | µA |
| I/O leakage current | $I_{OZ}$ | $V_{I/O}$ = NVDD or 0<br>I/O = High impedance state | – | – | ±5 | µA |

1. Data labeled Typical is not guaranteed, but is intended as an indication of the IC's potential performance.
2. For DSCR definition refer to the System Control chapter in the reference manual.

Table 6 shows the input and output capacitance for the device.

**Table 6. Input/Output Capacitance**

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Input capacitance | $C_i$ | _ | _ | 5 | pF |
| Output capacitance | $C_o$ | _ | _ | 5 | pF |

Table 7 shows the power consumption for the device.

**Table 7. Power Consumption**

| ID | Parameter | Conditions | Symbol | Typ | Max | Units |
|---|---|---|---|---|---|---|
| 1 | Run Current | QVDD = QVDDX = 1.80V (333MHz), NVDD1 = 1.7V. NVDD2 through NVDD6 = VDDA = 3.1V. Core = 333 MHz, System = 111 MHz. MPEG4 Playback (QVGA) from MMC/SD card, 30fps, 44.1kHz audio. | $I_{QVDD} + I_{QVDDX}$ | 180 | – | mA |
| | | | $I_{NVDD1}$ | 8 | – | mA |
| | | | $I_{NVDD2}$ through $I_{NVDD6} + I_{VDDA}$ | 6.6 | – | mA |
| 2 | Sleep Current | Standby current with Well Biasing System enabled.<br>Well Bias Control Register (WBCR) must be set as follows:<br>WBCR:<br>CRM_WBS bits = 01<br>CRM_WBFA bit = 1<br>CRM_WBM bits = 001<br>CRM_SPA_SEL bit = 1<br>FMCR bit = 1<br>For WBCR definition refer to System Control Chapter in the reference manual. | **$I_{STBY}$** | | | |
| | | | QVDD = QVDDX = 1.80V, 70° | – | 6 | mA |
| | | | QVDD = QVDDX = 1.80V, 25° | – | 3 | mA |

## 3.4 AC Electrical Characteristics

The AC characteristics consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of other signals. All timing specifications are specified at a system operating frequency (HCLK) from 0 MHz to 117 MHz (core operating frequency 333 or 350 MHz) with an operating supply voltage from $V_{DD\ min}$ to $V_{DD\ max}$ under an operating temperature from $T_L$ to $T_H$. All timing is measured at 30 pF loading with the exception of fast I/O signals which is measured at 21 pF at a 6.5 mA drive strength setting. Refer to the reference manual's System Control Chapter for details on drive strength settings.

**Table 8. 32k/26M Oscillator Signal Timing**

| Parameter | Minimum | RMS | Maximum | Unit |
|---|---|---|---|---|
| EXTAL32k input jitter (peak to peak) for both System PLL and MCUPLL | – | 5 | 20 | ns |
| EXTAL32k input jitter (peak to peak) for MCUPLL only | – | 5 | 100 | ns |
| EXTAL32k startup time | 800 | – | – | ms |

**Table 9. CLKO Rise/Fall Time (at 30pF Loaded)**

| | Best Case | Typical | Worst Case | Units |
|---|---|---|---|---|
| Rise Time | 0.80 | 1.00 | 1.40 | ns |
| Fall Time | 0.74 | 1.08 | 1.67 | ns |

## 3.5 DPLL Timing Specifications

Parameters of the DPLL are given in Table 10. In this table, $T_{ref}$ is a reference clock period after the predivider and $T_{dck}$ is the output double clock period.

**Table 10. DPLL Specifications**

| Parameter | Test Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| Reference clock frequency range | Vcc = 1.7V | 16 | – | 320 | MHz |
| Pre-divider output clock frequency range | Vcc = 1.7V | 16 | – | 32 | MHz |
| Double clock frequency range | Vcc = 1.7V | 220 | – | 560 | MHz |
| Pre-divider factor (PD) | – | 1 | – | 16 | – |
| Total multiplication factor (MF) | Includes both integer and fractional parts | 5 | – | 15 | – |
| MF integer part | – | 5 | – | 15 | – |
| MF numerator | Should be less than the denominator | 0 | – | 1022 | – |
| MF denominator | – | 1 | – | 1023 | – |
| Frequency lock-in time after full reset | FOL mode for non-integer MF (does not include pre-multi lock-in time) | 350 | 400 | 450 | $T_{ref}$ |
| Frequency lock-in time after partial reset | FOL mode for non-integer MF (does not include pre-multi lock-in time) | 220 | 280 | 330 | $T_{ref}$ |
| Phase lock-in time after full reset | FPL mode and integer MF (does not include pre-multi lock-in time) | 480 | 530 | 580 | $T_{ref}$ |
| Phase lock-in time after partial reset | FPL mode and integer MF (does not include pre-multi lock-in time) | 360 | 410 | 460 | $T_{ref}$ |
| Frequency jitter (p-p) | – | – | 0.02 | 0.03 | $2 \bullet T_{dck}$ |
| Phase jitter (p-p) | Integer MF, FPL mode, Vcc=1.7V | – | 1.0 | 1.5 | ns |
| Power dissipation | FOL mode, integer MF, $f_{dck}$ = 560 MHz, Vcc = 1.7V | – | 1.5 | – | mW (Avg) |

## 3.6 Reset Module

The timing relationships of the Reset module with the $\overline{\text{POR}}$ and $\overline{\text{RESET_IN}}$ are shown in Figure 2 and Figure 3. Be aware that NVDD must ramp up to at least 1.7V for NVDD1 and 2.7V for NVDD2-6 before QVDD is powered up to prevent forward biasing.

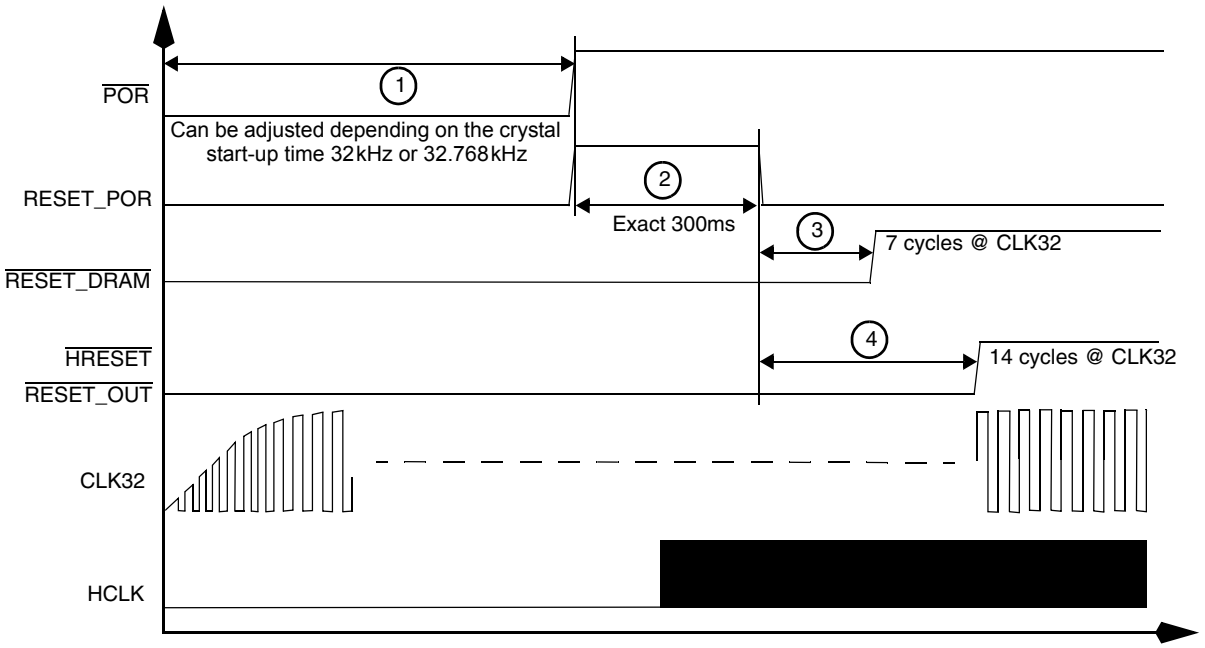



**Figure 2. Timing Relationship with $\overline{\text{POR}}$**

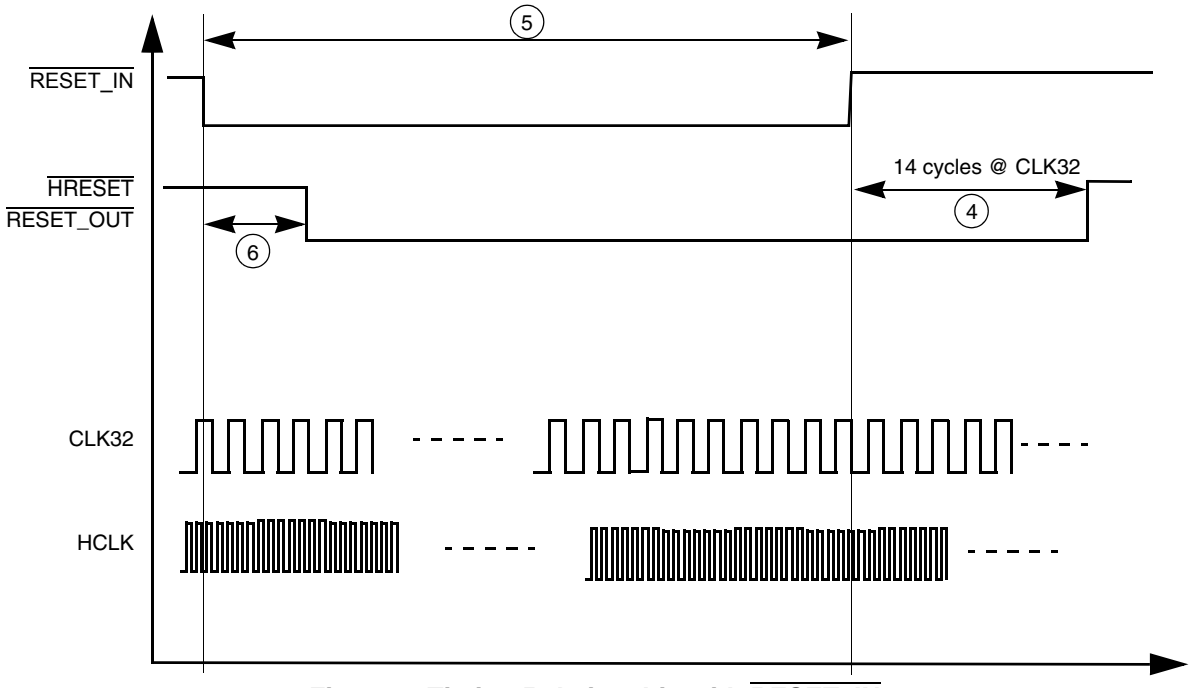



**Figure 3. Timing Relationship with $\overline{\text{RESET_IN}}$**

**Table 11. Reset Module Timing Parameters**

| Ref No. | Parameter | 1.8V ± 0.10V | | 3.0V ± 0.30V | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| 1 | Width of input POWER_ON_RESET | 800 | – | 800 | – | ms |
| 2 | Width of internal $\overline{\text{POWER_ON_RESET}}$ (CLK32 at 32 kHz) | 300 | 300 | 300 | 300 | ms |
| 3 | 7k to 32k-cycle stretcher for SDRAM reset | 7 | 7 | 7 | 7 | Cycles of CLK32 |
| 4 | 14k to 32k-cycle stretcher for internal system reset $\overline{\text{HRESERT}}$ and output reset at pin $\overline{\text{RESET_OUT}}$ | 14 | 14 | 14 | 14 | Cycles of CLK32 |
| 5 | Width of external hard-reset $\overline{\text{RESET_IN}}$ | 4 | – | 4 | – | Cycles of CLK32 |
| 6 | 4k to 32k-cycle qualifier | 4 | 4 | 4 | 4 | Cycles of CLK32 |

## 3.7 External DMA Request and Grant

The External DMA request is an active low signal to be used by devices external to i.MX21 processor to request the DMAC for data transfer.

After assertion of External DMA request the DMA burst will start when the channel on which the External request is the source (as per the RSSR settings) becomes the current highest priority channel. The external device using the External DMA request should keep its request asserted until it is serviced by the DMAC. One External DMA request will initiate one DMA burst.

The output External Grant signal from the DMAC is an active-low signal.When the following conditions are true, the External DMA Grant signal is asserted with the initiation of the DMA burst.

- The DMA channel for which the DMA burst is ongoing has request source as external DMA Request (as per source select register setting).
- REN and CEN bit of this channel are set.
- External DMA Request is asserted.

After the grant is asserted, the External DMA request will not be sampled until completion of the DMA burst. As the external request is synchronized, the request synchronization will not be done during this period. The priority of the external request becomes low for the next consecutive burst, if another DMA request signal is asserted.

Worst case—that is, the smallest burst (1 byte read/write) timing diagrams are shown in Figure 4 and Figure 5. Minimum and maximum timings for the External request and External grant signals are present in Table 12.

Figure 4 shows the minimum time for which the External Grant signal remains asserted when an External DMA request is de-asserted immediately after sensing grant signal active.

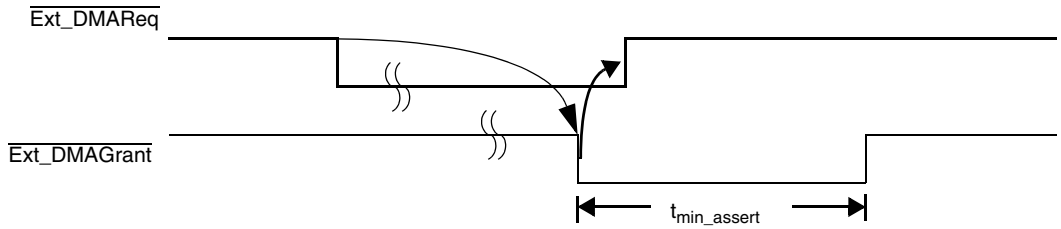
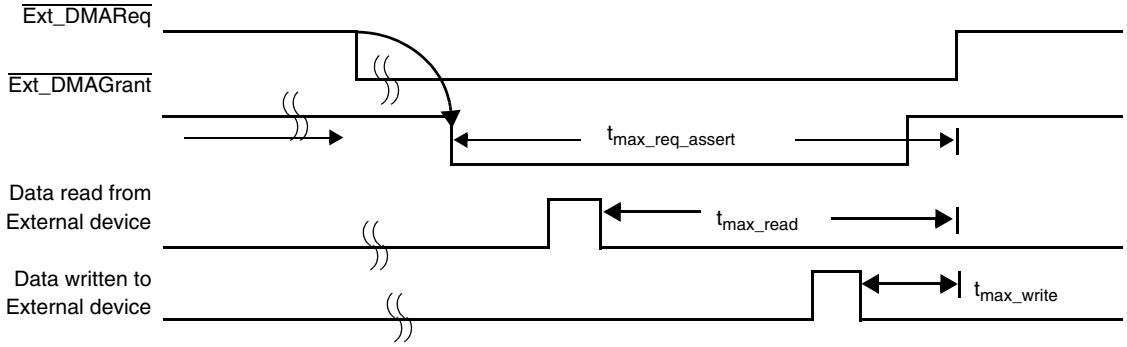



**Figure 4. Assertion of DMA External Grant Signal**

Figure 5 shows the safe maximum time for which External DMA request can be kept asserted, after sensing grant signal active such that a new burst is not initiated.




NOTE: Assuming in worst case the data is read/written from/to External device as per the above waveform.

**Figure 5. Safe Maximum Timings for External Request De-Assertion**

**Table 12. DMA External Request and Grant Timing Parameters**

| Parameter | Description | 3.0 V | | 1.8 V | | Unit |
|---|---|---|---|---|---|---|
| | | WCS | BCS | WCS | BCS | |
| $t_{min_assert}$ | Minimum assertion time of External Grant signal | 8 hclk + 8.6 | 8 hclk + 2.74 | 8 hclk + 7.17 | 8 hclk + 3.25 | ns |
| $t_{max_req_assert}$ | Maximum External request assertion time after assertion of Grant signal | 9 hclk - 20.66 | 9 hclk - 6.7 | 9 hclk - 17.96 | 9 hclk - 8.16 | ns |
| $t_{max_read}$ | Maximum External request assertion time after first read completion | 8 hclk - 6.21 | 8 hclk - 0.77 | 8 hclk - 5.84 | 8 hclk - 0.66 | ns |
| $t_{max_write}$ | Maximum External request assertion time after completion of first write | 3 hclk - 15.87 | 3 hclk - 8.83 | 3 hclk - 15.9 | 3 hclk - 9.12 | ns |

# 3.8 BMI Interface Timing Diagram

## 3.8.1 Connecting BMI to ATI MMD Devices

### 3.8.1.1 ATI MMD Devices Drive the BMI_CLK/CS

In this mode MMD_MODE_SEL bit is set and MMD_CLKOUT bit is cleared. $\overline{\text{BMI_WRITE}}$ and BMI_CLK/CS are input signals to BMI driving by ATI MMD chip set. Output signal BMI_READ_REQ can be used as interrupt signal to inform MMD that data is ready in BMI TxFIFO for read access. MMD

can write data to BMI RxFIFO anytime as CPU or DMA can move data out from RxFIFO much faster than the BMI interface. Overflow interrupt is generated if RxFIFO overflow is detected. Once this happens, the new coming data is ignored.

#### 3.8.1.1.1 MMD Read BMI Timing

Figure 6 shows the MMD read BMI timing when the MMD drives clock.

On each rising edge of BMI_CLK/CS BMI checks the $\overline{\text{BMI_WRITE}}$ logic level to determine if the current cycle is a read cycle. It puts data into the data bus and enables the data out on the rising edge of BMI_CLK/CS if BMI_WRITE is logic high. The BMI_READ_REQ is negated one hclk cycle after the BMI_CLK/CS rising edge of last data read. The MMD cannot issues read command when BMI_READ_REQ is low (no data in TxFIFO).

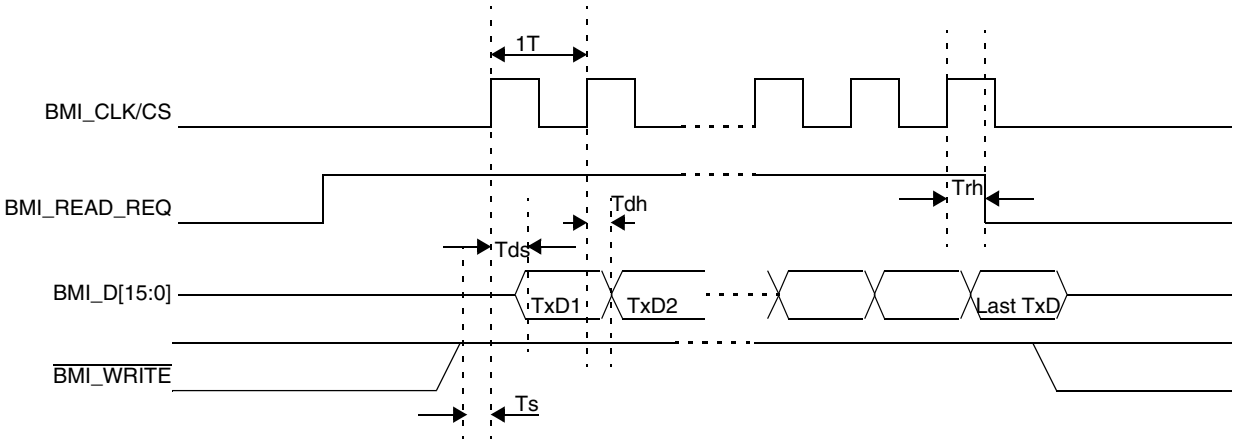



**Figure 6. MMD (ATI) Drives Clock, MMD Read BMI Timing (MMD_MODE_SEL=1, MASTER_MODE_SEL=0,MMD_CLKOUT=0)**

**Table 13. MMD Read BMI Timing Table when MMD Drives Clock**

| Item | Symbol | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| Clock period | 1T | 33.3 | – | – | ns |
| $\overline{\text{write}}$ setup time | Ts | 11 | – | – | ns |
| read_req hold time | Trh | 6 | – | 24 | ns |
| transfer data setup time | Tds | 6 | – | 14 | ns |
| transfer data hold time | Tdh | 6 | - | 14 | ns |

**Note:** All the timings assume that the hclk is running at 133 MHz.

**Note:** The MIN period of the 1T is assumed that MMD latch data at falling edge.

**Note:** If the MMD latch data at next rising edge, the ideally max clock can be as much as double, but because the BMI data pads are slow pads and it max frequency can only up to 18MHz, the max clock frequency can only up to 36 MHz.

#### 3.8.1.1.2 MMD Write BMI Timing

Figure 7 shows the MMD write BMI timing when MMD drives clock. On each falling edge of BMI_CLK/CS BMI checks the BMI_WRITE logic level to determine if the current cycle is a write cycle. If the BMI_WRITE is logic low, it latches data into the RxFIFO on each falling edge of BMI_CLK/CS signal.

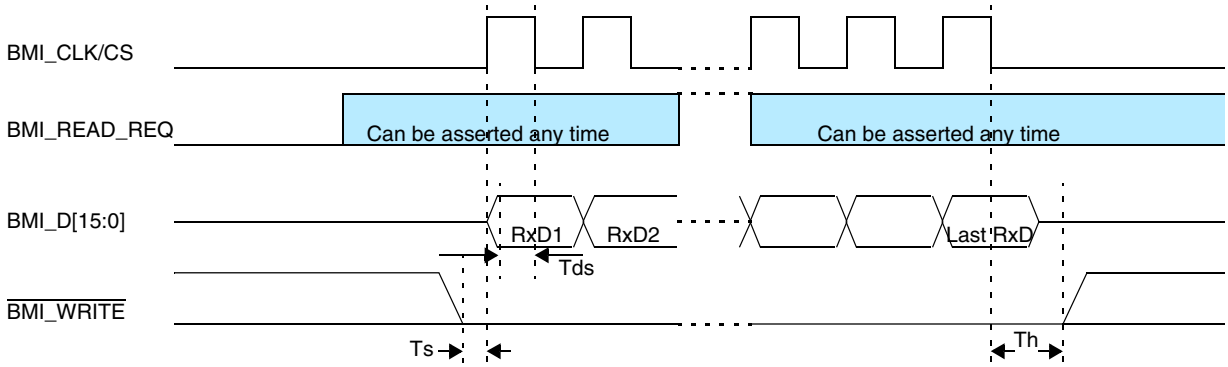



**Figure 7. MMD (ATI) Drives Clock, MMD Write BMI Timing (MMD_MODE_SEL=1, MASTER_MODE_SEL=0, MMD_CLKOUT=0)**

**Table 14. MMD Write BMI Timing**

| Item | Symbol | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| write setup time | Ts | 11 | – | – | ns |
| write hold time | Th | 0 | – | – | ns |
| receive data setup time | Tds | 5 | – | – | ns |

**Note:** All timings assume that the hclk is running at 133 MHz.

**Note:** At this mode, the maximum frequency of the BMI_CLK/CS can be up to 36 MHz (doubles as maximum data pad speed).

### 3.8.1.2 BMI Drives the BMI_CLK/CS

In this mode MMD_MODE_SEL and MMD_CLKOUT are both set. The software must know which mode it is now (READ or WRITE). When the BMI_WRITE is high, BMI drives BMI_CLK/CS out if the TxFIFO is not emptied. When BMI_WRITE is low, user can write a 1 to READ bit of control register1 to issue a write cycle (MMD write BMI).

### 3.8.1.3 MMD Read BMI Timing

Figure 13 shows the MMD read BMI timing when BMI drives the BMI_CLK/CS. When the BMI_WRITE is high, the BMI drives BMI_CLK/CS out if data is written to TxFIFO (BMI_READ_REQ become high), BMI puts data into data bus and enable data out on the rising edge of BMI_CLK/CS. The MMD devices can latch the data on each falling edge of BMI_CLK/CS.

It is recommended that the MMD do not change the BMI_WRITE signal from high to low when the BMI_READ_REQ is asserted. If user writes data to the TxFIFO when the BMI_WRITE is low, the BMI will drive BMI_CLK/CS out once the BMI_WRITE is changed from low to high.

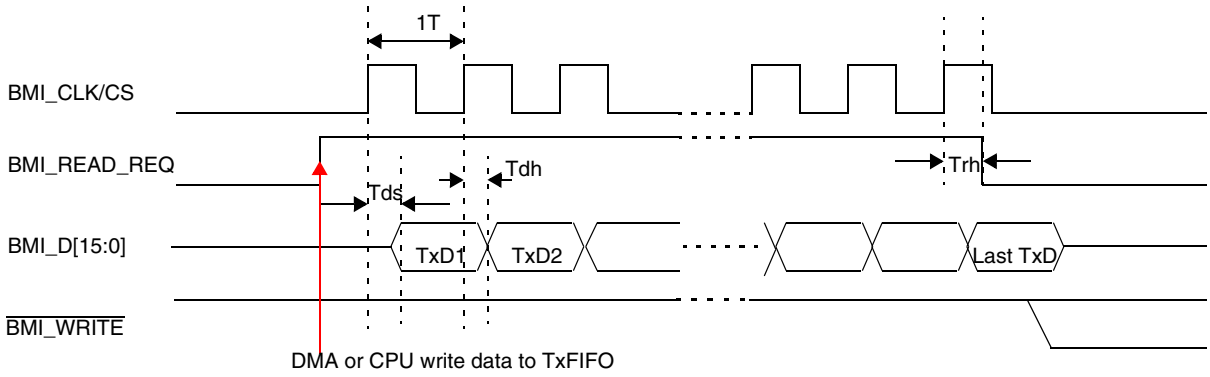



**Figure 8. BMI Drives Clock, MMD Read BMI Timing (MASTER_MODE_SEL=0, MMD_MODE_SEL=1, MMD_CLKOUT=1)**

**Table 15. MMD Read BMI Timing Table when BMI Drives Clock**

| Item | Symbol | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| Transfer data setup time | Tds | 2 | – | 8 | ns |
| Transfer data hold time | Tdh | 2 | – | 8 | ns |
| Read_req hold time | Trh | 2 | – | 18 | ns |

**Note:** In this mode, the max frequency of the BMI_CLK/CS can be up to 36MHz (double as max data pad speed).
**Note:** The BMI_CLK/CS can only be divided by 2,4,8,16 from HCLK.

### 3.8.1.4 MMD Write BMI Timing

Figure 9 shows the MMD write BMI timing when BMI drives BMI_CLK/CS.

When the $\overline{\text{BMI_WRITE}}$ signal is asserted, the BMI can write a 1 to READ bit of control register to issue a WRITE cycle. This bit is cleared automatically when the WRITE operation is completed. In a WRITE burst the MMD will write COUNT+1 data to the BMI. The user can issue another WRITE operation if the MMD still has data to write after the first operation completed.

The BMI can latch the data either at falling edge or the next rising edge of the BMI_CLK/CS according to the DATA_LATCH bit. When the DATA_LATCH bit is set, the BMI latch data at the next rising edge and latch the last data using the internal clock.

$\overline{\text{BMI_WRITE}}$ signal can not be negated when the WRITE operation is proceeding.

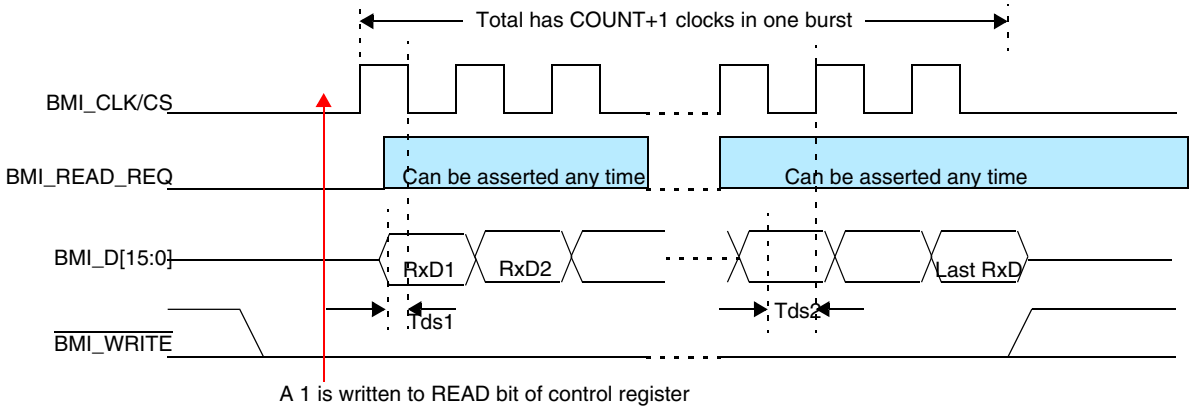



**Figure 9. BMI Drives Clock, MMD Write BMI Timing (MASTER_MODE_SEL=0, MMD_MODE_SEL=1, MMD_CLKOUT=1)**

**Table 16. MMD Write BMI Timing Table when BMI Drives Clock**

| Item | Symbol | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| Receive data setup time1 | Tds1 | 14 | – | – | ns |
| Receive data setup time2 | Tds2 | 14 | – | – | ns |

**Note:** The BMI_CLK/CS can only be up to 30MHz if BMI latch data at the falling edge and can be up to 36MHz (double as max data pad speed) if BMI latch data at the next rising edge.

**Note:** Tds1 is the receive data setup time when BMI latch data at the falling edge.

**Note:** Tds2 is the receive data setup time when BMI latch data at the next rising edge.

## 3.8.2 Connecting BMI to External Bus Master Devices

In this mode both MASTER_SEL bit and MMD_MODE_SEL bit are cleared and the MMD_CLKOUT bit is no useful. $\overline{\text{BMI_WRITE}}$ and BMI_CLK/CS are input signals driving by the external bus master. The Output signal BMI_READ_REQ can be used as an interrupt signal to inform external bus master that data is ready in the BMI TxFIFO for a read access. The external bus master can write data to the BMI RxFIFO anytime since the CPU or DMA can move data out from RxFIFO much faster than the BMI interface. An overflow interrupt is generated if RxFIFO overflow is detected. Once this happens, the new coming data is ignored.

Each falling edge of BMI_CLK/CS will determine if the current cycle is read or write cycle. It drives data and enables data out if $\overline{\text{BMI_WRITE}}$ is logic high. The D_EN signal remains active only while BMI_CLK/CS is logic low and $\overline{\text{BMI_WRITE}}$ is logic high.

Each rising edge of BMI_CLK/CS will determine if data should be latched to RxFIFO from the data bus.

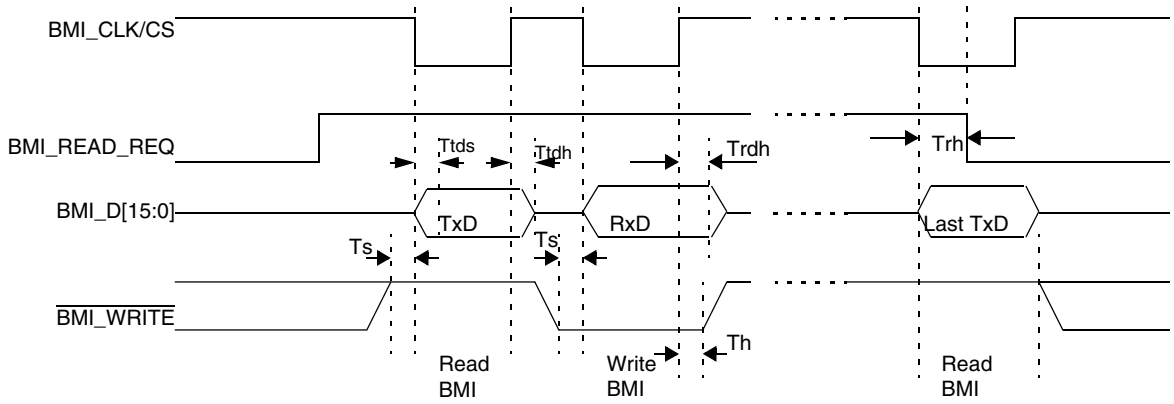



**Figure 10. Memory Interface Slave Mode, External Bus Master Read/Write to BMI Timing (MMD_MODE_SEL=0, MASTER_MODE_SEL=0)**

**Table 17. External Bus Master Read/Write to BMI Timing Table**

| Item | Symbol | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| $\overline{\text{Write}}$ setup time | Ts | 11 | – | – | ns |
| $\overline{\text{Write}}$ hold time | Th | 0 | – | – | ns |
| Receive data hold time | Trdh | 3 | – | – | ns |
| Transfer data setup time | Ttds | 6 | – | 14 | ns |
| Transfer data hold time | Ttdh | 6 | – | 14 | ns |
| Read_req hold time | Trh | 6 | – | 24 | ns |

**Note:** All the timings are assumed that the hclk is running at 133 MHz.

## 3.8.3 Connecting BMI to External Bus Slave Devices

In this mode the $\overline{\text{BMI_WRITE}}$, $\overline{\text{BMI_READ}}$ and BMI_CLK/CS are output signals driving by the BMI module. The output signal BMI_READ_REQ is still driving active-in on a write cycle, but it can be ignored in this case. Instead, it is used to trigger internal logic to generate the read or write signals. Data write cycles are continuously generated when TxFIFO is not emptied.

To issue a read cycle, the user can write a value of 1 to the READ bit of control register. This bit is cleared automatically when the read operation is completed. A read cycle reads COUNT+1 data from the external bus slave. The user can write a 1 to the READ bit while there is still data in the TxFIFO, but the read cycle will not start until all data in the TxFIFO is emptied. If the read cycle begins, the write operation also cannot begin until this read cycle complete.

In this master mode operation, Int_Clk is derived from HCLK through an integer divider DIV of BMI control register and it is used to control the read/write cycle timing by generate $\overline{\text{WRITE}}$ and CLK/CS signals.

### 3.8.3.1 Memory Interface Master Mode Without $\overline{\text{WAIT}}$ Signal

The WAIT control bit (BMICTLR1[29]) is used in this mode. When this bit is cleared (default), the $\overline{\text{BMI_WAIT}}$ signal is ignored and the CS cycle is terminated by Wait State (WS) control bits. Figure 11 shows the BMI timing when the WAIT bit is cleared.

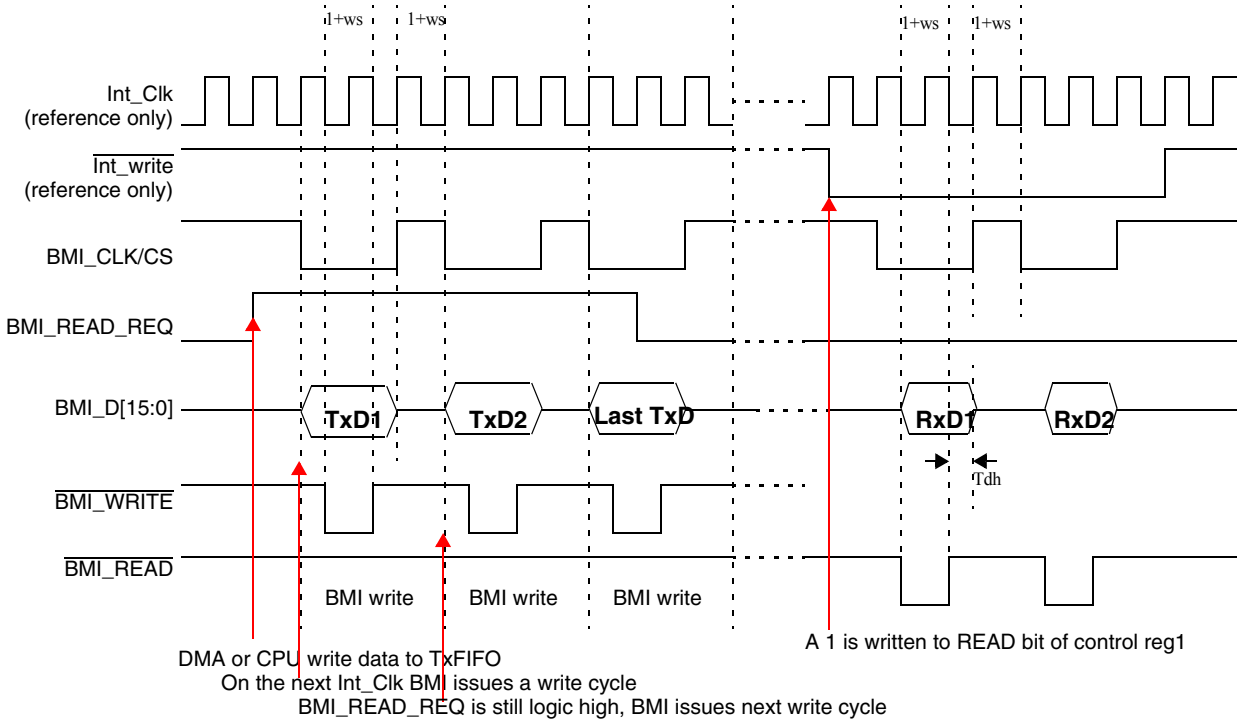



**Figure 11. Memory Interface Master Mode, BMI Read/Write to External Slave Device Timing without $\overline{\text{Wait}}$ Signal (MMD_MODE_SEL=0, MASTER_MODE_SEL=1)**

### 3.8.3.2 Memory Interface Master Mode with $\overline{\text{WAIT}}$ Signal

When the WAIT control bit is set, the $\overline{\text{BMI_WAIT}}$ signal is used and the CS cycle is terminated upon sampling a logic high $\overline{\text{BMI_WAIT}}$ signal. Figure 12 shows the BMI write timing when the WAIT bit is set. When the $\overline{\text{BMI_WRITE}}$ is asserted, the BMI will detect the $\overline{\text{BMI_WAIT}}$ signal on every falling edge of the Int_Clk. When it detected the high level of the $\overline{\text{BMI_WAIT}}$, the $\overline{\text{BMI_WRITE}}$ will be negated after 1+WS Int_Clk period. If the $\overline{\text{BMI_WAIT}}$ is always high or already high before BMI_WRITE is asserted, this timing will same as without $\overline{\text{WAIT}}$ signal. So the $\overline{\text{BMI_WRITE}}$ will be asserted at least for 1+WS Int_Clk period.

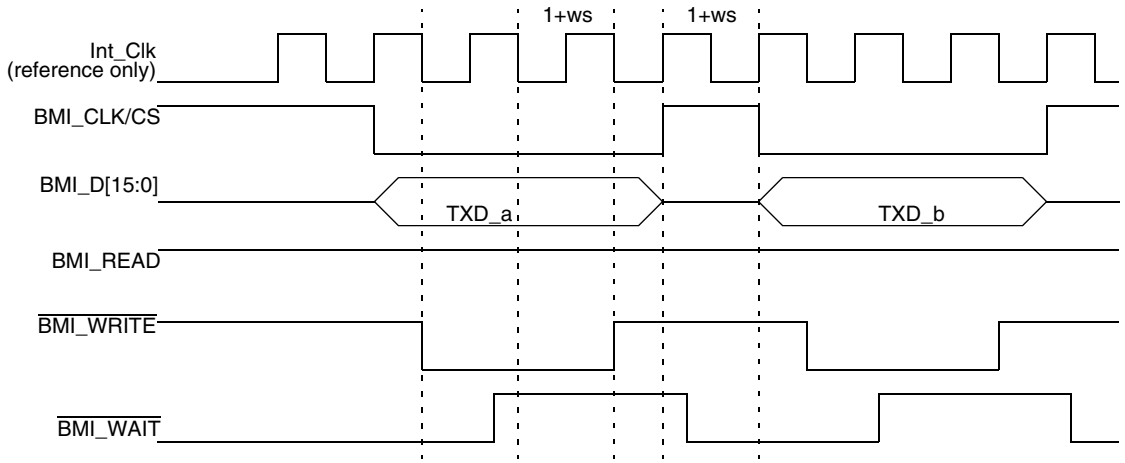



**Figure 12. Memory Interface Master Mode, BMI Write to External Slave Device Timing with Wait Signal (MMD_MODE_SEL=0, MASTER_MODE_SEL=1,WAIT=1)**

Figure 13 shows the BMI read timing when the WAIT bit is set. As write timing, when the BMI_READ is asserted, the BMI will detect the BMI_WAIT signal on every falling edge of the Int_Clk. When it detected the high level of the BMI_WAIT, the BMI_READ will be negated after 1+WS Int_Clk period. If the BMI_WAIT is always high or already high before BMI_READ is asserted, this timing will same as without WAIT signal. So the BMI_READ will be asserted at least for 1+WS Int_Clk period.

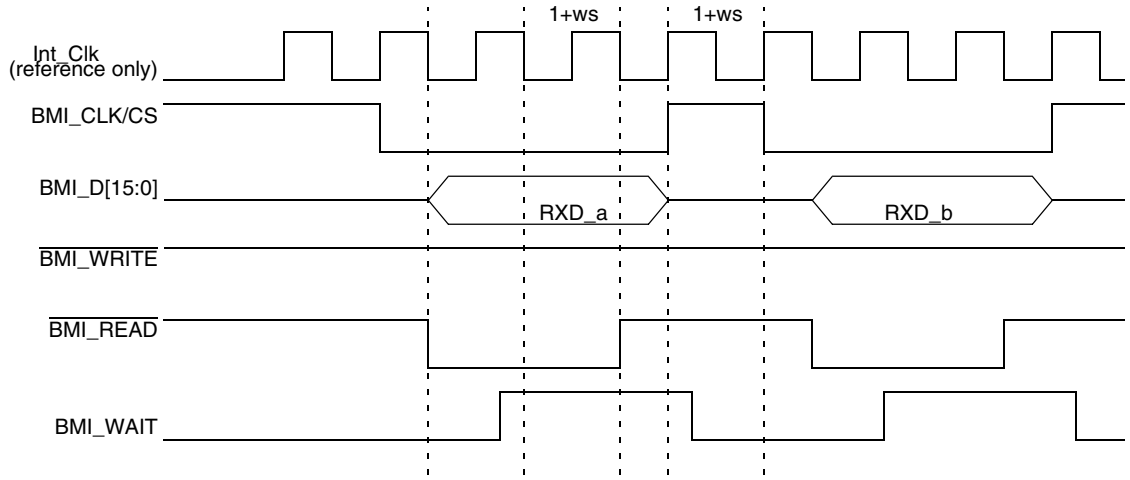



**Figure 13. Memory Interface Master Mode, BMI Read to External Slave Device Timing with Wait Signal (MMD_MODE_SEL=0, MASTER_MODE_SEL=1,WAIT=1)**

## 3.9 CSPI Timing Diagrams

To use the internal transmit (TX) and receive (RX) data FIFOs when the CSPI1 module is configured as a master, two control signals are used for data transfer rate control: the SS signal (output) and the SPI_RDY signal (input). The SPI 1 Sample Period Control Register (PERIODREG1) and the SPI 2 Sample Period Control Register (PERIODREG2) can also be programmed to a fixed data transfer rate for either CSPI1 or CSPI2. When the CSPI1 module is configured as a slave, the user can configure the SPI 1 Control Register (CONTROLREG1) to match the external CSPI master's timing. In this configuration, SS

becomes an input signal, and is used to latch data into or load data out to the internal data shift registers, as well as to increment the data FIFO.

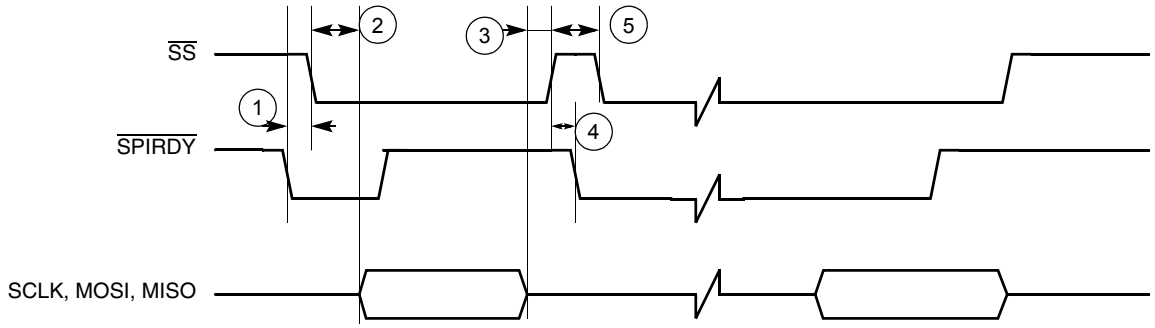



**Figure 14. Master CSPI Timing Diagram Using SPI_RDY Edge Trigger**

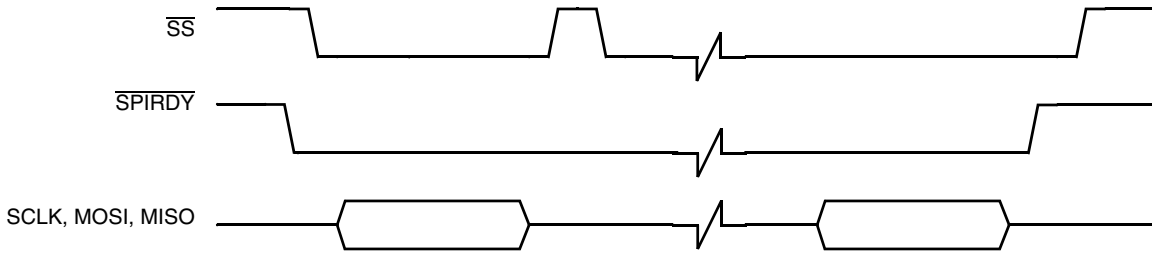



**Figure 15. Master CSPI Timing Diagram Using SPI_RDY Level Trigger**

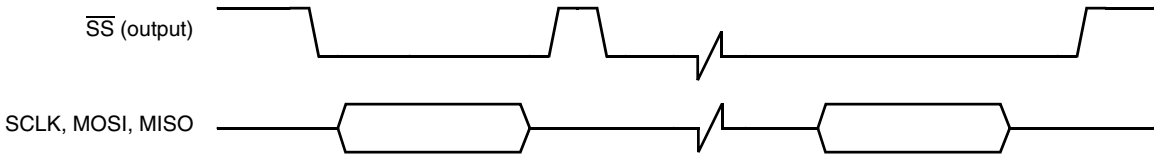



**Figure 16. Master CSPI Timing Diagram Ignore SPI_RDY Level Trigger**

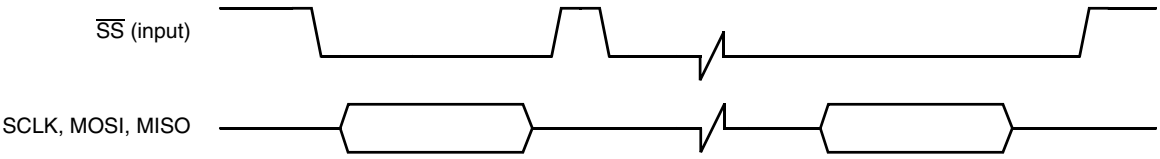



**Figure 17. Slave CSPI Timing Diagram FIFO Advanced by BIT COUNT**

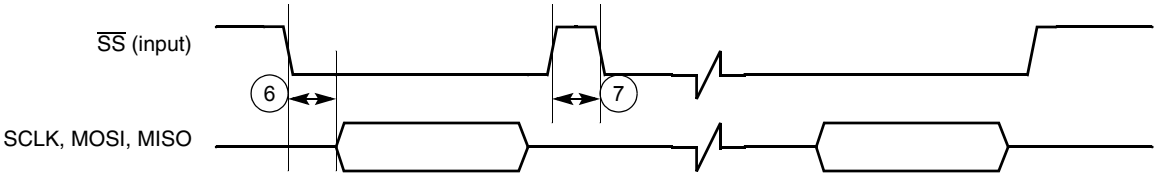



**Figure 18. Slave CSPI Timing Diagram FIFO Advanced by SS Rising Edge**

**Table 18. Timing Parameters for Figure 14 through Figure 18**

| Ref No. | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| 1 | $\overline{\text{SPI_RDY}}$ to $\overline{\text{SS}}$ output low | 2T [1] | – | ns |
| 2 | $\overline{\text{SS}}$ output low to first SCLK edge | 3·Tsclk [2] | – | ns |
| 3 | Last SCLK edge to $\overline{\text{SS}}$ output high | 2·Tsclk | – | ns |
| 4 | $\overline{\text{SS}}$ output high to $\overline{\text{SPI_RDY}}$ low | 0 | – | ns |
| 5 | $\overline{\text{SS}}$ output pulse width | Tsclk + WAIT [3] | – | ns |
| 6 | $\overline{\text{SS}}$ input low to first SCLK edge | T | – | ns |
| 7 | $\overline{\text{SS}}$ input pulse width | T | – | ns |

1. T = CSPI system clock period (PERCLK2).
2. Tsclk = Period of SCLK.
3. WAIT = Number of bit clocks (SCLK) or 32.768 kHz clocks per Sample Period Control Register.

## 3.10 LCD Controller

This section includes timing diagrams for the LCD controller. For detailed timing diagrams of the LCD controller with various display configurations, refer to the LCD controller chapter of the *i.MX21 Reference Manual*.

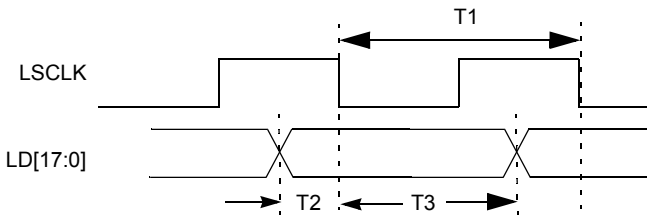



**Figure 19. SCLK to LD Timing Diagram**

**Table 19. LCDC SCLK Timing Parameters**

| Symbol | Parameter | 3.0 ± 0.3V | | Unit |
|---|---|---|---|---|
| | | Minimum | Maximum | |
| T1 | SCLK period | 23 | 2000 | ns |
| T2 | Pixel data setup time | 11 | – | ns |
| T3 | Pixel data up time | 11 | – | ns |
| The pixel clock is equal to LCDC_CLK / (PCD + 1).<br>When it is in CSTN, TFT or monochrome mode with bus width = 1, SCLK is equal to the pixel clock.<br>When it is in monochrome with other bus width settings, SCLK is equal to the pixel clock divided by bus width.<br>The polarity of SCLK and LD can also be programmed.<br>Maximum frequency of SCLK is HCLK / 3 for TFT and CSTN, otherwise LD output will be incorrect. | | | | |

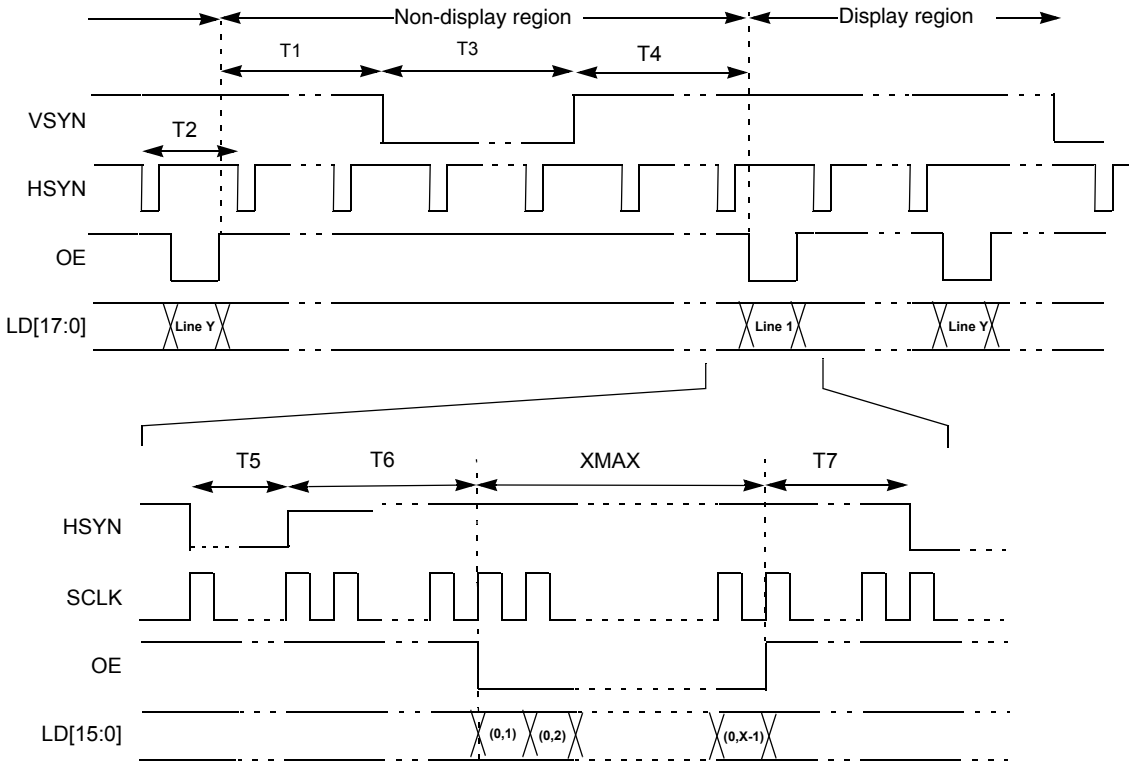



**Figure 20. 4/8/12/16/18 Bit/Pixel TFT Color Mode Panel Timing**

**Table 20. 4/8/12/16/18 Bit/Pixel TFT Color Mode Panel Timing**

| Symbol | Description | Minimum | Value | Unit |
|---|---|---|---|---|
| T1 | End of OE to beginning of VSYN | T5+T6+T7-1 | (VWAIT1·T2)+T5+T6+T7-1 | Ts |
| T2 | HSYN period | – | XMAX+T5+T6+T7 | Ts |
| T3 | VSYN pulse width | T2 | VWIDTH·T2 | Ts |
| T4 | End of VSYN to beginning of OE | 1 | (VWAIT2·T2)+1 | Ts |
| T5 | HSYN pulse width | 1 | HWIDTH+1 | Ts |
| T6 | End of HSYN to beginning to OE | 3 | HWAIT2+3 | Ts |
| T7 | End of OE to beginning of HSYN | 1 | HWAIT1+1 | Ts |

**Note:**
- Ts is the SCLK period.
- VSYN, HSYN and OE can be programmed as active high or active low. In Figure 20, all 3 signals are active low.
- SCLK can be programmed to be deactivated during the VSYN pulse or the OE deasserted period. In Figure 20, SCLK is always active.
- XMAX is defined in number of pixels in one line.

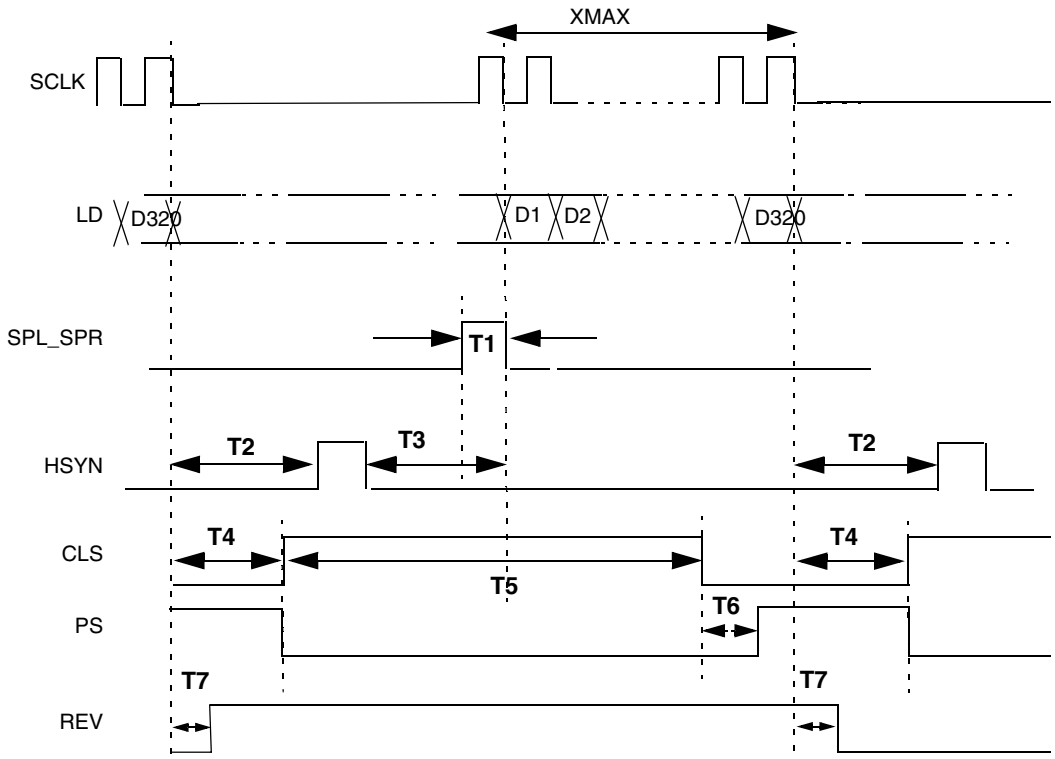



**Figure 21. Sharp TFT Panel Timing**

**Table 21. Sharp TFT Panel Timing**

| Symbol | Description | Minimum | Value | Unit |
|---|---|---|---|---|
| T1 | SPL/SPR pulse width | – | 1 | Ts |
| T2 | End of LD of line to beginning of HSYN | 1 | HWAIT1+1 | Ts |
| T3 | End of HSYN to beginning of LD of line | 4 | HWAIT2 + 4 | Ts |
| T4 | CLS rise delay from end of LD of line | 3 | CLS_RISE_DELAY+1 | Ts |
| T5 | CLS pulse width | 1 | CLS_HI_WIDTH+1 | Ts |
| T6 | PS rise delay from CLS negation | 0 | PS_RISE_DELAY | Ts |
| T7 | REV toggle delay from last LD of line | 1 | REV_TOGGLE_DELAY+1 | Ts |

**Note:**
- Falling of SPL/SPR aligns with first LD of line.
- Falling of PS aligns with rising edge of CLS.
- REV toggles in every HSYN period.

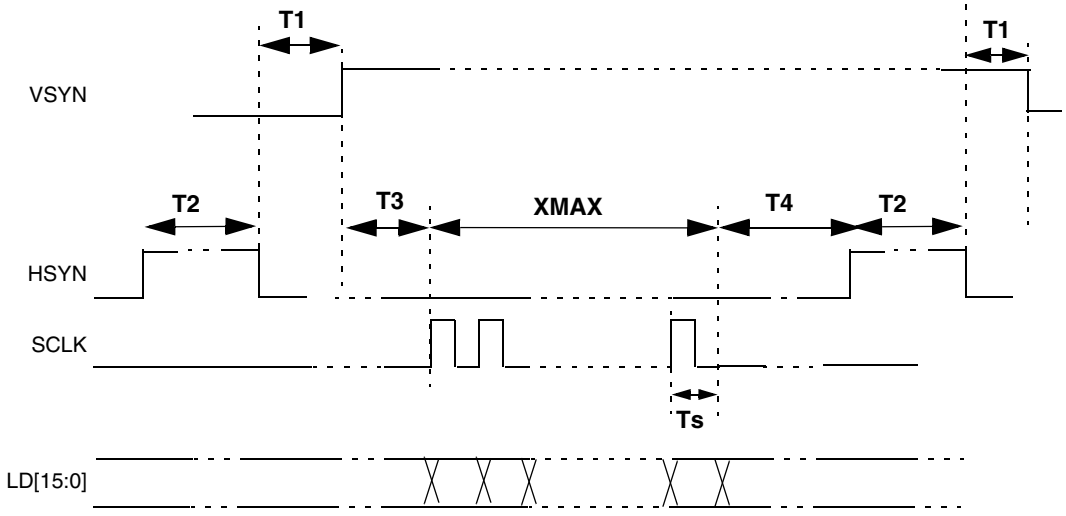



**Figure 22. Non-TFT Mode Panel Timing**

**Table 22. Non-TFT Mode Panel Timing**

| Symbol | Description | Minimum | Value | Unit |
|---|---|---|---|---|
| T1 | HSYN to VSYN delay | 2 | HWAIT2+2 | Tpix |
| T2 | HSYN pulse width | 1 | HWIDTH+1 | Tpix |
| T3 | VSYN to SCLK | – | $0 \leq T3 \leq Ts$ | – |
| T4 | SCLK to HSYN | 1 | HWAIT1+1 | Tpix |

**Note:**
- Ts is the SCLK period while Tpix is the pixel clock period.
- VSYN, HSYN and SCLK can be programmed as active high or active low. In Figure 67, all these 3 signals are active high.
- When it is in CSTN mode or monochrome mode with bus width = 1, T3 = Tpix = Ts.
- When it is in monochrome mode with bus width = 2, 4, and 8, T3 = 1, 2 and 4 Tpix respectively.

## 3.11 Smart LCD Controller

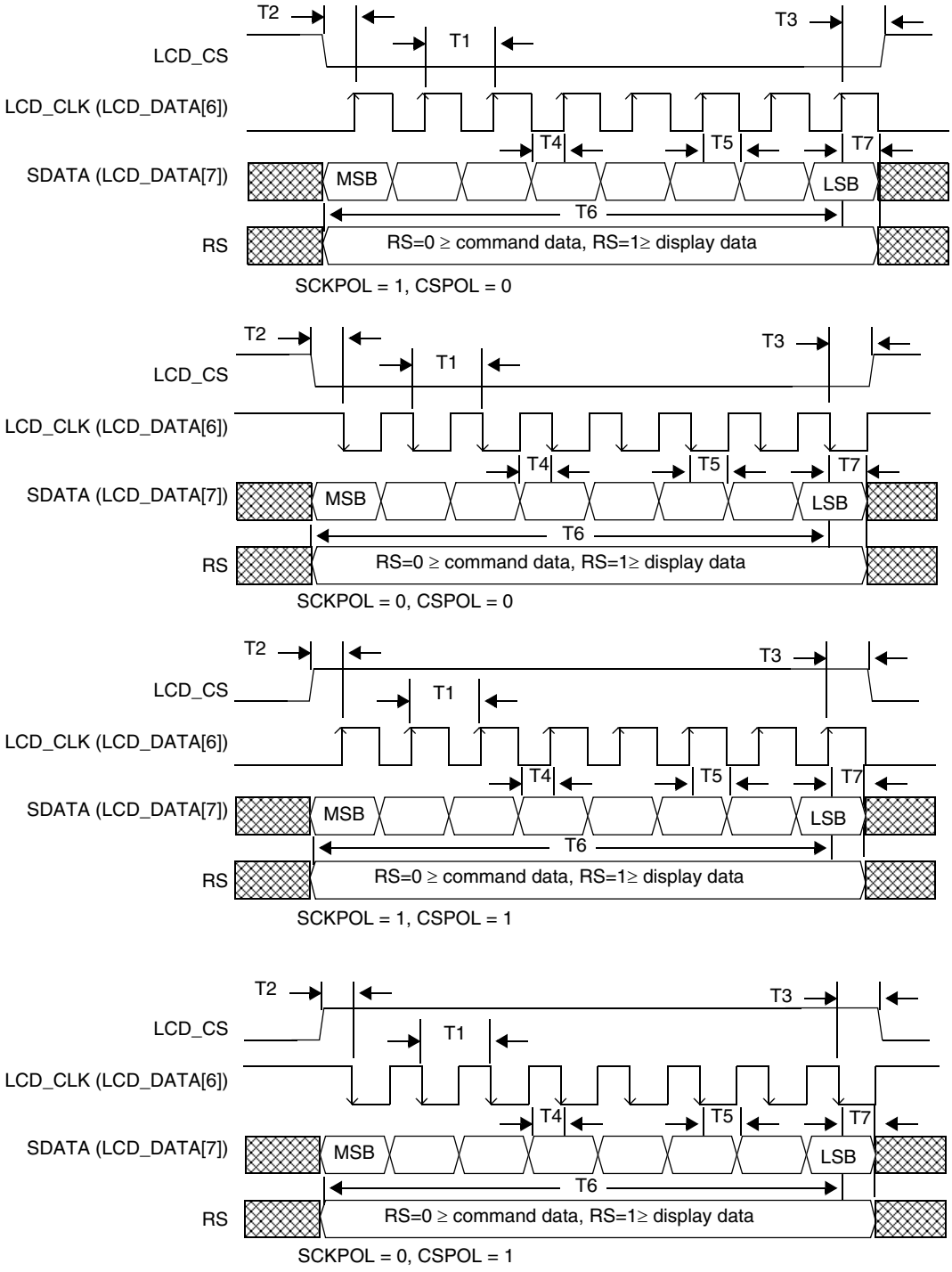
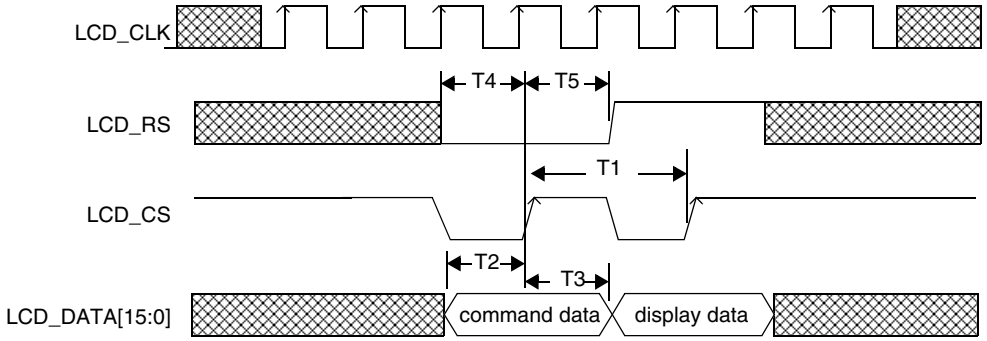


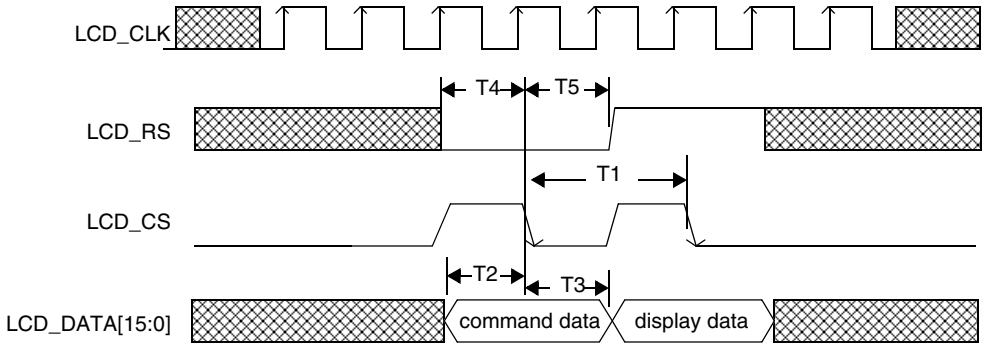

**Figure 23. SLCDC Serial Transfer Timing**

**Table 23. SLCDC Serial Transfer Timing**

| Symbol | Description | Minimum | Maximum | Unit |
|---|---|---|---|---|
| T1 | Pixel clock period | 42 | 962 | ns |
| T2 | Chip select setup time | 5 | – | ns |
| T3 | Chip select hold time | 5 | – | ns |
| T4 | Data setup time | 5 | – | ns |
| T4 | Data hold time | 5 | – | ns |
| T6 | Register select setup time | 5 | – | ns |
| T7 | Register select hold time | 5 | – | ns |




**CSPOL = 0**




**CSPOL = 1**

**Figure 24. SLCDC Parallel Transfers Timing**

**Table 24. SLCDC Parallel Transfers Timing**

| Symbol | Description | Minimum | Maximum | Unit |
|---|---|---|---|---|
| T1 | Pixel clock period | 23 | 962 | ns |
| T2 | Data setup time | 5 | – | ns |
| T3 | Data hold time | 5 | – | ns |
| T4 | Register select setup time | 5 | – | ns |
| T5 | Register select hold time | 5 | – | ns |

## 3.12 Multimedia Card/Secure Digital Host Controller

The DMA interface block controls all data routing between the external data bus (DMA access), internal MMC/SD module data bus, and internal system FIFO access through a dedicated state machine that monitors the status of FIFO content (empty or full), FIFO address, and byte/block counters for the MMC/SD module (inner system) and the application (user programming).

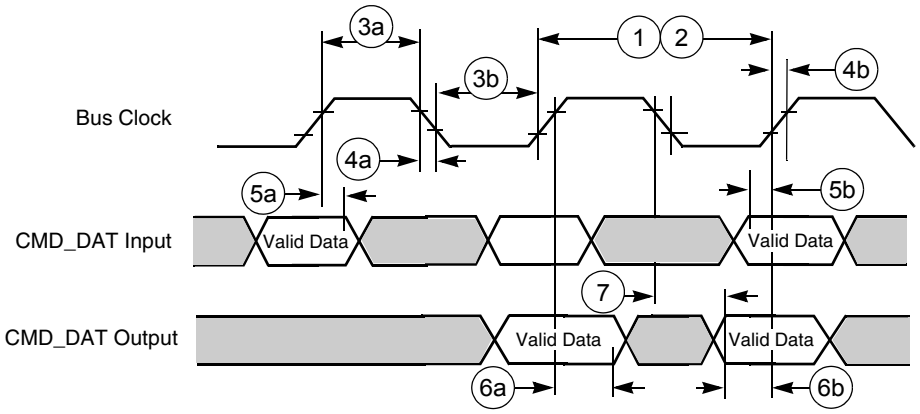



**Figure 25. Chip-Select Read Cycle Timing Diagram**

**Table 25. SDHC Bus Timing Parameters**

| Ref No. | Parameter | 1.8 V ± 0.1 V | | 3.0 V ± 0.3 V | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| 1 | CLK frequency at Data transfer Mode (PP)[1]—10/30 cards | 0 | 25/5 | 0 | 25/5 | MHz |
| 2 | CLK frequency at Identification Mode[2] | 0 | 400 | 0 | 400 | kHz |
| 3a | Clock high time[1]—10/30 cards | 6/33 | – | 10/50 | – | ns |
| 3b | Clock low time[1]—10/30 cards | 15/75 | – | 10/50 | – | ns |
| 4a | Clock fall time[1]—10/30 cards | – | 10/50 (5.00)[3] | – | 10/50 | ns |
| 4b | Clock rise time[1]—10/30 cards | – | 14/67 (6.67)[3] | – | 10/50 | ns |
| 5a | Input hold time[3]—10/30 cards | 5.7/5.7 | – | 5/5 | – | ns |
| 5b | Input setup time[3]—10/30 cards | 5.7/5.7 | – | 5/5 | – | ns |
| 6a | Output hold time[3]—10/30 cards | 5.7/5.7 | – | 5/5 | – | ns |
| 6b | Output setup time[3]—10/30 cards | 5.7/5.7 | – | 5/5 | – | ns |
| 7 | Output delay time[3] | 0 | 16 | 0 | 14 | ns |

1. $C_L \leq 100$ pF / 250 pF (10/30 cards)
2. $C_L \leq 250$ pF (21 cards)
3. $C_L \leq 25$ pF (1 card)

### 3.12.1 Command Response Timing on MMC/SD Bus

The card identification and card operation conditions timing are processed in open-drain mode. The card response to the host command starts after exactly $N_{ID}$ clock cycles. For the card address assignment, SET_RCA is also processed in the open-drain mode. The minimum delay between the host command and card response is NCR clock cycles as illustrated in Figure 26. The symbols for Figure 26 through Figure 30 are defined in Table 26.

**Table 26. State Signal Parameters for Figure 26 through Figure 30**

| Card Active | | Host Active | |
|---|---|---|---|
| **Symbol** | **Definition** | **Symbol** | **Definition** |
| Z | High impedance state | S | Start bit (0) |
| D | Data bits | T | Transmitter bit (Host = 1, Card = 0) |
| * | Repetition | P | One-cycle pull-up (1) |
| CRC | Cyclic redundancy check bits (7 bits) | E | End bit (1) |

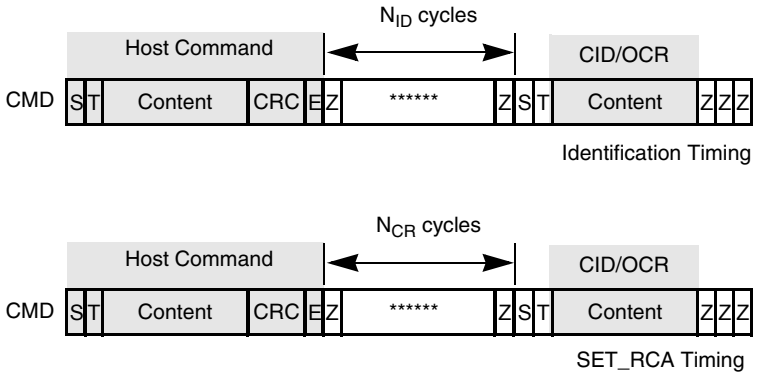



**Figure 26. Timing Diagrams at Identification Mode**

After a card receives its RCA, it switches to data transfer mode. As shown on the first diagram in Figure 27, SD_CMD lines in this mode are driven with push-pull drivers. The command is followed by a period of two Z bits (allowing time for direction switching on the bus) and then by P bits pushed up by the responding card. The other two diagrams show the separating periods $N_{RC}$ and $N_{CC}$.

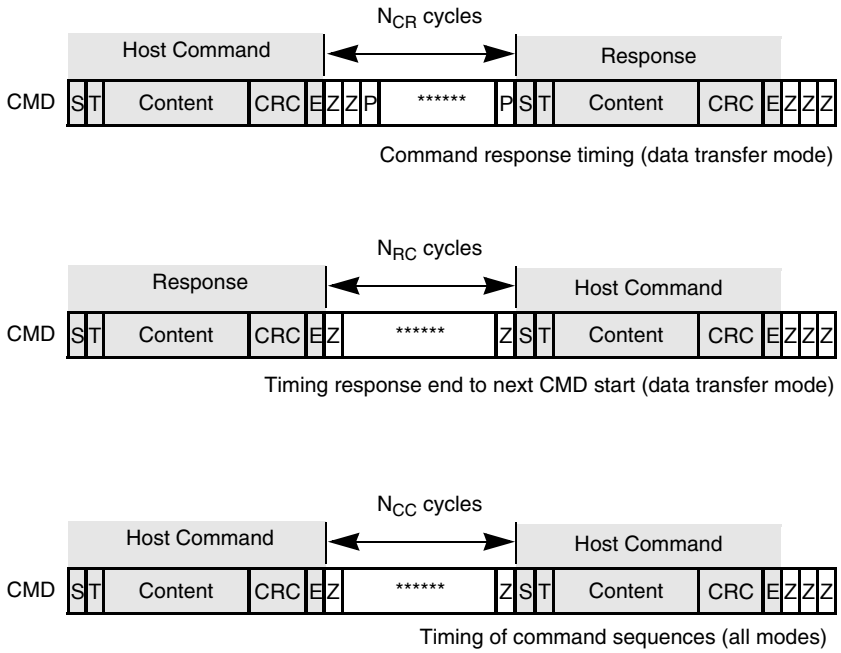



**Figure 27. Timing Diagrams at Data Transfer Mode**

Figure 28 shows basic read operation timing. In a read operation, the sequence starts with a single block read command (which specifies the start address in the argument field). The response is sent on the SD_CMD lines as usual. Data transmission from the card starts after the access time delay $N_{AC}$, beginning from the last bit of the read command. If the system is in multiple block read mode, the card sends a continuous flow of data blocks with distance $N_{AC}$ until the card sees a stop transmission command. The data stops two clock cycles after the end bit of the stop command.

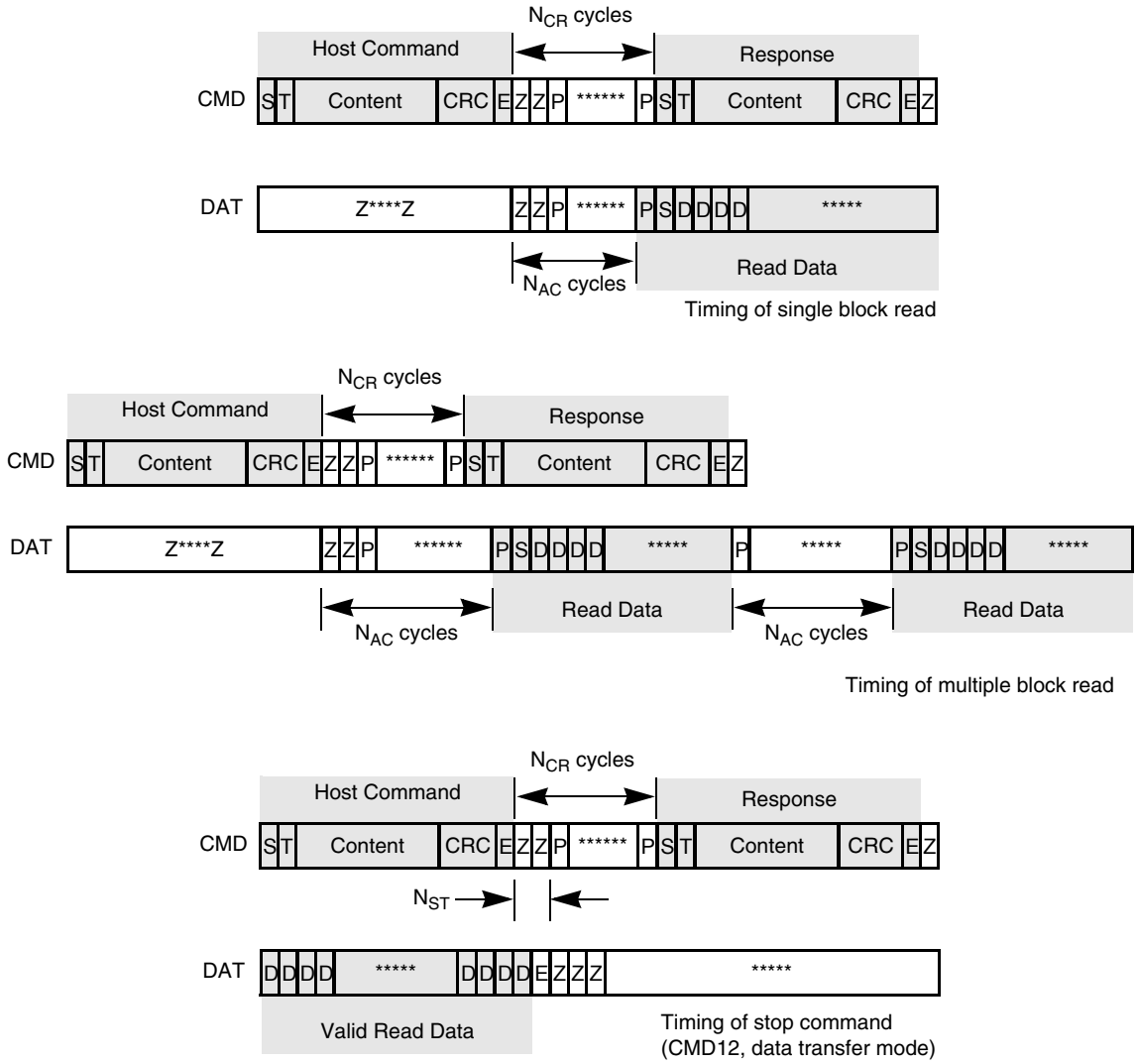



**Figure 28. Timing Diagrams at Data Read**

Figure 29 shows the basic write operation timing. As with the read operation, after the card response, the data transfer starts after $N_{WR}$ cycles. The data is suffixed with CRC check bits to allow the card to check for transmission errors. The card sends back the CRC check result as a CC status token on the data line. If there was a transmission error, the card sends a negative CRC status (101); otherwise, a positive CRC status (010) is returned. The card expects a continuous flow of data blocks if it is configured to multiple block mode, with the flow terminated by a stop transmission command.

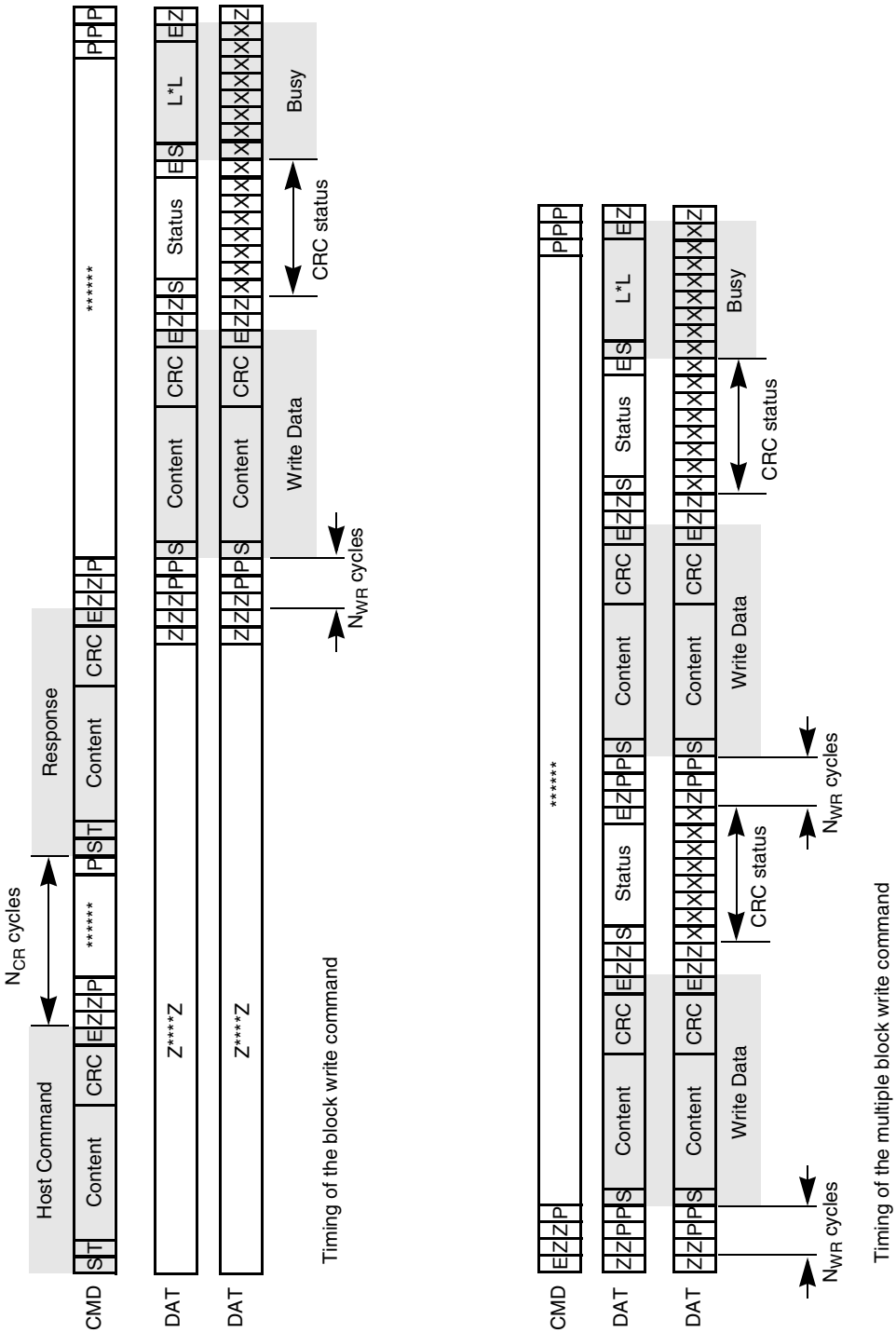



**Figure 29. Timing Diagrams at Data Write**

The stop transmission command may occur when the card is in different states. Figure 30 shows the different scenarios on the bus.

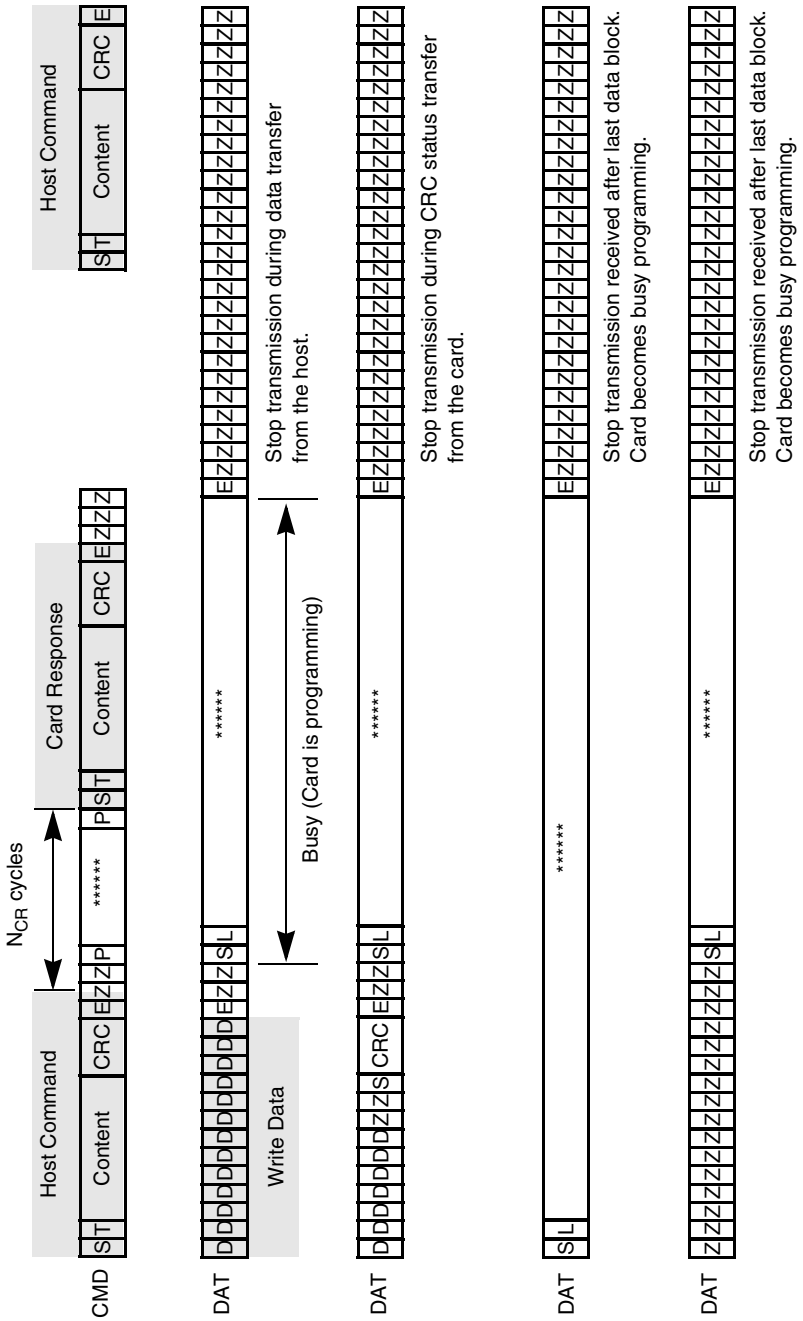



**Figure 30. Stop Transmission During Different Scenarios**

**Table 27. Timing Values for Figure 26 through Figure 30**

| Parameter | Symbol | Minimum | Maximum | Unit |
|---|---|---|---|---|
| MMC/SD bus clock, CLK (All values are referred to minimum (VIH) and maximum (VIL) | | | | |
| Command response cycle | NCR | 2 | 64 | Clock cycles |
| Identification response cycle | NID | 5 | 5 | Clock cycles |
| Access time delay cycle | NAC | 2 | TAAC + NSAC | Clock cycles |

**Table 27. Timing Values for Figure 26 through Figure 30 (Continued)**

| Parameter | Symbol | Minimum | Maximum | Unit |
|---|---|---|---|---|
| Command read cycle | NRC | 8 | – | Clock cycles |
| Command-command cycle | NCC | 8 | – | Clock cycles |
| Command write cycle | NWR | 2 | – | Clock cycles |
| Stop transmission cycle | NST | 2 | 2 | Clock cycles |
| TAAC: Data read access time -1 defined in CSD register bit[119:112]<br>NSAC: Data read access time -2 in CLK cycles (NSAC·100) defined in CSD register bit[111:104] | | | | |

## 3.12.2 SDIO-IRQ and ReadWait Service Handling

In SDIO, there is a 1-bit or 4-bit interrupt response from the SDIO peripheral card. In 1-bit mode, the interrupt response is simply that the SD_DAT[1] line is held low. The SD_DAT[1] line is not used as data in this mode. The memory controller generates an interrupt according to this low and the system interrupt continues until the source is removed (SD_DAT[1] returns to its high level).

In 4-bit mode, the interrupt is less simple. The interrupt triggers at a particular period called the *Interrupt Period* during the data access, and the controller must sample SD_DAT[1] during this short period to determine the IRQ status of the attached card. The interrupt period only happens at the boundary of each block (512 bytes).

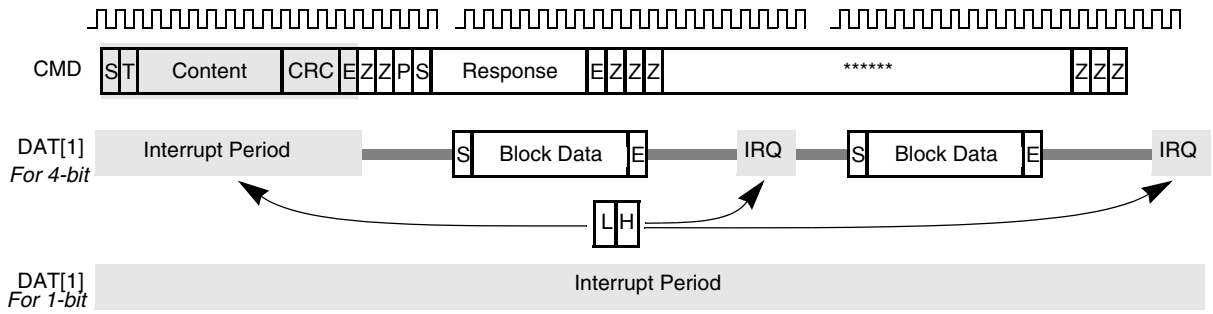



**Figure 31. SDIO IRQ Timing Diagram**

ReadWait is another feature in SDIO that allows the user to submit commands during the data transfer. In this mode, the block temporarily pauses the data transfer operation counter and related status, yet keeps the clock running, and allows the user to submit commands as normal. After all commands are submitted, the user can switch back to the data transfer operation and all counter and status values are resumed as access continues.

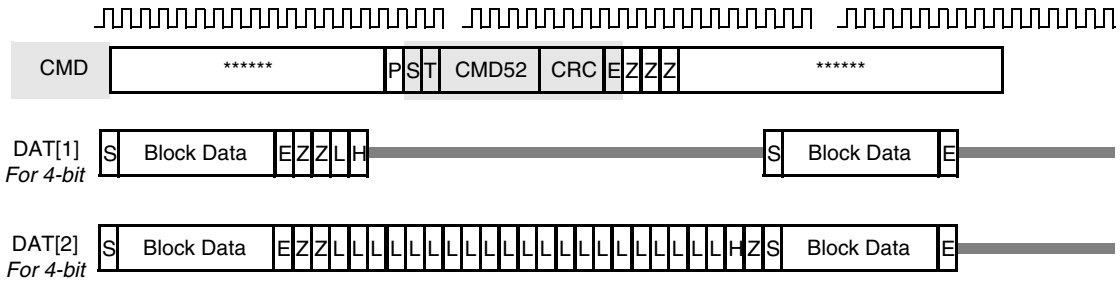



**Figure 32. SDIO ReadWait Timing Diagram**

## 3.13 External Memory Interface (EMI) Electricals

### 3.13.1 NAND-Flash Controller (NFC) Interface

Figure 33, Figure 34, Figure 35, and Figure 36 depict the relative timing requirements among different signals of the NFC at module level, and Table 28 lists the timing parameters. The NAND Flash Controller (NFC) timing parameters are based on the internal NFC clock generated by the Clock Controller module, where time T is the period of the NFC clock in ns. Per the i.MX21 Reference Manual, specifically the *Phase-Locked (PLL), Clock, and Reset Controller* chapter, the NFC clock is derived from the same clock which drives the CPU clock (FCLK) that is fed through the NFCDIV block to generate the NFC clock. The relationship between the NFC clock and the external timing parameters of the NFC is provided in Table 28.

Table 28 also provides two examples of external timing parameters with NFC clock frequencies of 22.17 MHz and 33.25 MHz. For example, assuming a 266 MHz FCLK (CPU clock), NFCDIV should be set to divide-by-12 to generate a 22.17 MHz NFC clock and divide-by-8 to generate a 33.25 MHz NFC clock. The user should compare the parameters of the selected NAND Flash memory with the NFC external timing parameters to determine the proper NFC clock. *The maximum NFC clock allowed is 66 MHz*. It should also be noted that the default NFC clock on power up is 16.63 MHz.

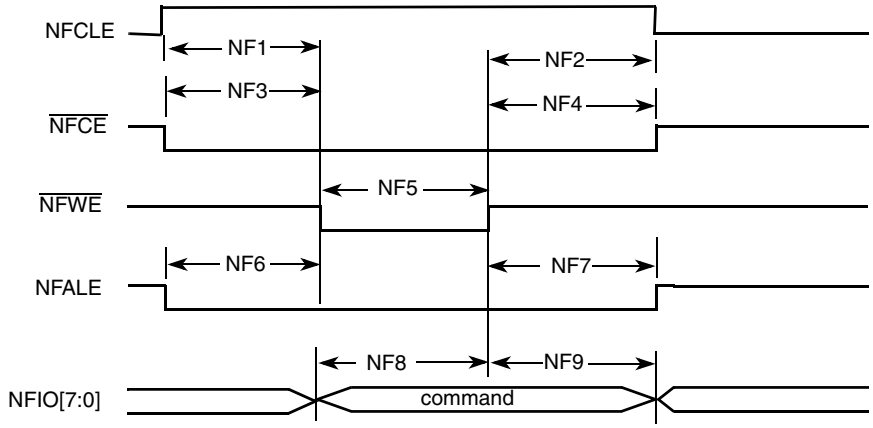



**Figure 33. Command Latch Cycle Timing Diagram**

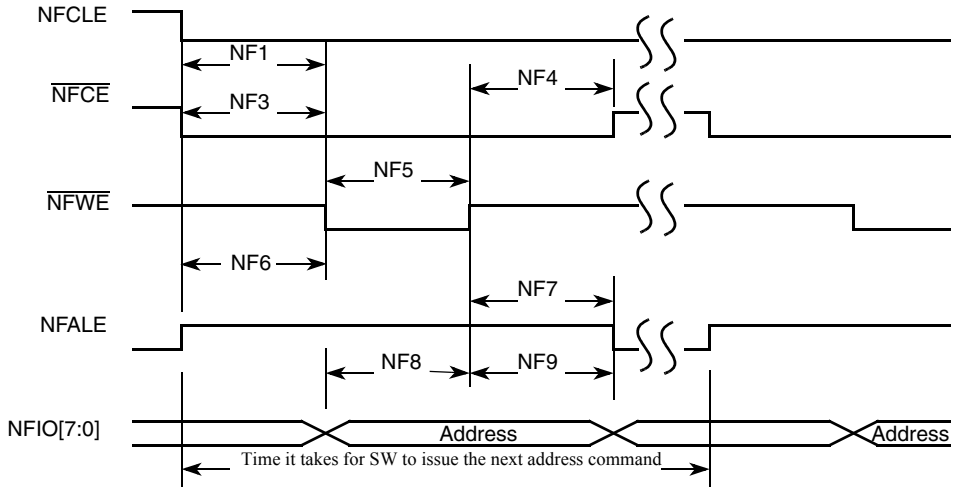



**Figure 34. Address Latch Cycle Timing Diagram**

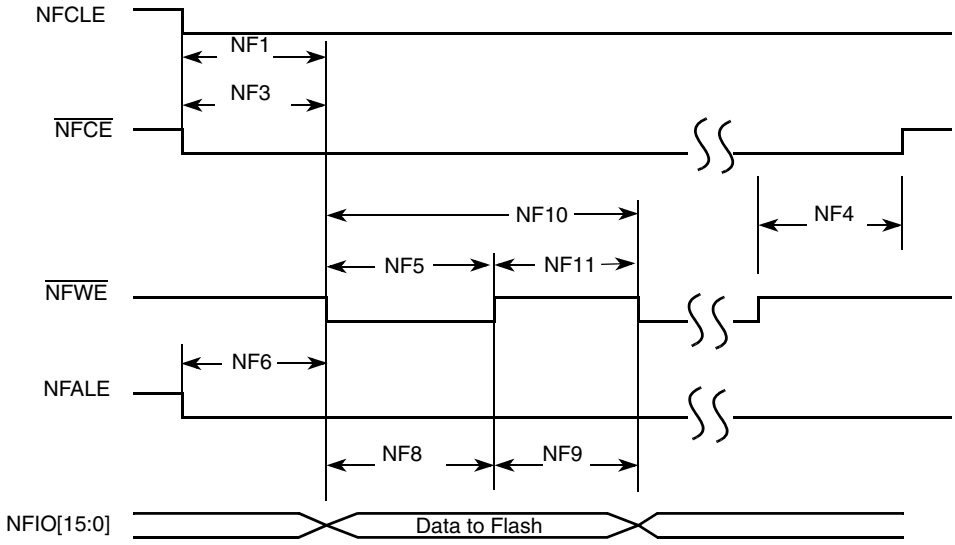



**Figure 35. Write Data Latch Timing Diagram**

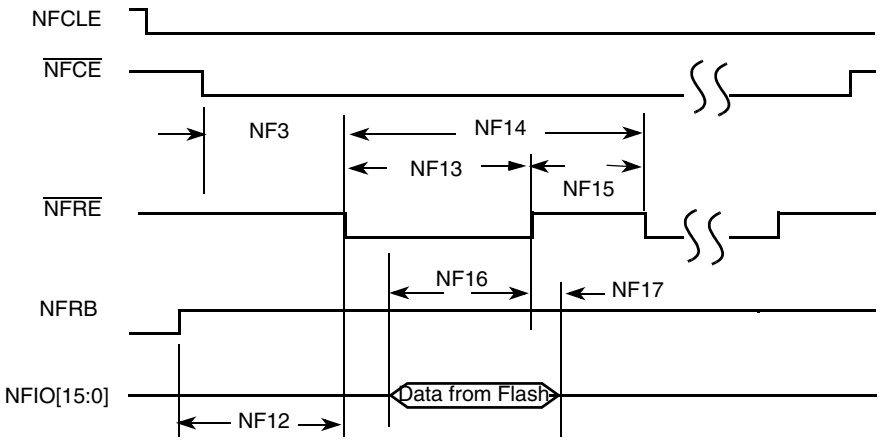



**Figure 36. Read Data Latch Timing Diagram**

**Table 28. NFC Target Timing Parameters[1,2]**

| ID | Parameter | Symbol | Relationship to NFC Clock Period (T) | | NFC Clock 22.17 MHz T = 45 ns | | NFC Clock 33.25 MHz T = 30 ns | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| NF1 | NFCLE Setup Time | tCLS | T | – | 45 | – | 30 | – | ns |
| NF2 | NFCLE Hold Time | tCLH | T | – | 45 | – | 30 | – | ns |
| NF3 | $\overline{\text{NFCE}}$ Setup Time | tCS | T | – | 45 | – | 30 | – | ns |
| NF4 | $\overline{\text{NFCE}}$ Hold Time | tCH | T | – | 45 | – | 30 | – | ns |
| NF5 | $\overline{\text{NF_WP}}$ Pulse Width | tWP | T | – | 45 | – | 30 | – | ns |
| NF6 | NFALE Setup Time | tALS | T | – | 45 | – | 30 | – | ns |
| NF7 | NFALE Hold Time | tALH | T | – | 45 | – | 30 | – | ns |
| NF8 | Data Setup Time | tDS | T | – | 45 | – | 30 | – | ns |
| NF9 | Data Hold Time | tDH | T | – | 45 | – | 30 | – | ns |
| NF10 | Write Cycle Time | tWC | 2T | – | 90 | – | 60 | – | ns |
| NF11 | $\overline{\text{NFWE}}$ Hold Time | tWH | T | – | 45 | – | 30 | – | ns |
| NF12 | Ready to $\overline{\text{NFRE}}$ Low | tRR | 4T | – | 180 | – | 120 | – | ns |
| NF13 | $\overline{\text{NFRE}}$ Pulse Width | tRP | 1.5T | – | 67.5 | – | 45 | – | ns |
| NF14 | READ Cycle Time | tRC | 2T | – | 90 | – | 60 | – | ns |
| NF15 | $\overline{\text{NFRE}}$ High Hold Time | tREH | 0.5T | – | 22.5 | – | 15 | – | ns |
| NF16 | Data Setup on READ | tDSR | 15 | – | 15 | – | 15 | – | ns |
| NF17 | Data Hold on READ | tDHR | 0 | – | 0 | – | 0 | – | ns |

1. High is defined as 80% of signal value and low is defined as 20% of signal value. All timings are listed according to this NFC clock frequency (multiples of NFC clock period) except NF16, which is not NFC clock related.
2. The read data is generated by the NAND Flash device and sampled with the internal NFC clock.

## 3.14 Pulse-Width Modulator

The PWM can be programmed to select one of two clock signals as its source frequency. The selected clock signal is passed through a divider and a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

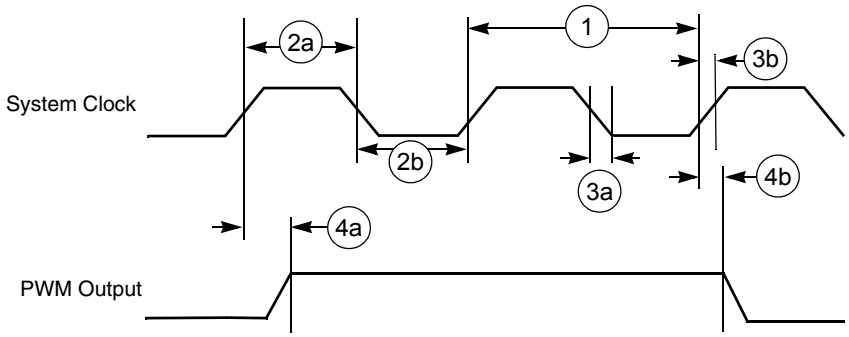



**Figure 37. PWM Output Timing Diagram**

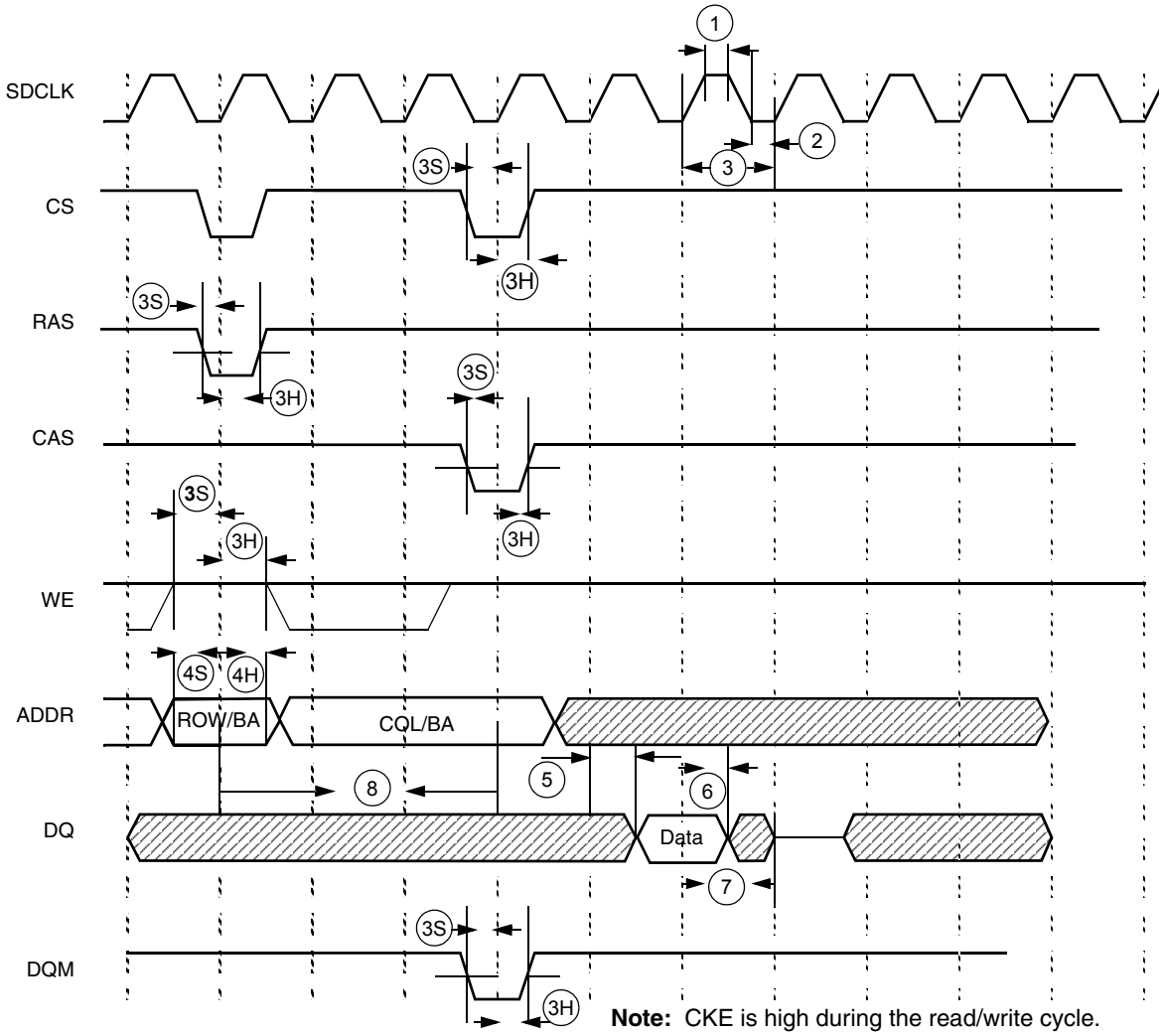
**Table 29. PWM Output Timing Parameters**

| Ref No. | Parameter | 1.8 V ± 0.1 V | | 3.0 V ± 0.3 V | | Unit |
|---|---|---|---|---|---|---|
| | | Minimum | Maximum | Minimum | Maximum | |
| 1 | System CLK frequency[1] | 0 | 45 | 0 | 45 | MHz |
| 2a | Clock high time[1] | 12.29 | – | 12.29 | – | ns |
| 2b | Clock low time[1] | 9.91 | – | 9.91 | – | ns |
| 3a | Clock fall time[1] | – | 0.5 | – | 0.5 | ns |
| 3b | Clock rise time[1] | – | 0.5 | – | 0.5 | ns |
| 4a | Output delay time[1] | 9.37 | – | 3.61 | – | ns |
| 4b | Output setup time[1] | 8.71 | – | 3.03 | – | ns |

1. $C_L$ of PWMO = TBD

## 3.15 SDRAM Memory Controller

The following figures (Figure 38 through Figure 41) and their associated tables specify the timings related to the SDRAMC module in the i.MX21.




**Note:** CKE is high during the read/write cycle.

**Figure 38. SDRAM Read Cycle Timing Diagram**

**Table 30. SDRAM Read Cycle Timing Parameter**

| Ref No. | Parameter | 1.8 V ± 0.1 V | | 3.0 V ± 0.3 V | | Unit |
|---|---|---|---|---|---|---|
| | | Minimum | Maximum | Minimum | Maximum | |
| 1 | SDRAM clock high-level width | 3.00 | – | 3 | – | ns |
| 2 | SDRAM clock low-level width | 3.00 | – | 3 | – | ns |
| 3 | SDRAM clock cycle time | 7.5 | – | 7.5 | – | ns |
| 3S | CS, RAS, CAS, WE, DQM setup time | 4.78 | – | 3 | – | ns |
| 3H | CS, RAS, CAS, WE, DQM hold time | 3.03 | – | 2 | – | ns |

**Table 30. SDRAM Read Cycle Timing Parameter (Continued)**

| Ref No. | Parameter | 1.8 V ± 0.1 V | | 3.0 V ± 0.3 V | | Unit |
|---|---|---|---|---|---|---|
| | | Minimum | Maximum | Minimum | Maximum | |
| 4S | Address setup time | 3.67 | – | 2 | – | ns |
| 4H | Address hold time | 2.95 | – | 2 | – | ns |
| 5 | SDRAM access time (CL = 3) | – | 5.4 | – | 5.4 | ns |
| 5 | SDRAM access time (CL = 2) | – | 6.0 | – | 6.0 | ns |
| 5 | SDRAM access time (CL = 1) | – | – | – | – | ns |
| 6 | Data out hold time | 2 | – | 2 | – | ns |
| 7 | Data out high-impedance time (CL = 3) | – | $t_{HZ}$[1] | – | $t_{HZ}$[1] | ns |
| 7 | Data out high-impedance time (CL = 2) | – | $t_{HZ}$[1] | – | $t_{HZ}$[1] | ns |
| 7 | Data out high-impedance time (CL = 1) | – | – | – | – | ns |
| 8 | Active to read/write command period (RC = 1) | $t_{RCD}$[2] | – | $t_{RCD}$[2] | – | ns |

1. $t_{HZ}$ = SDRAM data out high-impedance time, external SDRAM memory device dependent parameter.
2. $t_{RCD}$ = SDRAM clock cycle time. The $t_{RCD}$ setting can be found in the i.MX21 reference manual.

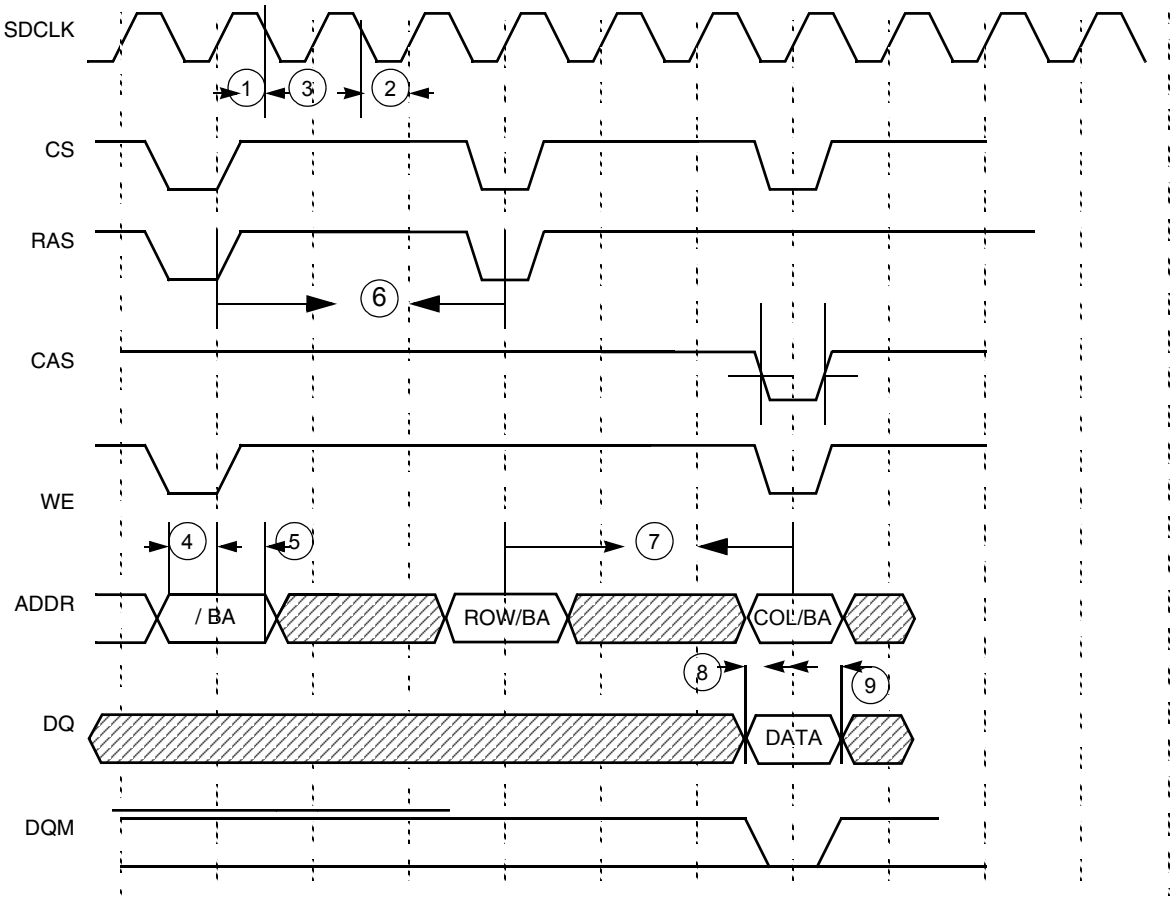



**Figure 39. SDRAM Write Cycle Timing Diagram**

**Table 31. SDRAM Write Cycle Timing Parameter**

| Ref No. | Parameter | 1.8 V ± 0.1 V | | 3.0 V ± 0.3 V | | Unit |
|---|---|---|---|---|---|---|
| | | Minimum | Maximum | Minimum | Maximum | |
| 1 | SDRAM clock high-level width | 3.00 | – | 3 | – | ns |
| 2 | SDRAM clock low-level width | 3.00 | – | 3 | – | ns |
| 3 | SDRAM clock cycle time | 7.5 | – | 7.5 | – | ns |
| 4 | Address setup time | 3.67 | – | 2 | – | ns |
| 5 | Address hold time | 2.95 | – | 2 | – | ns |
| 6 | Precharge cycle period[1] | $t_{RP}$[2] | – | $t_{RP}$[2] | – | ns |
| 7 | Active to read/write command delay | $t_{RCD}$[2] | – | $t_{RCD}$[2] | – | ns |
| 8 | Data setup time | 3.41 | – | 2 | – | ns |
| 9 | Data hold time | 2.45 | – | 2 | – | ns |

1. Precharge cycle timing is included in the write timing diagram.
2. $t_{RP}$ and $t_{RCD}$ = SDRAM clock cycle time. These settings can be found in the i.MX21 reference manual.

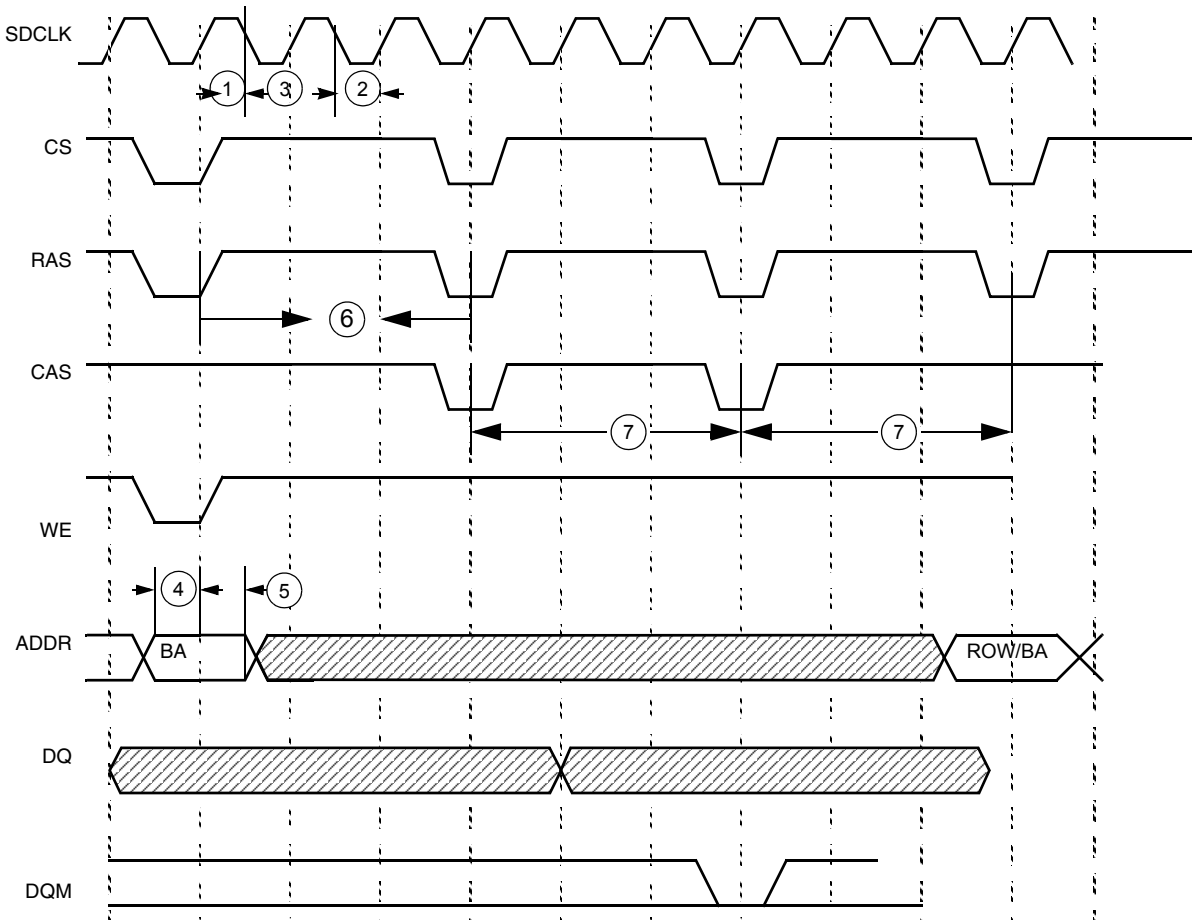



**Figure 40. SDRAM Refresh Timing Diagram**

**Table 32. SDRAM Refresh Timing Parameters**

| Ref No. | Parameter | 1.8 V ± 0.1 V | | 3.0 V ± 0.3 V | | Unit |
|---|---|---|---|---|---|---|
| | | Minimum | Maximum | Minimum | Maximum | |
| 1 | SDRAM clock high-level width | 3.00 | – | 3 | – | ns |
| 2 | SDRAM clock low-level width | 3.00 | – | 3 | – | ns |
| 3 | SDRAM clock cycle time | 7.5 | – | 7.5 | – | ns |
| 4 | Address setup time | 3.67 | – | 2 | – | ns |
| 5 | Address hold time | 2.95 | – | 2 | – | ns |
| 6 | Precharge cycle period | $t_{RP}$[1] | – | $t_{RP}$[1] | – | ns |
| 7 | Auto precharge command period | $t_{RC}$[1] | – | $t_{RC}$[1] | – | ns |

1. $t_{RP}$ and $t_{RC}$ = SDRAM clock cycle time. These settings can be found in the i.MX21 reference manual.

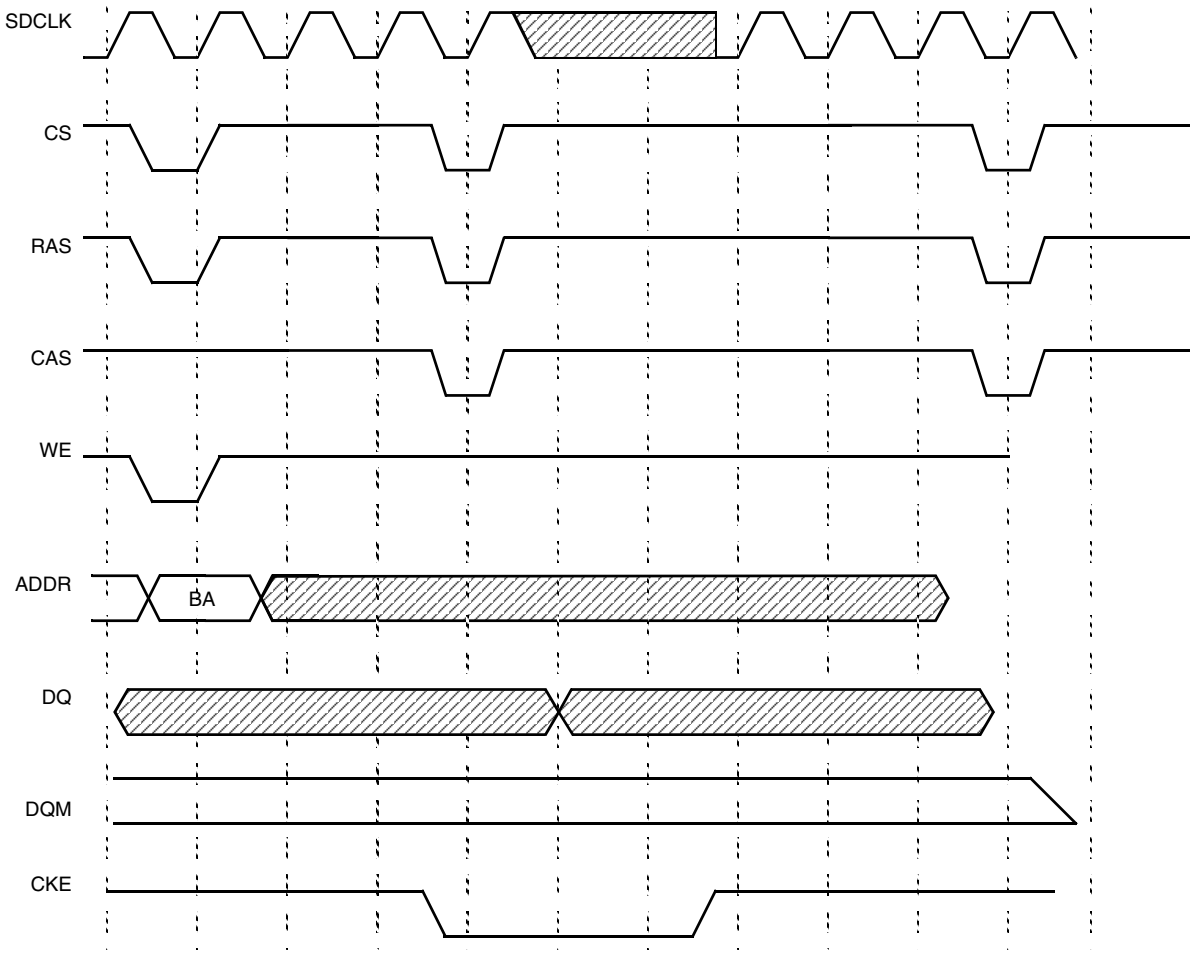


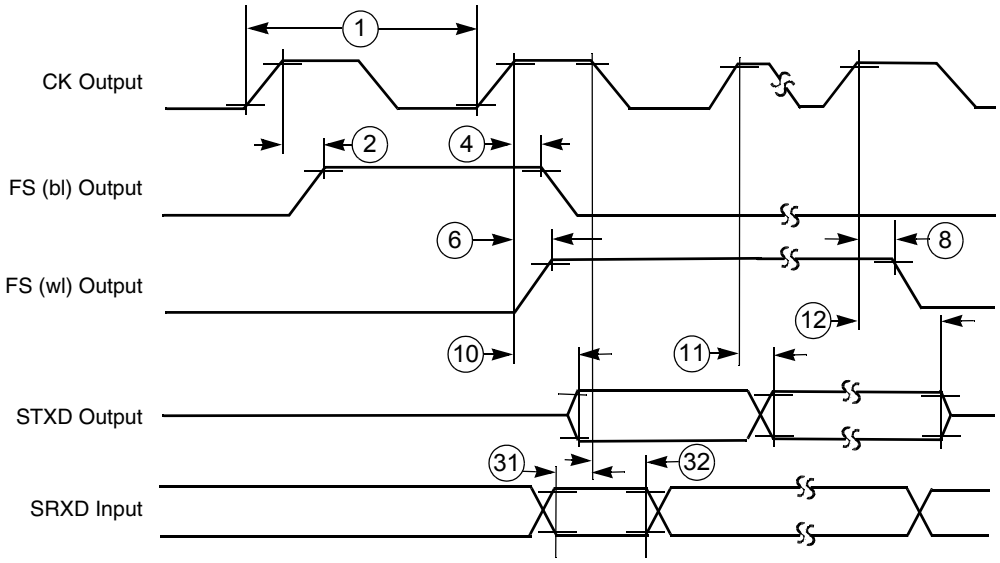

**Figure 41. SDRAM Self-Refresh Cycle Timing Diagram**

## 3.16 Synchronous Serial Interface

The transmit and receive sections of the SSI can be synchronous or asynchronous. In synchronous mode, the transmitter and the receiver use a common clock and frame synchronization signal. In asynchronous mode, the transmitter and receiver each have their own clock and frame synchronization signals. Continuous or gated clock mode can be selected. In continuous mode, the clock runs continuously. In gated clock mode, the clock functions only during transmission. The internal and external clock timing diagrams are shown in Figure 42 through Figure 45.

Normal or network mode can also be selected. In normal mode, the SSI functions with one data word of I/O per frame. In network mode, a frame can contain between 2 and 32 data words. Network mode is typically used in star or ring-time division multiplex networks with other processors or codecs, allowing interface to time division multiplexed networks without additional logic. Use of the gated clock is not allowed in network mode. These distinctions result in the basic operating modes that allow the SSI to communicate with a wide variety of devices.

The SSI can be connected to 4 set of ports, SAP, SSI1, SSI2 and SSI3.




**Note:** SRXD input in synchronous mode only.

**Figure 42. SSI Transmitter Internal Clock Timing Diagram**

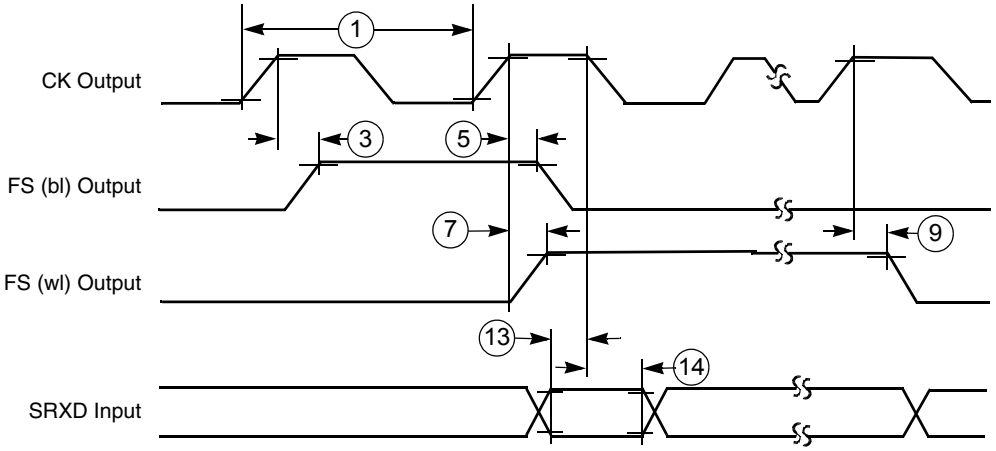
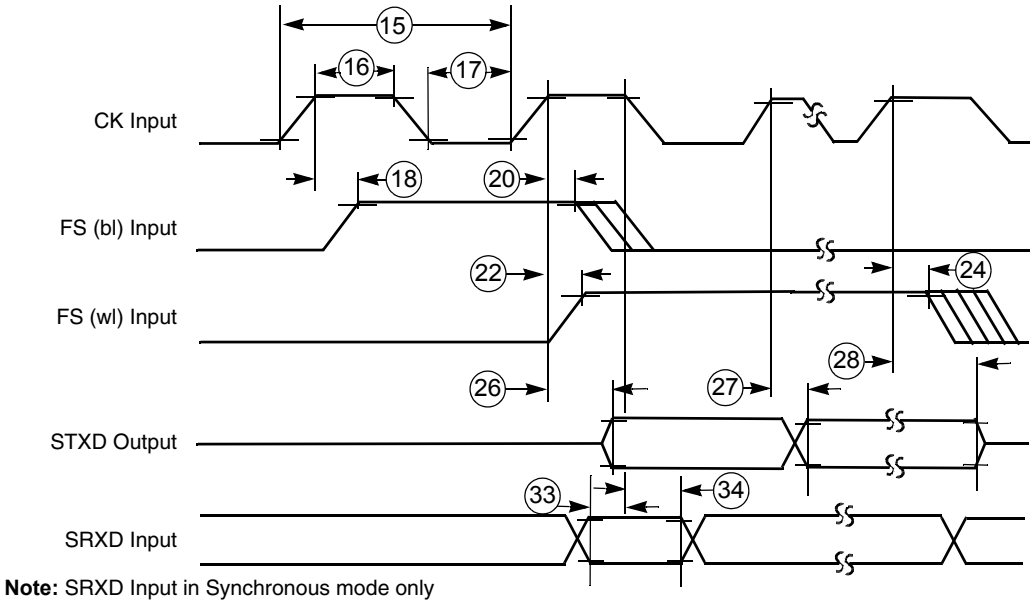



**Figure 43. SSI Receiver Internal Clock Timing Diagram**




**Note:** SRXD Input in Synchronous mode only

**Figure 44. SSI Transmitter External Clock Timing Diagram**

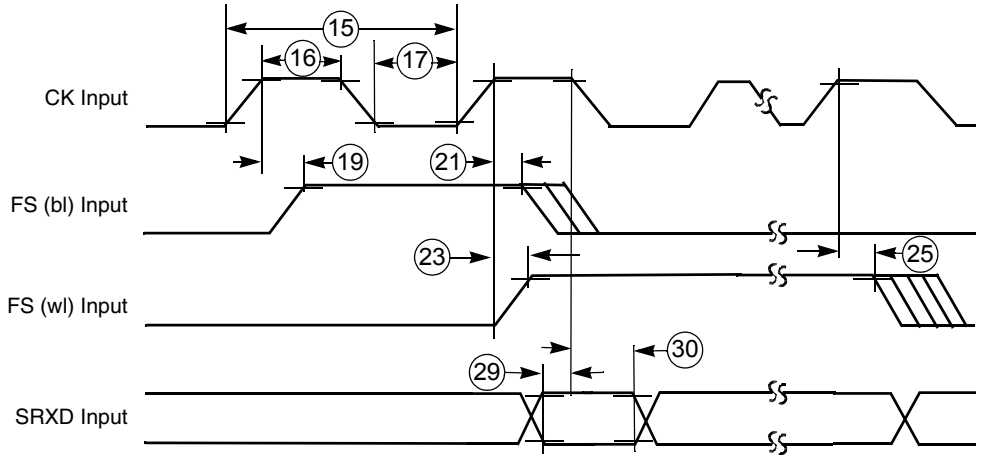



**Figure 45. SSI Receiver External Clock Timing Diagram**

**Table 33. SSI to SAP Ports Timing Parameters**

| Ref No. | Parameter | 1.8 V ± 0.1 V | | 3.0 V ± 0.3 V | | Unit |
|---|---|---|---|---|---|---|
| | | Minimum | Maximum | Minimum | Maximum | |
| **Internal Clock Operation[1] (SAP Ports)** | | | | | | |
| 1 | (Tx/Rx) CK clock period[1] | 90.91 | – | 90.91 | – | ns |
| 2 | (Tx) CK high to FS (bl) high | -3.30 | -1.16 | -2.98 | -1.10 | ns |
| 3 | (Rx) CK high to FS (bl) high | -3.93 | -1.34 | -4.18 | -1.43 | ns |
| 4 | (Tx) CK high to FS (bl) low | -3.30 | -1.16 | -2.98 | -1.10 | ns |
| 5 | (Rx) CK high to FS (bl) low | -3.93 | -1.34 | -4.18 | -1.43 | ns |
| 6 | (Tx) CK high to FS (wl) high | -3.30 | -1.16 | -2.98 | -1.10 | ns |
| 7 | (Rx) CK high to FS (wl) high | -3.93 | -1.34 | -4.18 | -1.43 | ns |
| 8 | (Tx) CK high to FS (wl) low | -3.30 | -1.16 | -2.98 | -1.10 | ns |
| 9 | (Rx) CK high to FS (wl) low | -3.93 | -1.34 | -4.18 | -1.43 | ns |
| 10 | (Tx) CK high to STXD valid from high impedance | -2.44 | -0.60 | -2.65 | -0.98 | ns |
| 11a | (Tx) CK high to STXD high | -2.44 | -0.60 | -2.65 | -0.98 | ns |
| 11b | (Tx) CK high to STXD low | -2.44 | -0.60 | -2.65 | -0.98 | ns |
| 12 | (Tx) CK high to STXD high impedance | -2.67 | -0.99 | -2.65 | -0.98 | ns |
| 13 | SRXD setup time before (Rx) CK low | 23.68 | – | 22.09 | – | ns |
| 14 | SRXD hold time after (Rx) CK low | 0 | – | 0 | – | ns |
| **External Clock Operation (SAP Ports)** | | | | | | |
| 15 | (Tx/Rx) CK clock period[1] | 90.91 | – | 90.91 | – | ns |
| 16 | (Tx/Rx) CK clock high period | 36.36 | – | 36.36 | – | ns |
| 17 | (Tx/Rx) CK clock low period | 36.36 | – | 36.36 | – | ns |
| 18 | (Tx) CK high to FS (bl) high | 10.24 | 19.50 | 7.16 | 8.65 | ns |
| 19 | (Rx) CK high to FS (bl) high | 10.89 | 21.27 | 7.63 | 9.12 | ns |
| 20 | (Tx) CK high to FS (bl) low | 10.24 | 19.50 | 7.16 | 8.65 | ns |
| 21 | (Rx) CK high to FS (bl) low | 10.89 | 21.27 | 7.63 | 9.12 | ns |
| 22 | (Tx) CK high to FS (wl) high | 10.24 | 19.50 | 7.16 | 8.65 | ns |
| 23 | (Rx) CK high to FS (wl) high | 10.89 | 21.27 | 7.63 | 9.12 | ns |
| 24 | (Tx) CK high to FS (wl) low | 10.24 | 19.50 | 7.16 | 8.65 | ns |
| 25 | (Rx) CK high to FS (wl) low | 10.89 | 21.27 | 7.63 | 9.12 | ns |
| 26 | (Tx) CK high to STXD valid from high impedance | 12.08 | 19.36 | 7.71 | 9.20 | ns |
| 27a | (Tx) CK high to STXD high | 10.80 | 19.36 | 7.71 | 9.20 | ns |
| 27b | (Tx) CK high to STXD low | 10.80 | 19.36 | 7.71 | 9.20 | ns |
| 28 | (Tx) CK high to STXD high impedance | 12.08 | 19.36 | 7.71 | 9.20 | ns |
| 29 | SRXD setup time before (Rx) CK low | 0.37 | – | 0.42 | – | ns |
| 30 | SRXD hole time after (Rx) CK low | 0 | – | 0 | – | ns |

**Table 33. SSI to SAP Ports Timing Parameters (Continued)**

| Ref No. | Parameter | 1.8 V ± 0.1 V | | 3.0 V ± 0.3 V | | Unit |
|---|---|---|---|---|---|---|
| | | Minimum | Maximum | Minimum | Maximum | |
| **Synchronous Internal Clock Operation (SAP Ports)** | | | | | | |
| 31 | SRXD setup before (Tx) CK falling | 23.00 | – | 21.41 | – | ns |
| 32 | SRXD hold after (Tx) CK falling | 0 | – | 0 | – | ns |
| **Synchronous External Clock Operation (SAP Ports)** | | | | | | |
| 33 | SRXD setup before (Tx) CK falling | 1.20 | – | 0.88 | – | ns |
| 34 | SRXD hold after (Tx) CK falling | 0 | – | 0 | – | ns |

1. All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

**Table 34. SSI to SSI1 Ports Timing Parameters**

| Ref No. | Parameter | 1.8 V ± 0.1 V | | 3.0 V ± 0.3 V | | Unit |
|---|---|---|---|---|---|---|
| | | Minimum | Maximum | Minimum | Maximum | |
| **Internal Clock Operation[1] (SSI1 Ports)** | | | | | | |
| 1 | (Tx/Rx) CK clock period[1] | 90.91 | – | 90.91 | – | ns |
| 2 | (Tx) CK high to FS (bl) high | -0.68 | -0.15 | -0.68 | -0.15 | ns |
| 3 | (Rx) CK high to FS (bl) high | -0.96 | -0.27 | -0.96 | -0.27 | ns |
| 4 | (Tx) CK high to FS (bl) low | -0.68 | -0.15 | -0.68 | -0.15 | ns |
| 5 | (Rx) CK high to FS (bl) low | -0.96 | -0.27 | -0.96 | -0.27 | ns |
| 6 | (Tx) CK high to FS (wl) high | -0.68 | -0.15 | -0.68 | -0.15 | ns |
| 7 | (Rx) CK high to FS (wl) high | -0.96 | -0.27 | -0.96 | -0.27 | ns |
| 8 | (Tx) CK high to FS (wl) low | -0.68 | -0.15 | -0.68 | -0.15 | ns |
| 9 | (Rx) CK high to FS (wl) low | -0.96 | -0.27 | -0.96 | -0.27 | ns |
| 10 | (Tx) CK high to STXD valid from high impedance | -1.68 | -0.36 | -1.68 | -0.36 | ns |
| 11a | (Tx) CK high to STXD high | -1.68 | -0.36 | -1.68 | -0.36 | ns |
| 11b | (Tx) CK high to STXD low | -1.68 | -0.36 | -1.68 | -0.36 | ns |
| 12 | (Tx) CK high to STXD high impedance | -1.58 | -0.31 | -1.58 | -0.31 | ns |
| 13 | SRXD setup time before (Rx) CK low | 20.41 | – | 20.41 | – | ns |
| 14 | SRXD hold time after (Rx) CK low | 0 | – | 0 | – | ns |
| **External Clock Operation (SSI1 Ports)** | | | | | | |
| 15 | (Tx/Rx) CK clock period[1] | 90.91 | – | 90.91 | – | ns |
| 16 | (Tx/Rx) CK clock high period | 36.36 | – | 36.36 | – | ns |
| 17 | (Tx/Rx) CK clock low period | 36.36 | – | 36.36 | – | ns |
| 18 | (Tx) CK high to FS (bl) high | 10.22 | 17.63 | 8.82 | 16.24 | ns |
| 19 | (Rx) CK high to FS (bl) high | 10.79 | 19.67 | 9.39 | 18.28 | ns |

**Table 34. SSI to SSI1 Ports Timing Parameters (Continued)**

| Ref No. | Parameter | 1.8 V ± 0.1 V | | 3.0 V ± 0.3 V | | Unit |
|---|---|---|---|---|---|---|
| | | Minimum | Maximum | Minimum | Maximum | |
| 20 | (Tx) CK high to FS (bl) low | 10.22 | 17.63 | 8.82 | 16.24 | ns |
| 21 | (Rx) CK high to FS (bl) low | 10.79 | 19.67 | 9.39 | 18.28 | ns |
| 22 | (Tx) CK high to FS (wl) high | 10.22 | 17.63 | 8.82 | 16.24 | ns |
| 23 | (Rx) CK high to FS (wl) high | 10.79 | 19.67 | 9.39 | 18.28 | ns |
| 24 | (Tx) CK high to FS (wl) low | 10.22 | 17.63 | 8.82 | 16.24 | ns |
| 25 | (Rx) CK high to FS (wl) low | 10.79 | 19.67 | 9.39 | 18.28 | ns |
| 26 | (Tx) CK high to STXD valid from high impedance | 10.05 | 15.75 | 8.66 | 14.36 | ns |
| 27a | (Tx) CK high to STXD high | 10.00 | 15.63 | 8.61 | 14.24 | ns |
| 27b | (Tx) CK high to STXD low | 10.00 | 15.63 | 8.61 | 14.24 | ns |
| 28 | (Tx) CK high to STXD high impedance | 10.05 | 15.75 | 8.66 | 14.36 | ns |
| 29 | SRXD setup time before (Rx) CK low | 0.78 | – | 0.47 | – | ns |
| 30 | SRXD hole time after (Rx) CK low | 0 | – | 0 | – | ns |
| **Synchronous Internal Clock Operation (SSI1 Ports)** | | | | | | |
| 31 | SRXD setup before (Tx) CK falling | 19.90 | – | 19.90 | – | ns |
| 32 | SRXD hold after (Tx) CK falling | 0 | – | 0 | – | ns |
| **Synchronous External Clock Operation (SSI1 Ports)** | | | | | | |
| 33 | SRXD setup before (Tx) CK falling | 2.59 | – | 2.28 | – | ns |
| 34 | SRXD hold after (Tx) CK falling | 0 | – | 0 | – | ns |

1. All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

**Table 35. SSI to SSI2 Ports Timing Parameters**

| Ref No. | Parameter | 1.8 V ± 0.1 V | | 3.0 V ± 0.3 V | | Unit |
|---|---|---|---|---|---|---|
| | | Minimum | Maximum | Minimum | Maximum | |
| **Internal Clock Operation[1] (SSI2 Ports)** | | | | | | |
| 1 | (Tx/Rx) CK clock period[1] | 90.91 | – | 90.91 | – | ns |
| 2 | (Tx) CK high to FS (bl) high | 0.01 | 0.15 | 0.01 | 0.15 | ns |
| 3 | (Rx) CK high to FS (bl) high | -0.21 | 0.05 | -0.21 | 0.05 | ns |
| 4 | (Tx) CK high to FS (bl) low | 0.01 | 0.15 | 0.01 | 0.15 | ns |
| 5 | (Rx) CK high to FS (bl) low | -0.21 | 0.05 | -0.21 | 0.05 | ns |
| 6 | (Tx) CK high to FS (wl) high | 0.01 | 0.15 | 0.01 | 0.15 | ns |
| 7 | (Rx) CK high to FS (wl) high | -0.21 | 0.05 | -0.21 | 0.05 | ns |
| 8 | (Tx) CK high to FS (wl) low | 0.01 | 0.15 | 0.01 | 0.15 | ns |
| 9 | (Rx) CK high to FS (wl) low | -0.21 | 0.05 | -0.21 | 0.05 | ns |
| 10 | (Tx) CK high to STXD valid from high impedance | 0.34 | 0.72 | 0.34 | 0.72 | ns |

**Table 35. SSI to SSI2 Ports Timing Parameters (Continued)**

| Ref No. | Parameter | 1.8 V ± 0.1 V | | 3.0 V ± 0.3 V | | Unit |
|---|---|---|---|---|---|---|
| | | Minimum | Maximum | Minimum | Maximum | |
| 11a | (Tx) CK high to STXD high | 0.34 | 0.72 | 0.34 | 0.72 | ns |
| 11b | (Tx) CK high to STXD low | 0.34 | 0.72 | 0.34 | 0.72 | ns |
| 12 | (Tx) CK high to STXD high impedance | 0.34 | 0.48 | 0.34 | 0.48 | ns |
| 13 | SRXD setup time before (Rx) CK low | 21.50 | – | 21.50 | – | ns |
| 14 | SRXD hold time after (Rx) CK low | 0 | – | 0 | – | ns |
| **External Clock Operation (SSI2 Ports)** | | | | | | |
| 15 | (Tx/Rx) CK clock period[1] | 90.91 | – | 90.91 | – | ns |
| 16 | (Tx/Rx) CK clock high period | 36.36 | – | 36.36 | – | ns |
| 17 | (Tx/Rx) CK clock low period | 36.36 | – | 36.36 | – | ns |
| 18 | (Tx) CK high to FS (bl) high | 10.40 | 17.37 | 8.67 | 15.88 | ns |
| 19 | (Rx) CK high to FS (bl) high | 11.00 | 19.70 | 9.28 | 18.21 | ns |
| 20 | (Tx) CK high to FS (bl) low | 10.40 | 17.37 | 8.67 | 15.88 | ns |
| 21 | (Rx) CK high to FS (bl) low | 11.00 | 19.70 | 9.28 | 18.21 | ns |
| 22 | (Tx) CK high to FS (wl) high | 10.40 | 17.37 | 8.67 | 15.88 | ns |
| 23 | (Rx) CK high to FS (wl) high | 11.00 | 19.70 | 9.28 | 18.21 | ns |
| 24 | (Tx) CK high to FS (wl) low | 10.40 | 17.37 | 8.67 | 15.88 | ns |
| 25 | (Rx) CK high to FS (wl) low | 11.00 | 19.70 | 9.28 | 18.21 | ns |
| 26 | (Tx) CK high to STXD valid from high impedance | 9.59 | 17.08 | 7.86 | 15.59 | ns |
| 27a | (Tx) CK high to STXD high | 9.59 | 17.08 | 7.86 | 15.59 | ns |
| 27b | (Tx) CK high to STXD low | 9.59 | 17.08 | 7.86 | 15.59 | ns |
| 28 | (Tx) CK high to STXD high impedance | 9.59 | 16.84 | 7.86 | 15.35 | ns |
| 29 | SRXD setup time before (Rx) CK low | 2.52 | – | 2.52 | – | ns |
| 30 | SRXD hole time after (Rx) CK low | 0 | – | 0 | – | ns |
| **Synchronous Internal Clock Operation (SSI2 Ports)** | | | | | | |
| 31 | SRXD setup before (Tx) CK falling | 20.78 | – | 20.78 | – | ns |
| 32 | SRXD hold after (Tx) CK falling | 0 | – | 0 | – | ns |
| **Synchronous External Clock Operation (SSI2 Ports)** | | | | | | |
| 33 | SRXD setup before (Tx) CK falling | 4.42 | – | 4.42 | – | ns |
| 34 | SRXD hold after (Tx) CK falling | 0 | – | 0 | – | ns |

1. All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

**Table 36. SSI to SSI3 Ports Timing Parameters**

| Ref No. | Parameter | 1.8 V ± 0.1 V | | 3.0 V ± 0.3 V | | Unit |
|---|---|---|---|---|---|---|
| | | Minimum | Maximum | Minimum | Maximum | |
| **Internal Clock Operation[1] (SSI3 Ports)** | | | | | | |
| 1 | (Tx/Rx) CK clock period[1] | 90.91 | – | 90.91 | – | ns |
| 2 | (Tx) CK high to FS (bl) high | -2.09 | -0.66 | -2.09 | -0.66 | ns |
| 3 | (Rx) CK high to FS (bl) high | -2.74 | -0.84 | -2.74 | -0.84 | ns |
| 4 | (Tx) CK high to FS (bl) low | -2.09 | -0.66 | -2.09 | -0.66 | ns |
| 5 | (Rx) CK high to FS (bl) low | -2.74 | -0.84 | -2.74 | -0.84 | ns |
| 6 | (Tx) CK high to FS (wl) high | -2.09 | -0.66 | -2.09 | -0.66 | ns |
| 7 | (Rx) CK high to FS (wl) high | -2.74 | -0.84 | -2.74 | -0.84 | ns |
| 8 | (Tx) CK high to FS (wl) low | -2.09 | -0.66 | -2.09 | -0.66 | ns |
| 9 | (Rx) CK high to FS (wl) low | -2.74 | -0.84 | -2.74 | -0.84 | ns |
| 10 | (Tx) CK high to STXD valid from high impedance | -1.73 | -0.26 | -1.73 | -0.26 | ns |
| 11a | (Tx) CK high to STXD high | -2.87 | -0.80 | -2.87 | -0.80 | ns |
| 11b | (Tx) CK high to STXD low | -2.87 | -0.80 | -2.87 | -0.80 | ns |
| 12 | (Tx) CK high to STXD high impedance | -1.73 | -0.26 | -1.73 | -0.26 | ns |
| 13 | SRXD setup time before (Rx) CK low | 22.77 | – | 22.77 | – | ns |
| 14 | SRXD hold time after (Rx) CK low | 0 | – | 0 | – | ns |
| **External Clock Operation (SSI3 Ports)** | | | | | | |
| 15 | (Tx/Rx) CK clock period[1] | 90.91 | – | 90.91 | – | ns |
| 16 | (Tx/Rx) CK clock high period | 36.36 | – | 36.36 | – | ns |
| 17 | (Tx/Rx) CK clock low period | 36.36 | – | 36.36 | – | ns |
| 18 | (Tx) CK high to FS (bl) high | 9.62 | 17.10 | 7.90 | 15.61 | ns |
| 19 | (Rx) CK high to FS (bl) high | 10.30 | 19.54 | 8.58 | 18.05 | ns |
| 20 | (Tx) CK high to FS (bl) low | 9.62 | 17.10 | 7.90 | 15.61 | ns |
| 21 | (Rx) CK high to FS (bl) low | 10.30 | 19.54 | 8.58 | 18.05 | ns |
| 22 | (Tx) CK high to FS (wl) high | 9.62 | 17.10 | 7.90 | 15.61 | ns |
| 23 | (Rx) CK high to FS (wl) high | 10.30 | 19.54 | 8.58 | 18.05 | ns |
| 24 | (Tx) CK high to FS (wl) low | 9.62 | 17.10 | 7.90 | 15.61 | ns |
| 25 | (Rx) CK high to FS (wl) low | 10.30 | 19.54 | 8.58 | 18.05 | ns |
| 26 | (Tx) CK high to STXD valid from high impedance | 9.02 | 16.46 | 7.29 | 14.97 | ns |
| 27a | (Tx) CK high to STXD high | 8.48 | 15.32 | 6.75 | 13.83 | ns |
| 27b | (Tx) CK high to STXD low | 8.48 | 15.32 | 6.75 | 13.83 | ns |

**Table 36. SSI to SSI3 Ports Timing Parameters (Continued)**

| Ref No. | Parameter | 1.8 V ± 0.1 V | | 3.0 V ± 0.3 V | | Unit |
|---|---|---|---|---|---|---|
| | | Minimum | Maximum | Minimum | Maximum | |
| 28 | (Tx) CK high to STXD high impedance | 9.02 | 16.46 | 7.29 | 14.97 | ns |
| 29 | SRXD setup time before (Rx) CK low | 1.49 | – | 1.49 | – | ns |
| 30 | SRXD hole time after (Rx) CK low | 0 | – | 0 | – | ns |
| **Synchronous Internal Clock Operation (SSI3 Ports)** | | | | | | |
| 31 | SRXD setup before (Tx) CK falling | 21.99 | – | 21.99 | – | ns |
| 32 | SRXD hold after (Tx) CK falling | 0 | – | 0 | – | ns |
| **Synchronous External Clock Operation (SSI3 Ports)** | | | | | | |
| 33 | SRXD setup before (Tx) CK falling | 3.80 | – | 3.80 | – | ns |
| 34 | SRXD hold after (Tx) CK falling | 0 | – | 0 | – | ns |

1. All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.

## 3.17 1-Wire Interface Timing

### 3.17.1 Reset Sequence with Reset Pulse Presence Pulse

To begin any communications with the DS2502, it is required that an initialization procedure be issued. A reset pulse must be generated and then a presence pulse must be detected. The minimum reset pulse length is 480 us. The bus master (one-wire) will generate this pulse, then after the DS2502 detects a rising edge on the one-wire bus, it will wait 15-60 us before it will transmit back a presence pulse. The presence pulse will exist for 60-240 us.

The timing diagram for this sequence is shown in Figure 46.

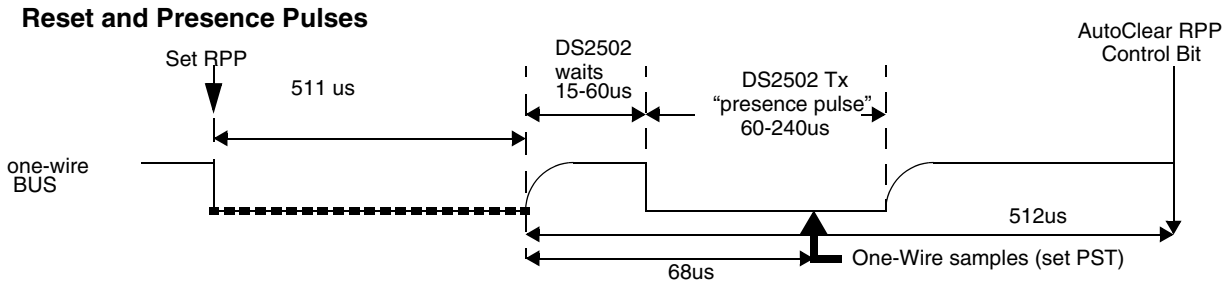



**Figure 46. 1-Wire Initialization**

The reset pulse begins the initialization sequence and it is initiated when the RPP control register bit is set. When the presence pulse is detected, this bit will be cleared. The presence pulse is used by the bus master to determine if at least one DS2502 is connected. Software will determine if more than one DS2502 exists. The one-wire will sample for the DS2502 presence pulse. The presence pulse is latched in the one-wire

control register PST. When the PST bit is set to a one, it means that a DS2502 is present; if the bit is set to a zero, then no device was found.

### 3.17.2 Write 0

The Write 0 function simply writes a zero bit to the DS2502. The sequence takes 117 us. The one-wire bus is held low for 100us.

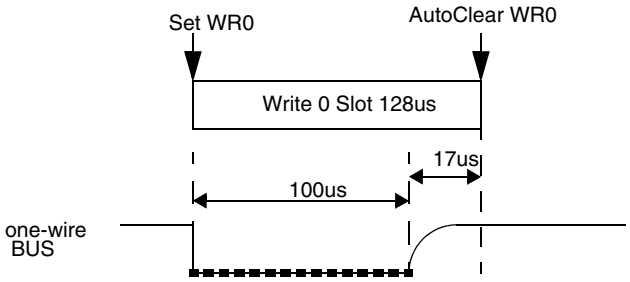



**Figure 47. Write 0 Timing**

The Write 0 pulse sequence is initiated when the WR0 control bit register is set. When the write is complete, the WR0 register will be auto cleared.

### 3.17.3 Write 1/Read Data

The Write 1 and Read timing is identical. The time slot is first driven low. According to the DS2502 documentation, the DS2502 has a delay circuit which is used to synchronize the DS2502 with the bus master (one-wire). This delay circuit is triggered by the falling edge of the data line and is used to decide when the DS2502 should sample the line. In the case of a write 1 or read 1, after a delay, a 1 will be transmitted / received. When a read 0 slot is issued, the delay circuit will hold the data line low to override the 1 generated by the bus master (one-wire).

For the Write 1 or Read, the control register WR1/RD is set and auto-cleared when the sequence has been completed. After a Read, the control register RDST bit is set to the value of the read.

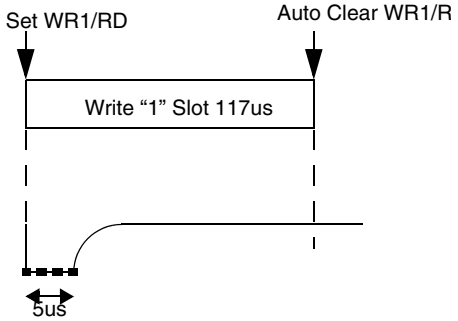



**Figure 48. Write 1 Timing**

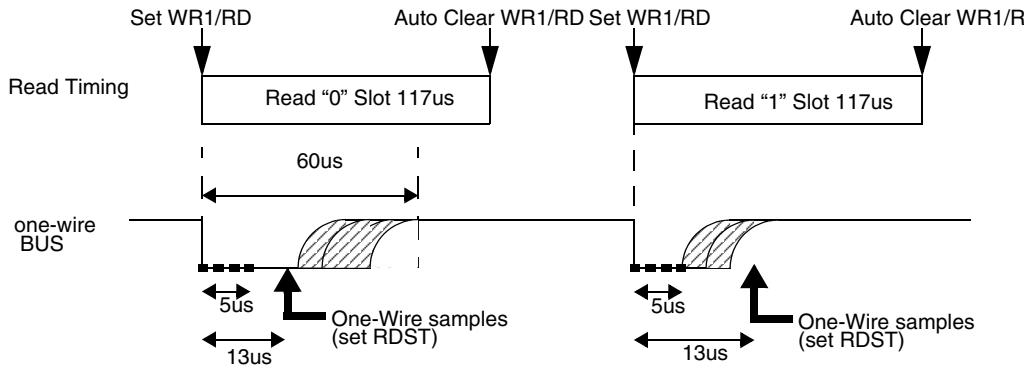



**Figure 49. Read Timing**

The precision of the generated clock is very important to get a proper behavior of the one-wire module. This module is based on a state machine which undertakes actions at defined times.

**Table 37. System Timing Requirements**

| Times | Values (Microsec) | Minimum (Microsec) | Maximum (microsec) | Absolute Precision | Relative Precision |
|---|---|---|---|---|---|
| RSTL | 511 | 480 | – | 31 | 0.0645 |
| PST | 68 | 60 | 75 | 7 | 0.1 |
| RSTH | 512 | 480 | – | 32 | 0.0645 |
| LOW0 | 100 | 60 | 120 | 20 | 0.2 |
| LOWR | 5 | 1 | 15 | 4 | 0.8 |
| READ_sample | 13 | – | 15 | 2 | 0.15 |

The most stringent constraint is 0.0645 as a relative time imprecision.

The time relative precision is directly derived from the frequency of the derivative clock (f):

Time relative precision = 1/f -1 = divider/clock (MHz) - 1

The Figure 38 gathers relative time precision for different main clock frequencies.

**Table 38. System Clock Requirements**

| Main Clock Frequency (MHz) | 13 | 16.8 | 19.44 |
|---|---|---|---|
| Clock divide ratio | 13 | 17 | 19 |
| Generated frequency (MHz) | 1 | 0.9882 | 1.023 |
| Relative time imprecision | 0 | 0.0117 | 0.023 |

This shows that the user should take care of the main clock frequency when using the one-wire module. If the main clock is an exact integer multiple of 1 MHz, then the generated frequency will be exactly 1 MHz.

**NOTE:**

A main clock frequency below 10 MHz might cause a misbehavior of the module.

## 3.18 USB On-The-Go

Four types of data transfer modes exist for the USB module: control transfers, bulk transfers, isochronous transfers and interrupt transfers. From the perspective of the USB module, the interrupt transfer type is identical to the bulk data transfer mode, and no additional hardware is supplied to support it. This section covers the transfer modes and how they work from the ground up.

Data moves across the USB in packets. Groups of packets are combined to form data transfers. The same packet transfer mechanism applies to bulk, interrupt, and control transfers. Isochronous data is also moved in the form of packets, but because isochronous pipes are given a fixed portion of the USB bandwidth at all times, there is no end-of-transfer.

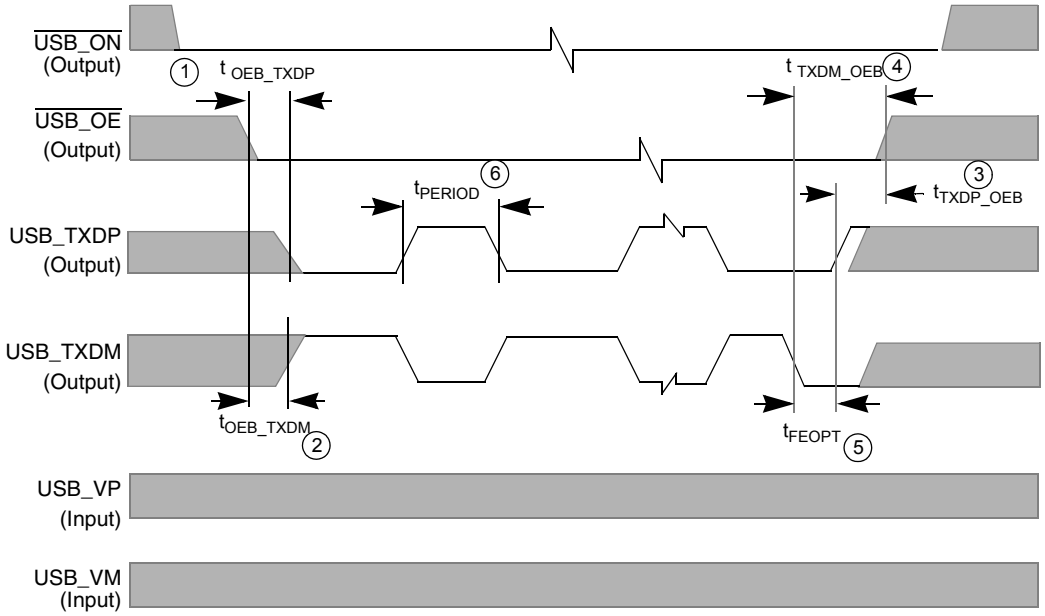



**Figure 50. USB Timing Diagram for Data Transfer to USB Transceiver (TX)**

**Table 39. USB Timing Parameters for Data Transfer to USB Transceiver (TX)**

| Ref No. | Parameter | 3.0 V ± 0.3 V | | Unit |
|---|---|---|---|---|
| | | Minimum | Maximum | |
| 1 | $t_{OEB_TXDP}$; $\overline{USBD_OE}$ active to USBD_TXDP low | 83.14 | 83.47 | ns |
| 2 | $t_{OEB_TXDM}$; $\overline{USBD_OE}$ active to USBD_TXDM high | 81.55 | 81.98 | ns |
| 3 | $t_{TXDP_OEB}$; USBD_TXDP high to $\overline{USBD_OE}$ deactivated | 83.54 | 83.8 | ns |
| 4 | $t_{TXDM_OEB}$; USBD_TXDM low to $\overline{USBD_OE}$ deactivated (includes SE0) | 248.9 | 249.13 | ns |
| 5 | $t_{FEOPT}$; SE0 interval of EOP | 160 | 175 | ns |
| 6 | $t_{PERIOD}$; Data transfer rate | 11.97 | 12.03 | Mb/s |

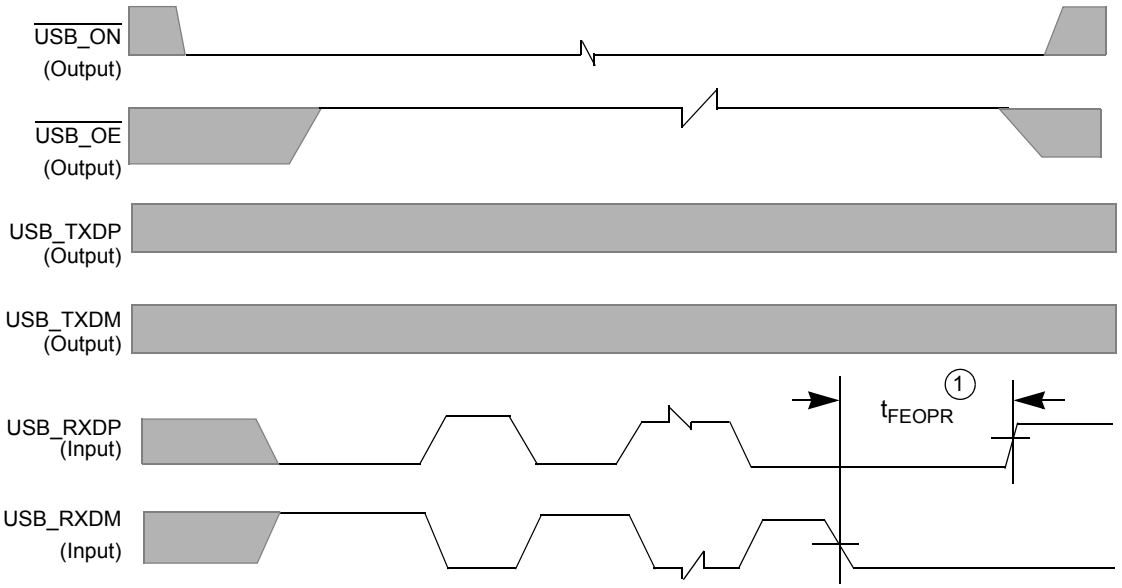



**Figure 51. USB Timing Diagram for Data Transfer from USB Transceiver (RX)**

**Table 40. USB Timing Parameters for Data Transfer from USB Transceiver (RX)**

| Ref No. | Parameter | 3.0 V ± 0.3 V | | Unit |
|---|---|---|---|---|
| | | Minimum | Maximum | |
| 1 | $t_{FEOPR}$; Receiver SE0 interval of EOP | 82 | – | ns |

The USBOTG I$^2$C communication protocol consists of six components: START, Data Source/Recipient, Data Direction, Slave Acknowledge, Data, Data Acknowledge, and STOP.

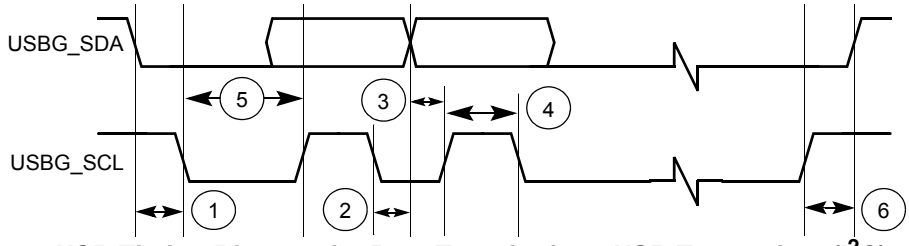



**Figure 52. USB Timing Diagram for Data Transfer from USB Transceiver (I$^2$C)**

**Table 41. USB Timing Parameters for Data Transfer from USB Transceiver (I$^2$C)**

| Ref No. | Parameter | 1.8 V ± 0.1 V | | Unit |
|---|---|---|---|---|
| | | Minimum | Maximum | |
| 1 | Hold time (repeated) START condition | 188 | – | ns |
| 2 | Data hold time | 0 | 188 | ns |
| 3 | Data setup time | 88 | – | ns |
| 4 | HIGH period of the SCL clock | 500 | – | ns |
| 5 | LOW period of the SCL clock | 500 | – | ns |
| 6 | Setup time for STOP condition | 185 | – | ns |

## 3.19 External Interface Module (EIM)

The External Interface Module (EIM) handles the interface to devices external to the i.MX21, including generation of chip-selects for external peripherals and memory. The timing diagram for the EIM is shown in Figure 53, and Table 42 defines the parameters of signals.

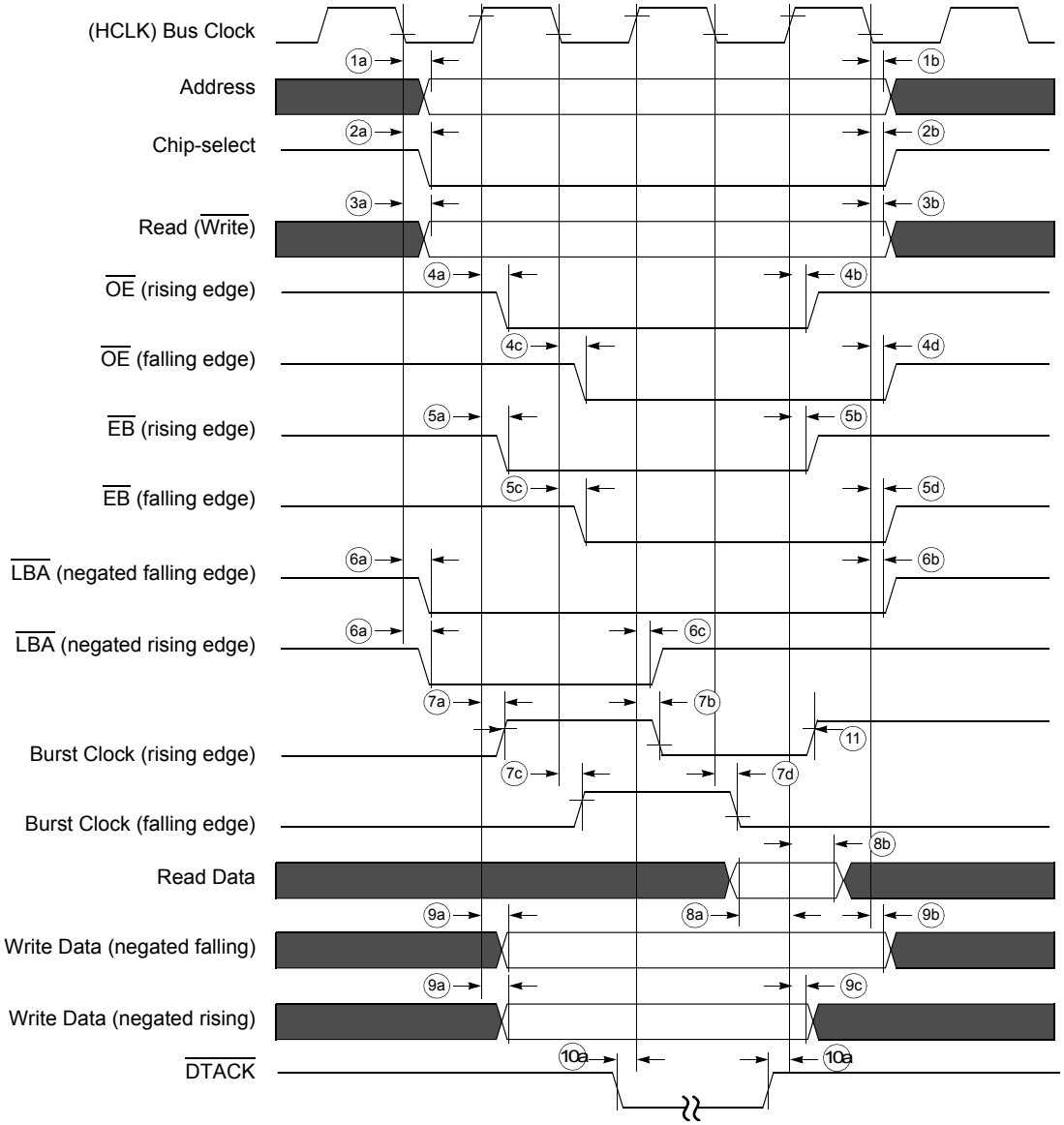



**Figure 53. EIM Bus Timing Diagram**

**Table 42. EIM Bus Timing Parameters**

| Ref No. | Parameter | 1.8 V ± 0.1 V | | 3.0 V ± 0.3 V | | | 1.8 V ± 0.1 V | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typical | Max | Min | Typical | Max | |
| 1a | Clock fall to address valid | 3.97 | 6.02 | 9.89 | 3.83 | 5.89 | 9.79 | ns |
| 1b | Clock fall to address invalid | 3.93 | 6.00 | 9.86 | 3.81 | 5.86 | 9.76 | ns |
| 2a | Clock fall to chip-select valid | 3.47 | 5.59 | 8.62 | 3.30 | 5.09 | 8.45 | ns |
| 2b | Clock fall to chip-select invalid | 3.39 | 5.09 | 8.27 | 3.15 | 4.85 | 8.03 | ns |
| 3a | Clock fall to Read ($\overline{\text{Write}}$) Valid | 3.51 | 5.56 | 8.79 | 3.39 | 5.39 | 8.51 | ns |
| 3b | Clock fall to Read ($\overline{\text{Write}}$) Invalid | 3.59 | 5.37 | 9.14 | 3.36 | 5.20 | 8.50 | ns |
| 4a | Clock[1] rise to Output Enable Valid | 3.62 | 5.49 | 8.98 | 3.46 | 5.33 | 9.02 | ns |
| 4b | Clock[1] rise to Output Enable Invalid | 3.70 | 5.61 | 9.26 | 3.46 | 5.37 | 8.81 | ns |
| 4c | Clock[1] fall to Output Enable Valid | 3.60 | 5.48 | 8.77 | 3.44 | 5.30 | 8.88 | ns |
| 4d | Clock[1] fall to Output Enable Invalid | 3.69 | 5.62 | 9.12 | 3.42 | 5.36 | 8.60 | ns |
| 5a | Clock[1] rise to Enable Bytes Valid | 3.69 | 5.46 | 8.71 | 3.46 | 5.25 | 8.54 | ns |
| 5b | Clock[1] rise to Enable Bytes Invalid | 4.64 | 5.47 | 8.70 | 3.46 | 5.25 | 8.54 | ns |
| 5c | Clock[1] fall to Enable Bytes Valid | 3.52 | 5.06 | 8.39 | 3.41 | 5.18 | 8.36 | ns |
| 5d | Clock[1] fall to Enable Bytes Invalid | 3.50 | 5.05 | 8.27 | 3.41 | 5.18 | 8.36 | ns |
| 6a | Clock[1] fall to Load Burst Address Valid | 3.65 | 5.28 | 8.69 | 3.30 | 5.23 | 8.81 | ns |
| 6b | Clock[1] fall to Load Burst Address Invalid | 3.65 | 5.67 | 9.36 | 3.41 | 5.43 | 9.13 | ns |
| 6c | Clock[1] rise to Load Burst Address Invalid | 3.66 | 5.69 | 9.48 | 3.33 | 5.47 | 9.25 | ns |
| 7a | Clock[1] rise to Burst Clock rise | 3.50 | 5.22 | 8.42 | 3.26 | 4.99 | 8.19 | ns |
| 7b | Clock[1]rise to Burst Clock fall | 3.49 | 5.19 | 8.30 | 3.31 | 5.03 | 8.17 | ns |
| 7c | Clock[1] fall to Burst Clock rise | 3.50 | 5.22 | 8.39 | 3.26 | 4.98 | 8.15 | ns |
| 7d | Clock[1] fall to Burst Clock fall | 3.49 | 5.19 | 8.29 | 3.31 | 5.02 | 8.12 | ns |
| 8a | Read Data setup time | 4.54 | – | – | 4.54 | – | – | ns |
| 8b | Read Data hold time | 0.5 | – | – | 0.5 | – | – | ns |
| 9a | Clock[1] rise to Write Data Valid | 4.13 | 5.86 | 9.16 | 3.95 | 6.36 | 10.31 | ns |
| 9b | Clock[1] fall to Write Data Invalid | 4.10 | 5.79 | 9.15 | 4.04 | 6.27 | 9.16 | ns |
| 9c | Clock[1] rise to Write Data Invalid | 4.02 | 5.81 | 9.37 | 4.22 | 5.29 | 9.24 | ns |
| 10a | DTACK setup time | 2.65 | 4.63 | 8.40 | 2.64 | 4.61 | 8.41 | ns |
| 11 | Burst Clock (BCLK) cycle time | 15 | – | – | 15 | – | – | ns |

1. Clock refers to the system clock signal, HCLK, generated from the System DPLL

### 3.19.1 EIM External Bus Timing Diagrams

The following timing diagrams show the timing of accesses to memory or a peripheral.

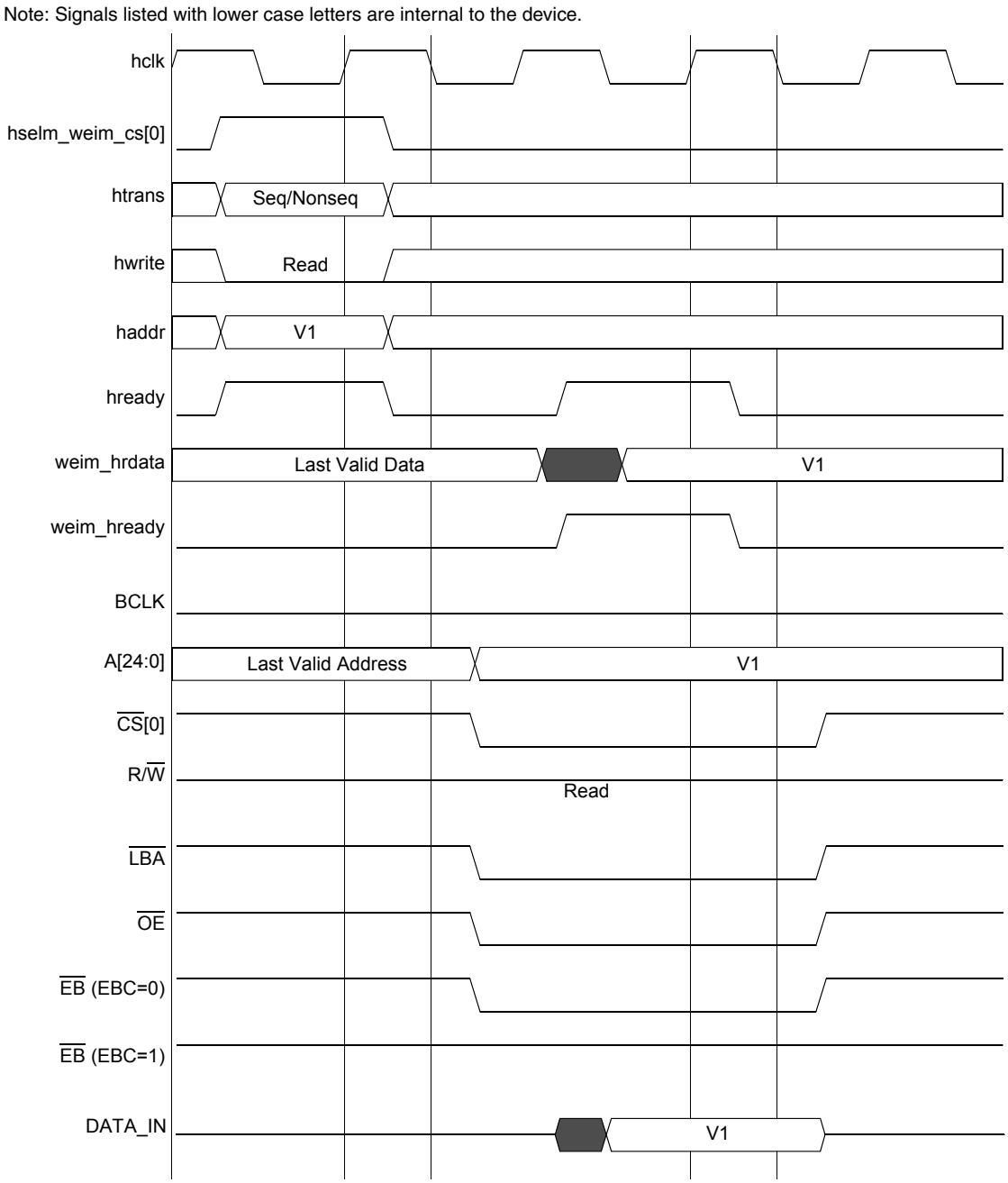



**Figure 54. WSC = 1, A.HALF/E.HALF**

Note: Signals listed with lower case letters are internal to the device.

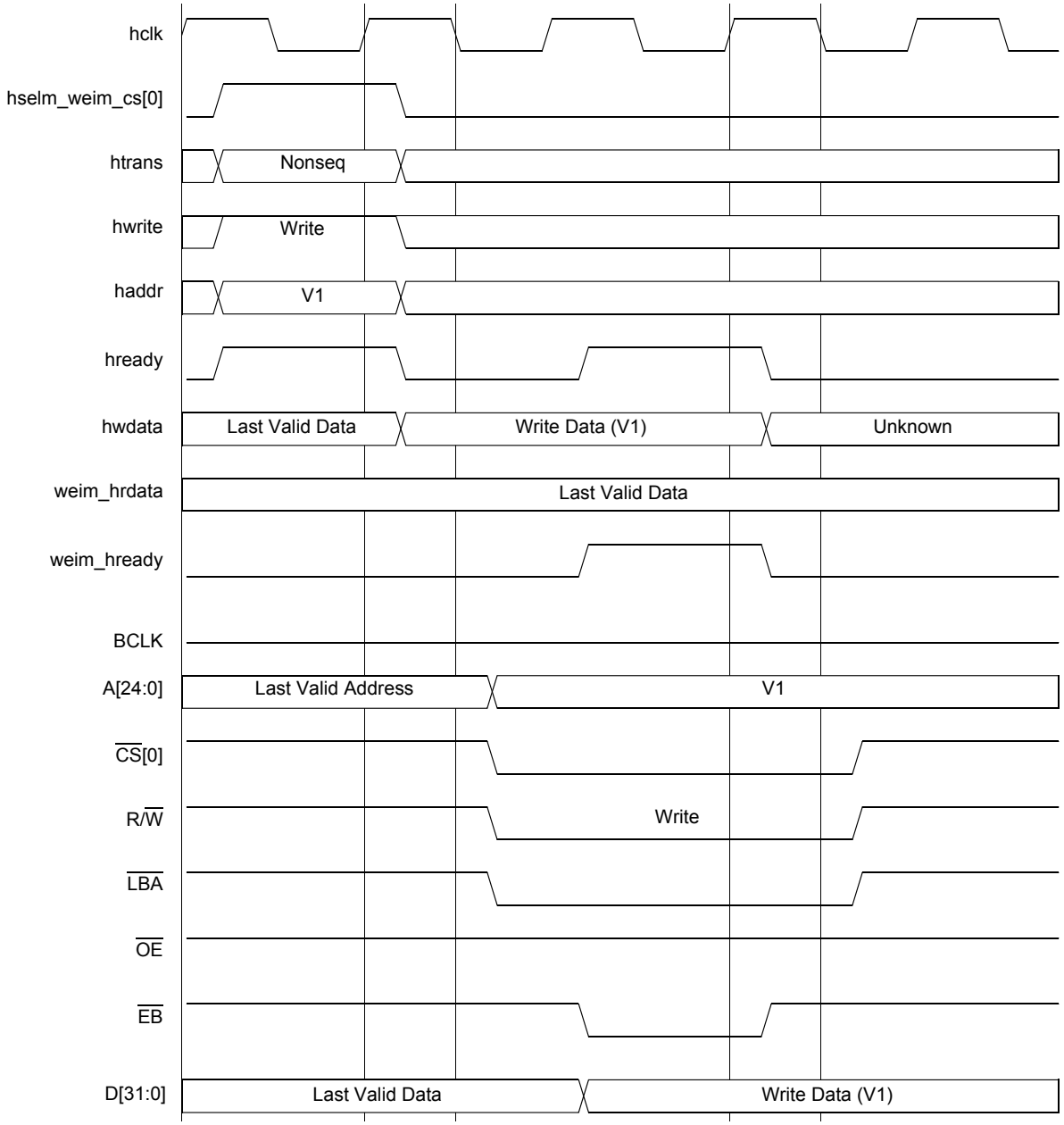



**Figure 55. WSC = 1, WEA = 1, WEN = 1, A.HALF/E.HALF**

Note: Signals listed with lower case letters are internal to the device.

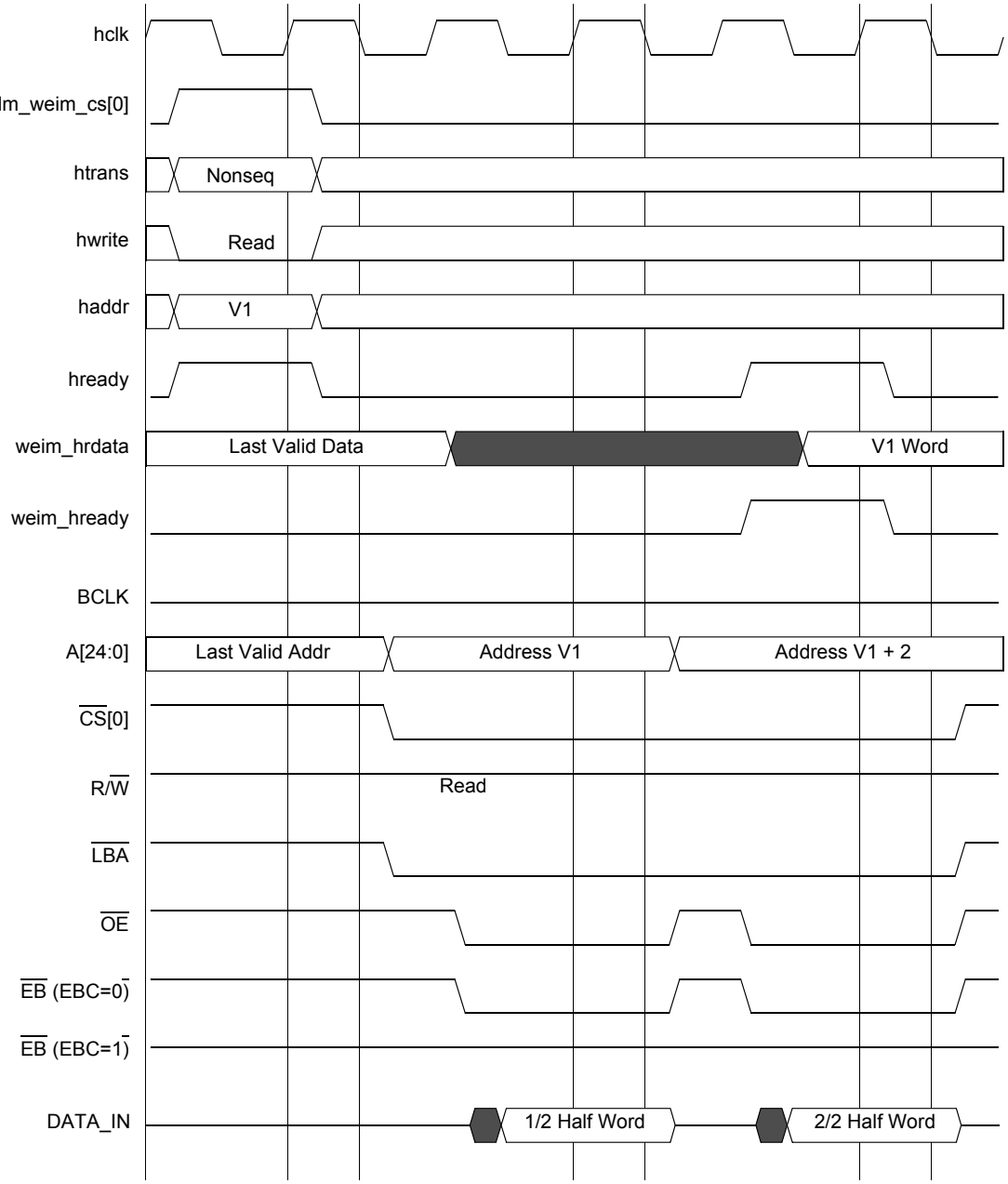



**Figure 56. WSC = 1, OEA = 1, A.WORD/E.HALF**

Note: Signals listed with lower case letters are internal to the device.

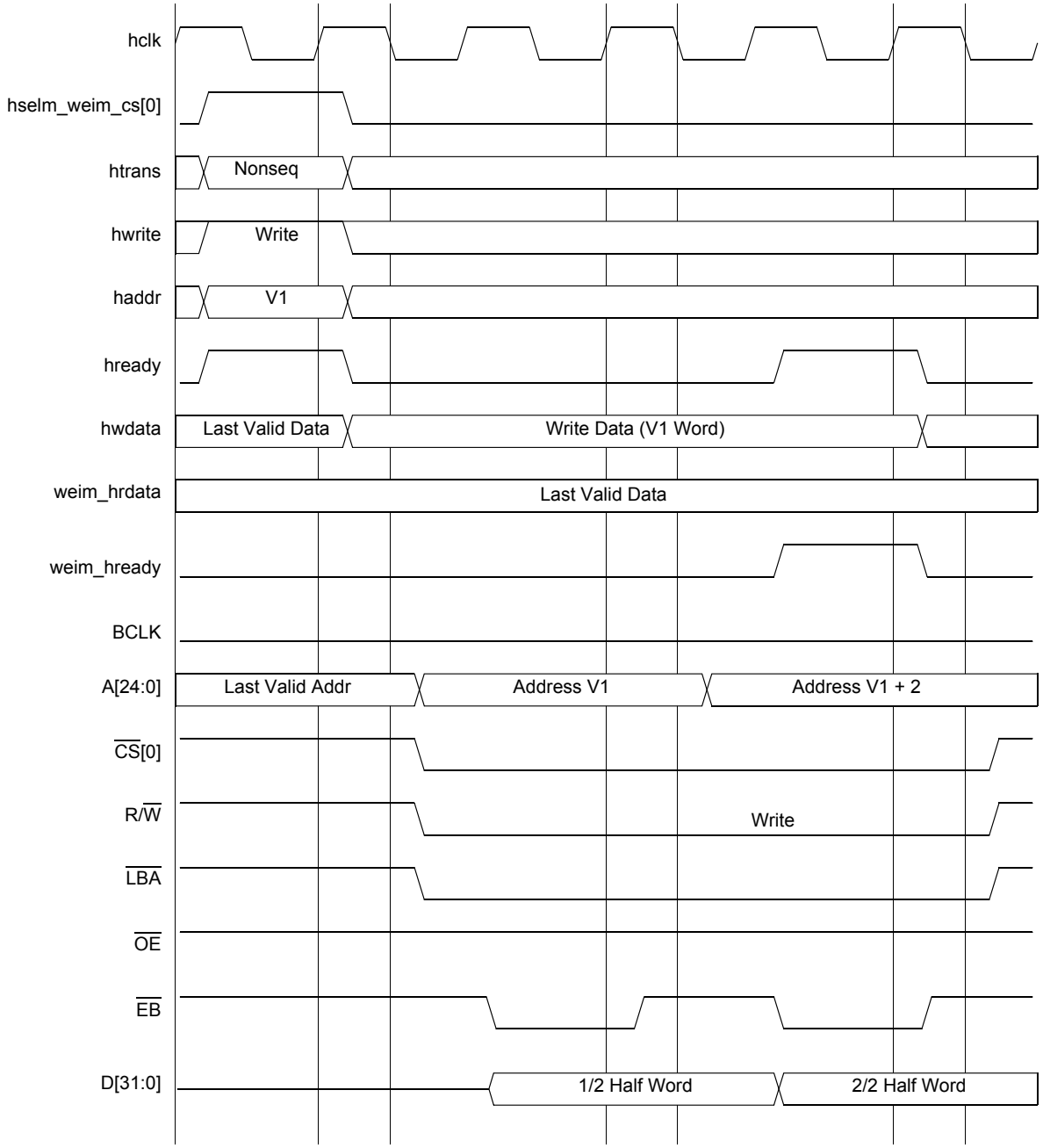



**Figure 57. WSC = 1, WEA = 1, WEN = 1, A.WORD/E.HALF**

Note: Signals listed with lower case letters are internal to the device.

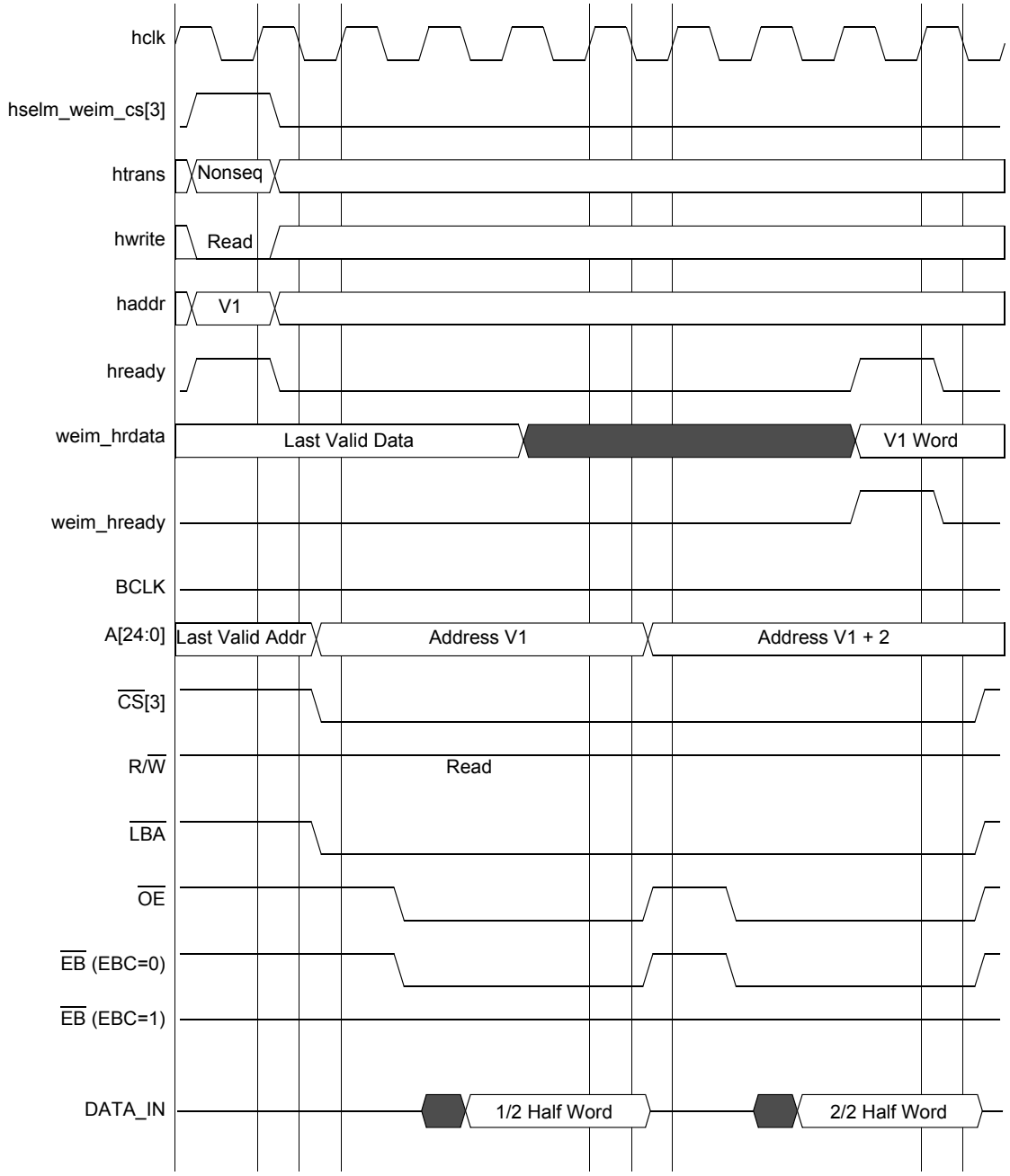



**Figure 58. WSC = 3, OEA = 2, A.WORD/E.HALF**

Note: Signals listed with lower case letters are internal to the device.

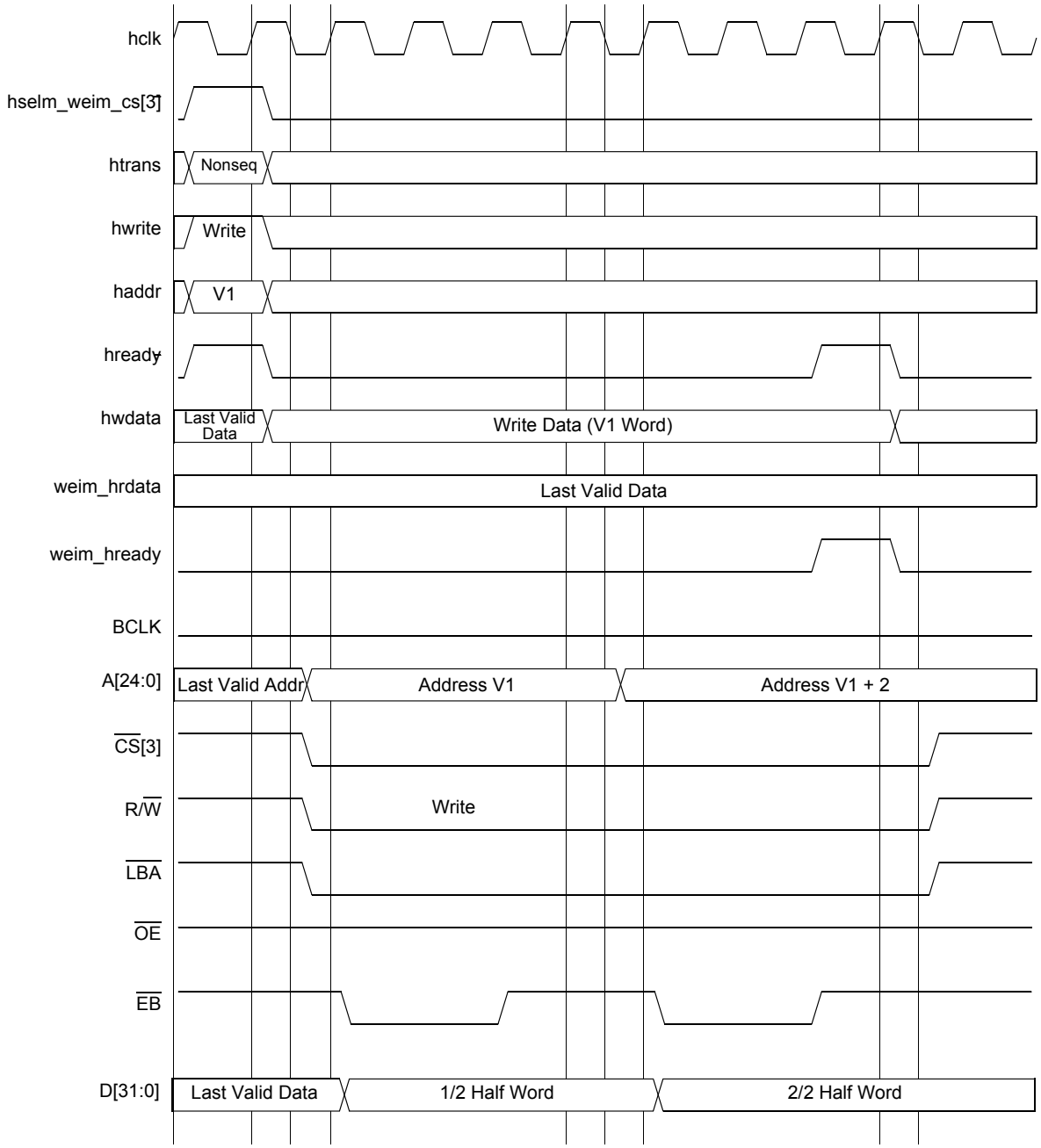



**Figure 59. WSC = 3, WEA = 1, WEN = 3, A.WORD/E.HALF**

Note: Signals listed with lower case letters are internal to the device.

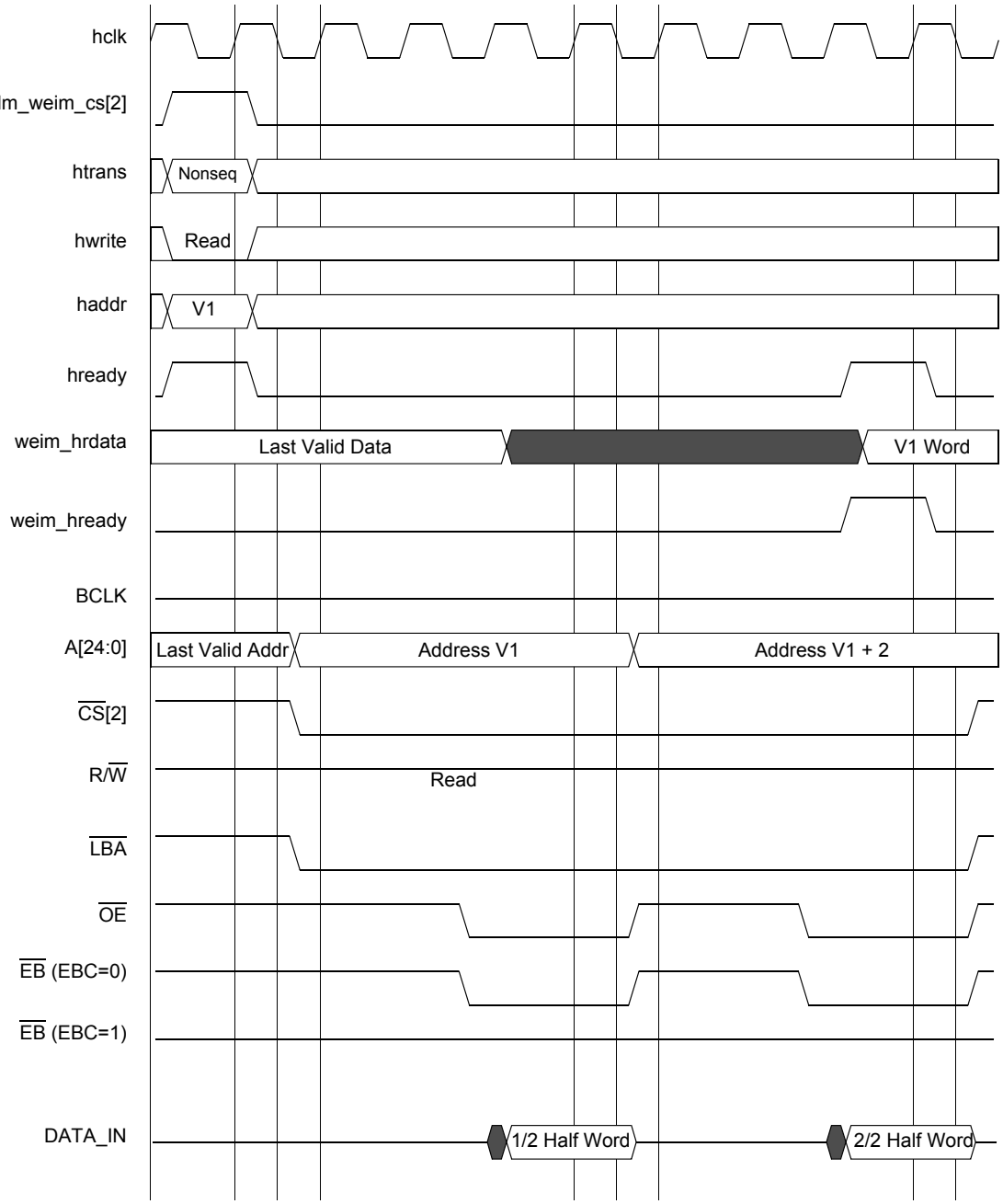



**Figure 60. WSC = 3, OEA = 4, A.WORD/E.HALF**

Note: Signals listed with lower case letters are internal to the device.

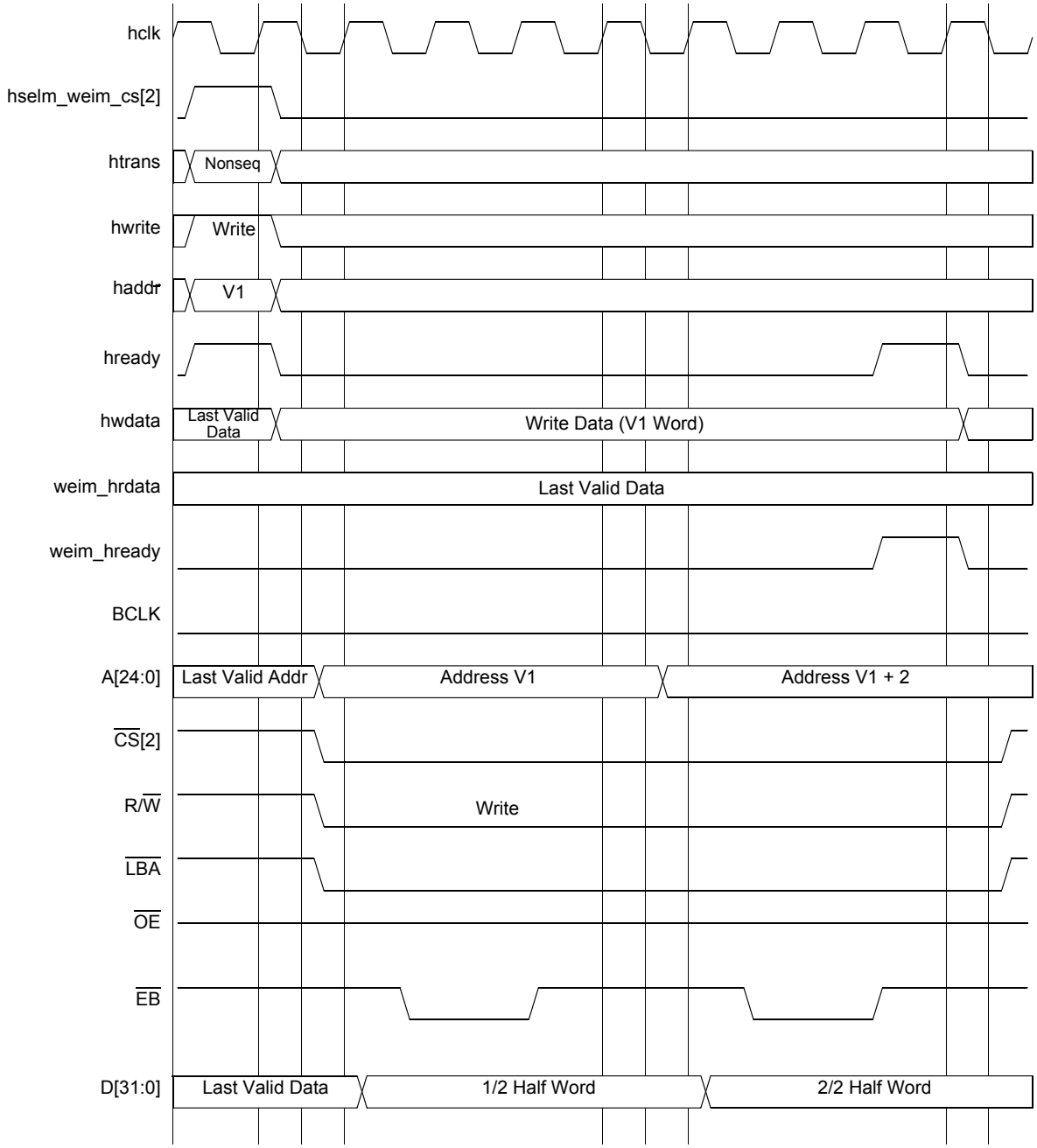



**Figure 61. WSC = 3, WEA = 2, WEN = 3, A.WORD/E.HALF**

Note: Signals listed with lower case letters are internal to the device.

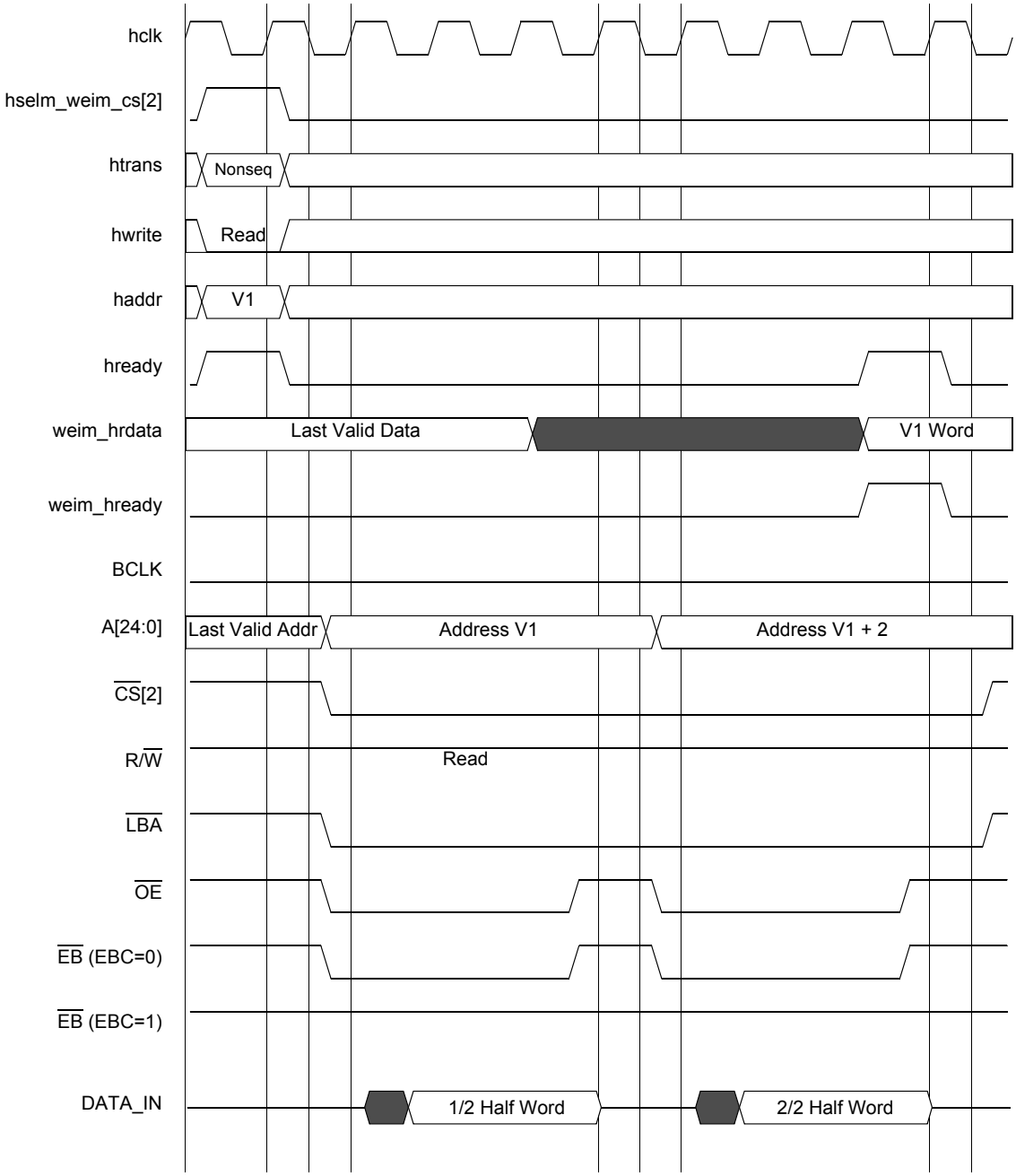



**Figure 62. WSC = 3, OEN = 2, A.WORD/E.HALF**

Note: Signals listed with lower case letters are internal to the device.

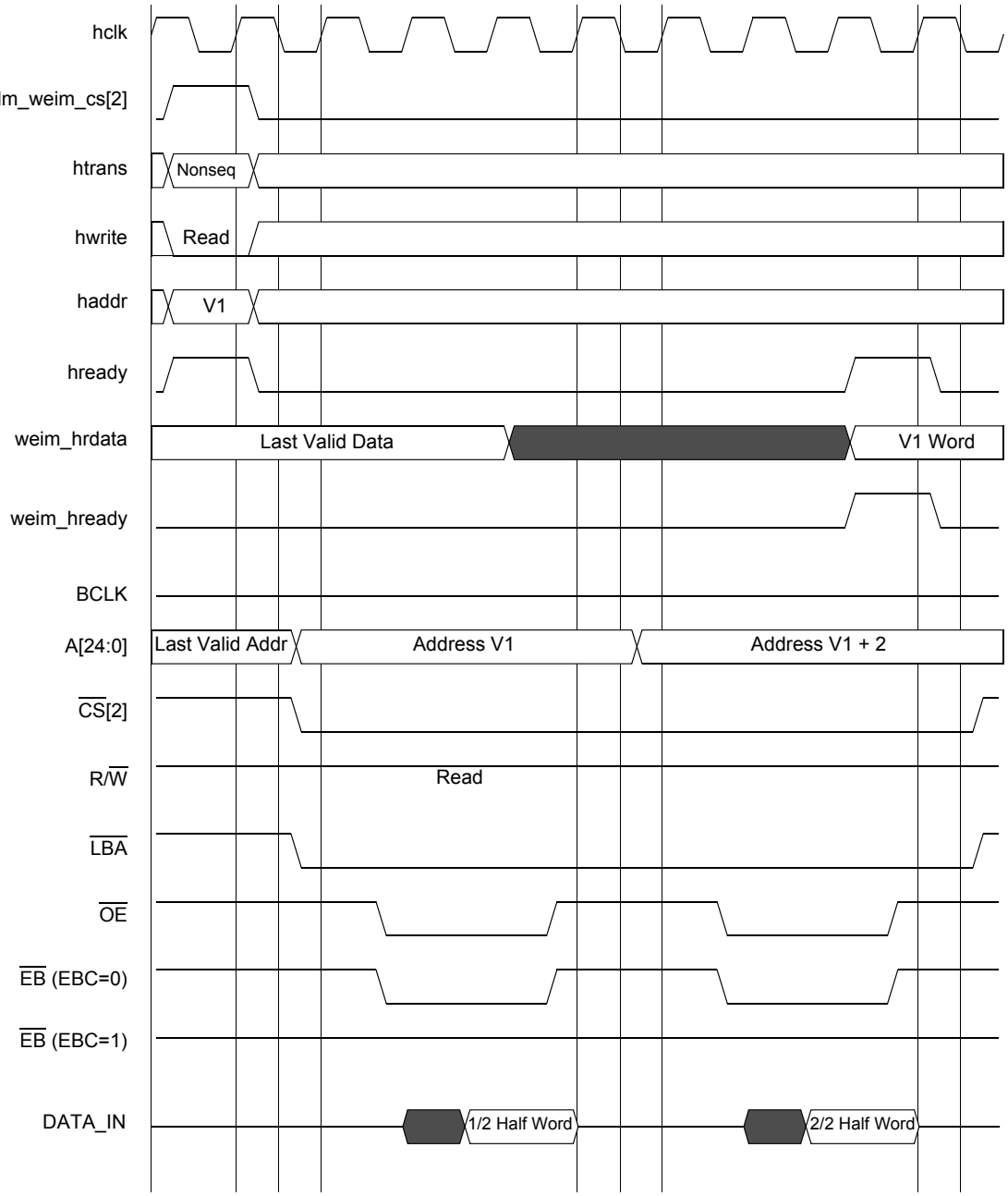



**Figure 63. WSC = 3, OEA = 2, OEN = 2, A.WORD/E.HALF**

Note: Signals listed with lower case letters are internal to the device.

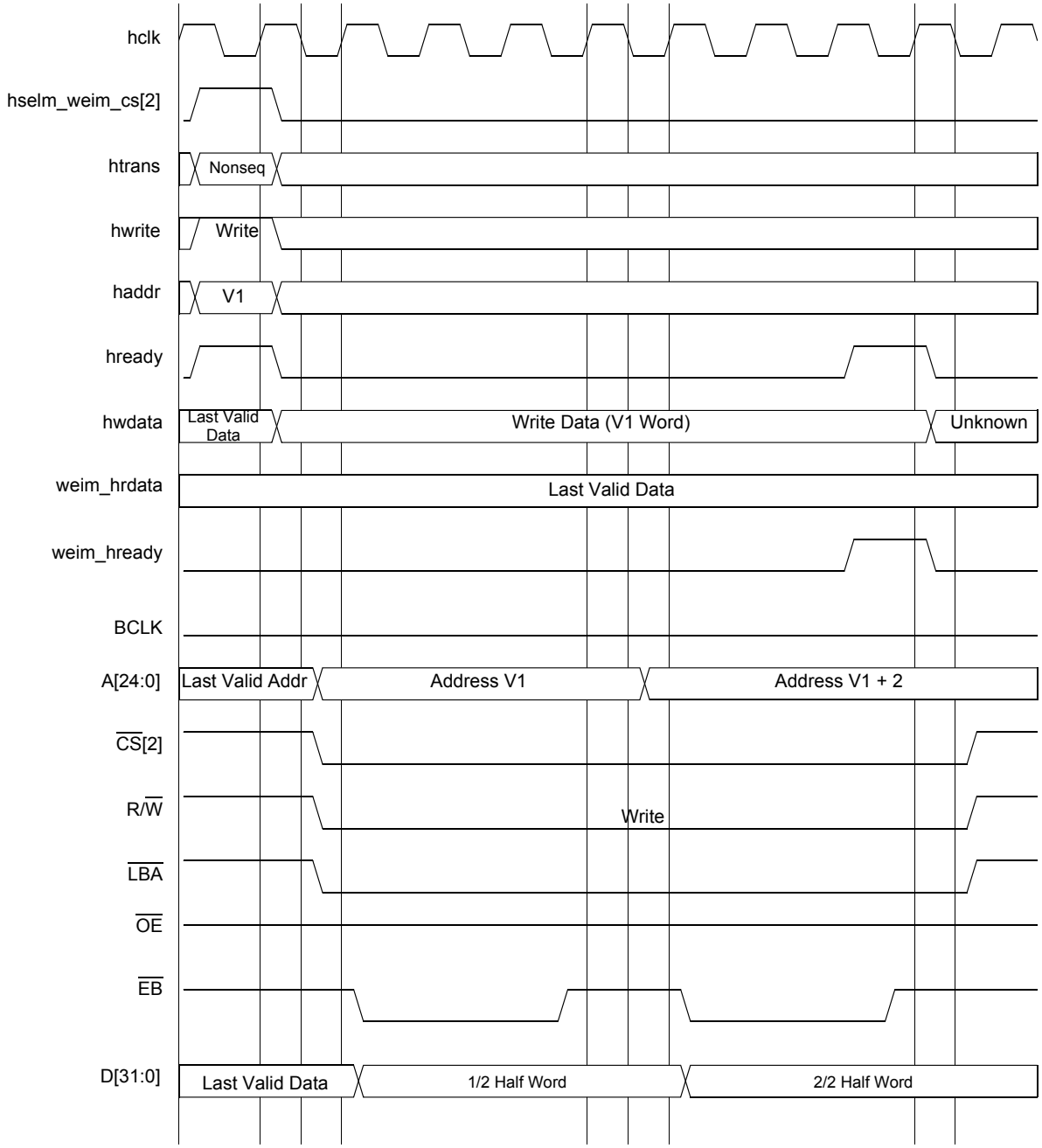



**Figure 64. WSC = 2, WWS = 1, WEA = 1, WEN = 2, A.WORD/E.HALF**

Note: Signals listed with lower case letters are internal to the device.

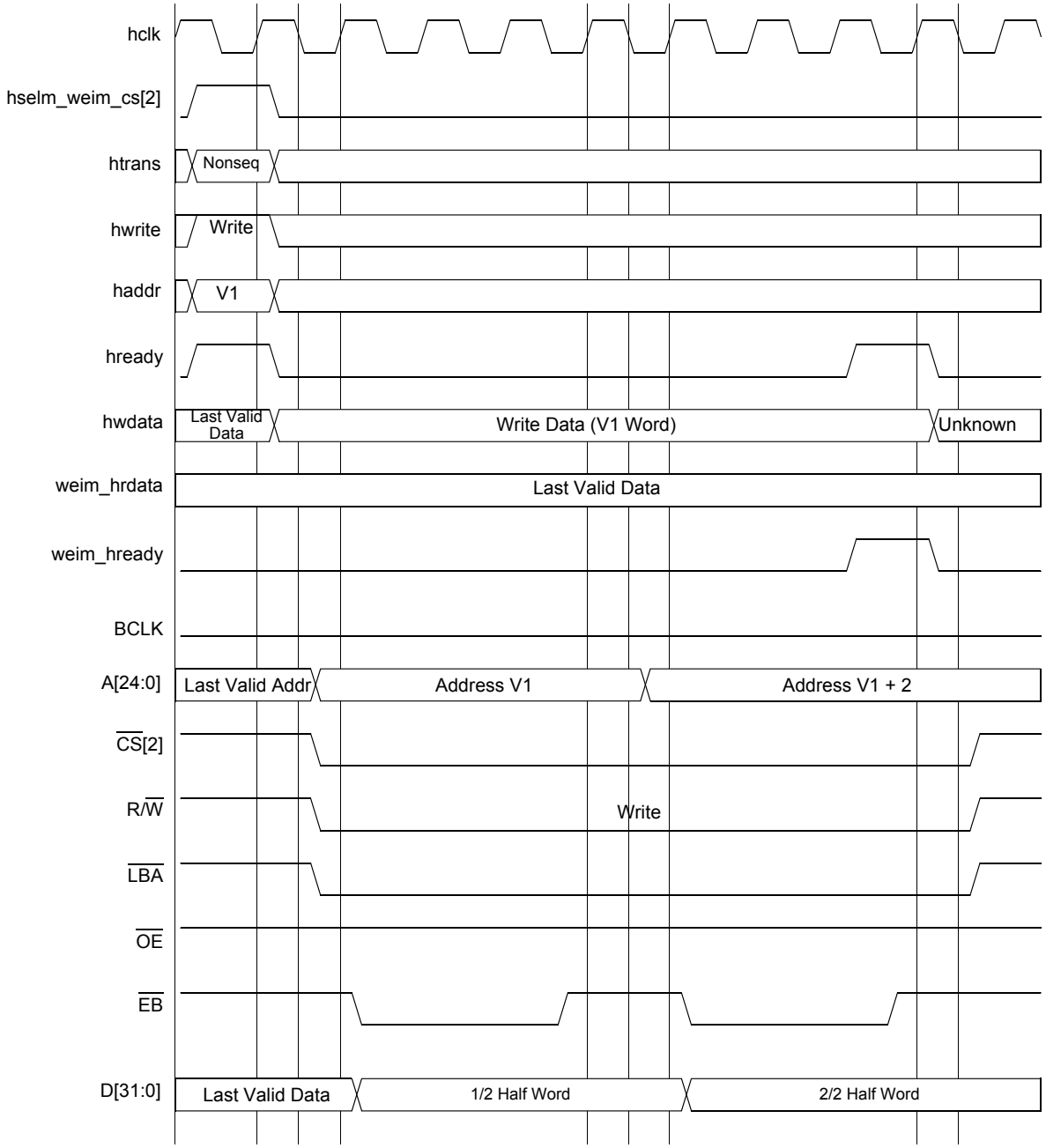



**Figure 65. WSC = 1, WWS = 2, WEA = 1, WEN = 2, A.WORD/E.HALF**

Note: Signals listed with lower case letters are internal to the device.

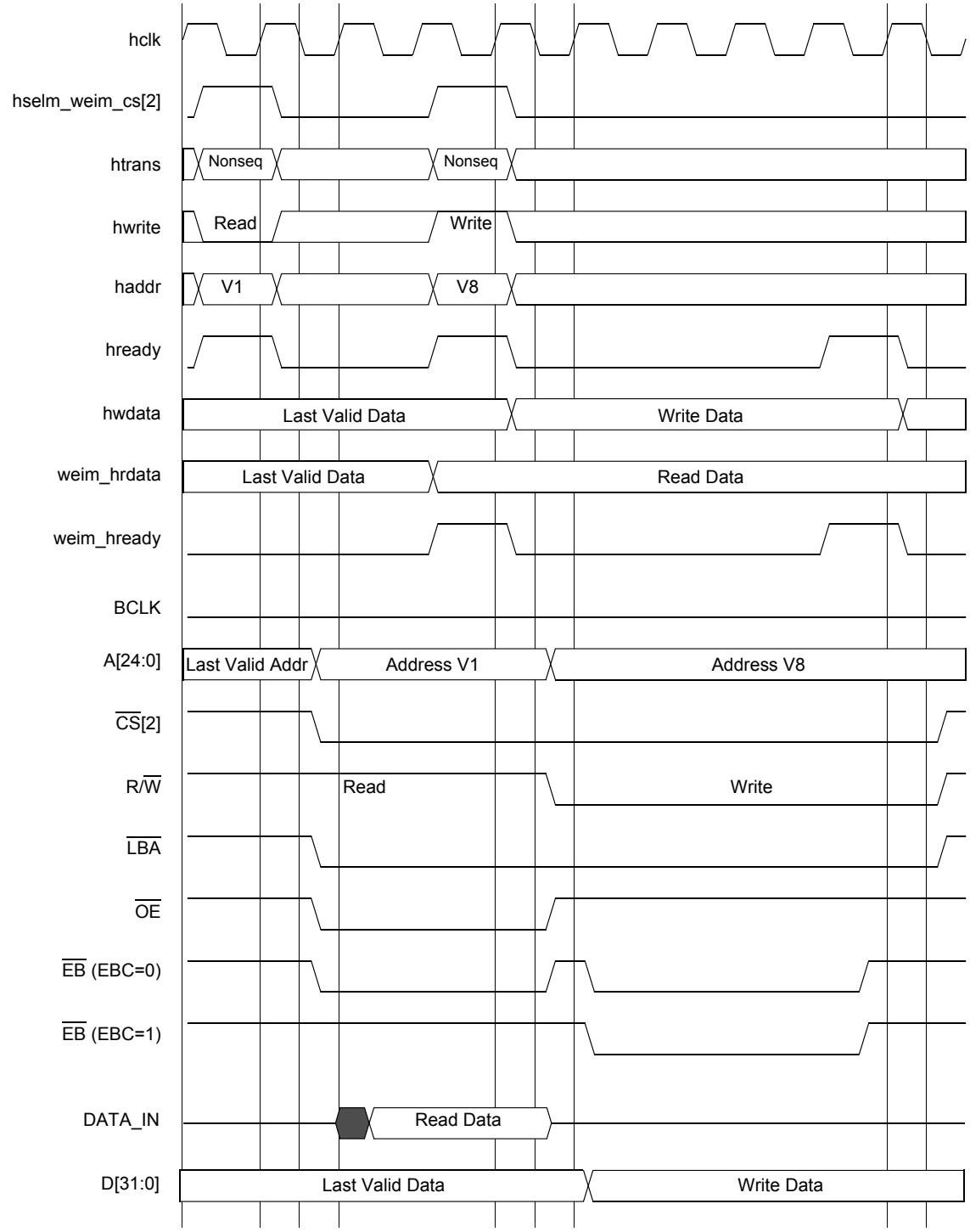



**Figure 66. WSC = 2, WWS = 2, WEA = 1, WEN = 2, A.HALF/E.HALF**

Note: Signals listed with lower case letters are internal to the device.

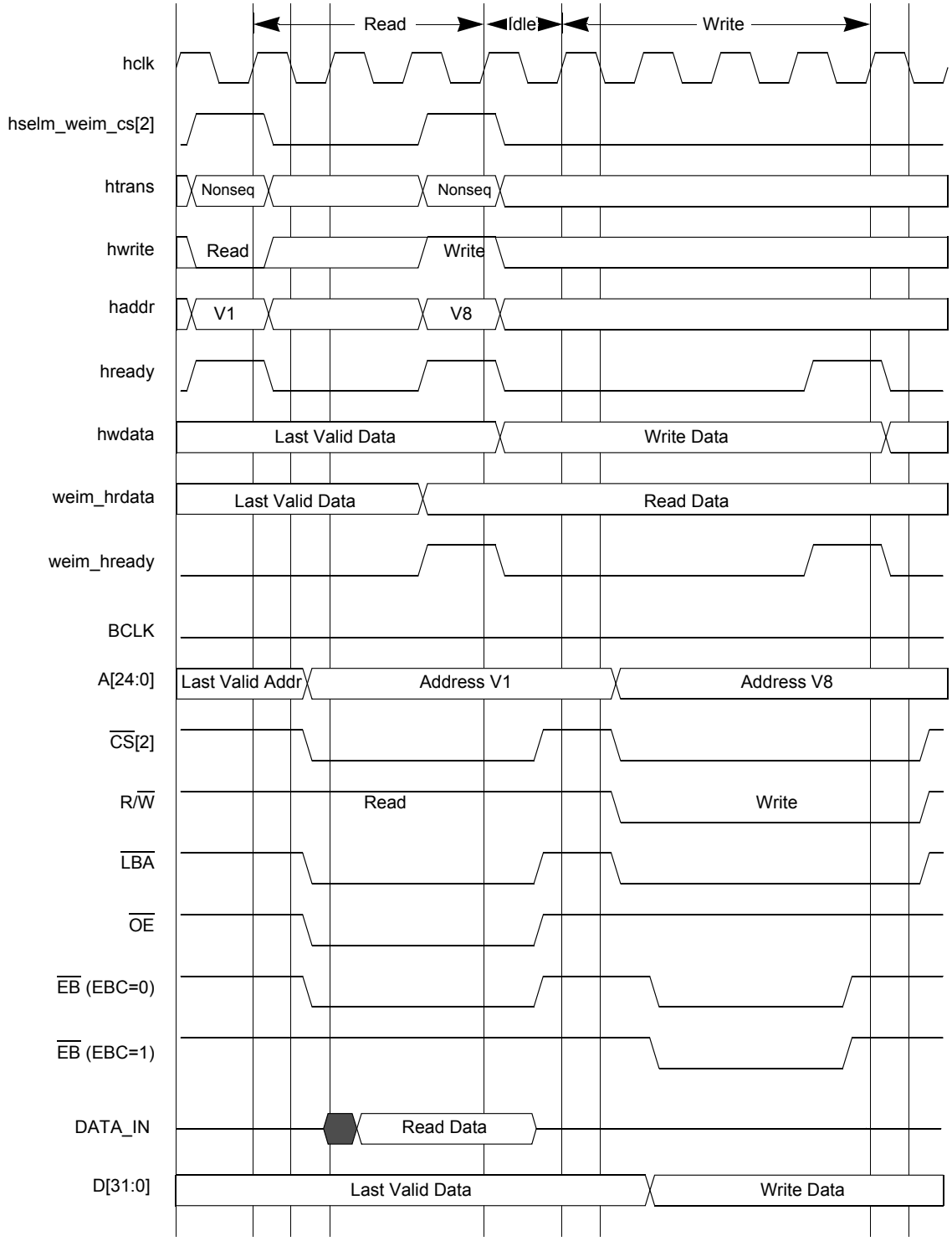



**Figure 67. WSC = 2, WWS = 1, WEA = 1, WEN = 2, EDC = 1, A.HALF/E.HALF**

Note: Signals listed with lower case letters are internal to the device.

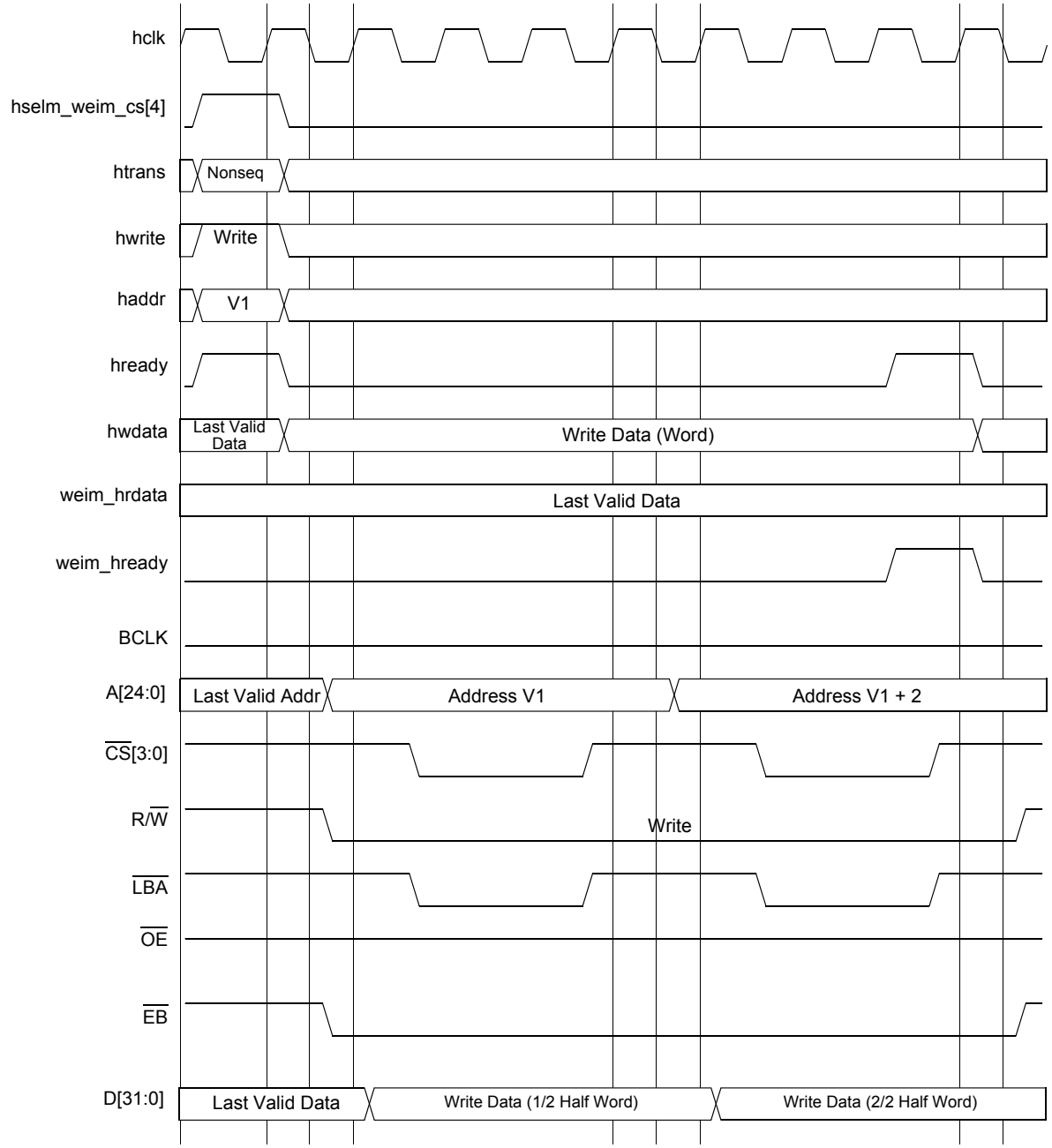



**Figure 68. WSC = 2, CSA = 1, WWS = 1, A.WORD/E.HALF**

Note: Signals listed with lower case letters are internal to the device.

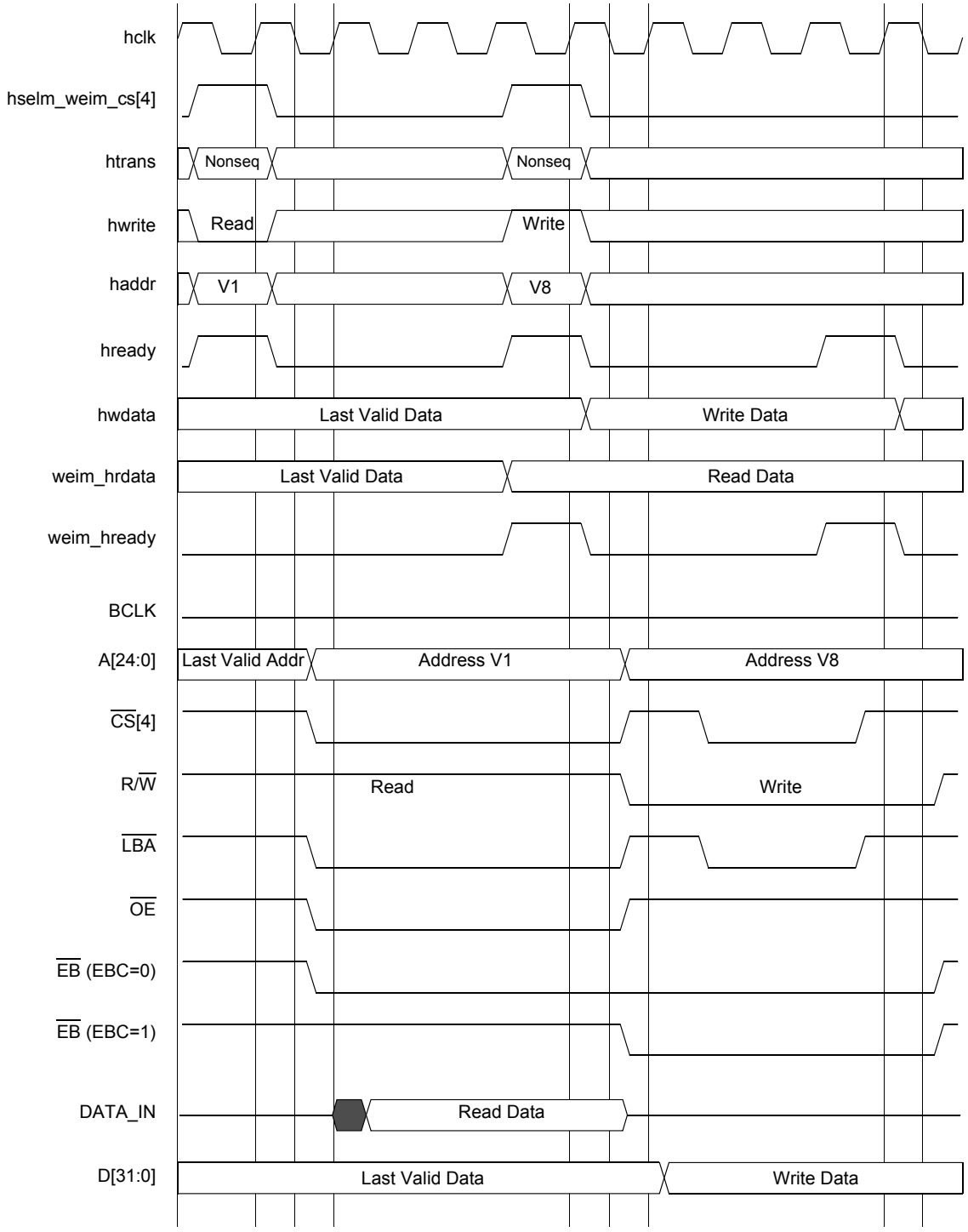



**Figure 69. WSC = 3, CSA = 1, A.HALF/E.HALF**

Note: Signals listed with lower case letters are internal to the device.

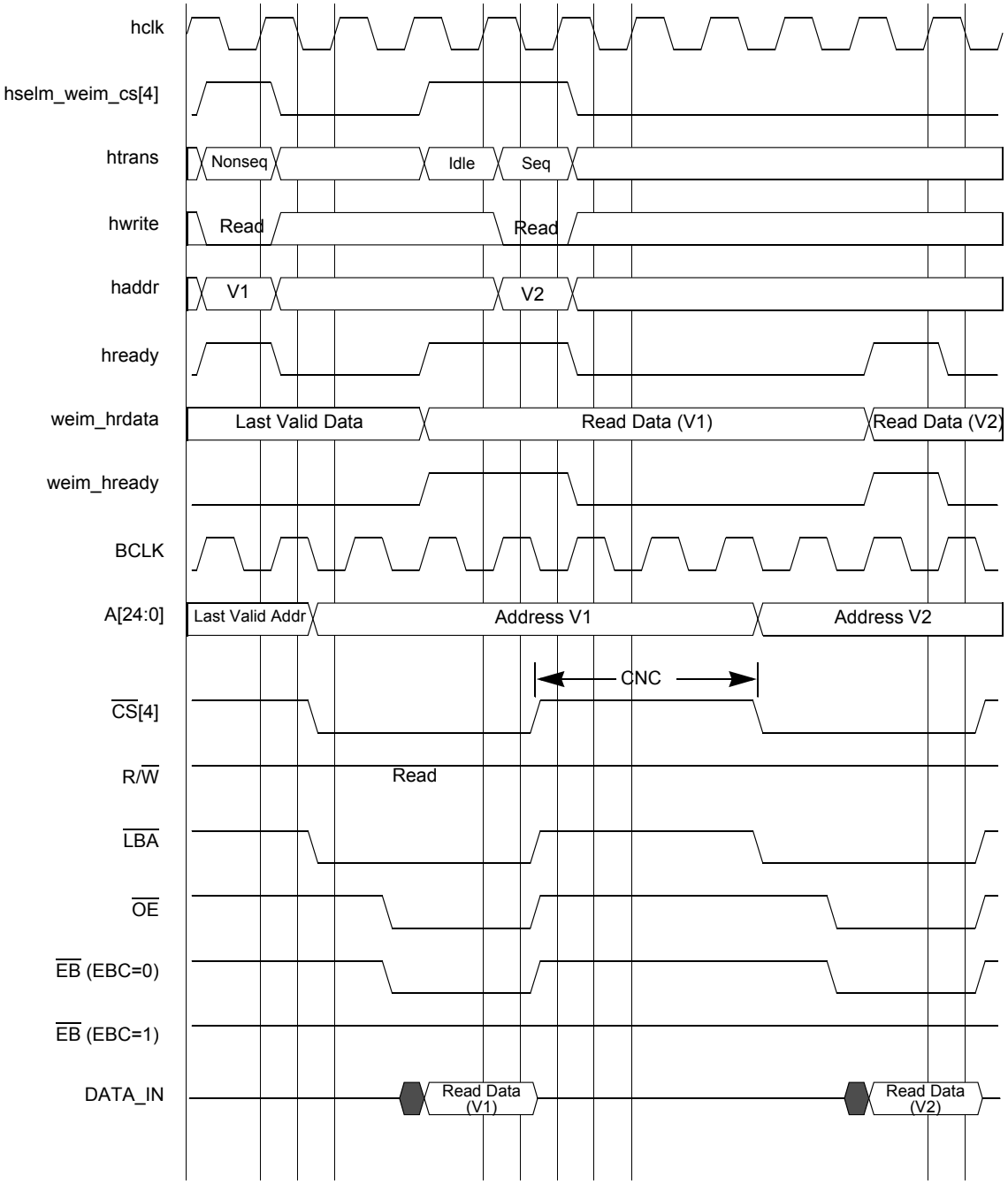



**Figure 70. WSC = 2, OEA = 2, CNC = 3, BCM = 1, A.HALF/E.HALF**

Note: Signals listed with lower case letters are internal to the device.

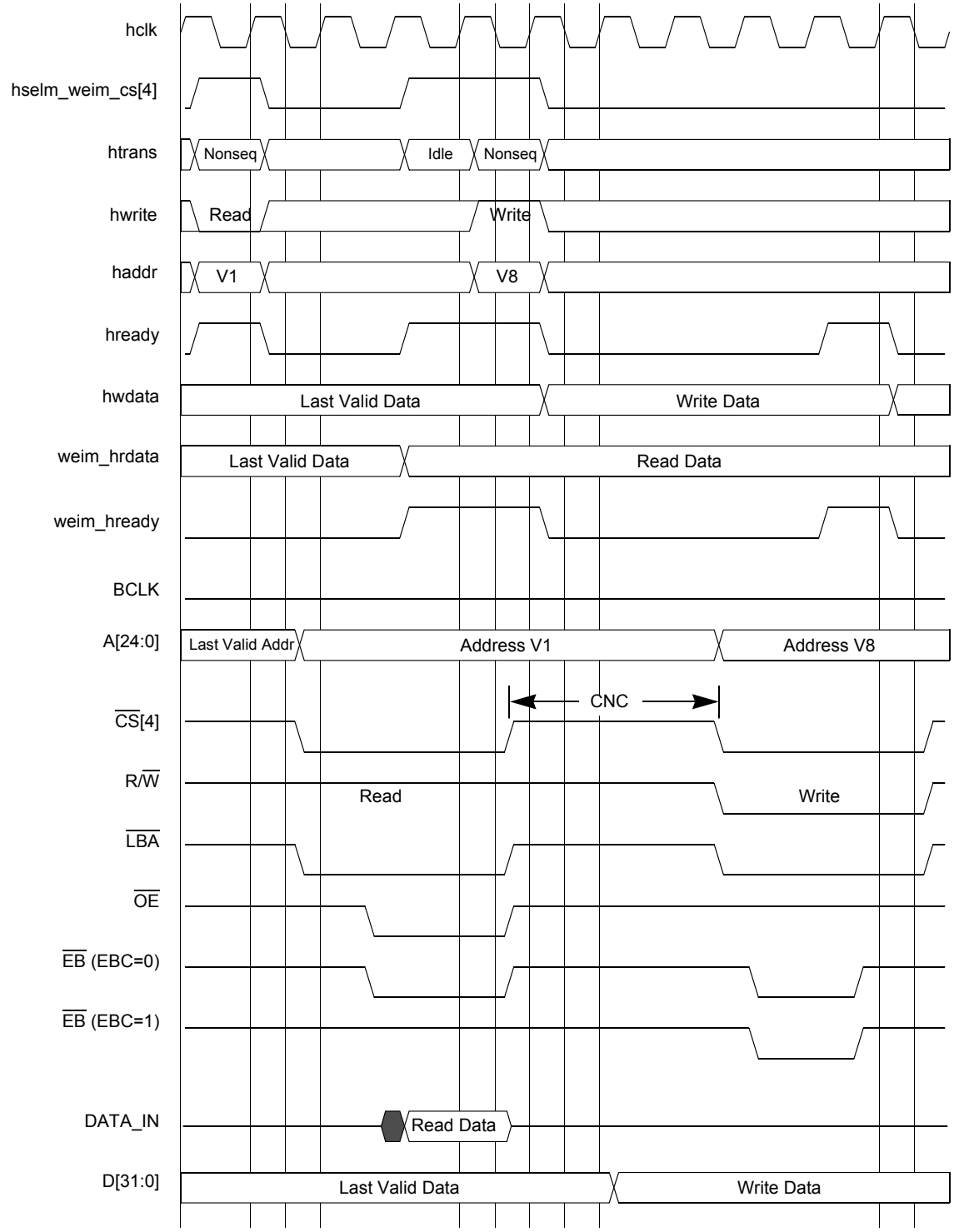



**Figure 71. WSC = 2, OEA = 2, WEA = 1, WEN = 2, CNC = 3, A.HALF/E.HALF**

Note: Signals listed with lower case letters are internal to the device.

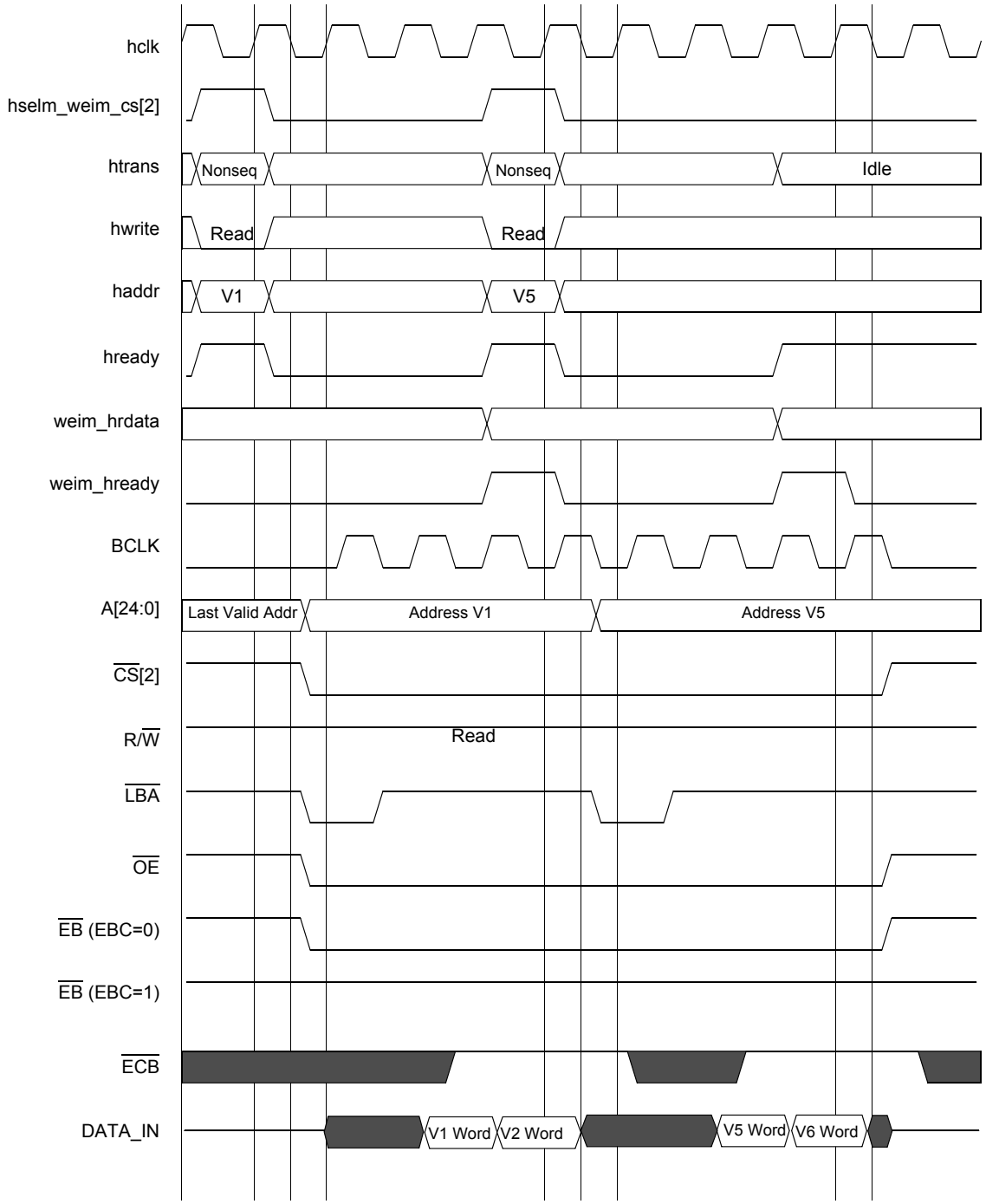



**Figure 72. WSC = 3, SYNC = 1, A.HALF/E.HALF**

Note: Signals listed with lower case letters are internal to the device.

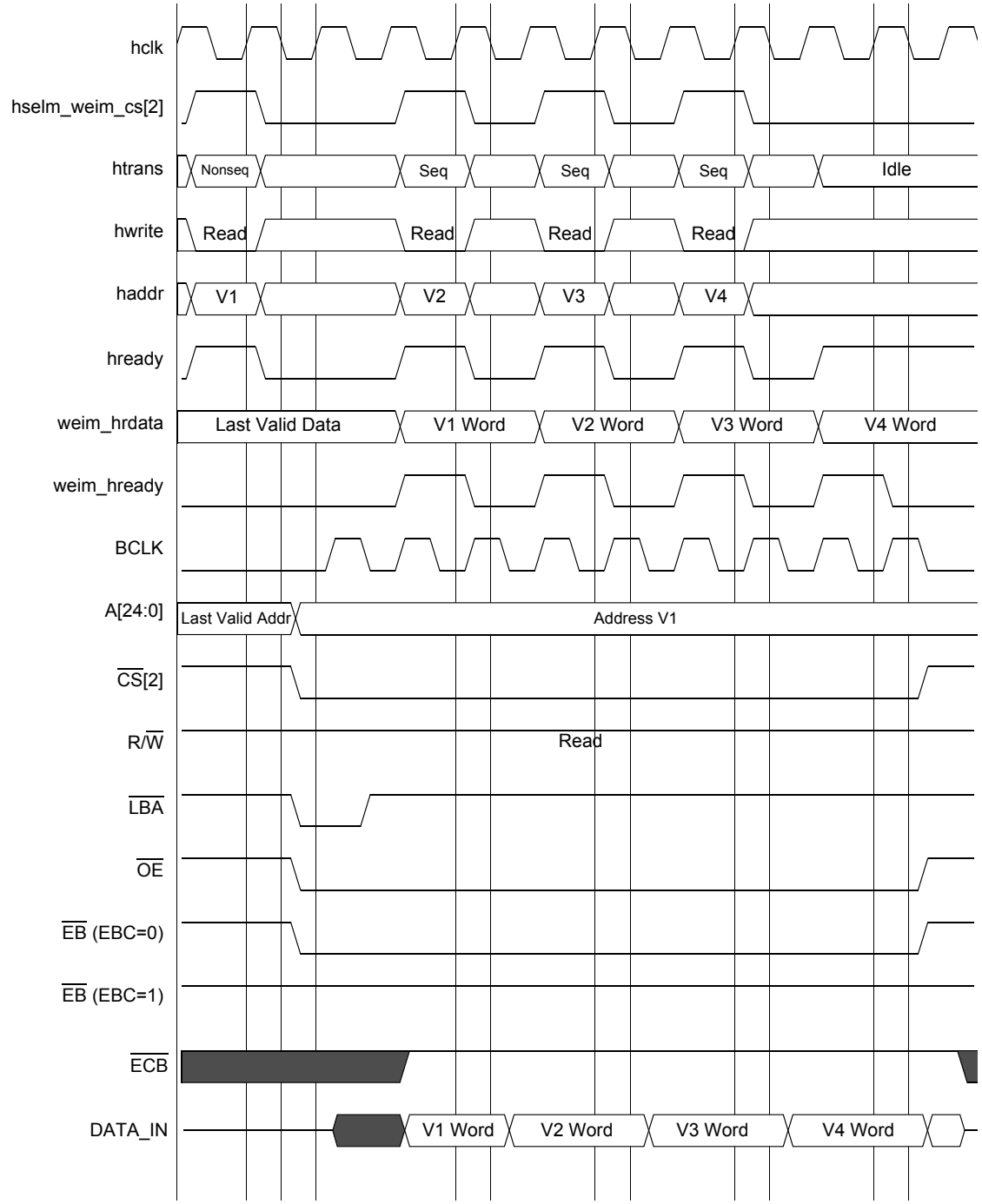



**Figure 73. WSC = 2, SYNC = 1, DOL = [1/0], A.WORD/E.WORD**

Note: Signals listed with lower case letters are internal to the device.

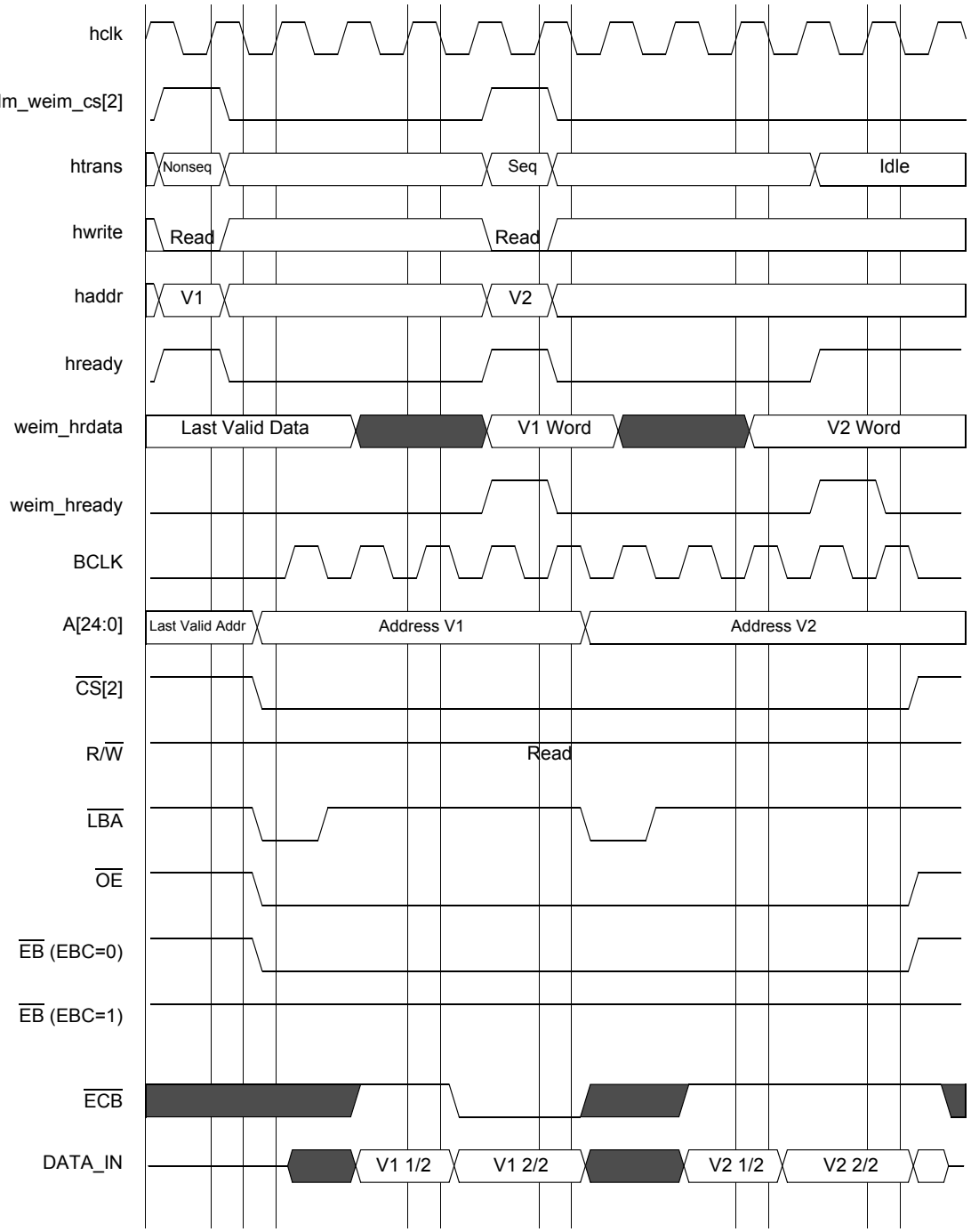



**Figure 74. WSC = 2, SYNC = 1, DOL = [1/0], A.WORD/E.HALF**

Note: Signals listed with lower case letters are internal to the device.

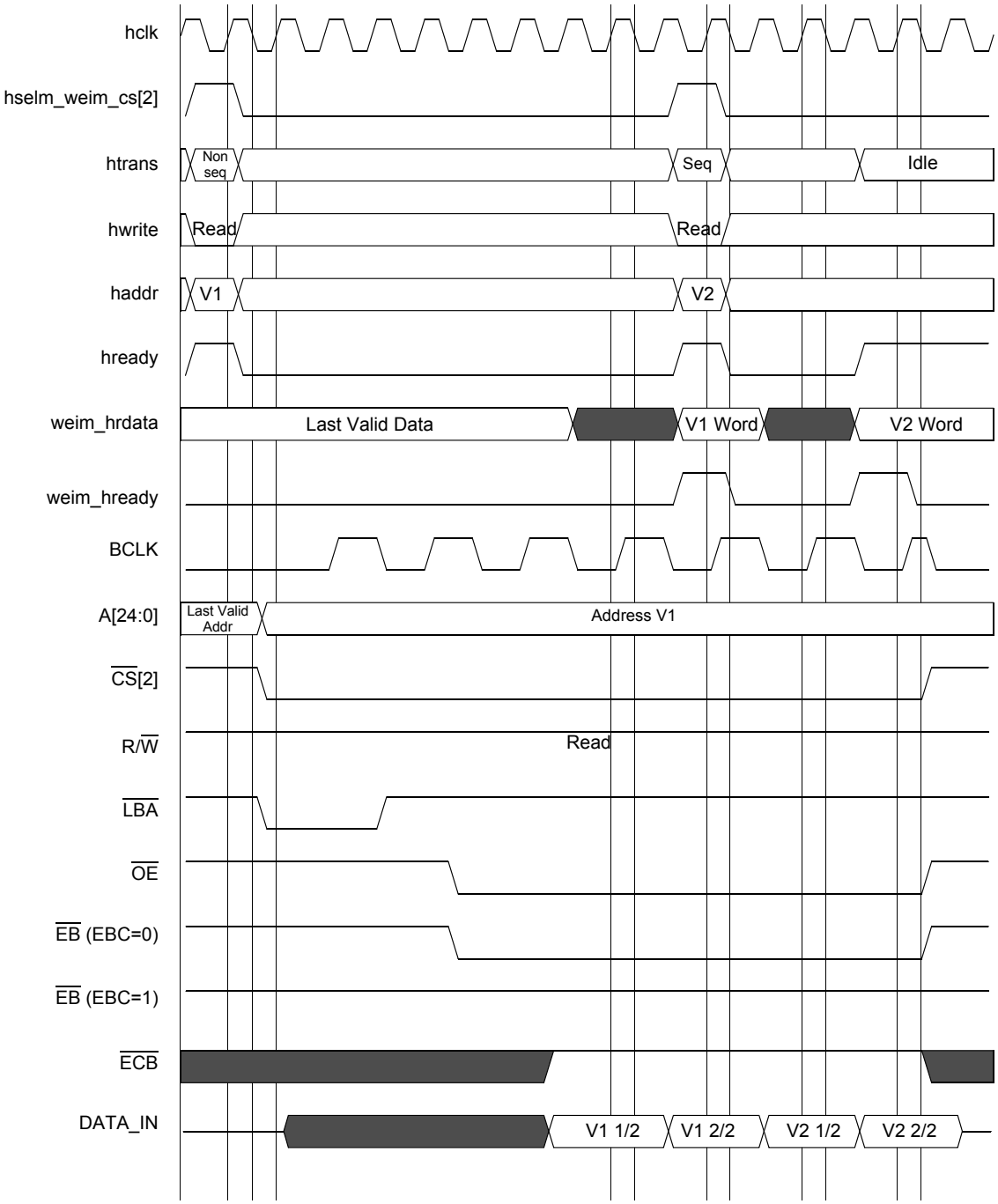



**Figure 75. WSC = 7, OEA = 8, SYNC = 1, DOL = 1, BCD = 1, BCS = 2, A.WORD/E.HALF**

Note: Signals listed with lower case letters are internal to the device.

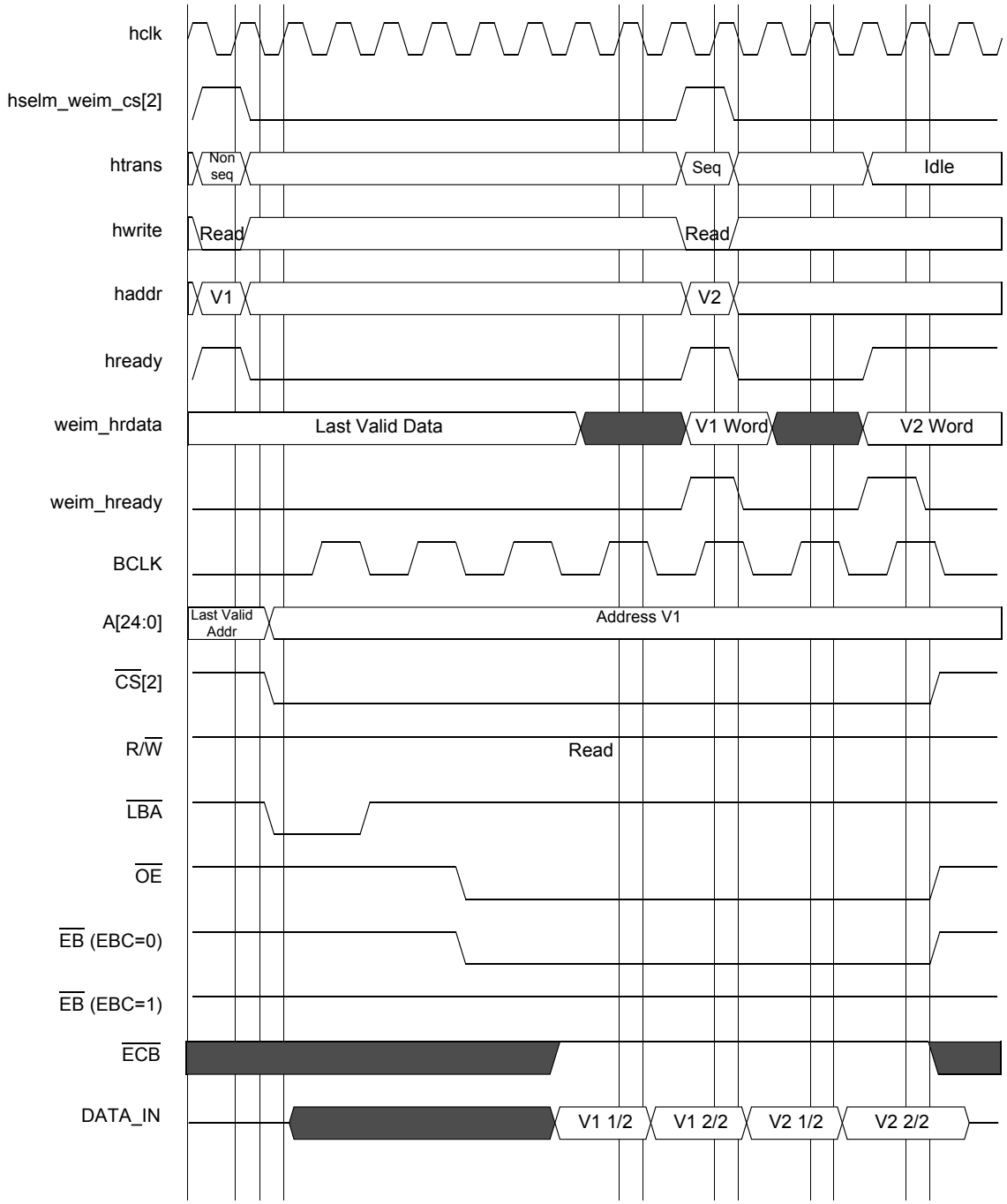



**Figure 76. WSC = 7, OEA = 8, SYNC = 1, DOL = 1, BCD = 1, BCS = 1, A.WORD/E.HALF**

## 3.20 DTACK Mode Memory Access Timing Diagrams

When enabled, the DTACK input signal is used to externally terminate a data transfer. For DTACK enabled operations, a bus time-out monitor generates a bus error when an external bus cycle is not terminated by the DTACK input signal after 1024 HCLK clock cycles have elapsed, where HCLK is the internal system clock driven from the PLL module. For a 133 MHz HCLK setting, this time equates to 7.7 µs. Refer to the Section 3.5, "DPLL Timing Specifications" for more information on how to generate different HCLK frequencies.

There are two modes of operation for the DTACK input signal: rising edge detection or level sensitive detection with a programmable insensitivity time. DTACK is only used during external asynchronous data transfers, thus the SYNC bit in the chip select control registers must be cleared.

During edge detection mode, the EIM will terminate an external data transfer following the detection of the DTACK signal's rising edge, so long as it occurs within the 1024 HCLK cycle time. Edge detection mode is used for devices that follow the PCMCIA standard. Note that DTACK rising edge detection mode can only be used for $\overline{CS}$[5] operations. To configure $\overline{CS}$[5] for DTACK rising edge detection, the following bits must be programmed in the Chip Select 5 Control Register and EIM Configuration Register:

- WSC bit field set to 0x3F and CSA (or CSN) set to 1 or greater in the Chip Select 5 Control Register
- AGE bit set in the EIM Configuration Register

Other bits such as DSZ, OEA, OEN, and so on, may be set according to system and timing requirements of the external device. The requirement of setting CSA or CSN is required to allow the EIM to wait for the rising edge of DTACK during back-to-back external transfers, such as during DMA transfers or an internal 32-bit access through an external 16-bit data port.

During level sensitive detection, the EIM will first hold off sampling the DTACK signal for at least 2 HCLK cycles, and up to 5 HCLK cycles as programmed by the DCT bits in the Chip Select Control Register. After this insensitivity time, the EIM will sample DTACK and if it detects that DTACK is logic high, it will continue the data transfer at the programmed number of wait states. However, if the EIM detects that DTACK is logic low, it will wait until DTACK goes to logic high to continue the access, so long as this occurs within the 1024 HCLK cycle time. If at anytime during an external data transfer DTACK goes to logic low, the EIM will wait until DTACK returns to logic high to resume the data transfer. Level detection is often used for asynchronous devices such graphic controller chips. Level detection may be used with any chip select except CS[4] as it is multiplexed with the DTACK signal. To configure a chip select for DTACK level sensitive detection, the following bits must be programmed in the Chip Select Control Register and EIM Configuration Register:

- EW bit set, WSC set to > 1, and CSN set to < 3 in the Chip Select Control Register
- BCD/DCT set to desired "insensitivity time" in the Chip Select Control Register. The "insensitivity time" is dictated by the external device's timing requirements.
- AGE bit cleared in the EIM Configuration Register

Other bits such as DSZ, OEA, OEN, and so on, may be set according to system and timing requirements of the external device.

The waveforms in the following section provide examples of the DTACK signal operation.

### 3.20.1 DTACK Example Waveforms: Internal ARM AHB Word Accesses to Word-Width (32-bit) Memory

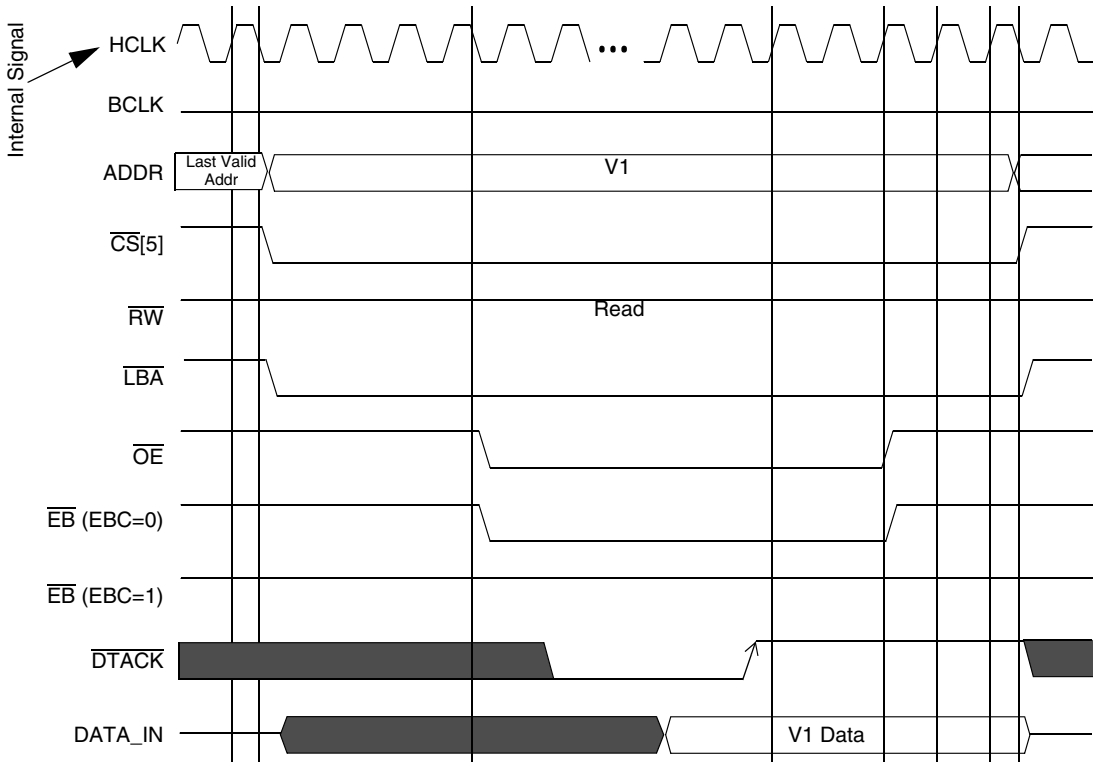



**Figure 77. DTACK Edge Triggered Read Access, WSC=3F, OEA=8, OEN=5, AGE=1.**

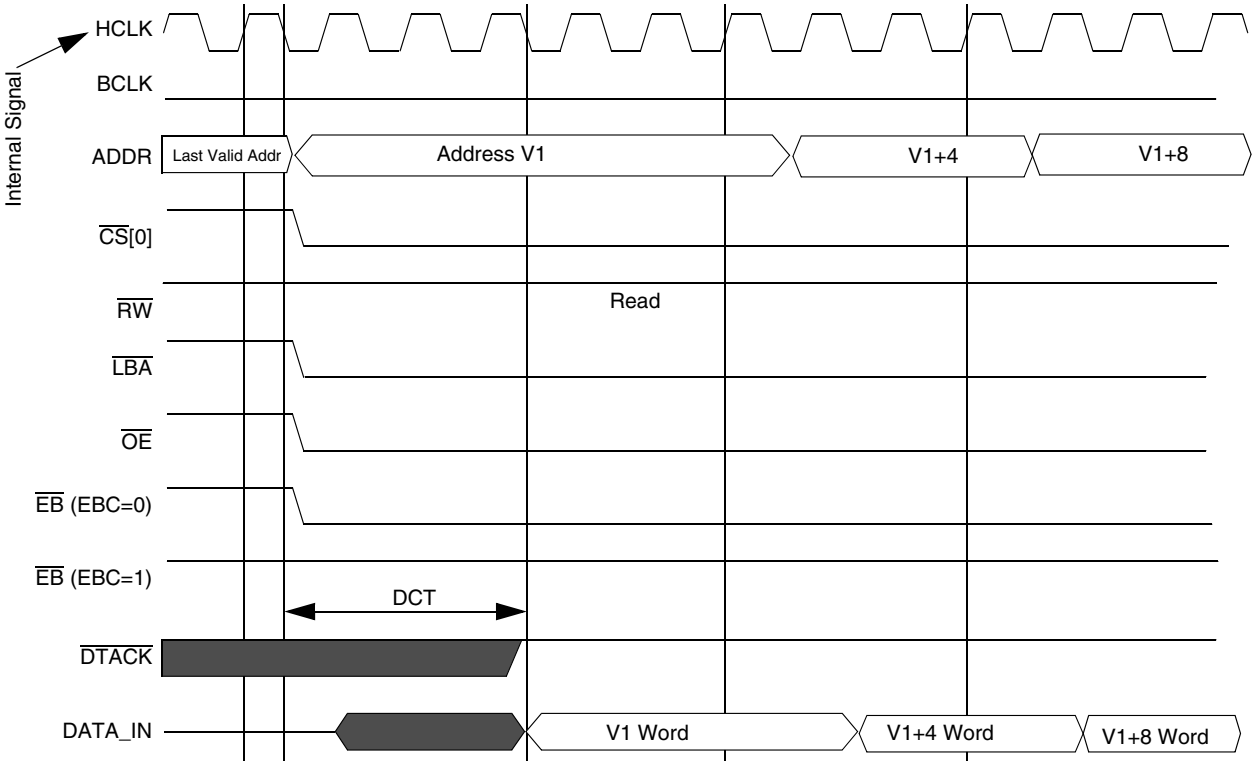



**Figure 78. DTACK Level Sensitive Sequential Read Accesses, WSC=2, EW=1, DCT=1, AGE=0 (Example of DTACK Remaining High)**

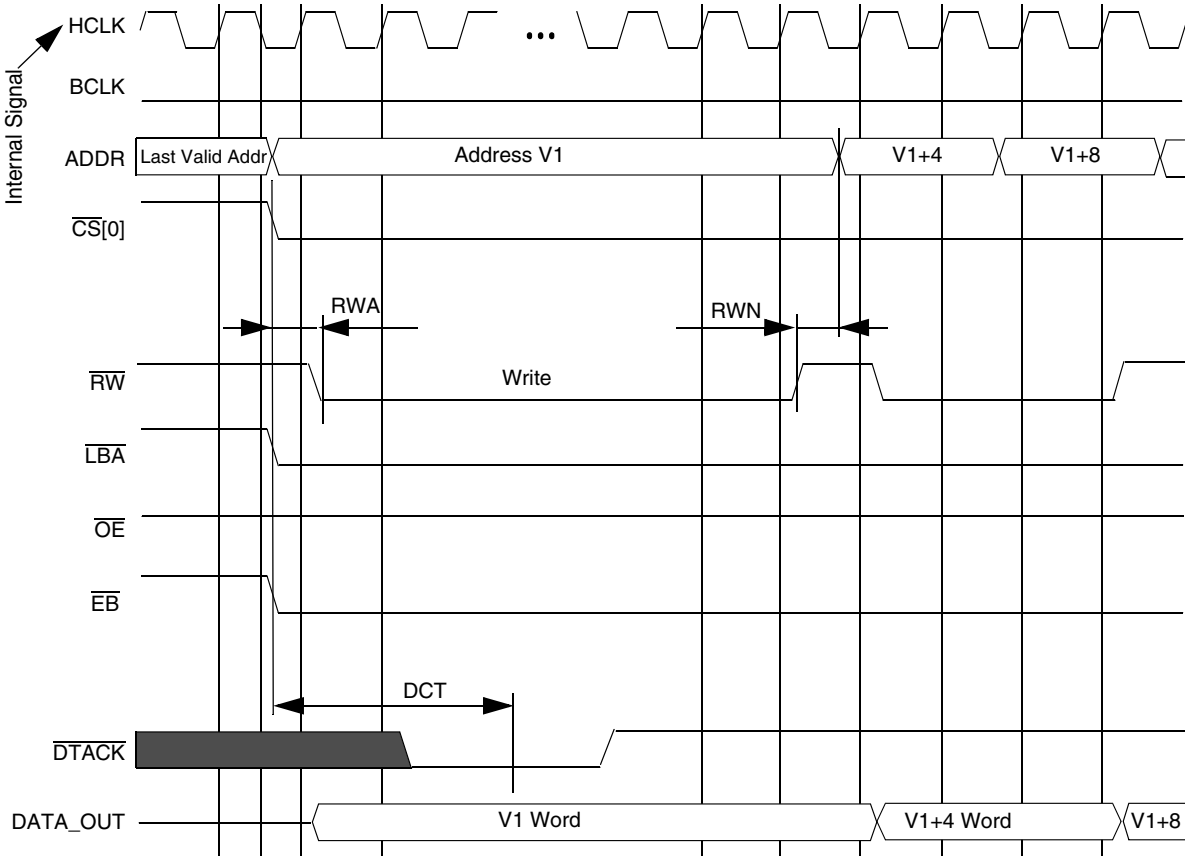



**Figure 79. DTACK Level Sensitive Sequential Write Accesses, WSC=2, EW=1, RWA=1, RWN=1, DCT=1, AGE=0 (Example of DTACK Asserting)**

## 3.21 I²C Module

The I²C communication protocol consists of seven elements: START, Data Source/Recipient, Data Direction, Slave Acknowledge, Data, Data Acknowledge, and STOP.

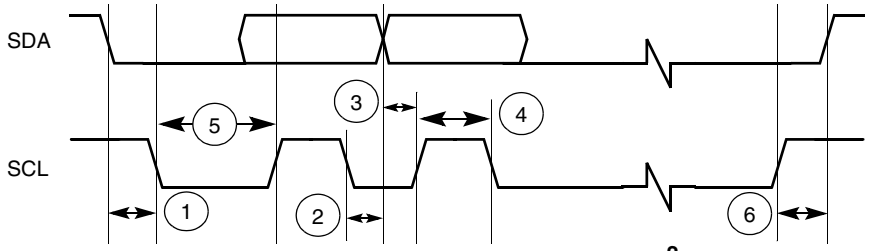



**Figure 80. Definition of Bus Timing for I²C**

**Table 43. I²C Bus Timing Parameters**

| Ref No. | Parameter | 1.8 V ± 0.1 V | | 3.0 V ± 0.3 V | | Unit |
|---|---|---|---|---|---|---|
| | | Minimum | Maximum | Minimum | Maximum | |
| | SCL Clock Frequency | 0 | 100 | 0 | 100 | kHz |
| 1 | Hold time (repeated) START condition | 114.8 | – | 111.1 | – | ns |
| 2 | Data hold time | 0 | 69.7 | 0 | 72.3 | ns |
| 3 | Data setup time | 3.1 | – | 1.76 | – | ns |
| 4 | HIGH period of the SCL clock | 69.7 | – | 68.3 | – | ns |
| 5 | LOW period of the SCL clock | 336.4 | – | 335.1 | – | ns |
| 6 | Setup time for STOP condition | 110.5 | – | 111.1 | – | ns |

## 3.22 CMOS Sensor Interface

The CSI module consists of a control register to configure the interface timing, a control register for statistic data generation, a status register, interface logic, a 32 × 32 image data receive FIFO, and a 16 × 32 statistic data FIFO.

### 3.22.1 Gated Clock Mode

Figure 81 shows the timing diagram when the CMOS sensor output data is configured for negative edge and the CSI is programmed to received data on the positive edge. Figure 82 shows the timing diagram when the CMOS sensor output data is configured for positive edge and the CSI is programmed to received data in negative edge. The parameters for the timing diagrams are listed in Table 44. The formula for calculating the pixel clock rise and fall time is located in Section 3.22.3, "Calculation of Pixel Clock Rise/Fall Time."

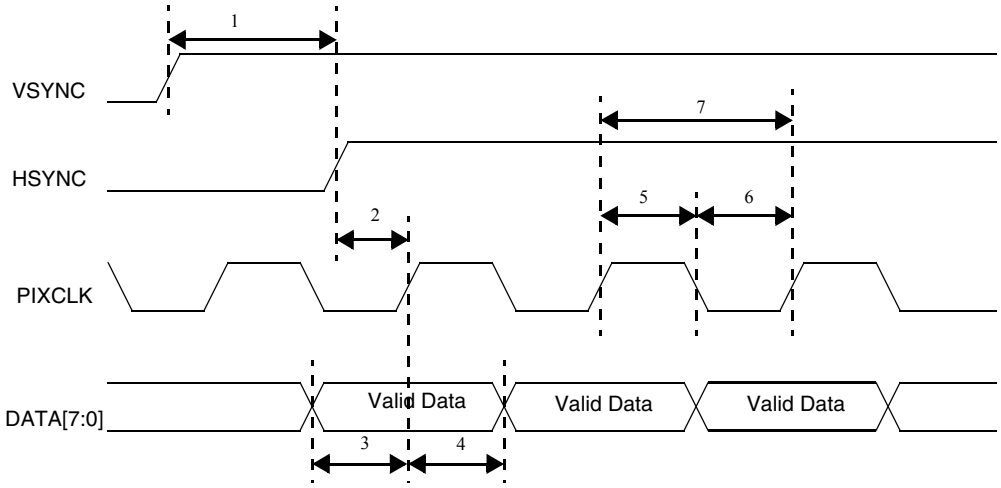



**Figure 81. Sensor Output Data on Pixel Clock Falling Edge CSI Latches Data on Pixel Clock Rising Edge**

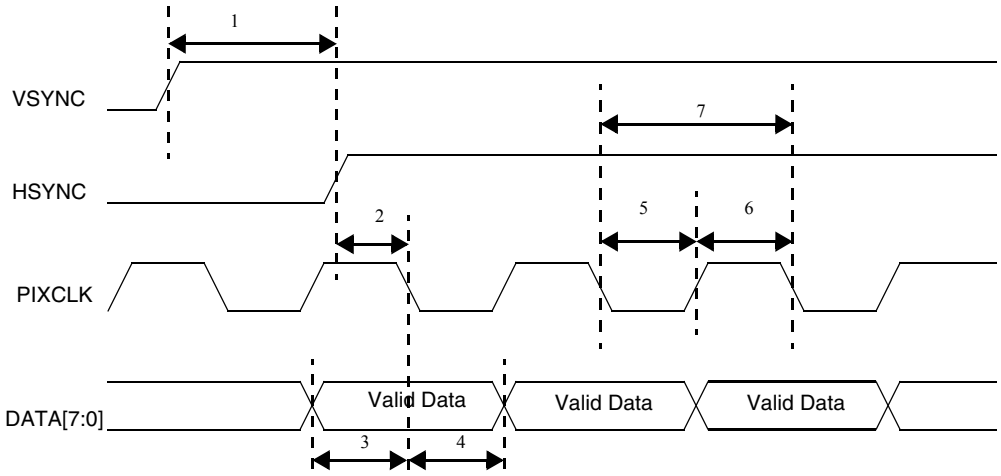



**Figure 82. Sensor Output Data on Pixel Clock Rising Edge CSI Latches Data on Pixel Clock Falling Edge**

**Table 44. Gated Clock Mode Timing Parameters**

| Number | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| 1 | csi_vsync to csi_hsync | 9 * $T_{HCLK}$ | – | ns |
| 2 | csi_hsync to csi_pixclk | 3 | ($T_P$/2) - 3 | ns |
| 3 | csi_d setup time | 1 | – | ns |
| 4 | csi_d hold time | 1 | – | ns |
| 5 | csi_pixclk high time | $T_{HCLK}$ | – | ns |
| 6 | csi_pixclk low time | $T_{HCLK}$ | – | ns |
| 7 | csi_pixclk frequency | 0 | HCLK / 2 | MHz |

HCLK = AHB System Clock, $T_{HCLK}$ = Period for HCLK, $T_P$ = Period of CSI_PIXCLK

The limitation on pixel clock rise time/fall time is not specified. It should be calculated from the hold time and setup time based on the following assumptions:

Rising-edge latch data

max rise time allowed = (positive duty cycle - hold time)
max fall time allowed = (negative duty cycle - setup time)

In most of case, duty cycle is 50 / 50, therefore

max rise time = (period / 2 - hold time)
max fall time = (period / 2 - setup time)

For example: Given pixel clock period = 10ns, duty cycle = 50 / 50, hold time = 1ns, setup time = 1ns.

positive duty cycle = 10 / 2 = 5ns
≥ max rise time allowed = 5 - 1 = 4ns

negative duty cycle = 10 / 2 = 5ns
≥ max fall time allowed = 5 - 1 = 4ns

Falling-edge latch data

max fall time allowed = (negative duty cycle - hold time)
max rise time allowed = (positive duty cycle - setup time)

## 3.22.2 Non-Gated Clock Mode

Figure 83 shows the timing diagram when the CMOS sensor output data is configured for negative edge and the CSI is programmed to received data on the positive edge. Figure 84 shows the timing diagram when the CMOS sensor output data is configured for positive edge and the CSI is programmed to received data in negative edge. The parameters for the timing diagrams are listed in Table 45. The formula for calculating the pixel clock rise and fall time is located in Section 3.22.3, "Calculation of Pixel Clock Rise/ Fall Time."

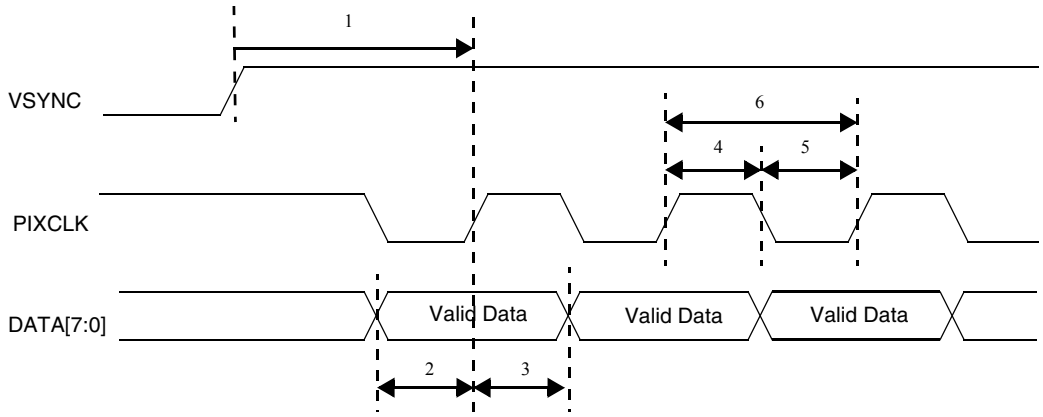



**Figure 83. Sensor Output Data on Pixel Clock Falling Edge**
**CSI Latches Data on Pixel Clock Rising Edge**

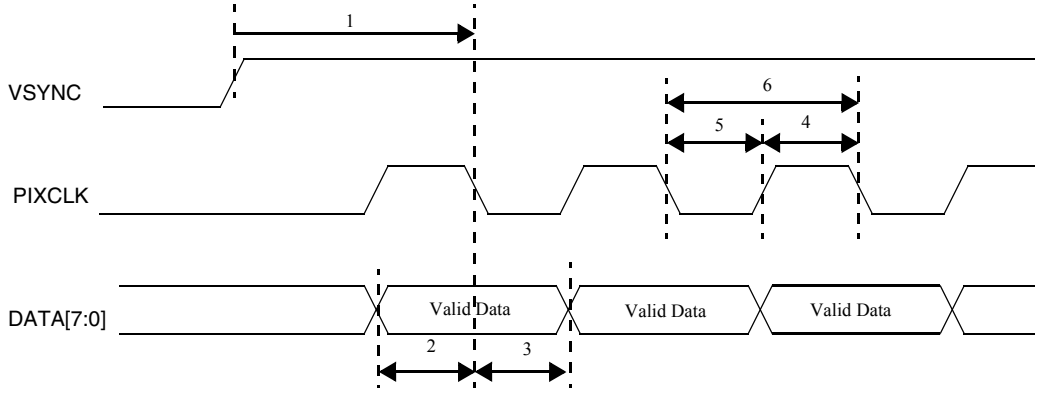



**Figure 84. Sensor Output Data on Pixel Clock Rising Edge**
**CSI Latches Data on Pixel Clock Falling Edge**

**Table 45. Non-Gated Clock Mode Parameters[1]**

| Number | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| 1 | csi_vsync to csi_pixclk | 9 * $T_{HCLK}$ | – | ns |
| 2 | csi_d setup time | 1 | – | ns |
| 3 | csi_d hold time | 1 | – | ns |
| 4 | csi_pixclk high time | $T_{HCLK}$ | – | ns |
| 5 | csi_pixclk low time | $T_{HCLK}$ | – | ns |
| 6 | csi_pixclk frequency | 0 | HCLK / 2 | MHz |

1. HCLK = AHB System Clock, $T_{HCLK}$ = Period of HCLK

## 3.22.3 Calculation of Pixel Clock Rise/Fall Time

The limitation on pixel clock rise time/fall time is not specified. It should be calculated from the hold time and setup time based on the following assumptions:

Rising-edge latch data

- max rise time allowed = (positive duty cycle - hold time)
- max fall time allowed = (negative duty cycle - setup time)

In most of case, duty cycle is 50 / 50, therefore:

- max rise time = (period / 2 - hold time)
- max fall time = (period / 2 - setup time)

For example: Given pixel clock period = 10ns, duty cycle = 50 / 50, hold time = 1ns, setup time = 1ns.

positive duty cycle = 10 / 2 = 5ns
≥ max rise time allowed = 5 - 1 = 4ns
negative duty cycle = 10 / 2 = 5ns
≥ max fall time allowed = 5 - 1 = 4ns

Falling-edge latch data

- max fall time allowed = (negative duty cycle - hold time)
- max rise time allowed = (positive duty cycle - setup time)

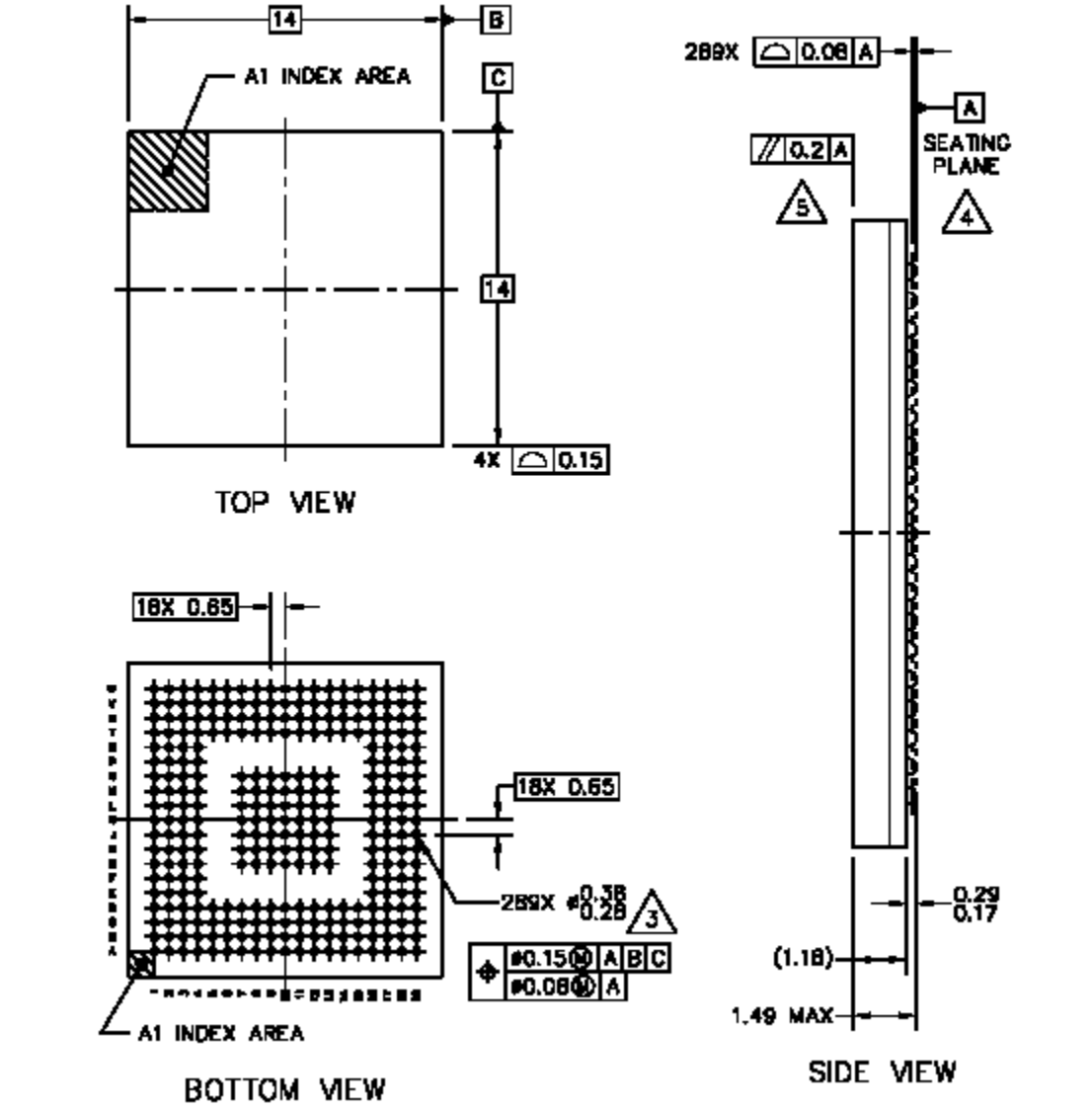
# 4 Pin Assignment and Package Information

**Table 46. i.MX21 Pin Assignment**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | LD9 | LD12 | LD14 | REV | HSYNC | OE_ ACD | SD2_D2 | CSI_ D0 | CSI_ PIXCLK | CSI_ VSYNC | USBH1_ FS | USBH1_ OE | USBG_ FS | TOUT | SAP_ TXDAT | SSI1_ CLK |
| B | LD7 | LD5 | LD11 | LD16 | PS | CON TRAST | SD2_D0 | SD2_ CMD | CSI_ D4 | CSI_D6 | USB_ PWR | USBG_ SCL | USBG_ TXDM | SAP_ FS | SSI1_ FS | SSI2_ FS |
| C | LD1 | LD3 | LD6 | LD10 | LD17 | VSYNC | SD2_D3 | CSI_ D1 | CSI_ MCLK | CSI_ HSYNC | USB_ OC | USBH1_ RXDM | USBG_ RXDM | TIN | SSI1_ TXDAT | SSI3_ RXDAT |
| D | LD2 | LD0 | LD13 | CLS | QVDD | QVSS | SD2_D1 | SD2_ CLK | CSI_ D2 | CSI_D7 | USBH1_ TXDM | USBH1_ RXDP | USBG_ ON | USBG_ RXDP | SAP_ RXDAT | SSI1_ RXDAT |
| E | LD8 | LD4 | LD15 | SPL_ SPR | | | | | | | | | | | | SAP_ CLK |
| F | A24_ NFIO14 | D31 | A25_ NFIO15 | LSCLK | | | | | | | | | | | | CSPI1_ SS1 |
| G | A22_ NFIO12 | D29 | A23_ NFIO13 | D30 | | | NVDD6 | NVSS6 | CSI_D3 | USB_ BYP | USBH_ ON | USBG_ SDA | USBG_ TXDP | | | KP_ ROW1 |
| H | A20 | D27 | A21_ NFIO11 | D28 | | | NVDD1 | NVSS5 | CSI_D5 | CSPI1_ SCLK | CSPI1_ RDY | USBH1_ TXDP | USBG_ OE | | | TEST_ WB4 |
| J | A19 | A18 | D25 | D26 | | | NVDD1 | NVDD5 | NVDD4 | KP_ ROW5 | KP_ ROW2 | CSPI1_ MOSI | TEST_ WB0 | | | UART2_ RTS |
| K | A16 | A17 | D23 | D24 | | | NVSS1 | NVSS4 | QVDDX | UART1_ RXD | TDO | QVDD | QVSS | | | KP_ COL3 |
| L | A14_ NFIO9 | A15_ NFIO10 | D21 | D22 | | | NVSS1 | NVDD3 | QVDD | QVSS | NFIO2 | NFWP | UART1_ TXD | | | UART2_ TXD |
| M | D19 | A13_ NFIO8 | D20 | D18 | | | NVDD2 | NVDD3 | NVSS3 | QVSS | NFIO7 | NFRB | EXT_ 48M | | | UART2_ RXD |
| N | A11 | A12 | D17 | D16 | | | LBA | NVSS3 | SDCKE0 | NVSS1 | NVSS1 | NVDD1 | NVDD1 | | | SD1_ D0 |
| P | A9 | A10 | D15 | D14 | | | | | | | | | | | | SD1_ D2 |
| R | A7 | A8 | D13 | D12 | | | | | | | | | | | | SD1_ CLK |
| T | A5 | A6 | EB3 | D10 | CS3 | CS1 | BCLK | MA11 | RAS | CAS | NFIO5 | NFIO3 | NFWE | RESET_ IN | NFCE | BOOT1 |
| U | D11 | EB1 | EB2 | OE | CS4 | D6 | ECB | D3 | MA10 | PC_ PWRON | PF16 | NFIO4 | NFIO1 | NFALE | NFCLE | POR |
| V | A4 | EB0 | D9 | D8 | CS5 | D5 | CS0 | RW | D1 | JTAG_ CTRL | SDWE | CLKO | NFIO6 | QVSS | RESET_ OUT | BOOT0 |
| W | A3 | A2 | D7 | A1 | CS2 | A0 | D4 | D2 | D0 | SDCLK | SDCKE1 | NFIO0 | NFRE | QVDD | QVSS | EXTAL 26M |

## 4.1 MAPBGA Package Dimensions

Figure 85 illustrates the MAPBGA 14 mm × 14 mm × 1.41 mm package, which has 0.65 mm ball pitch.




NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

**Figure 85. i.MX21 MAPBGA Mechanical Drawing**

# 5 Document Revision History

Rev 1.4 is the initial public release of this document.

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