



**THE DATASHEET OF
MC74VHC1G66DTT1G**



MC74VHC1G66

SPST (NO) Normally Open Analog Switch

The MC74VHC1G66 is a single pole single throw (SPST) analog switch. It achieves high speed propagation delays and low ON resistances while maintaining low power dissipation. This bilateral switch controls analog and digital voltages that may vary across the full power-supply range (from V_{CC} to GND).

The MC74VHC1G66 is compatible in function to a single gate of the High Speed CMOS MC74VHC4066 and the metal-gate CMOS MC14066. The device has been designed so that the ON resistances (R_{ON}) are much lower and more linear over input voltage than R_{ON} of the metal-gate CMOS or High Speed CMOS analog switches.

The ON/OFF control inputs are compatible with standard CMOS outputs. The ON/OFF control input structure provides protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. This input structure helps prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

Features

- High Speed: $t_{PD} = 20$ ns (Typ) at $V_{CC} = 5.0$ V
- Low Power Dissipation: $I_{CC} = 1.0$ μ A (Max) at $T_A = 25^\circ$ C
- Diode Protection Provided on Inputs and Outputs
- Improved Linearity and Lower ON Resistance over Input Voltage
- Chip Complexity: 11 FETs or 3 Equivalent Gates
- ON/OFF Control Input has OVT
- Chip Complexity: FETs = 11
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



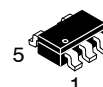
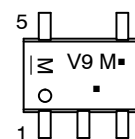
ON Semiconductor®

www.onsemi.com

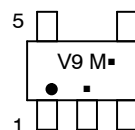
MARKING DIAGRAMS



SC-88A
DF SUFFIX
CASE 419A



TSOP-5
DT SUFFIX
CASE 483



V9 = Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

PIN ASSIGNMENT

| | |
|---|----------------|
| 1 | IN/OUT X_A |
| 2 | OUT/IN Y_A |
| 3 | GND |
| 4 | ON/OFF CONTROL |
| 5 | V_{CC} |

FUNCTION TABLE

| On/Off Control Input | State of Analog Switch |
|----------------------|------------------------|
| L | Off |
| H | On |

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

MC74VHC1G66

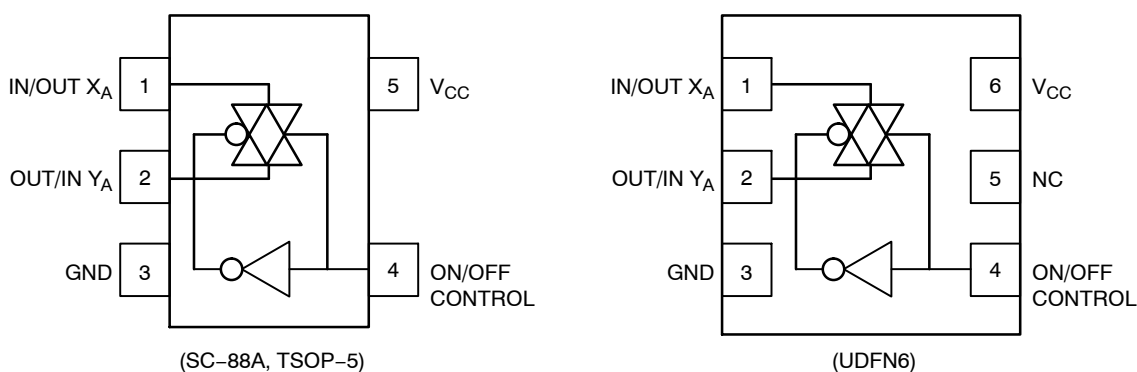


Figure 1. Pinout Diagrams

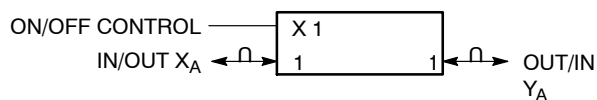


Figure 2. Logic Symbol

MAXIMUM RATINGS

| Symbol | Characteristics | Value | Unit |
|---------------|---|--|------|
| V_{CC} | DC Supply Voltage | -0.5 to +7.0 | V |
| V_{IN} | Digital Input Voltage | -0.5 to +7.0 | V |
| V_{IS} | Analog Output Voltage | -0.5 to $V_{CC} + 0.5$ | V |
| I_{IK} | Digital Input Diode Current | -20 | mA |
| I_{CC} | DC Supply Current, V_{CC} and GND | +25 | mA |
| T_{STG} | Storage Temperature Range | -65 to +150 | °C |
| T_L | Lead Temperature, 1 mm from Case for 10 Seconds | 260 | °C |
| T_J | Junction Temperature Under Bias | +150 | °C |
| θ_{JA} | Thermal Resistance | SC70-5 (Note 1) SOT23-5 350 230 | °C/W |
| P_D | Power Dissipation in Still Air at 85°C | SC70-5 SOT23-5 150 200 | mW |
| MSL | Moisture Sensitivity | Level 1 | |
| F_R | Flammability Rating | Oxygen Index: 28 to 34 UL 94 V-0 @ 0.125 in | |
| V_{ESD} | ESD Withstand Voltage | Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4) > 2000 > 200 N/A | V |
| $I_{LATCHUP}$ | Latchup Performance | Above V_{CC} and Below GND at 125°C (Note 5) ± 500 | mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2-ounce copper trace with no air flow.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA/JESD78.

MC74VHC1G66

RECOMMENDED OPERATING CONDITIONS

| Symbol | Characteristics | Min | Max | Unit |
|---------------------------------|--|--|-----------------|------|
| V _{CC} | DC Supply Voltage | 2.0 | 5.5 | V |
| V _{IN} | DC Input Voltage | GND | 5.5 | V |
| V _{IS} | DC Output Voltage | GND | V _{CC} | V |
| T _A | Operating Temperature Range | -55 | +125 | °C |
| t _r , t _f | Input Rise and Fall Time ON/OFF Control Input | V _{CC} = 3.3 V ± 0.3 V 0 V _{CC} = 5.0 V ± 0.5 V 0 | 100 20 | ns/V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Device Junction Temperature versus Time to 0.1% Bond Failures

| Junction Temperature °C | Time, Hours | Time, Years |
|-------------------------|-------------|-------------|
| 80 | 1,032,200 | 117.8 |
| 90 | 419,300 | 47.9 |
| 100 | 178,700 | 20.4 |
| 110 | 79,600 | 9.4 |
| 120 | 37,000 | 4.2 |
| 130 | 17,800 | 2.0 |
| 140 | 8,900 | 1.0 |

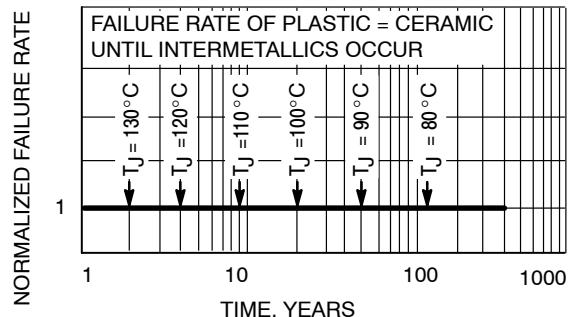


Figure 3. Failure Rate vs. Time Junction Temperature

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | V _{CC} (V) | T _A = 25°C | | T _A ≤ 85°C | | -55 ≤ T _A ≤ 125°C | | Unit |
|------------------|--|---|---------------------|-----------------------|------|-----------------------|------|------------------------------|------|------|
| | | | | Min | Max | Min | Max | Min | Max | |
| V _{IH} | Minimum High-Level Input Voltage ON/OFF Control Input | R _{ON} = Per Spec | 2.0 | 1.5 | | 1.5 | | 1.5 | | V |
| | | | 3.0 | 2.1 | | 2.1 | | 2.1 | | |
| | | | 4.5 | 3.15 | | 3.15 | | 3.15 | | |
| | | | 5.5 | 3.85 | | 3.85 | | 3.85 | | |
| V _{IL} | Maximum Low-Level Input Voltage ON/OFF Control Input | R _{ON} = Per Spec | 2.0 | | 0.5 | | 0.5 | | 0.5 | V |
| | | | 3.0 | | 0.9 | | 0.9 | | 0.9 | |
| | | | 4.5 | | 1.35 | | 1.35 | | 1.35 | |
| | | | 5.5 | | 1.65 | | 1.65 | | 1.65 | |
| I _{IN} | Maximum Input Leakage Current ON/OFF Control Input | V _{IN} = V _{CC} or GND | 0 to 5.5 | | ±0.1 | | ±1.0 | | ±1.0 | μA |
| I _{CC} | Maximum Quiescent Supply Current | V _{IN} = V _{CC} or GND V _{IO} = 0 V | 5.5 | | 1.0 | | 20 | | 40 | μA |
| R _{ON} | Maximum "ON" Resistance | V _{IN} = V _{IH} V _{IS} = V _{CC} or GND I _{IS} ≤ 5 mA (Figure 4) | 3.0 | | 60 | | 70 | | 100 | Ω |
| | | | 4.5 | | 45 | | 50 | | 60 | |
| | | | 5.5 | | 40 | | 45 | | 55 | |
| I _{OFF} | Maximum Off-Channel Leakage Current | V _{IN} = V _{IL} V _{IS} = V _{CC} or GND Switch Off (Figure 5) | 5.5 | | 0.1 | | 0.5 | | 1.0 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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AC ELECTRICAL CHARACTERISTICS $C_{load} = 50 \text{ pF}$, Input $t_r/t_f = 3.0 \text{ ns}$

| Symbol | Parameter | Test Conditions | V_{CC} (V) | $T_A = 25^\circ\text{C}$ | | | $T_A \leq 85^\circ\text{C}$ | | $-55 \leq T_A \leq 125^\circ\text{C}$ | | Unit |
|--------------------------|--|--|-----------------|--|-----|-----|-----------------------------|-----|---------------------------------------|-----|------|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| t_{PLH} , t_{PHL} | Maximum Propagation Delay, Input X to Y | $Y_A = \text{Open}$ (Figure 14) | 2.0 | | 1 | 5 | | 6 | | 7 | ns |
| | | | 3.0 | | 0.6 | 2 | | 3 | | 4 | |
| | | | 4.5 | | 0.6 | 1 | | 1 | | 2 | |
| | | | 5.5 | | 0.6 | 1 | | 1 | | 1 | |
| t_{PLZ} , t_{PHZ} | Maximum Propagation Delay, ON/OFF Control to Analog Output | $R_L = 1000 \Omega$ (Figure 15) | 2.0 | | 32 | 40 | | 45 | | 50 | ns |
| | | | 3.0 | | 28 | 35 | | 40 | | 45 | |
| | | | 4.5 | | 24 | 30 | | 35 | | 40 | |
| | | | 5.5 | | 20 | 25 | | 30 | | 35 | |
| t_{PZL} , t_{PZH} | Maximum Propagation Delay, ON/OFF Control to Analog Output | $R_L = 1000 \Omega$ (Figure 15) | 2.0 | | 32 | 40 | | 45 | | 50 | ns |
| | | | 3.0 | | 28 | 35 | | 40 | | 45 | |
| | | | 4.5 | | 24 | 30 | | 35 | | 40 | |
| | | | 5.5 | | 20 | 25 | | 30 | | 35 | |
| C_{IN} | Maximum Input Capacitance | ON/OFF Control Input | 0.0 | | 3 | 10 | | 10 | | 10 | pF |
| | | Control Input = GND Analog I/O Feedthrough | 5.0 | | 4 | 10 | | 10 | | 10 | |
| | | | | Typical @ 25°C, $V_{CC} = 5.0 \text{ V}$ | | | | | | | |
| C_{PD} | Power Dissipation Capacitance (Note 6) | | | 18 | | | | | | pF | |

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$. C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted)

| Symbol | Parameter | Test Conditions | V_{CC} | Limit 25°C | Unit |
|----------------|--|--|-------------------|-------------------|------------------|
| BW | Maximum On-Channel Bandwidth or Minimum Frequency Response (Figure 10) | $f_{in} = 1 \text{ MHz}$ Sine Wave Adjust f_{in} voltage to obtain 0 dBm at V_{OS} Increase $f_{in} =$ frequency until dB meter reads -3 dB $R_L = 50 \Omega$ | 3.0 4.5 5.5 | 150 175 180 | MHz |
| ISO_{off} | Off-Channel Feedthrough Isolation (Figure 11) | $f_{in} =$ Sine Wave Adjust f_{in} voltage to obtain 0 dBm at V_{IS} $f_{in} = 10 \text{ kHz}$, $R_L = 600 \Omega$ | 3.0 4.5 5.5 | -80 -80 -80 | dB |
| $NOISE_{feed}$ | Feedthrough Noise Control to Switch (Figure 12) | $V_{in} \leq 1 \text{ MHz}$ Square Wave ($t_r = t_f = 2 \text{ ns}$) $R_L = 600 \Omega$ | 3.0 4.5 5.5 | 45 60 130 | mV _{PP} |
| THD | Total Harmonic Distortion (Figure 13) | $f_{in} = 1 \text{ kHz}$, $R_L = 10 \text{ k}\Omega$ $THD = THD_{Measured} - THD_{Source}$ $V_{IS} = 3.0 \text{ V}_{PP}$ sine wave $V_{IS} = 5.0 \text{ V}_{PP}$ sine wave | 3.3 5.5 | 0.30 0.15 | % |

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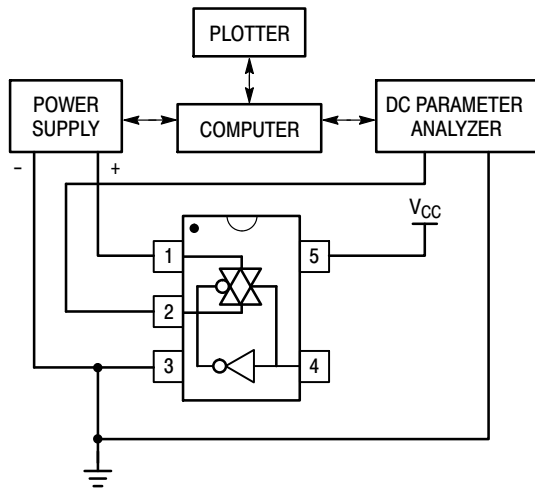


Figure 4. On Resistance Test Set-Up

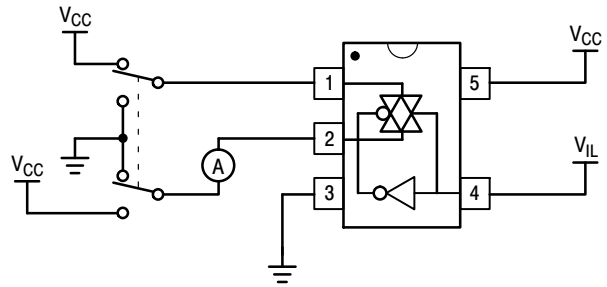


Figure 5. Maximum Off-Channel Leakage Current Test Set-Up

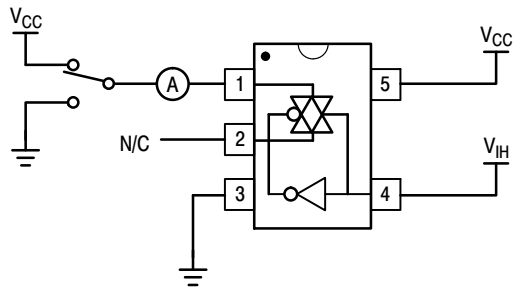


Figure 6. Maximum On-Channel Leakage Current Test Set-Up

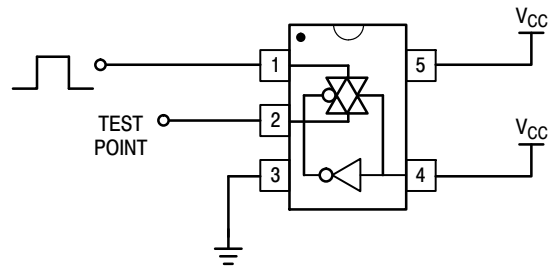


Figure 7. Propagation Delay Test Set-Up

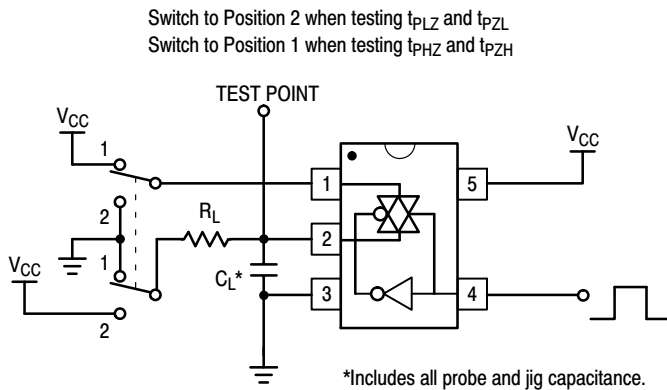


Figure 8. Propagation Delay Output Enable/Disable Test Set-Up

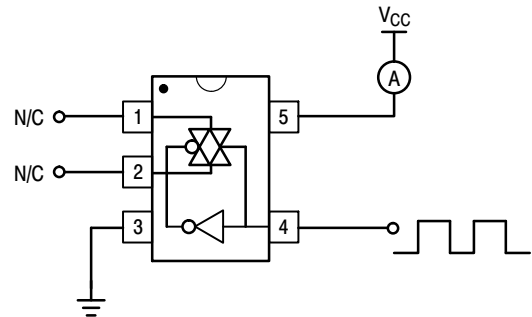


Figure 9. Power Dissipation Capacitance Test Set-Up

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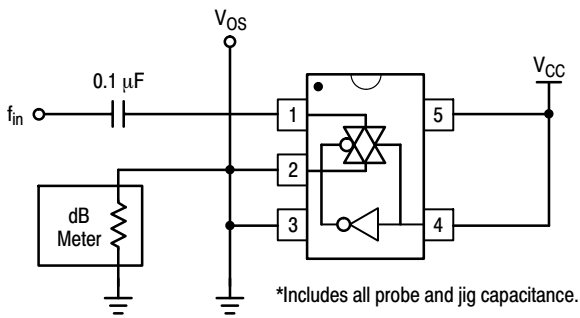


Figure 10. Maximum On-Channel Bandwidth Test Set-Up

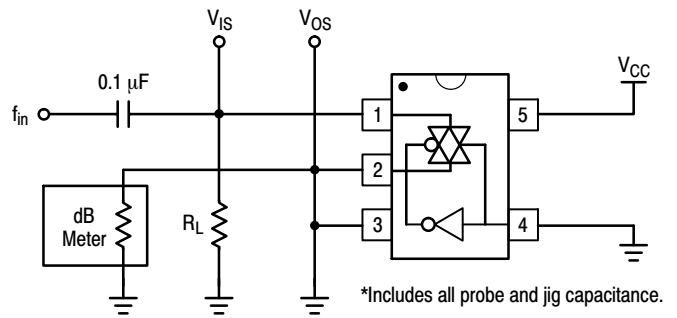


Figure 11. Off-Channel Feedthrough Isolation Test Set-Up

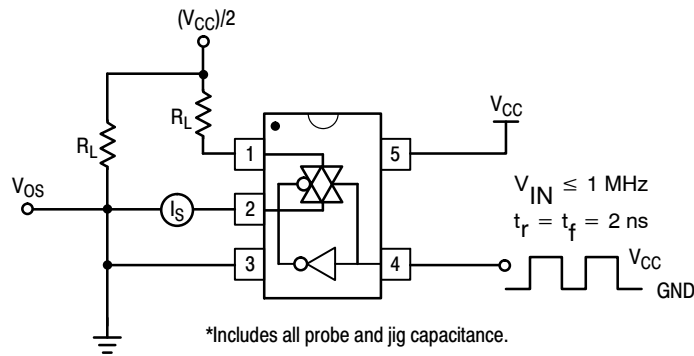


Figure 12. Feedthrough Noise, ON/OFF Control to Analog Out, Test Set-Up

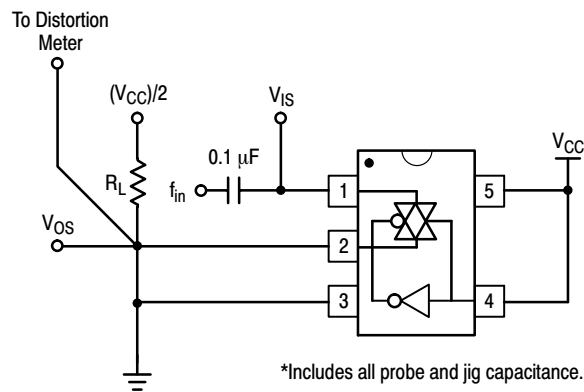


Figure 13. Total Harmonic Distortion Test Set-Up

MC74VHC1G66

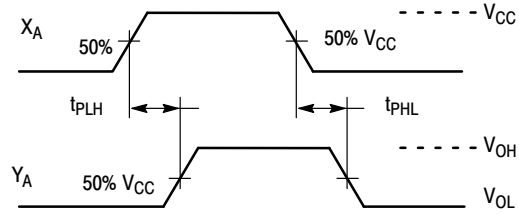


Figure 14. Propagation Delay, Analog In to Analog Out Waveforms

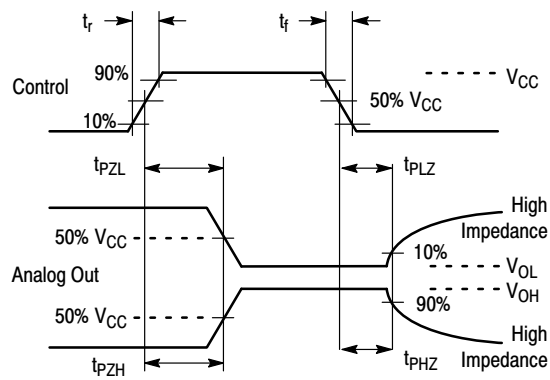


Figure 15. Propagation Delay, ON/OFF Control

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|------------------|---------------------|-----------------------|
| MC74VHC1G66DFT1G | SC-88A (Pb-Free) | 3000 / Tape & Reel |
| NLVVHC1G66DFT1G* | | |
| MC74VHC1G66DFT2G | | |
| NLVVHC1G66DFT2G* | | |
| MC74VHC1G66DTT1G | TSOP-5 (Pb-Free) | 3000 / Tape & Reel |
| NLVVHC1G66DTT1G* | | |

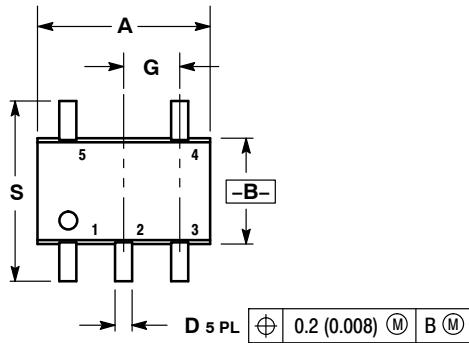
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

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PACKAGE DIMENSIONS

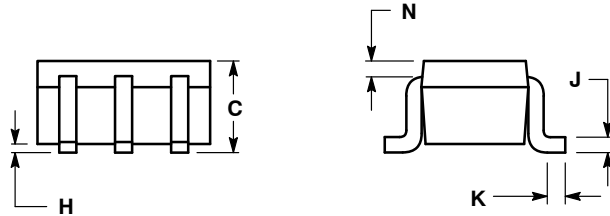
SC-88A (SC-70-5/SOT-353)
CASE 419A-02
ISSUE L



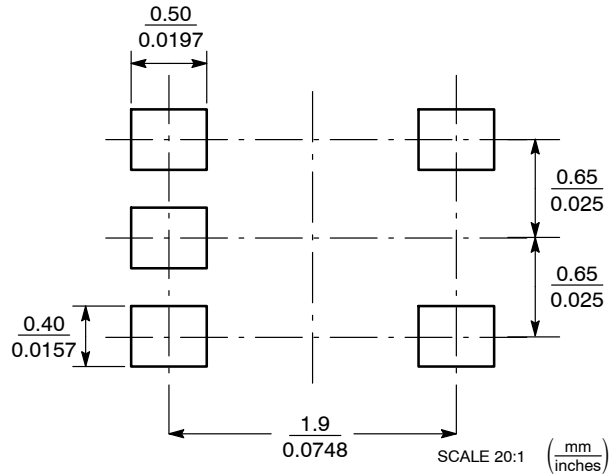
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|------|
| | MIN | MAX | MIN | MAX |
| A | 0.071 | 0.087 | 1.80 | 2.20 |
| B | 0.045 | 0.053 | 1.15 | 1.35 |
| C | 0.031 | 0.043 | 0.80 | 1.10 |
| D | 0.004 | 0.012 | 0.10 | 0.30 |
| G | 0.026 BSC | | 0.65 BSC | |
| H | --- | 0.004 | --- | 0.10 |
| J | 0.004 | 0.010 | 0.10 | 0.25 |
| K | 0.004 | 0.012 | 0.10 | 0.30 |
| N | 0.008 REF | | 0.20 REF | |
| S | 0.079 | 0.087 | 2.00 | 2.20 |



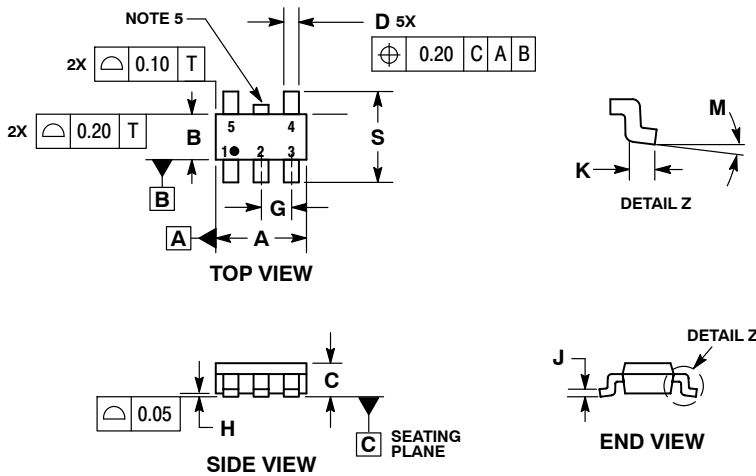
SOLDER FOOTPRINT



MC74VHC1G66

PACKAGE DIMENSIONS

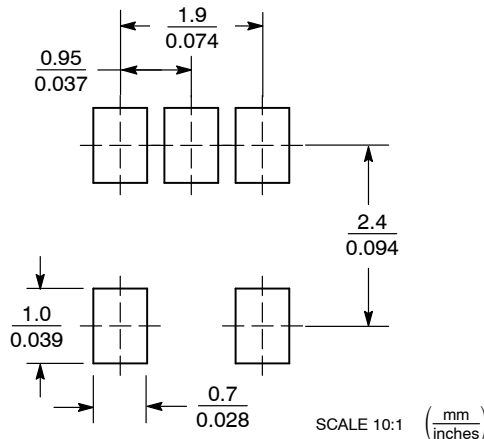
TSOP-5 CASE 483-02 ISSUE M



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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