



**THE DATASHEET OF
MC74VHC132MELG**



MC74VHC132

Quad 2-Input NAND Schmitt Trigger

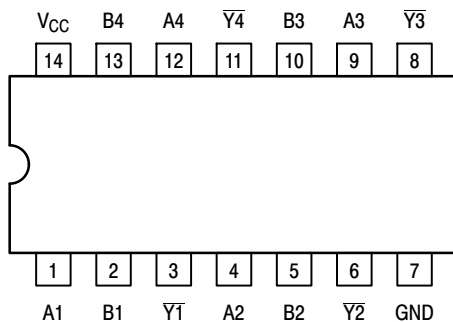
The MC74VHC132 is an advanced high speed CMOS Schmitt NAND trigger fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

Pin configuration and function are the same as the MC74VHC00, but the inputs have hysteresis and, with its Schmitt trigger function, the VHC132 can be used as a line receiver which will receive slow input signals.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

Features

- High Speed: $t_{PD} = 4.9$ ns (Typ) at $V_{CC} = 5.0$ V
- Low Power Dissipation: $I_{CC} = 2$ μ A (Max) at $T_A = 25^\circ$ C
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\%$ V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise: $V_{OLP} = 0.8$ V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance:
 - Human Body Model > 2000 V;
 - Machine Model > 200 V
- Chip Complexity: 72 FETs or 18 Equivalent Gates
- These Devices are Pb-Free and are RoHS Compliant



(Top View)

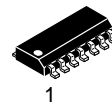
Figure 1. Pinout: 14-Lead Packages



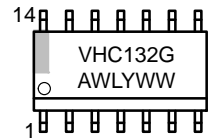
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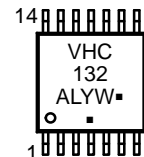
MARKING DIAGRAMS



SOIC-14
D SUFFIX
CASE 751A



TSSOP-14
DT SUFFIX
CASE 948G



A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

| Inputs | | Output |
|--------|---|-----------|
| A | B | \bar{Y} |
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MC74VHC132

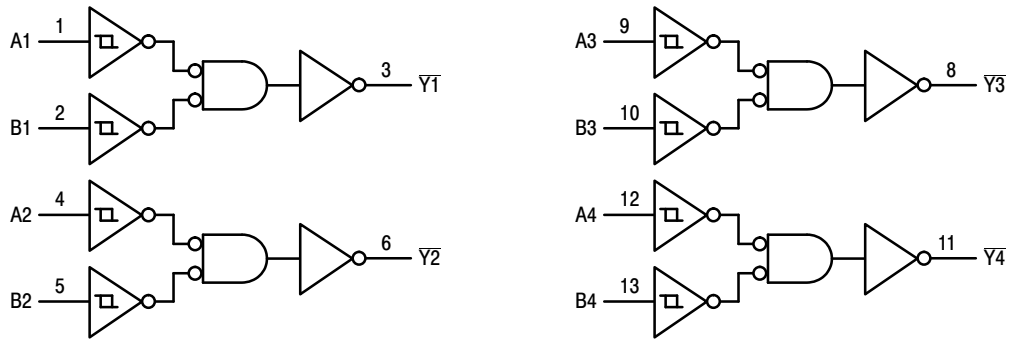


Figure 2. Logic Diagram

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|-----------|--|------------------------|------|
| V_{CC} | DC Supply Voltage | -0.5 to +7.0 | V |
| V_{in} | DC Input Voltage | -0.5 to +7.0 | V |
| V_{out} | DC Output Voltage | -0.5 to $V_{CC} + 0.5$ | V |
| I_{IK} | Input Diode Current | -20 | mA |
| I_{OK} | Output Diode Current | ± 20 | mA |
| I_{out} | DC Output Current, per Pin | ± 25 | mA |
| I_{CC} | DC Supply Current, V_{CC} and GND Pins | ± 50 | mA |
| P_D | Power Dissipation in Still Air, SOIC Packages† TSSOP Package† | 500 450 | mW |
| T_{stg} | Storage Temperature | -65 to +150 | °C |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating - SOIC Packages: - 7 mW/°C from 65° to 125°C
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|-----------|--|-----|----------|------|
| V_{CC} | DC Supply Voltage | 2.0 | 5.5 | V |
| V_{in} | DC Input Voltage | 0 | 5.5 | V |
| V_{out} | DC Output Voltage | 0 | V_{CC} | V |
| T_A | Operating Temperature, All Package Types | -55 | + 125 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

MC74VHC132

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | V _{CC} V | T _A = 25°C | | | T _A = -55 to +125°C | | Unit |
|-----------------|---------------------------------------|--|----------------------|-----------------------|-------------------|----------------------|--------------------------------|----------------------|------|
| | | | | Min | Typ | Max | Min | Max | |
| V _{T+} | Positive Threshold Voltage (Figure 5) | | 3.0 4.5 5.5 | | | 2.20 3.15 3.85 | | 2.20 3.15 3.85 | V |
| V _{T-} | Negative Threshold Voltage (Figure 5) | | 3.0 4.5 5.5 | 0.9 1.35 1.65 | | | 0.90 1.35 1.65 | | V |
| V _H | Hysteresis Voltage (Figure 5) | | 3.0 4.5 5.5 | 0.30 0.40 0.50 | | 1.20 1.40 1.60 | 0.30 0.40 0.50 | 1.20 1.40 1.60 | V |
| V _{OH} | Minimum High-Level Output Voltage | V _{in} = V _{IH} or V _{IL} I _{OH} = -50 μA | 2.0 3.0 4.5 | 1.9 2.9 4.4 | 2.0 3.0 4.5 | | 1.9 2.9 4.4 | | V |
| | | V _{in} = V _{IH} or V _{IL} I _{OH} = -4 mA I _{OH} = -8 mA | 3.0 4.5 | 2.58 3.94 | | | 2.48 3.80 | | |
| V _{OL} | Maximum Low-Level Output Voltage | V _{in} = V _{IH} or V _{IL} I _{OL} = 50 μA | 2.0 3.0 4.5 | | 0 0 0 | 0.1 0.1 0.1 | | 0.1 0.1 0.1 | V |
| | | V _{in} = V _{IH} or V _{IL} I _{OL} = 4 mA I _{OL} = 8 mA | 3.0 4.5 | | | 0.36 0.36 | | 0.44 0.44 | |
| I _{in} | Maximum Input Leakage Current | V _{in} = 5.5 V or GND | 0 to 5.5 | | | ± 0.1 | | ± 1.0 | μA |
| I _{CC} | Maximum Quiescent Supply Current | V _{in} = V _{CC} or GND | 5.5 | | | 2.0 | | 20.0 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0ns)

| Symbol | Parameter | Test Conditions | T _A = 25°C | | | T _A = -55 to +125°C | | Unit |
|--|---|--|-----------------------|-------------|--------------|--------------------------------|--------------|------|
| | | | Min | Typ | Max | Min | Max | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, A or B to \bar{Y} | V _{CC} = 3.3 ± 0.3 V C _L = 15 pF C _L = 50 pF | | 7.6 10.1 | 11.9 15.4 | 1.0 1.0 | 14.0 17.5 | ns |
| | | V _{CC} = 5.0 ± 0.5 V C _L = 15 pF C _L = 50 pF | | 4.9 6.4 | 7.7 9.7 | 1.0 1.0 | 9.0 11.0 | |
| C _{in} | Maximum Input Capacitance | | | 4 | 10 | | 10 | pF |

| C _{PD} | Power Dissipation Capacitance (Note 1) | Typical @ 25°C, V _{CC} = 5.0 V | | Unit |
|-----------------|--|---|--|------|
| | | 16 | | |
| | | | | pF |

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/4 (per gate). C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

NOISE CHARACTERISTICS (Input t_r = t_f = 3.0ns, C_L = 50pF, V_{CC} = 5.0 V)

| Symbol | Characteristic | T _A = 25°C | | Unit |
|------------------|--|-----------------------|------|------|
| | | Typ | Max | |
| V _{OLP} | Quiet Output Maximum Dynamic V _{OL} | 0.3 | 0.8 | V |
| V _{OLV} | Quiet Output Minimum Dynamic V _{OL} | -0.3 | -0.8 | V |
| V _{IHD} | Minimum High Level Dynamic Input Voltage | | 3.5 | V |
| V _{ILD} | Maximum Low Level Dynamic Input Voltage | | 1.5 | V |

MC74VHC132

ORDERING INFORMATION

| Device | Package | Shipping† |
|-----------------|-----------------------|------------------|
| MC74VHC132DG | SOIC-14 (Pb-Free) | 55 Units / Rail |
| MC74VHC132DR2G | SOIC-14 (Pb-Free) | 2500 Tape & Reel |
| MC74VHC132DTR2G | TSSOP-14 (Pb-Free) | 2500 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MC74VHC132

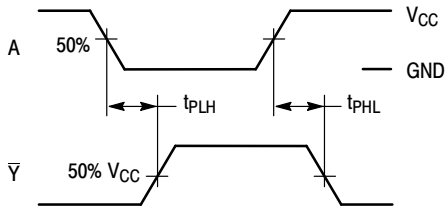
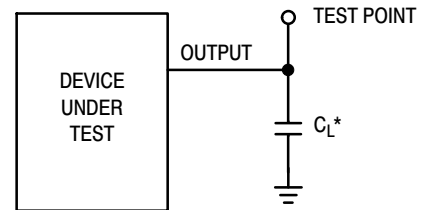
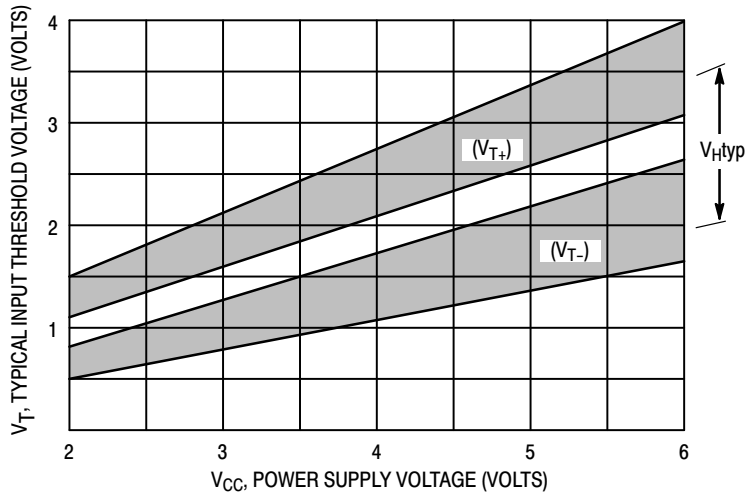


Figure 3. Switching Waveforms



*Includes all probe and jig capacitance

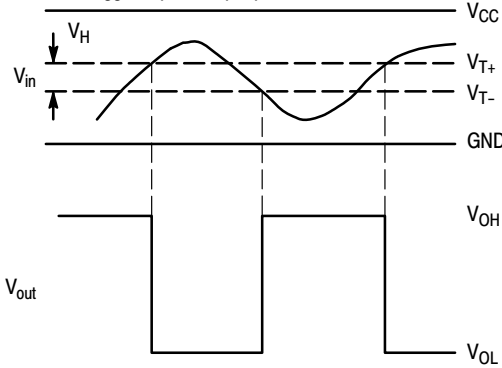
Figure 4. Test Circuit



$$V_{HTyp} = (V_{T+, typ}) - (V_{T-, typ})$$

Figure 5. Typical Input Threshold, V_{T+} , V_{T-} versus Power Supply Voltage

(a) A Schmitt-Trigger Squares Up Inputs With Slow Rise and Fall Times



(b) A Schmitt-Trigger Offers Maximum Noise Immunity

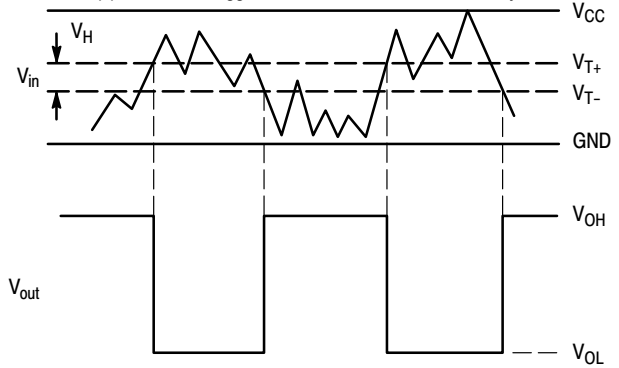


Figure 6. Typical Schmitt-Trigger Applications

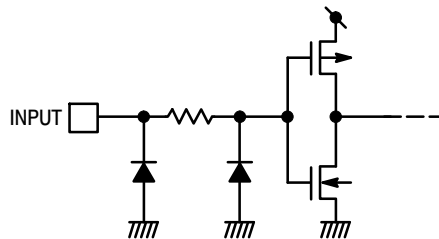
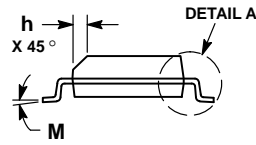
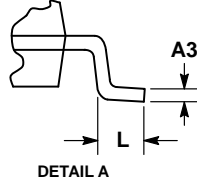
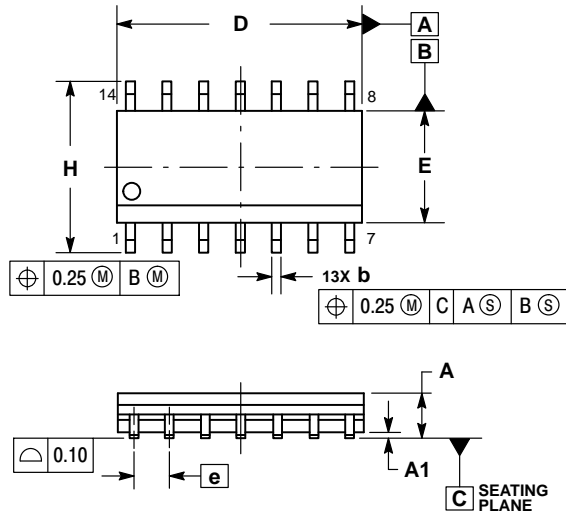


Figure 7. Input Equivalent Circuit

MC74VHC132

PACKAGE DIMENSIONS

SOIC-14
CASE 751A-03
ISSUE L

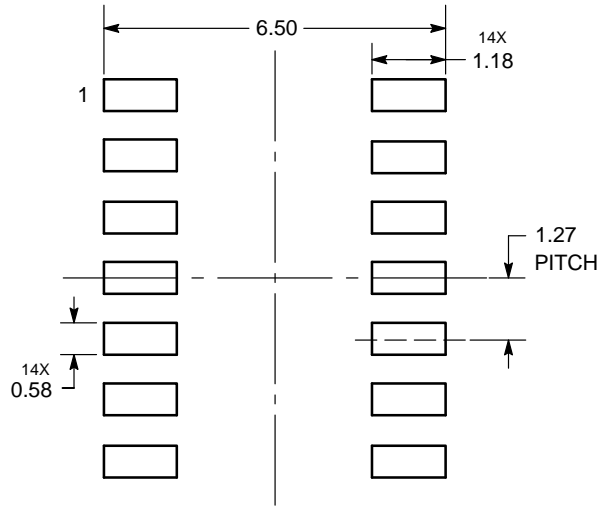


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | 0.054 | 0.068 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A3 | 0.19 | 0.25 | 0.008 | 0.010 |
| b | 0.35 | 0.49 | 0.014 | 0.019 |
| D | 8.55 | 8.75 | 0.337 | 0.344 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.019 |
| L | 0.40 | 1.25 | 0.016 | 0.049 |
| M | 0° | 7° | 0° | 7° |

SOLDERING FOOTPRINT*



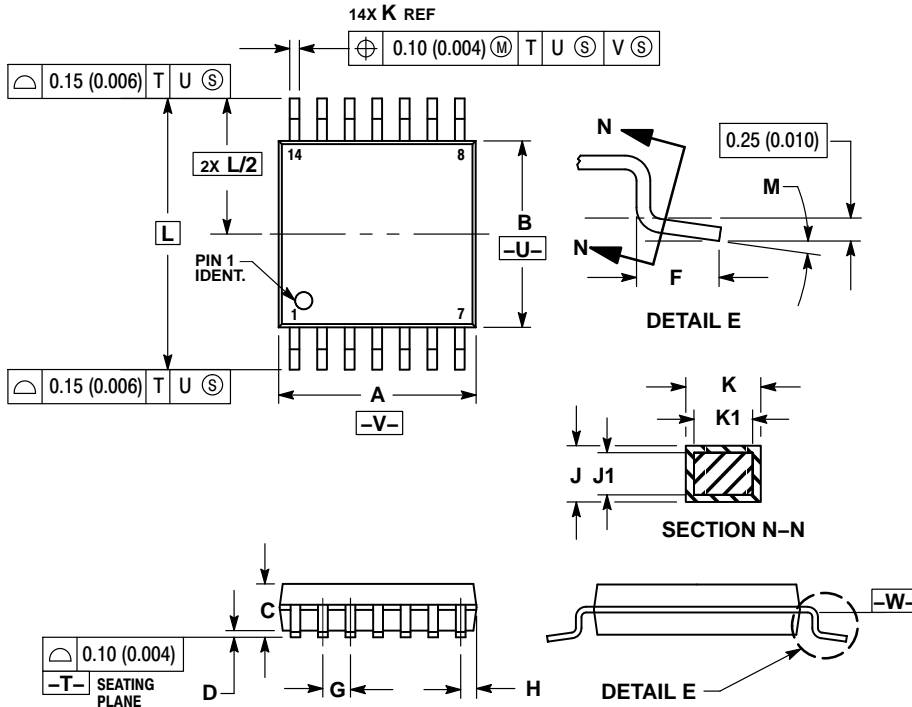
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC74VHC132

PACKAGE DIMENSIONS

TSSOP-14
CASE 948G
ISSUE C

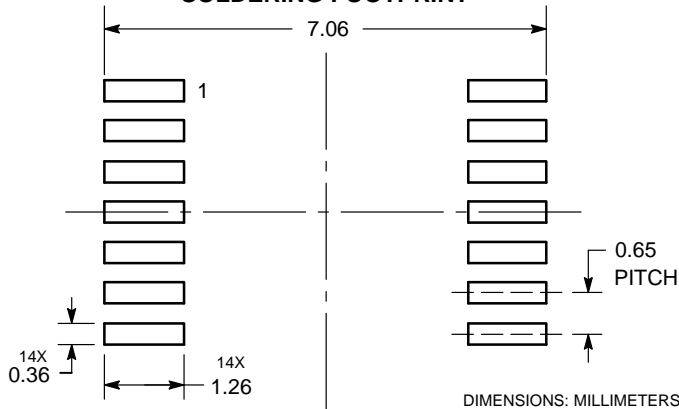


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

SOLDERING FOOTPRINT



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