



**THE DATASHEET OF  
MC74HC595ADTR2G**



# MC74HC595A

## 8-Bit Serial-Input/Serial or Parallel-Output Shift Register with Latched 3-State Outputs

### High-Performance Silicon-Gate CMOS

The MC74HC595A consists of an 8-bit shift register and an 8-bit D-type latch with three-state parallel outputs. The shift register accepts serial data and provides a serial output. The shift register also provides parallel data to the 8-bit latch. The shift register and latch have independent clock inputs. This device also has an asynchronous reset for the shift register.

The HC595A directly interfaces with the SPI serial data port on CMOS MPUs and MCUs.

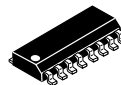
#### Features

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7 A
- Chip Complexity: 328 FETs or 82 Equivalent Gates
- Improvements over HC595
  - ◆ Improved Propagation Delays
  - ◆ 50% Lower Quiescent Power
  - ◆ Improved Input Noise and Latchup Immunity
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

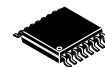


ON Semiconductor®

[www.onsemi.com](http://www.onsemi.com)



SOIC-16  
D SUFFIX  
CASE 751B

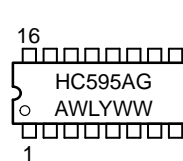


TSSOP-16  
DT SUFFIX  
CASE 948F

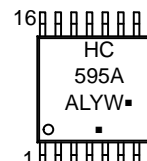


QFN16  
MN SUFFIX  
CASE 485AW

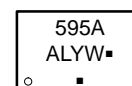
#### MARKING DIAGRAMS



SOIC-16



TSSOP-16



QFN16\*

\*V595A marking used for NLV74HC595AMN1TWG

A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G, ■ = Pb-Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

# MC74HC595A

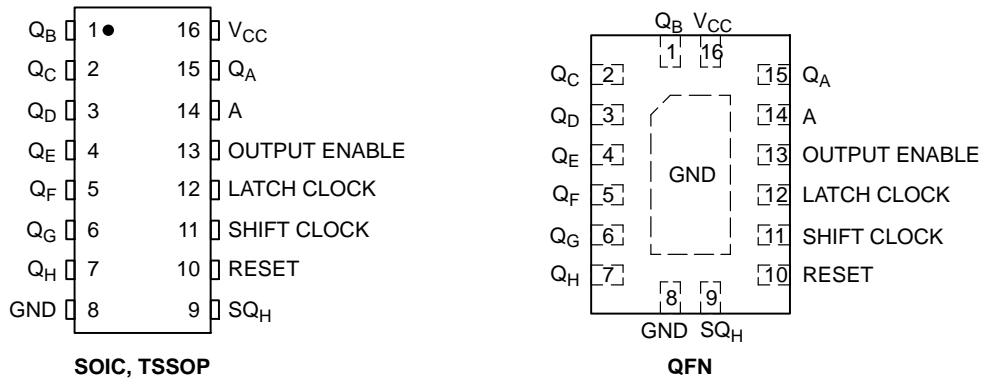
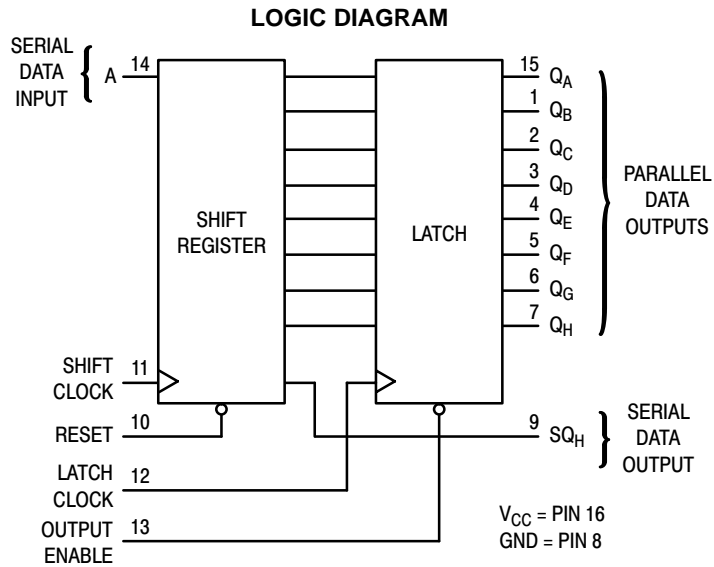


Figure 1. Pin Assignments



# MC74HC595A

## MAXIMUM RATINGS

| Symbol    | Parameter  | Value                  | Unit |
|-----------|--|------------------------|------|
| $V_{CC}$  | DC Supply Voltage (Referenced to GND)  | -0.5 to +7.0           | V    |
| $V_{in}$  | DC Input Voltage (Referenced to GND)   | -0.5 to $V_{CC}+0.5$   | V    |
| $V_{out}$ | DC Output Voltage (Referenced to GND)  | -0.5 to $V_{CC}+0.5$   | V    |
| $I_{in}$  | DC Input Current, per Pin  | $\pm 20$               | mA   |
| $I_{out}$ | DC Output Current, per Pin   | $\pm 35$               | mA   |
| $I_{CC}$  | DC Supply Current, $V_{CC}$ and GND Pins   | $\pm 75$               | mA   |
| $P_D$     | Power Dissipation in Still Air, SOIC Package†<br>TSSOP Package†  | 500<br>450             | mW   |
| $T_{stg}$ | Storage Temperature  | -65 to +150            | °C   |
| $T_L$     | Lead Temperature, 1 mm from Case for 10 Seconds<br>(Plastic DIP, SOIC or TSSOP Package)                    | 260                    | °C   |
| $V_{ESD}$ | ESD Withstand Voltage Human Body Model (Note 1)<br>Machine Model (Note 2)<br>Charged Device Model (Note 3) | > 3000<br>> 400<br>N/A | V    |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating: SOIC Package: -7 mW/°C from 65° to 125°C  
TSSOP Package: -6.1 mW/°C from 65° to 125°C

1. Tested to EIA/JESD22-A114-A.
2. Tested to EIA/JESD22-A115-A.
3. Tested to JESD22-C101-A.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

## RECOMMENDED OPERATING CONDITIONS

| Symbol            | Parameter   | Min  | Max                     | Unit |
|-------------------|---|--|-------------------------|------|
| $V_{CC}$          | DC Supply Voltage (Referenced to GND)                   | 2.0  | 6.0                     | V    |
| $V_{in}, V_{out}$ | DC Input Voltage, Output Voltage<br>(Referenced to GND) | 0  | $V_{CC}$                | V    |
| $T_A$             | Operating Temperature, All Package Types                | -55  | +125                    | °C   |
| $t_r, t_f$        | Input Rise and Fall Time<br>(Figure 1)                  | $V_{CC} = 2.0 \text{ V}$<br>$V_{CC} = 4.5 \text{ V}$<br>$V_{CC} = 6.0 \text{ V}$ | 0<br>1000<br>500<br>400 | ns   |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

# MC74HC595A

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol          | Parameter  | Test Conditions  | V <sub>CC</sub><br>V | Guaranteed Limit |        |         | Unit |
|-----------------|--|--|----------------------|------------------|--------|---------|------|
|                 |  |  |                      | -55 to 25°C      | ≤ 85°C | ≤ 125°C |      |
| V <sub>IH</sub> | Minimum High-Level Input Voltage                                     | V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V<br> I <sub>out</sub>   ≤ 20 μA   | 2.0                  | 1.5              | 1.5    | 1.5     | V    |
|                 |  |  | 3.0                  | 2.1              | 2.1    | 2.1     |      |
|                 |  |  | 4.5                  | 3.15             | 3.15   | 3.15    |      |
|                 |  |  | 6.0                  | 4.2              | 4.2    | 4.2     |      |
| V <sub>IL</sub> | Maximum Low-Level Input Voltage                                      | V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V<br> I <sub>out</sub>   ≤ 20 μA   | 2.0                  | 0.5              | 0.5    | 0.5     | V    |
|                 |  |  | 3.0                  | 0.9              | 0.9    | 0.9     |      |
|                 |  |  | 4.5                  | 1.35             | 1.35   | 1.35    |      |
|                 |  |  | 6.0                  | 1.8              | 1.8    | 1.8     |      |
| V <sub>OH</sub> | Minimum High-Level Output Voltage, Q <sub>A</sub> - Q <sub>H</sub>   | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20 μA  | 2.0                  | 1.9              | 1.9    | 1.9     | V    |
|                 |  |  | 4.5                  | 4.4              | 4.4    | 4.4     |      |
|                 |  |  | 6.0                  | 5.9              | 5.9    | 5.9     |      |
|                 |  | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 2.4 mA<br> I <sub>out</sub>   ≤ 6.0 mA<br> I <sub>out</sub>   ≤ 7.8 mA | 3.0                  | 2.48             | 2.34   | 2.2     |      |
|                 |  |  | 4.5                  | 3.98             | 3.84   | 3.7     |      |
|                 |  |  | 6.0                  | 5.48             | 5.34   | 5.2     |      |
| V <sub>OL</sub> | Maximum Low-Level Output Voltage, Q <sub>A</sub> - Q <sub>H</sub>    | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20 μA  | 2.0                  | 0.1              | 0.1    | 0.1     | V    |
|                 |  |  | 4.5                  | 0.1              | 0.1    | 0.1     |      |
|                 |  |  | 6.0                  | 0.1              | 0.1    | 0.1     |      |
|                 |  | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 2.4 mA<br> I <sub>out</sub>   ≤ 6.0 mA<br> I <sub>out</sub>   ≤ 7.8 mA | 3.0                  | 0.26             | 0.33   | 0.4     |      |
|                 |  |  | 4.5                  | 0.26             | 0.33   | 0.4     |      |
|                 |  |  | 6.0                  | 0.26             | 0.33   | 0.4     |      |
| V <sub>OH</sub> | Minimum High-Level Output Voltage, SQ <sub>H</sub>                   | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20 μA  | 2.0                  | 1.9              | 1.9    | 1.9     | V    |
|                 |  |  | 4.5                  | 4.4              | 4.4    | 4.4     |      |
|                 |  |  | 6.0                  | 5.9              | 5.9    | 5.9     |      |
|                 |  | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 2.4 mA<br> I <sub>out</sub>   ≤ 4.0 mA<br> I <sub>out</sub>   ≤ 5.2 mA | 3.0                  | 2.48             | 2.34   | 2.2     |      |
|                 |  |  | 4.5                  | 3.98             | 3.84   | 3.7     |      |
|                 |  |  | 6.0                  | 5.48             | 5.34   | 5.2     |      |
| V <sub>OL</sub> | Maximum Low-Level Output Voltage, SQ <sub>H</sub>                    | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20 μA  | 2.0                  | 0.1              | 0.1    | 0.1     | V    |
|                 |  |  | 4.5                  | 0.1              | 0.1    | 0.1     |      |
|                 |  |  | 6.0                  | 0.1              | 0.1    | 0.1     |      |
|                 |  | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 2.4 mA<br> I <sub>out</sub>   ≤ 4.0 mA<br> I <sub>out</sub>   ≤ 5.2 mA | 3.0                  | 0.26             | 0.33   | 0.4     |      |
|                 |  |  | 4.5                  | 0.26             | 0.33   | 0.4     |      |
|                 |  |  | 6.0                  | 0.26             | 0.33   | 0.4     |      |
| I <sub>in</sub> | Maximum Input Leakage Current  | V <sub>in</sub> = V <sub>CC</sub> or GND   | 6.0                  | ±0.1             | ±1.0   | ±1.0    | μA   |
| I <sub>OZ</sub> | Maximum Three-State Leakage Current, Q <sub>A</sub> - Q <sub>H</sub> | Output in High-Impedance State<br>V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>V <sub>out</sub> = V <sub>CC</sub> or GND                  | 6.0                  | ±0.5             | ±5.0   | ±10     | μA   |
| I <sub>CC</sub> | Maximum Quiescent Supply Current (per Package)                       | V <sub>in</sub> = V <sub>CC</sub> or GND<br>I <sub>out</sub> = 0 μA  | 6.0                  | 4.0              | 40     | 160     | μA   |

# MC74HC595A

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6.0 ns)

| Symbol                                 | Parameter  | V <sub>CC</sub><br>V                    | Guaranteed Limit |        |         | Unit |
|--|--|---|------------------|--------|---------|------|
|  |  |   | -55 to 25°C      | ≤ 85°C | ≤ 125°C |      |
| f <sub>max</sub>                       | Maximum Clock Frequency (50% Duty Cycle)<br>(Figures 1 and 7)  | 2.0                                     | 6.0              | 4.8    | 4.0     | MHz  |
|  |  | 3.0                                     | 15               | 10     | 8.0     |      |
|  |  | 4.5                                     | 30               | 24     | 20      |      |
|  |  | 6.0                                     | 35               | 28     | 24      |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Shift Clock to SQ <sub>H</sub><br>(Figures 1 and 7)                           | 2.0                                     | 140              | 175    | 210     | ns   |
|  |  | 3.0                                     | 100              | 125    | 150     |      |
|  |  | 4.5                                     | 28               | 35     | 42      |      |
|  |  | 6.0                                     | 24               | 30     | 36      |      |
| t <sub>PHL</sub>                       | Maximum Propagation Delay, Reset to SQ <sub>H</sub><br>(Figures 2 and 7)                                 | 2.0                                     | 145              | 180    | 220     | ns   |
|  |  | 3.0                                     | 100              | 125    | 150     |      |
|  |  | 4.5                                     | 29               | 36     | 44      |      |
|  |  | 6.0                                     | 25               | 31     | 38      |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Latch Clock to Q <sub>A</sub> – Q <sub>H</sub><br>(Figures 3 and 7)           | 2.0                                     | 140              | 175    | 210     | ns   |
|  |  | 3.0                                     | 100              | 125    | 150     |      |
|  |  | 4.5                                     | 28               | 35     | 42      |      |
|  |  | 6.0                                     | 24               | 30     | 36      |      |
| t <sub>PLZ</sub> ,<br>t <sub>PHZ</sub> | Maximum Propagation Delay, Output Enable to Q <sub>A</sub> – Q <sub>H</sub><br>(Figures 4 and 8)         | 2.0                                     | 150              | 190    | 225     | ns   |
|  |  | 3.0                                     | 100              | 125    | 150     |      |
|  |  | 4.5                                     | 30               | 38     | 45      |      |
|  |  | 6.0                                     | 26               | 33     | 38      |      |
| t <sub>PZL</sub> ,<br>t <sub>PZH</sub> | Maximum Propagation Delay, Output Enable to Q <sub>A</sub> – Q <sub>H</sub><br>(Figures 4 and 8)         | 2.0                                     | 135              | 170    | 205     | ns   |
|  |  | 3.0                                     | 90               | 110    | 130     |      |
|  |  | 4.5                                     | 27               | 34     | 41      |      |
|  |  | 6.0                                     | 23               | 29     | 35      |      |
| t <sub>TLH</sub> ,<br>t <sub>THL</sub> | Maximum Output Transition Time, Q <sub>A</sub> – Q <sub>H</sub><br>(Figures 3 and 7)                     | 2.0                                     | 60               | 75     | 90      | ns   |
|  |  | 3.0                                     | 23               | 27     | 31      |      |
|  |  | 4.5                                     | 12               | 15     | 18      |      |
|  |  | 6.0                                     | 10               | 13     | 15      |      |
| t <sub>TLH</sub> ,<br>t <sub>THL</sub> | Maximum Output Transition Time, SQ <sub>H</sub><br>(Figures 1 and 7)                                     | 2.0                                     | 75               | 95     | 110     | ns   |
|  |  | 3.0                                     | 27               | 32     | 36      |      |
|  |  | 4.5                                     | 15               | 19     | 22      |      |
|  |  | 6.0                                     | 13               | 16     | 19      |      |
| C <sub>in</sub>                        | Maximum Input Capacitance  | –                                       | 10               | 10     | 10      | pF   |
| C <sub>out</sub>                       | Maximum Three–State Output Capacitance (Output in High–Impedance State), Q <sub>A</sub> – Q <sub>H</sub> | –                                       | 15               | 15     | 15      | pF   |
| C <sub>PD</sub>                        | Power Dissipation Capacitance (Per Package)*   | Typical @ 25°C, V <sub>CC</sub> = 5.0 V |                  |        | pF      |      |
|  |  | 300                                     |                  |        |         |      |

# MC74HC595A

## TIMING REQUIREMENTS (Input $t_r = t_f = 6.0$ ns)

| Symbol                          | Parameter  | V <sub>CC</sub><br>V | Guaranteed Limit |        |         | Unit |
|---------------------------------|--|----------------------|------------------|--------|---------|------|
|                                 |  |                      | 25°C to -55°C    | ≤ 85°C | ≤ 125°C |      |
| t <sub>su</sub>                 | Minimum Setup Time, Serial Data Input A to Shift Clock<br>(Figure 5) | 2.0                  | 50               | 65     | 75      | ns   |
|                                 |  | 3.0                  | 40               | 50     | 60      |      |
|                                 |  | 4.5                  | 10               | 13     | 15      |      |
|                                 |  | 6.0                  | 9.0              | 11     | 13      |      |
| t <sub>su</sub>                 | Minimum Setup Time, Shift Clock to Latch Clock<br>(Figure 6)         | 2.0                  | 75               | 95     | 110     | ns   |
|                                 |  | 3.0                  | 60               | 70     | 80      |      |
|                                 |  | 4.5                  | 15               | 19     | 22      |      |
|                                 |  | 6.0                  | 13               | 16     | 19      |      |
| t <sub>h</sub>                  | Minimum Hold Time, Shift Clock to Serial Data Input A<br>(Figure 5)  | 2.0                  | 5.0              | 5.0    | 5.0     | ns   |
|                                 |  | 3.0                  | 5.0              | 5.0    | 5.0     |      |
|                                 |  | 4.5                  | 5.0              | 5.0    | 5.0     |      |
|                                 |  | 6.0                  | 5.0              | 5.0    | 5.0     |      |
| t <sub>rec</sub>                | Minimum Recovery Time, Reset Inactive to Shift Clock<br>(Figure 2)   | 2.0                  | 50               | 65     | 75      | ns   |
|                                 |  | 3.0                  | 40               | 50     | 60      |      |
|                                 |  | 4.5                  | 10               | 13     | 15      |      |
|                                 |  | 6.0                  | 9.0              | 11     | 13      |      |
| t <sub>w</sub>                  | Minimum Pulse Width, Reset<br>(Figure 2)                             | 2.0                  | 60               | 75     | 90      | ns   |
|                                 |  | 3.0                  | 45               | 60     | 70      |      |
|                                 |  | 4.5                  | 12               | 15     | 18      |      |
|                                 |  | 6.0                  | 10               | 13     | 15      |      |
| t <sub>w</sub>                  | Minimum Pulse Width, Shift Clock<br>(Figure 1)                       | 2.0                  | 50               | 65     | 75      | ns   |
|                                 |  | 3.0                  | 40               | 50     | 60      |      |
|                                 |  | 4.5                  | 10               | 13     | 15      |      |
|                                 |  | 6.0                  | 9.0              | 11     | 13      |      |
| t <sub>w</sub>                  | Minimum Pulse Width, Latch Clock<br>(Figure 6)                       | 2.0                  | 50               | 65     | 75      | ns   |
|                                 |  | 3.0                  | 40               | 50     | 60      |      |
|                                 |  | 4.5                  | 10               | 13     | 15      |      |
|                                 |  | 6.0                  | 9.0              | 11     | 13      |      |
| t <sub>r</sub> , t <sub>f</sub> | Maximum Input Rise and Fall Times<br>(Figure 1)                      | 2.0                  | 1000             | 1000   | 1000    | ns   |
|                                 |  | 3.0                  | 800              | 800    | 800     |      |
|                                 |  | 4.5                  | 500              | 500    | 500     |      |
|                                 |  | 6.0                  | 400              | 400    | 400     |      |

# MC74HC595A

## FUNCTION TABLE

| Operation  | Inputs |                |             |             |               | Resulting Function   |                                   |                                   |  |
|--|--------|----------------|-------------|-------------|---------------|--|-----------------------------------|-----------------------------------|--|
|  | Reset  | Serial Input A | Shift Clock | Latch Clock | Output Enable | Shift Register Contents                                      | Latch Register Contents           | Serial Output SQ <sub>H</sub>     | Parallel Outputs Q <sub>A</sub> – Q <sub>H</sub> |
| Reset shift register                               | L      | X              | X           | L, H, ↓     | L             | L  | U                                 | L                                 | U  |
| Shift data into shift register                     | H      | D              | ↑           | L, H, ↓     | L             | D → SR <sub>A</sub> ;<br>SR <sub>N</sub> → SR <sub>N+1</sub> | U                                 | SR <sub>G</sub> → SR <sub>H</sub> | U  |
| Shift register remains unchanged                   | H      | X              | L, H, ↓     | L, H, ↓     | L             | U  | U                                 | U                                 | U  |
| Transfer shift register contents to latch register | H      | X              | L, H, ↓     | ↑           | L             | U  | SR <sub>N</sub> → LR <sub>N</sub> | U                                 | SR <sub>N</sub>                                  |
| Latch register remains unchanged                   | X      | X              | X           | L, H, ↓     | L             | *  | U                                 | *                                 | U  |
| Enable parallel outputs                            | X      | X              | X           | X           | L             | *  | **                                | *                                 | Enabled  |
| Force outputs into high impedance state            | X      | X              | X           | X           | H             | *  | **                                | *                                 | Z  |

SR = shift register contents  
LR = latch register contents

D = data (L, H) logic level  
U = remains unchanged

↑ = Low-to-High  
↓ = High-to-Low

\* = depends on Reset and Shift Clock inputs  
\*\* = depends on Latch Clock input

## PIN DESCRIPTIONS

### INPUTS A (Pin 14)

Serial Data Input. The data on this pin is shifted into the 8-bit serial shift register.

### CONTROL INPUTS Shift Clock (Pin 11)

Shift Register Clock Input. A low-to-high transition on this input causes the data at the Serial Input pin to be shifted into the 8-bit shift register.

### Reset (Pin 10)

Active-low, Asynchronous, Shift Register Reset Input. A low on this pin resets the shift register portion of this device only. The 8-bit latch is not affected.

### Latch Clock (Pin 12)

Storage Latch Clock Input. A low-to-high transition on this input latches the shift register data.

### Output Enable (Pin 13)

Active-low Output Enable. A low on this input allows the data from the latches to be presented at the outputs. A high on this input forces the outputs (Q<sub>A</sub>–Q<sub>H</sub>) into the high-impedance state. The serial output is not affected by this control unit.

### OUTPUTS Q<sub>A</sub> – Q<sub>H</sub> (Pins 15, 1, 2, 3, 4, 5, 6, 7)

Noninverted, 3-state, latch outputs.

### SQ<sub>H</sub> (Pin 9)

Noninverted, Serial Data Output. This is the output of the eighth stage of the 8-bit shift register. This output does not have three-state capability.

# MC74HC595A

## SWITCHING WAVEFORMS

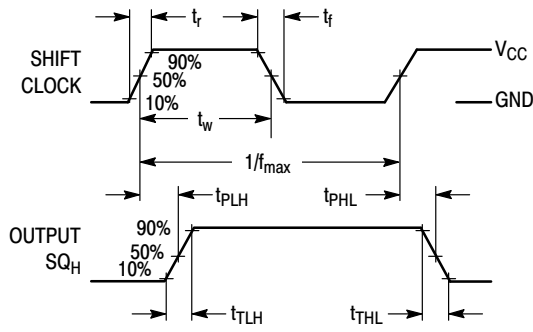


Figure 1.

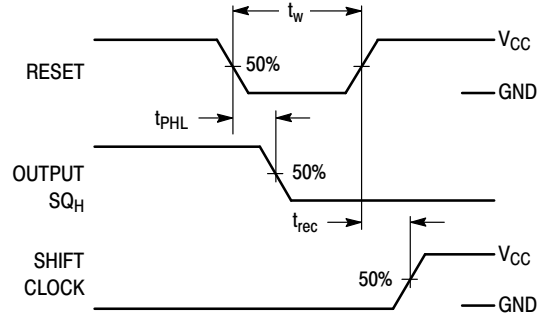


Figure 2.

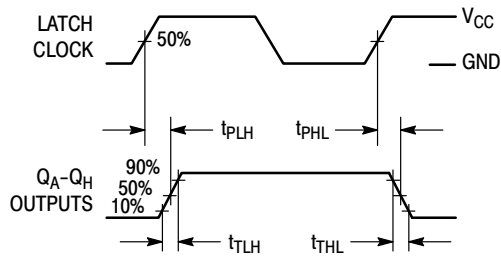


Figure 3.

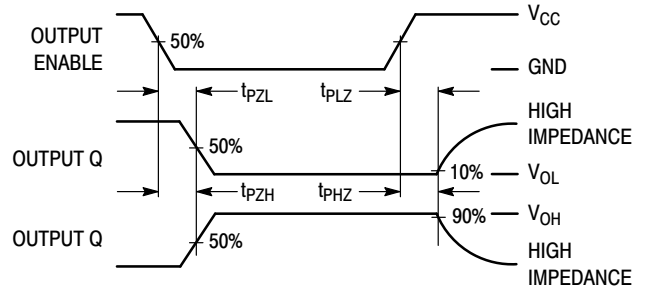


Figure 4.

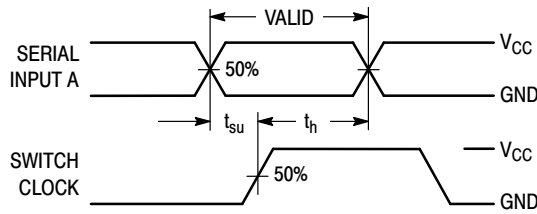


Figure 5.

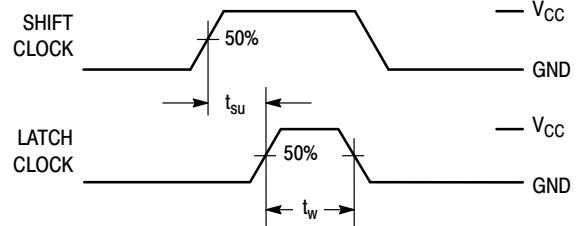
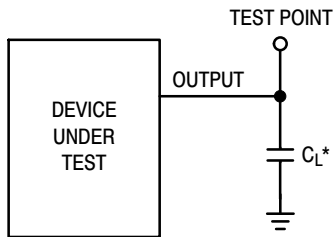


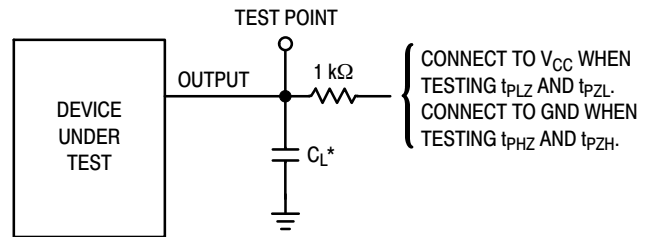
Figure 6.

## TEST CIRCUITS



\*Includes all probe and jig capacitance

Figure 7.

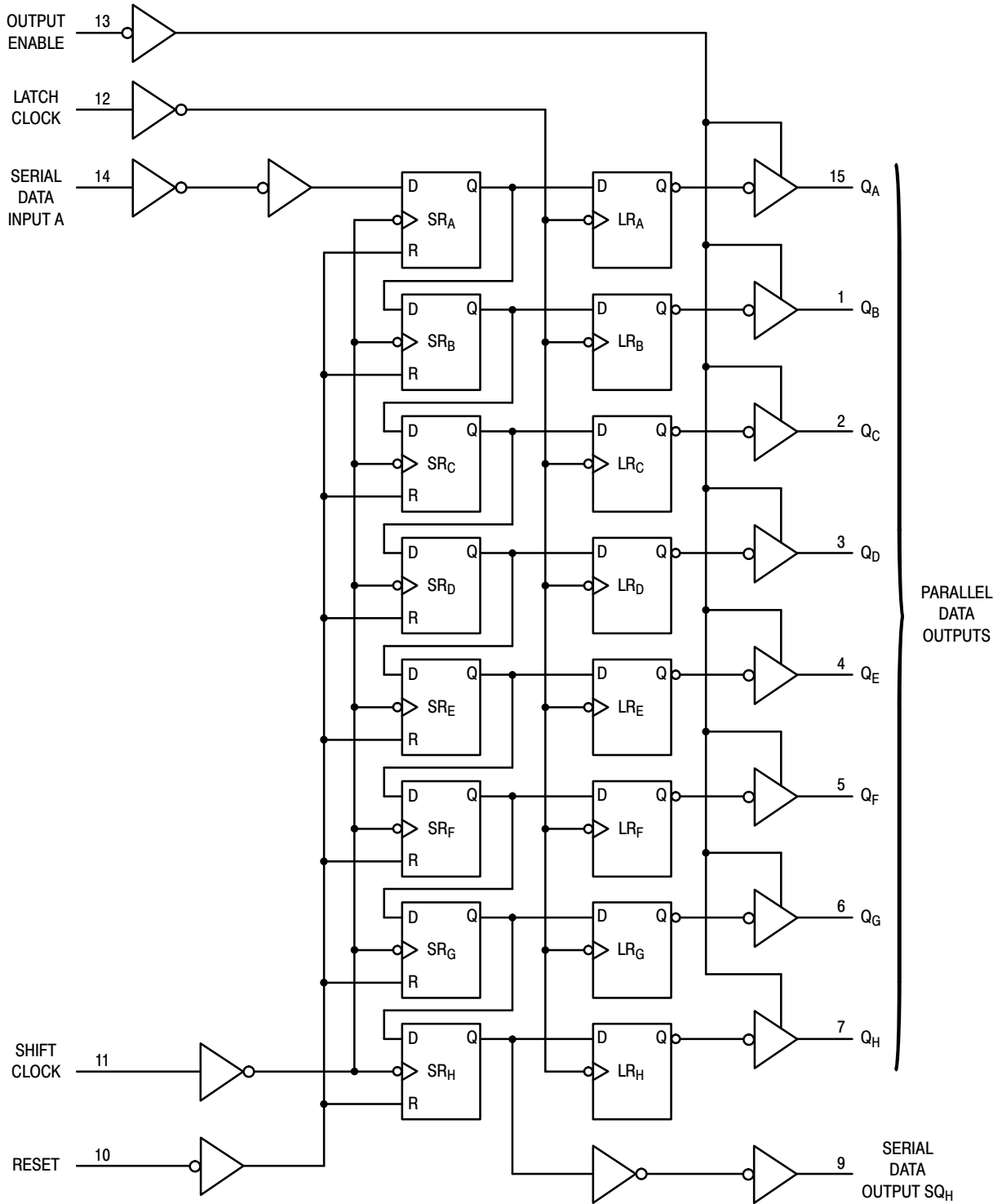


\*Includes all probe and jig capacitance

Figure 8.

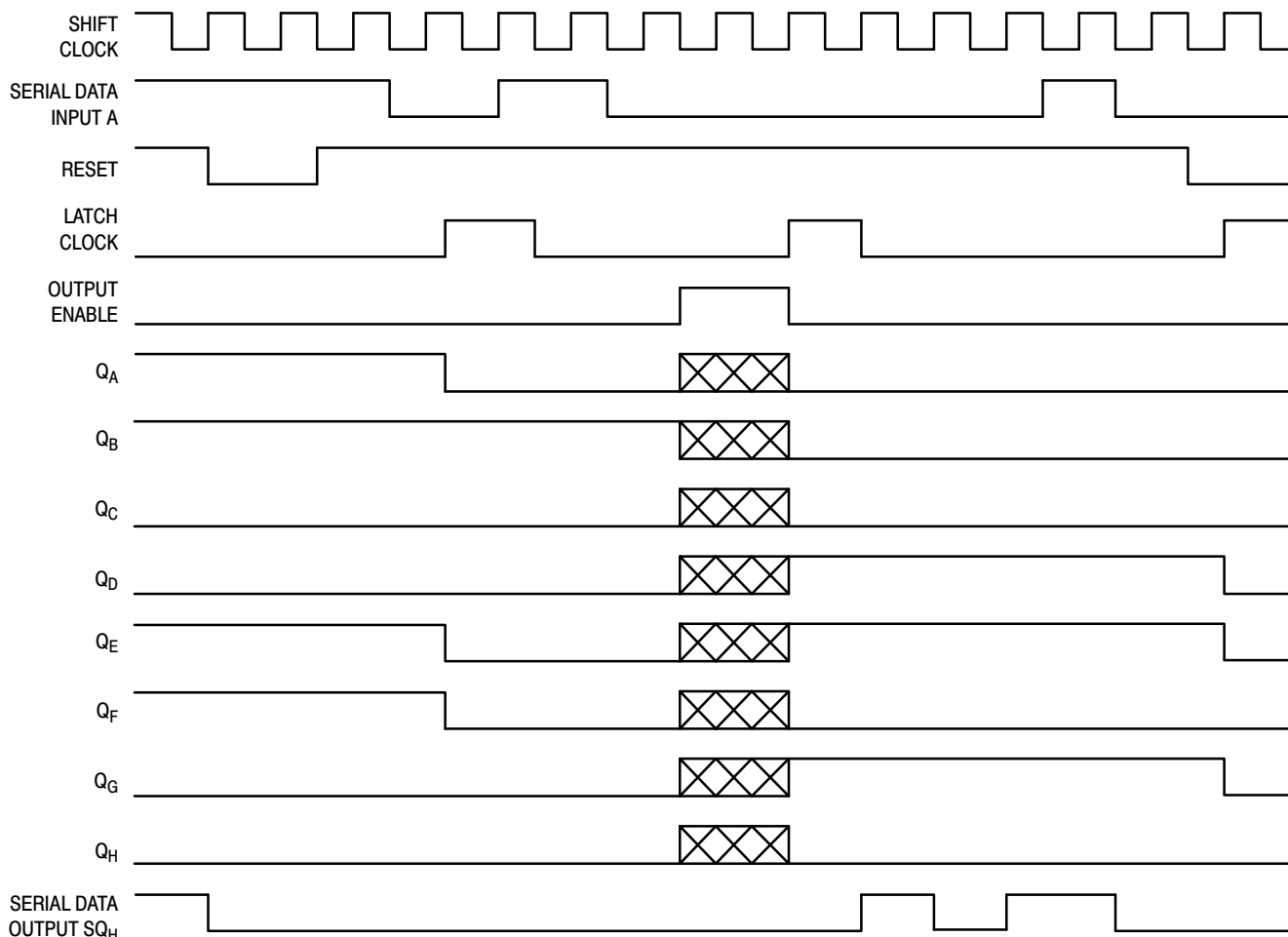
# MC74HC595A


## EXPANDED LOGIC DIAGRAM



# MC74HC595A

## TIMING DIAGRAM



NOTE:  implies that the output is in a high-impedance state.

### ORDERING INFORMATION

| Device              | Package               | Shipping <sup>†</sup> |
|---------------------|-----------------------|-----------------------|
| MC74HC595ADG        | SOIC-16<br>(Pb-Free)  | 48 Units / Rail       |
| NLV74HC595ADG*      |                       | 48 Units / Rail       |
| MC74HC595ADR2G      |                       | 2500 / Tape & Reel    |
| NLV74HC595ADR2G*    |                       | 2500 / Tape & Reel    |
| MC74HC595ADTG       | TSSOP-16<br>(Pb-Free) | 96 Units / Tube       |
| NLV74HC595ADTG*     |                       | 96 Units / Tube       |
| MC74HC595ADTR2G     |                       | 2500 / Tape & Reel    |
| NLV74HC595ADTR2G*   |                       | 2500 / Tape & Reel    |
| MC74HC595AMNTWG#    | QFN16<br>(Pb-Free)    | 3000 / Tape & Reel    |
| NLV74HC595AMNTWG*#  |                       | 3000 / Tape & Reel    |
| NLV74HC595AMN1TWG*# |                       | 3000 / Tape & Reel    |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

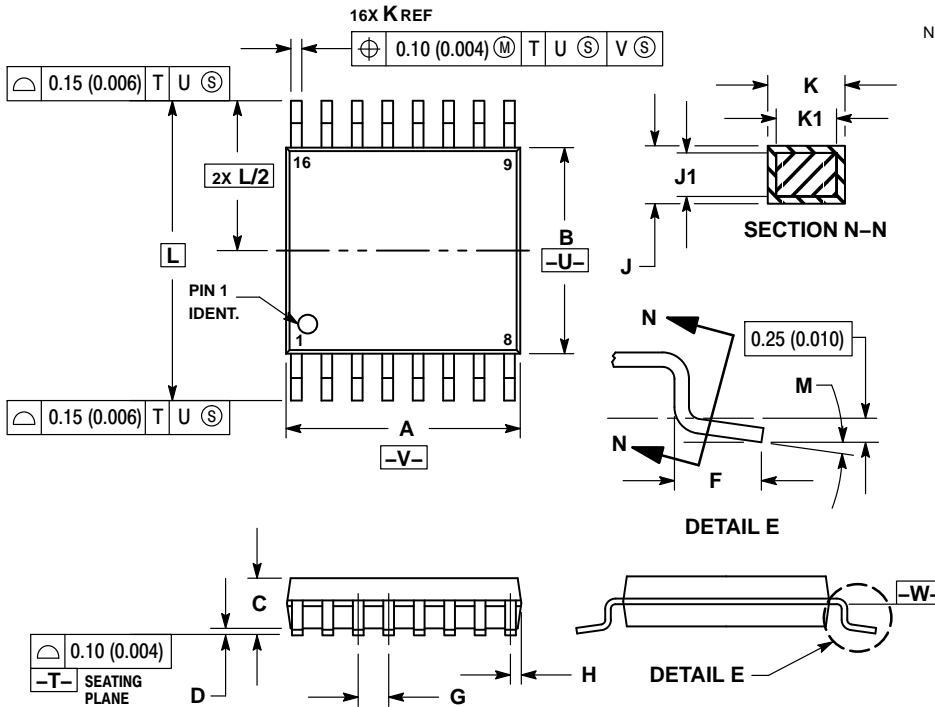
\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

#MN suffix is with pull-back lead, MN1 is without pull-back lead. Refer to 'Detail A' of case outline on page 13.

# MC74HC595A

## PACKAGE DIMENSIONS

TSSOP-16  
CASE 948F  
ISSUE B

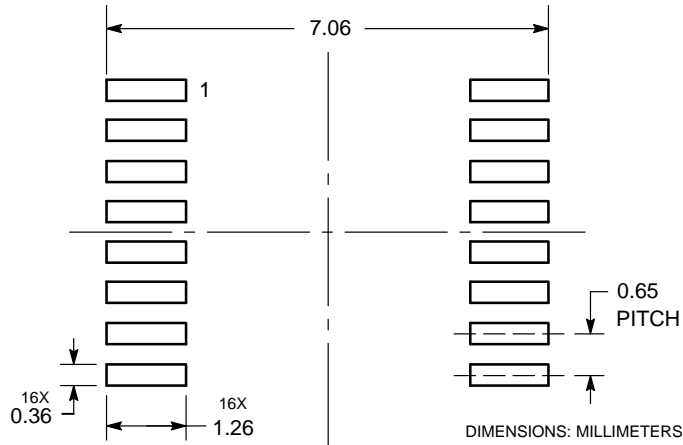


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.18        | 0.28 | 0.007     | 0.011 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

### SOLDERING FOOTPRINT\*

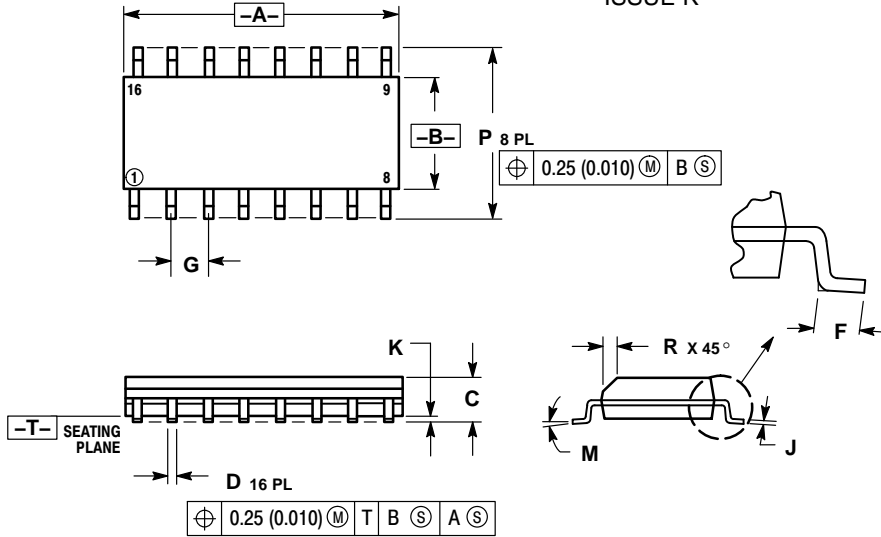


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MC74HC595A

## PACKAGE DIMENSIONS

SOIC-16  
CASE 751B-05  
ISSUE K

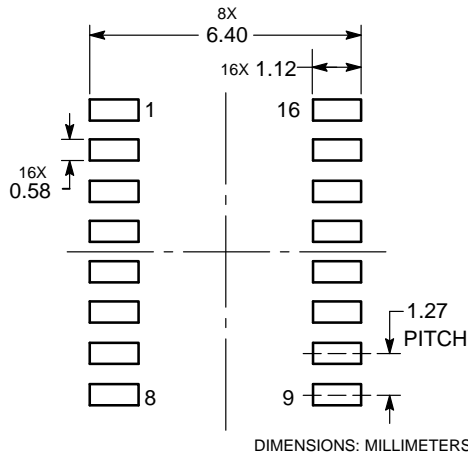


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 9.80        | 10.00 | 0.386     | 0.393 |
| B   | 3.80        | 4.00  | 0.150     | 0.157 |
| C   | 1.35        | 1.75  | 0.054     | 0.068 |
| D   | 0.35        | 0.49  | 0.014     | 0.019 |
| F   | 0.40        | 1.25  | 0.016     | 0.049 |
| G   | 1.27 BSC    |       | 0.050 BSC |       |
| J   | 0.19        | 0.25  | 0.008     | 0.009 |
| K   | 0.10        | 0.25  | 0.004     | 0.009 |
| M   | 0°          | 7°    | 0°        | 7°    |
| P   | 5.80        | 6.20  | 0.229     | 0.244 |
| R   | 0.25        | 0.50  | 0.010     | 0.019 |

### SOLDERING FOOTPRINT\*

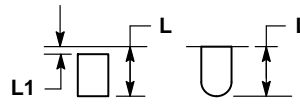
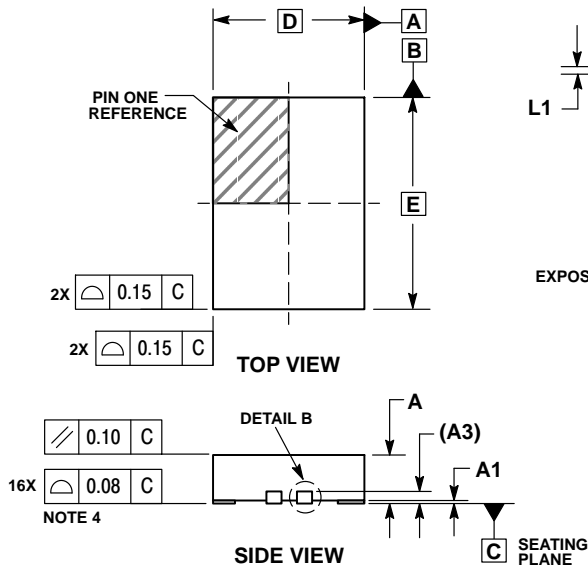


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MC74HC595A

## PACKAGE DIMENSIONS

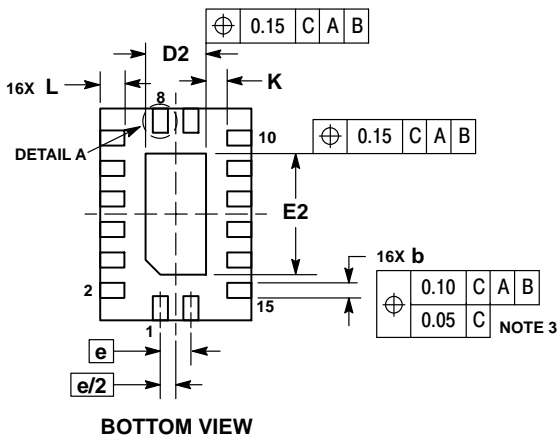
QFN16, 2.5x3.5, 0.5P  
CASE 485AW  
ISSUE O



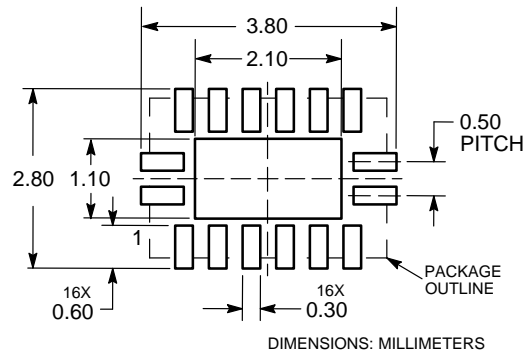
**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS |      |
|-----|-------------|------|
|     | MIN         | MAX  |
| A   | 0.80        | 1.00 |
| A1  | 0.00        | 0.05 |
| A3  | 0.20 REF    |      |
| b   | 0.20        | 0.30 |
| D   | 2.50 BSC    |      |
| D2  | 0.85        | 1.15 |
| E   | 3.50 BSC    |      |
| E2  | 1.85        | 2.15 |
| e   | 0.50 BSC    |      |
| K   | 0.20        | ---  |
| L   | 0.35        | 0.45 |
| L1  | ---         | 0.15 |



**SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marketing.pdf](http://www.onsemi.com/site/pdf/Patent-Marketing.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

**PUBLICATION ORDERING INFORMATION**

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local Sales Representative

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- ⊖ [View MC74HC595ADTR2G on WIN SOURCE](#)
- ⊖ [ON Semiconductor Information](#)

## Optimize Your Supply Chain with WIN SOURCE Solutions

- ✓ Global Sourcing Solution
- ✓ Obsolete Management
- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management