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MC68HC908RF2/D
Rev. 4
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Revision History

Revision History

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June, 2001	1.0	First bulleted paragraph under the subsection **11.5 Interrupts** reworded for clarity	137
		Revision to the description of the CHxMAX bit and the note that follows that description	145
		14.2 Absolute Maximum Ratings — ESD HBM and ESD MM entries added	171
		14.8 UHF Transmitter Module — Table entries and figures revised throughout	176
		14.11 LVI Characteristics — V_{LVS} and V_{LVR} specifications updated — low voltage reset and detection entries deleted	183
		14.12 Memory Characteristics — Maximum value for FLASH page program pulses updated	184
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		14.3 Functional Operating Range — Corrected oprating temperature range	172
		14.5 1.8-Volt to 3.3-Volt DC Electrical Characteristics Excluding UHF Module — Added values for Stop I_{DD} at –40°C to 125°C and corrected Note 1	173
		14.6 3.0-Volt DC Electrical Characteristics Excluding UHF Module — Added values for Stop I_{DD} at –40°C to 125°C and corrected Note 1	174
		14.7 2.0-Volt DC Electrical Characteristics Excluding UHF Module — Added values for Stop I_{DD} at –40°C to 125°C and corrected Note 1	175
		Table 15-1. MC Order Numbers — Added ordering information for –40°C to 125°C temperature range	185

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Section 1. General Description

1.1 Introduction

The MC68HC908RF2 MCU is a member of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). Optimized for low-power operation and available in a small 32-pin low-profile quad flat pack (LQFP), this MCU is well suited for remote keyless entry (RKE) transmitter designs.

All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

1.2 Features

Features MCU include:

- High-performance M68HC08 architecture
- Fully upward-compatible object code with M6805, M146805, and M68HC05 Families
- Maximum internal bus frequency of 4 MHz at 3.3 volts
- Maximum internal bus frequency of 2 MHz at 1.8 volts
- Internal oscillator requiring no external components:
  - Software selectable bus frequencies
  - ± 25 percent accuracy with trim capability to ±2 percent
  - Option to allow use of external clock source or external crystal/ceramic resonator
- 2 Kbytes of on-chip FLASH memory
- FLASH program memory security[1]
- 128 bytes of on-chip RAM
- 16-bit, 2-channel timer interface module (TIM)

1. No security feature is absolutely secure. However, Motorola's strategy is to make reading or copying the FLASH difficult for unauthorized users.

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- 12 general-purpose input/output (I/O) ports:
  - Six shared with keyboard wakeup function
  - Two shared with the timer module
  - Port A pins have 3-mA sink capabilities
- Low-voltage inhibit (LVI) module:
  - 1.85-V detection forces MCU into reset
  - 2.0-V detection sets indicator flag
- 6-bit keyboard interrupt with wakeup feature
- External asynchronous interrupt pin with internal pullup ($\overline{\text{IRQ}}$)
- Ultra high frequency (UHF) transmitter
- System protection features:
  - Computer operating properly (COP) reset
  - Low-voltage detection with reset
  - Illegal opcode detection with reset
  - Illegal address detection with reset
- 32-pin plastic LQFP package
- Low-power design with stop and wait modes
- Master reset pin and power-on reset (POR)
- –40°C to 85°C and –40°C to 125°C operation

Features of the CPU08 include:

- Enhanced HC05 programming model
- Extensive loop control functions
- 16 addressing modes (eight more than the HC05)
- 16-bit index register and stack pointer
- Memory-to-memory data transfers
- Fast 8 × 8 multiply instruction
- Fast 16/8 divide instruction
- Binary-coded decimal (BCD) instructions
- Optimization for controller applications
- Third party C language support

1.3 MCU Block Diagram

Figure 1-1 shows the structure of the MC68HC908RF2 MCU.

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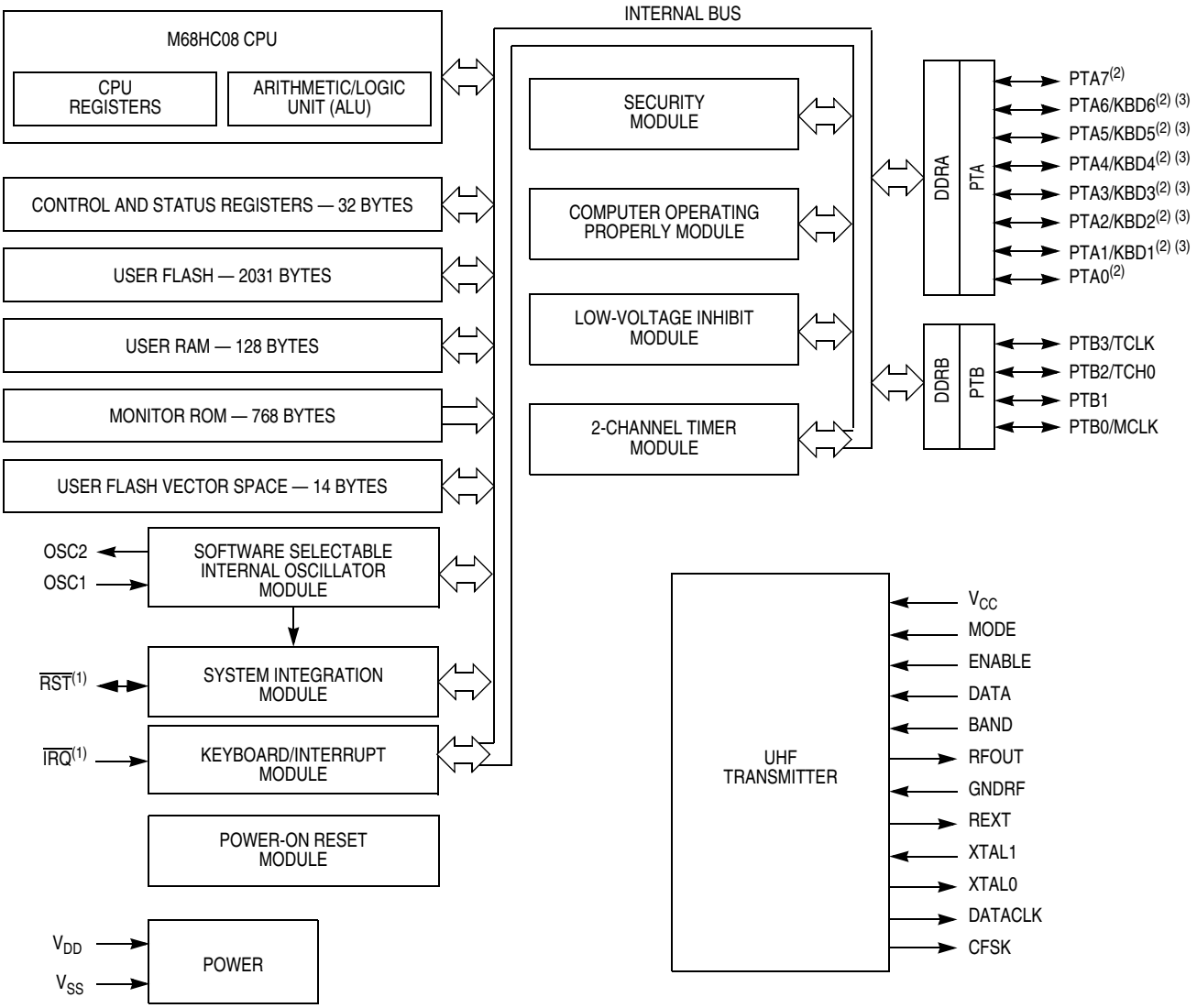

1. Pin contains integrated pullup resistor
2. High current sink pin
3. Pin contains software selectable pullup resistor

Figure 1-1. MC68HC908RF2 MCU Block Diagram

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1.4 Pin Assignments

Figure 1-2 shows the pin assignments.

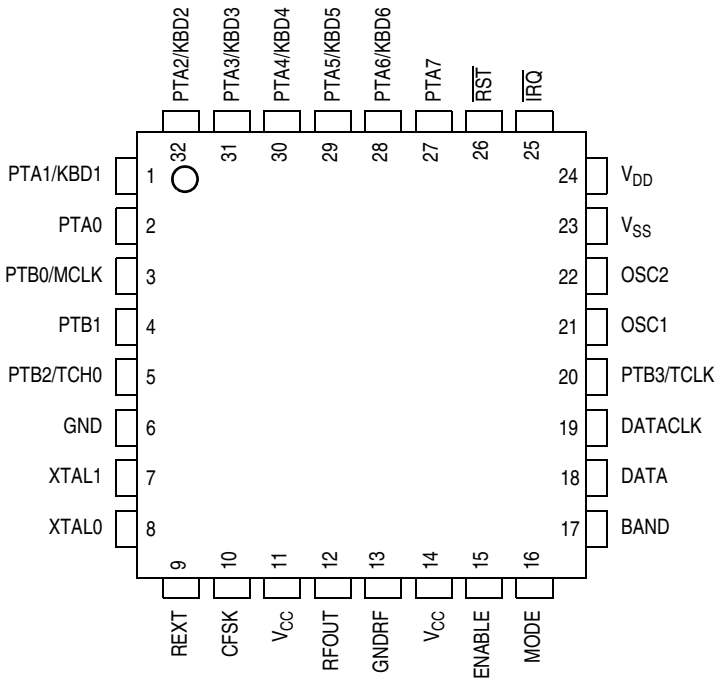

Figure 1-2. LQFP Pin Assignments

1.4.1 Power Supply Pins (V_{DD} and V_{SS})

V_{DD} and V_{SS} are the power supply and ground pins. The MCU operates from a single power supply.

Fast signal transitions on MCU pins place high, short-duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU as shown in **Figure 1-3**. Place the bypass capacitors as close to the MCU power pins as possible. Use high-frequency-response ceramic capacitors for C_{Bypass}. C_{Bulk} are optional bulk current bypass capacitors for use in applications that require the port pins to source high-current levels.

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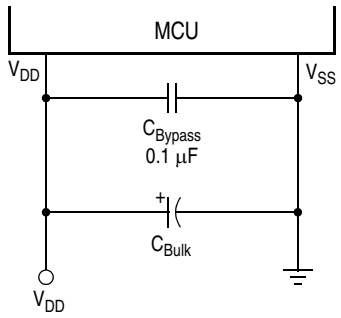

Note: Component values shown represent typical applications.

Figure 1-3. Power Supply Bypassing

1.4.2 Oscillator Pins (OSC1 and OSC2)

The OSC1 and OSC2 pins are the connections to an external clock source or crystal/ceramic resonator.

1.4.3 External Reset ($\overline{\text{RST}}$)

A logic 0 on the $\overline{\text{RST}}$ pin forces the MCU to a known startup state. $\overline{\text{RST}}$ is bidirectional, allowing a reset of the entire system. It is driven low when any internal reset source is asserted.

The $\overline{\text{RST}}$ pin contains an internal pullup resistor.

For additional information, see **Section 10. System Integration Module (SIM)**.

1.4.4 External Interrupt Pin ($\overline{\text{IRQ}}$)

$\overline{\text{IRQ}}$ is an asynchronous external interrupt pin.

The $\overline{\text{IRQ}}$ pin contains an internal pullup resistor.

1.4.5 Port A Input/Output Pins (PTA7, PTA6/KBD6–PTA1/KBD1, and PTA0)

Port A is an 8-bit special function port that shares its pins with the keyboard interrupt.

Six port A pins (PTA6–PTA1) can be programmed to serve as an external interrupt. Once enabled, that pin will contain an internal pullup resistor.

All port A pins are high-current sink pins.

1.4.6 Port B Input/Output Pins (PTB3/TCLK, PTB2/TCH0, PTB1, and PTB0/MCLK)

Port B is a 4-bit, general-purpose, bidirectional I/O port, with some of its pins shared with the timer (TIM) module.

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1.4.7 UHF Transmitter Pins

The MC68HC908RF2 uses dedicated pins for its UHF module. These pins are described in **Table 1-1**.

Table 1-1. UHF Transmitter Pins

Pin	Function	Description
6	GND	Ground
7	XTAL1	Reference oscillator input
8	XTAL0	Reference oscillator output
9	REXT	Output amplifier current setting resistor
10	CFSK	FSK switch output
11	V_{CC}	Power supply
12	RFOUT	Power amplifier output
13	GNDRF	Power amplifier ground
14	V_{CC}	Power supply
15	ENABLE	Enable input
16	MODE	Modulation type selection input
17	BAND	Frequency band selection
18	DATA	Data input
19	DATACLK	Clock output to the microcontroller

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Section 2. Memory

2.1 Introduction

The memory map, shown in **Figure 2-1**, includes:

- 2031 bytes of user FLASH memory
- 128 bytes of random-access memory (RAM)
- 14 bytes of user-defined vectors in FLASH memory
- 768 bytes of monitor read-only memory (ROM)

These definitions apply to the memory map representation of reserved and unimplemented locations:

- Reserved — Accessing a reserved location can have unpredictable effects on MCU operation.
- Unimplemented — Accessing an unimplemented location causes an illegal address reset.

2.2 Input/Output Section

Addresses $0000–$003F, shown in **Figure 2-2**, contain most of the control, status, and data registers. Additional I/O registers have these addresses:

- $FE00 — SIM break status register, SBSR
- $FE01 — SIM reset status register, SRSR
- $FE02 — SIM break flag control register, BFCR
- $FE08 — FLASH control register, FLCR
- $FE0C — BREAK address register high, BRKH
- $FE0D — BREAK address register low, BRKL
- $FE0E — BREAK status and control register, BSCR
- $FE0F — LVI status register, LVISR
- $FFF0 — FLASH block protection register, FLBPR
- $FFFF — COP control register, COPCTL

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$0000 ↓ $003F	I/O REGISTERS (28 BYTES)
$0040 ↓ $007F	UNIMPLEMENTED (64 BYTES)
$0080 ↓ $00FF	RAM (128 BYTES)
$0100 ↓ $77FF	UNIMPLEMENTED (30,464 BYTES)
$7800 ↓ $7FEE	FLASH MEMORY (2031 BYTES)
$7FEF	OPTIONAL FACTORY DETERMINED ICG TRIM VALUE(1)
$7FF0 ↓ $EFFF	UNIMPLEMENTED (28,688 BYTES)
$F000 ↓ $F2EF	MONITOR ROM (752 BYTES)
$F2F0 ↓ $FDFF	UNIMPLEMENTED (2832 BYTES)
$FE00	SIM BREAK STATUS REGISTER (SBSR)
$FE01	SIM RESET STATUS REGISTER (SRSR)
$FE02	SIM BREAK FLAG CONTROL REGISTER (SBFCR)
$FE03 ↓ $FE06	RESERVED (4 BYTES)
$FE07	UNIMPLEMENTED (1 BYTE)
$FE08	FLASH CONTROL REGISTER (FLCR)
$FE09	RESERVED
$FE0A ↓ $FE0B	UNIMPLEMENTED (2 BYTES)
$FE0C	BREAK ADDRESS REGISTER HIGH (BRKH)
$FE0D	BREAK ADDRESS REGISTER LOW (BRKL)

1. Address $7FEF is reserved for an optional factory-determined ICG trim value. Consult with a local Motorola representative for more information and availability of this option.

Figure 2-1. Memory Map

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$FE0E	BREAK STATUS AND CONTROL REGISTER (BSCR)
$FE0F	LVI STATUS REGISTER (LVISR)
$FE10 ↓ $FEEF	UNIMPLEMENTED (222 BYTES)
$FEF0 ↓ $FEFF	MONITOR ROM (16 BYTES)
$FF00 ↓ $FFEF	UNIMPLEMENTED (240 BYTES)
$FFF0	FLASH BLOCK PROTECT REGISTER (FLBPR)
$FFF1	RESERVED
$FFF2 ↓ $FFFF	FLASH VECTORS (14 BYTES)

Figure 2-1. Memory Map (Continued)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0000	Port A Data Register (PTA) See page 108.	Read: Write:	PTA7	PTA6	PTA5	PTA4	PTA3	PTA2	PTA1	PTA0
		Reset:	Unaffected by reset							
$0001	Port B Data Register (PTB) See page 110.	Read: Write:					PTB3	PTB2	PTB1	PTB0
		Reset:	Unaffected by reset							
$0002 ↓ $0003	Unimplemented									
$0004	Data Direction Register A (DDRA) See page 109.	Read: Write:	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
		Reset:	0	0	0	0	0	0	0	0
$0005	Data Direction Register B (DDRB) See page 111.	Read:	MCLKEN	0			DDRB3	DDRB2	DDRB1	DDRB0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0006 ↓ $0019	Unimplemented									

= Unimplemented R = Reserved U = Unaffected X = Indeterminate

Figure 2-2. Control, Status, and Data Registers (Sheet 1 of 5)

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Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$001A	IRQ and Keyboard Status and Control Register (INTKBSCR) See page 101.	Read:	IRQF	0	IMASKI	MODEI	KEYF	0	IMASKK	MODEK
		Write:	R	ACKI			R	ACKK		
		Reset:	0	0	0	0	0	0	0	0
$001B	Keyboard Interrupt Enable Register (INTKBIER) See page 102.	Read:	0	KBIE6	KBIE5	KBIE4	KBIE3	KBIE2	KBIE1	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$001C ↓ $001E	Unimplemented									
$001F	Configuration Register (CONFIG) See page 43.	Read: Write:	EXTSLOW	LVISTOP	LVIRST	LVIPWR	COPRS	SSREC	STOP	COPD
		Reset:	0	0	1	1	0	0	0	0
$0020	Timer Status and Control Register (TSC) See page 143.	Read:	TOF	TOIE	TSTOP	0	0	PS2	PS1	PS0
		Write:	0			TRST				
		Reset:	0	0	1	0	0	0	0	0
$0021	Timer Counter Register High (TCNTH) See page 141.	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0022	Timer Counter Register Low (TCNTL) See page 141.	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0023	Timer Counter Modulo Register High (TMODH) See page 142.	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
		Reset:	1	1	1	1	1	1	1	1
$0024	Timer Counter Modulo Register Low (TMODL) See page 142.	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
		Reset:	1	1	1	1	1	1	1	1
$0025	Timer Channel 0 Status and Control Register (TSC0) See page 143.	Read:	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	TOV0	CH0MAX
		Write:	0							
		Reset:	0	0	0	0	0	0	0	0
$0026	Timer Channel 0 Register High (TCH0H) See page 146.	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
		Reset:	Indeterminate after reset							
$0027	Timer Channel 0 Register Low (TCH0L) See page 146.	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
		Reset:	Indeterminate after reset							

= Unimplemented R = Reserved U = Unaffected X = Indeterminate

Figure 2-2. Control, Status, and Data Registers (Sheet 2 of 5)

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Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0028	Timer Channel 1 Status and Control Register (TSC1) See page 143.	Read:	CH1F	CH1IE	0	MS1A	ELS1B	ELS1A	TOV1	CH1MAX
		Write:	0							
		Reset:	0	0	0	0	0	0	0	0
$0029	Timer Channel 1 Register High (TCH1H) See page 146.	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	Indeterminate after reset							
$002A	Timer Channel 1 Register Low (TCH1L) See page 146.	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	Indeterminate after reset							
$002B ↓ $0035	Unimplemented									
$0036	Internal Clock Generator Control Register (ICGCR) See page 88.	Read:	CMIE	CMF	CMON	CS	ICGON	ICGS	ECGON	ECGS
		Write:								
		Reset:	0	0	0	0	1	0	0	0
$0037	Internal Clock Generator Multiplier Register (ICGMR) See page 90.	Read:	R	N6	N5	N4	N3	N2	N1	N0
		Write:								
		Reset:	0	0	0	1	0	1	0	1
$0038	Internal Clock Generator Trim Register (ICGTR) See page 90.	Read:	TRIM7	TRIM6	TRIM5	TRIM4	TRIM3	TRIM2	TRIM1	TRIM0
		Write:								
		Reset:	1	0	0	0	0	0	0	0
$0039	ICG DCO Divider Control Register (ICGDVR) See page 91.	Read:	R	R	R	R	DDIV3	DDIV2	DDIV1	DDIV0
		Write:								
		Reset:	0	0	0	0	U	U	U	U
$003A	ICG DCO Stage Register (ICGDSR) See page 91.	Read:	DSTG7	DSTG6	DSTG5	DSTG4	DSTG3	DSTG2	DSTG1	DSTG0
		Write:								
		Reset:	Unaffected by reset							
$003B	Reserved		R	R	R	R	R	R	R	R
$003C ↓ $003F	Unimplemented									
$FE00	SIM Break Status Register (SBSR) See page 126.	Read:	R	R	R	R	R	R	SBSW	R
		Write:							See Note	
		Reset:							0	

Note: Writing a 0 clears SBSW

= Unimplemented R = Reserved U = Unaffected X = Indeterminate

Figure 2-2. Control, Status, and Data Registers (Sheet 3 of 5)

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Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$FE01	SIM Reset Status Register (SRSR) See page 127.	Read:	POR	PIN	COP	ILOP	ILAD	0	LVI	0
		Write:								
		POR:	1	X	X	X	X	X	X	X
$FE02	SIM Break Flag Control Register (SBFCR) See page 128.	Read:	BCFE	R	R	R	R	R	R	R
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$FE03 ↓ $FE04	Reserved		R	R	R	R	R	R	R	R
$FE05 ↓ $FE07	Unimplemented									
$FE08	FLASH 2TS Control Register (FLCR) See page 29.	Read:	0	FDIV0	BLK1	BLK0	HVEN	MARGIN	ERASE	PGM
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$FE09	Reserved		R	R	R	R	R	R	R	R
$FE0A ↓ $FE0B	Unimplemented									
$FE0C	Break Address Register High (BRKH) See page 161.	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$FE0D	Break Address Register Low (BRKL) See page 161.	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$FE0E	Break Status and Control Register (BSCR) See page 160.	Read:	BRKE	BRKA	0	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$FE0F	LVI Status Register (LVISR) See page 105.	Read:	LVIOUT	0	LOWV	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented R = Reserved U = Unaffected X = Indeterminate

Figure 2-2. Control, Status, and Data Registers (Sheet 4 of 5)

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Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$FFF0	FLASH 2TS Block Protect Register (FLBPR)† See page 34.	Read: Write:	R	R	R	R	BPR3	BPR2	BPR1	BPR0
		Reset:	Unaffected by reset							

† Non-volatile FLASH register

$FFFF	COP Control Register (COPCTL) See page 49.	Read:	LOW BYTE OF RESET VECTOR
		Write:	WRITING CLEARS COP COUNTER (ANY VALUE)
		Reset:	Unaffected by reset

= Unimplemented R = Reserved U = Unaffected X = Indeterminate

Figure 2-2. Control, Status, and Data Registers (Sheet 5 of 5)

Table 2-1 is a list of vector locations.

Table 2-1. Vector Locations

	Address	Vector
Low	$FFF2	ICG vector (high)
	$FFF3	ICG vector (low)
	$FFF4	TIM overflow vector (high)
	$FFF5	TIM overflow vector (low)
	$FFF6	TIM channel 1 vector (high)
	$FFF7	TIM channel 1 vector (low)
Priority	$FFF8	TIM channel 0 vector (high)
	$FFF9	TIM channel 0 vector (low)
	$FFFA	IRQ/keyboard vector (high)
	$FFFB	IRQ/keyboard vector (low)
	$FFFC	SWI vector (high)
	$FFFD	SWI vector (low)
High	$FFFE	Reset vector (high)
	$FFFF	Reset vector (low)

2.3 Monitor ROM

The 768 bytes at addresses $F000–F2EF and $FEF0–$FEFF are utilized by the monitor ROM.

The address range $F000–F2EF is reserved for the monitor code functions, FLASH memory programming, and erase algorithms.

The address range $FEF0–$FEFF holds reserved ROM addresses that contain the monitor code reset vectors.

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2.4 Random-Access Memory (RAM)

Addresses $0080–$00FF are RAM locations. The location of the stack RAM is programmable.

NOTE: *For correct operation, the stack pointer must point only to RAM locations.*

Before processing an interrupt, the CPU uses five bytes of the stack to save the contents of the CPU registers.

NOTE: *For M68HC05, M6805, and M146805 compatibility, the H register is not stacked.*

During a subroutine call, the CPU uses two bytes of the stack to store the return address. The stack pointer decrements during pushes and increments during pulls.

NOTE: *Be careful when using nested subroutines. The CPU could overwrite data in the RAM during a subroutine or during the interrupt stacking operation.*

2.5 FLASH 2TS Memory

This section describes the operation of the embedded FLASH 2TS memory. This memory can be read, programmed, and erased from a single external supply. The program and erase operations are enabled through the use of an internal charge pump.

The FLASH 2TS memory is appropriately named to describe its 2-transistor source-select bit cell. The FLASH 2TS memory is an array of 2031 bytes with an additional 14 bytes of user vectors and one byte for block protection. An erased bit reads as a 0 and a programmed bit reads as a 1.

The address ranges for the user memory, control register, and vectors are:

- $7800–$7FEE, user space
- $7FEF, reserved — optional ICG trim value, see **6.7.3 ICG Trim Register**
- $FFF0, block protect register
- $FE08, FLASH 2TS control register
- $FFF2–$FFFF, these locations are reserved for user-defined interrupt and reset vectors

This list is the row architecture for the user space array:

$7800–$7807 (Row 0)

$7808–$780F (Row 1)

$7810–$7817 (Row 2)

$7818–$781F (Row 3)

$7820–$7827 (Row 4)

$7FE8–$7FEF (Row 253)

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Program and erase operations are facilitated through control bits in a memory mapped register. Details for these operations appear later in this section. Memory in the FLASH 2TS array is organized into pages within rows. For the 2-Kbyte array on the MC68HC908RF2, the page size is one byte. There are eight pages (or eight bytes) per row. Programming operations are performed on a page basis, one byte at a time. Erase operations are performed on a block basis. The minimum block size is one row of eight bytes. Refer to **Table 2-3** for additional block size options.

NOTE: *Sometimes a program disturb condition, in which case an erased bit on the row being programmed unintentionally becomes programmed, occurs. The embedded smart programming algorithm implements a margin read technique to avoid program disturb. The margin read step of the smart programming algorithm is used to ensure programmed bits are programmed to sufficient margin for data retention over the device's lifetime. In the application code, perform an erase operation after eight program operations (on the same row) to further avoid program disturb.*

For availability of programming tools and more information, contact a local Motorola representative.

NOTE: *A security feature prevents viewing of the FLASH 2TS contents.*[1]

2.5.1 FLASH 2TS Control Register

The FLASH 2TS control register (FLCR) controls program, erase, and margin read operations.

Address: $FE08

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	FDIV0	BLK1	BLK0	HVEN	MARGIN	ERASE	PGM
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 2-3. FLASH 2TS Control Register (FLCR)

FDIV0 — Frequency Divide Control Bit

This read/write bit selects the factor by which the charge pump clock is divided from the system clock. See **2.5.2 FLASH 2TS Charge Pump Frequency Control**.

BLK1 — Block Erase Control Bit

This read/write bit together with BLK0 allows erasing of blocks of varying size. See **2.5.3 FLASH 2TS Erase Operation** for a description of available block sizes.

1. No security feature is absolutely secure. However, Motorola's strategy is to make reading or copying the FLASH 2TS difficult for unauthorized users.

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BLK0 — Block Erase Control Bit

This read/write bit together with BLK1 allows erasing of blocks of varying size. See **2.5.3 FLASH 2TS Erase Operation** for a description of available block sizes.

HVEN — High-Voltage Enable Bit

This read/write bit enables the charge pump to drive high voltages for program and erase operations in the array. HVEN can be set only if either PGM = 1 or ERASE = 1 and the proper sequence for smart programming or erase is followed.

1 = High voltage enabled to array and charge pump on
0 = High voltage disabled to array and charge pump off

MARGIN — Margin Read Control Bit

This read/write bit configures the memory for margin read operation. MARGIN cannot be set if the HVEN = 1. MARGIN will automatically return to unset (0) if asserted when HVEN = 1.

1 = Margin read operation selected
0 = Margin read operation unselected

ERASE — Erase Control Bit

This read/write bit configures the memory for erase operation. ERASE is interlocked with the PGM bit such that both bits cannot be set at the same time.

1 = Erase operation selected
0 = Erase operation unselected

PGM — Program Control Bit

This read/write bit configures the memory for program operation. PGM is interlocked with the ERASE bit such that both bits cannot be set at the same time.

1 = Program operation selected
0 = Program operation unselected

2.5.2 FLASH 2TS Charge Pump Frequency Control

The internal charge pump, required for program, margin read, and erase operations, is designed to operate most efficiently with a 2-MHz clock. The charge pump clock is derived from the bus clock. **Table 2-2** shows how the FDIV bits are used to select a charge pump frequency based on the bus clock frequency. Program, margin read, and erase operations cannot be performed if the bus clock frequency is below 2 MHz.

Table 2-2. Charge Pump Clock Frequency

FDIV0	Pump Clock Frequency
0	Bus frequency ÷ 1
1	Bus frequency ÷ 2

NOTE: *The charge pump is optimized for 2-MHz operation.*

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2.5.3 FLASH 2TS Erase Operation

Use this step-by-step procedure to erase a block of FLASH 2TS memory. Refer to **14.12 Memory Characteristics** for a detailed description of the times used in this algorithm.

1. Set the ERASE, BLK0, BLK1, and FDIV0 bits in the FLASH 2TS control register. Refer to **Table 2-2** for FDIV settings and to **Table 2-3** for block sizes.
2. Ensure target portion of array is unprotected by reading the block protect register at address $FFF0. Refer to **2.5.5 FLASH 2TS Block Protection** and **2.5.6 FLASH 2TS Block Protect Register** for more information.
3. Write to any FLASH 2TS address with any data within the block address range desired.
4. Set the HVEN bit.
5. Wait for a time, t_{Erase}.
6. Clear the HVEN bit.
7. Wait for a time, t_{Kill}, for the high voltages to dissipate.
8. Clear the ERASE bit.
9. After a time, t_{HVD}, the memory can be accessed in read mode again.

NOTE: *While these operations must be performed in the order shown, other unrelated operations may occur between the steps.*

Table 2-3 shows the various block sizes which can be erased in one erase operation.

Table 2-3. Erase Block Sizes

BLK1	BLK0	Block Size, Addresses Cared
0	0	Full array: 2 Kbytes
0	1	One-half array: 1 Kbyte
1	0	Eight rows: 64 bytes
1	1	Single row: 8 bytes

In step 3 of the erase operation, the cared addresses are latched and used to determine the location of the block to be erased. For instance, with BLK0 = BLK1 = 0, writing to any FLASH 2TS address in the range $7800 to $78F0 will enable the erase of all FLASH memory.

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2.5.4 FLASH 2TS Program/Margin Read Operation

NOTE: *After a total of eight program operations have been applied to a row, the row must be erased before further programming to avoid program disturb. An erased byte will read $00.*

The FLASH 2TS memory is programmed on a page basis. A page consists of one byte. The smart programming algorithm (**Figure 2-4**) is recommended to program every page in the FLASH 2TS memory.

The embedded smart programming algorithm uses this step-by-step sequence to program the data into the FLASH memory. The algorithm optimizes the time required to program each page. Refer to **2.5.7 Embedded Program/Erase Routines** for information on utilizing embedded routines.

1. Set the FDIV bits. These bits determine the charge pump frequency.
2. Set PGM = 1. This configures the memory for program operation and enables the latching of address and data for programming.
3. Read the FLASH 2TS block protect register (FLBPR).
4. Write data to the one byte being programmed.
5. Set HVEN = 1.
6. Wait for a time, t_{Step}.
7. Set HVEN = 0.
8. Wait for a time, t_{HVTV}.
9. Set MARGIN = 1.
10. Wait for a time, t_{VTP}.
11. Set PGM = 0.
12. Wait for a time, t_{HVD}.
13. Read back data in margin read mode. This read operation is stretched by eight cycles.
14. Clear the MARGIN bit. If the margin read data is identical to write data, the program operation is complete; otherwise, jump to step 2.

NOTE: *While these operations must be performed in the order shown, other unrelated operations may occur between the steps.*

The smart programming algorithm guarantees the minimum possible program time.

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Page Program/Margin Read Procedure

Note: This algorithm is mandatory for programming the FLASH 2TS.

Note: This page program algorithm assumes the page/s to be programmed are initially erased.

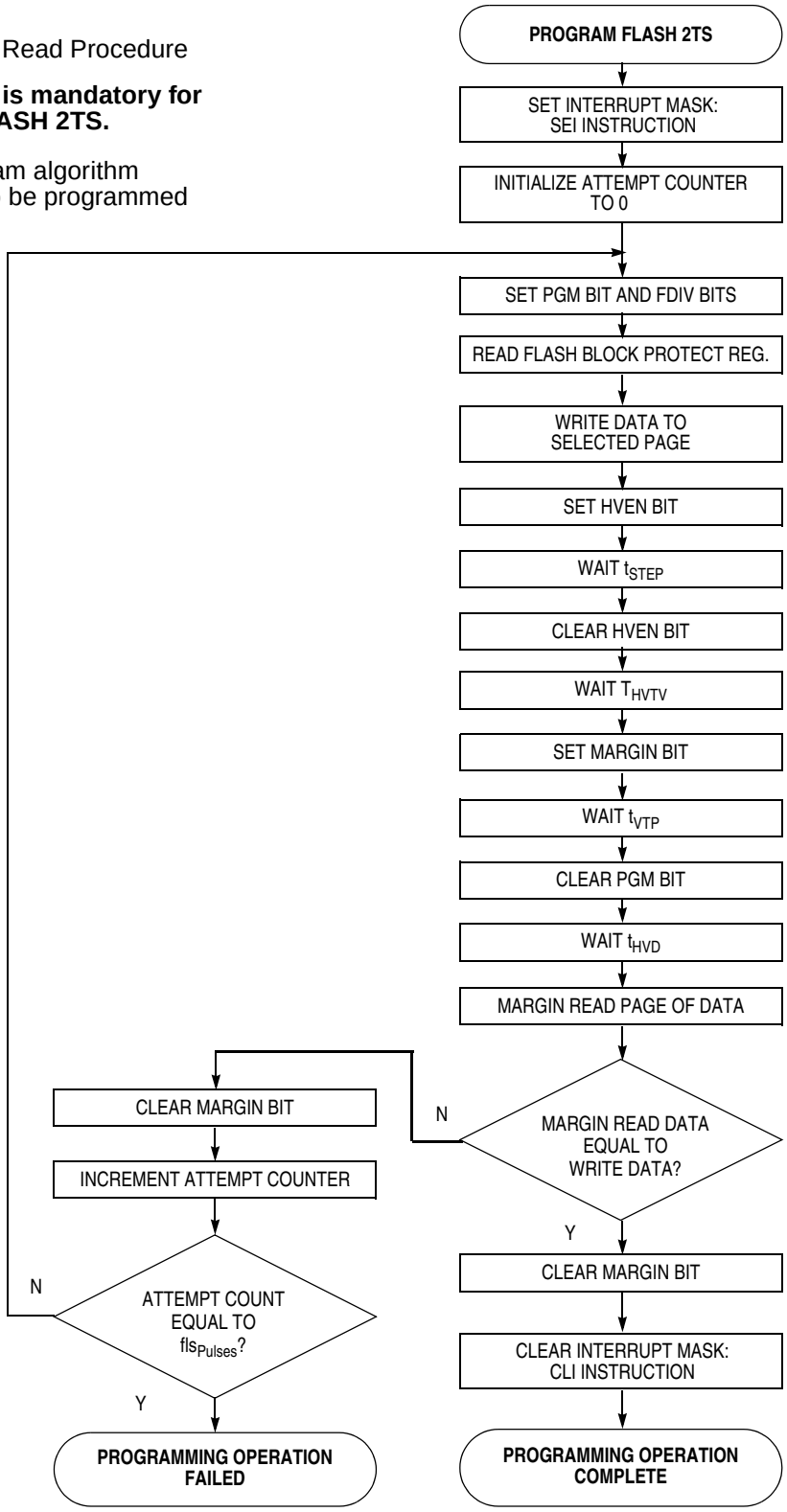

Figure 2-4. Smart Programming Algorithm Flowchart

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2.5.5 FLASH 2TS Block Protection

NOTE: *In performing a program or erase operation, the FLASH 2TS block protect register must be read after setting the PGM or ERASE bit and before asserting the HVEN bit.*

Due to the ability of the on-board charge pump to erase and program the FLASH 2TS memory in the target application, provision is made for protecting blocks of memory from unintentional erase or program operations due to system malfunction. This protection is implemented by a reserved location in the memory for block protect information. This block protect register must be read before setting HVEN = 1. When the block protect register is read, its contents are latched by the FLASH 2TS control logic. If the address range for an erase or program operation includes a protected block, the PGM or ERASE bit is cleared which prevents the HVEN bit in the FLASH 2TS control register from being set such that no high-voltage operation is allowed in the array.

When the block protect register is erased (all 0s), the entire memory is accessible for program and erase. When bits within the register are programmed, they lock blocks of memory address ranges as shown in **2.5.6 FLASH 2TS Block Protect Register**. The block protect register itself can be erased or programmed only with an external voltage V_{TST} present on the $\overline{IRQ}$ pin. The presence of V_{TST} on the $\overline{IRQ}$ pin also allows entry into monitor mode out of reset. Therefore, the ability to change the block protect register is voltage-level dependent and can occur in either user or monitor modes.

2.5.6 FLASH 2TS Block Protect Register

The block protect register (FLBPR) is implemented as a byte within the FLASH 2TS memory. Each bit, when programmed, protects a range of addresses in the FLASH 2TS.

Address: $FFF0

	Bit 7	6	5	4	3	2	1	Bit 0
Read: / Write:	R	R	R	R	BPR3	BPR2	BPR1	BPR0
Reset:	Unaffected by reset							

R = Reserved

Figure 2-5. FLASH 2TS Block Protect Register (FLBPR)

BPR3 — Block Protect Register Bit 3

This bit protects the memory contents in the address ranges $7A00–$7FEF and $FFF0–$FFFF.

1 = Address range protected from erase or program

0 = Address range open to erase or program

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BPR2 — Block Protect Register Bit 2
This bit protects the memory contents in the address ranges $7900–$7FEF and $FFF0–$FFFF.
1 = Address range protected from erase or program
0 = Address range open to erase or program

BPR1 — Block Protect Register Bit 1
This bit protects the memory contents in the address ranges $7880–$7FEF and $FFF0–$FFFF.
1 = Address range protected from erase or program
0 = Address range open to erase or program

BPR0 — Block Protect Register Bit 0
This bit protects the FLASH memory contents in the address ranges $7800–$7FEF and $FFF0–$FFFF.
1 = Address range protected from erase or program
0 = Address range open to erase or program

By programming the block protect bits, a portion of the memory will be locked so that no further erase or program operations may be performed. Programming more than one bit at a time is redundant. If both bit 1 and bit 2 are set, for instance, the FLASH address ranges between $7880–$FFFF are locked. If all bits are erased, then all of the memory is available for erase and program.

The presence of a voltage V_{TST} on the $\overline{IRQ}$ pin will bypass the block protection so that all of memory, including the block protect register, can be programmed or erased.

2.5.7 Embedded Program/Erase Routines

The MC68HC908RF2 monitor ROM contains numerous routines for programming and erasing the FLASH memory. These embedded routines are intended to assist the programmer with modifying the FLASH memory array. These routines will implement the smart programming algorithm as defined in **Figure 2-4**. The functions are listed in **Table 2-4**

Table 2-4. Embedded FLASH Routines

Function Description	Call	JSR to Address[1]
Read/verify a range	RDVRRNG	ROMSTRT + 0
Program range of FLASH	PRGRNGE	ROMSTRT + 3
Erase range of FLASH	ERARNGE	ROMSTRT + 6
Redundant program FLASH	REDPROG	ROMSTRT + 9

1. ROMSTRT is defined as the starting address of the monitor ROM in the memory map. This is address $F000.

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The functions shown in **Table 2-4** accept data through the CPU registers and global variables in RAM. **Table 2-5** shows the RAM locations that are used for passing parameters.

Table 2-5. Embedded FLASH Routine Global Variables

Variable Location	Variable Address(1)
CTRLBYT	RAMSTART + 8
CPUSPD	RAMSTART + 9
LADDR	RAMSTART + 10
BUMPS	RAMSTART + 12
DERASE	RAMSTART + 13
DATA	RAMSTART + 15

1. RAMSTART is defined as the starting address of the RAM in the memory map. This is address $0080.

2.5.8 Embedded Function Descriptions

This subsection describes the embedded functions.

2.5.8.1 RDVRRNG Routine

Name: RDVRRNG

Purpose: Read and/or verify a range of FLASH memory

Entry conditions:

H:X	Contains the first address of the range
LADDR	Contains the last address of the range
DATA	Contains the data to compare the read data against for read/verify to RAM only (length is user determined)
ACC	Non-zero for read/verify to RAM, 0 for output to PA0

Exit conditions:

C bit	Set if good compare for read/verify to RAM only
ACC	Contains checksum
DATA	Contains read FLASH data for read/verify to RAM only

Ready/verify RAM option: This subroutine both compares data passed in the DATA array to the FLASH data and reads the data from FLASH into the DATA array. It also calculates the checksum of the data.

Output to PA0 option: This subroutine dumps the data from the range to PA0 in the same format as monitor data. It also calculates the checksum of the data.

NOTE: *This serial dump does not circumvent security because the security vectors must still be passed to make FLASH readable in monitor mode.*

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2.5.8.2 PRGRNGE Routine

Name: PRGRNGE

Purpose: Programs a range of addresses in FLASH memory

Entry conditions:

H:X	Contains the first address in the range
LADDR	Contains the last address in the range
DATA	Contains the data to be programmed (length is user determined)
CPUSPD	Contains the bus frequency times 4 in MHz
BUMPS	Contains the maximum allowable number of programming bumps to use

Exit conditions:

C bit	Set if successful program; cleared otherwise
I bit	Set, masking interrupts

This routine programs a range of FLASH defined by H:X and LADDR. The range can be from one byte to as much RAM as can be allocated to DATA. The smart programming algorithm defined in **2.5.4 FLASH 2TS Program/Margin Read Operation** is used.

2.5.8.3 ERARNGE Routine

Name: ERARNGE

Purpose: Erase a range of addresses in FLASH memory

Entry conditions:

H:X	Contains an address in the range to be erased; range size specified by control byte
CTLBYTE	Contains the erase block size in bits 5 and 6 (see **Table 2-6**)
DERASE	Contains the erase delay time in μs/24
CPUSPD	CPU frequency times 4 in MHz

Table 2-6. CTLBYTE-Erase Block Size

Bit 6	Bit 5	Block Size
0	0	Full array
0	1	One half array
1	0	Eight rows: 64 pages
1	1	Single row: 8 pages

Exit conditions:

I bit	Set, masking interrupts.

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This routine erases the block of FLASH defined by H:X and CTLBYTE. The algorithm defined in **2.5.3 FLASH 2TS Erase Operation** is used.

Preserves the contents of H:X (address passed)

2.5.8.4 REDPROG Routine

Name: REDPROG

Purpose: This routine will use a range of multiple rows in the FLASH array to emulate increased write/erase cycling capability of one row.

Entry conditions:

H:X	Contains the address of the first row in the range. This address must be the first address of a row (multiple of eight bytes)
LADDR	Address of last row in the range; must be the first address of a row (multiple of eight bytes)
DATA	Data to program in the row (bit 7 of DATA + 0 is used internally and will be overwritten). Routine will always use 8 bytes starting at DATA
BUMPS	Contains the maximum allowable number of programming bumps to use
CPUSPD	Contains the bus frequency times 4 in MHz
DERASE	Contains the erase delay time in µs/24

Exit conditions:

C bit	Set if successful program; cleared otherwise
I bit	Set, masking interrupts

This routine uses a range of the FLASH array containing multiple rows to emulate increased write/erase cycling capability for data storage. The routine will write data to each row of the FLASH array (in the range defined) upon subsequent calls. The number of rows is the difference between the value in H:X and LADDR, divided by 8.

A row is the minimum range that can be programmed with the REDPROG routine. All rows in the range will be programmed once before any are programmed again. This approach is taken to ensure that all rows reach the end of lifetime at approximately the same time.

A special bit will be maintained by the routine, called a cycling bit, in each row. This bit is used to ensure that the data is programmed to all the rows defined in the range. This is the high bit of the first byte in each row. This bit cannot be used to store user data. It will be modified by the REDPROG routine. This is at bit 7 of the byte at address DATA+0.

To determine which row to program, the algorithm will step from the first to the last row in a range looking for the first row whose cycling bit is different from the first. If all rows contain the same cycling bit, then the first row will be used.

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The row whose cycling bit is different will be erased and the entire row will be programmed with the given data, including a toggled version of the cycling bit.

2.5.8.5 Example Routine Calls

This code is for illustrative purposes only and does not represent valid syntax for any particular assembler.

```
RAM             EQU     $80
RDVRRNG         EQU     $F000
PRGRNGE         EQU     $F003
ERANRGE         EQU     $F006
REDPROG         EQU     $F009
;*************************************************************
 RAM Definitions for Subroutines
;*************************************************************

ORG     RAM+8

CTRLBYT         RMB     1
CPUSPD          RMB     1
LADDR           RMB     2
BUMPS           RMB     1
DERASE          RMB     2

;Allocation of "DATA" space is dependent on the device and
;application

DATA    RMB     8
;*************************************************************
; CALLING EXAMPLE FOR READ/VERIFY A RANGE (RDVRRNG)
;*************************************************************
LDA     #$FF            ;TARGET IS RAM
LDHX    #$7807          ;END AFTER FIRST ROW
STHX    LADDR
LDHX    #$7800          ;START AT FIRST ROW
JSR     RDVRRNG         ;DATA WILL CONTAIN FLASH INFO
;*************************************************************;
CALLING EXAMPLE FOR ERASE A RANGE (RNGEERA)
;*************************************************************
MOV     #$08,CPUSPD     ;Load Bus frequency in MHz * 4
MOV     #$60,CTRLBYT    ;Bits 5&6 hold the block size to erase
                        ;00  Full Array
                        ;20  One-Half Array
                        ;40  Eight Rows
                        ;60  Singe Row
                        ;Remember a Row is 1 byte

                        ;Set erase time in uS/24, number in
                        ;decimal
LDHX    #100000/24
STHX    DERASE
```


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```
LDHX    #$7800          ;Address in the range to erase
JSR     ERARNGE         ;Call through jump table

;*************************************************************;
; CALLING EXAMPLE FOR PROGRAM A RANGE (RNGEPROG)
;*************************************************************
MOV     #'P',DATA
MOV     #'R',DATA+1
MOV     #'O',DATA+2
MOV     #'G',DATA+3
MOV     #'T',DATA+4
MOV     #'E',DATA+5
MOV     #'S',DATA+6
MOV     #'T',DATA+7

MOV     #$08,CPUSPD     ;Load Bus frequency in MHz * 4
MOV     #$0A,BUMPS      ;Load max number of programming steps
                        ;before a failure is returned
LDHX     #$7807         ;Load the last address to program
STHX     LADDR          ;into LADDR
LDHX    #$7800          ;Load the first address to program
                        ;into H:X
                        ;This range may cross page boundaries
                        ;and may be any length, so long as the
                        ;data to program is loaded in RAM
                        ;beginning at DATA.
JSR     PRGRNGE         ;Call through jump table.
;*************************************************************
; CALLING EXAMPLE FOR REDUNDANT PROGRAM A ROW (REDPROG)
;*************************************************************
MOV     #$56,DATA
MOV     #'P',DATA+1
MOV     #'R',DATA+2
MOV     #'O',DATA+3
MOV     #'G',DATA+4
MOV     #'R',DATA+5
MOV     #'E',DATA+6
MOV     #'D',DATA+7

MOV     #$08,CPUSPD     ;Load Bus frequency in MHz * 4
MOV     #$0A,BUMPS      ;Load max number of programming steps
                        ;before a failure is returned
                        ;Set erase time in uS/24
LDHX    #100000/24
STHX    DERASE

LDHX     #$7808         ;Load the last address of the multi-row
                        ;range; (in this case, 2 rows)
STHX     LADDR          ;into LADDR
LDHX    #$7800          ;Load the first address of the
                        ;multi-row range into H:X
JSR     REDPROG         ;Call through jump table.
```

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2.5.9 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power-consumption standby modes.

2.5.9.1 Wait Mode

Putting the MCU into wait mode while the FLASH 2TS is in read mode does not affect the operation of the FLASH 2TS memory directly, but there will be no memory activity since the CPU is inactive.

The WAIT instruction should not be executed while performing a program or erase operation on the FLASH 2TS. When the MCU is put into wait mode, the charge pump for the FLASH 2TS is disabled so that either a program or erase operation will not continue. If the memory is in either program mode (PGM = 1, HVEN = 1) or erase mode (ERASE = 1, HVEN= 1), then it will remain in that mode during wait. Exit from wait mode must now be done with a reset rather than an interrupt because if exiting wait with an interrupt, the memory will not be in read mode and the interrupt vector cannot be read from the memory.

2.5.9.2 Stop Mode

When the MCU is put into stop mode, if the FLASH 2TS is in read mode, it will be put into low-power standby.

The STOP instruction should not be executed while performing a program or erase operation on the FLASH 2TS. When the MCU is put into stop mode, the charge pump for the FLASH 2TS is disabled so that either a program or erase operation will not continue. If the memory is in either program mode (PGM = 1, HVEN = 1) or erase mode (ERASE = 1, HVEN = 1), then it will remain in that mode during stop. Exit from stop mode now must be done with a reset rather than an interrupt because if exiting stop with an interrupt, the memory will not be in read mode and the interrupt vector cannot be read from the memory.

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Section 3. Configuration Register (CONFIG)

3.1 Introduction

This section describes the configuration register (CONFIG). The configuration register enables or disables these options:

- Stop mode recovery time (32 CGMXCLK cycles or 4,096 CGMXCLK cycles)
- COP timeout period ($2^{18} – 2^4$ or $2^{13} – 2^4$ CGMXCLK cycles)
- STOP instruction
- Computer operating properly module (COP)
- Low-voltage inhibit (LVI) module control

3.2 Functional Description

The CONFIG register is used in the initialization of various options and can be written once after each reset. The register is set to the documented value during reset. Since the various options affect the operation of the MCU, it is recommended that these registers be written immediately after reset. The configuration register is located at $001F.

NOTE: *On a FLASH device, the options are one-time writable by the user after each reset. The CONFIG register is not in the FLASH memory but is a special register containing one-time writable latches after each reset. Upon a reset, the CONFIG register defaults to predetermined settings as shown in* ***Figure 2-1. Memory Map****.*

Address: $001F

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	EXTSLOW	LVISTOP	LVIRST	LVIPWR	COPRS	SSREC	STOP	COPD
Reset:	0	0	1	1	0	0	0	0

Figure 3-1. Configuration Register (CONFIG)

EXTSLOW — Slow External Crystal Enable Bit

The EXTSLOW bit has two functions. It configures the ICG module for a fast (1 MHz–8 MHz) or slow (30 kHz–100 kHz) speed crystal. The option also configures the clock monitor operation in the ICG module to expect an external

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frequency higher (307.2 kHz–32 MHz) or lower (60 Hz–307.2 kHz) than the base frequency of the internal oscillator. (See **Section 6. Internal Clock Generator Module (ICG)**.)

1 = ICG set for slow external crystal operation
0 = ICG set for fast external crystal operation

LVISTOP — LVI Enable in Stop Mode Bit

When the LVIPWR bit is set, setting the LVISTOP bit enables the LVI to operate during stop mode. Reset clears LVISTOP.

1 = LVI enabled during stop mode
0 = LVI disabled during stop mode

LVIRST — LVI Reset Enable Bit

LVIRST enables the reset signal from the LVI module. (See **Section 8. Low-Voltage Inhibit (LVI)**.)

1 = LVI module resets enabled
0 = LVI module resets disabled

LVIPWR — LVI Power Enable Bit

LVIPWR disables the LVI module. (See **Section 8. Low-Voltage Inhibit (LVI)**.)

1 = LVI module power enabled
0 = LVI module power disabled

COPRS — COP Rate Select Bit

COPRS selects the COP timeout period. Reset clears COPRS. (See **Section 4. Computer Operating Properly Module (COP)**.)

1 = COP timeout period = $2^{13} – 2^4$ CGMXCLK cycles
0 = COP timeout period = $2^{18} – 2^4$ CGMXCLK cycles

SSREC — Short Stop Recovery Bit

SSREC enables the CPU to exit stop mode with a delay of 32 CGMXCLK cycles instead of a 4096-CGMXCLK cycle delay.

1 = Stop mode recovery after 32 CGMXCLK cycles
0 = Stop mode recovery after 4096 CGMXCLK cycles

NOTE: *Exiting stop mode by pulling reset will result in the long stop recovery.*

If using the internal clock generator module or an external crystal oscillator, do not set the SSREC bit.

The LVI has an enable time of t_{EN}. The system stabilization time for power-on reset and long stop recovery (both 4096 CGMXCLK cycles) gives a delay longer than the LVI enable time for these startup scenarios. There is no period where the MCU is not protected from a low-power condition. However, when using the short stop recovery configuration option, the 32 CGMXCLK delay must be greater than the LVI's turn on time to avoid a period in startup where the LVI is not protecting the MCU.

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STOP — STOP Instruction Enable Bit
STOP enables the STOP instruction.
1 = STOP instruction enabled
0 = STOP instruction treated as illegal opcode

COPD — COP Disable Bit
COPD disables the COP module. (See **Section 4. Computer Operating Properly Module (COP)**.)
1 = COP module disabled
0 = COP module enabled

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Configuration Register (CONFIG)

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Section 4. Computer Operating Properly Module (COP)

4.1 Introduction

The computer operating properly (COP) module contains a free-running counter that generates a reset if allowed to overflow. The COP module helps software recover from runaway code. Prevent a COP reset by periodically clearing the COP counter.

4.2 Functional Description

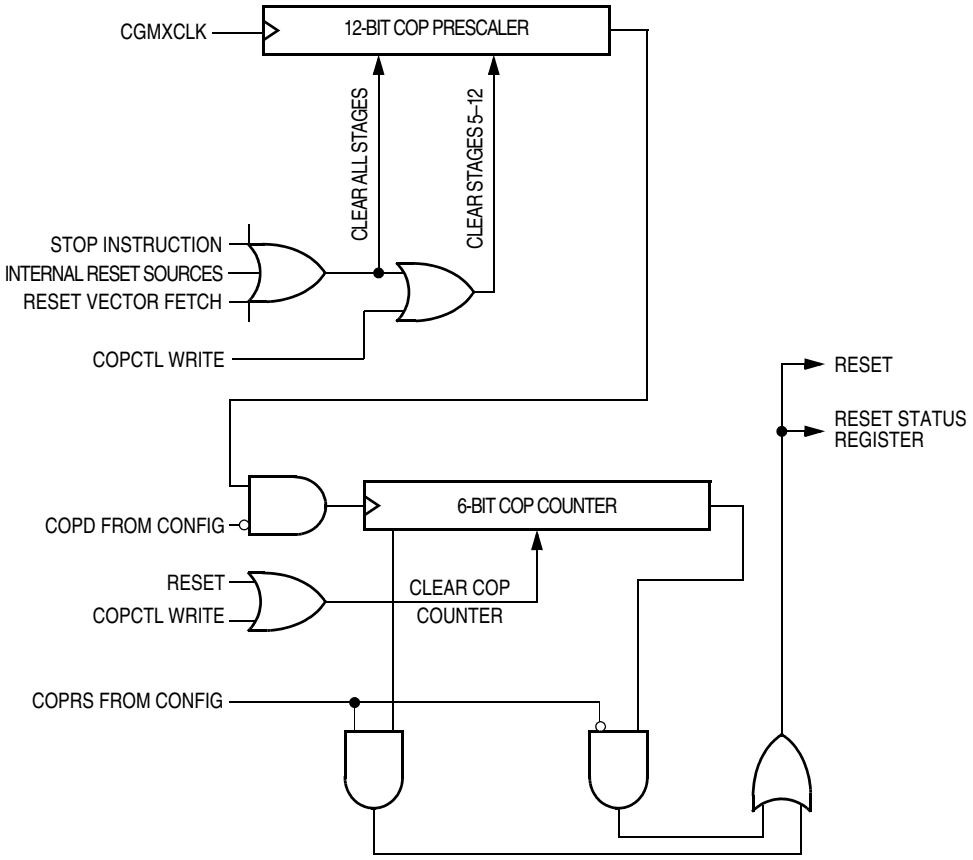

Figure 4-1. COP Block Diagram

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The COP counter is a free-running 6-bit counter preceded by a 12-bit prescaler. If not cleared by software, the COP counter overflows and generates an asynchronous reset after $2^{13} - 2^4$ or $2^{18} - 2^4$ CGMXCLK cycles, depending on the state of the COP rate select bit, COPRS, in the configuration register. When COPRS = 1, a 4.9152-MHz crystal gives a COP timeout period of 53.3 ms. Writing any value to location $FFFF before an overflow occurs prevents a COP reset by clearing the COP counter and stages 5 through 12 of the prescaler.

NOTE: *Service the COP immediately after reset and before entering or after exiting stop mode to guarantee the maximum time before the first COP counter overflow.*

A COP reset pulls the $\overline{\text{RST}}$ pin low for 32 CGMXCLK cycles and sets the COP bit in the SIM reset status register (SRSR).

In monitor mode, the COP is disabled if the $\overline{\text{RST}}$ pin or the $\overline{\text{IRQ}}$ pin is held at V_{TST}. During the break state, V_{TST} on the $\overline{\text{RST}}$ pin disables the COP.

NOTE: *Place COP clearing instructions in the main program and not in an interrupt subroutine. Such an interrupt subroutine could keep the COP from generating a reset even while the main program is not working properly.*

4.3 I/O Signals

The following paragraphs describe the signals shown in **Figure 4-1**.

4.3.1 CGMXCLK

CGMXCLK is the oscillator output signal. See **6.3.5 Clock Selection Circuit** for a description of CGMXCLK.

4.3.2 STOP Instruction

The STOP instruction clears the COP prescaler.

4.3.3 COPCTL Write

Writing any value to the COP control register (COPCTL) (see **4.4 COP Control Register**) clears the COP counter and clears stages 12 through 5 of the COP prescaler. Reading the COP control register returns the reset vector.

4.3.4 Power-On Reset

The power-on reset (POR) circuit clears the COP prescaler 4096 CGMXCLK cycles after power-up.

4.3.5 Internal Reset

An internal reset clears the COP prescaler and the COP counter.

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4.3.6 Reset Vector Fetch

A reset vector fetch occurs when the vector address appears on the data bus. A reset vector fetch clears the COP prescaler.

4.3.7 COPD

The COPD signal reflects the state of the COP disable bit (COPD) in the configuration register. (See **Section 3. Configuration Register (CONFIG)**).

4.3.8 COPRS

The COPRS signal reflects the state of the COP rate select bit (COPRS) in the configuration register. (See **Section 3. Configuration Register (CONFIG)**).

4.4 COP Control Register

The COP control register is located at address $FFFF and overlaps the reset vector. Writing any value to $FFFF clears the COP counter and starts a new timeout period. Reading location $FFFF returns the low byte of the reset vector.

Address: $FFFF

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	LOW BYTE OF RESET VECTOR							
Write:	CLEAR COP COUNTER							
Reset:	Unaffected by reset							

Figure 4-2. COP Control Register (COPCTL)

4.5 Interrupts

The COP does not generate CPU interrupt requests.

4.6 Monitor Mode

The COP is disabled in monitor mode when V_{TST} is present on the $\overline{IRQ}$ pin or on the $\overline{RST}$ pin.

4.7 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power-consumption standby modes.

4.7.1 Wait Mode

The COP remains active in wait mode. To prevent a COP reset during wait mode, periodically clear the COP counter in a CPU interrupt routine.

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4.7.2 Stop Mode

Stop mode turns off the CGMXCLK input to the COP and clears the COP prescaler. Service the COP immediately before entering or after exiting stop mode to ensure a full COP timeout period after entering or exiting stop mode.

The STOP bit (see **Section 3. Configuration Register (CONFIG)**) enables the STOP instruction. To prevent inadvertently turning off the COP with a STOP instruction, disable the STOP instruction by clearing the STOP bit.

4.8 COP Module During Break Interrupts

The COP is disabled during a break interrupt when V_{TST} is present on the $\overline{RST}$ pin.

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Section 5. Central Processor Unit (CPU)

5.1 Contents

The M68HC08 CPU (central processor unit) is an enhanced and fully object-code-compatible version of the M68HC05 CPU. The *CPU08 Reference Manual* (Motorola document order number CPU08RM/AD) contains a description of the CPU instruction set, addressing modes, and architecture.

5.2 Features

Features of the CPU include:

- Object code fully upward-compatible with M68HC05 Family
- 16-bit stack pointer with stack manipulation instructions
- 16-bit index register with x-register manipulation instructions
- 8-MHz CPU internal bus frequency
- 64-Kbyte program/data memory space
- 16 addressing modes
- Memory-to-memory data moves without using accumulator
- Fast 8-bit by 8-bit multiply and 16-bit by 8-bit divide instructions
- Enhanced binary-coded decimal (BCD) data handling
- Modular architecture with expandable internal bus definition for extension of addressing range beyond 64 Kbytes
- Low-power stop and wait modes

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5.3 CPU Registers

Figure 5-1 shows the five CPU registers. CPU registers are not part of the memory map.

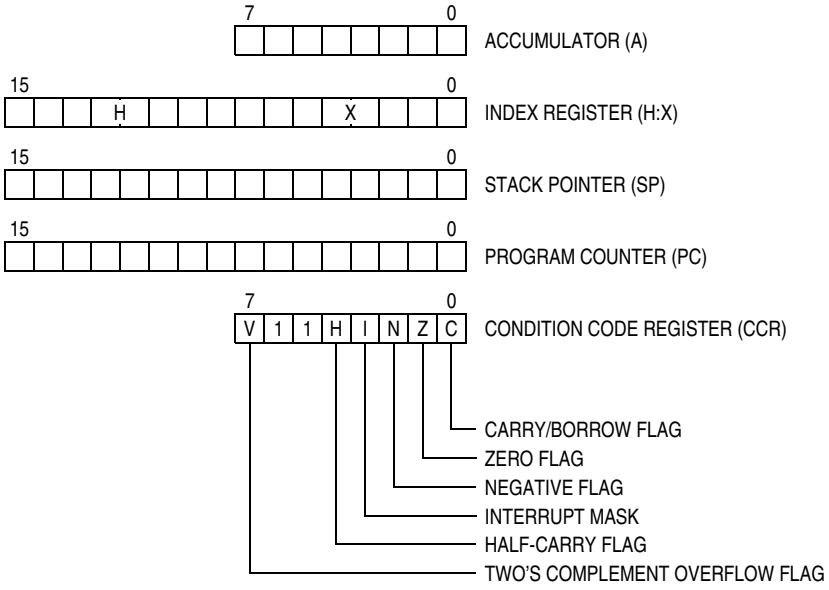

Figure 5-1. CPU Registers

5.3.1 Accumulator

The accumulator is a general-purpose 8-bit register. The CPU uses the accumulator to hold operands and the results of arithmetic/logic operations.

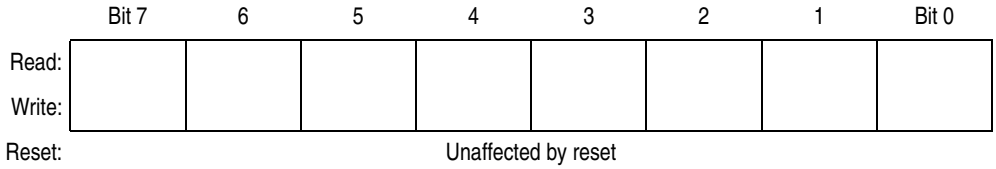

Figure 5-2. Accumulator (A)

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5.3.2 Index Register

The 16-bit index register allows indexed addressing of a 64-Kbyte memory space. H is the upper byte of the index register, and X is the lower byte. H:X is the concatenated 16-bit index register.

In the indexed addressing modes, the CPU uses the contents of the index register to determine the conditional address of the operand.

The index register can serve also as a temporary data storage location.

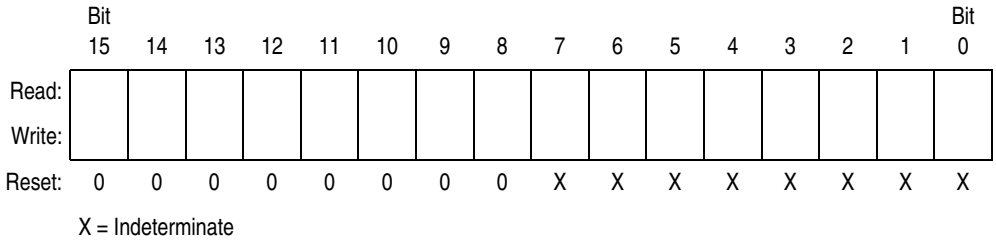

Figure 5-3. Index Register (H:X)

5.3.3 Stack Pointer

The stack pointer is a 16-bit register that contains the address of the next location on the stack. During a reset, the stack pointer is preset to $00FF. The reset stack pointer (RSP) instruction sets the least significant byte to $FF and does not affect the most significant byte. The stack pointer decrements as data is pushed onto the stack and increments as data is pulled from the stack.

In the stack pointer 8-bit offset and 16-bit offset addressing modes, the stack pointer can function as an index register to access data on the stack. The CPU uses the contents of the stack pointer to determine the conditional address of the operand.

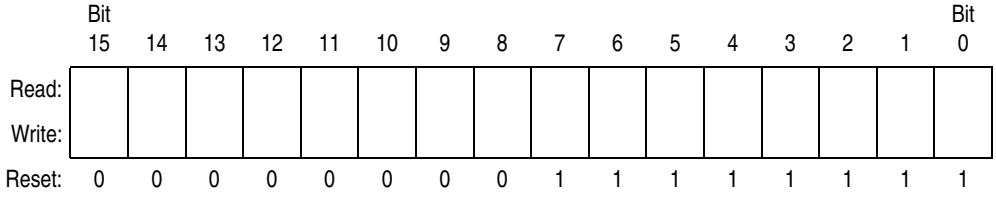

Figure 5-4. Stack Pointer (SP)

NOTE: *The location of the stack is arbitrary and may be relocated anywhere in random-access memory (RAM). Moving the SP out of page 0 ($0000 to $00FF) frees direct address (page 0) space. For correct operation, the stack pointer must point only to RAM locations.*

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5.3.4 Program Counter

The program counter is a 16-bit register that contains the address of the next instruction or operand to be fetched.

Normally, the program counter automatically increments to the next sequential memory location every time an instruction or operand is fetched. Jump, branch, and interrupt operations load the program counter with an address other than that of the next sequential location.

During reset, the program counter is loaded with the reset vector address located at $FFFE and $FFFF. The vector address is the address of the first instruction to be executed after exiting the reset state.

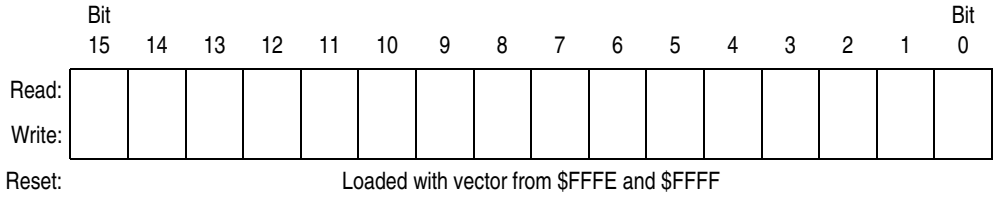

Figure 5-5. Program Counter (PC)

5.3.5 Condition Code Register

The 8-bit condition code register contains the interrupt mask and five flags that indicate the results of the instruction just executed. Bits 6 and 5 are set permanently to 1. The following paragraphs describe the functions of the condition code register.

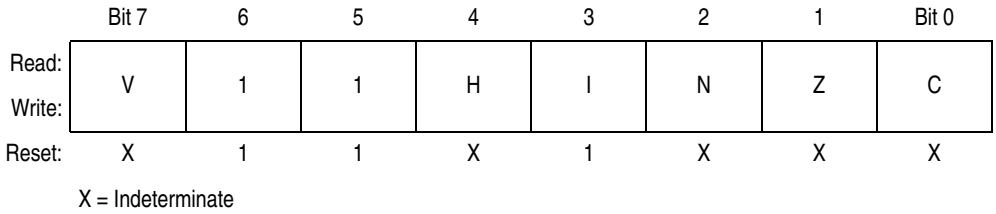

Figure 5-6. Condition Code Register (CCR)

V — Overflow Flag

The CPU sets the overflow flag when a two's complement overflow occurs. The signed branch instructions BGT, BGE, BLE, and BLT use the overflow flag.

1 = Overflow

0 = No overflow

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H — Half-Carry Flag

The CPU sets the half-carry flag when a carry occurs between accumulator bits 3 and 4 during an add-without-carry (ADD) or add-with-carry (ADC) operation. The half-carry flag is required for binary-coded decimal (BCD) arithmetic operations. The DAA instruction uses the states of the H and C flags to determine the appropriate correction factor.

1 = Carry between bits 3 and 4
0 = No carry between bits 3 and 4

I — Interrupt Mask

When the interrupt mask is set, all maskable CPU interrupts are disabled. CPU interrupts are enabled when the interrupt mask is cleared. When a CPU interrupt occurs, the interrupt mask is set
automatically after the CPU registers are saved on the stack, but before the interrupt vector is fetched.

1 = Interrupts disabled
0 = Interrupts enabled

NOTE: *To maintain M6805 Family compatibility, the upper byte of the index register (H) is not stacked automatically. If the interrupt service routine modifies H, then the user must stack and unstack H using the PSHH and PULH instructions.*

After the I bit is cleared, the highest-priority interrupt request is serviced first. A return-from-interrupt (RTI) instruction pulls the CPU registers from the stack and restores the interrupt mask from the stack. After any reset, the interrupt mask is set and can be cleared only by the clear interrupt mask software instruction (CLI).

N — Negative flag

The CPU sets the negative flag when an arithmetic operation, logic operation, or data manipulation produces a negative result, setting bit 7 of the result.

1 = Negative result
0 = Non-negative result

Z — Zero flag

The CPU sets the zero flag when an arithmetic operation, logic operation, or data manipulation produces a result of $00.

1 = Zero result
0 = Non-zero result

C — Carry/Borrow Flag

The CPU sets the carry/borrow flag when an addition operation produces a carry out of bit 7 of the accumulator or when a subtraction operation requires a borrow. Some instructions — such as bit test and branch, shift, and rotate — also clear or set the carry/borrow flag.

1 = Carry out of bit 7
0 = No carry out of bit 7

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5.4 Arithmetic/Logic Unit (ALU)

The ALU performs the arithmetic and logic operations defined by the instruction set.

Refer to the *CPU08 Reference Manual* (Motorola document order number CPU08RM/AD) for a description of the instructions and addressing modes and more detail about the architecture of the CPU.

5.5 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power-consumption standby modes.

5.5.1 Wait Mode

The WAIT instruction:

- Clears the interrupt mask (I bit) in the condition code register, enabling interrupts. After exit from wait mode by interrupt, the I bit remains clear. After exit by reset, the I bit is set.
- Disables the CPU clock

5.5.2 Stop Mode

The STOP instruction:

- Clears the interrupt mask (I bit) in the condition code register, enabling external interrupts. After exit from stop mode by external interrupt, the I bit remains clear. After exit by reset, the I bit is set.
- Disables the CPU clock

After exiting stop mode, the CPU clock begins running after the oscillator stabilization delay.

5.6 CPU During Break Interrupts

If a break module is present on the MCU, the CPU starts a break interrupt by:

- Loading the instruction register with the SWI instruction
- Loading the program counter with $FFFC:$FFFD or with $FEFC:$FEFD in monitor mode

The break interrupt begins after completion of the CPU instruction in progress. If the break address register match occurs on the last cycle of a CPU instruction, the break interrupt begins immediately.

A return-from-interrupt instruction (RTI) in the break routine ends the break interrupt and returns the MCU to normal operation if the break interrupt has been deasserted.

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5.7 Instruction Set Summary

Table 5-1 provides a summary of the M68HC08 instruction set.

Table 5-1. Instruction Set Summary (Sheet 1 of 7)

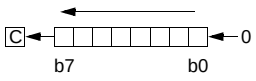
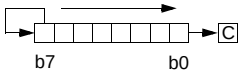
Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
ADC #*opr* ADC *opr* ADC *opr* ADC *opr*,X ADC *opr*,X ADC ,X ADC *opr*,SP ADC *opr*,SP	Add with Carry	A ← (A) + (M) + (C)	↕	↕	–	↕	↕	↕	IMM DIR EXT IX2 IX1 IX SP1 SP2	A9 B9 C9 D9 E9 F9 9EE9 9ED9	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
ADD #*opr* ADD *opr* ADD *opr* ADD *opr*,X ADD *opr*,X ADD ,X ADD *opr*,SP ADD *opr*,SP	Add without Carry	A ← (A) + (M)	↕	↕	–	↕	↕	↕	IMM DIR EXT IX2 IX1 IX SP1 SP2	AB BB CB DB EB FB 9EEB 9EDB	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
AIS #*opr*	Add Immediate Value (Signed) to SP	SP ← (SP) + (16 « M)	–	–	–	–	–	–	IMM	A7	ii	2
AIX #*opr*	Add Immediate Value (Signed) to H:X	H:X ← (H:X) + (16 « M)	–	–	–	–	–	–	IMM	AF	ii	2
AND #*opr* AND *opr* AND *opr* AND *opr*,X AND *opr*,X AND ,X AND *opr*,SP AND *opr*,SP	Logical AND	A ← (A) & (M)	0	–	–	↕	↕	–	IMM DIR EXT IX2 IX1 IX SP1 SP2	A4 B4 C4 D4 E4 F4 9EE4 9ED4	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
ASL *opr* ASLA ASLX ASL *opr*,X ASL ,X ASL *opr*,SP	Arithmetic Shift Left (Same as LSL)		↕	–	–	↕	↕	↕	DIR INH INH IX1 IX SP1	38 48 58 68 78 9E68	dd ff ff	4 1 1 4 3 5
ASR *opr* ASRA ASRX ASR *opr*,X ASR *opr*,X ASR *opr*,SP	Arithmetic Shift Right		↕	–	–	↕	↕	↕	DIR INH INH IX1 IX SP1	37 47 57 67 77 9E67	dd ff ff	4 1 1 4 3 5
BCC *rel*	Branch if Carry Bit Clear	PC ← (PC) + 2 + rel ? (C) = 0	–	–	–	–	–	–	REL	24	rr	3
BCLR *n*, *opr*	Clear Bit n in M	Mn ← 0	–	–	–	–	–	–	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	11 13 15 17 19 1B 1D 1F	dd dd dd dd dd dd dd dd	4 4 4 4 4 4 4 4
BCS *rel*	Branch if Carry Bit Set (Same as BLO)	PC ← (PC) + 2 + *rel* ? (C) = 1	–	–	–	–	–	–	REL	25	rr	3
BEQ *rel*	Branch if Equal	PC ← (PC) + 2 + *rel* ? (Z) = 1	–	–	–	–	–	–	REL	27	rr	3

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Table 5-1. Instruction Set Summary (Sheet 2 of 7)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
BGE *opr*	Branch if Greater Than or Equal To (Signed Operands)	PC ← (PC) + 2 + *rel* ? (N ⊕ V) = 0	–	–	–	–	–	–	REL	90	rr	3
BGT *opr*	Branch if Greater Than (Signed Operands)	PC ← (PC) + 2 + *rel* ? (Z) | (N ⊕ V) = 0	–	–	–	–	–	–	REL	92	rr	3
BHCC *rel*	Branch if Half Carry Bit Clear	PC ← (PC) + 2 + *rel* ? (H) = 0	–	–	–	–	–	–	REL	28	rr	3
BHCS *rel*	Branch if Half Carry Bit Set	PC ← (PC) + 2 + *rel* ? (H) = 1	–	–	–	–	–	–	REL	29	rr	3
BHI *rel*	Branch if Higher	PC ← (PC) + 2 + *rel* ? (C) | (Z) = 0	–	–	–	–	–	–	REL	22	rr	3
BHS *rel*	Branch if Higher or Same (Same as BCC)	PC ← (PC) + 2 + *rel* ? (C) = 0	–	–	–	–	–	–	REL	24	rr	3
BIH *rel*	Branch if $\overline{IRQ}$ Pin High	PC ← (PC) + 2 + *rel* ? $\overline{IRQ}$ = 1	–	–	–	–	–	–	REL	2F	rr	3
BIL *rel*	Branch if $\overline{IRQ}$ Pin Low	PC ← (PC) + 2 + *rel* ? $\overline{IRQ}$ = 0	–	–	–	–	–	–	REL	2E	rr	3
BIT #*opr* BIT *opr* BIT *opr* BIT *opr*,X BIT *opr*,X BIT ,X BIT *opr*,SP BIT *opr*,SP	Bit Test	(A) & (M)	0	–	–	↕	↕	–	IMM DIR EXT IX2 IX1 IX SP1 SP2	A5 B5 C5 D5 E5 F5 9EE5 9ED5	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
BLE *opr*	Branch if Less Than or Equal To (Signed Operands)	PC ← (PC) + 2 + *rel* ? (Z) | (N ⊕ V) = 1	–	–	–	–	–	–	REL	93	rr	3
BLO *rel*	Branch if Lower (Same as BCS)	PC ← (PC) + 2 + *rel* ? (C) = 1	–	–	–	–	–	–	REL	25	rr	3
BLS *rel*	Branch if Lower or Same	PC ← (PC) + 2 + *rel* ? (C) | (Z) = 1	–	–	–	–	–	–	REL	23	rr	3
BLT *opr*	Branch if Less Than (Signed Operands)	PC ← (PC) + 2 + *rel* ? (N ⊕ V) =1	–	–	–	–	–	–	REL	91	rr	3
BMC *rel*	Branch if Interrupt Mask Clear	PC ← (PC) + 2 + *rel* ? (I) = 0	–	–	–	–	–	–	REL	2C	rr	3
BMI *rel*	Branch if Minus	PC ← (PC) + 2 + *rel* ? (N) = 1	–	–	–	–	–	–	REL	2B	rr	3
BMS *rel*	Branch if Interrupt Mask Set	PC ← (PC) + 2 + *rel* ? (I) = 1	–	–	–	–	–	–	REL	2D	rr	3
BNE *rel*	Branch if Not Equal	PC ← (PC) + 2 + *rel* ? (Z) = 0	–	–	–	–	–	–	REL	26	rr	3
BPL *rel*	Branch if Plus	PC ← (PC) + 2 + *rel* ? (N) = 0	–	–	–	–	–	–	REL	2A	rr	3
BRA *rel*	Branch Always	PC ← (PC) + 2 + *rel*	–	–	–	–	–	–	REL	20	rr	3
BRCLR *n*,*opr*,*rel*	Branch if Bit *n* in M Clear	PC ← (PC) + 3 + *rel* ? (Mn) = 0	–	–	–	–	–	↕	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	01 03 05 07 09 0B 0D 0F	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BRN *rel*	Branch Never	PC ← (PC) + 2	–	–	–	–	–	–	REL	21	rr	3

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Table 5-1. Instruction Set Summary (Sheet 3 of 7)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
BRSET *n*,*opr*,*rel*	Branch if Bit *n* in M Set	PC ← (PC) + 3 + *rel* ? (Mn) = 1	–	–	–	–	–	↕	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	00 02 04 06 08 0A 0C 0E	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BSET *n*,*opr*	Set Bit *n* in M	Mn ← 1	–	–	–	–	–	–	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	10 12 14 16 18 1A 1C 1E	dd dd dd dd dd dd dd dd	4 4 4 4 4 4 4 4
BSR *rel*	Branch to Subroutine	PC ← (PC) + 2; push (PCL) SP ← (SP) – 1; push (PCH) SP ← (SP) – 1 PC ← (PC) + *rel*	–	–	–	–	–	–	REL	AD	rr	4
CBEQ *opr*,*rel* CBEQA #*opr*,*rel* CBEQX #*opr*,*rel* CBEQ *opr*,X+,*rel* CBEQ X+,*rel* CBEQ *opr*,SP,*rel*	Compare and Branch if Equal	PC ← (PC) + 3 + rel ? (A) – (M) = $00 PC ← (PC) + 3 + rel ? (A) – (M) = $00 PC ← (PC) + 3 + rel ? (X) – (M) = $00 PC ← (PC) + 3 + rel ? (A) – (M) = $00 PC ← (PC) + 2 + rel ? (A) – (M) = $00 PC ← (PC) + 4 + rel ? (A) – (M) = $00	–	–	–	–	–	–	DIR IMM IMM IX1+ IX+ SP1	31 41 51 61 71 9E61	dd rr ii rr ii rr ff rr rr ff rr	5 4 4 5 4 6
CLC	Clear Carry Bit	C ← 0	–	–	–	–	–	0	INH	98		1
CLI	Clear Interrupt Mask	I ← 0	–	–	0	–	–	–	INH	9A		2
CLR *opr* CLRA CLRX CLRH CLR *opr*,X CLR ,X CLR *opr*,SP	Clear	M ← $00 A ← $00 X ← $00 H ← $00 M ← $00 M ← $00 M ← $00	0	–	–	0	1	–	DIR INH INH INH IX1 IX SP1	3F 4F 5F 8C 6F 7F 9E6F	dd ff ff	3 1 1 1 3 2 4
CMP #*opr* CMP *opr* CMP *opr* CMP *opr*,X CMP *opr*,X CMP ,X CMP *opr*,SP CMP *opr*,SP	Compare A with M	(A) – (M)	↕	–	–	↕	↕	↕	IMM DIR EXT IX2 IX1 IX SP1 SP2	A1 B1 C1 D1 E1 F1 9EE1 9ED1	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
COM *opr* COMA COMX COM *opr*,X COM ,X COM *opr*,SP	Complement (One's Complement)	M ← ($\overline{M}$) = $FF – (M) A ← ($\overline{A}$) = $FF – (M) X ← ($\overline{X}$) = $FF – (M) M ← ($\overline{M}$) = $FF – (M) M ← ($\overline{M}$) = $FF – (M) M ← (M) = $FF – (M)	0	–	–	↕	↕	1	DIR INH INH IX1 IX SP1	33 43 53 63 73 9E63	dd ff ff	4 1 1 4 3 5
CPHX #*opr* CPHX *opr*	Compare H:X with M	(H:X) – (M:M + 1)	↕	–	–	↕	↕	↕	IMM DIR	65 75	ii ii+1 dd	3 4

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Table 5-1. Instruction Set Summary (Sheet 4 of 7)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
CPX #*opr* CPX *opr* CPX *opr* CPX ,X CPX *opr*,X CPX *opr*,X CPX *opr*,SP CPX *opr*,SP	Compare X with M	(X) – (M)	↕	–	–	↕	↕	↕	IMM DIR EXT IX2 IX1 IX SP1 SP2	A3 B3 C3 D3 E3 F3 9EE3 9ED3	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
DAA	Decimal Adjust A	$(A)_{10}$	U	–	–	↕	↕	↕	INH	72		2
DBNZ *opr,rel* DBNZA *rel* DBNZX *rel* DBNZ *opr,*X,*rel* DBNZ X,*rel* DBNZ *opr,*SP,*rel*	Decrement and Branch if Not Zero	A ← (A) – 1 or M ← (M) – 1 or X ← (X) – 1 PC ← (PC) + 3 + *rel* ? (result) ≠ 0 PC ← (PC) + 2 + *rel* ? (result) ≠ 0 PC ← (PC) + 2 + *rel* ? (result) ≠ 0 PC ← (PC) + 3 + *rel* ? (result) ≠ 0 PC ← (PC) + 2 + *rel* ? (result) ≠ 0 PC ← (PC) + 4 + *rel* ? (result) ≠ 0	–	–	–	–	–	–	DIR INH INH IX1 IX SP1	3B 4B 5B 6B 7B 9E6B	dd rr rr rr ff rr rr ff rr	5 3 3 5 4 6
DEC *opr* DECA DECX DEC *opr*,X DEC ,X DEC *opr*,SP	Decrement	M ← (M) – 1 A ← (A) – 1 X ← (X) – 1 M ← (M) – 1 M ← (M) – 1 M ← (M) – 1	↕	–	–	↕	↕	–	DIR INH INH IX1 IX SP1	3A 4A 5A 6A 7A 9E6A	dd ff ff	4 1 1 4 3 5
DIV	Divide	A ← (H:A)/(X) H ← Remainder	–	–	–	–	↕	↕	INH	52		7
EOR #*opr* EOR *opr* EOR *opr* EOR *opr*,X EOR *opr*,X EOR ,X EOR *opr*,SP EOR *opr*,SP	Exclusive OR M with A	A ← (A ⊕ M)	0	–	–	↕	↕	–	IMM DIR EXT IX2 IX1 IX SP1 SP2	A8 B8 C8 D8 E8 F8 9EE8 9ED8	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
INC *opr* INCA INCX INC *opr*,X INC ,X INC *opr*,SP	Increment	M ← (M) + 1 A ← (A) + 1 X ← (X) + 1 M ← (M) + 1 M ← (M) + 1 M ← (M) + 1	↕	–	–	↕	↕	–	DIR INH INH IX1 IX SP1	3C 4C 5C 6C 7C 9E6C	dd ff ff	4 1 1 4 3 5
JMP *opr* JMP *opr* JMP *opr*,X JMP *opr*,X JMP ,X	Jump	PC ← Jump Address	–	–	–	–	–	–	DIR EXT IX2 IX1 IX	BC CC DC EC FC	dd hh ll ee ff ff 	2 3 4 3 2
JSR *opr* JSR *opr* JSR *opr*,X JSR *opr*,X JSR ,X	Jump to Subroutine	PC ← (PC) + *n* (*n* = 1, 2, or 3) Push (PCL); SP ← (SP) – 1 Push (PCH); SP ← (SP) – 1 PC ← Unconditional Address	–	–	–	–	–	–	DIR EXT IX2 IX1 IX	BD CD DD ED FD	dd hh ll ee ff ff 	4 5 6 5 4
LDA #*opr* LDA *opr* LDA *opr* LDA *opr*,X LDA *opr*,X LDA ,X LDA *opr*,SP LDA *opr*,SP	Load A from M	A ← (M)	0	–	–	↕	↕	–	IMM DIR EXT IX2 IX1 IX SP1 SP2	A6 B6 C6 D6 E6 F6 9EE6 9ED6	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5

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Table 5-1. Instruction Set Summary (Sheet 5 of 7)

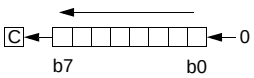
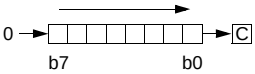
Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
LDHX #*opr* LDHX *opr*	Load H:X from M	H:X ← (M:M + 1)	0	–	–	↕	↕	–	IMM DIR	45 55	ii jj dd	3 4
LDX #*opr* LDX *opr* LDX *opr* LDX *opr*,X LDX *opr*,X LDX ,X LDX *opr*,SP LDX *opr*,SP	Load X from M	X ← (M)	0	–	–	↕	↕	–	IMM DIR EXT IX2 IX1 IX SP1 SP2	AE BE CE DE EE FE 9EEE 9EDE	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
LSL *opr* LSLA LSLX LSL *opr*,X LSL ,X LSL *opr*,SP	Logical Shift Left (Same as ASL)		↕	–	–	↕	↕	↕	DIR INH INH IX1 IX SP1	38 48 58 68 78 9E68	dd ff ff	4 1 1 4 3 5
LSR *opr* LSRA LSR*X* LSR *opr*,X LSR ,X LSR *opr*,SP	Logical Shift Right		↕	–	–	0	↕	↕	DIR INH INH IX1 IX SP1	34 44 54 64 74 9E64	dd ff ff	4 1 1 4 3 5
MOV *opr,opr* MOV *opr,*X+ MOV #*opr,opr* MOV X+*,opr*	Move	$(M)_{Destination} \leftarrow (M)_{Source}$ H:X ← (H:X) + 1 (IX+D, DIX+)	0	–	–	↕	↕	–	DD DIX+ IMD IX+D	4E 5E 6E 7E	dd dd dd ii dd dd	5 4 4 4
MUL	Unsigned multiply	X:A ← (X) × (A)	–	0	–	–	–	0	INH	42		5
NEG *opr* NEGA NEGX NEG *opr*,X NEG ,X NEG *opr*,SP	Negate (Two's Complement)	M ← –(M) = $00 – (M) A ← –(A) = $00 – (A) X ← –(X) = $00 – (X) M ← –(M) = $00 – (M) M ← –(M) = $00 – (M)	↕	–	–	↕	↕	↕	DIR INH INH IX1 IX SP1	30 40 50 60 70 9E60	dd ff ff	4 1 1 4 3 5
NOP	No Operation	None	–	–	–	–	–	–	INH	9D		1
NSA	Nibble Swap A	A ← (A[3:0]:A[7:4])	–	–	–	–	–	–	INH	62		3
ORA #*opr* ORA *opr* ORA *opr* ORA *opr*,X ORA *opr*,X ORA ,X ORA *opr*,SP ORA *opr*,SP	Inclusive OR A and M	A ← (A) | (M)	0	–	–	↕	↕	–	IMM DIR EXT IX2 IX1 IX SP1 SP2	AA BA CA DA EA FA 9EEA 9EDA	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
PSHA	Push A onto Stack	Push (A); SP ← (SP) – 1	–	–	–	–	–	–	INH	87		2
PSHH	Push H onto Stack	Push (H); SP ← (SP) – 1	–	–	–	–	–	–	INH	8B		2
PSHX	Push X onto Stack	Push (X); SP ← (SP) – 1	–	–	–	–	–	–	INH	89		2
PULA	Pull A from Stack	SP ← (SP + 1); Pull (A)	–	–	–	–	–	–	INH	86		2
PULH	Pull H from Stack	SP ← (SP + 1); Pull (H)	–	–	–	–	–	–	INH	8A		2
PULX	Pull X from Stack	SP ← (SP + 1); Pull (X)	–	–	–	–	–	–	INH	88		2

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Table 5-1. Instruction Set Summary (Sheet 6 of 7)

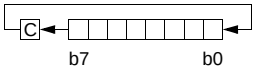
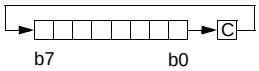
Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
ROL *opr* ROLA ROLX ROL *opr*,X ROL ,X ROL *opr*,SP	Rotate Left through Carry		↕	–	–	↕	↕	↕	DIR INH INH IX1 IX SP1	39 49 59 69 79 9E69	dd ff ff	4 1 1 4 3 5
ROR *opr* RORA RORX ROR *opr*,X ROR ,X ROR *opr*,SP	Rotate Right through Carry		↕	–	–	↕	↕	↕	DIR INH INH IX1 IX SP1	36 46 56 66 76 9E66	dd ff ff	4 1 1 4 3 5
RSP	Reset Stack Pointer	SP ← $FF	–	–	–	–	–	–	INH	9C		1
RTI	Return from Interrupt	SP ← (SP) + 1; Pull (CCR) SP ← (SP) + 1; Pull (A) SP ← (SP) + 1; Pull (X) SP ← (SP) + 1; Pull (PCH) SP ← (SP) + 1; Pull (PCL)	↕	↕	↕	↕	↕	↕	INH	80		7
RTS	Return from Subroutine	SP ← SP + 1; Pull (PCH) SP ← SP + 1; Pull (PCL)	–	–	–	–	–	–	INH	81		4
SBC #*opr* SBC *opr* SBC *opr* SBC *opr*,X SBC *opr*,X SBC ,X SBC *opr*,SP SBC *opr*,SP	Subtract with Carry	A ← (A) – (M) – (C)	↕	–	–	↕	↕	↕	IMM DIR EXT IX2 IX1 IX SP1 SP2	A2 B2 C2 D2 E2 F2 9EE2 9ED2	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
SEC	Set Carry Bit	C ← 1	–	–	–	–	–	1	INH	99		1
SEI	Set Interrupt Mask	I ← 1	–	–	1	–	–	–	INH	9B		2
STA *opr* STA *opr* STA *opr*,X STA *opr*,X STA ,X STA *opr*,SP STA *opr*,SP	Store A in M	M ← (A)	0	–	–	↕	↕	–	DIR EXT IX2 IX1 IX SP1 SP2	B7 C7 D7 E7 F7 9EE7 9ED7	dd hh ll ee ff ff ff ee ff	3 4 4 3 2 4 5
STHX *opr*	Store H:X in M	(M:M + 1) ← (H:X)	0	–	–	↕	↕	–	DIR	35	dd	4
STOP	Enable Interrupts, Stop Processing, Refer to MCU Documentation	I ← 0; Stop Processing	–	–	0	–	–	–	INH	8E		1
STX *opr* STX *opr* STX *opr*,X STX *opr*,X STX ,X STX *opr*,SP STX *opr*,SP	Store X in M	M ← (X)	0	–	–	↕	↕	–	DIR EXT IX2 IX1 IX SP1 SP2	BF CF DF EF FF 9EEF 9EDF	dd hh ll ee ff ff ff ee ff	3 4 4 3 2 4 5
SUB #*opr* SUB *opr* SUB *opr* SUB *opr*,X SUB *opr*,X SUB ,X SUB *opr*,SP SUB *opr*,SP	Subtract	A ← (A) – (M)	↕	–	–	↕	↕	↕	IMM DIR EXT IX2 IX1 IX SP1 SP2	A0 B0 C0 D0 E0 F0 9EE0 9ED0	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5

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Table 5-1. Instruction Set Summary (Sheet 7 of 7)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
SWI	Software Interrupt	PC ← (PC) + 1; Push (PCL) SP ← (SP) – 1; Push (PCH) SP ← (SP) – 1; Push (X) SP ← (SP) – 1; Push (A) SP ← (SP) – 1; Push (CCR) SP ← (SP) – 1; I ← 1 PCH ← Interrupt Vector High Byte PCL ← Interrupt Vector Low Byte	–	–	1	–	–	–	INH	83		9
TAP	Transfer A to CCR	CCR ← (A)	↕	↕	↕	↕	↕	↕	INH	84		2
TAX	Transfer A to X	X ← (A)	–	–	–	–	–	–	INH	97		1
TPA	Transfer CCR to A	A ← (CCR)	–	–	–	–	–	–	INH	85		1
TST *opr* TSTA TSTX TST *opr*,X TST ,X TST *opr*,SP	Test for Negative or Zero	(A) – $00 or (X) – $00 or (M) – $00	0	–	–	↕	↕	–	DIR INH INH IX1 IX SP1	3D 4D 5D 6D 7D 9E6D	dd ff ff	3 1 1 3 2 4
TSX	Transfer SP to H:X	H:X ← (SP) + 1	–	–	–	–	–	–	INH	95		2
TXA	Transfer X to A	A ← (X)	–	–	–	–	–	–	INH	9F		1
TXS	Transfer H:X to SP	(SP) ← (H:X) – 1	–	–	–	–	–	–	INH	94		2
WAIT	Enable Interrupts; Wait for Interrupt	I bit ← 0; Inhibit CPU clocking until interrupted	–	–	0	–	–	–	INH	8F		1

A	Accumulator	*n*	Any bit
C	Carry/borrow bit	*opr*	Operand (one or two bytes)
CCR	Condition code register	PC	Program counter
dd	Direct address of operand	PCH	Program counter high byte
dd rr	Direct address of operand and relative offset of branch instruction	PCL	Program counter low byte
DD	Direct to direct addressing mode	REL	Relative addressing mode
DIR	Direct addressing mode	*rel*	Relative program counter offset byte
DIX+	Direct to indexed with post increment addressing mode	rr	Relative program counter offset byte
ee ff	High and low bytes of offset in indexed, 16-bit offset addressing	SP1	Stack pointer, 8-bit offset addressing mode
EXT	Extended addressing mode	SP2	Stack pointer 16-bit offset addressing mode
ff	Offset byte in indexed, 8-bit offset addressing	SP	Stack pointer
H	Half-carry bit	U	Undefined
H	Index register high byte	V	Overflow bit
hh ll	High and low bytes of operand address in extended addressing	X	Index register low byte
I	Interrupt mask	Z	Zero bit
ii	Immediate operand byte	&	Logical AND
IMD	Immediate source to direct destination addressing mode	|	Logical OR
IMM	Immediate addressing mode	⊕	Logical EXCLUSIVE OR
INH	Inherent addressing mode	( )	Contents of
IX	Indexed, no offset addressing mode	–( )	Negation (two's complement)
IX+	Indexed, no offset, post increment addressing mode	#	Immediate value
IX+D	Indexed with post increment to direct addressing mode	«	Sign extend
IX1	Indexed, 8-bit offset addressing mode	←	Loaded with
IX1+	Indexed, 8-bit offset, post increment addressing mode	?	If
IX2	Indexed, 16-bit offset addressing mode	:	Concatenated with
M	Memory location	↕	Set or cleared
N	Negative bit	—	Not affected

5.8 Opcode Map

See **Table 5-2**.

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Table 5-2. Opcode Map

	Bit Manipulation		Branch	Read-Modify-Write						Control		Register/Memory							
	DIR	DIR	REL	DIR	INH	INH	IX1	SP1	IX	INH	INH	IMM	DIR	EXT	IX2	SP2	IX1	SP1	IX
MSB / LSB	0	1	2	3	4	5	6	9E6	7	8	9	A	B	C	D	9ED	E	9EE	F
0	5 BRSET0 3 DIR	4 BSET0 2 DIR	3 BRA 2 REL	4 NEG 2 DIR	1 NEGA 1 INH	1 NEGX 1 INH	4 NEG 2 IX1	5 NEG 3 SP1	3 NEG 1 IX	7 RTI 1 INH	3 BGE 2 REL	2 SUB 2 IMM	3 SUB 2 DIR	4 SUB 3 EXT	4 SUB 3 IX2	5 SUB 4 SP2	3 SUB 2 IX1	4 SUB 3 SP1	2 SUB 1 IX
1	5 BRCLR0 3 DIR	4 BCLR0 2 DIR	3 BRN 2 REL	5 CBEQ 3 DIR	4 CBEQA 3 IMM	4 CBEQX 3 IMM	5 CBEQ 3 IX1+	6 CBEQ 4 SP1	4 CBEQ 2 IX+	4 RTS 1 INH	3 BLT 2 REL	2 CMP 2 IMM	3 CMP 2 DIR	4 CMP 3 EXT	4 CMP 3 IX2	5 CMP 4 SP2	3 CMP 2 IX1	4 CMP 3 SP1	2 CMP 1 IX
2	5 BRSET1 3 DIR	4 BSET1 2 DIR	3 BHI 2 REL		5 MUL 1 INH	7 DIV 1 INH	3 NSA 1 INH		2 DAA 1 INH		3 BGT 2 REL	2 SBC 2 IMM	3 SBC 2 DIR	4 SBC 3 EXT	4 SBC 3 IX2	5 SBC 4 SP2	3 SBC 2 IX1	4 SBC 3 SP1	2 SBC 1 IX
3	5 BRCLR1 3 DIR	4 BCLR1 2 DIR	3 BLS 2 REL	4 COM 2 DIR	1 COMA 1 INH	1 COMX 1 INH	4 COM 2 IX1	5 COM 3 SP1	3 COM 1 IX	9 SWI 1 INH	3 BLE 2 REL	2 CPX 2 IMM	3 CPX 2 DIR	4 CPX 3 EXT	4 CPX 3 IX2	5 CPX 4 SP2	3 CPX 2 IX1	4 CPX 3 SP1	2 CPX 1 IX
4	5 BRSET2 3 DIR	4 BSET2 2 DIR	3 BCC 2 REL	4 LSR 2 DIR	1 LSRA 1 INH	1 LSRX 1 INH	4 LSR 2 IX1	5 LSR 3 SP1	3 LSR 1 IX	2 TAP 1 INH	2 TXS 1 INH	2 AND 2 IMM	3 AND 2 DIR	4 AND 3 EXT	4 AND 3 IX2	5 AND 4 SP2	3 AND 2 IX1	4 AND 3 SP1	2 AND 1 IX
5	5 BRCLR2 3 DIR	4 BCLR2 2 DIR	3 BCS 2 REL	4 STHX 2 DIR	3 LDHX 3 IMM	4 LDHX 2 DIR	3 CPHX 3 IMM		4 CPHX 2 DIR	1 TPA 1 INH	2 TSX 1 INH	2 BIT 2 IMM	3 BIT 2 DIR	4 BIT 3 EXT	4 BIT 3 IX2	5 BIT 4 SP2	3 BIT 2 IX1	4 BIT 3 SP1	2 BIT 1 IX
6	5 BRSET3 3 DIR	4 BSET3 2 DIR	3 BNE 2 REL	4 ROR 2 DIR	1 RORA 1 INH	1 RORX 1 INH	4 ROR 2 IX1	5 ROR 3 SP1	3 ROR 1 IX	2 PULA 1 INH		2 LDA 2 IMM	3 LDA 2 DIR	4 LDA 3 EXT	4 LDA 3 IX2	5 LDA 4 SP2	3 LDA 2 IX1	4 LDA 3 SP1	2 LDA 1 IX
7	5 BRCLR3 3 DIR	4 BCLR3 2 DIR	3 BEQ 2 REL	4 ASR 2 DIR	1 ASRA 1 INH	1 ASRX 1 INH	4 ASR 2 IX1	5 ASR 3 SP1	3 ASR 1 IX	2 PSHA 1 INH	1 TAX 1 INH	2 AIS 2 IMM	3 STA 2 DIR	4 STA 3 EXT	4 STA 3 IX2	5 STA 4 SP2	3 STA 2 IX1	4 STA 3 SP1	2 STA 1 IX
8	5 BRSET4 3 DIR	4 BSET4 2 DIR	3 BHCC 2 REL	4 LSL 2 DIR	1 LSLA 1 INH	1 LSLX 1 INH	4 LSL 2 IX1	5 LSL 3 SP1	3 LSL 1 IX	2 PULX 1 INH	1 CLC 1 INH	2 EOR 2 IMM	3 EOR 2 DIR	4 EOR 3 EXT	4 EOR 3 IX2	5 EOR 4 SP2	3 EOR 2 IX1	4 EOR 3 SP1	2 EOR 1 IX
9	5 BRCLR4 3 DIR	4 BCLR4 2 DIR	3 BHCS 2 REL	4 ROL 2 DIR	1 ROLA 1 INH	1 ROLX 1 INH	4 ROL 2 IX1	5 ROL 3 SP1	3 ROL 1 IX	2 PSHX 1 INH	1 SEC 1 INH	2 ADC 2 IMM	3 ADC 2 DIR	4 ADC 3 EXT	4 ADC 3 IX2	5 ADC 4 SP2	3 ADC 2 IX1	4 ADC 3 SP1	2 ADC 1 IX
A	5 BRSET5 3 DIR	4 BSET5 2 DIR	3 BPL 2 REL	4 DEC 2 DIR	1 DECA 1 INH	1 DECX 1 INH	4 DEC 2 IX1	5 DEC 3 SP1	3 DEC 1 IX	2 PULH 1 INH	2 CLI 1 INH	2 ORA 2 IMM	3 ORA 2 DIR	4 ORA 3 EXT	4 ORA 3 IX2	5 ORA 4 SP2	3 ORA 2 IX1	4 ORA 3 SP1	2 ORA 1 IX
B	5 BRCLR5 3 DIR	4 BCLR5 2 DIR	3 BMI 2 REL	5 DBNZ 3 DIR	3 DBNZA 2 INH	3 DBNZX 2 INH	5 DBNZ 3 IX1	6 DBNZ 4 SP1	4 DBNZ 2 IX	2 PSHH 1 INH	2 SEI 1 INH	2 ADD 2 IMM	3 ADD 2 DIR	4 ADD 3 EXT	4 ADD 3 IX2	5 ADD 4 SP2	3 ADD 2 IX1	4 ADD 3 SP1	2 ADD 1 IX
C	5 BRSET6 3 DIR	4 BSET6 2 DIR	3 BMC 2 REL	4 INC 2 DIR	1 INCA 1 INH	1 INCX 1 INH	4 INC 2 IX1	5 INC 3 SP1	3 INC 1 IX	1 CLRH 1 INH	1 RSP 1 INH		2 JMP 2 DIR	3 JMP 3 EXT	4 JMP 3 IX2		3 JMP 2 IX1		2 JMP 1 IX
D	5 BRCLR6 3 DIR	4 BCLR6 2 DIR	3 BMS 2 REL	3 TST 2 DIR	1 TSTA 1 INH	1 TSTX 1 INH	3 TST 2 IX1	4 TST 3 SP1	2 TST 1 IX		1 NOP 1 INH	4 BSR 2 REL	4 JSR 2 DIR	5 JSR 3 EXT	6 JSR 3 IX2		5 JSR 2 IX1		4 JSR 1 IX
E	5 BRSET7 3 DIR	4 BSET7 2 DIR	3 BIL 2 REL		5 MOV 3 DD	4 MOV 2 DIX+	4 MOV 3 IMD		4 MOV 2 IX+D	1 STOP 1 INH	*	2 LDX 2 IMM	3 LDX 2 DIR	4 LDX 3 EXT	4 LDX 3 IX2	5 LDX 4 SP2	3 LDX 2 IX1	4 LDX 3 SP1	2 LDX 1 IX
F	5 BRCLR7 3 DIR	4 BCLR7 2 DIR	3 BIH 2 REL	3 CLR 2 DIR	1 CLRA 1 INH	1 CLRX 1 INH	3 CLR 2 IX1	4 CLR 3 SP1	2 CLR 1 IX	1 WAIT 1 INH	1 TXA 1 INH	2 AIX 2 IMM	3 STX 2 DIR	4 STX 3 EXT	4 STX 3 IX2	5 STX 4 SP2	3 STX 2 IX1	4 STX 3 SP1	2 STX 1 IX

INH Inherent
IMM Immediate
DIR Direct
EXT Extended
DD Direct-Direct
IX+D Indexed-Direct
REL Relative
IX Indexed, No Offset
IX1 Indexed, 8-Bit Offset
IX2 Indexed, 16-Bit Offset
IMD Immediate-Direct
DIX+ Direct-Indexed
SP1 Stack Pointer, 8-Bit Offset
SP2 Stack Pointer, 16-Bit Offset
IX+ Indexed, No Offset with Post Increment
IX1+ Indexed, 1-Byte Offset with Post Increment

*Pre-byte for stack pointer indexed instructions

Low Byte of Opcode in Hexadecimal

MSB / LSB	0
0	5 BRSET0 3 DIR

High Byte of Opcode in Hexadecimal
Cycles
Opcode Mnemonic
Number of Bytes / Addressing Mode

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Section 6. Internal Clock Generator Module (ICG)

6.1 Introduction

The internal clock generator module (ICG) is used to create a stable clock source for the microcontroller without using any external components. The ICG generates the oscillator output clock (CGMXCLK), which is used by the COP, LVI, and other modules. The ICG also generates the clock generator output (CGMOUT), which is fed to the system integration module (SIM) to create the bus clocks. The bus frequency will be one-fourth the frequency of CGMXCLK and one-half the frequency of CGMOUT.

6.2 Features

The ICG has these features:

- External clock generator, either 1-pin external source or 2-pin crystal
- Internal clock generator with programmable frequency output in integer multiples of a nominal frequency (307.2 kHz ±25 percent)
- Frequency adjust (trim) register to improve variability to ±2 percent
- Bus clock software selectable from either internal or external clock
- Clock monitor for both internal and external clocks

6.3 Functional Description

The ICG, shown in **Figure 6-1**, contains these major submodules:

- Clock enable circuit
- Internal clock generator
- External clock generator
- Clock monitor circuit
- Clock selection circuit

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Internal Clock Generator Module (ICG)

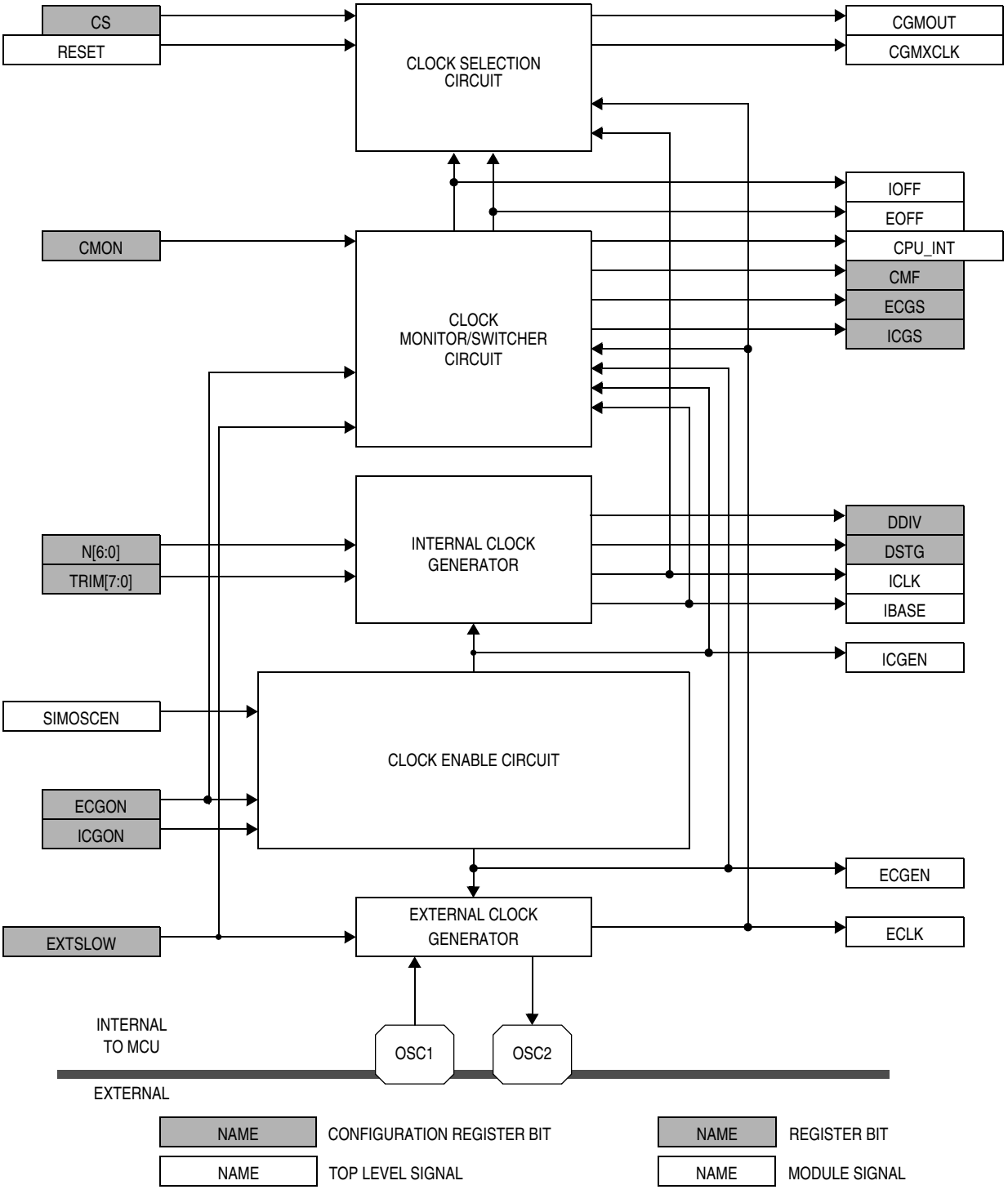

Figure 6-1. ICG Module Block Diagram

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6.3.1 Clock Enable Circuit

The clock enable circuit is used to enable the internal clock (ICLK) or external clock (ECLK). The clock enable circuit generates an ICG stop (ICGSTOP) signal which stops all clocks (ICLK, ECLK, and the low-frequency base clock, IBASE) low. ICGSTOP is set and the ICG is disabled in stop mode.

The internal clock enable signal (ICGEN) turns on the internal clock generator which generates ICLK. ICGEN is set (active) whenever the ICGON bit is set and the ICGSTOP signal is clear. When ICGEN is clear, ICLK and IBASE are both low.

The external clock enable signal (ECGEN) turns on the external clock generator which generates ECLK. ECGEN is set (active) whenever the ECGON bit is set and the ICGSTOP signal is clear. When ECGEN is clear, ECLK is low.

6.3.2 Internal Clock Generator

The internal clock generator, shown in **Figure 6-2**, creates a low-frequency base clock (IBASE), which operates at a nominal frequency (f_{NOM}) of 307.2 kHz ±25 percent, and an internal clock (ICLK) which is an integer multiple of IBASE. This multiple is the ICG multiplier factor (N), which is programmed in the ICG multiplier register (ICGMR). The internal clock generator is turned off and the output clocks (IBASE and ICLK) are held low when the internal clock generator enable signal (ICGEN) is clear.

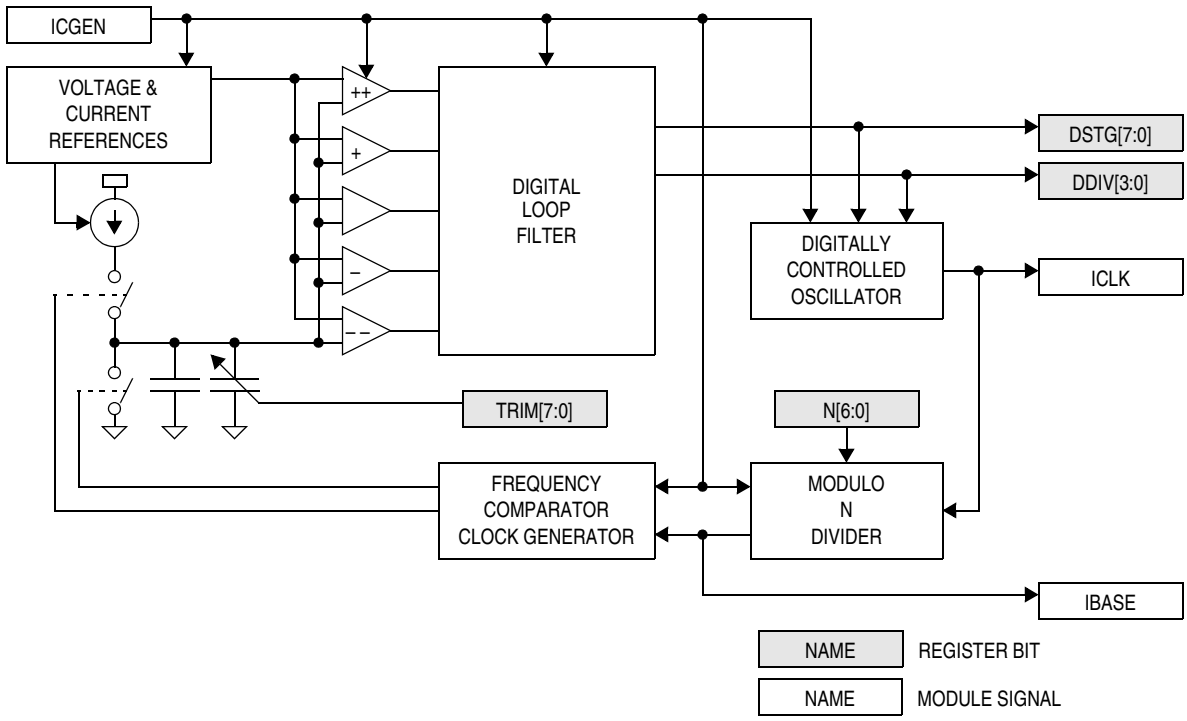

Figure 6-2. Internal Clock Generator Block Diagram

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The internal clock generator contains:

- A digitally controlled oscillator
- A modulo N divider
- A frequency comparator, which contains voltage and current references, a frequency to voltage converter, and comparators
- A digital loop filter

6.3.2.1 Digitally Controlled Oscillator

The digitally controlled oscillator (DCO) is an inaccurate oscillator which generates the internal clock (ICLK). The clock period of ICLK is dependent on the digital loop filter outputs (DSTG[7:0] and DDIV[3:0]). Because there is only a limited number of bits in DDIV and DSTG, the precision of the output (ICLK) is restricted to a long-term precision of approximately ±0.202 percent to ±0.368 percent when measured over several cycles (of the desired frequency). Additionally, since the propagation delays of the devices used in the DCO ring oscillator are a measurable fraction of the bus clock period, reaching the long-term precision may require alternately running faster and slower than desired, making the worst case cycle-to-cycle frequency variation ±6.45 percent to ±11.8 percent (of the desired frequency). The valid values of DDIV:DSTG range from $000 to $9FF. For more information on the quantization error in the DCO, see **6.4.4 Quantization Error in DCO Output**.

6.3.2.2 Modulo N Divider

The modulo N divider creates the low-frequency base clock (IBASE) by dividing the internal clock (ICLK) by the ICG multiplier factor (N) contained in the ICG multiplier register (ICGMR). When N is programmed to a $01 or $00, the divider is disabled and ICLK is passed through to IBASE undivided. When the internal clock generator is stable, the frequency of IBASE will be equal to the nominal frequency (f_{NOM}) of 307.2 kHz ±25 percent.

6.3.2.3 Frequency Comparator

The frequency comparator effectively compares the low-frequency base clock (IBASE) to a nominal frequency, f_{NOM}. First, the frequency comparator converts IBASE to a voltage by charging a known capacitor with a current reference for a period dependent on IBASE. This voltage is compared to a voltage reference with comparators, whose outputs are fed to the digital loop filter. The dependence of these outputs on the capacitor size, current reference, and voltage reference causes up to ±25 percent error in f_{NOM}.

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6.3.2.4 Digital Loop Filter

The digital loop filter (DLF) uses the outputs of the frequency comparator to adjust the internal clock (ICLK) clock period. The DLF generates the DCO divider control bits (DDIV[3:0]) and the DCO stage control bits (DSTG[7:0]), which are fed to the DCO. The DLF first concatenates the DDIV and DSTG registers (DDIV[3:0]:DSTG[7:0]) and then adds or subtracts a value dependent on the relative error in the low-frequency base clock's period, as shown in **Table 6-1**. In some extreme error conditions, such as operating at a V_{DD} level which is out of specification, the DLF may attempt to use a value above the maximum ($9FF) or below the minimum ($000). In both cases, the value for DDIV will be between $A and $F. In this range, the DDIV value will be interpreted the same as $9 (the slowest condition). Recovering from this condition requires subtracting (increasing frequency) in the normal fashion until the value is again below $9FF (if the desired value is $9xx, the value may settle at $Axx through $Fxx, an acceptable operating condition). If the error is less than ±5 percent, the internal clock generator's filter stable indicator (FICGS) is set, indicating relative frequency accuracy to the clock monitor.

Table 6-1. Correction Sizes from DLF to DCO

Frequency Error of IBASE Compared to f_{NOM}	DDVI[3:0]:DSTG[7:0] Correction	Current to New DDIV[3:0]:DSTG[7:0]		Relative Correction in DCO	
IBASE < 0.85 f_{NOM}	–32 (–$020)	Min	$xFF to $xDF	–2/31	–6.45%
		Max	$x20 to $x00	–2/19	–10.5%
0.85 f_{NOM} < IBASE IBASE < 0.95 f_{NOM}	–8 (–$008)	Min	$xFF to $xF7	–0.5/31	–1.61%
		Max	$x08 to $x00	–0.5/17.5	–2.86%
0.95 f_{NOM} < IBASE IBASE < f_{NOM}	–1 (–$001)	Min	$xFF to $xFE	–0.0625/31	–0.202%
		Max	$x01 to $x00	–0.0625/17.0625	–0.366%
f_{NOM} < IBASE IBASE < 1.05 f_{NOM}	+1 (+$001)	Min	$xFE to $xFF	+0.0625/30.9375	+0.202%
		Max	$x00 to $x01	+0.0625/17	+0.368%
1.05 f_{NOM} < IBASE IBASE < 1.15 f_{NOM}	+8 (+$008)	Min	$xF7 to $xFF	+0.5/30.5	+1.64%
		Max	$x00 to $x08	+0.5/17	+2.94%
1.15 f_{NOM} < IBASE	+32 (+$020)	Min	$xDF to $xFF	+2/29	+6.90%
		Max	$x00 to $x20	+2/17	+11.8%

x: Maximum error is independent of value in DDIV[3:0]. DDIV increments or decrements when an addition to DSTG[7:0] carries or borrows.

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6.3.3 External Clock Generator

The ICG also provides for an external oscillator or clock source, if desired. The external clock generator, shown in **Figure 6-3**, contains an external oscillator amplifier and an external clock input path.

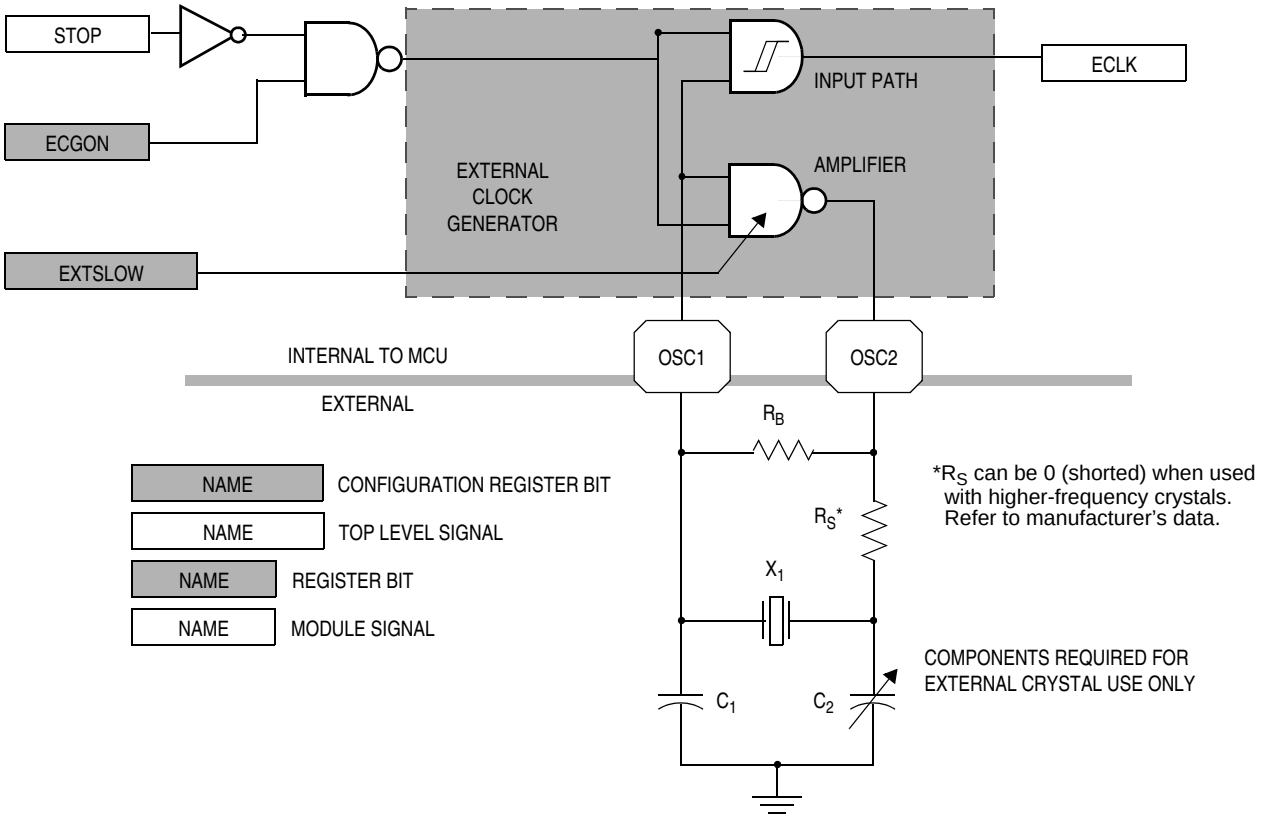

Figure 6-3. External Clock Generator Block Diagram

6.3.3.1 External Oscillator Amplifier

The external oscillator amplifier provides the gain required by an external crystal connected in a Pierce oscillator configuration. The amount of this gain is controlled by the slow external (EXTSLOW) bit in the configuration register. When EXTSLOW is set, the amplifier gain is reduced for operating low-frequency crystals (32 kHz to 100 kHz). When EXTSLOW is clear, the amplifier gain will be sufficient for 1-MHz to 8-MHz crystals. EXTSLOW must be configured correctly for the given crystal or the circuit may not operate.

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The amplifier is enabled when the ECGON bit is set and stop mode is not enabled. When the amplifier is enabled, it will be connected between the OSC1 and OSC2 pins. In its typical configuration, the external oscillator requires five external components:

1. Crystal, X_1
2. Fixed capacitor, C_1
3. Tuning capacitor, C_2 (can also be a fixed capacitor)
4. Feedback resistor, R_B
5. Series resistor, R_S (included in the diagram to follow strict Pierce oscillator guidelines and may not be required for all ranges of operation, especially with high frequency crystals). Refer to the crystal manufacturer's data for more information.

6.3.3.2 External Clock Input Path

The external clock input path is the means by which the microcontroller uses an external clock source. The input to the path is the OSC1 pin and the output is the external clock (ECLK). The path, which contains input buffering, is enabled when the ECGON bit is set and stop mode is not enabled.

6.3.4 Clock Monitor Circuit

The ICG contains a clock monitor circuit which, when enabled, will continuously monitor both the external clock (ECLK) and the internal clock (ICLK) to determine if either clock source has failed based on these conditions:

- Either ICLK or ECLK has stopped.
- The frequency of IBASE < frequency EREF divided by 4
- The frequency of ECLK < frequency of IREF divided by 4

Using the clock monitor requires both clocks to be active (ECGON and ICGON are both set). To enable the clock monitor, both clocks must also be stable (ECGS and ICGS both set). This is to prevent the use of the clock monitor when a clock is first turned on and potentially unstable

NOTE: *Although the clock monitor can be enabled only when the both clocks are stable (ICGS or ECGS is set), the clock monitor will remain enabled if one of the clocks goes unstable.*

The clock monitor only works if the external slow (EXTSLOW) bit in the configuration register is properly defined with respect to the external frequency source.

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The clock monitor circuit, shown in **Figure 6-4**, contains these blocks:

- Clock monitor reference generator
- Internal clock activity detector
- External clock activity detector

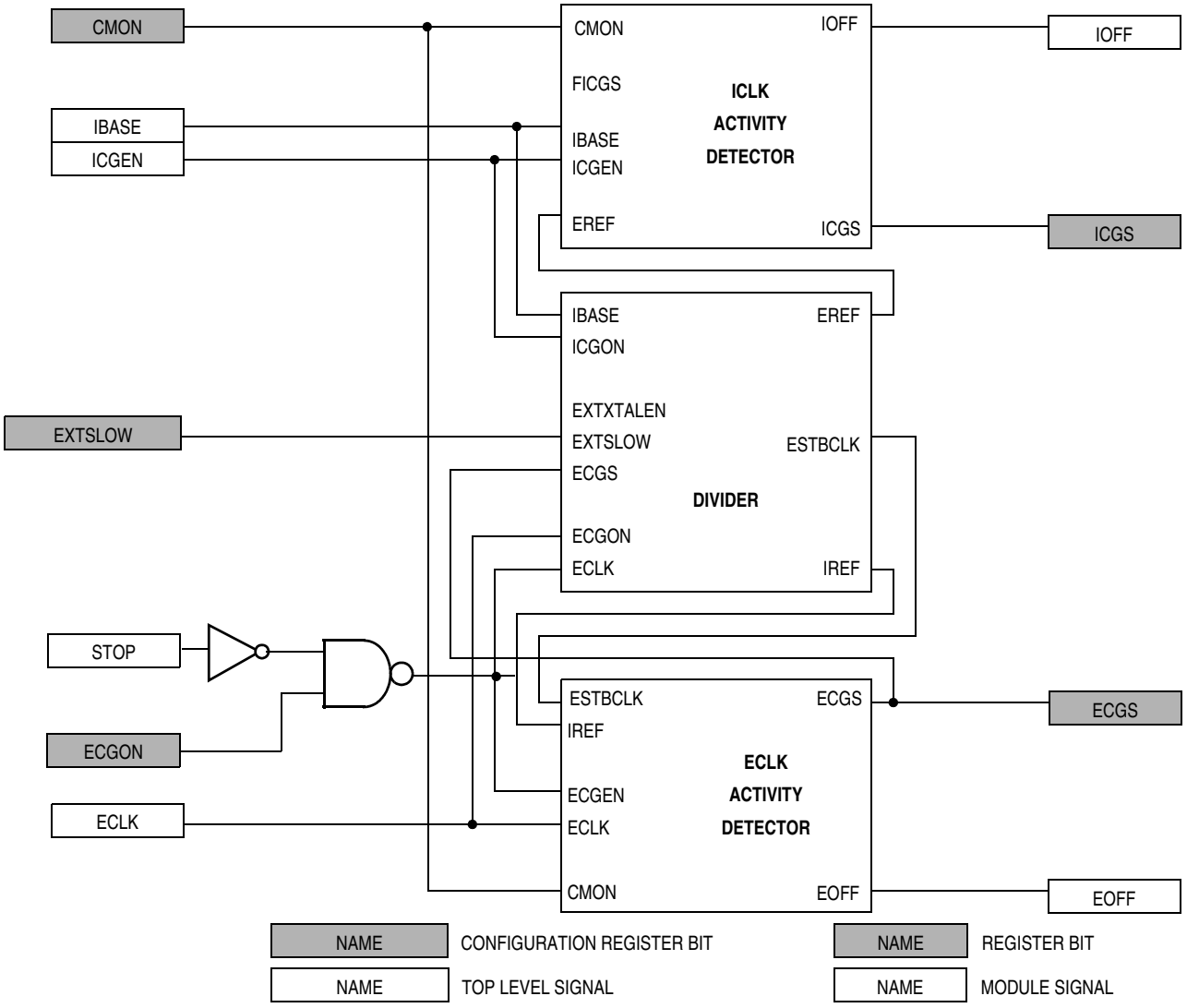

Figure 6-4. Clock Monitor Block Diagram

6.3.4.1 Clock Monitor Reference Generator

The clock monitor uses a reference based on one clock source to monitor the other clock source. The clock monitor reference generator generates the external reference clock (EREF) based on the external clock (ECLK) and the internal reference clock (IREF) based on the internal clock (ICLK). To simplify the circuit,

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the low-frequency base clock (IBASE) is used in place of ICLK because it always operates at or near 307.2 kHz. For proper operation, EREF must be at least twice as slow as IBASE and IREF must be at least twice as slow as ECLK.

To guarantee that IREF is slower than ECLK and EREF is slower than IBASE, one of the signals is divided down. Which signal is divided and by how much is determined by the external slow (EXTSLOW) bit in the configuration register, according to the rules in **Table 6-2**. Note that each signal (IBASE and ECLK) is always divided by four. A longer divider is used on either IBASE or ECLK based on the EXTSLOW bit.

NOTE: *If EXTSLOW is not set according to the rules defined in **Table 6-2**, the clock monitor could switch clock sources unexpectedly.*

The long divider (divide by 4096) is also used as an external crystal stabilization divider. The divider is reset when the external clock generator is off (ECGEN is clear). When the external clock generator is first turned on, the external clock generator stable bit (ECGS) will be clear. This condition automatically selects ECLK as the input to the long divider. The external stabilization clock (ESTBCLK) will be ECLK divided by 4096. This timeout allows the crystal to stabilize. The falling edge of ESTBCLK is used to set ECGS. (ECGS will set after a full 16 or 4096 cycles.) When ECGS is set, the divider returns to its normal function. ESTBCLK may be generated by either IBASE or ECLK, but any clocking will reinforce only the set condition. If ECGS is cleared because the clock monitor determined that ECLK was inactive, the divider will revert to a stabilization divider. Since this will change the EREF and IREF divide ratios, it is important to turn the clock monitor off (CMON = 0) after inactivity is detected to ensure valid recovery.

Table 6-2. Clock Monitor Reference Divider Ratios

ICGON	ECGON	ECGS	EXTSLOW	External Frequency		EREF Divider Ratio	EREF Frequency	ESTBCLK Divider Ratio	ESTBCLK Frequency	IREF Divider Ratio	IREF Frequency
0	x	x	x	U		U	U	U	U	Off	0
x	0	0	x	0		Off	0	Off	0	U	U
x	x	0	x	Min	30 kHz	Off	0	4096 (ECLK)	1.875 kHz	1*4	76.8 kHz ±25%
				Max	8 MHz				500 kHz		
x	x	1	0	Min	1 MHz	128*4	1.953 kHz	4096 (ECLK)	244 Hz	1*4	76.8 kHz ±25%
				Max	8 MHz		15.63 kHz		1.953 kHz		
x	x	1	1	Min	30 kHz	1*4	7.5 kHz	4096 (IBASE)	75 Hz ±25%	16*4	4.8 kHz ±25%
				Max	100 kHz		25.0 kHz				

U: Unaffected. Refer to section of table where ICGON or ECGON is set to x (don't care).
IBASE is always used as the internal frequency (307.2 kHz).

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6.3.4.2 Internal Clock Activity Detector

The internal clock activity detector looks for at least one falling edge on the low-frequency base clock (IBASE) every time the external reference (EREF) is low. Since EREF is less than half the frequency of IBASE, this should occur every time. If it does not occur two consecutive times, the internal clock inactivity indicator (IOFF) is set. IOFF will be cleared the next time there is a falling edge of IBASE while EREF is low.

The internal clock stable bit (ICGS) is set when IBASE is within approximately 5 percent of the target 307.2 kHz ±25 percent for two consecutive measurements. ICGS is cleared when IBASE is outside the 5 percent of the target 307.2 kHz ±25 percent, the internal clock generator is disabled (ICGEN is clear), or when IOFF is set.

6.3.4.3 External Clock Activity Detector

The external clock activity detector looks for at least one falling edge on the external clock (ECLK) every time the internal reference (IREF) is low. Since IREF is less than half the frequency of ECLK, this should occur every time. If it does not occur two consecutive times, the external clock inactivity indicator (EOFF) is set. EOFF will be cleared the next time there is a falling edge of ECLK while IREF is low.

The external clock stable bit (ECGS) is also generated in the external clock activity detector. ECGS is set on a falling edge of the external stabilization clock (ESTBCLK). This will be 4096 ECLK cycles after the external clock generator on bit (ECGON) is set. ECGS is cleared when the external clock generator is disabled (ECGON is clear) or when EOFF is set.

6.3.5 Clock Selection Circuit

The clock selection circuit, shown in **Figure 6-5**, contains two clock switches which generate the oscillator output clock (CGMXCLK) from either the internal clock (ICLK) or the external clock (ECLK). The clock selection circuit also contains a divide-by-two circuit which creates the clock generator output clock (CGMOUT), which generates the bus clocks.

6.3.5.1 Clock Selection Switch

The clock select switch creates the oscillator output clock (CGMXCLK) from either the internal clock (ICLK) or the external clock (ECLK), based on the clock select bit (CS; set selects ECLK, clear selects ICLK). When switching the CS bit, both ICLK and ECLK must be on (ICGON and ECGON set). The clock being switched to must also be stable (ICGS or ECGS set).

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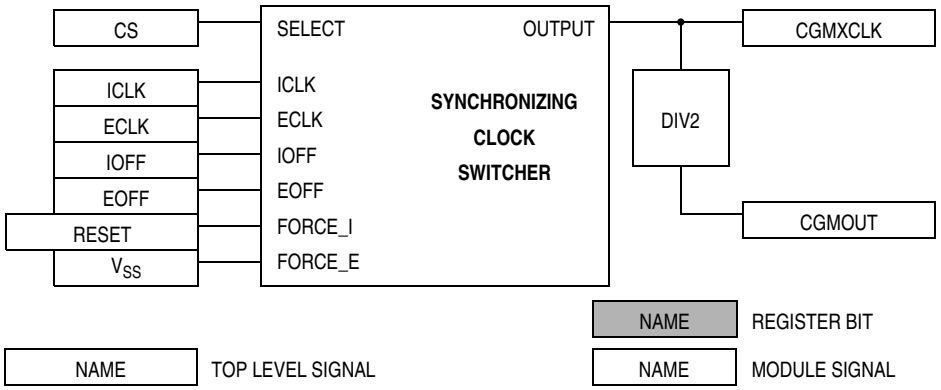
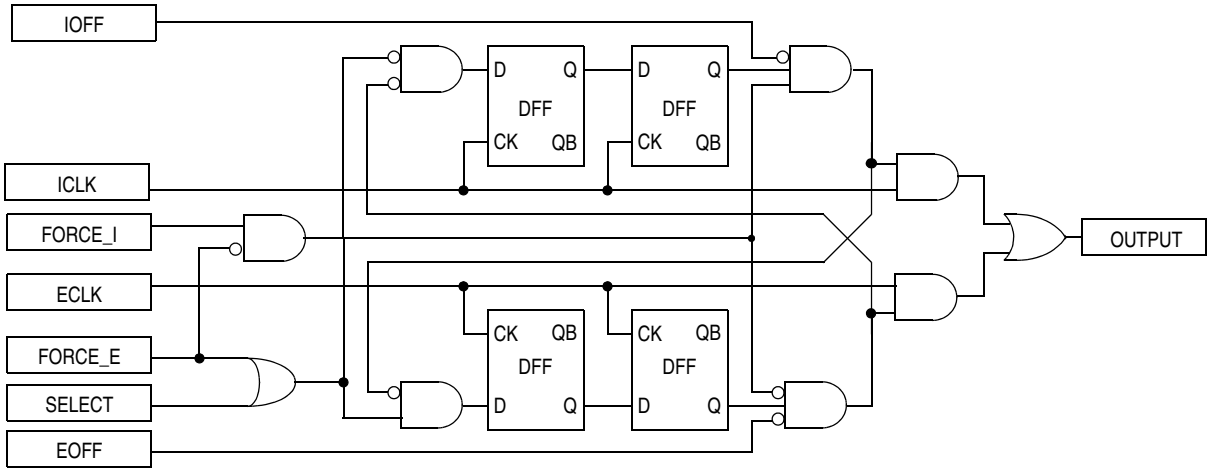


Figure 6-5. Clock Selection Circuit Block Diagram

6.3.5.2 Clock Switching Circuit

To robustly switch between the internal clock (ICLK) and the external clock (ECLK), the switch assumes the clocks are completely asynchronous, so a synchronizing circuit is required to make the transition (see **Figure 6-6**). When the clock select bit is changed, the switch will continue to operate off the original clock for between 1 and 2 cycles as the select input transitions through one side of the synchronizer. Next, the output will be held low for between 1 and 2 cycles of the new clock as the select input transitions through the other side. Then the output starts switching at the new clock's frequency. This transition guarantees that no glitches will be seen on the output even though the select input may change asynchronously to the clocks. The unpredictably of the transition period is a necessary result of the asynchronicity.



FORCE_I = Force internal; reset condition

FORCE_E = Force external

Figure 6-6. Synchronizing Clock Switcher Circuit Diagram

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The switch automatically selects ICLK during reset. When the clock monitor is on (CMON is set) and it determines one of the clock sources is inactive (as indicated by the IOFF or EOFF signals), the circuit is forced to select the active clock. There are no clocks for the inactive side of the synchronizer to properly operate, so that side is forced deselected. However, the active side will not be selected until one to two clock cycles after the IOFF or EOFF signal transitions.

6.4 Usage Notes

The ICG has several features which can provide protection to the microcontroller if properly used. There are other features which can greatly simplify usage of the ICG if certain techniques are employed. This section will describe several possible ways to use the ICG and its features. These techniques are not the only ways to use the ICG, and may not be optimum for all environments. In any case, these techniques should be used only as a template, and the user should modify them according to the application's requirements.

These notes include:

- Switching clock sources
- Enabling the clock monitor
- Using clock monitor interrupts
- Quantization error in DCO output
- Switching internal clock frequencies
- Nominal frequency settling time
- Improving frequency settling time
- Trimming frequency

6.4.1 Switching Clock Sources

Switching from one clock source to another requires both clock sources to be enabled and stable. A simple flow requires:

1. Enable desired clock source
2. Wait for it to become stable
3. Switch clocks
4. Disable previous clock source

The key point to remember in this flow is that the clock source cannot be switched (CS cannot be written) unless the desired clock is on and stable.

A short assembly code example of how to employ this flow is shown in **Figure 6-7**. This code is for illustrative purposes only and does not represent valid syntax for any particular assembler.

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```
                        ;Clock Switching Code Example
                        ;This code switches from Internal to External clock
                        ;Clock Monitor and interrupts are not enabled
start   lda     #$13    ;Mask for CS, ECGON, ECGS
                        ;If switching from External to Internal, mask is $0C.
loop    **      **      ;Other code here, such as writing the COP, since ECGS may
                        ;take some time to set
        sta     icgcr   ;Try to set CS, ECGON and clear ICGON. ICGON will not
                        ;clear until CS is set, and CS will not set until
                        ;ECGON and ECGS are set.
        cmpa    icgcr   ;Check to see if ECGS set, then CS set, then ICGON clear
        bne     loop    ;Keep looping until ICGON is clear.
```

Figure 6-7. Code Example for Switching Clock Sources

6.4.2 Enabling the Clock Monitor

Many applications require the clock monitor to determine if one of the clock sources has become inactive, so the other can be used to recover from a potentially dangerous situation. Using the clock monitor requires both clocks to be active (ECGON and ICGON both set). To enable the clock monitor, both clocks also must be stable (ECGS and ICGS both set). This is to prevent the use of the clock monitor when a clock is first turned on and potentially unstable.

Enabling the clock monitor and clock monitor interrupts requires a flow similar to this flow:

1. Enable the alternate clock source
2. Wait for both clock sources to be stable
3. Switch to the desired clock source if necessary
4. Enable the clock monitor
5. Enable clock monitor interrupts

These events must happen in sequence. A short assembly code example of how to employ this flow is shown in **Figure 6-8**. This code is for illustrative purposes only and does not represent valid syntax for any particular assembler.

```
                            ;Clock Monitor Enabling Code Example
                            ;This code turns on both clocks, selects the desired
                            ; one, then turns on the Clock Monitor and Interrupts
start   lda     #$AF        ;Mask for CMIE, CMON, ICGON, ICGS, ECGON, ECGS
                            ; If Internal Clock desired, mask is $AF
                            ; If External Clock desired, mask is $BF
                            ; If interrupts not desired mask is $2F int; $3F ext
loop    **      **          ;Other code here, such as writing the COP, since ECGS
                            ; and ICGS may take some time to set.
        sta     icgcr       ;Try to set CMIE. CMIE wont set until CMON set; CMON
                            ; won't set until ICGON, ICGS, ECGON, ECGS set.
        brset   6,ICGCR,error ;Verify CMF is not set
        cmpa    icgcr       ;Check if ECGS set, then CMON set, then CMIE set
        bne     loop        ;Keep looping until CMIE is set.
```

Figure 6-8. Code Example for Enabling the Clock Monitor

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6.4.3 Clock Monitor Interrupts

The clock monitor circuit can be used to recover from perilous situations such as crystal loss. To use the clock monitor effectively, these notes should be observed:

- Enable the clock monitor and clock monitor interrupts.
- The first statement in the clock monitor interrupt service routine should be a read to the ICG control register (ICGCR) to verify that the clock monitor flag (CMF) is set. This is also the first step in clearing the CMF bit.
- Never use BSET or BCLR instructions on the ICGCR, as this may inadvertently clear CMF. Only use the BRSET and BRCLR instructions to check the CMF bit and not to check any other bits in the ICGCR.
- When the clock monitor detects inactivity on the selected clock source (defined by the CS bit of the ICG control register), the inactive clock is deselected automatically and the remaining active clock is selected as the source for CGMXCLK. The interrupt service routine can use the state of the CS bit to check which clock is inactive.
- When the clock monitor detects inactivity, the application may have been subjected to extreme conditions which may have affected other circuits. The clock monitor interrupt service routine should take any appropriate precautions.

6.4.4 Quantization Error in DCO Output

The digitally controlled oscillator (DCO) is comprised of three major sub-blocks:

1. Binary weighted divider
2. Variable-delay ring oscillator
3. Ring oscillator fine-adjust circuit

Each of these blocks affects the clock period of the internal clock (ICLK). Since these blocks are controlled by the digital loop filter (DLF) outputs DDIV and DSTG, the output of the DCO can change only in quantized steps as the DLF increments or decrements its output. The following sections describe how each block will affect the output frequency.

6.4.4.1 Digitally Controlled Oscillator

The digitally controlled oscillator (DCO) is an inaccurate oscillator which generates the internal clock (ICLK), whose clock period is dependent on the digital loop filter outputs (DSTG[7:0] and DDIV[3:0]). Because of the digital nature of the DCO, the clock period of ICLK will change in quantized steps. This will create a clock period difference or quantization error (Q-ERR) from one cycle to the next. Over several cycles or for longer periods, this error is divided out until it reaches a minimum error of 0.202 percent to 0.368 percent. The dependence of this error on the DDIV[3:0] value and the number of cycles the error is measured over is shown in **Table 6-3**.

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Table 6-3. Quantization Error in ICLK

DDIV[3:0]	ICLK Cycles	Bus Cycles	t_{ICLK} Q-ERR
%0000 (min)	4	1	1.61%–2.94%
%0000 (min)	≥ 32	≥ 8	0.202%–0.368%
%0001	4	1	0.806%–1.47%
%0001	≥ 16	≥ 4	0.202%–0.368%
%0010	4	1	0.403%–0.735%
%0010	≥ 8	≥ 2	0.202%–0.368%
%0011	≥ 4	≥ 1	0.202%–0.368%
%0100	≥ 2	≥ 1	0.202%–0.368%
%0101–%1001 (max)	≥ 1	≥ 1	0.202%–0.368%

6.4.4.2 Binary Weighted Divider

The binary weighted divider divides the output of the ring oscillator by a power of 2, specified by the DCO divider control bits (DDIV[3:0]). DDIV maximizes at %1001 (values of %1010 through %1111 are interpreted as %1001), which corresponds to a divide by 512. When DDIV is %0000, the ring oscillator's output is divided by 1. Incrementing DDIV by 1 will double the period; decrementing DDIV will halve the period. The DLF cannot directly increment or decrement DDIV; DDIV is only incremented or decremented when an addition or subtraction to DSTG carries or borrows.

6.4.4.3 Variable-Delay Ring Oscillator

The variable-delay ring oscillator's period is adjustable from 17 to 31 stage delays, in increments of two, based on the upper three DCO stage control bits (DSTG[7:5]). A DSTG[7:5] of %000 corresponds to 17 stage delays; DSTG[7:5] of %111 corresponds to 31 stage delays. Adjusting the DSTG[5] bit has a 6.45 percent to 11.8 percent effect on the output frequency. This also corresponds to the size correction made when the frequency error is greater than ±15 percent. The value of the binary weighted divider does not affect the relative change in output clock period for a given change in DSTG[7:5].

6.4.4.4 Ring Oscillator Fine-Adjust Circuit

The ring oscillator fine-adjust circuit causes the ring oscillator to effectively operate at non-integer numbers of stage delays by operating at two different points for a variable number of cycles specified by the lower five DCO stage control bits (DSTG[4:0]). For example, when DSTG[7:5] is %011, the ring oscillator nominally operates at 23 stage delays. When DSTG[4:0] is %00000, the ring will always operate at 23 stage delays. When DSTG[4:0] is %00001, the ring will operate at 25 stage delays for one of 32 cycles and at 23 stage delays for 31 of 32 cycles.

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Likewise, when DSTG[4:0] is %11111, the ring operates at 25 stage delays for 31 of 32 cycles and at 23 stage delays for one of 32 cycles. When DSTG[7:5] is %111, similar results are achieved by including a variable divide-by-two, so the ring operates at 31 stages for some cycles and at 17 stage delays, with a divide-by-two for an effective 34 stage delays, for the remainder of the cycles. Adjusting the DSTG[0] bit has a 0.202 percent to 0.368 percent effect on the output clock period. This corresponds to the minimum size correction made by the DLF, and the inherent, long-term quantization error in the output frequency.

6.4.5 Switching Internal Clock Frequencies

The frequency of the internal clock (ICLK) may need to be changed for some applications. For example, if the reset condition does not provide the correct frequency, or if the clock is slowed down for a low-power mode (or sped up after a low-power mode), the frequency must be changed by programming the internal clock multiplier factor (N). The frequency of ICLK is N times the frequency of IBASE, which is 307.2 kHz ±25 percent.

Before switching frequencies by changing the N value, the clock monitor must be disabled. This is because when N is changed, the frequency of the low-frequency base clock (IBASE) will change proportionally until the digital loop filter has corrected the error. Since the clock monitor uses IBASE, it could erroneously detect an inactive clock. The clock monitor cannot be re-enabled until the internal clock is stable again (ICGS is set).

NOTE: *There is no hardware mechanism to prevent changing bus frequency dynamically. Be careful when changing bus frequency and consider the impact on the system.*

This flow is an example of how to change the clock frequency:

1. Verify there is no clock monitor interrupt by reading the CMF bit.
2. Turn off the clock monitor.
3. If desired, switch to the external clock (see **6.4.1 Switching Clock Sources**).
4. Change the value of N.
5. Switch back to internal (see **6.4.1 Switching Clock Sources**), if desired.
6. Turn on the clock monitor (see **6.4.2 Enabling the Clock Monitor**), if desired.

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6.4.6 Nominal Frequency Settling Time

Because the clock period of the internal clock (ICLK) is dependent on the digital loop filter outputs (DDIV and DSTG) which cannot change instantaneously, ICLK will temporarily operate at an incorrect clock period when any of the operating condition changes. This happens whenever the part is reset, the ICG multiply factor (N) is changed, the ICG trim factor (TRIM) is changed, or the internal clock is enabled after inactivity (STOP or disabled operation). The time that the ICLK takes to adjust to the correct period is known as the settling time.

Settling time depends primarily on how many corrections it takes to change the clock period, and the period of each correction. Since the corrections require four periods of the low-frequency base clock ($4*t_{IBASE}$), and since ICLK is N (the ICG multiply factor for the desired frequency) times faster than IBASE, each correction takes $4*N*t_{ICLK}$. The period of ICLK, however, will vary as the corrections occur.

6.4.6.1 Settling to Within 15 Percent

When the error is greater than 15 percent, the filter takes eight corrections to double or halve the clock period. Due to how the DCO increases or decreases the clock period, the total period of these eight corrections is approximately 11 times the period of the fastest correction. (If the corrections were perfectly linear, the total period would be 11.5 times the minimum period; however, the ring must be slightly non-linear.) Therefore, the total time it takes to double or halve the clock period is $44*N*t_{ICLKFAST}$.

If the clock period needs more than doubled or halved, the same relationship applies, only for each time the clock period needs doubled, the total number of cycles doubles.

That is, when transitioning from fast to slow:

- Going from the initial speed to half speed takes $44*N*t_{ICLKFAST}$
- From half speed to quarter speed takes $88*N*t_{ICLKFAST}$
- Going from quarter speed to eighth speed takes $176*N*t_{ICLKFAST}$, and so on.

This series can be expressed as $(2^X–1)*44*N*t_{ICLKFAST}$, where x is the number of times the speed needs doubled or halved. Since 2^X happens to be equal to $t_{ICLKSLOW}/t_{ICLKFAST}$, the equation reduces to $44*N*(t_{ICLKSLOW}-t_{ICLKFAST})$. Note that increasing speed takes much longer than decreasing speed since N is higher. This can be expressed in terms of the initial clock period (t_1) minus the final clock period (t_2) as such:

$$t_{15} = abs[44N(t_1 - t_2)]$$

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6.4.6.2 Settling to Within 5 Percent

Once the clock period is within 15 percent of the desired clock period, the filter starts making smaller adjustments. When between 15 percent and 5 percent error, each correction will adjust the clock period between 1.61 percent and 2.94 percent. In this mode, a maximum of eight corrections will be required to get to less than 5 percent error. Since the clock period is relatively close to desired, each correction takes approximately the same period of time, or $4*t_{IBASE}$. At this point, the internal clock stable bit (ICGS) will be set and the clock frequency is usable, although the error will be as high as 5 percent. The total time to this point is:

$$t_5 = abs[44N(t_1 - t_2)] + 32t_{IBASE}$$

6.4.6.3 Total Settling Time

Once the clock period is within 5 percent of the desired clock period, the filter starts making minimum adjustments. In this mode, each correction will adjust the frequency between 0.202 percent and 0.368 percent. A maximum of 24 corrections will be required to get to the minimum error. Each correction takes approximately the same period of time or $4*t_{IBASE}$. Added to the corrections for 15 percent to 5 percent, this makes 32 corrections ($128*t_{IBASE}$) to get from 15 percent to the minimum error. The total time to the minimum error is:

$$t_{tot} = abs[44N(t_1 - t_2)] + 128t_{IBASE}$$

The equations for t_{15}, t_5, and t_{tot} are dependent on the actual initial and final clock periods t_1 and t_2, not the nominal. This means the variability in the ICLK frequency due to process, temperature, and voltage must be considered. Additionally, other process factors and noise can affect the actual tolerances of the points at which the filter changes modes. This means a worst case adjustment of up to 35 percent (ICLK clock period tolerance plus 10 percent) must be added. This adjustment can be reduced with trimming. **Table 6-4** shows some typical values for settling time.

Table 6-4. Typical Settling Time Examples

t_1	t_2	N	t_{15}	t_5	t_{tot}
1/ (6.45 MHz)	1/ (25.8 MHz)	84	430 µs	535 µs	850 µs
1/ (25.8 MHz)	1/ (6.45 MHz)	21	107 µs	212 µs	525 µs
1/ (25.8 MHz)	1/ (307.2 kHz)	1	141 µs	246 µs	560 µs
1/ (307.2 kHz)	1/ (25.8 MHz)	84	11.9 ms	12.0 ms	12.3 ms

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6.4.7 Improving Settling Time

The settling time of the internal clock generator can be vastly improved if an external clock source can be used during the settling time. When the internal clock generator is disabled (ICGON is low), the DDIV[3:0] and DSTG[7:0] bits can be written. Then, when the internal clock generator is re-enabled, the clock period will automatically start at the point written in the DDIV and DSTG bits.

Since a change in the DDIV and DSTG bits only cause a change in the clock period relative to the starting point, the starting point must first be captured. The initial clock period can be expressed as in the next example, where t_X is a process, temperature, and voltage dependent constant and DDIV1 and DSTG1 are the values of DDIV and DSTG when operating at t_1.

$$t_1 = t_X \cdot 2^{DDIV1} \cdot DSTG1$$

Finding the new values for DDIV and DSTG is easy if the new clock period is a binary multiple or fraction of the original. In this case, DSTG is unchanged and DDIV2 is DDIV1 + $\log_2(t_2/t_1)$.

If the new clock period is not a binary multiple or fraction of the original, both DSTG and DDIV may need to change according to these equations:

$$DVFACT = \text{int}\left[\frac{\log(t_2/t_1)}{\log(2)}\right]$$

$$DDIV2 = DDIV1 + DVFACT$$

$$DSFACT = \left[\frac{(t_2/t_1)}{2^{(DDIV2 - DDIV1)}}\right]$$

$$DSTG2 = DSFACT \cdot DSTG1$$

If DSTG2 is greater than 255:

$$DDIV2 = DDIV2 + 1 \qquad DSTG2 = \frac{DSTG2}{2}$$

The software required to do this is relatively simple, since most of the math can be done before coding because the initial and final clock periods are known. An example of how to code this in assembly code is shown in **Figure 6-9**. This example is for illustrative purposes only and does not represent a valid syntax for any particular assembler.

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```
                        ;DDIV and DSTG modification code example
                        ;Changes DDIV and DSTG according to the initial and
                        ; desired clock period values
                        ;Requires ICGON to be clear (disabled)
                        ;User must previously calculate DVFACT and STFACT by
                        ; the equations listed in the specification
                        ;Modifies X and A registers

start   lda     icgcr   ;Verify ICGON clear (this will require
        cmp     #13     ; CMIE,CMF,CMON,ICGON,ICGS clear and CS,ECGON,ECGS set)
        lda     #dvfact ;Add the DDIV factor (calculated before
        add     icgdvr  ; coding by the DDIV2 equation)
        sta     icgdvr
        lda     #stfact ;Load the DSTG factor (calculated before coding and
                        ; multiplied by 128 to make it 0-255 for maximum precision
        ldx     icgdsr  ;Load current stage register contents
        mul             ;Multiply factor times current value
        rola            ;Since factor was multiplied by 128,
        rolx            ; result is x6-x0:a7, so put it all in X
        bcc     store   ;If result is >255, rolx will set carry
        rorx            ; so divide result by two and
        inc             ; add one to DDIV
store   stx     icgdsr  ;Store value
        lda     icgdvr  ;Test to see if DDIV too high or low
        cmp     #09     ;Valid range 0-9; too low is FF/FE; too high is 0A/0B
        bhi     exit    ;If DDIV is 0-9, you're almost done
        lda     #09     ;Otherwise, maximize period and execute error code
        sta     icgdvr
        jmp     error
exit    jmp     enable  ;Jump to code which turns on desired
                        ;clock, clock monitor, interrupts, etc.
```

Figure 6-9. Code Example for Writing DDIV and DSTG

6.4.8 Trimming Frequency on the Internal Clock Generator

The unadjusted frequency of the low-frequency base clock (IBASE), when the comparators in the frequency comparator indicate zero error, will vary as much as ±25 percent due to process, temperature, and voltage dependencies. These dependencies are in the voltage and current references, the offset of the comparators, and the internal capacitor. The voltage and temperature dependencies have been designed to be a maximum of approximately ±1 percent error. The process dependencies account for the rest.

Fortunately, for an individual part, the process dependencies are constant. An individual part can operate at approximately ±2 percent variance from its unadjusted operating point over the entire specification range of the application. If the unadjusted operating point can be changed, the entire variance can be limited to ±2 percent.

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The method of changing the unadjusted operating point is by changing the size of the capacitor. This capacitor is designed with 639 equally sized units, 384 of which are always connected. The remaining 255 units are put in by adjusting the ICG trim factor (TRIM). The default value for TRIM is $80, or 128 units, making the default capacitor size 512. Each unit added or removed will adjust the output frequency by about ±0.195 percent of the unadjusted frequency (adding to TRIM will decrease frequency). Therefore, the frequency of IBASE can be changed to ±25 percent of its unadjusted value, which is enough to cancel the process variability mentioned before.

The best way to trim the internal clock is to use the timer to measure the width of an input pulse on an input capture pin (this pulse must be supplied by the application and should be as long or wide as possible). Considering the prescale value of the timer and the theoretical (zero error) frequency of the bus (307.2 kHz *N/4), the error can be calculated. This error, expressed as a percentage, can be divided by 0.195 percent and the resultant factor added or subtracted from TRIM. This process should be repeated to eliminate any residual error.

NOTE: *It is recommended that the user preserve a copy of the contents of the ICG trim register (ICGTR) in non-volitale memory.*

Address $7FEF is reserved for an optional factory-determined value. Consult with a local Motorola representative for more information and availability of this option.

6.5 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power-consumption standby modes.

6.5.1 Wait Mode

The ICG remains active in wait mode. If enabled, the ICG interrupt to the CPU can bring the MCU out of wait mode.

In some applications, low-power consumption is desired in wait mode and a high-frequency clock is not needed. In these applications, reduce power consumption by either selecting a low-frequency external clock and turning the internal clock generator off, or reducing the bus frequency by minimizing the ICG multiplier factor (N) before executing the WAIT instruction.

6.5.2 Stop Mode

The ICG is disabled in stop mode. Upon execution of the STOP instruction, all ICG activity will cease and the output clocks (CGMXCLK and CGMOUT) will be held low. Power consumption will be minimal.

The STOP instruction does not affect the values in the ICG registers. Normal execution will resume after the MCU exits stop mode.

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6.6 Configuration Register Option

One configuration register option affects the functionality of the ICG: EXTSLOW (slow external clock).

All configuration register options will have a default setting. Refer to **Section 3. Configuration Register (CONFIG)** on how the configuration register is used.

6.6.1 EXTSLOW

Slow external clock (EXTSLOW), when set, will decrease the drive strength of the oscillator amplifier, enabling low-frequency crystal operation (30 kHz–100 kHz). When clear, EXTSLOW enables high frequency crystal operation (1 MHz to 8 MHz).

EXTSLOW, when set, also configures the clock monitor to expect an external clock source that is slower than the low-frequency base clock (60 Hz–307.2 kHz). When EXTSLOW is clear, the clock monitor will expect an external clock faster than the low-frequency base clock (307.2 kHz–32 MHz).

The default state for this option is clear.

6.7 I/O Registers

The ICG contains five registers, summarized in **Figure 6-10**. These registers are:

- ICG control register, ICGCR
- ICG multiplier register, ICGMR
- ICG trim register, ICGTR
- ICG DCO divider control register, ICGDVR
- ICG DCO stage control register, ICGDSR

Several of the bits in these registers have interaction where the state of one bit may force another bit to a particular state or prevent another bit from being set or cleared. A summary of this interaction is shown in **Table 6-5**.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0036	Internal Clock Generator Control Register (ICGCR) See page 88.	Read:	CMIE	CMF	CMON	CS	ICGON	ICGS	ECGON	ECGS
		Write:								
		Reset:	0	0	0	0	1	0	0	0
$0037	Internal Clock Generator Multiplier Register (ICGMR) See page 90.	Read:	R	N6	N5	N4	N3	N2	N1	N0
		Write:								
		Reset:	0	0	0	1	0	1	0	1

Figure 6-10. ICG I/O Register Summary

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Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0038	Internal Clock Generator Trim Register (ICGTR) See page 90.	Read: Write:	TRIM7	TRIM6	TRIM5	TRIM4	TRIM3	TRIM2	TRIM1	TRIM0
		Reset:	1	0	0	0	0	0	0	0
$0039	ICG DCO Divider Control Register (ICGDVR) See page 91.	Read: Write:	R	R	R	R	DDIV3	DDIV2	DDIV1	DDIV0
		Reset:	0	0	0	0	U	U	U	U
$003A	ICG DCO Stage Register (ICGDSR) See page 91.	Read: Write:	DSTG7	DSTG6	DSTG5	DSTG4	DSTG3	DSTG2	DSTG1	DSTG0
		Reset:	Unaffected by reset							

= Unimplemented R = Reserved U = Unaffected

Figure 6-10. ICG I/O Register Summary (Continued)

Table 6-5. ICG Module Register Bit Interaction Summary

Condition	Register Big Results for Given Condition											
	CMIE	CMF	CMON	CS	ICGON	ICGS	ECGON	ECGS	N[6:0]	TRIM[7:0]	DDIV[3:0]	DSTG[7:0]
Reset	0	0	0	0	1	0	0	0	$15	$80	—	—
CMF = 1	—	(1)	1	—	1	—	1	—	uw	uw	uw	uw
CMON = 0	0	0	(0)	—	—	—	—	—	—	—	—	—
CMON = 1	—	—	(1)	—	1	—	1	—	uw	uw	uw	uw
CS = 0	—	—	—	(0)	1	—	—	—	—	—	uw	uw
CS = 1	—	—	—	(1)	—	—	1	—	—	—	—	—
ICGON = 0	0	0	0	1	(0)	0	1	—	—	—	—	—
ICGON = 1	—	—	—	—	(1)	—	—	—	—	—	uw	uw
ICGS = 0	us	—	us	uc	—	(0)	—	—	—	—	—	—
ECGON = 0	0	0	0	0	1	—	(0)	0	—	—	uw	uw
ECGS = 0	us	—	us	us	—	—	—	(0)	—	—	—	—
IOFF = 1	—	1*	(1)	1	(1)	0	(1)	—	uw	uw	uw	uw
EOFF = 1	—	1*	(1)	0	(1)	—	(1)	0	uw	uw	uw	uw
N = written	(0)	(0)	(0)	—	—	0*	—	—	—	—	—	—
TRIM = written	(0)	(0)	(0)	—	—	0*	—	—	—	—	—	—

— Register bit is unaffected by the given condition.

0, 1 Register bit is forced clear or set, respectively, in the given condition.

0*, 1* Register bit is temporarily forced clear or set, respectively, in the given condition.

(0), (1) Register bit must be clear or set, respectively, for the given condition to occur.

us, uc, uw Register bit cannot be set, cleared, or written, respectively, in the given condition.

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6.7.1 ICG Control Register

The ICG control register (ICGCR) contains the control and status bits for the internal clock generator, external clock generator, and clock monitor as well as the clock select and interrupt enable bits.

Address: $0036

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	CMIE	CMF	CMON	CS	ICGON	ICGS	ECGON	ECGS
Write:								
Reset:	0	0	0	0	1	0	0	0

= Unimplemented

Figure 6-11. ICG Control Register (ICGCR)

CMIE — Clock Monitor Interrupt Enable Bit

This read/write bit enables clock monitor interrupts. An interrupt will occur when both CMIE and CMF are set. CMIE can be set when the CMON bit has been set for at least one cycle. CMIE is forced clear when CMON is clear or during reset.

1 = Clock monitor interrupts enabled
0 = Clock monitor interrupts disabled

CMF — Clock Monitor Interrupt Flag

This read-only bit is set when the clock monitor determines that either ICLK or ECLK becomes inactive and the CMON bit is set. This bit is cleared by first reading the bit while it is set, followed by writing the bit low. This bit is forced clear when CMON is clear or during reset.

1 = Either ICLK or ECLK has become inactive.
0 = ICLK and ECLK have not become inactive since the last read of the ICGCR or the clock monitor is disabled.

CMON — Clock Monitor On Bit

This read/write bit enables the clock monitor. CMON can be set when both ICLK and ECLK have been on and stable for at least one bus cycle (ICGON, ECGON, ICGS, and ECGS are all set). CMON is forced set when CMF is set, to avoid inadvertent clearing of CMF. CMON is forced clear when either ICGON or ECGON is clear or during reset.

1 = Clock monitor output enabled
0 = Clock monitor output disabled

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CS — Clock Select Bit

This read/write bit determines which clock will generate the oscillator output clock (CGMXCLK). This bit can be set when ECGON and ECGS have been set for at least one bus cycle and can be cleared when ICGON and ICGS have been set for at least one bus cycle. This bit is forced set when the clock monitor determines the internal clock (ICLK) is inactive or when ICGON is clear. This bit is forced clear when the clock monitor determines that the external clock (ECLK) is inactive, when ECGON is clear, or during reset.

1 = External clock (ECLK) sources CGMXCLK
0 = Internal clock (ICLK) sources CGMXCLK

ICGON — Internal Clock Generator On Bit

This read/write bit enables the internal clock generator. ICGON can be cleared when the CS bit has been set and the CMON bit has been clear for at least one bus cycle. ICGON is forced set when the CMON bit is set, the CS bit is clear, or during reset.

1 = Internal clock generator enabled
0 = Internal clock generator disabled

ICGS — Internal Clock Generator Stable Bit

This read-only bit indicates when the internal clock generator has determined that the internal clock (ICLK) is within about 5 percent of the desired value. This bit is forced clear when the clock monitor determines the ICLK is inactive, when ICGON is clear, when the ICG multiplier factor is written, or during reset.

1 = Internal clock is within 5 percent of the desired value.
0 = Internal clock may not be within 5 percent of the desired value.

ECGON — External Clock Generator On Bit

This read/write bit enables the external clock generator. ECGON can be cleared when the CS and CMON bits have been clear for at least one bus cycle. ECGON is forced set when the CMON bit or the CS bit is set. ECGON is forced clear during reset.

1 = External clock generator enabled
0 = External clock generator disabled

ECGS — External Clock Generator Stable Bit

This read-only bit indicates when at least 4096 external clock (ECLK) cycles have elapsed since the external clock generator was enabled. This is not an assurance of the stability of ECLK but is meant to provide a startup delay. This bit is forced clear when the clock monitor determines ECLK is inactive, when ECGON is clear, or during reset.

1 = 4096 ECLK cycles have elapsed since ECGON was set.
0 = External cock is unstable, inactive, or disabled.

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6.7.2 ICG Multiplier Register

Address: $0037

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	R	N6	N5	N4	N3	N2	N1	N0
Reset:	0	0	0	1	0	1	0	1

R = Reserved

Figure 6-12. ICG Multiplier Register (ICGMR)

N6–N0 — ICG Multiplier Factor Bits

These read/write bits change the multiplier used by the internal clock generator. The internal clock (ICLK) will be (307.2 kHz ±25 percent) * N. A value of $00 in this register is interpreted the same as a value of $01. This register cannot be written when the CMON bit is set. Reset sets this factor to $15 (decimal 21) for default frequency of 6.45 MHz ±25 percent (1.613 MHz ±25 percent bus).

6.7.3 ICG Trim Register

Address: $0038

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TRIM7	TRIM6	TRIM5	TRIM4	TRIM3	TRIM2	TRIM1	TRIM0
Reset:	1	0	0	0	0	0	0	0

Figure 6-13. ICG Trim Register (ICGTR)

TRIM7–TRIM0 — ICG Trim Factor Bits

These read/write bits change the size of the internal capacitor used by the internal clock generator. By testing the frequency of the internal clock and incrementing or decrementing this factor accordingly, the accuracy of the internal clock can be improved to ±2 percent. Incrementing this register by 1 decreases the frequency by 0.195 percent of the unadjusted value. Decrementing this register by one increases the frequency by 0.195 percent. This register cannot be written when the CMON bit is set. Reset sets these bits to $80, centering the range of possible adjustment.

NOTE: *It is recommended that the user preserve a copy of the contents of the ICG trim register (ICGTR) in non-volitale memory.*

Address $7FEF is reserved for an optional factory-determined ICG trim value. Consult with a local Motorola representative for more information and availability of this option.

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6.7.4 ICG DCO Divider Register

Address: $0039

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	R	R	R	R	DDIV3	DDIV2	DDIV1	DDIV0
Reset:	0	0	0	0	U	U	U	U

R = Reserved U = Unaffected

Figure 6-14. ICG DCO Divider Register (ICGDVR)

DDIV3–DDIV0 — ICG DCO Divider Control Bits

These bits indicate the number of divide-by-twos (DDIV) that follow the digitally controlled oscillator. Incrementing DDIV will add another divide-by-two, doubling the period (halving the frequency). Decrementing has the opposite effect. DDIV cannot be written when ICGON is set to prevent inadvertent frequency shifting. When ICGON is set, DDIV is controlled by the digital loop filter. The range of valid values for DDIV is from $0 to $9. Values of $A–$F are interpreted the same as $9. Since the DCO is active during reset, reset has no effect on DSTG and the value may vary.

6.7.5 ICG DCO Stage Register

Address: $003A

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DSTG7	DSTG6	DSTG5	DSTG4	DSTG3	DSTG2	DSTG1	DSTG0
Reset:	Unaffected by reset							

Figure 6-15. ICG DCO Stage Register (ICGDSR)

DSTG7–DSTG0 — ICG DCO Stage Control Bits

These bits indicate the number of stages DSTG (above the minimum) in the digitally controlled oscillator. The total number of stages is approximately equal to $1FF, so changing DSTG from $00 to $FF will approximately double the period. Incrementing DSTG will increase the period (decrease the frequency) by 0.202 percent to 0.368 percent (decrementing has the opposite effect). DSTG cannot be written when ICGON is set to prevent inadvertent frequency shifting. When ICGON is set, DSTG is controlled by the digital loop filter. Since the DCO is active during reset, reset has no effect on DSTG and the value may vary.

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Section 7. Keyboard/External Interrupt Module (KBI)

7.1 Introduction

This section describes the maskable external interrupt ($\overline{IRQ}$) input and six independently maskable keyboard wakeup interrupt pins.

7.2 Features

Features of the KBI include:

- Dedicated external interrupt pin ($\overline{IRQ}$)
- Six keyboard interrupt pins with separate keyboard interrupt enable bits and one keyboard interrupt mask
- Internal pullup resistor
- Hysteresis buffer
- Programmable edge-only or edge- and level-interrupt sensitivity
- Automatic interrupt acknowledge

7.3 Functional Description

This section provides a functional description of the keyboard/external interrupt module (KBI).

7.3.1 External Interrupt

A logic 0 applied to the external interrupt pin ($\overline{IRQ}$) can latch a CPU interrupt request. **Figure 7-2** shows the structure of the external ($\overline{IRQ}$) interrupt of the KBI module.

A logic 0 applied to one or more of the keyboard interrupt pins can latch a CPU interrupt request. **Figure 7-5** shows the structure of the keyboard interrupts of the KBI module

See **Figure 7-3** for a summary of the interrupt and keyboard input/output (I/O) registers.

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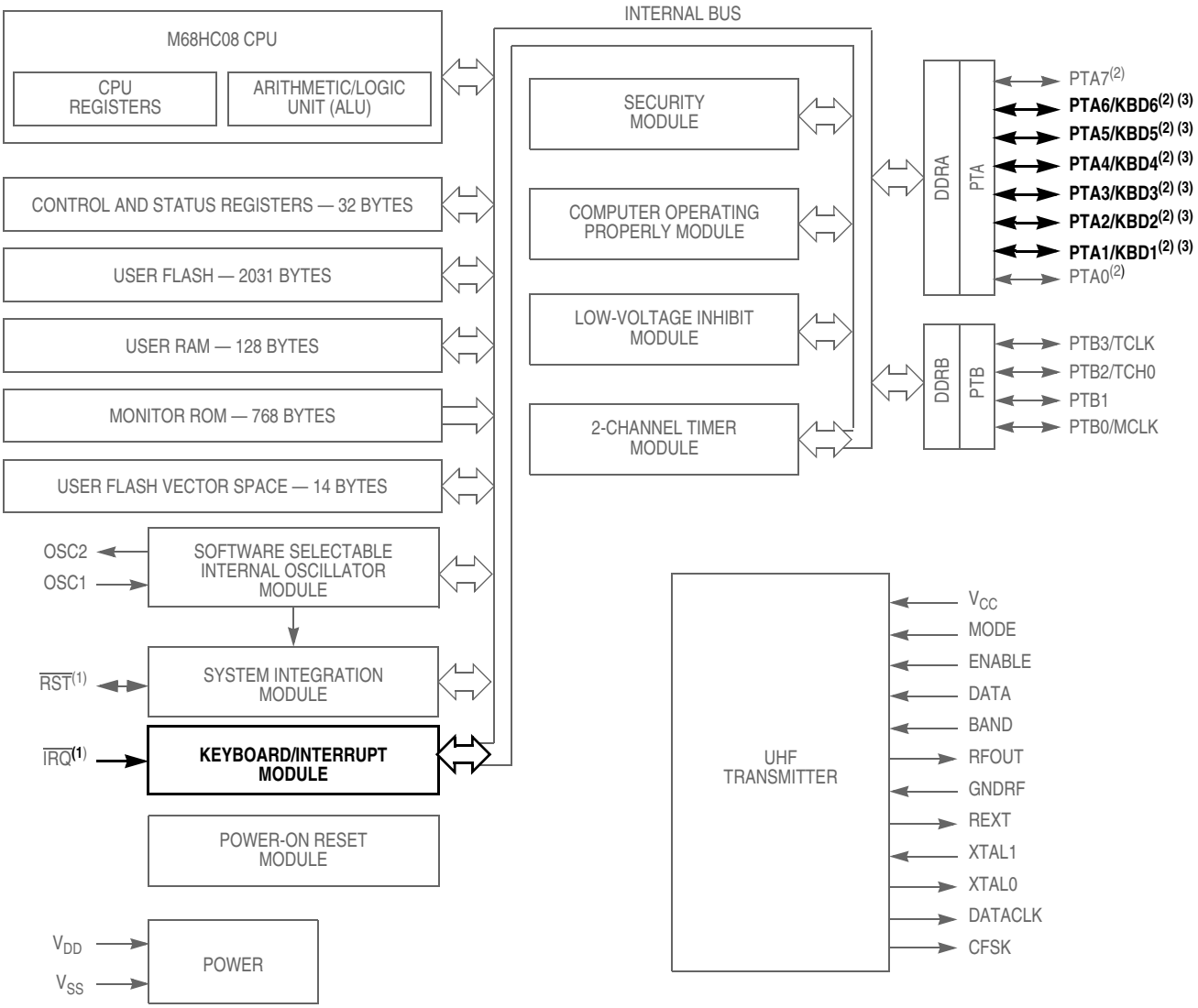

1. Pin contains integrated pullup resistor
2. High current sink pin
3. Pin contains software selectable pullup resistor

Figure 7-1. Block Diagram Highlighting KBI Block and Pins

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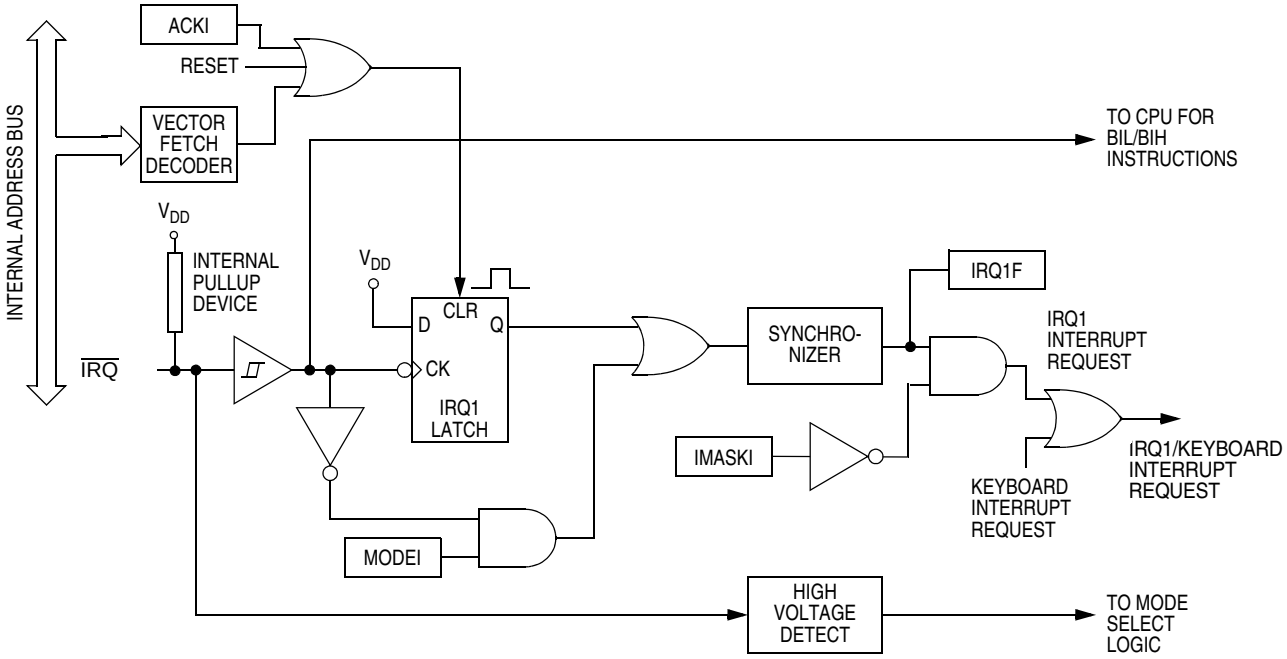

Figure 7-2. IRQ Block Diagram

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$001A	IRQ and Keyboard Status and Control Register (INTKBSCR) See page 101.	Read:	IRQ1F	0	IMASKI	MODEI	KEYF	0	IMASKK	MODEK
		Write:	R	ACKI			R	ACKK		
		Reset:	0	0	0	0	0	0	0	0
$001B	Keyboard Interrupt Enable Register (INTKBIER) See page 102.	Read:	0	KBIE6	KBIE5	KBIE4	KBIE3	KBIE2	KBIE1	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented R = Reserved

Figure 7-3. IRQ and Keyboard I/O Register Summary

Interrupt signals on the $\overline{\text{IRQ}}$ pin are latched into the IRQ1 latch. Keyboard interrupts are latched in the keyboard interrupt latch. An interrupt latch remains set until one of these actions occurs:

- Vector fetch — A vector fetch automatically generates an interrupt acknowledge signal that clears IRQ1 latch and keyboard interrupt latch.
- Software clear — Software can clear an interrupt latch by writing to the appropriate acknowledge bit in the interrupt status and control register (INTKBSCR). Writing a 1 to the ACKI bit clears the IRQ1 latch. Writing a 1 to the ACKK bit clears the keyboard interrupt latch.
- Reset — A reset automatically clears both interrupt latches.

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The $\overline{IRQ1}$ pin and keyboard interrupt pins are falling-edge triggered and are software-configurable to be both falling-edge and low-level triggered. The MODEI and MODEK bits in the INTKBSCR controls the triggering sensitivity of the $\overline{IRQ}$ pin and keyboard interrupt pins.

When an interrupt pin is edge-triggered only, the interrupt latch remains set until a vector fetch, software clear, or reset occurs.

When an interrupt pin is both falling-edge and low-level-triggered, the interrupt latch remains set until both of these occur:

- Vector fetch or software clear
- Return of the interrupt pin to logic 1

The vector fetch or software clear may occur before or after the interrupt pin returns to logic 1. As long as the pin is low, the interrupt request remains pending. A reset will clear the latch, the MODEI and MODEK control bits, thereby clearing the interrupt even if the pin stays low.

When set, the IMASKI and IMASKK bits in the INTKBSCR mask all external interrupt requests. A latched interrupt request is not presented to the interrupt priority logic unless the corresponding IMASK<x> bit is clear.

NOTE: *The interrupt mask (I) in the condition code register (CCR) masks all interrupt requests, including external interrupt requests. See* ***Figure 7-4****.*

7.3.2 $\overline{IRQ}$ Pin

A logic 0 on the $\overline{IRQ}$ pin can latch an interrupt request into the IRQ1 latch. A vector fetch, software clear, or reset clears the IRQ1 latch. If the MODEI bit is set, the $\overline{IRQ}$ pin is both falling-edge sensitive and low-level sensitive. With MODEI set, both of these actions must occur to clear the IRQ1 latch:

- Vector fetch or software clear — A vector fetch generates an interrupt acknowledge signal to clear the latch. Software may generate the interrupt acknowledge signal by writing a 1 to the ACKI bit in the IRQ and keyboard status and control register (INTKBSCR). The ACKI bit is useful in applications that poll the $\overline{IRQ}$ pin and require software to clear the IRQ1 latch. Writing to the ACKI bit can also prevent spurious interrupts due to noise. Setting ACKI does not affect subsequent transitions on the $\overline{IRQ}$ pin. A falling edge on $\overline{IRQ}$ that occurs after writing to the ACKI bit latches another interrupt request. If the IRQ1 mask bit, IMASKI, is clear, the CPU loads the program counter with the vector address at locations $FFFA and $FFFB.
- Return of the $\overline{IRQ}$ pin to logic 1 — As long as the $\overline{IRQ}$ pin is at logic 0, the IRQ1 latch remains set.

The vector fetch or software clear and the return of the $\overline{IRQ}$ pin to logic 1 can occur in any order. The interrupt request remains pending as long as the $\overline{IRQ}$ pin is at logic 0. A reset will clear the latch and the MODEI control bit, thereby clearing the interrupt even if the pin stays low.

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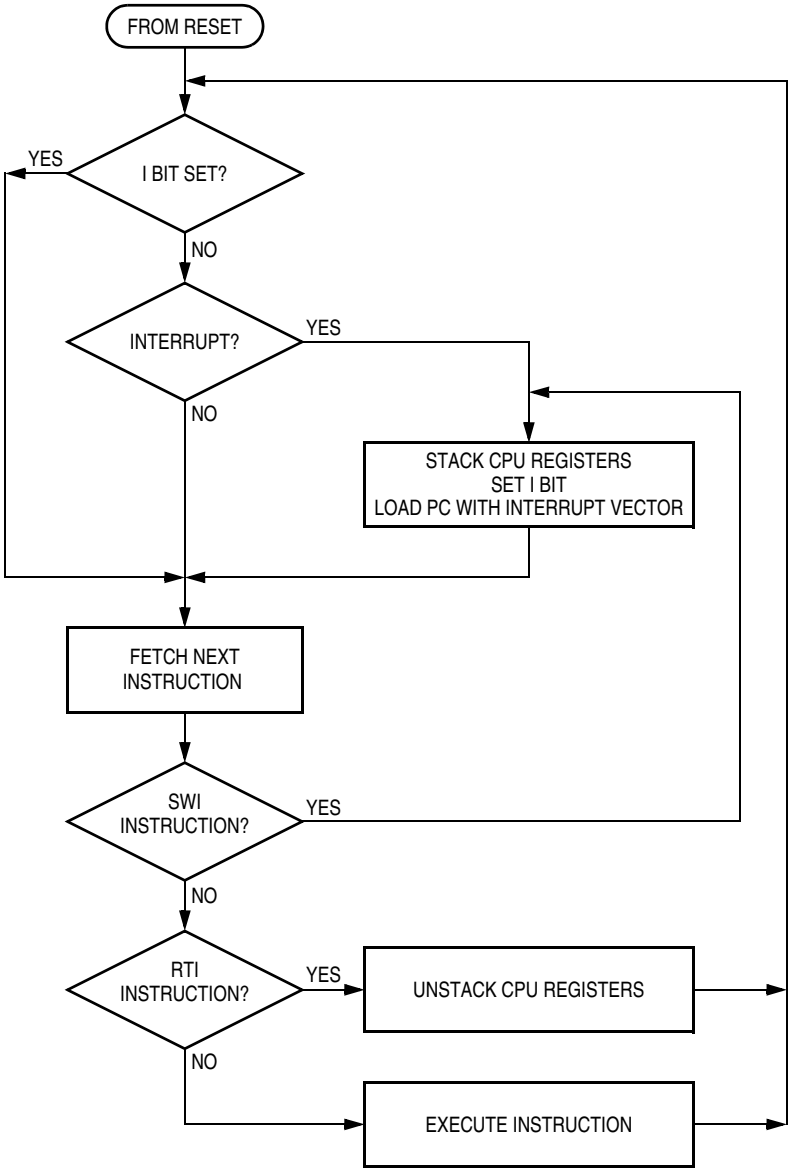

Figure 7-4. IRQ Interrupt Flowchart

If the MODEI bit is clear, the $\overline{IRQ}$ pin is falling-edge sensitive only. With MODEI clear, a vector fetch or software clear immediately clears the IRQ1 latch.The IRQ1F bit in the INTKBSCR register can be used to check for pending interrupts. The IRQ1F bit is not affected by the IMASKI bit, which makes it useful in applications where polling is preferred.

Use the BIH or BIL instruction to read the logic level on the $\overline{IRQ}$ pin.

NOTE: *When using the level-sensitive interrupt trigger, avoid false interrupts by masking interrupt requests in the interrupt routine.*

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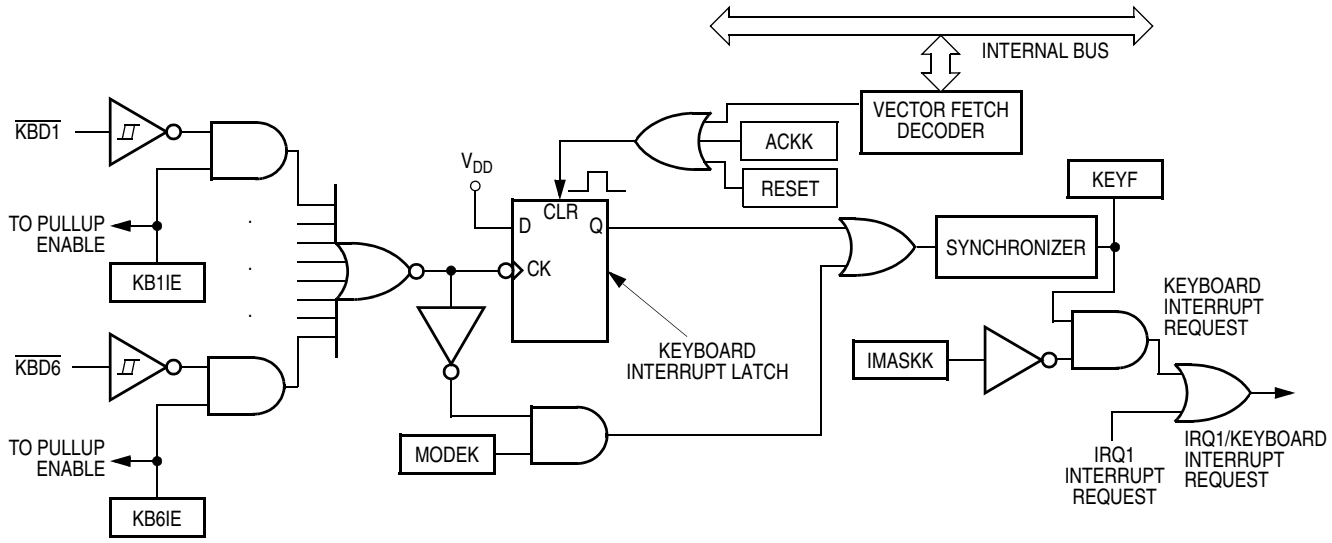

Figure 7-5. Keyboard Interrupt Block Diagram

7.3.3 KBI Module During Break Interrupts

The system integration module (SIM) controls whether the IRQ1 or keyboard interrupt latches can be cleared during the break state. The BCFE bit in the break flag control register (BFCR) enables software to clear the latches during the break state. (See **10.7.3 SIM Break Flag Control Register**.)

To allow software to clear the IRQ1 or keyboard latches during a break interrupt, write a 1 to the BCFE bit. If a latch is cleared during the break state, it remains cleared when the MCU exits the break state.

To protect the latch during the break state, write a 0 to the BCFE bit. With BCFE at 0 (its default state), writing to the ACKI or ACKK bits in the IRQ and keyboard status and control register during the break state has no effect on the IRQ1 or keyboard latches.

7.3.4 Keyboard Interrupt Pins

Writing to the KBIE6–KBIE1 bits in the keyboard interrupt enable register independently enables or disables each port A pin as a keyboard interrupt pin. Enabling a keyboard interrupt pin also enables its internal pullup device. A logic 0 applied to an enabled keyboard interrupt pin latches an IRQ1/keyboard interrupt request.

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An IRQ1/keyboard interrupt is latched when one or more keyboard pins goes low after all were high. The MODEK bit in the keyboard status and control register controls the triggering mode of the keyboard interrupt.

- If the keyboard interrupt is edge-sensitive only, a falling edge on a keyboard pin does not latch an interrupt request if another keyboard pin is already low. To prevent losing an interrupt request on one pin because another pin is still low, software can disable the latter pin while it is low.
- If the keyboard interrupt is falling edge- and low level-sensitive, an interrupt request is present as long as any keyboard pin is low.

If the MODEK bit is set, the keyboard interrupt pins are both falling edge- and low level-sensitive, and both of these actions must occur to clear a keyboard interrupt request:

- Vector fetch or software clear — A vector fetch generates an interrupt acknowledge signal to clear the interrupt request. Software may generate the interrupt acknowledge signal by writing a 1 to the ACKK bit in the keyboard status and control register (INTKBSCR). The ACKK bit is useful in applications that poll the keyboard interrupt pins and require software to clear the keyboard interrupt request. Writing to the ACKK bit prior to leaving an interrupt service routine also can prevent spurious interrupts due to noise. Setting ACKK does not affect subsequent transitions on the keyboard interrupt pins. A falling edge that occurs after writing to the ACKK bit latches another interrupt request. If the keyboard interrupt mask bit, IMASKK, is clear, the CPU loads the program counter with the vector address at locations $FFFA and $FFFB.
- Return of all enabled keyboard interrupt pins to logic 1. As long as any enabled keyboard interrupt pin is at logic 0, the keyboard interrupt remains set.

The vector fetch or software clear and the return of all enabled keyboard interrupt pins to logic 1 may occur in any order.

If the MODEK bit is clear, the keyboard interrupt pin is falling edge-sensitive only. With MODEK clear, a vector fetch or software clear immediately clears the keyboard interrupt request.

Reset clears the keyboard interrupt request and the MODEK bit, clearing the interrupt request even if a keyboard interrupt pin stays at logic 0.

The keyboard flag bit (KEYF) in the IRQ and keyboard status and control register can be used to see if a pending interrupt exists. The KEYF bit is not affected by the keyboard interrupt mask bit (IMASKK) which makes it useful in applications where polling is preferred.

To determine the logic level on a keyboard interrupt pin, use the data direction register to configure the pin as an input and read the data register.

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NOTE: *Setting a keyboard interrupt enable bit (KBIE<x>) forces the corresponding keyboard interrupt pin to be an input, overriding the data direction register. However, the data direction register bit must be a 0 for software to read the pin.*

7.3.5 Keyboard Initialization

When a keyboard interrupt pin is enabled, it takes time for the internal pullup to reach a logic 1. Therefore, a false interrupt can occur as soon as the pin is enabled.

To prevent a false interrupt on keyboard initialization:

1. Mask keyboard interrupts by setting the IMASKK bit in the keyboard status and control register.
2. Enable the KBI pins by setting the appropriate KBIEx bits in the keyboard interrupt enable register.
3. Write to the ACKK bit in the keyboard status and control register to clear any false interrupts.
4. Clear the IMASKK bit.

An interrupt signal on an edge-triggered pin can be acknowledged immediately after enabling the pin. An interrupt signal on an edge- and level-triggered interrupt pin must be acknowledged after a delay that depends on the external load.

Another way to avoid a false interrupt:

1. Configure the keyboard pins as outputs by setting the appropriate DDRA bits in data direction register A.
2. Write 1s to the appropriate port A data register bits.
3. Enable the KBI pins by setting the appropriate KBIEx bits in the keyboard interrupt enable register.

7.4 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power-consumption standby modes.

7.4.1 Wait Mode

The IRQ1/keyboard interrupts remain active in wait mode. Clearing the IMASKI or IMASKK bits in the IRQ and keyboard status and control register enables keyboard interrupt requests to bring the MCU out of wait mode.

7.4.2 Stop Mode

The IRQ1/keyboard interrupt remains active in stop mode. Clearing the IMASKI or IMASKK bit in the IRQ and keyboard status and control register enables keyboard interrupt requests to bring the MCU out of stop mode.

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7.5 I/O Registers

These registers control and monitor operation of the keyboard/external interrupt module:

- IRQ and keyboard status and control register, INTKBSCR
- Keyboard interrupt enable register, KBIER

7.5.1 IRQ and Keyboard Status and Control Register

The IRQ and keyboard status and control register (INTKBSCR) controls and monitors operation of the keyboard/external interrupt module. The INTKBSCR has these functions:

- Flags the keyboard interrupt requests
- Acknowledges the keyboard interrupt requests
- Masks the keyboard interrupt requests
- Shows the state of the $\overline{\text{IRQ1}}$ interrupt flag
- Clears the $\overline{\text{IRQ}}$ interrupt latch
- Masks the $\overline{\text{IRQ}}$ interrupt request
- Controls the triggering sensitivity of the keyboard and $\overline{\text{IRQ}}$ interrupt pins

Address: $001A

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	IRQ1F	0	IMASKI	MODEI	KEYF	0	IMASKK	MODEK
Write:	R	ACKI			R	ACKK		
Reset:	0	0	0	0	0	0	0	0

R = Reserved

Figure 7-6. IRQ and Keyboard Status and Control Register (INTKBSCR)

IRQ1F — $\overline{\text{IRQ}}$ Flag Bit

This read-only status bit is high when the $\overline{\text{IRQ}}$ interrupt is pending.

1 = $\overline{\text{IRQ}}$ interrupt pending
0 = $\overline{\text{IRQ}}$ interrupt not pending

ACKI — $\overline{\text{IRQ}}$ Interrupt Request Acknowledge Bit

Writing a 1 to this write-only bit clears the $\overline{\text{IRQ}}$ latch. ACKI always reads as 0. Reset clears ACKI.

IMASKI — $\overline{\text{IRQ}}$ Interrupt Mask Bit

Writing a 1 to this read/write bit disables $\overline{\text{IRQ}}$ interrupt requests. Reset clears IMASKI.

1 = $\overline{\text{IRQ}}$ interrupt requests disabled
0 = $\overline{\text{IRQ}}$ interrupt requests enabled

MODEI — $\overline{\text{IRQ}}$ Triggering Sensitivity Bit

This read/write bit controls the triggering sensitivity of the $\overline{\text{IRQ}}$ pin. Reset clears MODEI.

1 = $\overline{\text{IRQ}}$ interrupt requests on falling edges and low levels
0 = interrupt requests on falling edges only

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KEYF — Keyboard Flag Bit

This read-only bit is set when a keyboard interrupt is pending. Reset clears the KEYF bit.

1 = Keyboard interrupt pending
0 = No keyboard interrupt pending

ACKK — Keyboard Acknowledge Bit

Writing a 1 to this write-only bit clears the keyboard interrupt request. ACKK always reads as 0. Reset clears ACKK.

IMASKK — Keyboard Interrupt Mask Bit

Writing a 1 to this read/write bit prevents the output of the keyboard interrupt mask from generating interrupt requests. Reset clears the IMASKK bit.

1 = Keyboard interrupt requests masked
0 = Keyboard interrupt requests not masked

MODEK — Keyboard Triggering Sensitivity Bit

This read/write bit controls the triggering sensitivity of the keyboard interrupt pins. Reset clears MODEK.

1 = Keyboard interrupt requests on falling edges and low levels
0 = Keyboard interrupt requests on falling edges only

7.5.2 Keyboard Interrupt Enable Register

The keyboard interrupt enable register (INTKBIER) enables or disables each port A pin to operate as a keyboard interrupt pin.

Address: $001B

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	KBIE6	KBIE5	KBIE4	KBIE3	KBIE2	KBIE1	0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 7-7. Keyboard Interrupt Enable Register (INTKBIER)

KBIE6–KBIE1 — Keyboard Interrupt Enable Bits

Each of these read/write bits enables the corresponding keyboard interrupt pin to latch interrupt requests. These bits also enable the corresponding internal pullup resistor which is enabled only when the bit is set. Reset clears the keyboard interrupt enable register.

1 = PAx pin enabled as keyboard interrupt pin and corresponding internal pullup resistor enabled
0 = PAx pin not enabled as keyboard interrupt pin and corresponding internal pullup resistor disabled

NOTE: *Setting a keyboard interrupt enable bit (KBIEx) forces the corresponding keyboard interrupt pin to be an input, overriding the data direction register. However, the data direction register bit must be a 0 for software to read the pin.*

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Section 8. Low-Voltage Inhibit (LVI)

8.1 Introduction

The low-voltage inhibit (LVI) module monitors the voltage on the V_{DD} pin and will set a low voltage sense bit when V_{DD} voltage falls to the LVI sense voltage. The LVI will force a reset when the V_{DD} voltage falls to the LVI trip voltage.

8.2 Features

Features of the LVI module include:

- Two levels of low-voltage condition are detected:
  - Low-voltage detection
  - Low-voltage reset
- User-configurable for stop mode

8.3 Functional Description

Figure 8-1 shows the structure of the LVI module. The LVI module contains a bandgap reference circuit and two comparators. The LVI monitors V_{DD} voltage during normal MCU operation. When enabled, the LVI module generates a reset when V_{DD} falls below the V_{LVR} threshold.

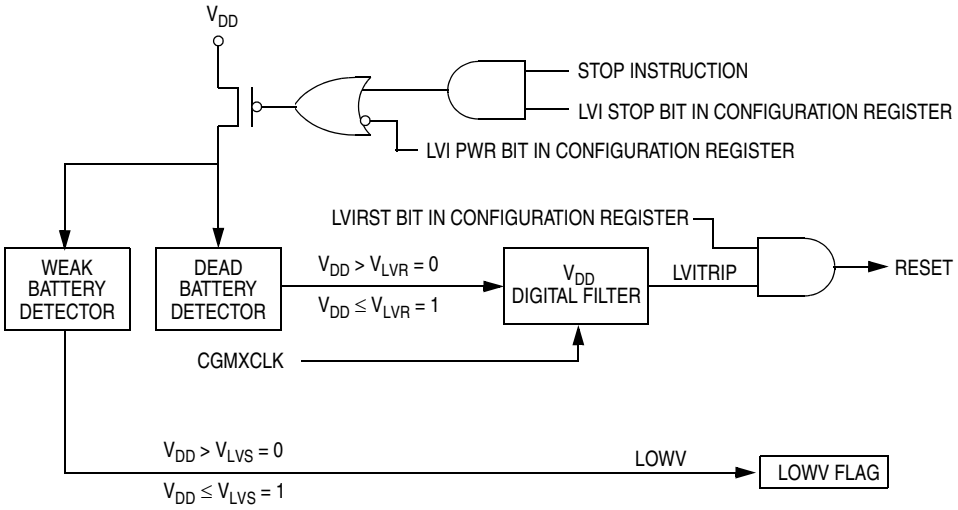

Figure 8-1. LVI Module Block Diagram

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In addition to forcing a reset condition, the LVI module has a second circuit dedicated to low-voltage detection. When V_{DD} falls below V_{LVS}, the output of the low-voltage comparator asserts the LOWV flag in the LVI status register (LVISR). In applications that require detecting low batteries, software can monitor by polling the LOWV bit.

8.3.1 False Trip Protection

The V_{DD} pin level is digitally filtered to reduce false dead battery detection due to power supply noise. For the LVI module to reset due to a low-power supply, V_{DD} must remain at or below the V_{LVR} level for a minimum 32–40 CGMXCLK cycles. See **Table 8-1**.

Table 8-1. LOWV Bit Indication

V_{DD}		Result
At Level:	**For Number of CGMXCLK Cycles:**	
$V_{DD} > V_{LVR}$	ANY	Filter counter remains clear
$V_{DD} < V_{LVR}$	< 32 CGMXCLK cycles	No reset, continue counting CGMXCLK
$V_{DD} < V_{LVR}$	Between 32 and 40 CGMXCLK cycles	LVI may generate a reset after 32 CGMXCLK cycles
$V_{DD} < V_{LVR}$	> 40 CGMXCLK cycles	LVI is guaranteed to generate a reset

8.3.2 Short Stop Recovery Option

The LVI has an enable time of t_{EN}. The system stabilization time for power-on reset and long stop recovery (both 4096 CGMXCLK cycles) gives a delay longer than the LVI enable time for these startup scenarios. There is no period where the MCU is not protected from a low-power condition. However, when using the short stop recovery configuration option, the 32 CGMXCLK delay must be greater than the LVI turn on time to avoid a period in startup where the LVI is not protecting the MCU.

NOTE: *The LVI is enabled automatically after reset or stop recovery, if the LVISTOP of the CONFIG register is set. (See **Section 3. Configuration Register (CONFIG)**.)*

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8.4 LVI Status Register

The LVI status register flags V_{DD} voltages below the V_{LVR} and V_{LVS} levels.

Address: $FE0F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	LVIOUT	0	LOWV	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 8-2. LVI Status Register (LVISR)

LVIOUT — LVI Output Bit

The read-only flag becomes set when the V_{DD} voltage falls below the V_{LVR} voltage for 32 to 40 CGMXCLK cycles. Reset clears the LVIOUT bit.

LOWV— LVI Low Indicator Bit

This read-only flag becomes set when the LVI is detecting V_{DD} voltage below the V_{LVS} threshold.

8.5 LVI Interrupts

The LVI module does not generate CPU interrupt requests.

8.6 Low-Power Modes

The STOP and WAIT instructions put the MCU in low power-consumption standby modes.

8.6.1 Wait Mode

The LVI module remains active in wait mode. The LVI module can generate a reset if a V_{DD} voltage below the V_{LVR} voltage is detected.

8.6.2 Stop Mode

The LVI can be enabled or disabled in stop mode by setting the LVISTOP bit in the CONFIG register. (See **Section 3. Configuration Register (CONFIG)**.)

NOTE: *To minimize STOP $I_{DD,}$ disable the LVI in stop mode.*

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Section 9. Input/Output (I/O) Ports

9.1 Introduction

Twelve bidirectional input/output (I/O) pins form two parallel ports in the 32-pin low-profile quad flat pack (LQFP). All I/O pins are programmable as inputs or outputs. Port A bits PTA6–PTA1 have keyboard wakeup interrupts and internal pullup resistors.

NOTE: *Connect any unused I/O pins to an appropriate logic level, either V_{DD} or V_{SS}. Although the I/O ports do not require termination for proper operation, termination reduces excess current consumption and the possibility of electrostatic damage.*

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0000	Port A Data Register (PTA) See page 108.	Read:	PTA7	PTA6	PTA5	PTA4	PTA3	PTA2	PTA1	PTA0
		Write:								
		Reset:	Unaffected by reset							
$0001	Port B Data Register (PTB) See page 110.	Read:					PTB3	PTB2	PTB1	PTB0
		Write:								
		Reset:	Unaffected by reset							
$0004	Data Direction Register A (DDRA) See page 109.	Read:	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0005	Data Direction Register B (DDRB) See page 111.	Read:	MCLKEN	0			DDRB3	DDRB2	DDRB1	DDRB0
		Write:								
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 9-1. I/O Port Register Summary

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9.2 Port A

Port A is an 8-bit special function port that shares six of its pins with the keyboard interrupt module (KBD). PTA6–PTA1 contain pullup resistors enabled when the port pin is enabled as a keyboard interrupt. Port A pins are also high-current port pins with 3-mA sink capabilities.

9.2.1 Port A Data Register

The port A data register (PTA) contains a data latch for each of the eight port A pins.

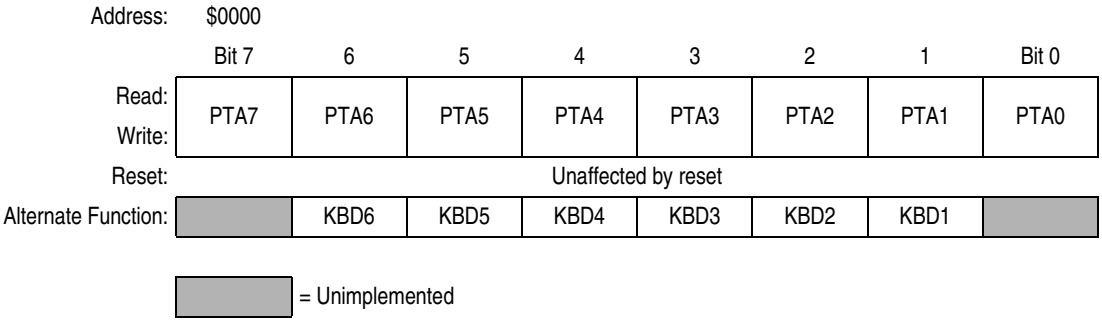

Figure 9-2. Port A Data Register (PTA)

PTA[7:0] — Port A Data Bits

These read/write bits are software programmable. Data direction of each port A pin is under the control of the corresponding bit in data direction register A. Reset has no effect on port A data.

KBD[6:1] — Keyboard Wakeup Pins

The keyboard interrupt enable bits, KBIE[6:1], in the keyboard interrupt control register enable the port A pin as external interrupt pins and related internal pullup resistor. See **Section 7. Keyboard/External Interrupt Module (KBI)**.

NOTE: *The enabling of a keyboard interrupt pin will override the corresponding definition of the pin in the data direction register. However, the data direction register bit must be a 0 for software to read the pin.*

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9.2.2 Data Direction Register A

Data direction register A (DDRA) determines whether each port A pin is an input or an output. Writing a 1 to a DDRA bit enables the output buffer for the corresponding port A pin; a 0 disables the output buffer.

Address:	$0004							
	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
Reset:	0	0	0	0	0	0	0	0

Figure 9-3. Data Direction Register A (DDRA)

DDRA[7:0] — Data Direction Register A Bits

These read/write bits control port A data direction. Reset clears DDRA[7:0], configuring all port A pins as inputs.

1 = Corresponding port A pin configured as output
0 = Corresponding port A pin configured as input

NOTE: *Avoid glitches on port A pins by writing to the port A data register before changing data direction register A bits from 0 to 1.*

Figure 9-4 shows the port A I/O logic.

When bit DDRAx is a 1, reading address $0000 reads the PTAx data latch. When bit DDRAx is a 0, reading address $0000 reads the voltage level on the pin. The data latch can always be written, regardless of the state of its data direction bit. **Table 9-1** summarizes the operation of the port A pins.

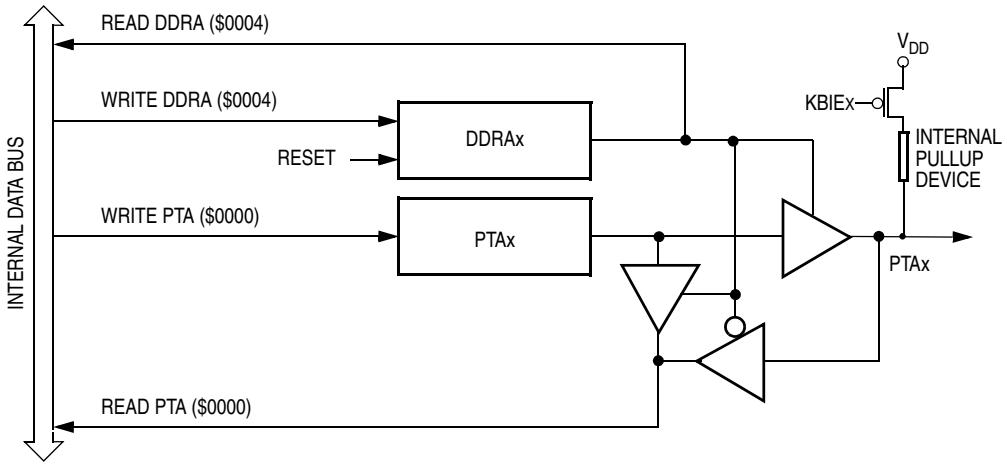

Figure 9-4. Port A I/O Circuit

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Table 9-1. Port A Pin Functions

KBIE[2] Bit	DDRA Bit	PTA Bit	I/O Pin Mode	Accesses to DDRA	Accesses to PTA	
				Read/Write	Read	Write
1	X	X[1]	Input, V_{DD}[4]	DDRA[7:0]	Pin	PTA[7:0][3]
0	0	X	Input, Hi-Z[5]	DDRA[7:0]	Pin	PTA[7:0][3]
0	1	X	Output	DDRA[7:0]	PTA[7:0]	PTA[7:0]

Notes:
1. X = Don't care
2. Keyboard interrupt enable bit (see **7.5.2 Keyboard Interrupt Enable Register**)
3. Writing affects data register, but does not affect input.
4. I/O pin pulled up to V_{DD} by internal pullup device
5. Hi-Z = High impedance

NOTE: *Setting a keyboard interrupt enable bit (KBIEx) forces the corresponding keyboard interrupt pin to be an input, overriding the data direction register. However, the data direction register bit must be a 0 for software to read the pin.*

9.3 Port B

Port B is a 4-bit special function port that shares two of its pins with the timer (TIM) module and one with the buffered internal bus clock MCLK.

9.3.1 Port B Data Register

The port B data register (PTB) contains a data latch for each of the four port B pins.

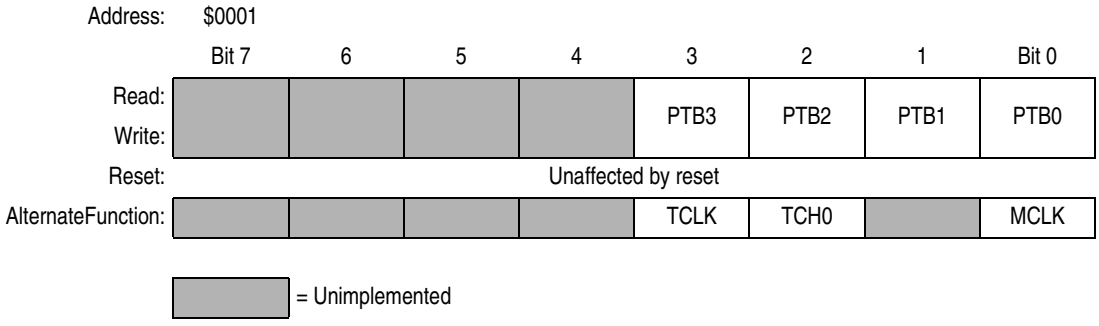

Figure 9-5. Port B Data Register (PTB)

PTB[3:0] — Port B Data Bits

These read/write bits are software-programmable. Data direction of each port B pin is under the control of the corresponding bit in data direction register B. Reset has no effect on port B data.

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TCH0 — Timer Channel I/O Bit

The PTB2/TCH0 pin is the TIM channel 0 input capture/output compare pin. The edge/level select bits, ELS0B:ELS0A, determine whether the PTB2/TCH0 pin is a timer channel I/O or a general-purpose I/O pin. See **Section 11. Timer Interface Module (TIM)**.

TCLK — Timer Clock Bit

The PTB3/TCLK pin is the external clock input for TIM. The prescaler select bits, PS[2:0], select PTB3/TCLK as the TIM clock input. (See **11.8.1 TIM Status and Control Register**.) When not selected as the TIM clock, PTB3/TCLK is available for general-purpose I/O.

MCLK — Bus Clock Bit

The bus clock (MCLK) is driven out of pin PTB0/MCLK when enabled by the MCLKEN bit in port B data direction register bit 7.

9.3.2 Data Direction Register B

Data direction register B (DDRB) determines whether each port B pin is an input or an output. Writing a 1 to a DDRB bit enables the output buffer for the corresponding port B pin; a 0 disables the output buffer.

Address: $0005

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	MCLKEN	0			DDRB3	DDRB2	DDRB1	DDRB0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 9-6. Data Direction Register B (DDRB)

MCLKEN — MCLK Enable Bit

This read/write bit enables MCLK to be an output signal on PTB0. If MCLK is enabled, PTB0 is under the control of MCLKEN. Reset clears this bit.

1 = MCLK output enabled
0 = MCLK output disabled

DDRB[3:0] — Data Direction Register B Bits

These read/write bits control port B data direction. Reset clears DDRB[3:0], configuring all port B pins as inputs.

1 = Corresponding port B pin configured as output
0 = Corresponding port B pin configured as input

NOTE: *Avoid glitches on port B pins by writing to the port B data register before changing data direction register B bits from 0 to 1.*

Figure 9-7 shows the port B I/O logic.

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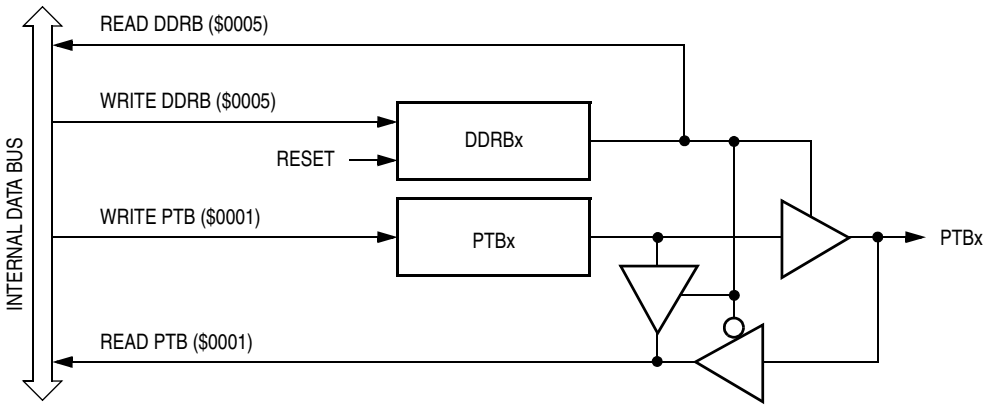

Figure 9-7. Port B I/O Circuit

When bit DDRBx is a 1, reading address $0001 reads the PTBx data latch. When bit DDRBx is a 0, reading address $0001 reads the voltage level on the pin. The data latch can always be written, regardless of the state of its data direction bit. **Table 9-2** summarizes the operation of the port B pins.

Table 9-2. Port B Pin Functions

DDRB Bit	PTB Bit	I/O Pin Mode	Accesses to DDRB	Accesses to PTB	
			Read/Write	Read	Write
0	X	Input, Hi-Z	DDRB[7] DDRB[3:0]	Pin	PTB[3:0](1)
1	X	Output	DDRB[7] DDRB[3:0]	PTB[3:0]	PTB[3:0]

X = Don't care
Hi-Z = High impedance
1. Writing affects data register, but does not affect input.

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Section 10. System Integration Module (SIM)

10.1 Introduction

This section describes the system integration module (SIM). Together with the central processor unit (CPU), the SIM controls all MCU activities. The SIM is a system state controller that coordinates CPU and exception timing. **Figure 10-1** is a summary of the SIM input/output (I/O) registers. A block diagram of the SIM is shown in **Figure 10-2**.

The SIM is responsible for:

- Bus clock generation and control for CPU and peripherals:
  - Stop/wait/reset/break entry and recovery
  - Internal clock control
- Master reset control, including power-on reset (POR) and computer operating properly (COP) timeout
- Interrupt control:
  - Acknowledge timing
  - Arbitration control timing
  - Vector address generation
- CPU enable/disable timing

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$FE00	SIM Break Status Register (SBSR) See page 126.	Read:	R	R	R	R	R	R	SBSW	R
		Write:							See Note	
		Reset:							0	
Note: Writing a 0 clears SBSW										
$FE01	SIM Reset Status Register (SRSR) See page 127.	Read:	POR	PIN	COP	ILOP	ILAD	0	LVI	0
		Write:								
		POR:	1	X	X	X	X	X	X	X
$FE02	SIM Break Flag Control Register (SBFCR) See page 128.	Read:	BCFE	R	R	R	R	R	R	R
		Write:								
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented R = Reserved X = Indeterminate

Figure 10-1. SIM I/O Register Summary

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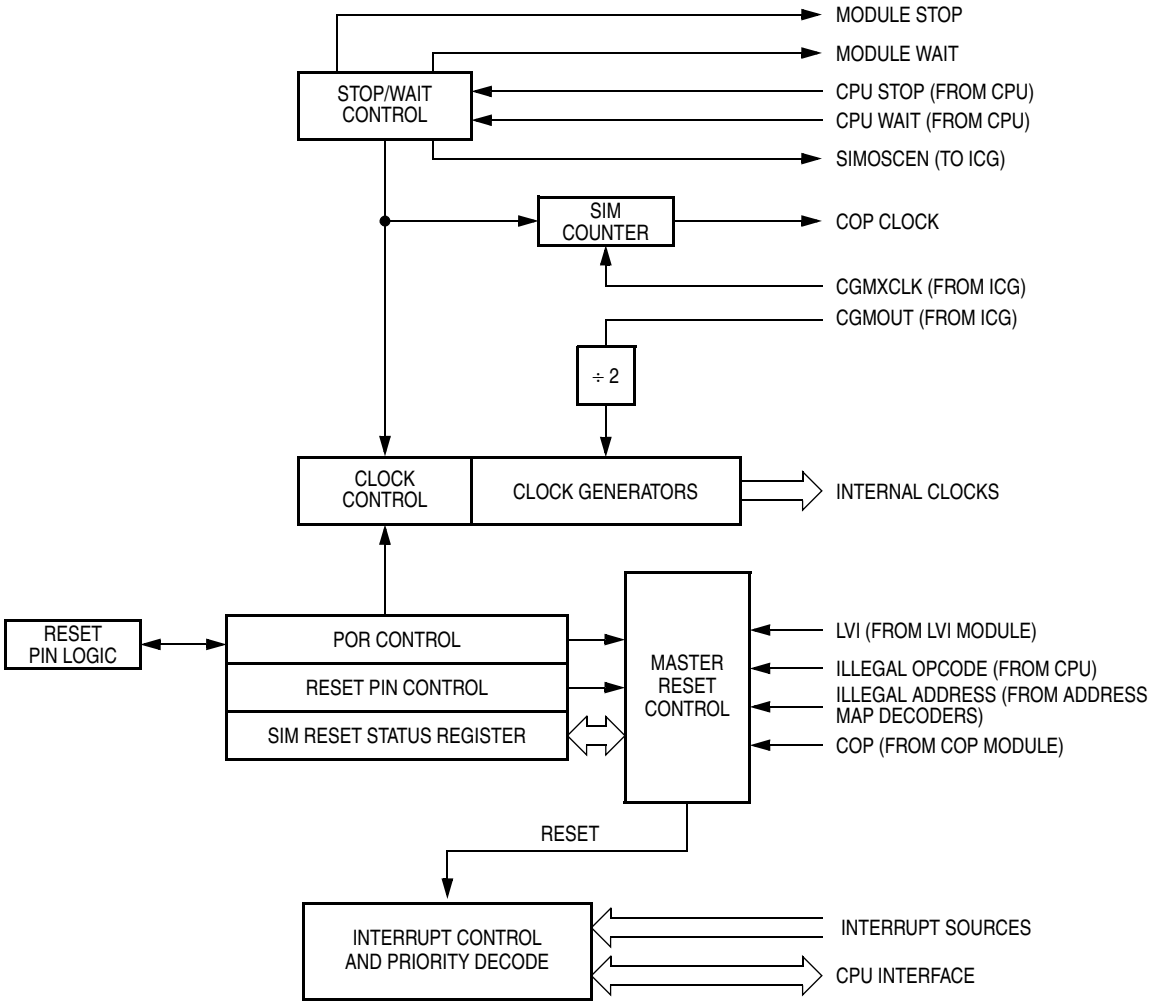

Figure 10-2. SIM Block Diagram

Table 10-1 shows the internal signal names used in this section.

Table 10-1. Signal Name Conventions

Signal Name	Description
CGMXCLK	Selected clock source from internal clock generator module (ICG)
CGMOUT	Clock output from ICG module (bus clock = CGMOUT divided by two)
ICLK	Output from internal clock generator
ECLK	External clock source
IAB	Internal address bus
IDB	internal data bus
PORRST	Signal from the power-on reset module to the SIM
IRST	Internal reset signal
R/$\overline{W}$	Read/write signal

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10.2 SIM Bus Clock Control and Generation

The bus clock generator provides system clock signals for the CPU and peripherals on the MCU. The system clocks are generated from an incoming clock, CGMOUT, as shown in **Figure 10-3**. This clock can come from either an external oscillator or from the internal clock generator (ICG) module.

10.2.1 Bus Timing

In user mode**,** the internal bus frequency is either the crystal oscillator output (ECLK) divided by four or the ICG output (ICLK) divided by four.

10.2.2 Clock Startup from POR or LVI Reset

When the power-on reset (POR) module or the low-voltage inhibit (LVI) module generates a reset, the clocks to the CPU and peripherals are inactive and held in an inactive phase until after 4096 CGMXCLK cycles. The $\overline{\text{RST}}$ pin is driven low by the SIM during this entire period. The bus clocks start upon completion of the timeout.

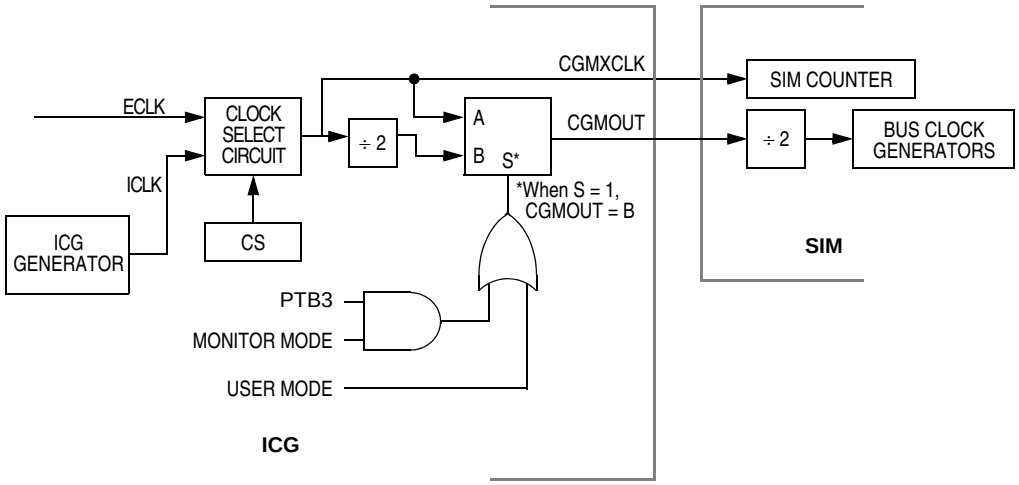

Figure 10-3. ICG Clock Signals

10.2.3 Clocks in Stop Mode and Wait Mode

Upon exit from stop mode by an interrupt, break, or reset, the SIM allows CGMXCLK to clock the SIM counter. The CPU and peripheral clocks do not become active until after the stop delay timeout. This timeout is selectable as 4096 or 32 CGMXCLK cycles. (See **10.6.2 Stop Mode**.)

In wait mode, the CPU clocks are inactive. Refer to the wait mode subsection of each module to see if the module is active or inactive in wait mode. Some modules can be programmed to be active in wait mode.

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10.3 Reset and System Initialization

The MCU has these reset sources:

- Power-on reset module (POR)
- External reset pin ($\overline{RST}$)
- Computer operating properly module (COP)
- Low-voltage inhibit module (LVI)
- Illegal opcode
- Illegal address

All of these resets produce the vector $FFFE–FFFF ($FEFE–FEFF in monitor mode) and assert the internal reset signal (IRST). IRST causes all registers to be returned to their default values and all modules to be returned to their reset states.

An internal reset clears the SIM counter (see **10.4 SIM Counter**), but an external reset does not. Each of the resets sets a corresponding bit in the SIM reset status register (SRSR). (See **10.7 SIM Registers**.)

10.3.1 External Pin Reset

Pulling the asynchronous $\overline{RST}$ pin low halts all processing. The PIN bit of the SIM reset status register (SRSR) is set as long as $\overline{RST}$ is held low for a minimum of 67 CGMXCLK cycles, assuming that neither the POR nor the LVI was the source of the reset.

Figure 10-4 shows the relative timing of an external reset recovery.

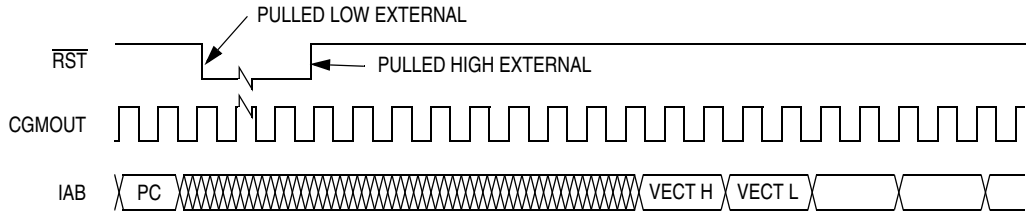

Figure 10-4. External Reset Recovery Timing

10.3.2 Active Resets from Internal Sources

All internal reset sources actively pull the $\overline{RST}$ pin low for 32 CGMXCLK cycles to allow resetting of external peripherals. The internal reset signal IRST continues to be asserted for an additional 32 cycles. (See **Figure 10-5**.) An internal reset can be caused by an illegal address, illegal opcode, COP timeout, LVI, or POR. (See **Figure 10-6**.) Note that for LVI or POR resets, the SIM cycles through 4096 CGMXCLK cycles during which the SIM forces the $\overline{RST}$ pin low. The internal reset

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signal then follows the sequence from the falling edge of $\overline{RST}$ shown in **Figure 10-5**.

The COP reset is asynchronous to the bus clock.

The active reset feature allows the part to issue a reset to peripherals and other chips within a system built around the MCU.

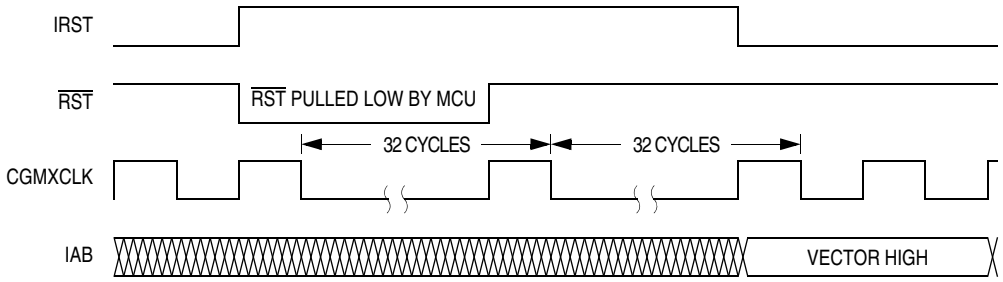

Figure 10-5. Internal Reset Timing

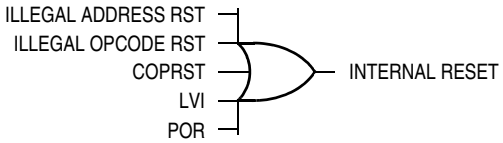

Figure 10-6. Sources of Internal Reset

10.3.2.1 Power-On Reset

When power is first applied to the MCU, the power-on reset module (POR) generates a pulse to indicate that power-on has occurred. The external reset pin ($\overline{RST}$) is held low while the SIM counter counts out 4096 CGMXCLK cycles. Another 64 CGMXCLK cycles later, the CPU and memories are released from reset to allow the reset vector sequence to occur.

At power-on, these events occur:

- A POR pulse is generated.
- The internal reset signal is asserted.
- The SIM enables CGMOUT.
- Internal clocks to the CPU and modules are held inactive for 4096 CGMXCLK cycles to allow stabilization of the oscillator.
- The $\overline{RST}$ pin is driven low during the oscillator stabilization time.
- The POR bit of the SIM reset status register (SRSR) is set and all other bits in the register are cleared.

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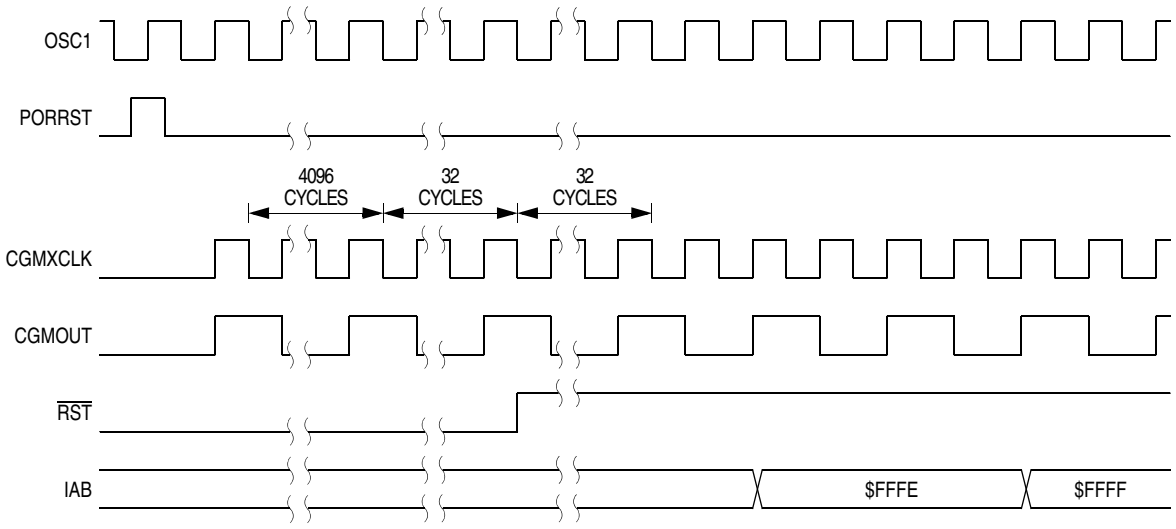

Figure 10-7. POR Recovery

10.3.2.2 Computer Operating Properly (COP) Reset

The overflow of the COP counter causes an internal reset and sets the COP bit in the SIM reset status register (SRSR) if the COPD bit in the CONFIG register is at 0. (See **Section 4. Computer Operating Properly Module (COP)**.)

10.3.2.3 Illegal Opcode Reset

The SIM decodes signals from the CPU to detect illegal instructions. An illegal instruction sets the ILOP bit in the SIM reset status register (SRSR) and causes a reset.

If the stop enable bit, STOP, in the configuration register (CONFIG) is 0, the SIM treats the STOP instruction as an illegal opcode and causes an illegal opcode reset.

10.3.2.4 Illegal Address Reset

An opcode fetch from an unmapped address generates an illegal address reset. The SIM verifies that the CPU is fetching an opcode prior to asserting the ILAD bit in the SIM reset status register (SRSR) and resetting the MCU. A data fetch from an unmapped address does not generate a reset.

10.3.2.5 Low-Voltage Inhibit (LVI) Reset

The low-voltage inhibit module (LVI) asserts its output to the SIM when the V_{DD} voltage falls to the V_{LVR} voltage. The LVI bit in the SIM reset status register (SRSR) is set and a chip reset is asserted if the LVIPWRD and LVIRSTD bits in the CONFIG register are at 0. The $\overline{RST}$ pin will be held low until the SIM counts 4096 CGMXCLK cycles after V_{DD} rises above V_{LVR}+ H_{LVR}. Another 64 CGMXCLK

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cycles later, the CPU is released from reset to allow the reset vector sequence to occur. (See **Section 8. Low-Voltage Inhibit (LVI)**.)

10.4 SIM Counter

The SIM counter is used by the power-on reset module (POR) and in stop mode recovery to allow the oscillator time to stabilize before enabling the internal bus (IBUS) clocks. The SIM counter also serves as a prescaler for the computer operating properly module (COP). The SIM counter overflow supplies the clock for the COP module. The SIM counter is 12 bits long and is clocked by the falling edge of CGMXCLK.

10.4.1 SIM Counter During Power-On Reset

The power-on reset module (POR) detects power applied to the MCU. At power-on, the POR circuit asserts the signal PORRST. Once the SIM is initialized, it enables the internal clock generation module (ICG) to drive the bus clock state machine.

10.4.2 SIM Counter During Stop Mode Recovery

The SIM counter also is used for stop mode recovery. The STOP instruction clears the SIM counter. After an interrupt, break, or reset, the SIM senses the state of the short stop recovery bit, SSREC, in the CONFIG register. If the SSREC bit is a 1, then the stop recovery is reduced from the normal delay of 4096 CGMXCLK cycles down to 32 CGMXCLK cycles. This is ideal for applications using canned oscillators that do not require long startup times from stop mode. External crystal applications should use the full stop recovery time, that is, with SSREC cleared.

10.4.3 SIM Counter and Reset States

External reset has no effect on the SIM counter. See **10.6.2 Stop Mode** for details. The SIM counter is free-running after all reset states. See **10.3.2 Active Resets from Internal Sources** for counter control and internal reset recovery sequences.

10.5 Program Exception Control

Normal, sequential program execution can be changed in three different ways:

1. Interrupts:
   a. Maskable hardware CPU interrupts
   b. Non-maskable software interrupt instruction (SWI)
2. Reset
3. Break interrupts

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10.5.1 Interrupts

At the beginning of an interrupt, the CPU saves the CPU register contents on the stack and sets the interrupt mask (I bit) to prevent additional interrupts. At the end of an interrupt, the RTI instruction recovers the CPU register contents from the stack so that normal processing can resume. **Figure 10-8** shows interrupt entry timing. **Figure 10-9** shows interrupt recovery timing.

Interrupts are latched, and arbitration is performed in the SIM at the start of interrupt processing. The arbitration result is a constant that the CPU uses to determine which vector to fetch. Once an interrupt is latched by the SIM, no other interrupt can take precedence, regardless of priority, until the latched interrupt is serviced (or the I bit is cleared). (See **Figure 10-10**.)

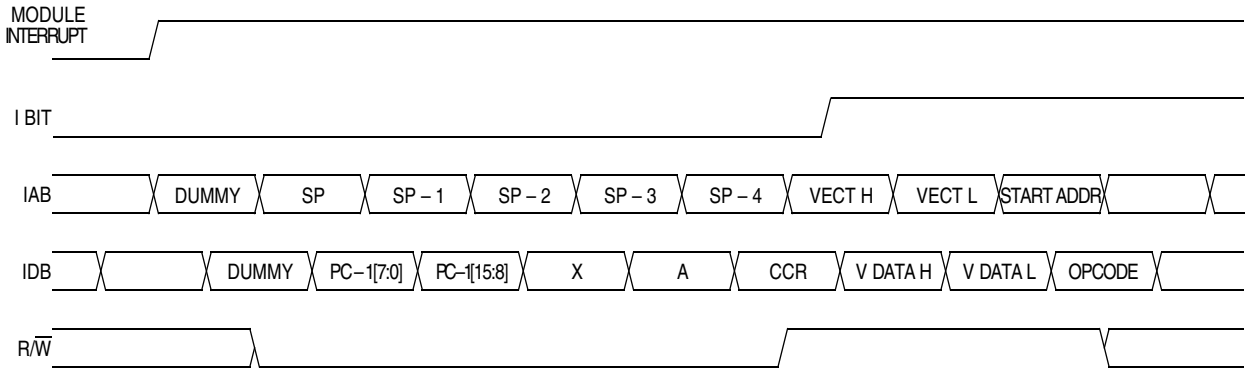

Figure 10-8. Interrupt Entry

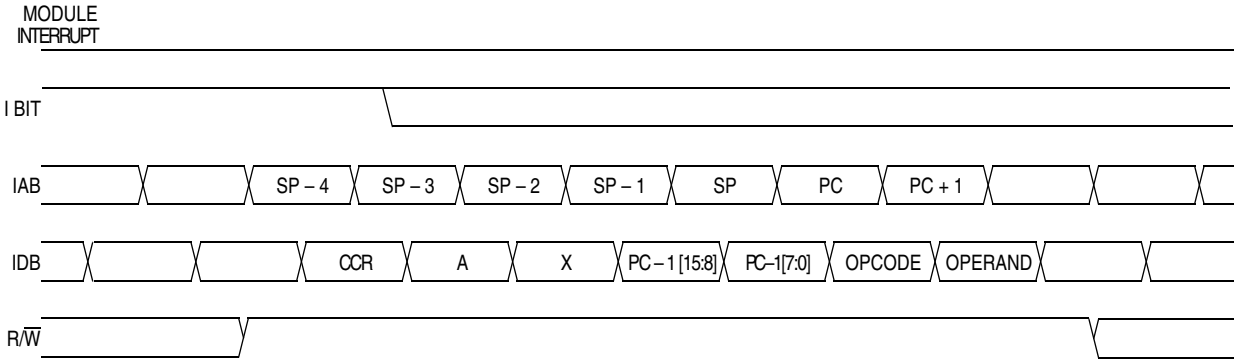

Figure 10-9. Interrupt Recovery

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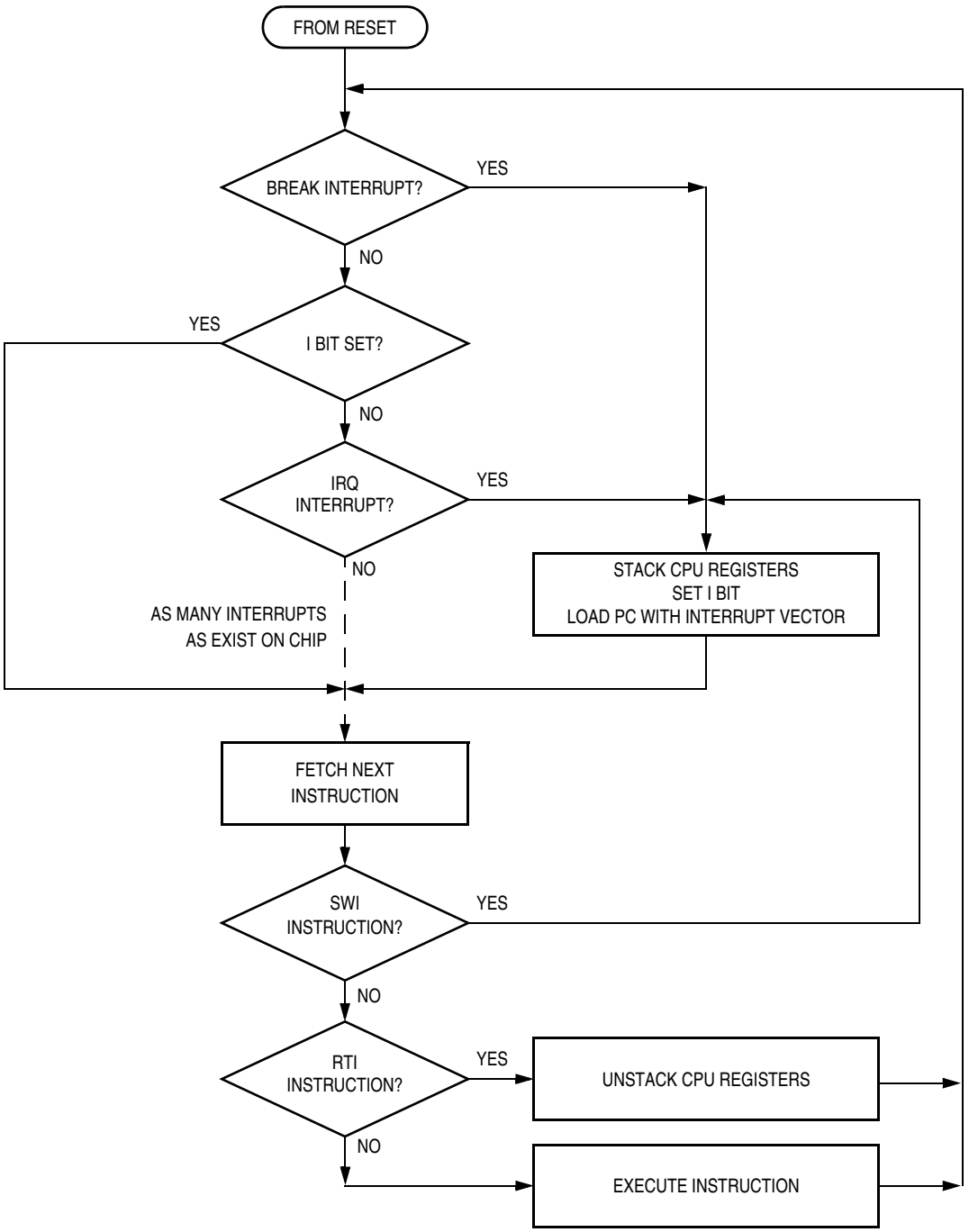

Figure 10-10. Interrupt Processing

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10.5.1.1 Hardware Interrupts

A hardware interrupt does not stop the current instruction. Processing of a hardware interrupt begins after completion of the current instruction. When the current instruction is complete, the SIM checks all pending hardware interrupts. If interrupts are not masked (I bit clear in the condition code register), and if the corresponding interrupt enable bit is set, the SIM proceeds with interrupt processing; otherwise, the next instruction is fetched and executed.

If more than one interrupt is pending at the end of an instruction execution, the highest priority interrupt is serviced first. **Figure 10-11** demonstrates what happens when two interrupts are pending. If an interrupt is pending upon exit from the original interrupt service routine, the pending interrupt is serviced before the LDA instruction is executed.

The LDA opcode is prefetched by both the INT1 and INT2 RTI instructions. However, in the case of the INT1 RTI prefetch, this is a redundant operation.

NOTE: *To maintain compatibility with the M68HC05, M6805, and M146805 Families, the H register is not pushed on the stack during interrupt entry. If the interrupt service routine modifies the H register or uses the indexed addressing mode, software should save the H register and then restore it prior to exiting the routine.*

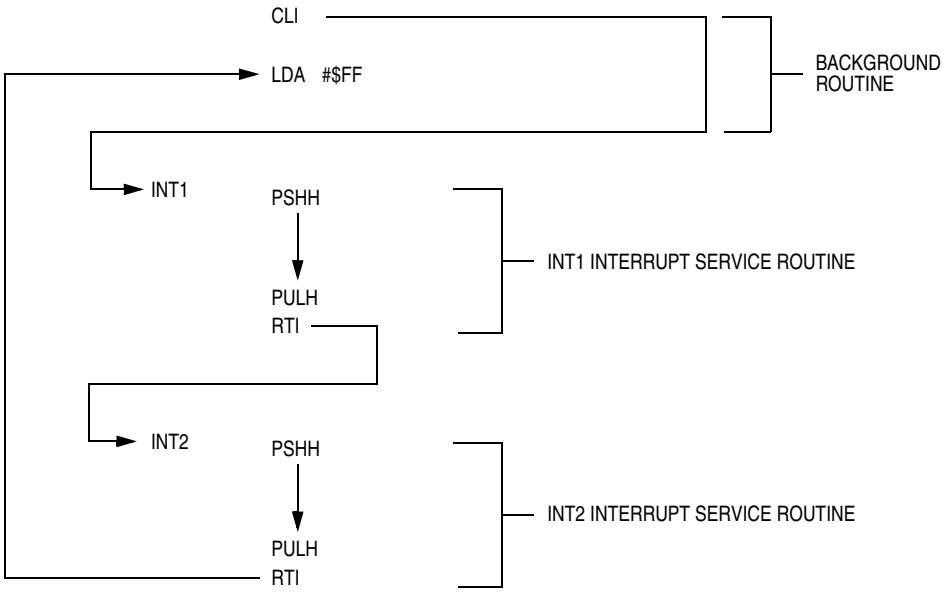

Figure 10-11. Interrupt Recognition Example

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10.5.1.2 SWI Instruction

The SWI instruction is a non-maskable instruction that causes an interrupt regardless of the state of the interrupt mask (I bit) in the condition code register.

NOTE: *A software interrupt pushes PC onto the stack. A software interrupt does **not** push PC – 1, as a hardware interrupt does.*

10.5.2 Reset

All reset sources always have higher priority than interrupts and cannot be arbitrated.

10.5.3 Break Interrupts

The break module can stop normal program flow at a software-programmable break point by asserting its break interrupt output. (See **Section 13. Development Support**.) The SIM puts the CPU into the break state by forcing it to the SWI vector location. Refer to the break interrupt subsection of each module to see how each module is affected by the break state.

10.5.4 Status Flag Protection in Break Mode

The SIM controls whether status flags contained in other modules can be cleared during break mode. The user can select whether flags are protected from being cleared by properly initializing the break clear flag enable bit (BCFE) in the break flag control register (BFCR).

Protecting flags in break mode ensures that set flags will not be cleared while in break mode. This protection allows registers to be freely read and written during break mode without losing status flag information.

Setting the BCFE bit enables the clearing mechanisms. Once cleared in break mode, a flag remains cleared even when break mode is exited. Status flags with a 2-step clearing mechanism — for example, a read of one register followed by the read or write of another — are protected, even when the first step is accomplished prior to entering break mode. Upon leaving break mode, execution of the second step will clear the flag as normal.

10.6 Low-Power Modes

Executing the WAIT or STOP instruction puts the MCU in a low power-consumption mode for standby situations. The SIM holds the CPU in a non-clocked state. The operation of each of these modes is described here. Both STOP and WAIT clear the interrupt mask (I) in the condition code register, allowing interrupts to occur.

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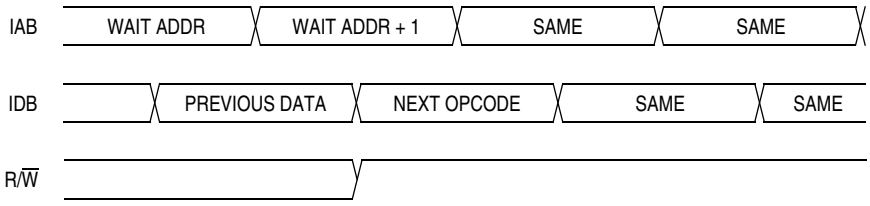
10.6.1 Wait Mode

In wait mode, the CPU clocks are inactive while one set of peripheral clocks continues to run. **Figure 10-12** shows the timing for wait mode entry.

A module that is active during wait mode can wake up the CPU with an interrupt if the interrupt is enabled. Stacking for the interrupt begins one cycle after the WAIT instruction during which the interrupt occurred. Refer to the wait mode subsection of each module to see if the module is active or inactive in wait mode. Some modules can be programmed to be active in wait mode.

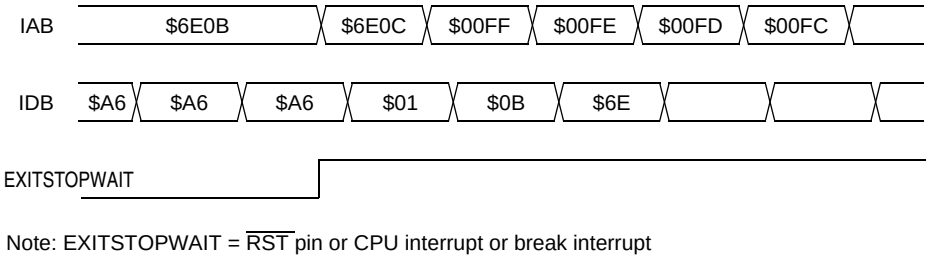
Wait mode can also be exited by a reset or break. A break interrupt during wait mode sets the SIM break stop/wait bit, SBSW, in the SIM break status register (SBSR). If the COP disable bit, COPD, in the mask option register is 0, then the computer operating properly module (COP) is enabled and remains active in wait mode.



Note: Previous data can be operand data or the WAIT opcode, depending on the last instruction.

Figure 10-12. Wait Mode Entry Timing

Figure 10-13 and **Figure 10-14** show the timing for WAIT recovery.



Note: EXITSTOPWAIT = $\overline{\text{RST}}$ pin or CPU interrupt or break interrupt

Figure 10-13. Wait Recovery from Interrupt or Break

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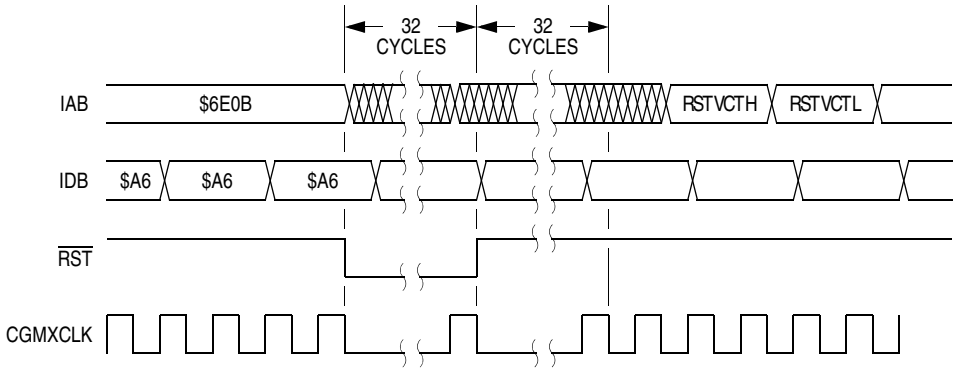


Figure 10-14. Wait Recovery from Internal Reset

10.6.2 Stop Mode

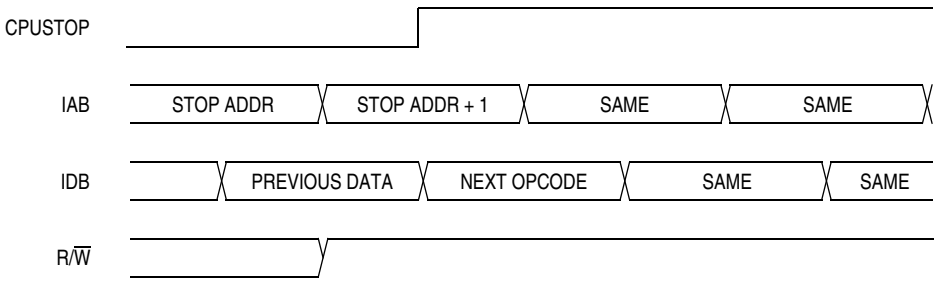
In stop mode, the SIM counter is reset and the system clocks are disabled. An interrupt request from a module can cause an exit from stop mode. Stacking for interrupts begins after the selected stop recovery time has elapsed. Reset or break also causes an exit from stop mode.

The SIM disables the clock generator module outputs (CGMOUT and CGMXCLK) in stop mode, stopping the CPU and peripherals. Stop recovery time is selectable using the SSREC bit in the CONFIG register. If SSREC is set, stop recovery is reduced from the normal delay of 4096 CGMXCLK cycles down to 32. This is ideal for applications using canned oscillators that do not require long startup times from stop mode.

NOTE: *External crystal applications should use the full stop recovery time by clearing the SSREC bit.*

A break interrupt during stop mode sets the SIM break stop/wait bit (SBSW) in the SIM break status register (SBSR).

The SIM counter is held in reset from the execution of the STOP instruction until the beginning of stop recovery. It is then used to time the recovery period. **Figure 10-15** shows stop mode entry timing.



Note: Previous data can be operand data or the STOP opcode, depending on the last instruction.

Figure 10-15. Stop Mode Entry Timing

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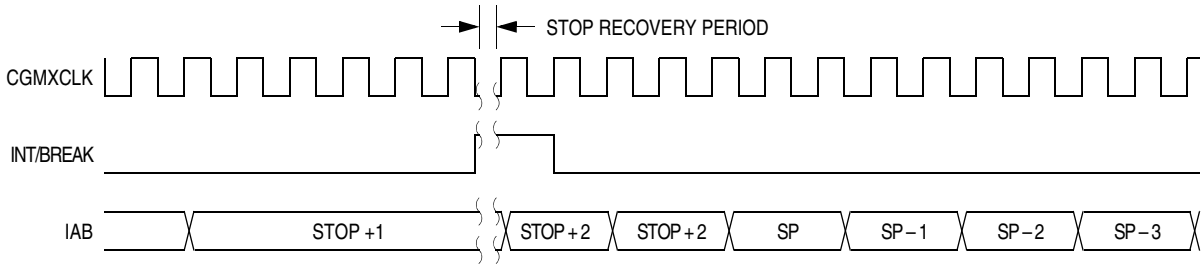

Figure 10-16. Stop Mode Recovery from Interrupt or Break

10.7 SIM Registers

The SIM has three memory mapped registers:

- SIM break status register, SBSR
- SIM reset status register, SRSR
- SIM break flag control register, SBFCR

10.7.1 SIM Break Status Register

The SIM break status register (SBSR) contains a flag to indicate that a break caused an exit from stop or wait mode.

Address: $FE00

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	R	R	R	R	R	R	SBSW	R
Write:							See Note	
Reset:							0	

R = Reserved

Note: Writing a 0 clears SBSW.

Figure 10-17. SIM Break Status Register (SBSR)

SBSW — SIM Break Stop/Wait Bit

SBSW can be read within the break state SWI routine. The user can modify the return address on the stack by subtracting one from it. Writing 0 to the SBSW bit clears it.

1 = Wait mode was exited by break interrupt.

0 = Wait mode was not exited by break interrupt.

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10.7.2 SIM Reset Status Register

This register contains six flags that show the source of the last reset. The status register will clear automatically after reading it. A power-on reset sets the POR bit.

Address: $FE01

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	POR	PIN	COP	ILOP	ILAD	0	LVI	0
Write:								
POR:	1	X	X	X	X	X	X	X

= Unimplemented X = Indeterminate

Figure 10-18. SIM Reset Status Register (SRSR)

POR — Power-On Reset Bit
- 1 = Last reset caused by POR circuit
- 0 = Read of SRSR

PIN — External Reset Bit
- 1 = Last reset caused by external reset pin ($\overline{RST}$)
- 0 = Read of SRSR

COP — Computer Operating Properly Reset Bit
- 1 = Last reset caused by COP counter
- 0 = Read of SRSR

ILOP — Illegal Opcode Reset Bit
- 1 = Last reset caused by an illegal opcode
- 0 = Read of SRSR

ILAD — Illegal Address Reset Bit (opcode fetches only)
- 1 = Last reset caused by an opcode fetch from an illegal address
- 0 = Read of SRSR

LVI — Low-Voltage Inhibit Reset Bit
- 1 = Last reset was caused by the LVI circuit
- 0 = Read of SRSR

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10.7.3 SIM Break Flag Control Register

The SIM break control register contains a bit that enables software to clear status bits while the MCU is in a break state.

Address: $FE02

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BCFE	R	R	R	R	R	R	R
Reset:	0	0	0	0	0	0	0	0

R = Reserved

Figure 10-19. SIM Break Flag Control Register (SBFCR)

BCFE — Break Clear Flag Enable Bit

This read/write bit enables software to clear status bits by accessing status registers while the MCU is in a break state. To clear status bits during the break state, the BCFE bit must be set.

1 = Status bits clearable during break

0 = Status bits not clearable during break

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Section 11. Timer Interface Module (TIM)

11.1 Introduction

This section describes the timer interface module (TIM). The TIM is a 2-channel timer:

- The first channel, channel 0, provides a timing reference with input capture, output compare, and pulse-width-modulation (PWM) functions.
- The second channel, channel 1, provides reduced functionality as it doesn't have an external pin.

Figure 11-2 is a block diagram of the TIM.

11.2 Features

Features of the TIM include:

- One input capture/output compare channel:
  - Rising-edge, falling-edge, or any-edge input capture trigger
  - Set, clear, or toggle output compare action
- Buffered and unbuffered PWM signal generation
- Programmable TIM clock input:
  - 7-frequency internal bus clock prescaler selection
  - External TIM clock input (bus frequency ÷ 2 maximum)
- Free-running or modulo up-count operation
- Toggle any channel pin on overflow
- TIM counter stop and reset bits

11.3 Pin Name Conventions

The TIM module shares pins with two port B input/output (I/O) port pins. The full names of the TIM I/O pins and generic pin names are listed in **Table 11-1**.

Table 11-1. Pin Name Conventions

TIM Generic Pin Names	TCH0	TCLK
Full TIM Pin Names	PTB2/TCH0	PTB3/TCLK

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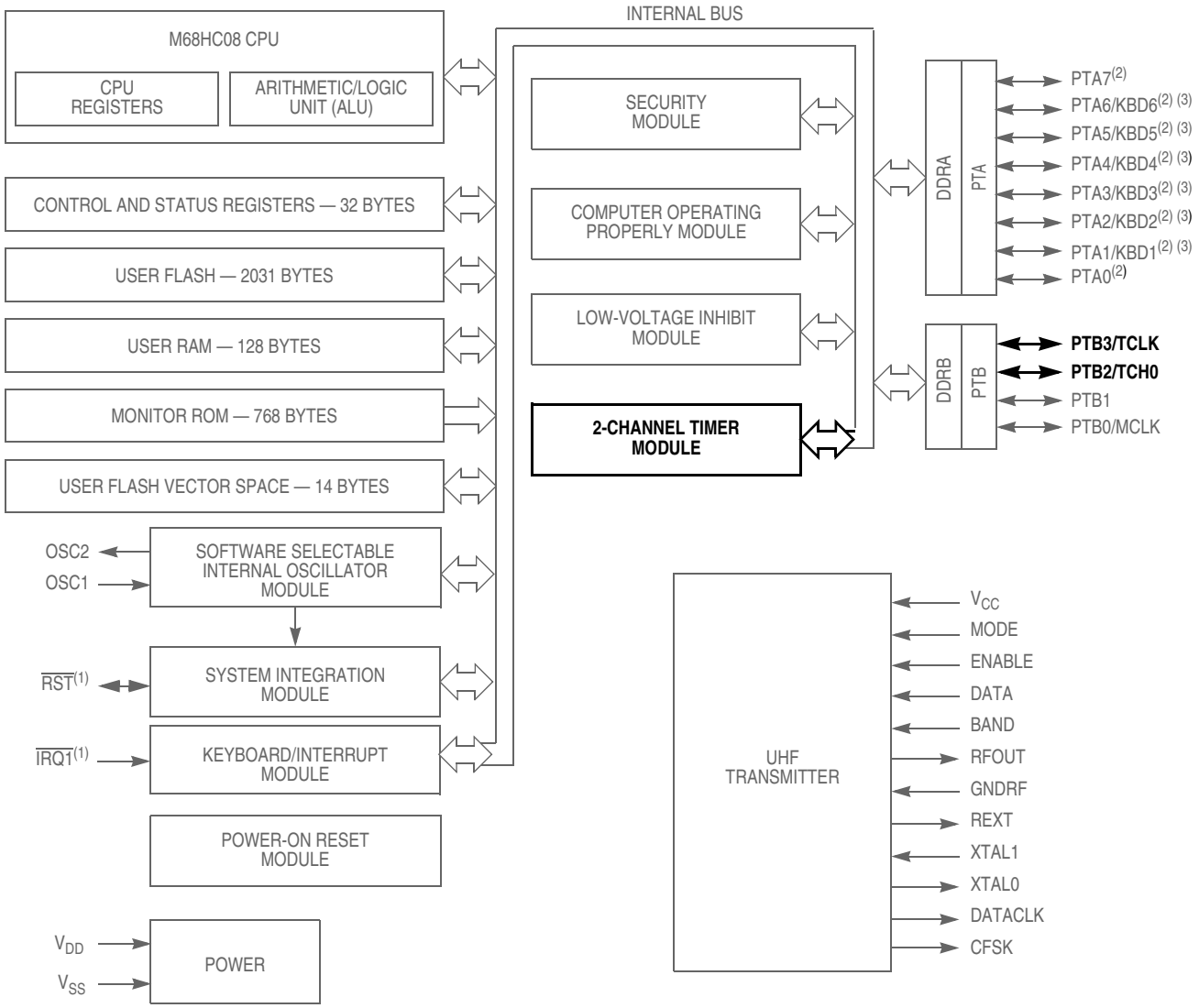

1. Pin contains integrated pullup resistor
2. High current sink pin
3. Pin contains software selectable pullup resistor

Figure 11-1. Block Diagram Highlighting TIM Block and Pins

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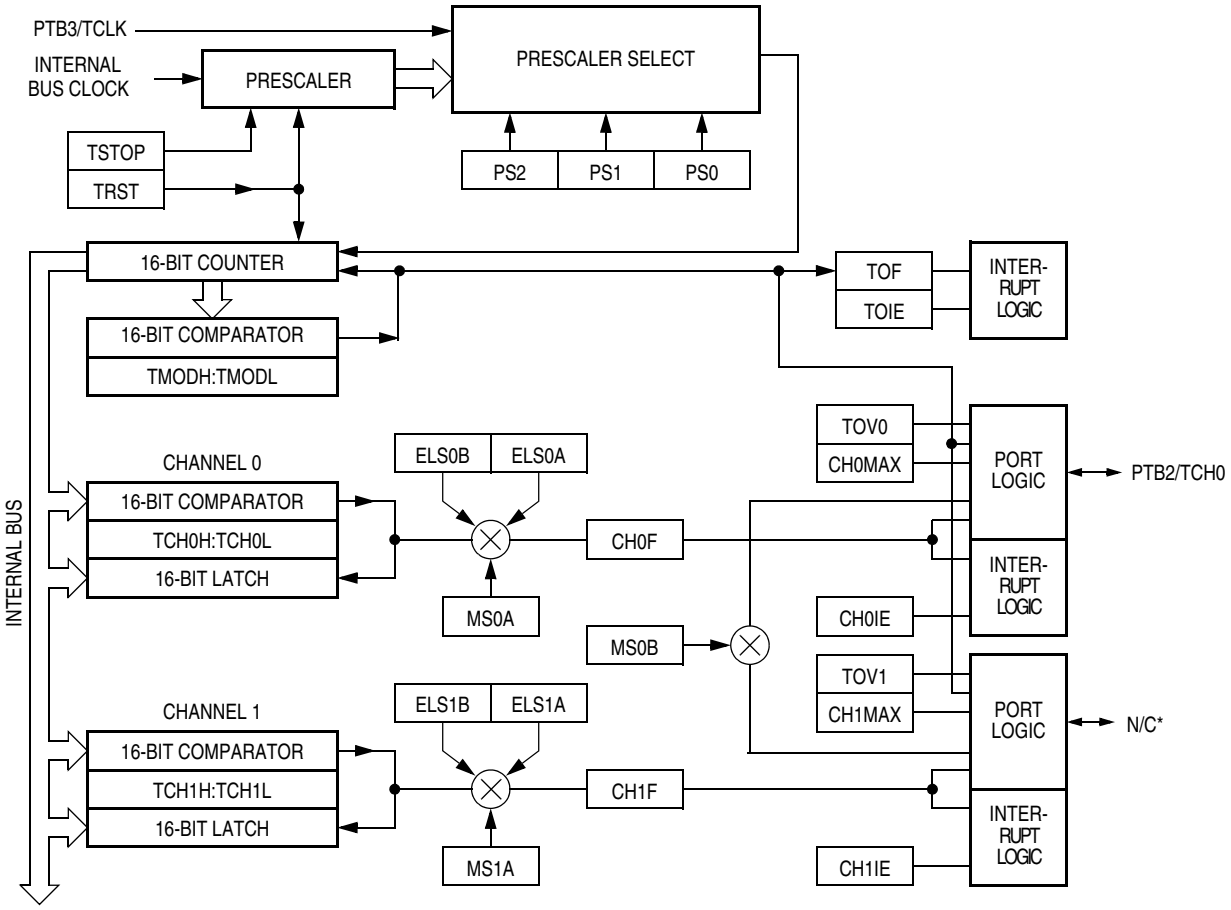
11.4 Functional Description

Figure 11-2 shows the structure of the TIM. The central component of the TIM is the 16-bit TIM counter that can operate as a free-running counter or a modulo up-counter. The TIM counter provides the timing reference for the input capture and output compare functions. The TIM counter modulo registers, TMODH and TMODL, control the modulo value of the TIM counter. Software can read the TIM counter value at any time without affecting the counting sequence.

TIM channel 0 is programmable independently as input capture or output compare. TIM channel 1 is programmable only as output compare. The output compare is detected only through an interrupt.

WARNING: ***TIM channel 1 should not be configured as an input capture because this would result in a floating input that would cause a higher I_{DD}.***

Refer to Figure 11-3 for a summary of the TIM I/O registers.



*This pin is not available on the MC68HC908RF2.

Figure 11-2. TIM Block Diagram

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Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0020	Timer Status and Control Register (TSC) See page 139.	Read:	TOF	TOIE	TSTOP	0	0	PS2	PS1	PS0
		Write:	0			TRST				
		Reset:	0	0	1	0	0	0	0	0
$0021	Timer Counter Register High (TCNTH) See page 141.	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0022	Timer Counter Register Low (TCNTL) See page 141.	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0023	Timer Counter Modulo Register High (TMODH) See page 142.	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	1	1	1	1	1	1	1	1
$0024	Timer Counter Modulo Register Low (TMODL) See page 142.	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	1	1	1	1	1	1	1	1
$0025	Timer Channel 0 Status and Control Register (TSC0) See page 143.	Read:	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	TOV0	CH0MAX
		Write:	0							
		Reset:	0	0	0	0	0	0	0	0
$0026	Timer Channel 0 Register High (TCH0H) See page 146.	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	Indeterminate after reset							
$0027	Timer Channel 0 Register Low (TCH0L) See page 146.	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	Indeterminate after reset							
$0028	Timer Channel 1 Status and Control Register (TSC1) See page 143.	Read:	CH1F	CH1IE	0	MS1A	ELS1B	ELS1A	TOV1	CH1MAX
		Write:	0							
		Reset:	0	0	0	0	0	0	0	0
$0029	Timer Channel 1 Register High (TCH1H)) See page 146.	Read:	Bit 15	14	13	12	11	10	9	Bit 8
		Write:								
		Reset:	Indeterminate after reset							
$002A	Timer Channel 1 Register Low (TCH1L)) See page 146.	Read:	Bit 7	6	5	4	3	2	1	Bit 0
		Write:								
		Reset:	Indeterminate after reset							

= Unimplemented

Figure 11-3. TIM I/O Register Summary

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11.4.1 TIM Counter Prescaler

The TIM clock source can be one of the seven prescaler outputs or the TIM clock pin, TCLK. The prescaler generates seven clock rates from the internal bus clock. The prescaler select bits, PS[2:0], in the TIM status and control register select the TIM clock source.

11.4.2 Input Capture

With the input capture function, the TIM can capture the time at which an external event occurs. When an active edge occurs on the pin of an input capture channel, the TIM latches the contents of the TIM counter into the TIM channel registers, TCHxH and TCHxL. The polarity of the active edge is programmable. Input captures can generate TIM CPU interrupt requests.

NOTE: *TIM channel 1 should not be configured in this mode.*

11.4.3 Output Compare

With the output compare function, the TIM can generate a periodic pulse with a programmable polarity, duration, and frequency. When the counter reaches the value in the registers of an output compare channel, the TIM channel 0 can set, clear, or toggle the channel pin. Output compares can generate TIM CPU interrupt requests for both TIM channel 0 and TIM channel 1.

NOTE: *TIM channel 1 does not have an external pin associated with it.*

11.4.4 Unbuffered Output Compare

Any output compare channel can generate unbuffered output compare pulses as described in **11.4.3 Output Compare**. The pulses are unbuffered because changing the output compare value requires writing the new value over the old value currently in the TIM channel registers.

An unsynchronized write to the TIM channel registers to change an output compare value could cause incorrect operation for up to two counter overflow periods. For example, writing a new value before the counter reaches the old value but after the counter reaches the new value prevents any compare during that counter overflow period. Also, using a TIM overflow interrupt routine to write a new, smaller output compare value may cause the compare to be missed. The TIM may pass the new value before it is written.

Use these methods to synchronize unbuffered changes in the output compare value on channel x:

- When changing to a smaller value, enable channel x output compare interrupts and write the new value in the output compare interrupt routine. The output compare interrupt occurs at the end of the current output compare pulse. The interrupt routine has until the end of the counter overflow period to write the new value.

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- When changing to a larger output compare value, enable TIM overflow interrupts and write the new value in the TIM overflow interrupt routine. The TIM overflow interrupt occurs at the end of the current counter overflow period. Writing a larger value in an output compare interrupt routine (at the end of the current pulse) could cause two output compares to occur in the same counter overflow period.

11.4.5 Buffered Output Compare

Channels 0 and 1 can be linked to form a buffered output compare channel whose output appears on the PTB2/TCH0 pin. The TIM channel registers of the linked pair alternately control the output.

Setting the MS0B bit in TIM channel 0 status and control register (TSC0) links channel 0 and channel 1. The output compare value in the TIM channel 0 registers initially controls the output on the TCH0 pin. Writing to the TIM channel 1 registers enables the TIM channel 1 registers to synchronously control the output after the TIM overflows. At each subsequent overflow, the TIM channel registers (0 or 1) that control the output are the ones written to last. TSC0 controls and monitors the buffered output compare function, and TIM channel 1 status and control register (TSC1) is unused.

NOTE: *In buffered output compare operation, do not write new output compare values to the currently active channel registers. User software should track the currently active channel to prevent writing a new value to the active channel. Writing to the active channel registers is the same as generating unbuffered output compares.*

11.4.6 Pulse-Width Modulation (PWM)

By using the toggle-on-overflow feature with an output compare channel, the TIM can generate a pulse-width modulation (PWM) signal. The value in the TIM counter modulo registers determines the period of the PWM signal. The channel pin toggles when the counter reaches the value in the TIM counter modulo registers. The time between overflows is the period of the PWM signal.

As **Figure 11-4** shows, the output compare value in the TIM channel registers determines the pulse width of the PWM signal. The time between overflow and output compare is the pulse width. Program the TIM to clear channel 0 pin on output compare if the state of the PWM pulse is logic 1. Program the TIM to set the pin if the state of the PWM pulse is logic 0.

The value in the TIM counter modulo registers and the selected prescaler output determines the frequency of the PWM output. The frequency of an 8-bit PWM signal is variable in 256 increments. Writing $00FF (255) to the TIM counter modulo registers produces a PWM period of 256 times the internal bus clock period if the prescaler select value is $000. See **11.8.1 TIM Status and Control Register**.

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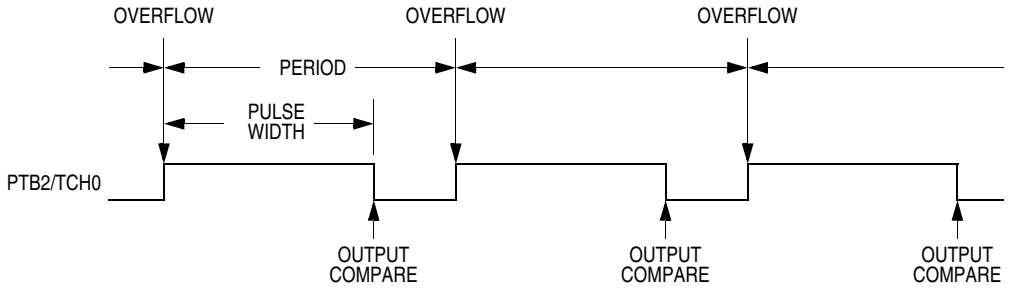

Figure 11-4. PWM Period and Pulse Width

The value in the TIM channel registers determines the pulse width of the PWM output. The pulse width of an 8-bit PWM signal is variable in 256 increments. Writing $0080 (128) to the TIM channel registers produces a duty cycle of 128/256 or 50 percent.

11.4.7 Unbuffered PWM Signal Generation

Any output compare channel can generate unbuffered PWM pulses as described in **11.4.6 Pulse-Width Modulation (PWM)**. The pulses are unbuffered because changing the pulse width requires writing the new pulse width value over the old value currently in the TIM channel registers.

An unsynchronized write to the TIM channel registers to change a pulse width value could cause incorrect operation for up to two PWM periods. For example, writing a new value before the counter reaches the old value but after the counter reaches the new value prevents any compare during that PWM period. Also, using a TIM overflow interrupt routine to write a new, smaller pulse width value may cause the compare to be missed. The TIM may pass the new value before it is written.

Use these methods to synchronize unbuffered changes in the PWM pulse width on channel:

- When changing to a shorter pulse width, enable channel output compare interrupts and write the new value in the output compare interrupt routine. The output compare interrupt occurs at the end of the current pulse. The interrupt routine has until the end of the PWM period to write the new value.
- When changing to a longer pulse width, enable TIM overflow interrupts and write the new value in the TIM overflow interrupt routine. The TIM overflow interrupt occurs at the end of the current PWM period. Writing a larger value in an output compare interrupt routine (at the end of the current pulse) could cause two output compares to occur in the same PWM period.

NOTE: *In PWM signal generation, do not program the PWM channel to toggle on output compare. Toggling on output compare prevents reliable 0 percent duty cycle generation and removes the ability of the channel to self-correct in the event of software error or noise. Toggling on output compare also can cause incorrect PWM signal generation when changing the PWM pulse width to a new, much larger value.*

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11.4.8 Buffered PWM Signal Generation

Channels 0 and 1 can be linked to form a buffered PWM channel whose output appears on the TCH0 pin. The TIM channel registers of the linked pair alternately control the pulse width of the output.

Setting the MS0B bit in TIM channel 0 status and control register (TSC0) links channel 0 and channel 1. The TIM channel 0 registers initially control the pulse width on the TCH0 pin. Writing to the TIM channel 1 registers enables the TIM channel 1 registers to synchronously control the pulse width at the beginning of the next PWM period. At each subsequent overflow, the TIM channel registers (0 or 1) that control the pulse width are the ones written to last. TSC0 controls and monitors the buffered PWM function, and TIM channel 1 status and control register (TSC1) is unused.

NOTE: *In buffered PWM signal generation, do not write new pulse width values to the currently active channel registers. User software should track the currently active channel to prevent writing a new value to the active channel. Writing to the active channel registers is the same as generating unbuffered PWM signals.*

11.4.9 PWM Initialization

To ensure correct operation when generating unbuffered or buffered PWM signals, use this initialization procedure:

1. In the TIM status and control register (TSC):
   a. Stop the TIM counter by setting the TIM stop bit, TSTOP.
   b. Reset the TIM counter and prescaler by setting the TIM reset bit, TRST.
2. In the TIM counter modulo registers (TMODH and TMODL), write the value for the required PWM period.
3. In the TIM channel x registers (TCHxH and TCHxL), write the value for the required pulse width.
4. In TIM channel x status and control register (TSCx):
   a. Write 0:1 (for unbuffered output compare or PWM signals) or 1:0 (for buffered output compare or PWM signals) to the mode select bits, MSxB and MSxA. See **Table 11-3**.
   b. Write 1 to the toggle-on-overflow bit, TOVx.
   c. Write 1:0 (to clear output on compare) or 1:1 (to set output on compare) to the edge/level select bits, ELSxB and ELSxA. The output action on compare must force the output to the complement of the pulse width level. See **Table 11-3**.

NOTE: *In PWM signal generation, do not program the PWM channel to toggle on output compare. Toggling on output compare prevents reliable 0 percent duty cycle generation and removes the ability of the channel to self-correct in the event of software error or noise. Toggling on output compare can also cause incorrect PWM*

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signal generation when changing the PWM pulse width to a new, much larger value.

5. In the TIM status control register (TSC), clear the TIM stop bit, TSTOP.

Setting MS0B links channels 0 and 1 and configures them for buffered PWM operation. The TIM channel 0 registers (TCH0H and TCH0L) initially control the buffered PWM output. TIM status control register 0 (TSCR0) controls and monitors the PWM signal from the linked channels.

Clearing the toggle-on-overflow bit, TOVx, inhibits output toggles on TIM overflows. Subsequent output compares try to force the output to a state it is already in and have no effect. The result is a 0 percent duty cycle output.

Setting the channel x maximum duty cycle bit (CHxMAX) and setting the TOVx bit generates a 100 percent duty cycle output. See **11.8.4 TIM Channel Status and Control Registers**.

11.5 Interrupts

These TIM sources can generate interrupt requests:

- TIM overflow flag (TOF) — The timer overflow flag (TOF) bit is set when the TIM counter reaches the modulo value programmed in the TIM counter modulo registers. The TIM overflow interrupt enable bit, TOIE, enables TIM overflow interrupt requests. TOF and TOIE are in the TIM status and control registers.
- TIM channel flag (CH0F) — The CH0F bit is set when an input capture or output compare occurs on channel. Channel TIM CPU interrupt requests are controlled by the channel interrupt enable bit, CH1IE.

11.5.1 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power- consumption standby modes.

11.5.2 Wait Mode

The TIM remains active after the execution of a WAIT instruction. In wait mode, the TIM registers are not accessible by the CPU. Any enabled CPU interrupt request from the TIM can bring the MCU out of wait mode.

If TIM functions are not required during wait mode, reduce power consumption by stopping the TIM before executing the WAIT instruction.

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11.5.3 Stop Mode

The TIM is inactive after the execution of a STOP instruction. The STOP instruction does not affect register conditions or the state of the TIM counter. TIM operation resumes when the MCU exits stop mode after an external interrupt.

11.6 TIM During Break Interrupts

A break interrupt stops the TIM counter.

The system integration module (SIM) controls whether status bits in other modules can be cleared during the break state. The BCFE bit in the SIM break flag control register (SBFCR) enables software to clear status bits during the break state. See **10.7.3 SIM Break Flag Control Register**.

To allow software to clear status bits during a break interrupt, write a 1 to the BCFE bit. If a status bit is cleared during the break state, it remains cleared when the MCU exits the break state.

To protect status bits during the break state, write a 0 to the BCFE bit. With BCFE at 0 (its default state), software can read and write I/O registers during the break state without affecting status bits. Some status bits have a 2-step read/write clearing procedure. If software does the first step on such a bit before the break, the bit cannot change during the break state as long as BCFE is at 0. After the break, doing the second step clears the status bit.

11.7 I/O Signals

Port B shares two of its pins with the TIM. TCLK can be used as an external clock input to the TIM prescaler and the TIM channel 0 I/O pin PTB2/TCH0.

11.7.1 TIM Clock Pin (TCLK)

TCLK is an external clock input that can be the clock source for the TIM counter instead of the prescaled internal bus clock. Select the TCLK input by writing 1s to the three prescaler select bits, PS2–PS0. See **11.8.1 TIM Status and Control Register**. The minimum TCLK pulse width, $TCLK_{LMIN}$ or $TCLK_{HMIN}$, is:

$$\frac{1}{\text{bus frequency}} + t_{su}$$

The maximum TCLK frequency is:
bus frequency ÷ 2

Refer to **14.9 Control Timing**.

TCLK is available as a general-purpose I/O pin when not used as the TIM clock input. When the TCLK pin is the TIM clock input, it is an input regardless of the state of the DDRB3 bit in data direction register B.

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11.7.2 TIM Channel I/O Pins (TCH0)

The channel I/O pins are programmable independently as an input capture pin or an output compare pin. TCH0 can be configured as buffered output compare or buffered PWM pins.

11.8 I/O Registers

These I/O registers control and monitor operation of the TIM:

- TIM status and control register, TSC
- TIM control registers, TCNTH and TCNTL
- TIM counter modulo registers, TMODH and TMODL
- TIM channel status and control registers, TSC0 and TSC1
- TIM channel registers, TCH0H, TCH0L, TCH1H, and TCH1L

11.8.1 TIM Status and Control Register

The TIM status and control register (TSC):

- Enables TIM overflow interrupts
- Flags TIM overflows
- Stops the TIM counter
- Resets the TIM counter
- Prescales the TIM counter clock

Address: $0020

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TOF	TOIE	TSTOP	0	0	PS2	PS1	PS0
Write:	0			TRST				
Reset:	0	0	1	0	0	0	0	0

= Unimplemented

Figure 11-5. TIM Status and Control Register

TOF — TIM Overflow Flag Bit

This read/write flag is set when the TIM counter reaches the modulo value programmed in the TIM counter modulo registers. Clear TOF by reading the TIM status and control register when TOF is set and then writing a 0 to TOF. If another TIM overflow occurs before the clearing sequence is complete, then writing 0 to TOF has no effect. Therefore, a TOF interrupt request cannot be lost due to inadvertent clearing of TOF. Reset clears the TOF bit. Writing a 1 to TOF has no effect.

1 = TIM counter has reached modulo value.
0 = TIM counter has not reached modulo value.

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TOIE — TIM Overflow Interrupt Enable Bit

This read/write bit enables TIM overflow interrupts when the TOF bit becomes set. Reset clears the TOIE bit.

1 = TIM overflow interrupts enabled
0 = TIM overflow interrupts disabled

TSTOP — TIM Stop Bit

This read/write bit stops the TIM counter. Counting resumes when TSTOP is cleared. Reset sets the TSTOP bit, stopping the TIM counter until software clears the TSTOP bit.

1 = TIM counter stopped
0 = TIM counter active

NOTE: *Do not set the TSTOP bit before entering wait mode if the TIM is required to exit wait mode.*

TRST — TIM Reset Bit

Setting this write-only bit resets the TIM counter and the TIM prescaler. Setting TRST has no effect on any other registers. Counting resumes from $0000. TRST is cleared automatically after the TIM counter is reset and always reads as 0. Reset clears the TRST bit.

1 = Prescaler and TIM counter cleared
0 = No effect

NOTE: *Setting the TSTOP and TRST bits simultaneously stops the TIM counter at a value of $0000.*

PS2–PS0 — Prescaler Select Bits

These read/write bits select either the TCLK pin or one of the seven prescaler outputs as the input to the TIM counter as **Table 11-2** shows. Reset clears the PS2–PS0 bits.

Table 11-2. Prescaler Selection

PS2–PS0	TIM Clock Source
000	Internal bus clock ÷1
001	Internal bus clock ÷ 2
010	Internal bus clock ÷ 4
011	Internal bus clock ÷ 8
100	Internal bus clock ÷ 16
101	Internal bus clock ÷ 32
110	Internal bus clock ÷ 64
111	TCLK

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11.8.2 TIM Counter Registers

The two read-only TIM counter registers contain the high and low bytes of the value in the TIM counter. Reading the high byte (TCNTH) latches the contents of the low byte (TCNTL) into a buffer. Subsequent reads of TCNTH do not affect the latched TCNTL value until TCNTL is read. Reset clears the TIM counter registers. Setting the TIM reset bit (TRST) also clears the TIM counter registers

NOTE: *If you read TCNTH during a break interrupt, be sure to unlatch TCNTL by reading TCNTL before exiting the break interrupt. Otherwise, TCNTL retains the value latched during the break.*

Register Name and Address: TCNTH—$0021

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 15	14	13	12	11	10	9	Bit 8
Write:								
Reset:	0	0	0	0	0	0	0	0

Register Name and Address: TCNTL—$0022

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	6	5	4	3	2	1	Bit 0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 11-6. TIM Counter Registers (TCNTH and TCNTL)

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11.8.3 TIM Counter Modulo Registers

The read/write TIM modulo registers contain the modulo value for the TIM counter. When the TIM counter reaches the modulo value, the overflow flag (TOF) becomes set, and the TIM counter resumes counting from $0000 at the next timer clock. Writing to the high byte (TMODH) inhibits the TOF bit and overflow interrupts until the low byte (TMODL) is written. Reset sets the TIM counter modulo registers.

Register Name and Address: TMODH—$0023

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
Reset:	1	1	1	1	1	1	1	1

Register Name and Address: TMODL—$0024

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
Reset:	1	1	1	1	1	1	1	1

Figure 11-7. TIM Counter Modulo Registers (TMODH and TMODL)

NOTE: *Reset the TIM counter before writing to the TIM counter modulo registers.*

11.8.4 TIM Channel Status and Control Registers

Each of the TIM channel status and control registers (TSC0 and TSC1):

- Flags input captures and output compares
- Enables input capture and output compare interrupts
- Selects input capture, output compare, or PWM operation
- Selects high, low, or toggling output on output compare
- Selects rising edge, falling edge, or any edge as the active input capture trigger
- Selects output toggling on TIM overflow
- Selects 0 percent and 100 percent PWM duty cycle
- Selects buffered or unbuffered output compare/PWM operation

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Register Name and Address: TSC0—$0025

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	CH0F	CH0IE	MS0B	MS0A	ELS0B	ELS0A	TOV0	CH0MAX
Write:	0							
Reset:	0	0	0	0	0	0	0	0

Register Name and Address: TSC1—$0028

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	CH1F	CH1IE	0	MS1A	ELS1B	ELS1A	TOV1	CH1MAX
Write:	0							
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 11-8. TIM Channel Status and Control Registers (TSC0 and TSC1)

CHxF — Channel x Flag Bit

When channel x is an input capture channel, this read/write bit is set when an active edge occurs on the channel x pin. When channel x is an output compare channel, CHxF is set when the value in the TIM counter registers matches the value in the TIM channel x registers.

When TIM CPU interrupt requests are enabled (CHxIE = 1), clear CHxF by reading TIM channel x status and control register with CHxF set and then writing a 0 to CHxF. If another interrupt request occurs before the clearing sequence is complete, then writing 0 to CHxF has no effect. Therefore, an interrupt request cannot be lost due to inadvertent clearing of CHxF.

Reset clears the CHxF bit. Writing a 1 to CHxF has no effect.

1 = Input capture or output compare on channel x
0 = No input capture or output compare on channel x

CHxIE — Channel x Interrupt Enable Bit

This read/write bit enables TIM CPU interrupts on channel x.

Reset clears the CHxIE bit.

1 = Channel x CPU interrupt requests enabled
0 = Channel x CPU interrupt requests disabled

MSxB — Mode Select Bit B

This read/write bit selects buffered output compare/PWM operation. MSxB exists only in the TIM channel 0 and TIM channel 1 status and control registers. Setting MS0B disables the TIM channel 1 status and control register. Reset clears the MSxB bit.

1 = Buffered output compare/PWM operation enabled
0 = Buffered output compare/PWM operation disabled

MSxA — Mode Select Bit A

When ELSxB:A ≠ 00, this read/write bit selects either input capture operation or unbuffered output compare/PWM operation. See **Table 11-3**.

1 = Unbuffered output compare/PWM operation
0 = Input capture operation

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When ELSxB:A = 00, this read/write bit selects the initial output level of the TCH0 pin. See **Table 11-3**. Reset clears the MSxA bit.

1 = Initial output level low
0 = Initial output level high

NOTE: *Before changing a channel function by writing to the MSxB or MSxA bit, set the TSTOP and TRST bits in the TIM status and control register (TSC).*

Table 11-3. Mode, Edge, and Level Selection

MSxB	MSxA	ELSxB	ELSxA	Mode	Configuration
X	0	0	0	Output preset	Pin under port control; initial output level high
X	1	0	0		Pin under port control; initial output level low
0	0	0	1	Input capture	Capture on rising edge only
0	0	1	0		Capture on falling edge only
0	0	1	1		Capture on rising or falling edge
0	1	0	0	Output compare or PWM	Software compare only
0	1	0	1		Toggle output on compare
0	1	1	0		Clear output on compare
0	1	1	1		Set output on compare
1	X	0	1	Buffered output compare or buffered PWM	Toggle output on compare
1	X	1	0		Clear output on compare
1	X	1	1		Set output on compare

ELSxB and ELSxA — Edge/Level Select Bits

When channel 0 is an input capture channel, these read/write bits control the active edge-sensing logic on channel x. When channel x is an output compare channel, ELSxB and ELSxA control the channel x output behavior when an output compare occurs.

When ELSxB and ELSxA are both clear, channel x is not connected to port B, and pin PTB0/TCH0 is available as a general-purpose I/O pin. **Table 11-3** shows how ELSxB and ELSxA work. Reset clears the ELSxB and ELSxA bits.

NOTE: *TIM channel 1 does not have an external pin associated with it.*

NOTE: *Before enabling a TIM channel register for input capture operation, make sure that the PTB/TCH0 pin is stable for at least two bus clocks.*

TOVx — Toggle On Overflow Bit

When channel 0 is an output compare channel, this read/write bit controls the behavior of the channel 0 output when the TIM counter overflows. When channel 0 is an input capture channel, TOV0 has no effect. Reset clears the TOV0 bit.

1 = Channel x pin toggles on TIM counter overflow.
0 = Channel x pin does not toggle on TIM counter overflow.

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NOTE: *The state of TOV1 has no effect since there is no pin.*

When TOVx is set, a TIM counter overflow takes precedence over a channel x output compare if both occur at the same time.

Channel 1 should not be configured in input capture mode.

WARNING: ***The user must configure TIM channel 1 in a mode other than input capture. It is recommended that this procedure be part of the initialization of the system after reset.***

CHxMAX — Channel x Maximum Duty Cycle Bit

When the TOVx bit is at 1 and clear output on compare is selected, setting the CHxMAX bit forces the duty cycle of buffered and unbuffered PWM signals to 100 percent. As **Figure 11-9** shows, the CHxMAX bit takes effect in the cycle after it is set or cleared. The output stays at 100 percent duty cycle level until the cycle after CHxMAX is cleared.

NOTE: *The PWM 0 percent duty cycle is defined as output low all of the time. To generate the 0 percent duty cycle, select clear output on compare and then clear the TOVx bit (CHxMAX = 0). The PWM 100 percent duty cycle is defined as output high all of the time. To generate the 100 percent duty cycle, use the CHxMAX bit in the TSCx register.*

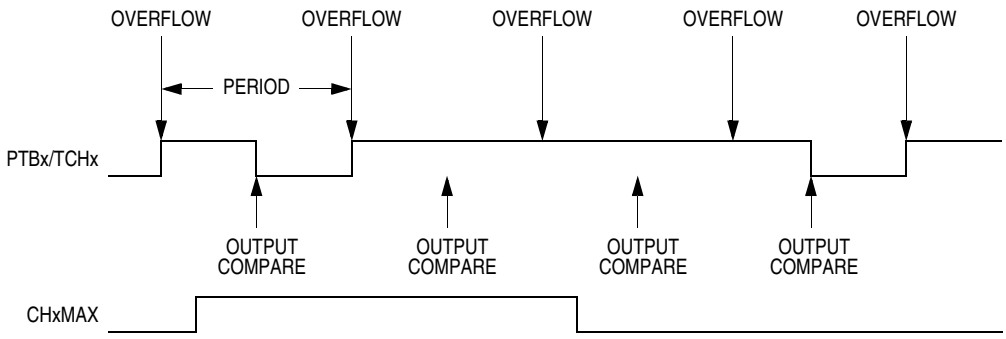

Figure 11-9. CHxMAX Latency

11.8.5 TIM Channel Registers

These read/write registers contain the captured TIM counter value of the input capture function or the output compare value of the output compare function. The state of the TIM channel registers after reset is unknown.

In input capture mode (MSxB:MSxA = 0:0), reading the high byte of the TIM channel x registers (TCHxH) inhibits input captures until the low byte (TCHxL) is read.

In output compare mode (MSxB:MSxA ≠ 0:0), writing to the high byte of the TIM channel x registers (TCHxH) inhibits output compares until the low byte (TCHxL) is written.

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Register Name and Address: TCH0H—$0026

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
Reset:	Indeterminate after reset							

Register Name and Address: TCH0L—$0027

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
Reset:	Indeterminate after reset							

Figure 11-10. TIM Channel 0 Registers (TCH0H and TCH0L)

Register Name and Address: TCH1H—$0029

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
Reset:	Indeterminate after reset							

Register Name and Address: TCH1L—$002A

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
Reset:	Indeterminate after reset							

Figure 11-11. TIM Channel 1 Registers (TCH1H and TCH1L)

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Section 12. PLL Tuned UHF Transmitter Module

12.1 Introduction

This section describes the integrated radio frequency (RF) module. This module integrates an ultra high frequency (UHF) transmitter offering these key features:

- Switchable frequency bands: 315, 434, and 868 MHz
- On/off keying (OOK) and frequency shift keying (FSK) modulation
- Adjustable output power range
- Fully integrated voltage-controlled oscillator (VCO)
- Supply voltage range: 1.9 to 3.7 V
- Very low standby current: 0.5 nA @ T_A = 25°C
- Low supply voltage shutdown
- Data clock output for microcontroller
- Low external component count

Architecture of the module is described in **Figure 12-1**.

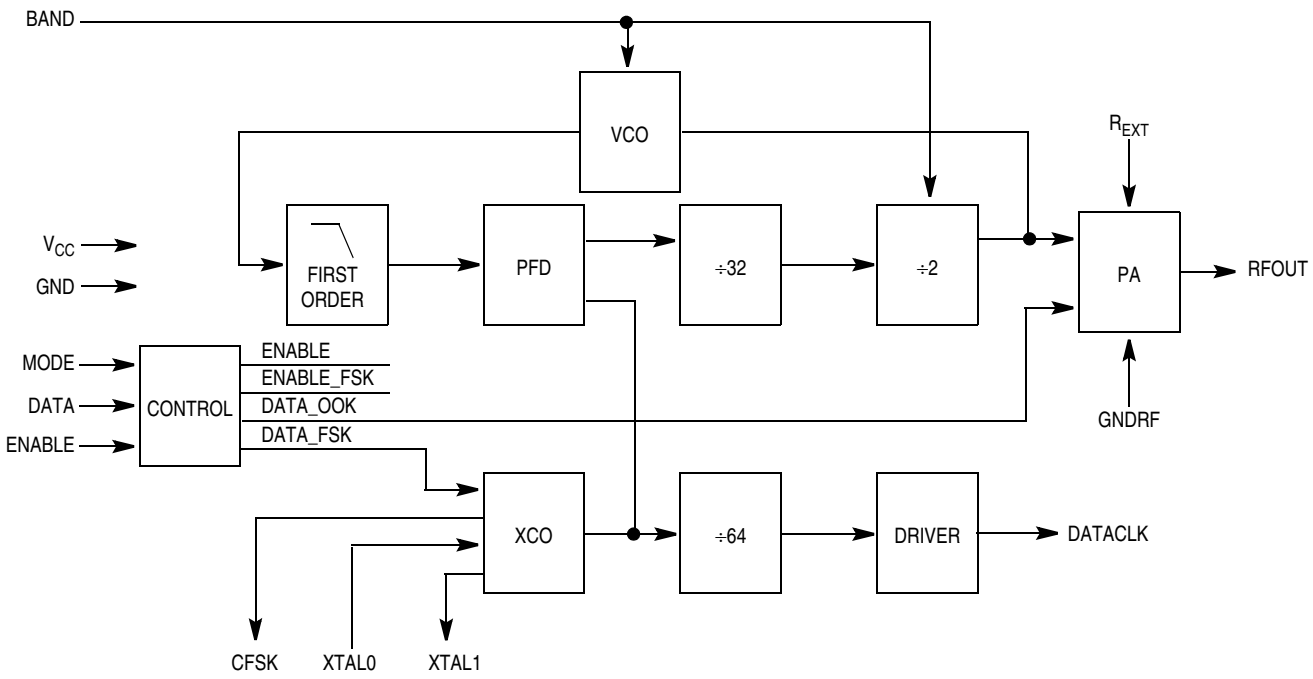

Figure 12-1. Simplified Integrated RF Module Block Diagram

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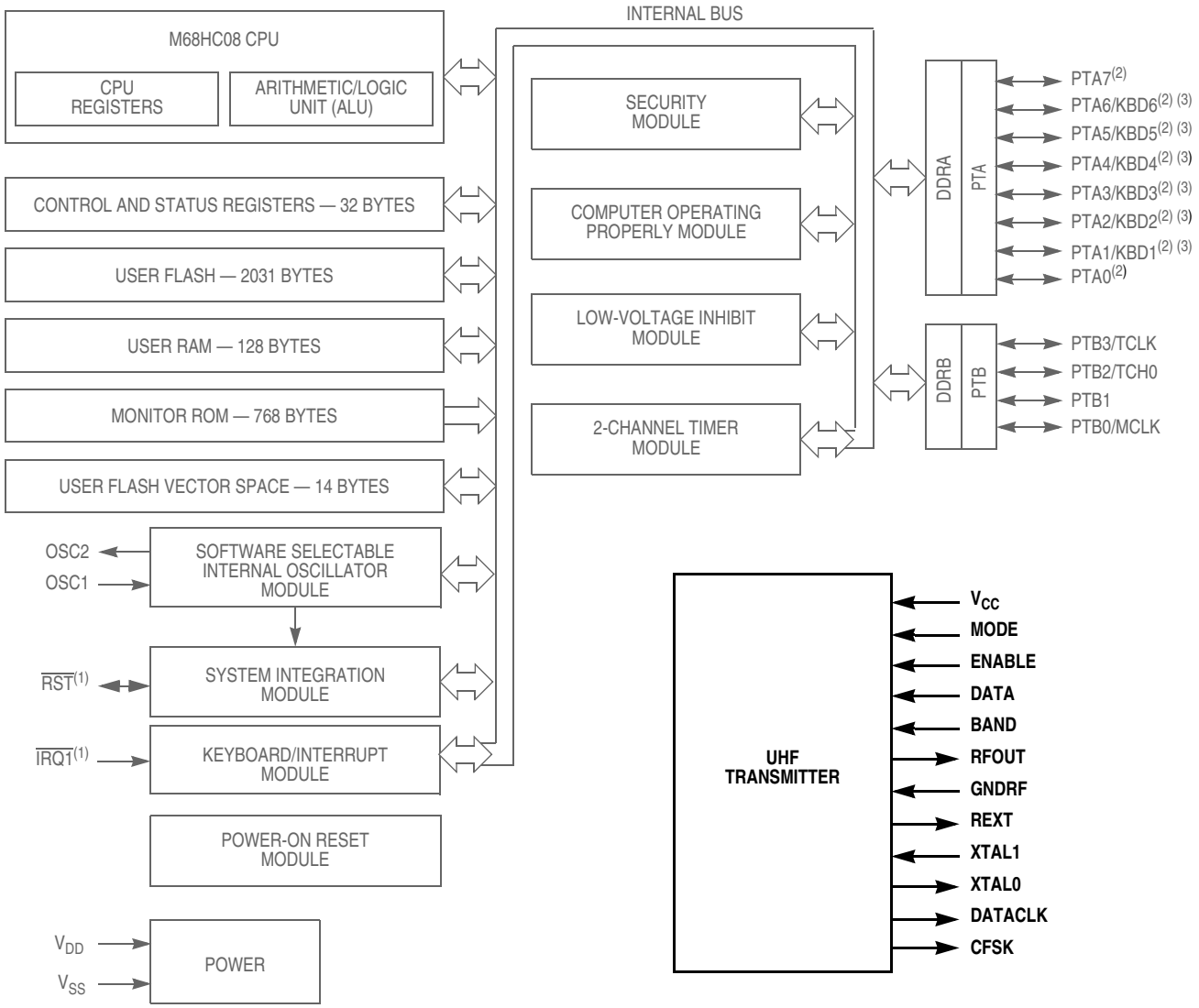

1. Pin contains integrated pullup resistor
2. High current sink pin
3. Pin contains software selectable pullup resistor

Figure 12-2. Block Diagram Highlighting UHF Transmitter Block and Pins

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12.2 Transmitter Functional Description

The transmitter is a phase-locked loop (PLL) tuned low-power UHF transmitter. The different modes of operation are controlled by the microcontroller through several digital input pins. The power supply voltage ranges from 1.9 V to 3.7 V allowing operation with a single lithium cell.

12.3 Phase-Lock Loop (PLL) and Local Oscillator

The VCO is a completely integrated relaxation oscillator. The phase frequency detector (PFD) and the loop filter are fully integrated. The exact output frequency is equal to:

$$f_{RFOUT} = f_{XTAL} \times \text{PLL divider ratio}$$

The frequency band of operation is selected through the BAND pin. **Table 12-1** provides details for each frequency band selection.

Table 12-1. Frequency Band Selection and Associated Divider Ratios

BAND Input Level	Frequency Band (MHz)	PLL Divider Ratio	Crystal Oscillator Frequency (MHz)
High	315	32	9.84
	434		13.56
Low	868	64	

An out-of-lock function is performed by monitoring the internal PFD output voltage. When it exceeds its limits, the RF output stage is disabled.

12.4 RF Output Stage

The output stage is a single-ended square wave switched current source. Harmonics will be present in the output current drive. Their radiated absolute level depends on the antenna characteristics and output power. Typical application demonstrates compliance to European Telecommunications Standards Institute (ETSI) standard. A resistor R_{EXT} connected to the REXT pin controls the output power allowing a tradeoff between radiated power and current consumption. The output voltage is internally clamped to:

$V_{CC} \pm 2\ V_{BE}$ (typically $V_{CC} \pm 1.5$ V @ $T_A = 25°C$)

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12.5 Modulation

If a low-logic level is applied on pin MODE, then the on/off keying (OOK) modulation is selected. This modulation is performed by switching on/off the RF output stage. The logic level applied on pin DATA controls the output stage state:

DATA = 0 → output stage off
DATA = 1 → output stage on

If a high-logic level is applied on pin MODE, then frequency shift keying (FSK) modulation is selected. This modulation is achieved by modulating the frequency of the reference oscillator. This frequency change is performed by switching the external crystal load capacitor. The logic level applied on pin DATA controls the internal switch connected to pin CFSK:

DATA = 0 → switch off
DATA = 1 → switch on

In case of **Figure 12-6**, where the two capacitors C6 and C9 are in series:

DATA = 0 leads to the high value of the carrier frequency
DATA = 1 leads to the low value of the carrier frequency

This crystal pulling solution implies that the RF output frequency deviation equals the crystal frequency deviation multipled by the PLL divider ratio (see **Table 12-1**).

12.6 Microcontroller Interfaces

Four digital input pins (ENABLE, DATA, BAND, and MODE) enable the circuit to be controlled by a microcontroller. It is recommended to configure the band frequency and the modulation type before enabling the circuit. In a typical application the input pins BAND and MODE are hardwired.

One digital output (DATACLK) provides the microcontroller a reference frequency for data clocking. This frequency is equal to the crystal oscillator frequency divided by 64 (see **Table 12-2**).

Table 12-2. DATACLK Frequency versus Crystal Oscillator Frequency

Crystal Oscillator Frequency (MHz)	DATACLK Frequency (kHz)
9.84	154
13.56	212

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12.7 State Machine

Figure 12-3 details the main state machine.

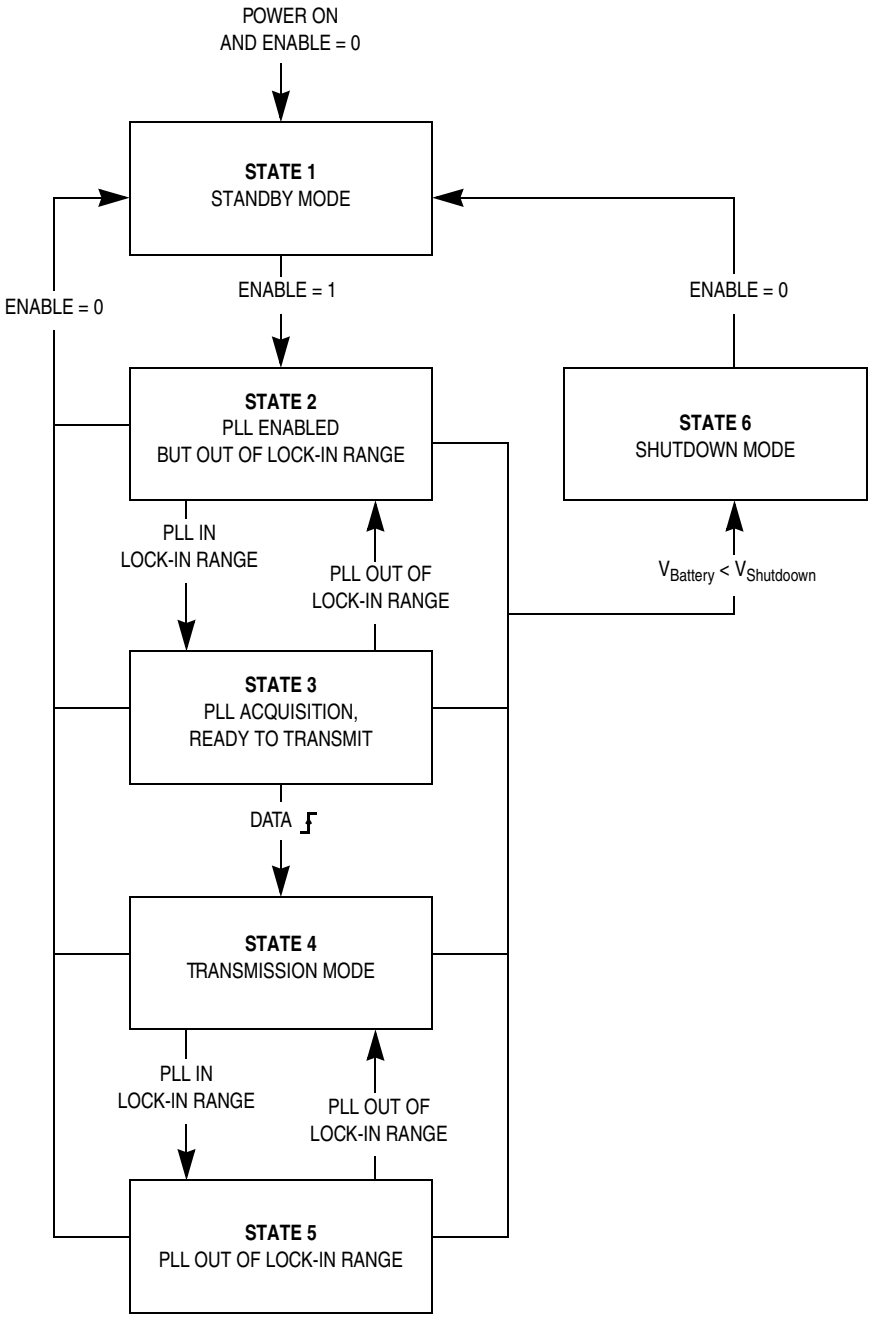

Figure 12-3. Main State Machine

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State 1

The circuit is in standby mode and draws only a leakage current from the power supply.

State 2

In this state, the PLL is enabled but out of the lock-in range. Therefore the RF output stage is switched off preventing any data transmission. Data clock is available on pin DATACLK. In normal operation, this state is transitional.

State 3

In this state, the PLL is within the lock-in range.

If $t < t_{PLL_Lock_In}$, then the PLL can still be in acquisition mode.

If $t \geq t_{PLL_Lock_In}$, then the PLL is locked.

The circuit is ready to transmit in band and is waiting for the first data (see **Figure 12-4**).

State 4

A rising edge on pin DATA starts the transmission. Data entered on pin DATA are output on pin RFOUT. The modulation is the one selected through the level applied on pin MODE.

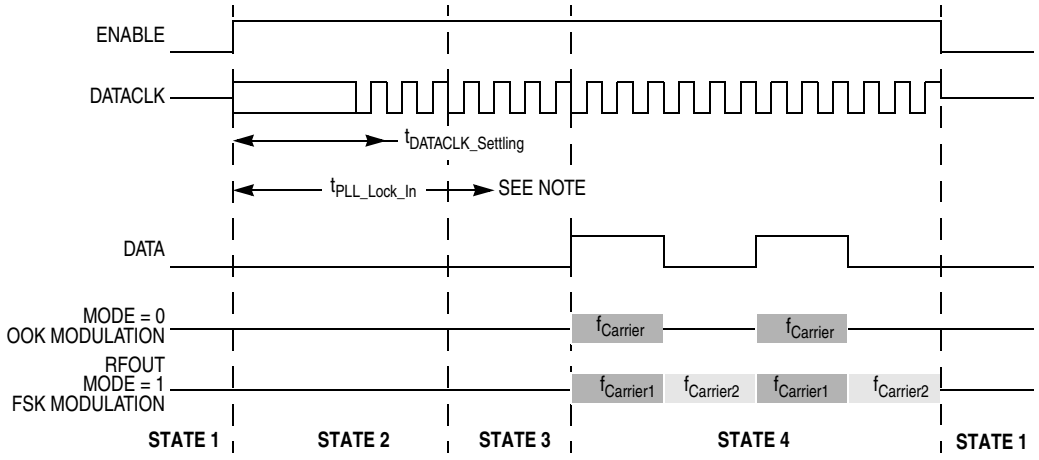
State 5

An out-of-lock condition has been detected. The RF output stage is switched off preventing any data transmission. Data clock is available on pin DATACLK.

State 6

When the supply voltage falls below the shutdown voltage threshold (V_{SDWN}) the whole circuit is switched off. Applying a low level on pin ENABLE is the only condition to get out of this state.

Figure 12-4 shows the waveforms of the main signals for a typical application cycle



Note: PLL locked, circuit ready to tramsmit in band.

Figure 12-4. Signals, Waveforms, and Timing Definitions

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12.8 Power Management

When the battery voltage falls below the shutdown voltage threshold (V_{SDWN}) the whole circuit is switched off.

NOTE: *After this shutdown, the circuit is latched until a low level is applied on pin ENABLE (see state 6 under **12.7 State Machine**).*

12.9 Data Clock

When the data clock starts, the high-to-low ratio may be uneven. Similarly the clock is switched off asynchronously so the last period length is not guaranteed.

12.10 Application Information

This subsection provides application information for the usage of the UHF transmitter module.

12.10.1 Application Schematics in OOK and FSK Modulation

Figure 12-5 and **Figure 12-6** show application schematics in OOK and FSK modulation for the 315-MHz and 434-MHz frequency bands. For 868-MHz band application, the input pin BAND must be wired to GND. See component description in **Table 12-4** and **Table 12-5**.

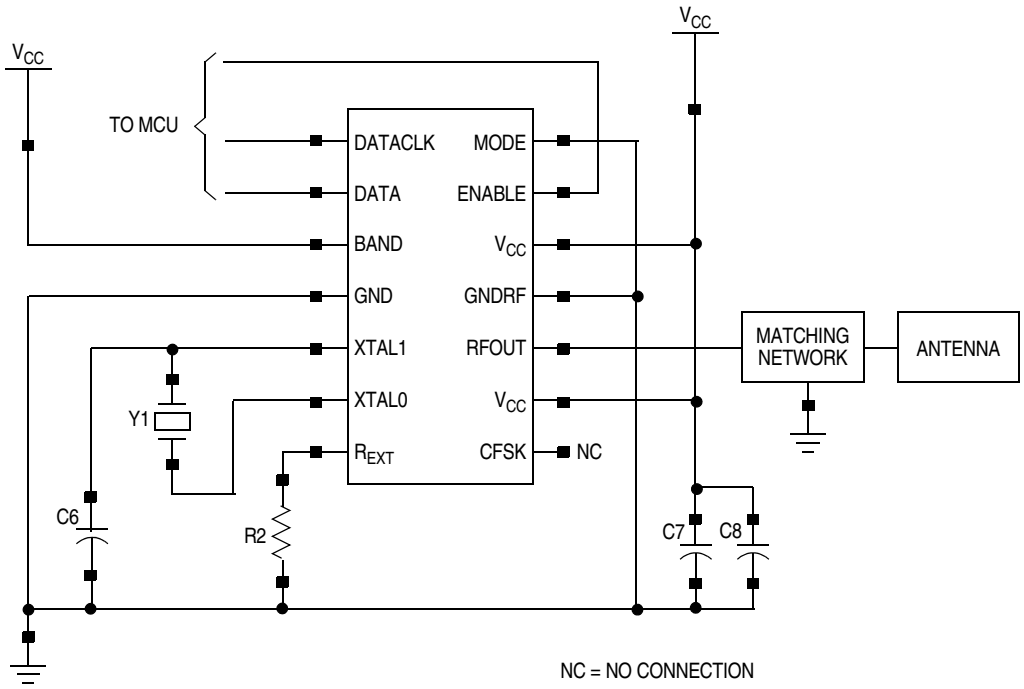

Figure 12-5. Application Schematic in OOK Modulation, 315-MHz and 434-MHz Frequency Bands

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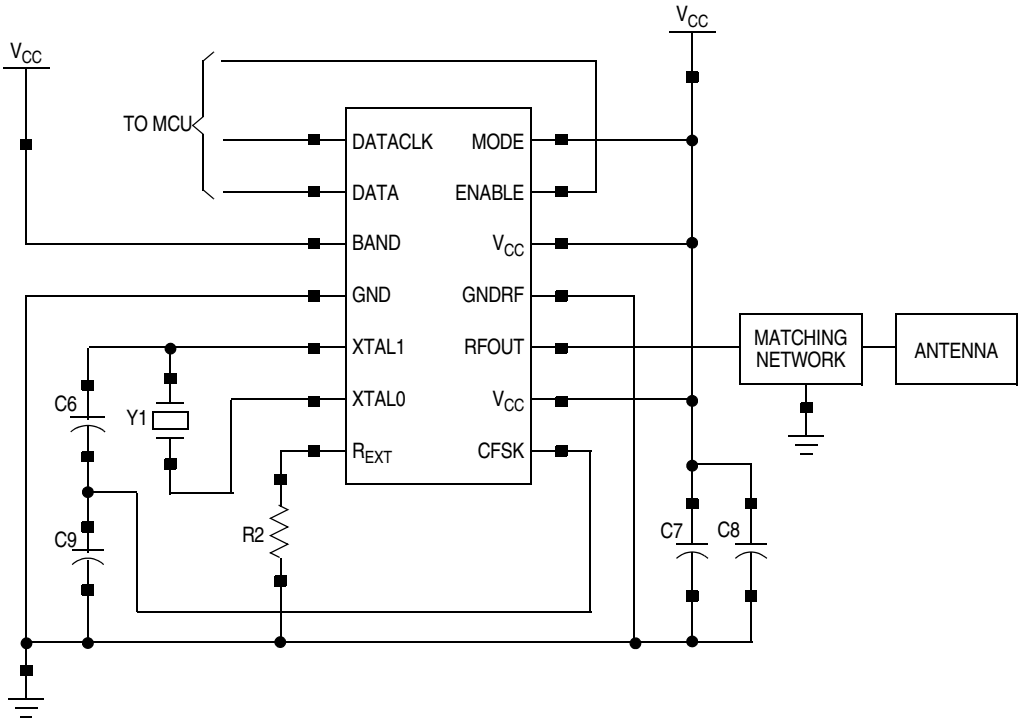

Figure 12-6. Application Schematic in FSK Modulation, 315-MHz and 434-MHz Frequency Bands

Table 12-3. Component Description

Component	Function	Value	Unit
Y1	Crystal	315-MHz band: 9.84, see **Table 12-5**	MHz
		434-MHz band: 13.56, see **Table 12-5**	MHz
		868-MHz band: 13.56, see **Table 12-5**	MHz
R2	RF output level setting resistor (R_{EXT})	12	kΩ
C6	Crystal load capacitor	OOK modulation: 18	pF
		FSK modulation: 22	pF
C7	Power supply decoupling capacitor	10	nF
C8		100	pF
C9	Crystal pulling capacitor for FSK modulation only	See **Table 12-5**	pF

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A example of crystal reference is: Tokyo Denpa TTS-3B 13568.750 kHz, see **Table 12-4**.

Table 12-4. Recommended Crystal Characteristics (SMD Ceramic Package)

Parameter	Value	Unit
Load capacitance	20	pF
Motional capacitance	6.7	fF
Static capacitance	2	pF
Loss resistance	40	W

Table 12-5. Crystal Pulling Capacitor Value versus Carrier Frequency Total Deviation

Carrier Frequency (MHz)	Carrier Frequency Total Deviation (kHz)	Capacitor Value (pF)
434	40	18
	70	10
	100	6.8
868	80	18
	140	10
	200	6.8

12.10.2 Complete Application Schematic

Figure 12-7 gives a complete application schematic using the Motorola MC68HC908RF2. OOK modulation is selected, $f_{Carrier}$ = 433.92 MHz.

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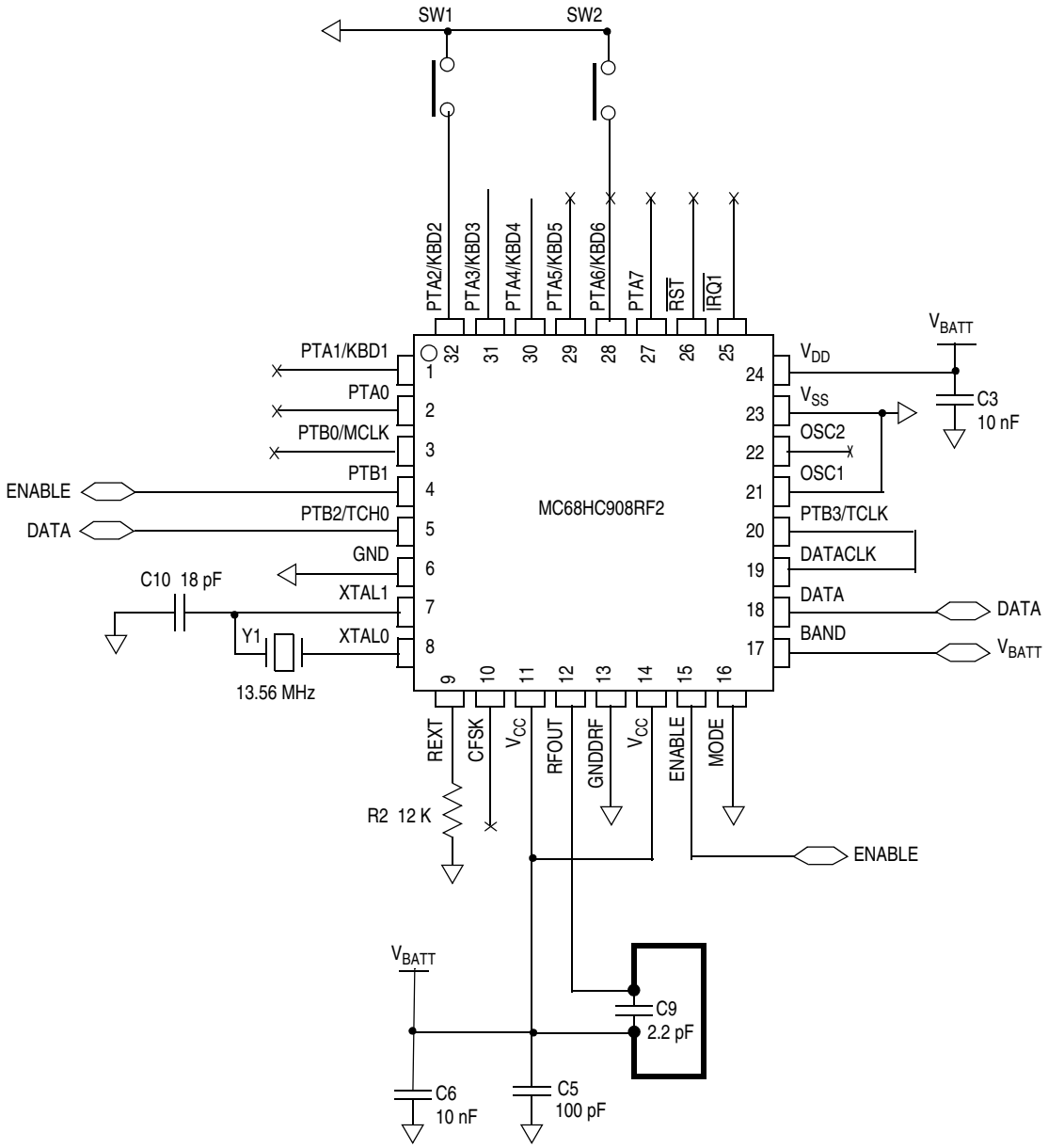

Figure 12-7. Complete Application Schematic in OOK Modulation, 434-MHz Frequency Band

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Section 13. Development Support

13.1 Introduction

This section describes the break module, the monitor module (MON), and the monitor mode entry methods.

13.2 Break Module (BRK)

The break module can generate a break interrupt that stops normal program flow at a defined address to enter a background program.

Features include:

- Accessible input/output (I/O) registers during break interrupts
- CPU-generated break interrupts
- Software-generated break interrupts
- COP disabling during break interrupts

13.2.1 Functional Description

When the internal address bus matches the value written in the break address registers, the break module issues a breakpoint signal to the CPU. The CPU then loads the instruction register with a software interrupt instruction (SWI) after completion of the current CPU instruction. The program counter vectors to $FFFC and $FFFD ($FEFC and $FEFD in monitor mode).

These events can cause a break interrupt to occur:

- A CPU-generated address (the address in the program counter) matches the contents of the break address registers.
- Software writes a 1 to the BRKA bit in the break status and control register.

When a CPU-generated address matches the contents of the break address registers, the break interrupt begins after the CPU completes its current instruction. A return-from-interrupt instruction (RTI) in the break routine ends the break interrupt and returns the MCU to normal operation. **Figure 13-1** shows the structure of the break module.

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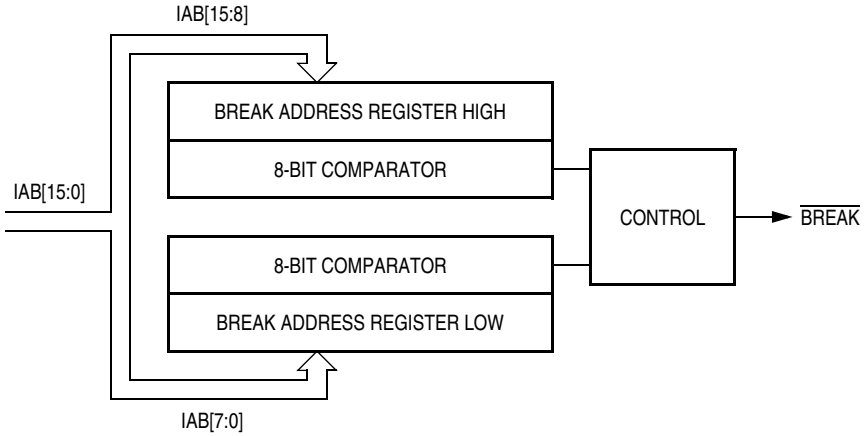

Figure 13-1. Break Module Block Diagram

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$FE0C	Break Address Register High (BRKH) See page 161.	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
		Reset:	0	0	0	0	0	0	0	0
$FE0D	Break Address Register Low (BRKL) See page 161.	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$FE0E	Break Status and Control Register (BSCR) See page 160.	Read:	BRKE	BRKA	0	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 13-2. I/O Register Summary

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13.2.1.1 Flag Protection During Break Interrupts

The system integration module (SIM) controls whether module status bits can be cleared during the break state. The BCFE bit in the SIM break flag control register (BFCR) enables software to clear status bits during the break state. (See **10.7.3 SIM Break Flag Control Register** and the **Break Interrupts** subsection for each module.)

13.2.1.2 CPU During Break Interrupts

The CPU starts a break interrupt by:

- Loading the instruction register with the SWI instruction
- Loading the program counter with $FFFC and $FFFD ($FEFC and $FEFD in monitor mode)

The break interrupt begins after completion of the CPU instruction in progress. If the break address register match occurs on the last cycle of a CPU instruction, the break interrupt begins immediately.

13.2.1.3 TIM During Break Interrupts

A break interrupt stops the timer counter.

13.2.1.4 COP During Break Interrupts

The COP is disabled during a break interrupt when V_{HI} is present on the $\overline{RST}$ pin.

13.2.2 Low-Power Modes

The WAIT and STOP instructions put the MCU in low power-consumption standby modes.

13.2.2.1 Wait Mode

If enabled, the break module is active in wait mode.

13.2.2.2 Stop Mode

The break module is inactive in stop mode. The STOP instruction does not affect break module register states.

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13.2.3 Break Module Registers

These registers control and monitor operation of the break module:

- Break status and control register, BSCR
- Break address register high, BRKH
- Break address register low, BRKL

13.2.3.1 Break Status and Control Register

The break status and control register (BSCR) contains break module enable and status bits.

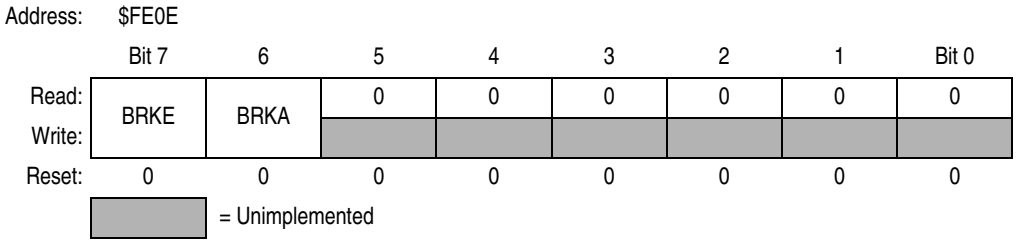

Figure 13-3. Break Status and Control Register (BSCR)

BRKE — Break Enable Bit

This read/write bit enables breaks on break address register matches. Clear BRKE by writing a 0 to bit 7. Reset clears the BRKE bit.

1 = Breaks enabled on 16-bit address match
0 = Breaks disabled on 16-bit address match

BRKA — Break Active Bit

This read/write status and control bit is set when a break address match occurs. Writing a 1 to BRKA generates a break interrupt. Clear BRKA by writing a 0 to it before exiting the break routine.

1 = Break address match
0 = No break address match

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13.2.3.2 Break Address Registers

The break address registers contain the high and low bytes of the desired breakpoint address. Reset clears the break address registers.

Register Name and Address: BRKH — $FE0C

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
Reset:	0	0	0	0	0	0	0	0

Register Name and Address: BRKL — $FE0D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
Reset:	0	0	0	0	0	0	0	0

Figure 13-4. Break Address Registers (BRKH and BRKL)

13.3 Monitor Module

This subsection describes the monitor read-only memory (MON). The MON allows complete testing of the MCU through a single-wire interface with a host computer.

Features include:

- Normal user-mode pin functionality
- One pin dedicated to serial communication between monitor ROM and host computer
- Standard mark/space non-return-to-zero (NRZ) communication with host computer
- 9600 baud communication with host computer when using a 9.8304-MHz crystal
- Execution of code in random-access memory (RAM) or FLASH
- FLASH security
- FLASH programming

13.3.1 Functional Description

Monitor ROM receives and executes commands from a host computer. **Figure 13-5** shows a sample circuit used to enter monitor mode and communicate with a host computer via a standard RS-232 interface.

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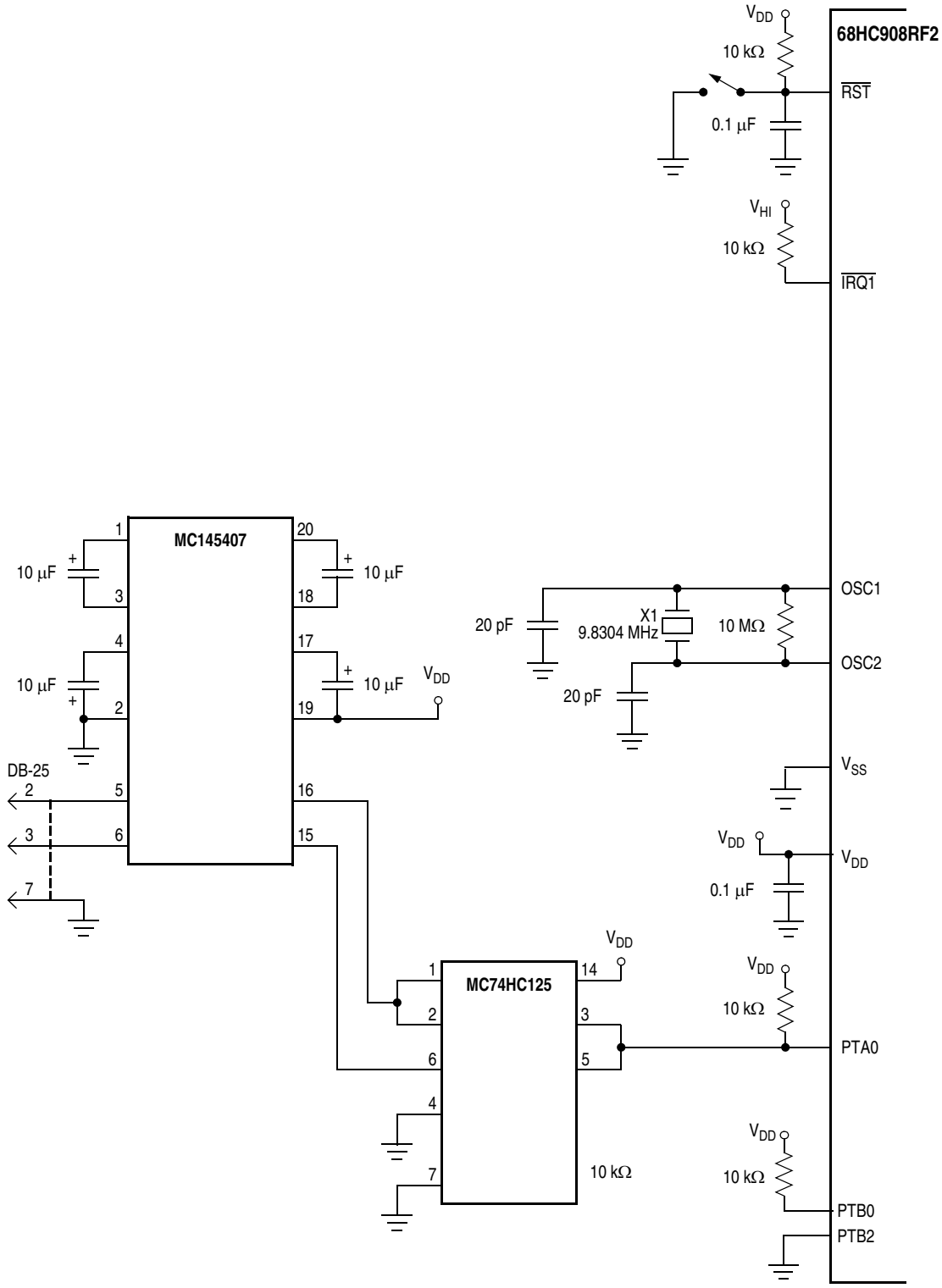

Figure 13-5. Monitor Mode Circuit

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While simple monitor commands can access any memory address, the MC68HC908RF2 has a FLASH security feature to prevent external viewing of the contents of FLASH. Proper procedures must be followed to verify FLASH content. Access to the FLASH is denied to unauthorized users of customer-specified software (see **13.3.2 Security**).

In monitor mode, the MCU can execute host-computer code in RAM while all MCU pins except PTA0 retain normal operating mode functions. All communication between the host computer and the MCU is through the PTA0 pin. A level-shifting and multiplexing interface is required between PTA0 and the host computer. PTA0 is used in a wired-OR configuration and requires a pullup resistor.

13.3.1.1 Monitor Mode Entry

Table 13-1 shows the pin conditions for entering monitor mode.

Table 13-1. Monitor Mode Entry

$\overline{\text{IRQ}}$ Pin	PTB0 Pin	PTB2 Pin	PTA0 Pin	CGMOUNT(1)	Bus Frequency
V_{TST}(2)	1	0	1	$\frac{\text{CGMXCLK}}{2}$	$\frac{\text{CGMOUT}}{2}$

1. If the high voltage (V_{TST}) is removed from the $\overline{\text{IRQ}}$ pin while in monitor mode, the clock select bit (CS) controls the source of CGMOUT.
2. For V_{TST}, see see **14.6 3.0-Volt DC Electrical Characteristics Excluding UHF Module** and **14.2 Absolute Maximum Ratings**.

Enter monitor mode by either:

- Executing a software interrupt instruction (SWI), or
- Applying a logic 0 and then a logic 1 to the $\overline{\text{RST}}$ pin

NOTE: *Upon entering monitor mode, an interrupt stack frame plus a stacked H register will leave the stack pointer at address $00F9.*

Once out of reset, the MCU waits for the host to send eight security bytes (see **13.3.2 Security**). After the security bytes, the MCU sends a break signal (10 consecutive logic 0s) to the host computer, indicating that it is ready to receive a command.

Monitor mode uses alternate vectors for reset, SWI, and break interrupt. The alternate vectors are in the $FE page instead of the $FF page and allow code execution from the internal monitor firmware instead of user code. The COP module is disabled in monitor mode as long as V_{HI} (see **Section 14. Electrical Specifications**) is applied to either the $\overline{\text{IRQ1}}$ pin or the $\overline{\text{RST}}$ pin. (See **Section 10. System Integration Module (SIM)** for more information on modes of operation.) The ICG module is bypassed in monitor mode as long as V_{HI} is applied to the $\overline{\text{IRQ1}}$ pin. $\overline{\text{RST}}$ does not affect the ICG.

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Table 13-2 is a summary of the differences between user mode and monitor mode.

Table 13-2. Mode Differences

Modes	Functions						
	COP	Reset Vector High	Reset Vector Low	Break Vector High	Break Vector Low	SWI Vector High	SWI Vector Low
User	Enabled	$FFFE	$FFFF	$FFFC	$FFFD	$FFFC	$FFFD
Monitor	Disabled(1)	$FEFE	$FEFF	$FEFC	$FEFD	$FEFC	$FEFD

1. If the high voltage (V_{HI}) is removed from the $\overline{IRQ1}$ pin while in monitor mode, the SIM asserts its COP enable output. The COP is a mask option enabled or disabled by the COPD bit in the configuration register. See **14.6 3.0-Volt DC Electrical Characteristics Excluding UHF Module**.

13.3.1.2 Data Format

Communication with the monitor ROM is in standard non-return-to-zero (NRZ) mark/space data format. (See **Figure 13-6** and **Figure 13-7**.)

The data transmit and receive rate is determined by the crystal. Transmit and receive baud rates must be identical.

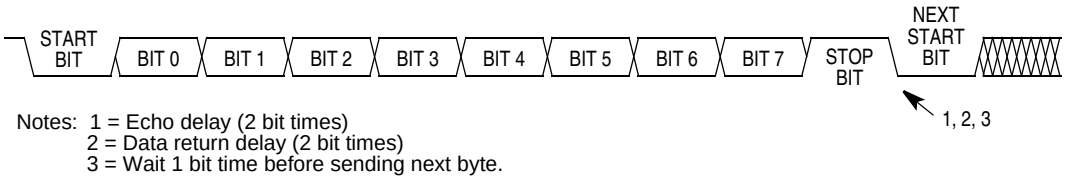

Figure 13-6. Monitor Data Format

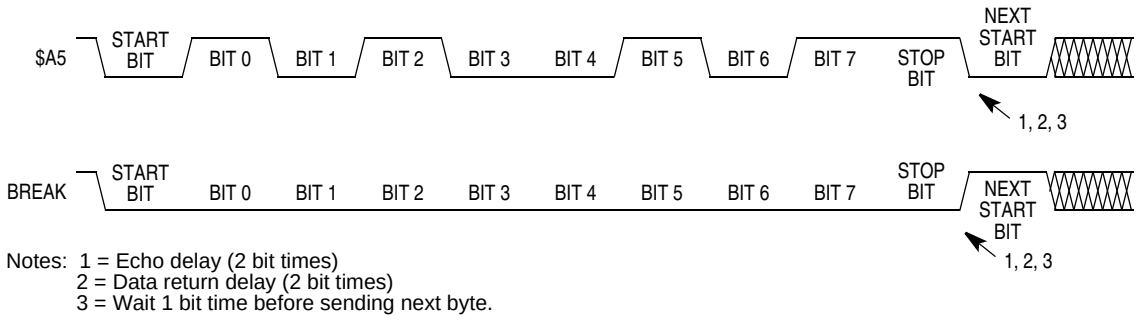

Figure 13-7. Sample Monitor Waveforms

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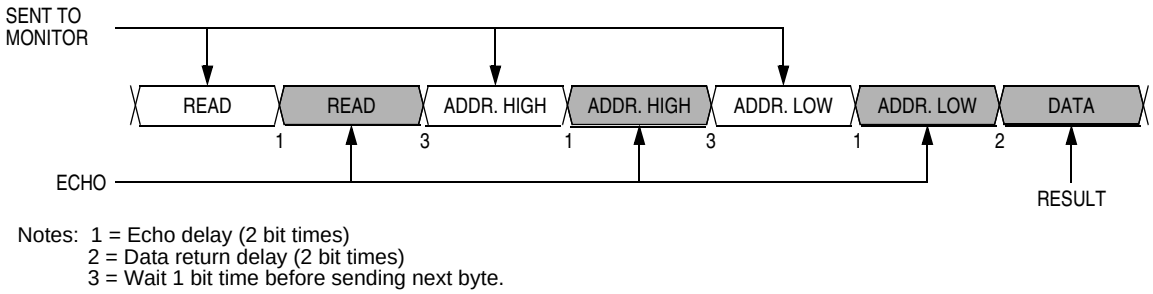
13.3.1.3 Echoing

As shown in **Figure 13-8**, the monitor ROM immediately echoes each received byte back to the PTA0 pin for error checking.

Any result of a command appears after the echo of the last byte of the command.



Notes: 1 = Echo delay (2 bit times)
2 = Data return delay (2 bit times)
3 = Wait 1 bit time before sending next byte.

Figure 13-8. Read Transaction

13.3.1.4 Break Signal

A start bit followed by nine low bits is a break signal. (See **Figure 13-9**.) When the monitor receives a break signal, it drives the PTA0 pin high for the duration of two bits before echoing the break signal.

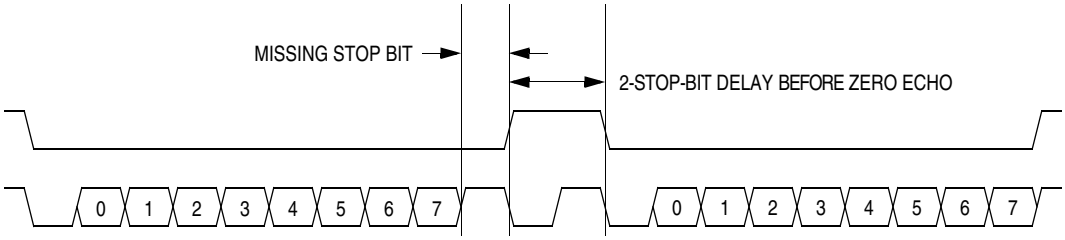


Figure 13-9. Break Transaction

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13.3.1.5 Commands

The monitor ROM firmware uses these commands:

- READ (read memory)
- WRITE (write memory)
- IREAD (indexed read)
- IWRITE (indexed write)
- READSP (read stack pointer)
- RUN (run user program)

The monitor ROM firmware echoes each received byte back to the PTA0 pin for error checking. An 11-bit delay at the end of each command allows the host to send a break character to cancel the command. A delay of two bit times occurs before each echo and before READ, IREAD, or READSP data is returned. The data returned by a read command appears after the echo of the last byte of the command.

NOTE: *Wait one bit time after each echo before sending the next byte.*

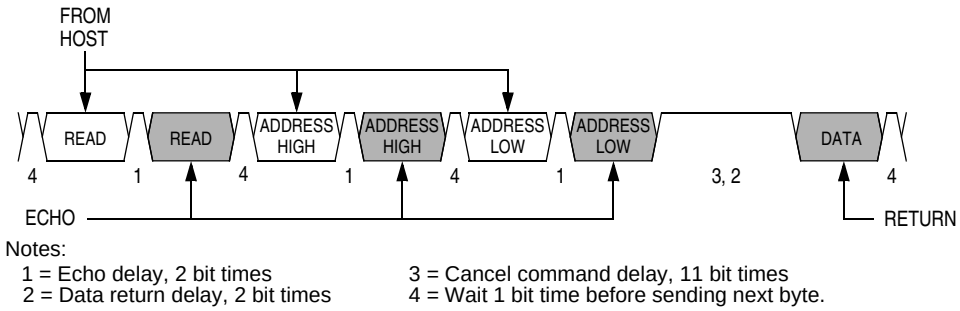

Figure 13-10. Read Transaction

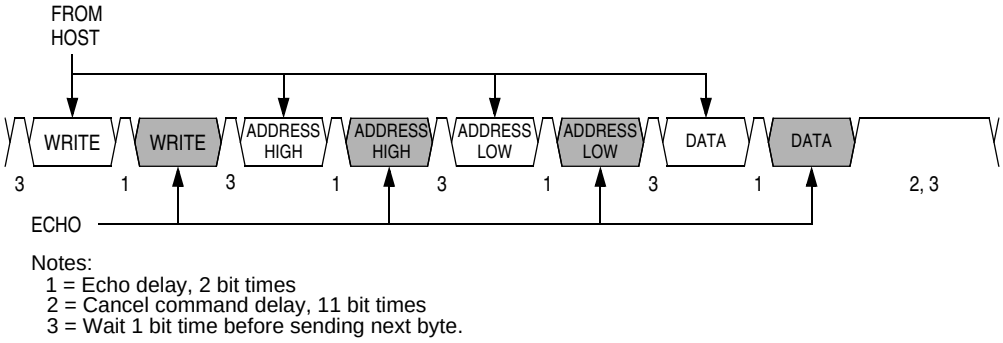

Figure 13-11. Write Transaction

A brief description of each monitor mode command is given in **Table 13-3** through **Table 13-8**.

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Table 13-3. READ (Read Memory) Command

Description	Read byte from memory
Operand	2-byte address in high-byte:low-byte order
Data Returned	Returns contents of specified address
Opcode	$4A

Command Sequence

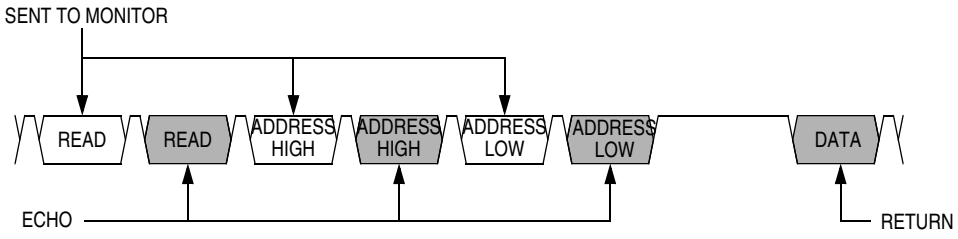

Table 13-4. WRITE (Write Memory) Command

Description	Write byte to memory
Operand	2-byte address in high-byte:low-byte order; low byte followed by data byte
Data Returned	None
Opcode	$49

Command Sequence

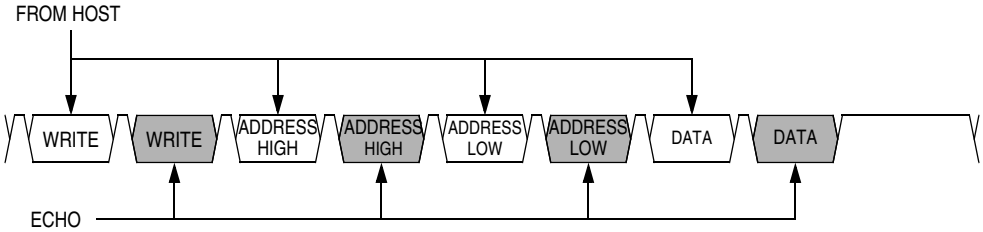

Table 13-5. IREAD (Indexed Read) Command

Description	Read next 2 bytes in memory from last address accessed
Operand	2-byte address in high byte:low byte order
Data Returned	Returns contents of next two addresses
Opcode	$1A

Command Sequence

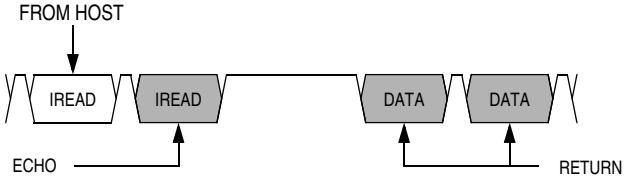

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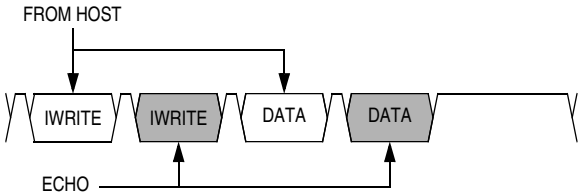
Table 13-6. IWRITE (Indexed Write) Command

Description	Write to last address accessed + 1
Operand	Single data byte
Data Returned	None
Opcode	$19
Command Sequence	



A sequence of IREAD or IWRITE commands can access a block of memory sequentially over the full 64-Kbyte memory map.

Table 13-7. READSP (Read Stack Pointer) Command

Description	Reads stack pointer
Operand	None
Data Returned	Returns incremented stack pointer value (SP + 1) in high-byte:low-byte order
Opcode	$0C
Command Sequence	

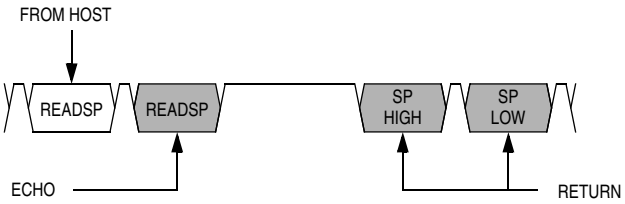
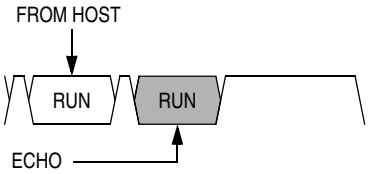


Table 13-8. RUN (Run User Program) Command

Description	Executes PULH and RTI instructions
Operand	None
Data Returned	None
Opcode	$28
Command Sequence	



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The MCU executes the SWI and PSHH instructions when it enters monitor mode. The RUN command tells the MCU to execute the PULH and RTI instructions. Before sending the RUN command, the host can modify the stacked CPU registers to prepare to run the host program. The READSP command returns the incremented stack pointer value, SP + 1. The high and low bytes of the program counter are at addresses SP + 5 and SP + 6.

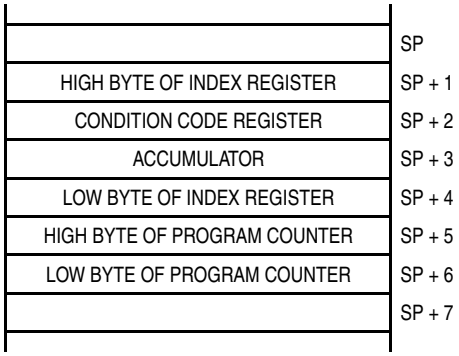

Figure 13-12. Stack Pointer at Monitor Mode Entry

13.3.1.6 Baud Rate

With a 9.8304-MHz crystal, data is transferred between the monitor and host at 9600 baud. If a 14.7456-MHz crystal is used, the monitor baud rate is 14400.

NOTE: *While in monitor mode with V_{HI} applied to $\overline{IRQ1}$, the MCU bus clock is always driven from the external clock.*

13.3.2 Security

A security feature discourages unauthorized reading of FLASH locations while in monitor mode. The host can bypass the security feature at monitor mode entry by sending eight consecutive security bytes that match the bytes at locations $FFF6–$FFFD. Locations $FFF6–$FFFD contain user-defined data.

NOTE: *Do not leave locations $FFF6–$FFFD blank. For security reasons, program locations $FFF6–$FFFD even if they are not used for vectors. If FLASH is unprogrammed, the eight security byte values to be sent are $00, the unprogrammed state of the FLASH.*

During monitor mode entry, the MCU waits after the power-on reset for the host to send the eight security bytes on pin PA0.

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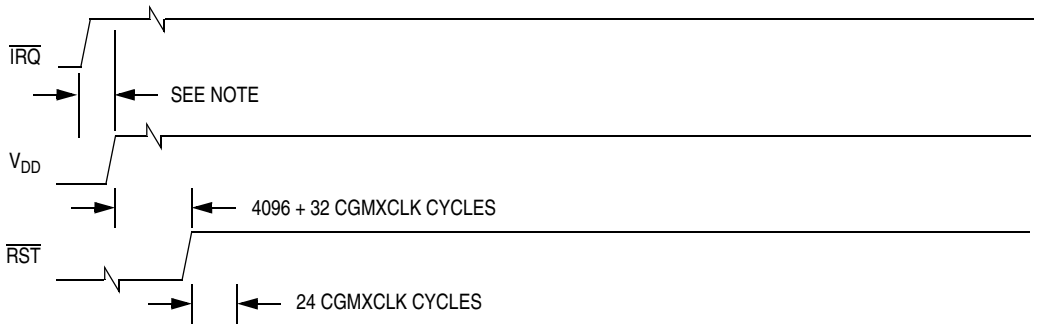
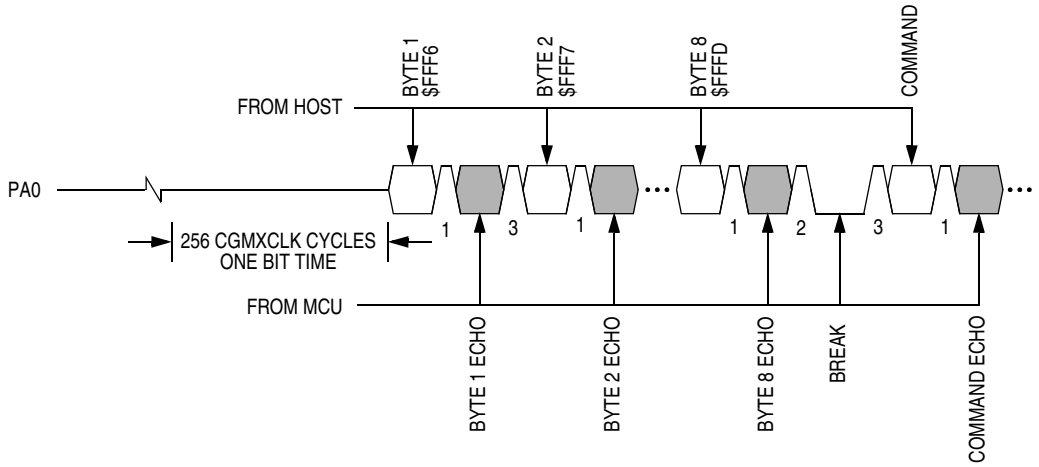


Note: Any delay between rising $\overline{IRQ}$ and rising V_{DD} will guarantee that the MCU bus is driven by the external clock.



Notes: 1 = Echo delay (2 bit times)
2 = Data return delay (2 bit times)
3 = Wait 1 bit time before sending next byte.

Figure 13-13. Monitor Mode Entry Timing

If the received bytes match those at locations $FFF6–$FFFD, the host bypasses the security feature and can read all FLASH locations and execute code from FLASH. Security remains bypassed until a power-on reset occurs. After the host bypasses security, any reset other than a power-on reset requires the host to send another eight bytes, but security remains bypassed regardless of the data that the host sends.

If the received bytes do not match the data at locations $FFF6–$FFFD, the host fails to bypass the security feature. The MCU remains in monitor mode, but reading FLASH locations returns undefined data, and trying to execute code from FLASH causes an illegal address reset. After the host fails to bypass security, any reset other than a power-on reset causes an endless loop of illegal address resets.

After receiving the eight security bytes from the host, the MCU transmits a break character signalling that it is ready to receive a command.

NOTE: *The MCU does not transmit a break character until after the host sends the eight security bytes.*

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Section 14. Electrical Specifications

14.1 Introduction

This section contains electrical and timing specifications.

14.2 Absolute Maximum Ratings

Maximum ratings are the extreme limits to which the MCU can be exposed without permanently damaging it.

NOTE: *This device is not guaranteed to operate properly at the maximum ratings. Refer to **14.5 1.8-Volt to 3.3-Volt DC Electrical Characteristics Excluding UHF Module**, **14.6 3.0-Volt DC Electrical Characteristics Excluding UHF Module**, **14.7 2.0-Volt DC Electrical Characteristics Excluding UHF Module**, and **14.8.1 UHF Module Electrical Characteristics** for guaranteed operating conditions.*

Characteristic(1)	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +3.6	V
Input voltage	V_{In}	V_{SS} –0.3 to V_{DD} +0.3	V
ESD HBM voltage capability on each pin(2)	—	± 2000	V
ESD MM voltage capability on each pin(3)	—	± 150	V
Maximum current per pin excluding V_{DD}, V_{SS}, P_{TA7}–P_{TA0}, and UHF module pins	I	± 15	mA
Maximum current for pins PTA7–PTA0	I_{PTA7}–I_{PTA0}	± 25	mA
Maximum current out of V_{SS}	I_{MVSS}	100	mA
Maximum current into V_{DD}	I_{MVDD}	100	mA
Storage temperature	T_{STG}	–55 to +150	°C

1. Voltages referenced to V_{SS}.
2. Human Body Model, AEC-Q100-002 Rev. C
3. Machine Model, AEC-Q100-003 Rev. D

NOTE: *This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. For proper operation, it is recommended that V_{In} and V_{Out} be constrained to the range $V_{SS} \le (V_{In}$ or $V_{Out}) \le V_{DD}$. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (for example, either V_{SS} or V_{DD}).*

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14.3 Functional Operating Range

Characteristic	Symbol	Min	Max	Unit	Temp. Code
Operating temperature range(1)	T_A	–40 –40	85 125	°C	C M
Operating voltage range	V_{DD}	1.8	3.6	V	–

1. Extended temperature range to be determined

14.4 Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance LQFP (32 pin)	θ_{JA}	TBD	°C/W
I/O pin power dissipation	$P_{I/O}$	User determined	W
Power dissipation(1)	P_D	$P_D = (I_{DD} \times V_{DD}) + P_{I/O} = K/(T_J + 273°C)$	W
Constant(2)	K	$P_D \times (T_A + 273°C) + P_D^2 \times \theta_{JA}$	W/°C
Average junction temperature	T_J	$T_A + (P_D \times \theta_{JA})$	°C
Maximum junction temperature	T_{JM}	100	°C

1. Power dissipation is a function of temperature.
2. K is a constant unique to the device. K can be determined for a known T_A and measured P_D. With this value of K, P_D and T_J can be determined for any value of T_A.

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14.5 1.8-Volt to 3.3-Volt DC Electrical Characteristics Excluding UHF Module

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output high voltage (I_{Load} = –1.2 mA) (I_{Load} = –2.0 mA)	V_{OH}	 V_{DD} –0.3 V_{DD} –1.0	 — —	 — —	V
Output low voltage (I_{Load} = 1.2 mA) (I_{Load} = 3.0 mA) (I_{Load} = 3.0 mA) PTA7–PTA0 only	V_{OL}	 — — —	 — — —	 0.3 1.0 0.3	V
Input high voltage, all ports, $\overline{IRQ1}$, OSC1	V_{IH}	0.7 x V_{DD}	—	V_{DD} + 0.3	V
Input low voltage, all ports, $\overline{IRQ1}$, OSC1	V_{IL}	V_{SS}	—	0.3 x V_{DD}	V
V_{DD} supply current Run[3] (f_{op}= 2.0 MHz) Wait[4] (f_{op}= 2.0 MHz) Stop[5] 25°C –40°C to 85°C –40°C to 125°C 25°C with LVI enabled –40°C to 85°C with LVI enabled	I_{DD}	 — — — — — — —	 — — 10 — 800 50 —	 4.3 1.2 — 100 1100 — 350	 mA mA nA nA nA µA µA
I/O ports high-impedance leakage current[6]	I_{IL}	—	—	± 1	µA
Input current	I_{In}	—	—	± 1	µA
Capacitance Ports (as input or output)	C_{Out} C_{In}	— —	— —	12 8	pF
POR re-arm voltage[7]	V_{POR}	0	—	200	mV
POR reset voltage[8]	V_{POR}	0	700	800	mV
POR rise time ramp rate[9]	R_{POR}	0.02	—	—	V/ms
Monitor mode entry voltage	V_{HI}	V_{DD} + 2.5	—	8	V
Pullup resistor, PTA6–PTA1, $\overline{IRQ}$	R_{PU}	50	80	120	kΩ

1. Parameters are design targets at V_{DD} = 1.8 V to 3.3 V, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted
2. Typical values reflect average measurements at midpoint of voltage range, 25°C only.
3. Run (operating) I_{DD} measured using internal clock generator module (f_{op}= 2.0 MHz). V_{DD} = 3.3 Vdc. All inputs 0.2 V from rail. No dc loads. Less than 100 pF on all outputs. All ports configured as inputs. C_L = 20 pF. OSC2 capacitance linearly affects run I_{DD}. Measured with all modules enabled.
4. Wait I_{DD} measured using internal clock generator module, f_{op} = 2.0 MHz. All inputs 0.2 V from rail; no dc loads; less than 100 pF on all outputs. C_L = 20 pF. OSC2 capacitance linearly affects wait I_{DD}. All ports configured as inputs.
5. Stop I_{DD} measured with no port pins sourcing current, all modules disabled except as noted.
6. Pullups and pulldowns are disabled.
7. Maximum is highest voltage that POR is guaranteed.
8. Maximum is highest voltage that POR is possible.
9. If minimum V_{DD} is not reached before the internal POR reset is released, $\overline{RST}$ must be driven low externally until minimum V_{DD} is reached.

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14.6 3.0-Volt DC Electrical Characteristics Excluding UHF Module

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output high voltage (I_{Load} = –2.0 mA) (I_{Load} = –8.0 mA)	V_{OH}	 V_{DD} –0.3 V_{DD} –1.0	 — —	 — —	V
Output low voltage (I_{Load} = 2.0 mA) (I_{Load} = 6.5 mA) (I_{Load} = 5.0 mA) PTA7–PTA0 only	V_{OL}	 — — —	 — — —	 0.3 1.0 0.3	V
Input high voltage, all ports, $\overline{IRQ}$, OSC1	V_{IH}	0.7 x V_{DD}	—	V_{DD} + 0.3	V
Input low voltage, all ports, $\overline{IRQ}$, OSC1	V_{IL}	V_{SS}	—	0.3 x V_{DD}	V
V_{DD} supply current Run[3] (f_{op}= 4.0 MHz) Wait[4] (f_{op}= 4.0 MHz) Stop[5] 25°C –40°C to 85°C –40°C to 125°C 25°C with LVI enabled –40°C to 85°C with LVI enabled	I_{DD}	 — — — — — — —	 — — 10 — 800 50 —	 8.6 1.2 — 100 1100 — 350	 mA mA nA nA nA µA µA
I/O ports high-impedance leakage current[6]	I_{IL}	—	—	± 1	µA
Input current	I_{In}	—	—	± 1	µA
Capacitance Ports (as input or output)	C_{Out} C_{In}	— —	— —	12 8	pF
POR re-arm voltage[7]	V_{POR}	0	—	200	mV
POR reset voltage[8]	V_{POR}	0	700	800	mV
POR rise time ramp rate[9]	R_{POR}	0.02	—	—	V/ms
Monitor mode entry voltage	V_{HI}	V_{DD}+ 2.5	—	8	V
Pullup resistor, PTA6–PTA1, $\overline{IRQ}$	R_{PU}	50	80	120	kΩ

1. Parameters are design targets at V_{DD} = 3.0 ± 10%, V_{SS} = 0 Vdc, T_A = T_L to T_H, unless otherwise noted
2. Typical values reflect average measurements at midpoint of voltage range, 25°C only.
3. Run (operating) I_{DD} measured using internal clock generator module (f_{op}= 4.0 MHz). V_{DD} = 3.3 Vdc. All inputs 0.2 V from rail. No dc loads. Less than 100 pF on all outputs. All ports configured as inputs. C_L = 20 pF. OSC2 capacitance linearly affects run I_{DD}. Measured with all modules enabled.
4. Wait I_{DD} measured using internal clock generator module, f_{op} = 4.0 MHz. All inputs 0.2 V from rail; no dc loads; less than 100 pF on all outputs. C_L = 20 pF. OSC2 capacitance linearly affects wait I_{DD}. All ports configured as inputs.
5. Stop I_{DD} measured with no port pins sourcing current, all modules disabled except as noted.
6. Pullups and pulldowns are disabled.
7. Maximum is highest voltage that POR is guaranteed.
8. Maximum is highest voltage that POR is possible.
9. If minimum V_{DD} is not reached before the internal POR reset is released, $\overline{RST}$ must be driven low externally until minimum V_{DD} is reached.

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14.7 2.0-Volt DC Electrical Characteristics Excluding UHF Module

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output high voltage (I_{Load} = –1.2 mA) (I_{Load} = –2.0 mA)	V_{OH}	 V_{DD} –0.3 V_{DD} –1.0	 — —	 — —	V
Output low voltage (I_{Load} = 1.2 mA) (I_{Load} = 3.0 mA) (I_{Load} = 3.0 mA) PTA7–PTA0 only	V_{OL}	 — — —	 — — —	 0.3 1.0 0.3	V
Input high voltage, all ports, $\overline{IRQ}$, OSC1	V_{IH}	0.7 x V_{DD}	—	V_{DD} + 0.3	V
Input low voltage, all ports, $\overline{IRQ}$, OSC1	V_{IL}	V_{SS}	—	0.3 x V_{DD}	V
V_{DD} supply current Run[3] (f_{op}= 2.0 MHz) Wait[4] (f_{op}= 2.0 MHz) Stop[5] 25°C –40 °C to 85°C –40°C to 125°C 25°C with LVI enabled –40°C to 85°C with LVI enabled	I_{DD}	 — — — — — — —	 — — 10 — 800 50 —	 2.5 850 — 100 1100 — 350	 mA µA nA nA nA µA µA
I/O ports high-impedance leakage current[6]	I_{IL}	—	—	± 1	µA
Input current	I_{In}	—	—	± 1	µA
Capacitance Ports (as input or output)	C_{Out} C_{In}	— —	— —	12 8	pF
POR re-arm voltage[7]	V_{POR}	0	—	200	mV
POR reset voltage[8]	V_{POR}	0	700	800	mV
POR rise time ramp rate[9]	R_{POR}	0.02	—	—	V/ms
Monitor mode entry voltage	V_{HI}	V_{DD}+ 2.5	—	8	V
Pullup resistor, PTA6–PTA1, $\overline{IRQ}$	R_{PU}	50	80	120	kΩ

1. Parameters are design targets at V_{DD} = 2.0 ± 10%, V_{SS} = 0 Vdc, T_A = T_L to T_H, unless otherwise noted
2. Typical values reflect average measurements at midpoint of voltage range, 25°C only.
3. Run (operating) I_{DD} measured using internal clock generator module (f_{op}= 2.0 MHz). V_{DD} = 2.0 Vdc. All inputs 0.2 V from rail. No dc loads. Less than 100 pF on all outputs. All ports configured as inputs. C_L = 20 pF. OSC2 capacitance linearly affects run I_{DD}. Measured with all modules enabled.
4. Wait I_{DD} measured using internal clock generator module, f_{op} = 2.0 MHz. All inputs 0.2 V from rail; no dc loads; less than 100 pF on all outputs. C_L = 20 pF. OSC2 capacitance linearly affects wait I_{DD}. All ports configured as inputs.
5. Stop I_{DD} measured with no port pins sourcing current, all modules disabled except as noted.
6. Pullups and pulldowns are disabled.
7. Maximum is highest voltage that POR is guaranteed.
8. Maximum is highest voltage that POR is possible.
9. If minimum V_{DD} is not reached before the internal POR reset is released, $\overline{RST}$ must be driven low externally until minimum V_{DD} is reached.

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14.8 UHF Transmitter Module

This subsection provides electrical specifications and timing definitions for the UHF transmitter module.

14.8.1 UHF Module Electrical Characteristics

Unless otherwise specified:

- V_{CC} = 3 V
- R_{EXT} = 12 kΩ
- Operating temperature range (T_A) = –40°C to 85°C
- RF output frequency: $f_{Carrier}$ = 433.92 MHz
- Reference frequency: $f_{Reference}$ =13.56 MHz
- OOK modulation selected
- Output load is 50 Ω resistor (see **Figure 14-4**)

Values refer to the circuit shown in the recommended application schematic (see **Figure 12-5. Application Schematic in OOK Modulation, 315-MHz and 434-MHz Frequency Bands**).

Typical values reflect average measurement at V_{CC} = 3 V, T_A = 25°C.

NOTE: *Electrical characteristics shown at 125°C are for information only. These values have not been tested.*

Parameter	Test Conditions and Comments	Min	Typ	Max	Unit
General Parameters					
Supply current in standby mode	$T_A \le 25°C$	—	0.1	5	nA
	T_A = 60°C	—	7	30	nA
	T_A = 85°C	—	40	100	nA
	T_A = 125°C	—	800	1700	nA
Supply current in transmission mode	315 and 434 MHz bands, continuous wave, $T_A \le 85°C$	—	11.6	13.5	mA
	315 and 434 MHz bands, DATA = 0, $–40°C \le T_A \le 125°C$	—	4.4	6.0	mA
	868 MHz band, DATA = 0, $–40°C \le T_A \le 125°C$	—	4.6	6.2	mA
	315 and 434 MHz bands, continuous wave, $–40°C \le T_A \le 125°C$	—	11.6	14.9	mA
	868 MHz band, continuous wave, $–40°C \le T_A \le 125°C$	—	11.8	15.1	mA

Table continued on next page

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Parameter	Test Conditions and Comments	Min	Typ	Max	Unit
Supply voltage		—	3	3.7	V
Shutdown voltage threshold	T_A = –40°C	—	2.04	2.11	V
	T_A = –20°C	—	1.99	2.06	V
	T_A = 25°C	—	1.86	1.95	V
	T_A = 60°C	—	1.76	1.84	V
	T_A = 85°C	—	1.68	1.78	V
	T_A = 125°C	—	1.56	1.67	V
RF Parameters (assuming a 50 Ω matching network connected to the D.U.T. output)					
R_{EXT} value		12	—	21	kΩ
Output power	315 and 434 MHz bands, with 50 Ω matching network	—	5	—	dBm
	868 MHz band, with 50 Ω matching network	—	1	—	dBm
	315 and 434 MHz bands, –40°C ≤ T_A ≤ 125°C	–3	0	3	dBm
	868 MHz band, –40°C ≤ T_A ≤ 125°C	–7	–3	0	dBm
Current and output power variation vs R_{EXT} value	314 and 434 MHz bands, with 50 Ω matching network	—	–0.35	—	dB/kΩ mA/kΩ
Harmonic 2 level	315 and 434 MHz bands, with 50 Ω matching network	—	–34	—	dBc
	868 MHz band, with 50 Ω matching network	—	–49	—	dBc
	315 and 434 MHz bands	—	–23	–17	dBc
	868 MHz band	—	–38	–27	dBc
Harmonic 3 level	315 and 434MHz bands, with 50 Ω matching network	—	–32	—	dBc
	868 MHz band, with 50 Ω matching network	—	–57	—	dBc
	315 and 434 MHz bands	—	–21	–15	dBc
	868 MHz band	—	–48	–39	dBc
Spurious level @ $f_{Carrier} \pm f_{DATACLK}$	315 and 434 MHz bands	—	–36	–24	dBc
	868 MHz band		–29	–17	dBc
Spurious level @ $f_{Carrier} \pm f_{Reference}$	315 MHz band	—	–37	–30	dBc
	434 MHz band	—	–44	–34	dBc
	868 MHz band	—	–37	–27	dBc
Spurious level @ $f_{Carrier}/2$	315 MHz bands	—	–62	–53	dBc
	434 MHz bands	—	–80	–60	dBc
	868 MHz band	—	–45	–39	dBc

Table concluded on next page

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Electrical Specifications

Parameter	Test Conditions and Comments	Min	Typ	Max	Unit
RF spectrum	434 MHz bands	See Figure 14-1, Figure 14-2, and Figure 14-3			—
Phase noise	315 and 434 MHz bands, ±175 kHz from $f_{Carrier}$	—	–75	–68	dBc/Hz
	868 MHz band, ±175 kHz from $f_{Carrier}$	—	–73	–66	dBc/Hz
PLL lock-in time, $t_{PLL_Lock_In}$	$f_{Carrier}$ within 30 kHz from the final value, crystal series resistor = 150 Ω	—	350	1500	µs
XTAL1 input capacitance		—	1	2	pF
Crystal resistance		—	40	200	Ω
Modulation depth		75	90	—	dBc
Data rate		—	—	10	kBd
Microcontroller Interfaces					
Input low voltage	Pins BAND, MODE, ENABLE, and DATA	0	—	0.3 x V_{CC}	V
Input high voltage		0.7 x V_{CC}	—	V_{CC}	V
Input hysteresis voltage		—	—	150	mV
Input current	Pins BAND, MODE, DATA @ high level	—	—	100	nA
ENABLE pulldown resistor		—	180	—	kΩ
DATACLK output low voltage	C_{Load} = 2 pF	0	—	0.25 x V_{CC}	V
DATACLK output high voltage		0.75 x V_{CC}	—	V_{CC}	V
DATACLK rising time	C_{Load} = 2 pF, measured from 20% to 80% of the voltage swing	—	250	500	ns
DATACLK falling time		—	150	400	ns
DATACLK settling time, $t_{DATACLK_Settling}$	45 < duty cycle $f_{DATACLK}$ < 55%	—	800	1800	µs

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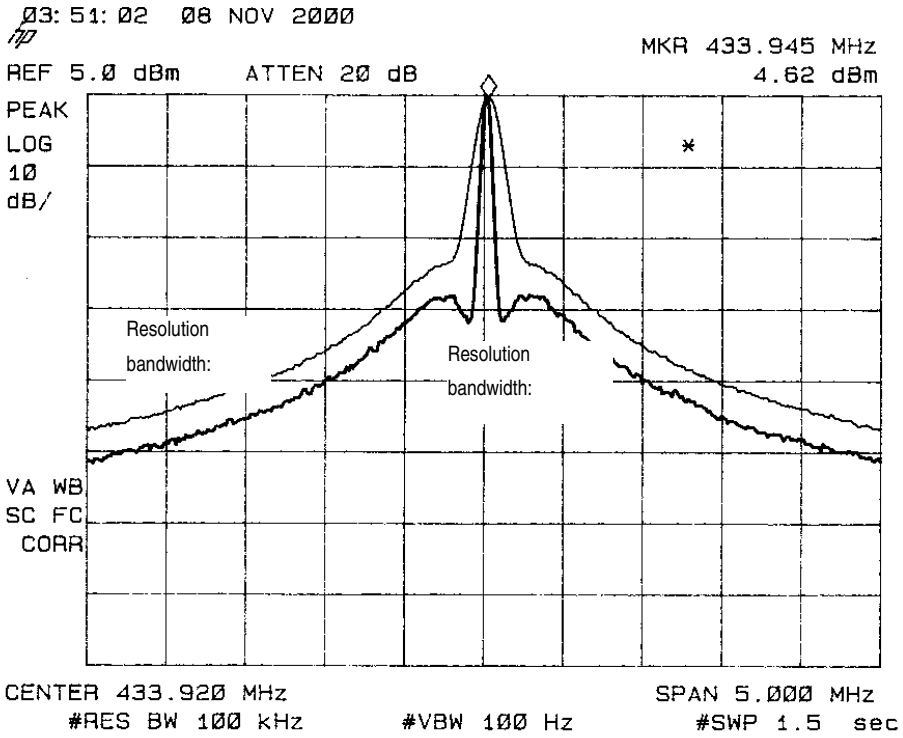

Figure 14-1. RF Spectrum at 434-MHz Frequency Band Displayed with a 5-MHz Span

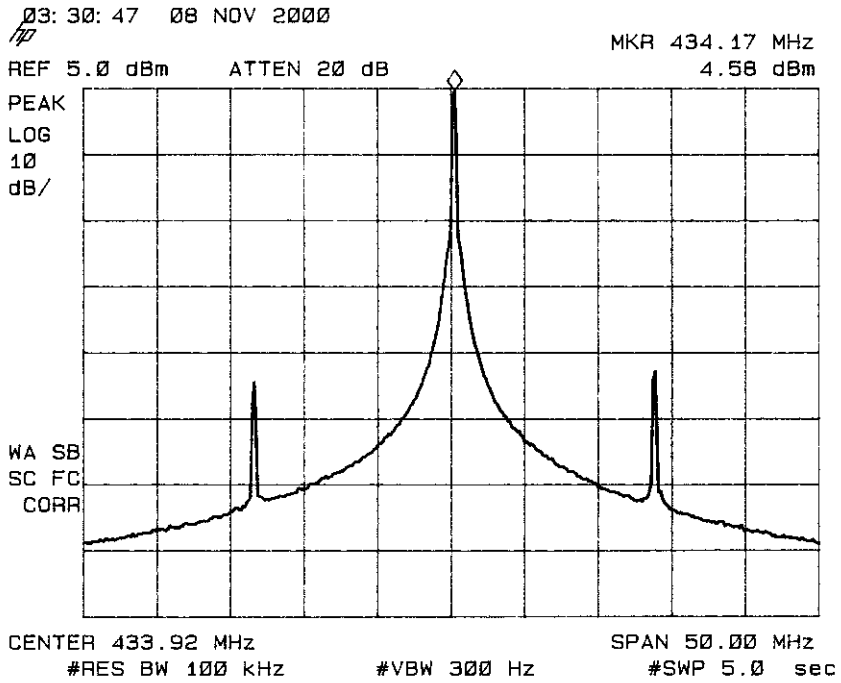

Figure 14-2. RF Spectrum at 434-MHz Frequency Band Displayed with a 50-MHz Span

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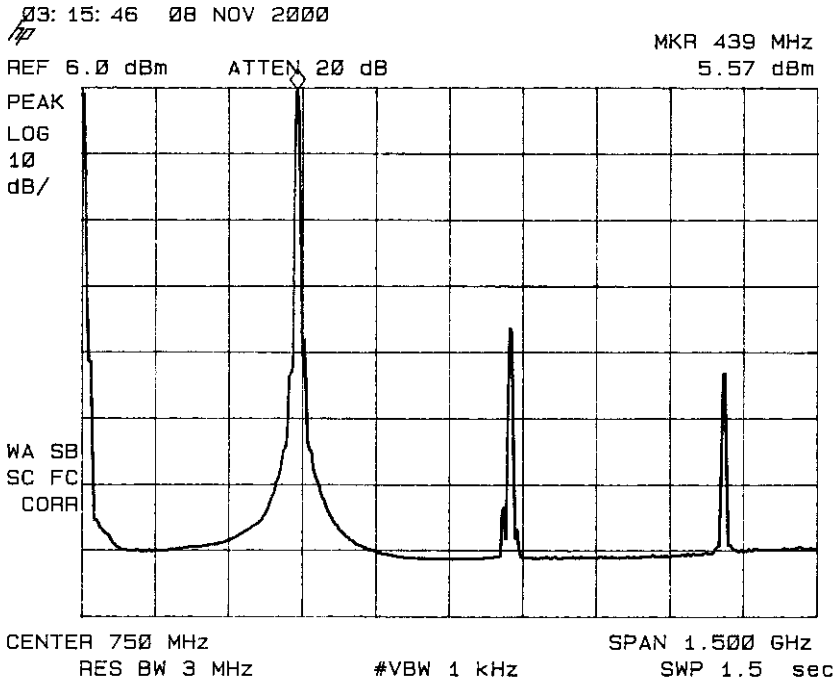

Figure 14-3. RF Spectrum at 434-MHz Frequency Band Displayed with a 1.5-GHz Span

14.8.2 UHF Module Output Power Measurement

The RF output levels given in the **14.8.1 UHF Module Electrical Characteristics** are measured whith a 50-Ω load directly connected to the pin RFOUT as shown in figure **Figure 14-4**. This wideband coupling method gives results independant of the application.

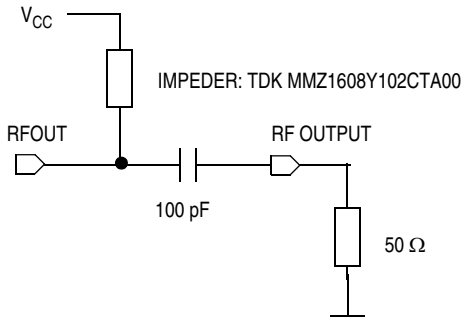

Figure 14-4. Output Power Measurement Configurations

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The configuration shown in **Figure 14-5(a)** provides a better efficiency in terms of output power and harmonics rejection. Schematic in **Figure 14-5(b)** gives the equivalent circuit of the pin RFOUT and impeder as well as the matching network components for 434-MHz frequency band.

NOTE: *Note that the impeder is moved to the load side to decrease its influence (similar to dc bias through the antenna).*

Figure 14-6 gives the output power versus the R_{EXT} resistor value, in both cases with 50-Ω load and with matching network.

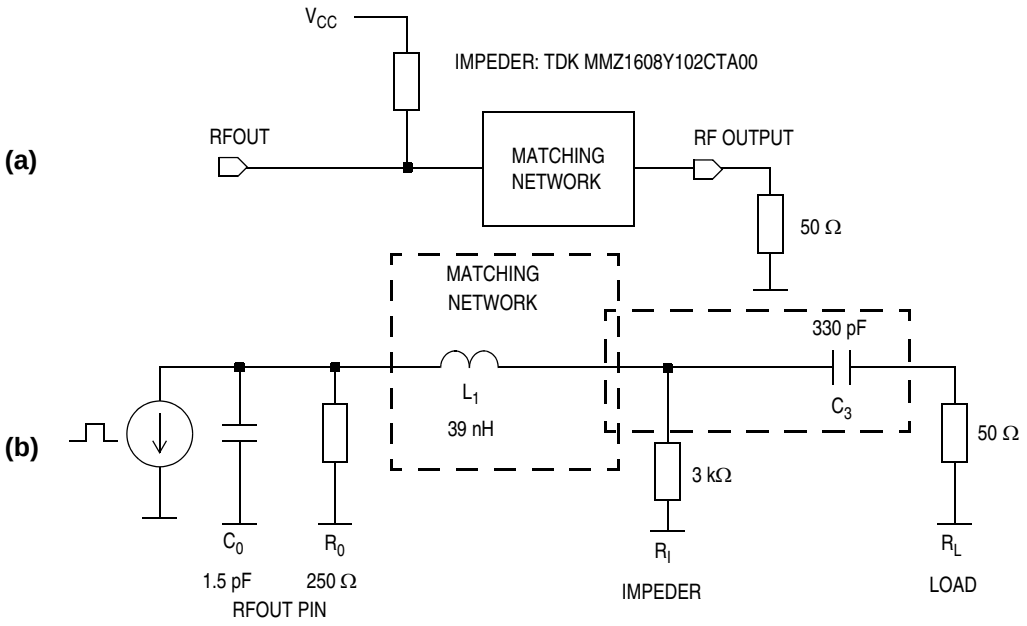

Figure 14-5. Ouput Characteristic and Matching Network for 434-MHz Frequency Band

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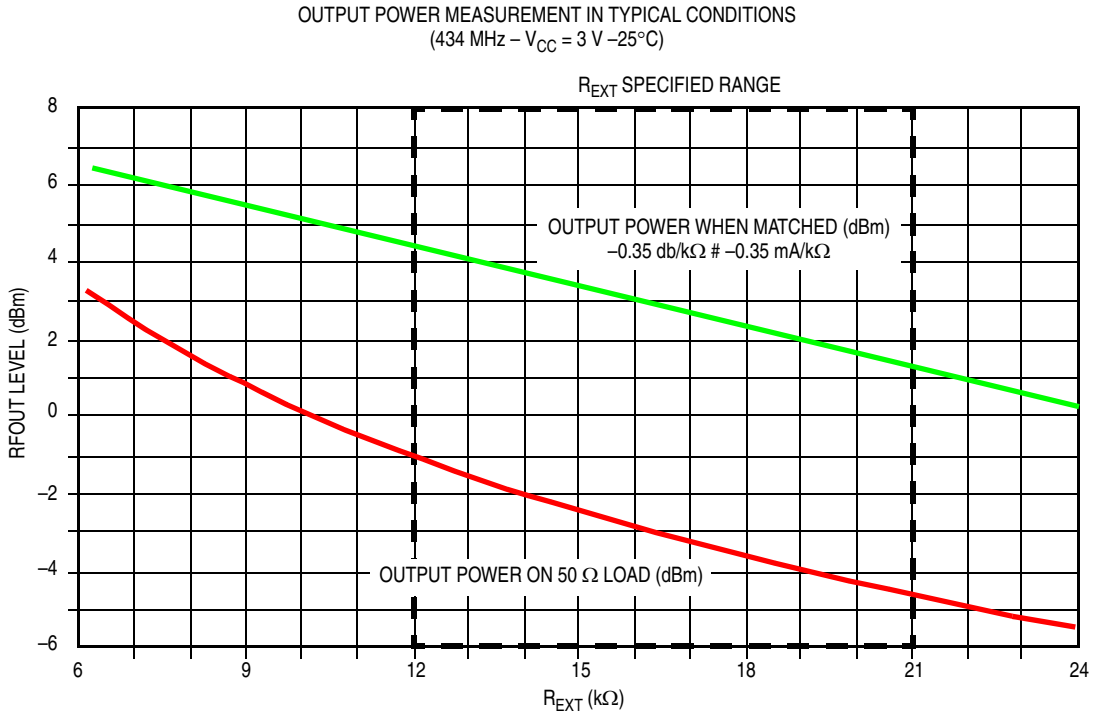

Figure 14-6. Output Power at 434-MHz Frequency Band versus R_{EXT} Value

14.9 Control Timing

Characteristic[1]	Symbol	Min	Max	Unit
Bus operating frequency V_{DD} = 3.0 V ± 10% V_{DD} = 2.0 V ± 10%	f_{Bus}	 32 k 32 k	 4.0 M 2.0 M	Hz
$\overline{\text{RESET}}$ pulse width low	t_{RL}	1.5	—	t_{cyc}
$\overline{\text{IRQ}}$ interrupt pulse width low (edge-triggered)	t_{ILHI}	1.5	—	t_{cyc}
$\overline{\text{IRQ}}$ interrupt pulse period	t_{ILIL}	Note 4	—	t_{cyc}
16-bit timer[2] Input capture pulse width[3] Input capture period Input clock pulse width	 t_{TH}, t_{TL} t_{TLTL} t_{TCH}, t_{TCL}	 2 Note[4] $(1/f_{OP})$ + 5	 — — —	 t_{cyc} t_{cyc} ns

1. V_{DD} = 1.8 V to 3.3 V, V_{SS} = 0 Vdc, T_A = –40°C to +85°C, unless otherwise noted
2. The 2-bit timer prescaler is the limiting factor in determining timer resolution.
3. Refer to **Table 11-3. Mode, Edge, and Level Selection** and supporting note.
4. The minimum period t_{TLTL} or t_{ILIL} should not be less than the number of cycles it takes to execute the capture interrupt service routine plus 2 t_{cyc}.

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14.10 Internal Oscillator Characteristics

Characteristic[1]	Symbol	Min	Typ	Max	Unit
Internal oscillator base frequency without trim[2] [3]	f_{INTOSC}	230.4	307.2	384.0	kHz
Internal oscillator base frequency with trim[2] [3]	$f_{INTOSC(I)}$	291.8	307.2	322.6	kHz
Internal oscillator multiplier[4]	N	1	—	127	—
External clock option[5] 3 V ± 10% 2 V ± 10%	f_{EXTOSC}	 128 k 128 k	 — —	 16 8	MHz

1. V_{DD} = 1.8 V to 3.3 V, V_{SS} = 0 Vdc, T_A = –40°C to +85°C, unless otherwise noted
2. Internal oscillator is selectable through software for a maximum frequency. Actual frequency will be multiplier (N) x base frequency.
3. f_{Bus} = (f_{INTOSC} / 4) x (internal oscillator multiplier)
4. Multiplier must be chosen to limit the maximum bus frequency to the maximum listed in **14.9 Control Timing**.
5. No more than 10% duty cycle deviation from 50%

14.11 LVI Characteristics

Characteristic[1]	Symbol	Min	Typ	Max	Unit
LVI low battery sense voltage[1]	V_{LVS}	1.90	2.00	2.15	V
LVI trip voltage[1]	V_{LVR}	1.76	1.85	2.00	V
LVI trip voltage hysteresis	H_{LVR}	50	70	90	mV
V_{DD} slew rate — rising	SR_R	—	—	0.05	V/µs
V_{DD} slew rate — falling	SR_F	—	—	0.10	V/µs
Response time — SR ≤ SR_{max}	t_{resp}	—	—	6.0	µs
Response time — SR > SR_{max}	t_{resp}	—	—	Note[2]	µs
Enable time (enable to output transition)	t_{en}	—	—	50	µs

1. The LVI samples V_{DD}, V_{LVR}, and V_{LVS} are V_{DD} voltages.
2. $\left(\frac{V_{DD}-V_{LVR}}{SR_{max}}-\frac{V_{DD}-V_{LVR}}{SR}\right)+1.5$

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14.12 Memory Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
RAM data retention voltage	V_{RDR}	1.3	—	—	V
FLASH pages per row	—	8	—	8	Pages
FLASH bytes per page	—	1	—	1	Bytes
FLASH read bus clock frequency	f_{Read}(1)	32 K	—	2.5 M	Hz
FLASH charge pump clock frequency (See **2.5.2 FLASH 2TS Charge Pump Frequency Control**)	f_{Pump}(2)	1.8	—	2.5	MHz
FLASH block/bulk erase time	t_{Erase}	100	—	—	ms
FLASH row erase time	$t_{RowErase}$	30	—	—	ms
FLASH high voltage kill time	t_{Kill}	200	—	—	µs
FLASH return to read time	t_{HVD}	50	—	—	µs
FLASH page program pulses	fls_{Pulses}(3)	—	—	15	Pulses
FLASH page program step size	t_{Step}(4)	1.0	—	1.2	ms
FLASH cumulative program time per row between erase cycles	t_{Row}(5)	—	—	8	Page program cycles
FLASH HVEN low to MARGIN high time	t_{HVTV}	50	—	—	µs
FLASH MARGIN high to PGM low time	t_{VTP}	150	—	—	µs
FLASH 2TS row program endurance(6)	—	10^4	-—	-—	Cycles
FLASH data retention time(7)	—	15	100	-—	Years

1. f_{Read} is defined as the frequency range for which the FLASH memory can be read.
2. f_{Pump} is defined as the charge pump clock frequency required for program, erase, and margin read operations.
3. fls_{Pulses} is defined as the number of pulses used to program the FLASH using the required smart program algorithm.
4. t_{Step} is defined as the amount of time during one page program cycle that HVEN is held high.
5. t_{Row} is defined as the cumulative time a row can see the program voltage before the row must be erased before further programming.
6. The minimum row endurance value specifies each row of the FLASH 2TS memory is guaranteed to work for at least this many erase/program cycles.
7. The FLASH is guaranteed to retain data over the entire temperature range for at least the minimum time specified.

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Section 15. Ordering Information and Mechanical Specifications

15.1 Introduction

This section contains ordering information for the MC68HC908RF2. In addition, package dimensions are given for the 32-pin low-profile quad flat pack (LQFP).

15.2 MC Order Numbers

Table 15-1. MC Order Numbers

MC Order Number[1]	Operating Temperature Range
MC68HC908RF2CFA	–40°C to +85°C
MC68HC908RF2MFA	–40°C to 125°C

1. FA = Low-profile quad flat pack (LQFP)

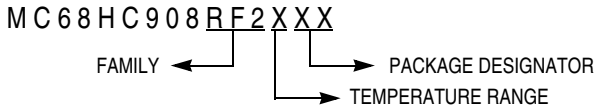

Figure 15-1. Device Numbering System

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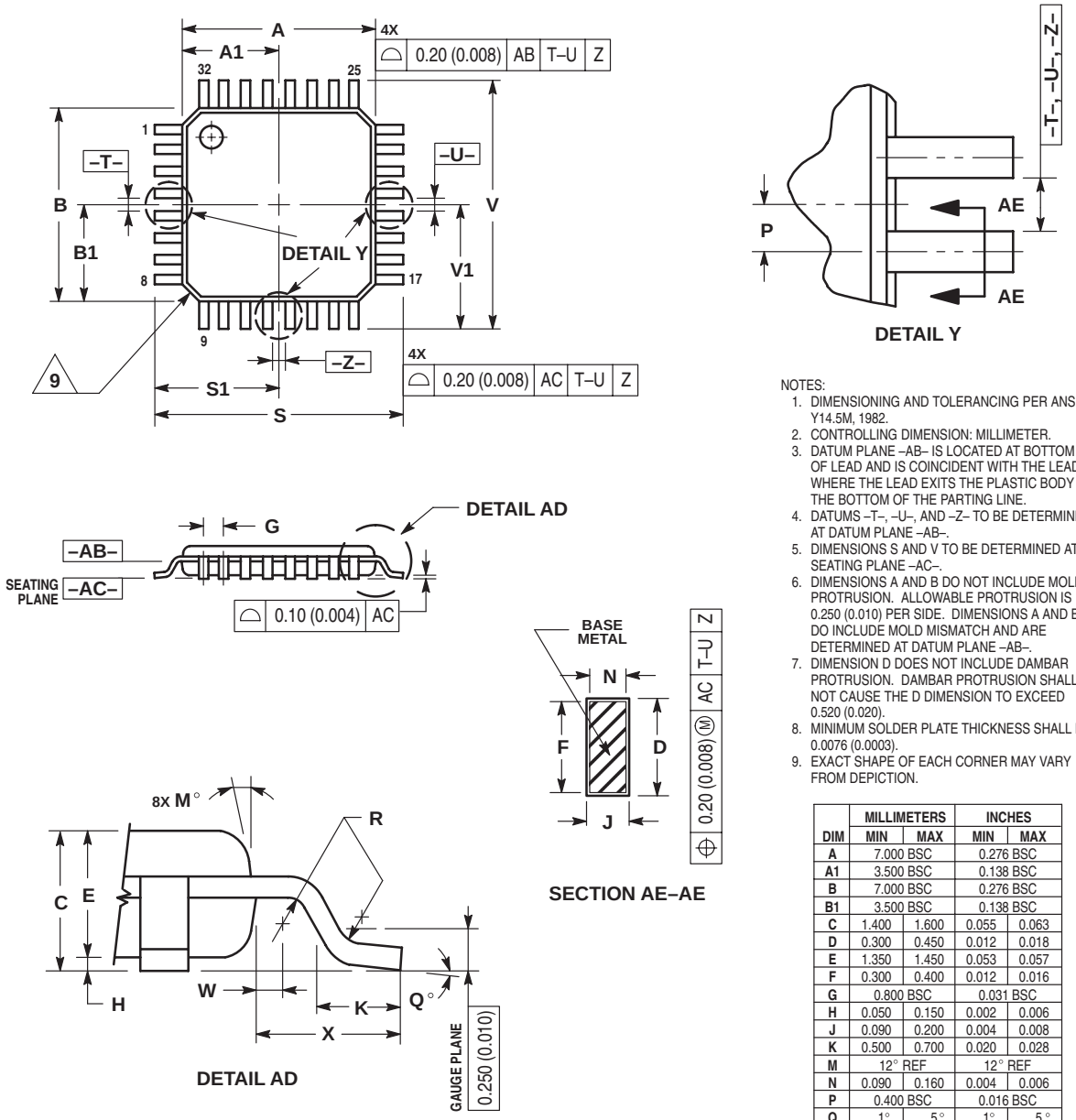
15.3 32-Pin LQFP Package (Case No. 873A)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

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