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Technical Data

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RoHS

MC56F825x/MC56F824x

44-pin LQFP
Case:
10 x 10 mm^2

48-pin LQFP
Case:
7 x 7 mm^2

64-pin LQFP
Case:
10 x 10 mm^2

MC56F825x/MC56F824x Digital Signal Controller

The MC56F825x/MC56F824x is a member of the 56800E core-based family of digital signal controllers (DSCs). It combines, on a single chip, the processing power of a DSP and the functionality of a microcontroller with a flexible set of peripherals to create a cost-effective solution. Because of its low cost, configuration flexibility, and compact program code, it is well-suited for many applications. The MC56F825x/MC56F824x includes many peripherals that are especially useful for cost-sensitive applications, including:

- Industrial control
- Home appliances
- Smart sensors
- Fire and security systems
- Solar inverters
- Battery chargers and management
- Switched-mode power supplies and power management
- Power metering
- Motor control (ACIM, BLDC, PMSM, SR, and stepper)
- Handheld power tools
- Arc detection
- Medical devices/equipment
- Instrumentation
- Lighting ballast

The 56800E core is based on a modified Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.

The MC56F825x/MC56F824x supports program execution from internal memories. Two data operands per instruction cycle can be accessed from the on-chip data RAM. A full set of programmable peripherals supports various applications. Each peripheral can be independently shut down to save power. Any pin, except Power pins and the Reset pin, can also be configured as General Purpose Input/Outputs (GPIOs).

On-chip features include:

- 60 MHz operation frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- On-chip memory
  - 56F8245/46: 48 KB (24K x 16) flash memory; 6 KB (3K x 16) unified data/program RAM
  - 56F8247: 48 KB (24K x 16) flash memory; 8 KB (4K x 16) unified data/program RAM
  - 56F8255/56/57: 64 KB (32K x 16) flash memory; 8 KB (4K x 16) unified data/program RAM
- eFlexPWM with up to 9 channels, including 6 channels with high (520 ps) resolution NanoEdge placement
- Two 8-channel, 12-bit analog-to-digital converters (ADCs) with dynamic x2 and x4 programmable amplifier, conversion time as short as 600 ns, and input current-injection protection
- Three analog comparators with integrated 5-bit DAC references
- Cyclic Redundancy Check (CRC) Generator
- Two high-speed queued serial communication interface (QSCI) modules with LIN slave functionality
- Queued serial peripheral interface (QSPI) module
- Two SMBus-compatible inter-integrated circuit (I^2C) ports
- Freescale's scalable controller area network (MSCAN) 2.0 A/B module
- Two 16-bit quad timers (2 x 4 16-bit timers)
- Computer operating properly (COP) watchdog module
- On-chip relaxation oscillator: 8 MHz (400 kHz at standby mode)
- Crystal/resonator oscillator
- Integrated power-on reset (POR) and low-voltage interrupt (LVI) and brown-out reset module
- Inter-module crossbar connection
- Up to 54 GPIOs
- 44-pin LQFP, 48-pin LQFP, and 64-pin LQFP packages
- Single supply: 3.0 V to 3.6 V

Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

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1 MC56F825x/MC56F824x Family Configuration

Table 1 compares the MC56F825x/MC56F824x devices.

Table 1. MC56F825x/MC56F824x Device Comparison

Feature		56F8245	56F8246	56F8247	56F8255	56F8256	56F8257
Operation Frequency (MHz)		60					
High Speed Peripheral Clock (MHz)		120					
Flash memory size (KB) with 1024 words per page		48	48	48	64	64	64
RAM size (KB)		6	6	8	8	8	8
Enhanced Flex PWM (eFlexPWM)	High resolution NanoEdge PWM (520 ps res.)	6	6	6	6	6	6
	Enhanced Flex PWM with Input Capture	0	0	3	0	0	3
	PWM Fault Inputs (from Crossbar Input)	4	4	4	4	4	4
12-bit ADC with x1, 2x, 4x Programmable Gain		2 x 4Ch	2 x 5Ch	2 x 8Ch	2 x 4Ch	2 x 5 Ch	2 x 8 Ch
Analog comparators (ACMP) each with integrated 5-bit DAC		3					
12-bit DAC		1					
Cyclic Redundancy Check (CRC)		Yes					
Inter-Integrated Circuit (I^2C) / SMBus		2					
Queued Serial peripheral Interface (QSPI)		1					
High speed Queued Serial Communications Interface (QSCI)[1]		2					
Controller Area Network (MSCAN)		0			1		
High Speed 16-bit multi-purpose timers (TMR)[2]		8					
Computer operating properly (COP) watchdog timer		Yes					
Integrated Power-On Reset and low voltage detection		Yes					
Phase-locked loop (PLL)		Yes					
8 MHz (400 kHz at standby mode) on-chip ROSC		Yes					
Crystal/resonator oscillator		Yes					
Crossbar	Input pins	6	6	6	6	6	6
	Output pins	2	2	6	2	2	6
General purpose I/O (GPIO)[3]		35	39	54	35	39	54
IEEE 1149.1 Joint Test Action Group (JTAG) interface		Yes					
Enhanced on-chip emulator (EOnCE)		Yes					
Operating temperature range	V temperature devices	–40 °C to 105 °C					
	M temperature devices	–40 °C to 125 °C					
Package		44LQFP	48LQFP	64LQFP	44LQFP	48LQFP	64LQFP

1 Can be clocked by high speed peripheral clock up to 120 MHz

2 Can be clocked by high speed peripheral clock up to 120 MHz

3 Shared with other function pins

2 Overview

2.1 MC56F825x/MC56F824x Features

2.1.1 Core

- Efficient 56800E digital signal processor (DSP) engine with modified Harvard architecture
  - Three internal address buses
  - Four internal data buses
- As many as 60 million instructions per second (MIPS) at 60 MHz core frequency
- 155 basic instructions in conjunction with up to 20 address modes
- 32-bit internal primary data buses supporting 8-bit, 16-bit, and 32-bit data movement, addition, subtraction, and logical operation
- Single-cycle 16 × 16-bit parallel multiplier-accumulator (MAC)
- Four 36-bit accumulators, including extension bits
- 32-bit arithmetic and logic multi-bit shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Instruction set supports DSP and controller functions
- Controller-style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/enhanced on-chip emulation (EOnCE) for unobtrusive, processor speed–independent, real-time debugging

2.1.2 Operation Range

- 3.0 V to 3.6 V operation (power supplies and I/O)
- From power-on-reset: approximately 2.7 V to 3.6 V
- Ambient temperature operating range
  - V temperature devices: –40 °C to +105 °C
  - M temperature devices: –40 °C to +125 °C

2.1.3 Memory

- Dual Harvard architecture that permits as many as three simultaneous accesses to program and data memory
- 48 KB (24K x 16) to 64 KB (32K x 16) on-chip flash memory with 2048 bytes (1024 x 16) page size
- 6 KB (3K x 16) to 8 KB (4K x 16) on-chip RAM with byte addressable
- EEPROM emulation capability using flash
- Support for 60 MHz program execution from both internal flash and RAM memories
- Flash security and protection that prevent unauthorized users from gaining access to the internal flash

2.1.4 Interrupt Controller

- Five interrupt priority levels
  - Three user programmable priority levels for each interrupt source: Level 0, 1, 2
  - Unmaskable level 3 interrupts include: illegal instruction, hardware stack overflow, misaligned data access, and SWI3 instruction
  - Maskable level 3 interrupts include: EOnCE step counter, EOnCE breakpoint unit, and EOnCE trace buffer
  - Lowest-priority software interrupt: level LP
- Nested interrupts: higher priority level interrupt request can interrupt lower priority interrupt subroutine
- Two programmable fast interrupts that can be assigned to any interrupt source
- Notification to system integration module (SIM) to restart clock out of wait and stop states
- Ability to relocate interrupt vector table

The masking of interrupt priority level is managed by the 56800E core.

2.1.5 Peripheral Highlights

- One Enhanced Flex Pulse Width Modulator (eFlexPWM) module
  - Up to nine output channels
  - 16-bit resolution for center aligned, edge aligned, and asymmetrical PWMs
  - Each complementary pair can operate with its own PWM frequency based and deadtime values
    - 4 Time base
    - Independent top and bottom deadtime insertion
  - PWM outputs can operate as complimentary pairs or independent channels
  - Independent control of both edges of each PWM output
  - 6-channel NanoEdge high resolution PWM
    - Fractional delay for enhanced resolution of the PWM period and edge placement
    - Arbitrary eFlexPWM edge placement - PWM phase shifting
    - NanoEdge implementation: 520 ps PWM frequency resolution
  - 3 Channel PWM with full Input Capture features
    - Three PWM Channels - PWMA, PWMB, and PWMX
    - Enhanced input capture functionality
  - Support for synchronization to external hardware or other PWM
  - Double buffered PWM registers
    - Integral reload rates from 1 to 16
    - Half cycle reload capability
  - Multiple output trigger events can be generated per PWM cycle via hardware
  - Support for double switching PWM outputs
  - Up to four fault inputs can be assigned to control multiple PWM outputs
    - Programmable filters for fault inputs
  - Independently programmable PWM output polarity
  - Individual software control for each PWM output
  - All outputs can be programmed to change simultaneously via a FORCE_OUT event
  - PWMX pin can optionally output a third PWM signal from each submodule
  - Channels not used for PWM generation can be used for buffered output compare functions
  - Channels not used for PWM generation can be used for input capture functions
  - Enhanced dual edge capture functionality

  - Option to supply the source for each complementary PWM signal pair from any of the following:
    - Crossbar module outputs
    - External ADC input, taking into account values set in ADC high and low limit registers
- Two independent 12-bit analog-to-digital converters (ADCs)
  - 2 x 8 channel external inputs
  - Built-in x1, x2, x4 programmable gain pre-amplifier
  - Maximum ADC clock frequency: up to 10 MHz
    - Single conversion time of 8.5 ADC clock cycles (8.5 x 100 ns = 850 ns)
    - Additional conversion time of 6-ADC clock cycles (6 x 100 ns = 600 ns)
  - Sequential, parallel, and independent scan mode
  - First 8 samples have Offset, Limit and Zero-crossing calculation supported
  - ADC conversions can be synchronized by eFlexPWM and timer modules via internal crossbar module
  - Support for simultaneous and software triggering conversions
  - Support for multi-triggering mode with a programmable number of conversions on each trigger
- Inter-module Crossbar Switch (XBAR)
  - Programmable internal module connections among the eFlexPWM, ADCs, Quad Timers, 12-bit DAC, HSCMPs, and package pins
  - User-defined input/output pins for PWM fault inputs, Timer input/output, ADC triggers, and Comparator outputs
- Three analog comparators (CMPs)
  - Selectable input source includes external pins, internal DACs
  - Programmable output polarity
  - Output can drive timer input, eFlexPWM fault input, eFlexPWM source, external pin output, and trigger ADCs
  - Output falling and rising edge detection able to generate interrupts
  - 32-tap programmable voltage reference per comparator
- One 12-bit digital-to-analog converter (12-bit DAC)
  - 12-bit resolution
  - Power down mode
  - Output can be routed to internal comparator, or off chip
- Two four-channel 16-bit multi-purpose timer (TMR) modules
  - Four independent 16-bit counter/timers with cascading capability per module
  - Up to 120 MHz operating clock
  - Each timer has capture and compare and quadrature decoder capability
  - Up to 12 operating modes
  - Four external inputs and two external outputs
- Two queued serial communication interface (QSCI) modules with LIN slave functionality
  - Up to 120 MHz operating clock
  - Four-byte-deep FIFOs available on both transmit and receive buffers
  - Full-duplex or single-wire operation
  - Programmable 8- or 9-bit data format
  - 13-bit integer and 3-bit fractional baud rate selection
  - Two receiver wakeup methods:
    - Idle line
    - Address mark
  - 1/16 bit-time noise detection
  - Support LIN slave operation

- One queued serial peripheral interface (QSPI) module
  - Full-duplex operation
  - Four-word deep FIFOs available on both transmit and receive buffers
  - Master and slave modes
  - Programmable length transactions (2 to 16 bits)
  - Programmable transmit and receive shift order (MSB as first or last bit transmitted)
  - Maximum slave module frequency = module clock frequency/2
  - 13-bit baud rate divider for low speed communication
- Two inter-integrated circuit (I^2C) ports
  - Operation at up to 100 kbps
  - Support for master and slave operation
  - Support for 10-bit address mode and broadcasting mode
  - Support for SMBus, Version 2
- One Freescale Scalable Controller Area Network (MSCAN) module
  - Fully compliant with CAN protocol Version 2.0 A/B
  - Support for standard and extended data frames
  - Support for data rate up to 1 Mbit/s
  - Five receive buffers and three transmit buffers
- Computer operating properly (COP) watchdog timer capable of selecting different clock sources
  - Programmable prescaler and timeout period
  - Programmable wait, stop, and partial powerdown mode operation
  - Causes loss of reference reset 128 cycles after loss of reference clock to the PLL is detected
  - Choice of clock sources from four sources in support of EN60730 and IEC61508:
    - On-chip relaxation oscillator
    - External crystal oscillator/external clock source
    - System clock (IP bus to 60 MHz)
- Power supervisor (PS)
  - On-chip linear regulator for digital and analog circuitry to lower cost and reduce noise
  - Integrated low voltage detection to generate warning interrupt if VDD is below low voltage detection (LVI) threshold
  - Integrated power-on reset (POR)
    - Reliable reset process during power-on procedure
    - POR is released after VDD passes low voltage detection (LVI) threshold
  - Integrated brown-out reset
  - Run, wait, and stop modes
- Phase lock loop (PLL) providing a high-speed clock to the core and peripherals
  - 2x system clock provided to Quad Timers and SCIs
  - Loss of lock interrupt
  - Loss of reference clock interrupt
- Clock sources
  - On-chip relaxation oscillator with two user selectable frequencies: 400 kHz for low speed mode, 8 MHz for normal operation
  - External clock: crystal oscillator, ceramic resonator, and external clock source
- Cyclic Redundancy Check (CRC) Generator
  - Hardware CRC generator circuit using 16-bit shift register

  - CRC16-CCITT compliancy with x16 + x12 + x5 + 1 polynomial
  - Error detection for all single, double, odd, and most multi-bit errors
  - Programmable initial seed value
  - High-speed hardware CRC calculation
  - Optional feature to transpose input data and CRC result via transpose register, required on applications where bytes are in LSb (Least Significant bit) format.
- Up to 54 general-purpose I/O (GPIO) pins
  - 5 V tolerant I/O
  - Individual control for each pin to be in peripheral or GPIO mode
  - Individual input/output direction control for each pin in GPIO mode
  - Individual control for each output pin to be in push-pull mode or open-drain mode
  - Hysteresis and configurable pullup device on all input pins
  - Ability to generate interrupt with programmable rising or falling edge and software interrupt
  - Configurable drive strength: 4 mA / 8 mA sink/source current
- JTAG/EOnCE debug programming interface for real-time debugging
  - IEEE 1149.1 Joint Test Action Group (JTAG) interface
  - EOnCE interface for real-time debugging

2.1.6 Power Saving Features

- Low-speed run, wait, and stop modes: as low as 781 Hz clock provided by OCCS and internal ROSC
- Large regulator standby mode available for reducing power consumption at low-speed mode
- Less than 30 µs typical wakeup time from stop modes
- Each peripheral can be individually disabled to save power

2.2 Award-Winning Development Environment

Processor Expert (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.

The CodeWarrior Integrated Development Environment (IDE) is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs), demonstration board kit, and development system cards supports concurrent engineering. Together, PE, CodeWarrior, and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

2.3 Architecture Block Diagram

The MC56F825x/MC56F824x's architecture appears in Figure 1 and Figure 2. Figure 1 illustrates how the 56800E system buses communicate with internal memories and the IP bus interface as well as the internal connections among the units of the 56800E core.

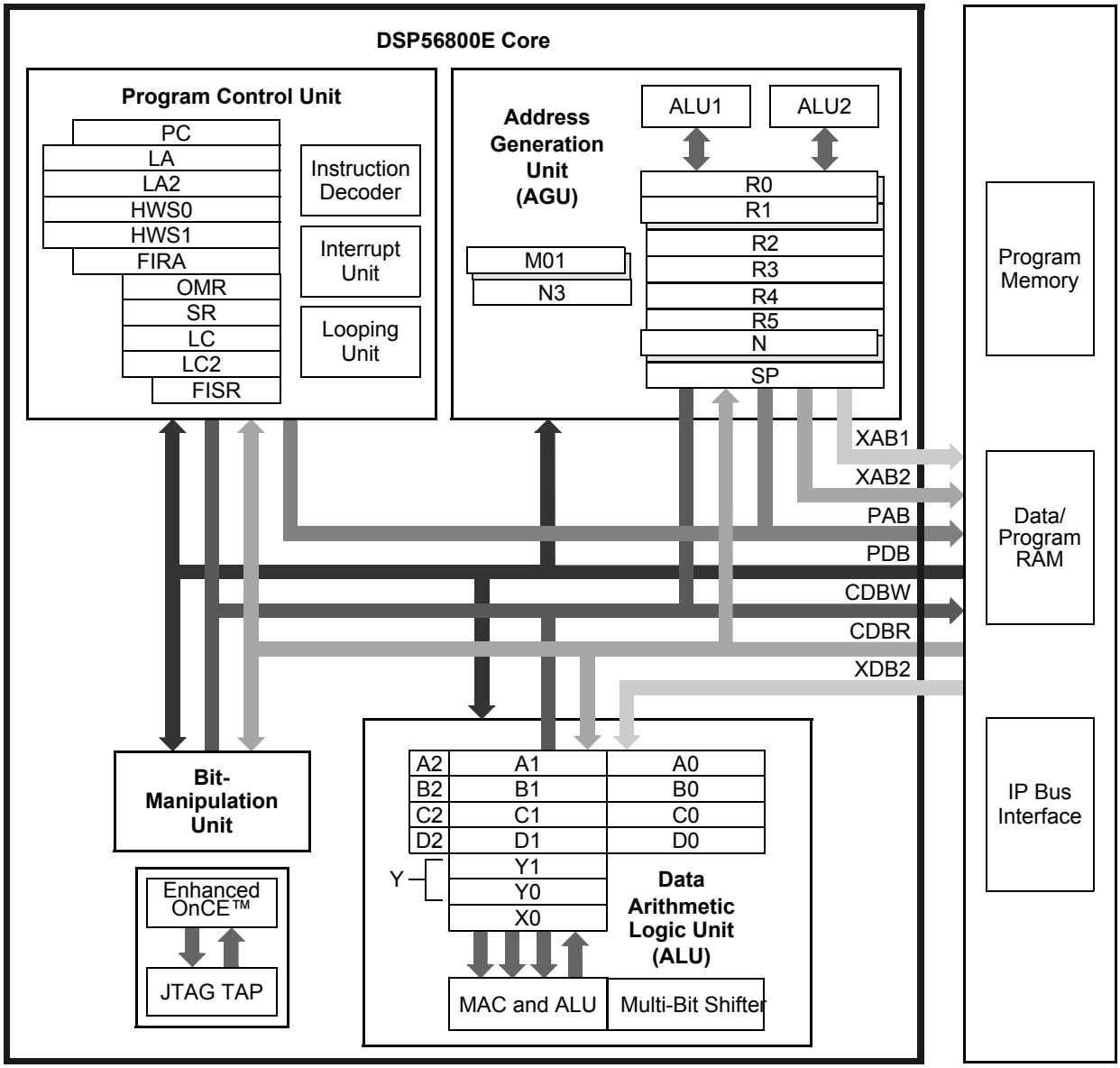


Figure 1. 56800E Core Block Diagram

Figure 2 shows the peripherals and control blocks connected to the IP bus bridge. Refer to the system integration module (SIM) section in the device's reference manual for information about which signals are multiplexed with those of other peripherals.

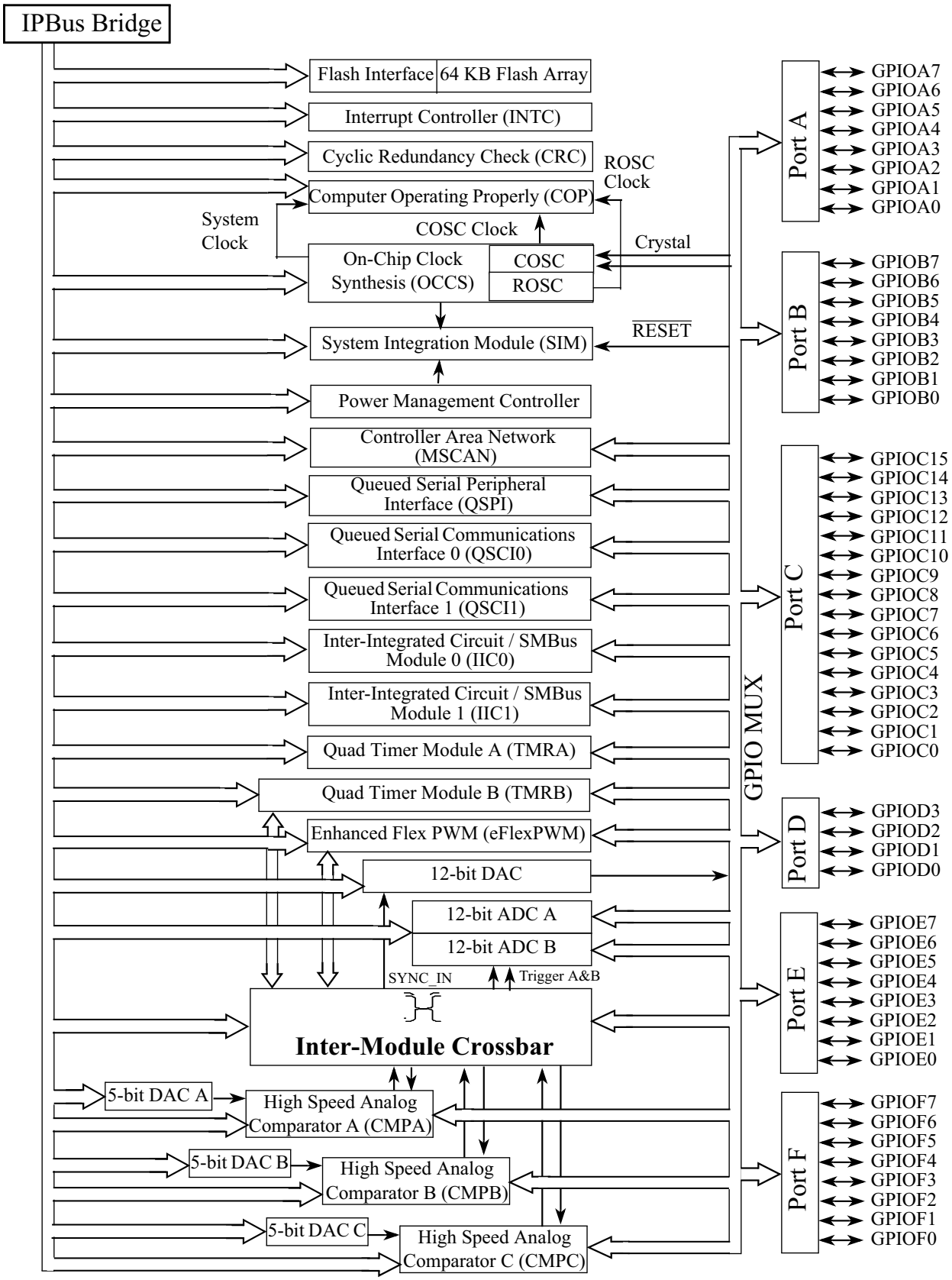


Figure 2. Peripheral Subsystem

2.4 Product Documentation

The documents listed in Table 2 are required for a complete description and proper design with the MC56F825x/MC56F824x. Documentation is available from local Freescale distributors, Freescale Semiconductor sales offices, Freescale Literature Distribution Centers, or online at http://www.freescale.com.

Table 2. MC56F825x/MC56F824x Device Documentation

Topic	Description	Order Number
DSP56800E Reference Manual	Detailed description of the 56800E family architecture, 16-bit digital signal controller core processor, and the instruction set	DSP56800ERM
MC56F825x Reference Manual	Detailed description of peripherals of the MC56F825x/MC56F824x devices	MC56F825XRM
MC56F824x/5x Serial Bootloader User Guide	Detailed description of the Serial Bootloader in the 56F800x family of devices	TBD
MC56F825x Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	MC56F825X
MC56F825x Errata	Detailed description of any chip issues that might be present	MC56F825XE

3 Signal/Connection Descriptions

3.1 Introduction

The input and output signals of the MC56F825x/MC56F824x are organized into functional groups, as detailed in Table 3.

Table 3. Functional Group Pin Allocations

Functional Group	Number of Pins in 44 LQFP	Number of Pins in 48 LQFP	Number of Pins in 64 LQFP
Power inputs (V_{DD}, V_{DDA}, V_{CAP})	5	5	6
Ground (V_{SS}, V_{SSA})	4	4	4
Reset[1]	1	1	1
Enhanced Flex Pulse Width Modulator (eFlexPWM) ports[1]	6	6	9
Queued Serial Peripheral Interface (SPI) ports[1]	4	4	4
Queued Serial Communications Interface 0&1 (QSCI0 & QSCI1) ports[1]	6	6	9
Inter-Integrated Circuit Interface 0&1 (I^2C0 & I^2C0) ports[1]	4	4	6
Analog-to-Digital Converter (ADC) inputs[1]	8	10	16
High Speed Analog Comparator inputs/outputs[1]	11	12	15
12-bit Digital-to-Analog Converter (DAC_12B) output	1	1	1
Quad Timer Module (TMRA & TMRB) ports[1]	5	5	8
Freescale's Scalable Controller-Area-Network (MSCAN)[1, 2]	2	2	2
Inter-Module Cross Bar package inputs/outputs[1]	10	12	17
Clock[1]	3	4	4
JTAG/Enhanced On-Chip Emulation (EOnCE)[1]	4	4	4

1 Pins may be shared with other peripherals. See Table 4.
2 Exclude MC56F824x.

Table 4 summarizes all device pins. Each table row describes the signal or signals present on a pin, sorted by pin number. Peripheral pins in bold identify reset state.

Table 4. MC56F825x/MC56F824x Pins

Pin Number			Pin Name	Peripherals													
44 LQFP	48 LQFP	64 LQFP		GPIO	I^2C	SCI	SPI	MS CAN[1]	ADC	Cross Bar	COMP	Quad Timer	eFlex PWM	Power	JTAG	Misc.
1	1	1	TCK/*GPIOD2*	*GPIOD2*											**TCK**	
2	2	2	$\overline{\text{RESET}}$ / *GPIOD4*	*GPIOD4*												**$\overline{\text{RESET}}$**
3	3	3	GPIOC0/*XTAL/CLKIN*	**GPIOC0**												*XTAL/ CLKIN*
4	4	4	GPIOC1/*EXTAL*	**GPIOC1**												*EXTAL*
5	5	5	GPIOC2/*TXD0/TB0/XB_IN2/ CLKO*	**GPIOC2**		*TXD0*				*XB_IN2*		*TB0*				*CLKO*
		6	GPIOF8/*RXD0/TB1*	**GPIOF8**		*RXD0*						*TB1*				
6	6	7	GPIOC3/*TA0/CMPA_O/RXD0*	**GPIOC3**		*RXD0*					*CMPA_O*	*TA0*				
7	7	8	GPIOC4/*TA1/CMPB_O*	**GPIOC4**							*CMPB_O*	*TA1*				
		9	GPIOA7/*ANA7*	**GPIOA7**					*ANA7*							
		10	GPIOA6/*ANA6*	**GPIOA6**					*ANA6*							
		11	GPIOA5/*ANA5*	**GPIOA5**					*ANA5*							
	8	12	GPIOA4/*ANA4*	**GPIOA4**					*ANA4*							
8	9	13	GPIOA0/*ANA0& CMPA_P2/CMPC_O*	**GPIOA0**					*ANA0*		*CMPA_P2/ CMPC_O*					
9	10	14	GPIOA1/ *ANA1&CMPA_M0*	**GPIOA1**					*ANA1*		*CMPA_M0*					
10	11	15	GPIOA2/*ANA2&VREFHA& CMPA_M1*	**GPIOA2**					*ANA2& VREFHA*		*CMPA_M1*					
11	12	16	GPIOA3/*ANA3&VREFLA& CMPA_M2*	**GPIOA3**					*ANA3& VREFLA*		*CMPA_M2*					
		17	GPIOB7/*ANB7&CMPB_M2*	**GPIOB7**					*ANB7*		*CMPB_M2*					
12	13	18	GPIOC5/*DACO/XB_IN7*	**GPIOC5**						*XB_IN7*						*DACO*
		19	GPIOB6/*ANB6&CMPB_M1*	**GPIOB6**					*ANB6*		*CMPB_M1*					
		20	GPIOB5/*ANB5&CMPC_M2*	**GPIOB5**					*ANB5*		*CMPC_M2*					
	14	21	GPIOB4/*ANB4&CMPC_M1*	**GPIOB4**					*ANB4*		*CMPC_M1*					
13	15	22	V_{DDA}											**V_{DDA}**		
14	16	23	V_{SSA}											**V_{SSA}**		
15	17	24	GPIOB0/ *ANB0&CMPB_P2*	**GPIOB0**					*ANB0*		*CMPB_P2*					
16	18	25	GPIOB1/ *ANB1&CMPB_M0*	**GPIOB1**					*ANB1*		*CMPB_M0*					
17	19	26	V_{CAP}											**V_{CAP}**		
18	20	27	GPIOB2/ *ANB2&VREFHB&CMPC_P2*	**GPIOB2**					*ANB2& VREFHB*		*CMPC_P2*					

Table 4. MC56F825x/MC56F824x Pins (continued)

Pin Number			Pin Name	Peripherals													
44 LQFP	48 LQFP	64 LQFP		GPIO	I^2C	SCI	SPI	MSCAN[1]	ADC	Cross Bar	COMP	Quad Timer	eFlex PWM	Power	JTAG	Misc.
19	21	28	GPIOB3/ *ANB3&VREFLB&CMPC_M0*	**GPIOB3**					*ANB3& VREFLB*		*CMPC_M0*					
		29	V_{DD}											**V_{DD}**		
20	22	30	V_{SS}											**V_{SS}**		
21	23	31	GPIOC6/*TA2/XB_IN3/ CMP_REF*	**GPIOC6**						*XB_IN3*	*CMP_REF*	*TA2*				
22	24	32	GPIOC7/$\overline{SS}$/*TXD0*	**GPIOC7**		*TXD0*	$\overline{SS}$									
23	25	33	GPIOC8/*MISO/RXD0*	**GPIOC8**		*RXD0*	*MISO*									
24	26	34	GPIOC9/*SCLK/XB_IN4*	**GPIOC9**			*SCLK*			*XB_IN4*						
25	27	35	GPIOC10/MOSI/XB_IN5/MISO	**GPIOC10**			MOSI/ MISO			XB_IN5						
	28	36	GPIOF0/*XB_IN6*	**GPIOF0**						*XB_IN6*						
26	29	37	GPIOC11/*CANTX/SCL1/TXD1*	**GPIOC11**	*SCL1*	*TXD1*		*CANTX*								
27	30	38	GPIOC12/*CANRX/SDA1/RXD1*	**GPIOC12**	*SDA1*	*RXD1*		*CANRX*								
		39	GPIOF2/*SCL1/XB_OUT2*	**GPIOF2**	*SCL1*					*XB_OUT2*						
		40	GPIOF3/*SDA1/XB_OUT3*	**GPIOF3**	*SDA1*					*XB_OUT3*						
		41	GPIOF4/*TXD1/XB_OUT4*	**GPIOF4**		*TXD1*				*XB_OUT4*						
		42	GPIOF5/*RXD1/XB_OUT5*	**GPIOF5**		*RXD1*				*XB_OUT5*						
28	31	43	V_{SS}											**V_{SS}**		
29	32	44	V_{DD}											**V_{DD}**		
30	33	45	GPIOE0/*PWM0B*	**GPIOE0**									*PWM0B*			
31	34	46	GPIOE1/*PWM0A*	**GPIOE1**									*PWM0A*			
32	35	47	GPIOE2/*PWM1B*	**GPIOE2**									*PWM1B*			
33	36	48	GPIOE3/*PWM1A*	**GPIOE3**									*PWM1A*			
34	37	49	GPIOC13/*TA3/XB_IN6*	**GPIOC13**						*XB_IN6*		TA3				
	38	50	GPIOF1/*CLKO/XB_IN7*	**GPIOF1**						*XB_IN7*						*CLKO*
35	39	51	GPIOE4/*PWM2B/XB_IN2*	**GPIOE4**						*XB_IN2*			*PWM2B*			
36	40	52	GPIOE5/*PWM2A/XB_IN3*	**GPIOE5**						*XB_IN3*			*PWM2A*			
		53	GPIOE6/*PWM3B/XB_IN4*	**GPIOE6**						*XB_IN4*			*PWM3B*			
		54	GPIOE7/*PWM3A/XB_IN5*	**GPIOE7**						*XB_IN5*			*PWM3A*			
37	41	55	GPIOC14/*SDA0/XB_OUT0*	**GPIOC14**	*SDA0*					*XB_OUT0*						
38	42	56	GPIOC15/*SCL0/XB_OUT1*	**GPIOC15**	*SCL0*					*XB_OUT1*						
39	43	57	V_{CAP}											**V_{CAP}**		
		58	GPIOF6/*TB2/PWM3X*	**GPIOF6**								*TB2*	*PWM3X*			
		59	GPIOF7/*TB3*	**GPIOF7**								*TB3*				
40	44	60	V_{DD}											**V_{DD}**		

Table 4. MC56F825x/MC56F824x Pins (continued)

Pin Number			Pin Name	Peripherals												
44 LQFP	48 LQFP	64 LQFP		GPIO	I^2C	SCI	SPI	MS CAN[1]	ADC	Cross Bar	COMP	Quad Timer	eFlex PWM	Power	JTAG	Misc.
41	45	61	V_{SS}											V_{SS}		
42	46	62	TDO/*GPIOD1*	***GPIOD1***											**TDO**	
43	47	63	TMS/*GPIOD3*	***GIPOD3***											**TMS**	
44	48	64	TDI/*GPIOD0*	***GPIOD0***											**TDI**	

1 The MSCAN module is not available on the MC56F824x devices.

3.2 Pin Assignment

Figure 3 shows the pin assignments of the 56F8245 and 56F8255's 44-pin low-profile quad flat pack (44LQFP). Figure 4 shows the pin assignments of the 56F8246 and 56F8256's 48-pin low-profile quad flat pack (48LQFP). Figure 5 shows the pin assignments of the 56F8247 and 56F8257's 64-pin low-profile quad flat pack (64LQFP).

NOTE

The CANRX and CANTX signals of the MSCAN module are not available on the MC56F824x devices.

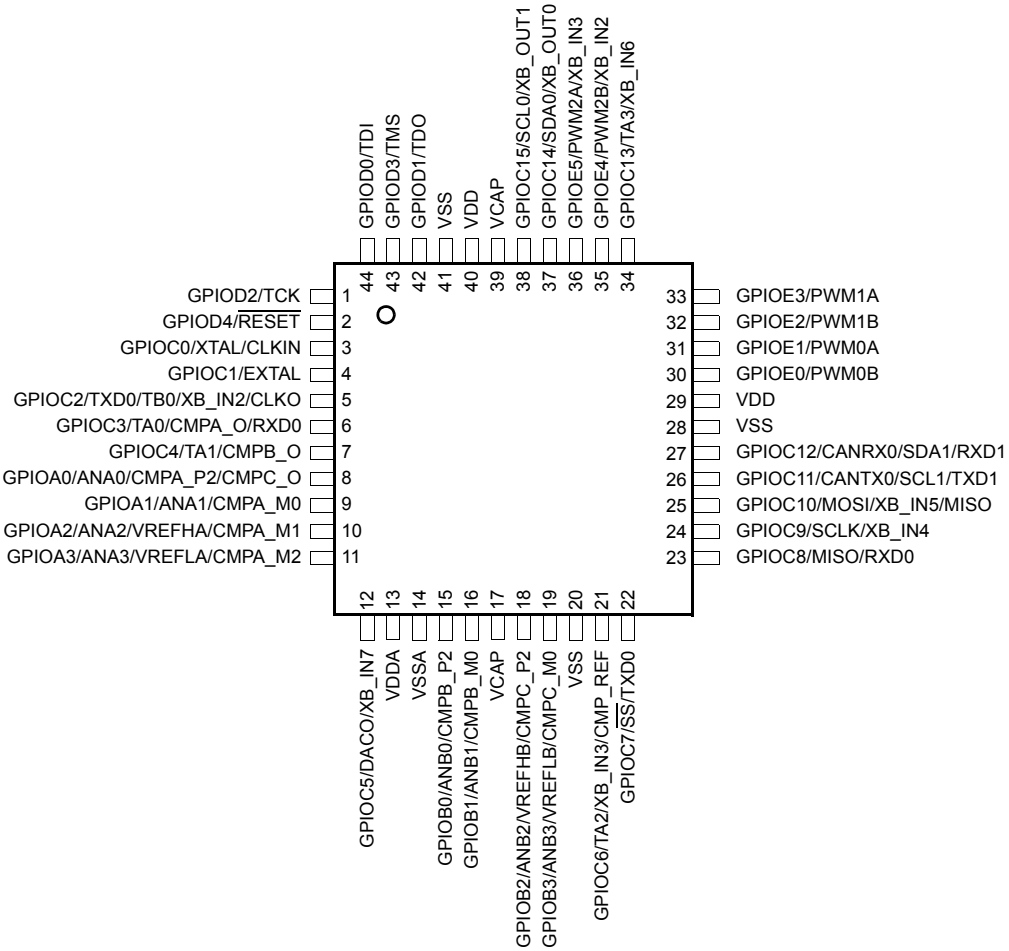


Figure 3. Top View: 56F8245 and 56F8255 44-Pin LQFP Package

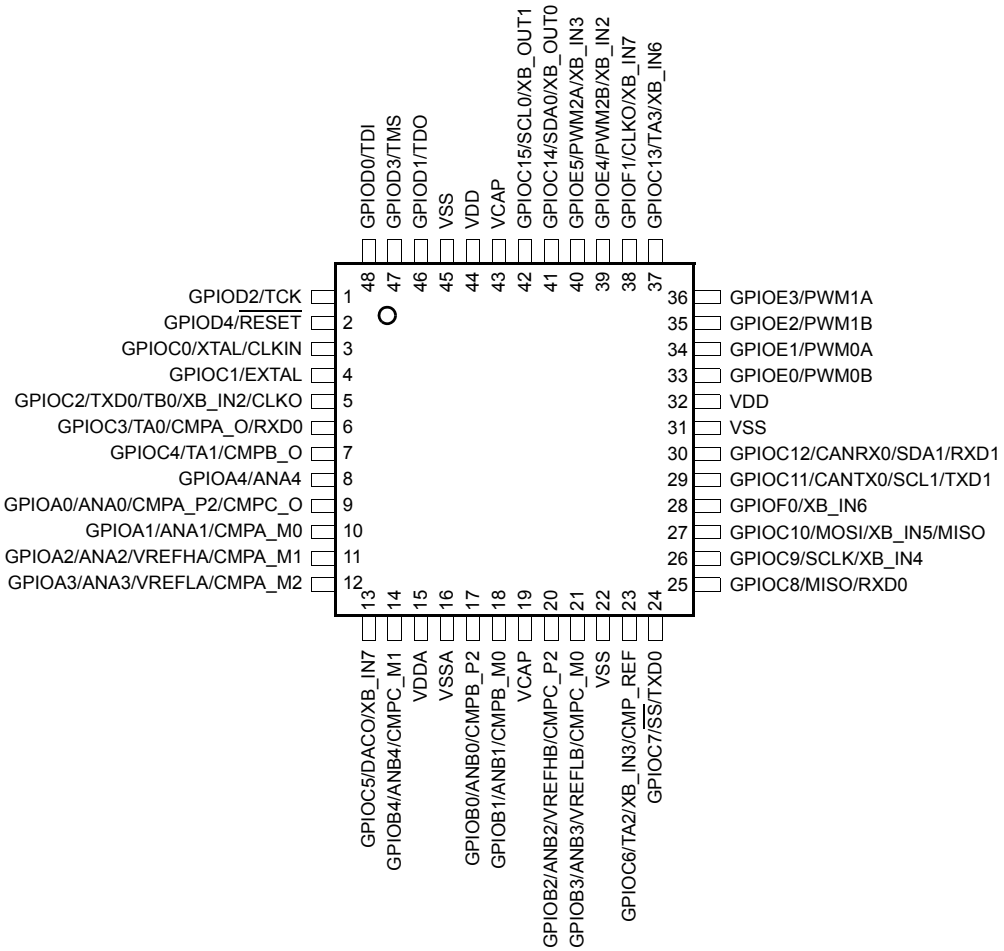


Figure 4. Top View: 56F8246 and 56F8256 48-Pin LQFP Package

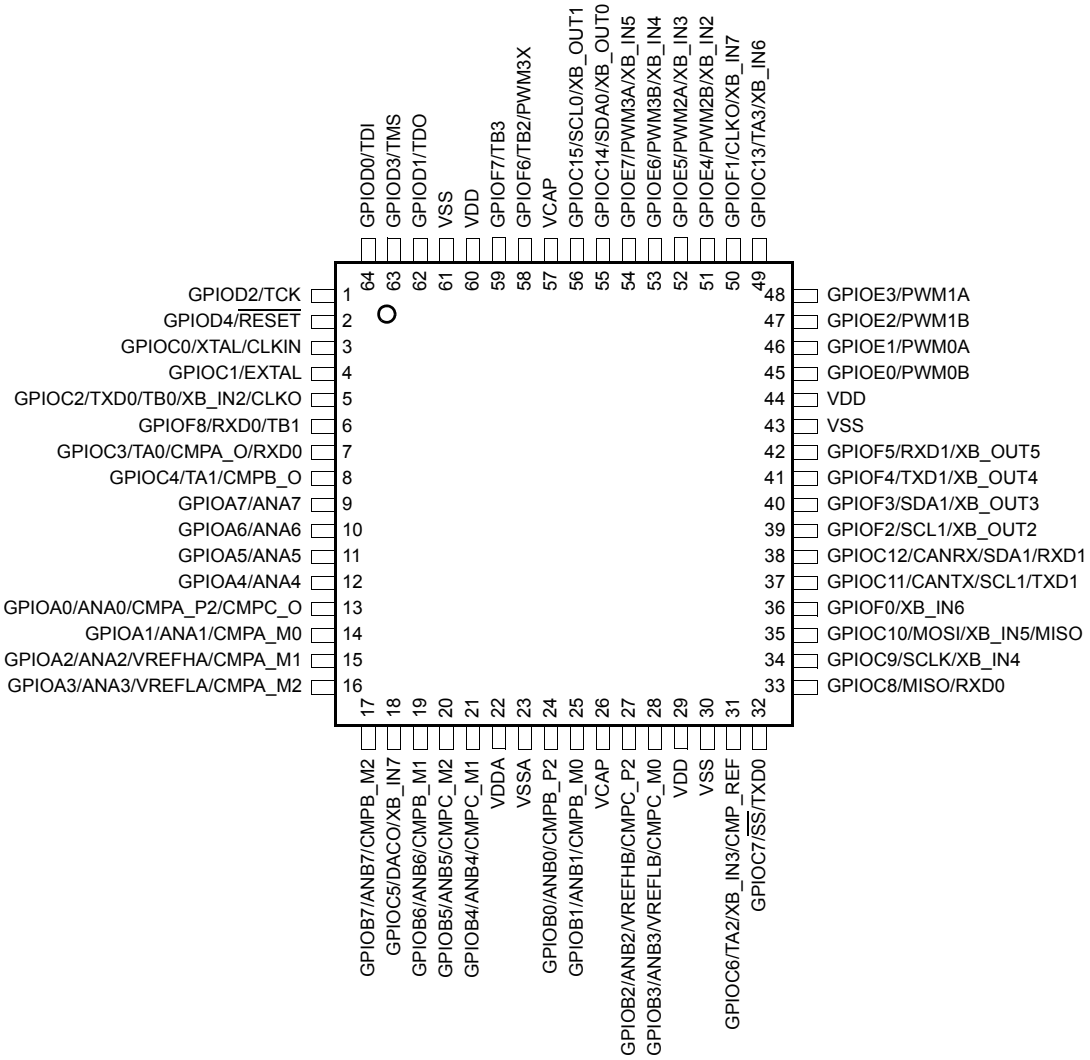


Figure 5. Top View: 56F8247 and 56F8257 64-Pin LQFP Package

3.3 MC56F825x/MC56F824x Signal Pins

After reset, each pin is configured for its primary function (listed first). Any alternative functionality, shown in parentheses and as *italic*, must be programmed via the GPIO module's peripheral enable registers (GPIO_x_PER) and the SIM module's GPIO peripheral select (GPSx) registers.

Table 5. MC56F825x/MC56F824x Signal and Package Information

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
V_{DD}			29	Supply	Supply	I/O Power — This pin supplies 3.3 V power to the chip I/O interface.
V_{DD}	29	32	44			
V_{DD}	40	44	60			
V_{SS}	20	22	30	Supply	Supply	I/O Ground — These pins provide ground for chip I/O interface.
V_{SS}	28	31	43			
V_{SS}	41	45	61			
V_{DDA}	13	15	22	Supply	Supply	Analog Power — This pin supplies 3.3 V power to the analog modules. It must be connected to a clean analog power supply.
V_{SSA}	14	16	23	Supply	Supply	Analog Ground — This pin supplies an analog ground to the analog modules. It must be connected to a clean power supply.
V_{CAP}	17	19	26	Supply	Supply	V_{CAP} — Connect a bypass capacitor of 2.2 µF or greater between this pin and V_{SS} to stabilize the core voltage regulator output required for proper device operation. See Section 8.2, "Electrical Design Considerations," on page 73.
V_{CAP}	39	43	57			
TDI *(GPIOD0)*	44	48	64	Input Input/ Output	Input, internal pullup enabled	Test Data Input — This input pin provides a serial input data stream to the JTAG/EOnCE port. It is sampled on the rising edge of TCK and has an on-chip pullup resistor. Port D GPIO — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TDI.
TDO *(GPIOD1)*	42	46	62	Output Input/ Output	Output	Test Data Output — This tri-stateable output pin provides a serial output data stream from the JTAG/EOnCE port. It is driven in the shift-IR and shift-DR controller states, and changes on the falling edge of TCK. Port D GPIO — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TDO.
TCK *(GPIOD2)*	1	1	1	Input Input/ Output	Input, internal pullup enabled	Test Clock Input — This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/EOnCE port. The pin is connected internally to a pullup resistor. A Schmitt-trigger input is used for noise immunity. Port D GPIO — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TCK

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
TMS *(GPIOD3)*	43	47	63	input Input/ Output	Input, internal pullup enabled	Test Mode Select Input — This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pullup resistor. Port D GPIO — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is TMS **Note**: Always tie the TMS pin to VDD through a 2.2K resistor if need to keep on-board debug capability. Otherwise directly tie to VDD
$\overline{\text{RESET}}$ *(GPIOD4)*	2	2	2	Input Input/ Open-drain Output	Input, internal pullup enabled	Reset — This input is a direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the device is initialized and placed in the reset state. A Schmitt-trigger input is used for noise immunity. The internal reset signal is deasserted synchronous with the internal clocks after a fixed number of internal clocks. Port D GPIO — This GPIO pin can be individually programmed as an input or open-drain output pin.If $\overline{\text{RESET}}$ functionality is disabled in this mode and the chip can be reset only via POR, COP reset, or software reset. After reset, the default state is $\overline{\text{RESET}}$.
GPIOA0 *(ANA0& CMPA_P2)* *(CMPC_O)*	8	9	13	Input/ Output Input Output	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA0 and CMPA_P2 — Analog input to channel 0 of ADCA and positive input 2 of analog comparator A. CMPC_O— Analog comparator C output When used as an analog input, the signal goes to the ANA0 and CMPA_P2. After reset, the default state is GPIOA0.
GPIOA1 *(ANA1& CMPA_M0)*	9	10	14	Input/ Output Input	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA1 and CMPA_M0 — Analog input to channel 1of ADCA and negative input 0 of analog comparator A. When used as an analog input, the signal goes to the ANA1 and CMPA_M0. After reset, the default state is GPIOA1.

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOA2 *(ANA2& VREFHA& CMPA_M1)*	10	11	15	Input/ Output Input	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA2 and VREFHA and CMPA_M1 — Analog input to channel 2 of ADCA and analog references high of ADCA and negative input 1 of analog comparator A. When used as an analog input, the signal goes to ANA2 and VREFHA and CMPA_M1. ADC control register configures this input as ANA2 or VREFHA. After reset, the default state is GPIOA2.
GPIOA3 *(ANA3& VREFLA& CMPA_M2)*	11	12	16	Input/ Output Input	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA3 and VREFLA and CMPA_M2 — Analog input to channel 3 of ADCA and analog references low of ADCA and negative input 2 of analog comparator A. When used as an analog input, the signal goes to ANA3 and VREFLA and CMPA_M2. ADC control register configures this input as ANA3 or VREFLA. After reset, the default state is GPIOA3.
GPIOA4 *(ANA4)*		8	12	Input/ Output Input	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA4 — Analog input to channel 4 of ADCA. After reset, the default state is GPIOA4.
GPIOA5 *(ANA5)*			11	Input/ Output Input	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA5 — Analog input to channel 5 of ADCA. After reset, the default state is GPIOA5.
GPIOA6 *(ANA6)*			10	Input/ Output Input	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA6 — Analog input to channel 5 of ADCA. After reset, the default state is GPIOA6.
GPIOA7 *(ANA7)*			9	Input/ Output Input	Input, internal pullup enabled	Port A GPIO — This GPIO pin can be individually programmed as an input or output pin. ANA7 — Analog input to channel 7 of ADCA. After reset, the default state is GPIOA7.

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOB0 *(ANB0& CMPB_P2)*	15	17	24	Input/ Output Input	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB0 and CMPB_P2 — Analog input to channel 0 of ADCB and positive input 2 of analog comparator B. When used as an analog input, the signal goes to ANB0 and CMPB_P2. After reset, the default state is GPIOB0.
GPIOB1 *(ANB1& CMPB_M0)*	16	18	25	Input/ Output Input	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB1 and CMPB_M0— Analog input to channel 1 of ADCB and negative input 0 of analog comparator B. When used as an analog input, the signal goes to ANB1 and CMPB_M0. After reset, the default state is GPIOB1.
GPIOB2 *(ANB2& VREFHB& CMPC_P2)*	18	20	27	Input/ Output Input	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB2 and VREFHB and CMPC_P2 — Analog input to channel 2 of ADCB and analog references high of ADCB and positive input 2 of analog comparator C. When used as an analog input, the signal goes to ANB2 and VREFHB and CMPC_P2. ADC control register configures this input as ANB2 or VREFHB. After reset, the default state is GPIOB2.
GPIOB3 *(ANB3& VREFLB& CMPC_M0)*	19	21	28	Input/ Output Input	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB3 and VREFLB and CMPC_M0 — Analog input to channel 3 of ADCB and analog references low of ADCB and negative input 0 of analog comparator C. When used as an analog input, the signal goes to ANB3 and VREFLB and MPC_M0. ADC control register configures this input as ANB3 or VREFLB. After reset, the default state is GPIOB3.

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOB4 *(ANB4& CMPC_M1)*		14	21	Input/ Output Input	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB4 and CMPC_M1 — Analog input to channel 4 of ADCB and negative input 1 of analog comparator C. After reset, the default state is GPIOB4.
GPIOB5 *(ANB5& CMPC_M2)*			20	Input/ Output Input	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB5 and CMPC_M2 — Analog input to channel 5 of ADCB and negative input 2 of analog comparator C. After reset, the default state is GPIOB5.
GPIOB6 *(ANB6& CMPB_M1)*			19	Input/ Output Input	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB6 and CMPB_M1 — Analog input to channel 6 of ADCB and negative input 1 of analog comparator B. After reset, the default state is GPIOB6.
GPIOB7 *(ANB7& CMPB_M2)*			17	Input/ Output Input	Input, internal pullup enabled	Port B GPIO — This GPIO pin can be individually programmed as an input or output pin. ANB7 and CMPB_M2 — Analog input to channel 7 of ADCB and negative input 2 of analog comparator B. After reset, the default state is GPIOB7.
GPIOC0 *XTAL* *CLKIN*	3	3	3	Input/ Output Analog Output Input	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. XTAL — External Crystal Oscillator Output. This output connects the internal crystal oscillator output to an external crystal or ceramic resonator. CLKIN — This pin serves as an external clock input.[1] After reset, the default state is GPIOC0.
GPIOC1 *(EXTAL)*	4	4	4	Input/ Output Analog Input	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. EXTAL — External Crystal Oscillator Input. This input connects the internal crystal oscillator input to an external crystal or ceramic resonator. After reset, the default state is GPIOC1.

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOC2	5	5	5	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(TXD0)				Output		TXD0 — The SCI0 transmit data output or transmit/receive in single wire operation.
(TB0)				Input/ Output		TB0 — Quad timer module B channel 0 input/output.
(XB_IN2)				Input		XB_IN2 — Crossbar module input 2
(CLKO)				Output		CLKO — This is a buffered clock output; the clock source is selected by clockout select (CLKOSEL) bits in the clock output select register (CLKOUT) of the SIM. After reset, the default state is GPIOC2.
GPIOC3	6	6	7	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(TA0)				Input/ Output		TA0 — Quad timer module A channel 0 input/output.
(CMPA_O)				Output		CMPA_O— Analog comparator A output
(RXD0)				Input		RXD0 — The SCI0 receive data input. After reset, the default state is GPIOC3.
GPIOC4	7	7	8	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(TA1)				Input/ Output		TA1 — Quad timer module A channel 1input/output
(CMPB_O)				Output		CMPB_O — Analog comparator B output After reset, the default state is GPIOC4.
GPIOC5	12	13	18	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(DACO)				Analog Output		DACO — 12-bit Digital-to-Analog Controller output
(XB_IN7)				Input		XB_IN7 — Crossbar module input 7 After reset, the default state is GPIOC5.

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOC6 *(TA2)* *(XB_IN3)* *(CMP_REF)*	21	23	31	Input/ Output Input/ Output Input Analog Input	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. TA2 — Quad timer module A channel 2 input/output XB_IN3 — Crossbar module input 3 CMP_REF— Positive input 3 of analog comparator A and B and C After reset, the default state is GPIOC6
GPIOC7 *($\overline{SS}$)* *(TXD0)*	22	24	32	Input/ Output Input/ Output Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. $\overline{SS}$ — $\overline{SS}$ is used in slave mode to indicate to the SPI module that the current transfer is to be received. TXD0 — SCI0 transmit data output or transmit/receive in single wire operation After reset, the default state is GPIOC7.
GPIOC8 *(MISO)* *(RXD0)*	23	25	33	Input/ Output Input/ Output Input	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. MISO — Master in/slave out. In master mode, this pin serves as the data input. In slave mode, this pin serves as the data output. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected. RXD0 — SCI0 receive data input After reset, the default state is GPIOC8.
GPIOC9 *(SCLK)* *(XB_IN4)*	24	26	34	Input/ Output Input/ Output Input	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. SCLK — The SPI serial clock. In master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input. XB_IN4 — Crossbar module input 4 After reset, the default state is GPIOC9.

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOC10	25	27	35	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(MOSI)				Input/ Output		MOSI — Master out/slave in. In master mode, this pin serves as the data output. In slave mode, this pin serves as the data input.
(XB_IN5)				Input		XB_IN5 — Crossbar module input 5
(MISO)				Input/ Output		MISO — Master in/slave out. In master mode, this pin serves as the data input. In slave mode, this pin serves as the data output. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected. After reset, the default state is GPIOC10.
GPIOC11	26	29	37	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(CANTX)				Open-drain Output		CANTX — CAN transmit data output (not available on 56F8245/46/47)
(SCL1)				Input/ Open-drain Output		SCL1 — I^2C1 serial clock
(TXD1)				Output		TXD1 — SCI1 transmit data output or transmit/receive in single wire operation After reset, the default state is GPIOC11.
GPIOC12	27	30	38	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(CANRX)				Input		CANRX — CAN receive data input (not available on 56F8245/46/47)
(SDA1)				Input/ Open-drain Output		SDA1 — I^2C1 serial data line
(RXD1)				Input		RXD1 — SCI1 receive data input After reset, the default state is GPIOC12.
GPIOC13	34	37	49	Input/ Output	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin.
(TA3)				Input/ Output		TA3 — Quad timer module A channel 3input/output.
(XB_IN6)				Input		XB_IN6 — Crossbar module input 6 After reset, the default state is GPIOC13.

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOC14 *(SDA0)* *(XB_OUT0)*	37	41	55	Input/ Output Input/ Open-drain Output Input	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. SDA0 — I^2C0 serial data line XB_OUT0 — Crossbar module output 0 After reset, the default state is GPIOC14.
GPIOC15 *(SCL0)* *(XB_OUT1)*	38	42	56	Input/ Output Input/ Open-drain Output Input	Input, internal pullup enabled	Port C GPIO — This GPIO pin can be individually programmed as an input or output pin. SCL0 — I^2C0 serial clock XB_OUT1 — Crossbar module output 1 After reset, the default state is GPIOC15.
GPIOE0 *PWM0B*	30	33	45	Input/ Output Input	Input, internal pullup enabled	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM0B — NanoEdge PWM submodule 0 output B After reset, the default state is GPIOE0.
GPIOE1 *(PWM0A)*	31	34	46	Input/ Output Output	Input, internal pullup enabled	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM0A — NanoEdge PWM submodule 0 output B After reset, the default state is GPIOE1.
GPIOE2 *(PWM1B)*	32	35	47	Input/ Output Output	Input, internal pullup enabled	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM1B — NanoEdge PWM submodule 1 output A After reset, the default state is GPIOE2.
GPIOE3 *(PWM1A)*	33	36	48	Input/ Output Output	Input, internal pullup enabled	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM1A — NanoEdge PWM submodule 1 output A After reset, the default state is GPIOE3.

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOE4 *(PWM2B)* *(XB_IN2)*	35	39	51	Input/ Output Output Input	Input, internal pullup enabled	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM2B — NanoEdge PWM submodule 2 output B XB_IN2 — Crossbar module input 2 After reset, the default state is GPIOE4.
GPIOE5 *(PWM2A)* *(XB_IN3)*	36	40	52	Input/ Output Output Input	Input, internal pullup enabled	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM2A — NanoEdge PWM submodule 2 output A XB_IN3 — Crossbar module input 3 After reset, the default state is GPIOE5.
GPIOE6 *(PWM3B)* *(XB_IN4)*			53	Input/ Output Input/ Output Input	Input, internal pullup enabled	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM3B — Enhanced PWM submodule 3 output B or input capture B XB_IN4 — Crossbar module input 4 After reset, the default state is GPIOE6.
GPIOE7 *(PWM3A)* *(XB_IN5)*			54	Input/ Output Input/ Output Input	Input, internal pullup enabled	Port E GPIO — This GPIO pin can be individually programmed as an input or output pin. PWM3A — Enhanced PWM submodule 3 output A or input capture A XB_IN5 — Crossbar module input 5 After reset, the default state is GPIOE7.
GPIOF0 *(XB_IN6)*		28	36	Input/ Output Input	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin. XB_IN6 — Crossbar module input 6 After reset, the default state is GPIOF0.

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOF1		38	50	Input/ Output	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin.
(CLKO)				Output		CLKO — This is a buffered clock output; the clock source is selected by clockout select (CLKOSEL) bits in the clock output select register (CLKOUT) of the SIM.
(XB_IN7)				Input		XB_IN7 — Crossbar module input 7 After reset, the default state is GPIOF1.
GPIOF2			39	Input/ Output	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin.
(SCL1)				Input/ Open-drain Output		SCL1 — The I^2C1 serial clock.
(XB_OUT2)				Output		XB_OUT2 — Crossbar module output 2 After reset, the default state is GPIOF2.
GPIOF3			40	Input/ Output	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin.
(SDA1)				Input/ Open-drain Output		SDA1 — The I^2C1 serial data line.
(XB_OUT3)				Output		XB_OUT3 — Crossbar module output 3 After reset, the default state is GPIOF3.
GPIOF4			41	Input/ Output	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin.
(TXD1)				Output		TXD1 — The SCI1 transmit data output or transmit/receive in single wire operation.
(XB_OUT4)				Output		XB_OUT4 — Crossbar module output 4 After reset, the default state is GPIOF4.
GPIOF5			42	Input/ Output	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin.
(RXD1)				Output		RXD1 — The SCI1 receive data input.
(XB_OUT5)				Output		XB_OUT5 — Crossbar module output 5 After reset, the default state is GPIOF5.

Table 5. MC56F825x/MC56F824x Signal and Package Information (continued)

Signal Name	44 LQFP	48 LQFP	64 LQFP	Type	State During Reset	Signal Description
GPIOF6 *(TB2)* *(PWM3X)*			58	Input/ Output Input/ Output Input/ Output	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin. TB2 — Quad timer module B channel 2 input/output. PWM3X — Enhanced PWM submodule 3 output X or input capture X After reset, the default state is GPIOF6.
GPIOF7 *(TB3)*			59	Input/ Output Input/ Output	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin. TB3 — Quad timer module B channel 3 input/output. After reset, the default state is GPIOF7.
GPIOF8 *(RXD0)* *(TB1)*			6	Input/ Output Input Input/ Output	Input, internal pullup enabled	Port F GPIO — This GPIO pin can be individually programmed as an input or output pin. RXD0 — The SCI0 receive data input. TB1 — Quad timer module B channel 1 input/output. After reset, the default state is GPIOF8.

1 If CLKIN is selected as the device's external clock input, both the GPS_C0 bit in GPS1 and the EXT_SEL bit in the OCCS oscillator control register (OSCTL) must be set. In this case, it is also recommended to power down the crystal oscillator.

4 Memory Maps

4.1 Introduction

The MC56F825x/MC56F824x device is based on the 56800E core. It uses a dual Harvard-style architecture with two independent memory spaces for data and program. On-chip RAM is shared by both data and program spaces; flash memory is used only in program space.

This section provides memory maps for:

- Program address space, including the interrupt vector table
- Data address space, including the EOnCE memory and peripheral memory maps

On-chip memory sizes for the device are summarized in Table 6. Flash memories' restrictions are identified in the "Use Restrictions" column of Table 6.

Table 6. Chip Memory Configurations

On-Chip Memory	56F8245 56F8246	56F8247	56F8255 56F8256 56F8357	Use Restrictions
Program Flash (PFLASH)	24K x 16 or 48 KB	24K x 16 or 48 KB	32K x 16 or 64 KB	Erase/program via flash interface unit and word writes to CDBW
Unified RAM (RAM)	3K x 16 or 6 KB	4K x 16 or 8 KB	4K x 16 or 8 KB	Usable by the program and data memory spaces

4.2 Program Map

The MC56F825x/MC56F824x series provide up to 64 KB on-chip flash memory. It primarily accesses through the program memory buses (PAB; PDB). PAB is used to select program memory addresses; instruction fetches are performed over PDB. Data can be read from and written to the program memory space through the primary data memory buses: CDBW for data write and CDBR for data read. Access time for accessing the program memory space over the data memory buses is longer than for accessing data memory space. The special MOVE instructions are provided to support these accesses. The benefit is that non-time-critical constants or tables can be stored and accessed in program memory.

The program memory map appears in Table 7, Table 8, and Table 9, depending on the device.

Table 7. Program Memory Map[1] for 56F8255/56/57 at Reset

Begin/End Address	Memory Allocation
P: 0x1F FFFF P: 0x00 8800	RESERVED
P: 0x00 8FFF P: 0x00 8000	On-chip RAM[2]: 8 KB
P: 0x00 7FFF P: 0x00 0000	• Internal program flash: 64 KB • Interrupt vector table locates from 0x00 0000 to 0x00 0085 • COP reset address = 0x00 0002 • Boot location = 0x00 0000

1 All addresses are 16-bit word addresses.

2 This RAM is shared with data space starting at address X: 0x00 0000. See Figure 6.

Table 8. Program Memory Map[1] for 56F82447 at Reset

Begin/End Address	Memory Allocation
P: 0x1F FFFF P: 0x00 8800	RESERVED
P: 0x00 8FFF P: 0x00 8000	On-chip RAM[2]: 8 KB
P: 0x00 7FFF P: 0x00 2000	• Internal program flash: 48 KB • Interrupt vector table locates from 0x00 2000 to 0x00 2085 • COP reset address = 0x00 2002 • Boot location = 0x00 2000
P: 0x00 2000 P: 0x00 0000	RESERVED

1 All addresses are 16-bit word addresses.
2 This RAM is shared with data space starting at address X: 0x00 0000. See Figure 7.

Table 9. Program Memory Map[1] for 56F8245/46 at Reset

Begin/End Address	Memory Allocation
P: 0x1F FFFF P: 0x00 8800	RESERVED
P: 0x00 8BFF P: 0x00 8000	On-chip RAM[2]: 6 KB
P: 0x00 7FFF P: 0x00 2000	• Internal program flash: 48 KB • Interrupt vector table locates from 0x00 2000 to 0x00 2085 • COP reset address = 0x00 2002 • Boot location = 0x00 2000
P: 0x00 2000 P: 0x00 0000	RESERVED

1 All addresses are 16-bit word addresses.
2 This RAM is shared with data space starting at address X: 0x00 0000. See Figure 7.

4.3 Data Map

The MC56F825x/MC56F824x series contains dual access memory. It can be accessed from core primary data buses (XAB1, CDBW, CDBR) and secondary data buses (XAB2, XDB2). Addresses in data memory are selected on the XAB1 and XAB2 buses. Byte, word, and long data transfers occur on the 32-bit CDBR and CDBW buses. A second 16-bit read operation can be performed in parallel on the XDB2 bus.

Peripheral registers and on-chip JTAG/EOnCE controller registers are memory mapped into data memory access. A special direct address mode is supported for accessing a first 64-location in data memory by using a single word instruction.

The data memory map appears in Table 10 and Table 11.

Table 10. 56F8247 and 56F8255/56/57 Data Memory Map[1]

Begin/End Address	Memory Allocation
X:0xFF FFFF X:0xFF FF00	EOnCE 256 locations allocated
X:0xFF FEFF X:0x01 0000	RESERVED
X:0x00 FFFF X:0x00 F000	On-chip peripherals 4096 locations allocated
X:0x00 EFFF X:0x00 9000	RESERVED
X:0x00 8FFF X:0x00 8000	On-chip data RAM alias
X:0x00 7FFF X:0x00 1000	RESERVED
X:0x00 0FFF X:0x00 0000	On-chip data RAM 8 KB[2]

1 All addresses are 16-bit word addresses.

[2] This RAM is shared with program space starting at P: 0x00 8000. See Figure 6 and Figure 7.

On-chip RAM is also mapped into program space starting at P: 0x00 8000. This mapping eases online reprogramming of on-chip flash.

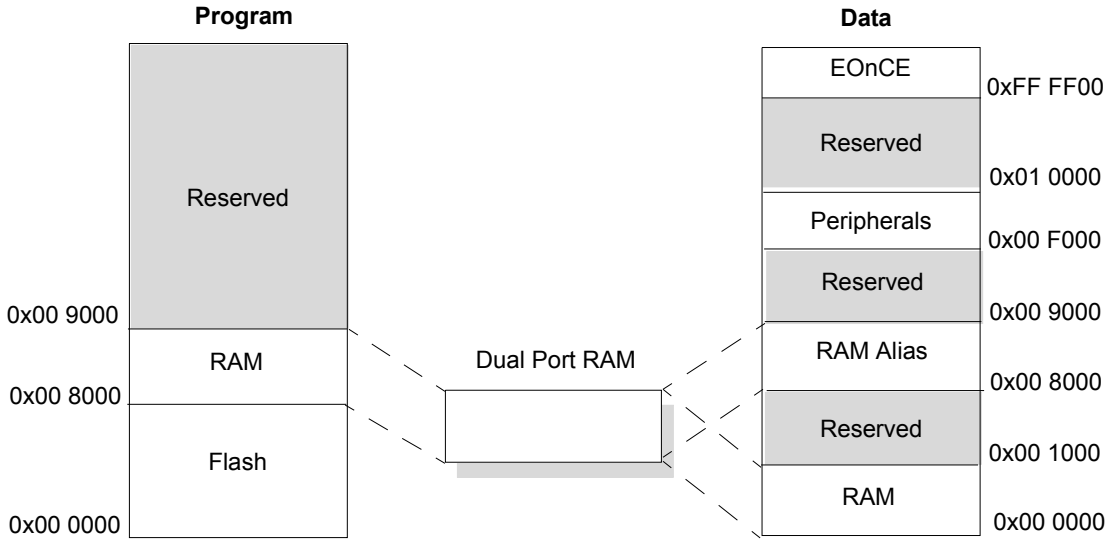


Figure 6. 56F8255/56/57 Dual Port RAM Map

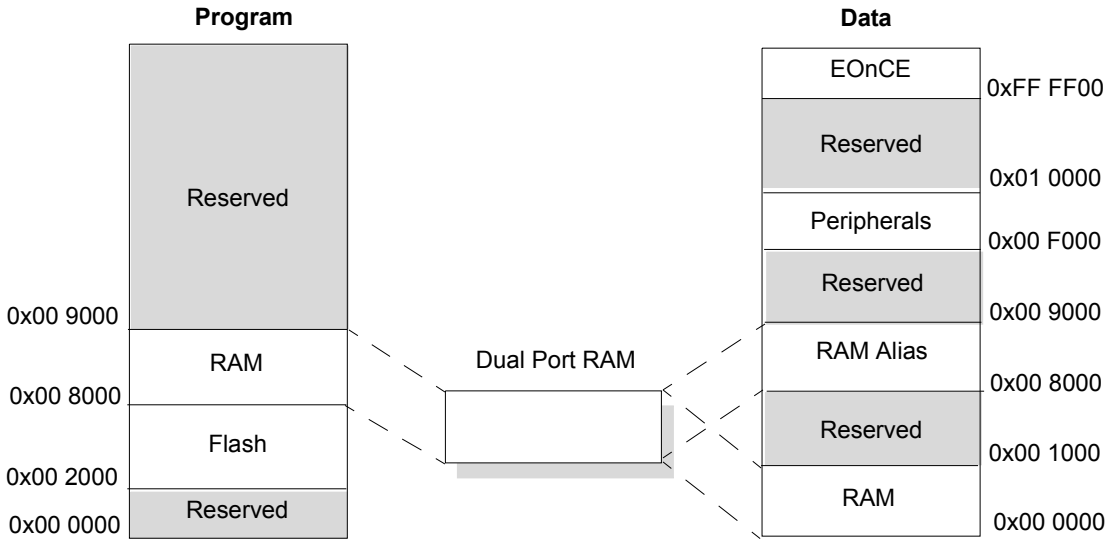


Figure 7. 56F8247 Dual Port RAM Map

Table 11. 56F8245/56 Data Memory Map[1]

Begin/End Address	Memory Allocation
X:0xFF FFFF X:0xFF FF00	EOnCE 256 locations allocated
X:0xFF FEFF X:0x01 0000	RESERVED
X:0x00 FFFF X:0x00 F000	On-Chip Peripherals 4096 locations allocated
X:0x00 EFFF X:0x00 8C00	RESERVED
X:0x00 8BFF X:0x00 8000	On-Chip Data RAM Alias
X:0x00 7FFF X:0x00 0C00	RESERVED
X:0x00 0BFF X:0x00 0000	On-Chip Data RAM 6 KB[2]

1 All addresses are 16-bit word addresses.

2 This RAM is shared with program space starting at P: 0x00 8000. See Figure 8.

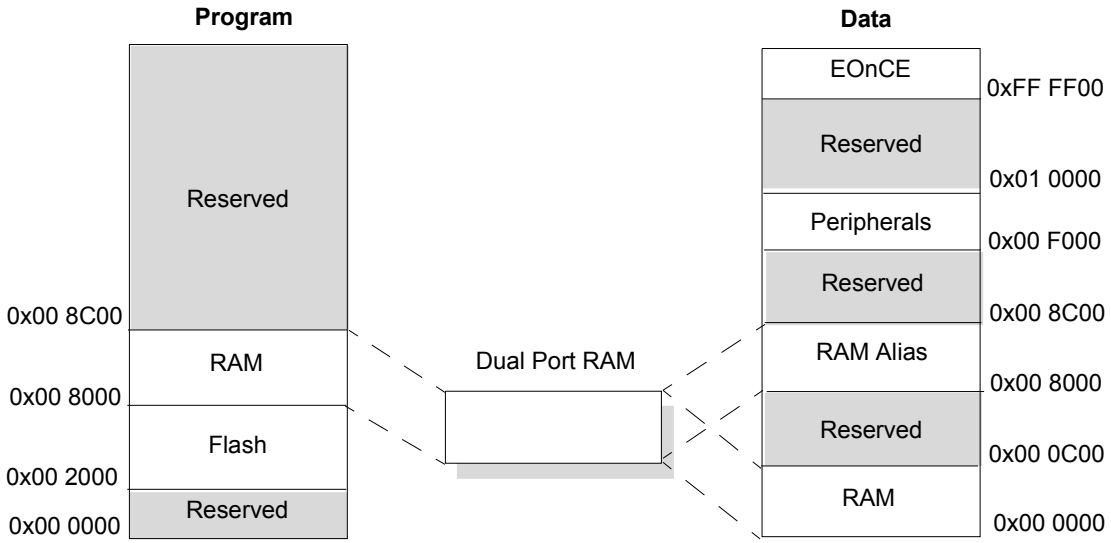


Figure 8. 56F8245/46 Dual Port RAM Map

4.4 Interrupt Vector Table and Reset Vector

The location of the vector table is determined by the vector base address register (VBA). The value in this register is used as the upper 14 bits of the interrupt vector VAB[20:0]. The lower seven bits are determined based on the highest priority interrupt and are then appended to VBA before presenting the full VAB to the core. Refer to the device's reference manual for details.

The reset startup addresses of 56F824x and 56F825x are different.

- The 56F825x's startup address is located at 0x00 0000. The reset value of VBA is reset to a value of 0x0000 that corresponds to the address 0x00 0000.

- The 56F824x's startup address is located at 0x00 2000. The reset value of VBA is reset to a value of 0x0020 that corresponds to the address 0x00 2000.

By default, the chip reset address and COP reset address correspond to vector 0 and 1 of the interrupt vector table. In these instances, the first two locations in the vector table must contain branch or JMP instructions. All other entries must contain JSR instructions.

Table 48 on page 85 provides the MC56F825x/MC56F824x's interrupt table contents and interrupt priority structure.

4.5 Peripheral Memory-Mapped Registers

The locations of on-chip peripheral registers are part of the data memory map on the 56800E series. These locations may be accessed with the same addressing modes used for ordinary data memory. However, all peripheral registers should be read or written using word accesses only.

Table 12 summarizes the base addresses for the set of peripherals on the MC56F825x/MC56F824x devices. Peripherals are listed in order of the base address.

Table 12. Data Memory Peripheral Base Address Map Summary

Peripheral	Prefix	Base Address
Quad Timer A	TMRA	X:0x00 F000
Quad Timer B	TMRB	X:0x00 F040
Analog-to-Digital Converter	ADC	X:0x00 F080
Interrupt Controller	INTC	X:0x00 F0C0
System Integration Module	SIM	X:0x00 F0E0
Crossbar module	XBAR	X:0x00 F100
Computer Operating Properly module	COP	X:0x00 F110
On-Chip Clock Synthesis module	OCCS	X:0x00 F120
Power Supervisor	PS	X:0x00 F130
GPIO Port A	GPIOA	X:0x00 F140
GPIO Port B	GPIOB	X:0x00 F150
GPIO Port C	GPIOC	X:0x00 F160
GPIO Port D	GPIOD	X:0x00 F170
GPIO Port E	GPIOE	X:0x00 F180
GPIO Port F	GPIOF	X:0x00 F190
12-bit Digital-to-Analog Converter	DAC	X:0x00 F1A0
Analog Comparator A	CMPA	X:0x00 F1B0
Analog Comparator B	CMPB	X:0x00 F1C0
Analog Comparator C	CMPC	X:0x00 F1D0
Queued Serial Communication Interface 0	QSCI0	X:0x00 F1E0
Queued Serial Communication Interface 1	QSCI1	X:0x00 F1F0
Queued Serial Peripheral Interface	QSPI	X:0x00 F200
Inter-Integrated Circuit 0	I^2C0	X:0x00 F210
Inter-Integrated Circuit 1	I^2C1	X:0x00 F220

Table 12. Data Memory Peripheral Base Address Map Summary (continued)

Peripheral	Prefix	Base Address
Cyclic Redundancy Check Generator	CRC	X:0x00 F230
Comparator Voltage Reference A	REFA	X:0x00 F240
Comparator Voltage Reference B	REFB	X:0x00 F250
Comparator Voltage Reference C	REFB	X:0x00 F260
Enhanced Flex PWM Module	eFlexPWM	X:0x00 F300
Flash Memory Interface	FM	X:0x00 F400
Freescale Controller Area Network [1]	MSCAN	X:0x00 F440

[1] The core must enable clocks to the Freescale Controller Area Network module prior to accessing MSCAN addresses. For details, refer to the MSCAN chapter of the device's reference manual.

4.6 EOnCE Memory Map

Control registers of the EOnCE are located at the top of data memory space. These locations are fixed by the 56800E core. These registers can also be accessed through the JTAG port if flash security is not set. Table 13 lists all EOnCE registers necessary to access or control the EOnCE.

Table 13. EOnCE Memory Map

Address	Register Abbreviation	Register Name
X:0xFF FFFF	OTX1/ORX1	Transmit Register Upper Word Receive Register Upper Word
X:0xFF FFFE	OTX/ORX (32 bits)	Transmit Register Receive Register
X:0xFF FFFD	OTXRXSR	Transmit and Receive Status and Control Register
X:0xFF FFFC	OCLSR	Core Lock/Unlock Status Register
X:0xFF FFFB– X:0xFF FFA1		Reserved
X:0xFF FFA0	OCR	Control Register
X:0xFF FF9F–X:0xFF FF9E	OSCNTR (24 bits)	Instruction Step Counter
X:0xFF FF9D	OSR	Status Register
X:0xFF FF9C	OBASE	Peripheral Base Address Register
X:0xFF FF9B	OTBCR	Trace Buffer Control Register
X:0xFF FF9A	OTBPR	Trace Buffer Pointer Register
X:0xFF FF99–X:0xFF FF98	OTB (21–24 bits/stage)	Trace Buffer Register Stages
X:0xFF FF97–X:0xFF FF96	OBCR (24 bits)	Breakpoint Unit Control Register
X:0xFF FF95–X:0xFF FF94	OBAR1 (24 bits)	Breakpoint Unit Address Register 1
X:0xFF FF93–X:0xFF FF92	OBAR2 (32 bits)	Breakpoint Unit Address Register 2

Table 13. EOnCE Memory Map

Address	Register Abbreviation	Register Name
X:0xFF FF91–X:0xFF FF90	OBMSK (32 bits)	Breakpoint Unit Mask Register 2
X:0xFF FF8F		Reserved
X:0xFF FF8E	OBCNTR	EOnCE Breakpoint Unit Counter
X:0xFF FF8D		Reserved
X:0xFF FF8C		Reserved
X:0xFF FF8B		Reserved
X:0xFF FF8A	OESCR	External Signal Control Register
X:0xFF FF89 –X:0xFF FF00		Reserved

5 General System Control Information

5.1 Overview

This section discusses power pins, reset sources, interrupt sources, clock sources, the system integration module (SIM), ADC synchronization, and JTAG/EOnCE interfaces.

5.2 Power Pins

V_{DD}, V_{SS} and V_{DDA}, V_{SSA} are the primary power supply pins for the device. The voltage source supplies power to all on-chip peripherals, I/O buffer circuitry, and internal voltage regulators. The device has multiple internal voltages to provide regulated lower-voltage sources for the peripherals, core, memory, and on-chip relaxation oscillators.

Typically, at least two separate capacitors are across the power pins to bypass the glitches and provide bulk charge storage. In this case, a bulk electrolytic or tantalum capacitor, such as a 10 µF tantalum capacitor, should provide bulk charge storage for the overall system, and a 0.1 µF ceramic bypass capacitor should be located as near to the device power pins as is practical to suppress high-frequency noise. Each pin must have a bypass capacitor for optimal noise suppression.

V_{DDA} and V_{SSA} are the analog power supply pins for the device. This voltage source supplies power to the ADC, PGA, and CMP modules. A 0.1 µF ceramic bypass capacitor should be located as near to the device V_{DDA} and V_{SSA} pins as is practical to suppress high-frequency noise. V_{DDA} and V_{SSA} are also the voltage reference high and voltage reference low inputs, respectively, for the ADC module.

5.3 Reset

Resetting the device provides a way to start processing from a known set of initial conditions. During reset, most control and status registers are forced to initial values, and the program counter is loaded from the reset vector. On-chip peripheral modules are disabled and I/O pins are initially configured at the reset status shown in Table 5 on page 18.

The MC56F825x/MC56F824x has the following sources for reset:

- Power-on reset (POR)
- Partial power-down reset (PPD)
- Low-voltage detect (LVD)
- External pin reset (EXTR)
- Computer operating properly loss of reference reset (COP_LOR)
- Computer operating properly time-out reset (COP_CPU)

- Software reset (SWR)

Each of these sources has an associated bit in the reset status register (RSTAT) in the system integration module (SIM).

The external pin reset function is shared with a GPIO port A7 on the $\overline{\text{RESET}}$/GPIOA7 pin. The reset function is enabled following any reset of the device. Bit 7 of the GPIOA_PER register must be cleared to use this pin as a GPIO port pin. When the pin is enabled as the $\overline{\text{RESET}}$ pin, an internal pullup device is automatically enabled.

5.4 On-chip Clock Synthesis

The on-chip clock synthesis (OCCS) module allows designers using an internal relaxation oscillator, an external crystal, or an external clock to run 56F8000 family devices at user-selectable frequencies up to 60 MHz.

The features of OCCS module include:

- Ability to power down the internal relaxation oscillator or crystal oscillator
- Ability to put the internal relaxation oscillator into standby mode
- Ability to power down the PLL
- Provides a 2x system clock that operates at two times the system clock to the timer and SCI modules
- Safety shutdown feature if the PLL reference clock is lost
- Ability to be driven from an external clock source

The clock generation module provides the programming interface for the PLL, internal relaxation oscillator, and crystal oscillator. It also provides a postscaler to divide clock frequency down by 1, 2, 4, 8, 16, 32, 64, 128, or 256 before feeding it to the SIM. The SIM is responsible for further dividing these frequencies by 2, which ensures a 50% duty cycle in the system clock output. For details, refer to the OCCS section of the device's reference manual.

5.4.1 Internal Clock Source

When an external frequency source or crystal is not used, an internal relaxation oscillator can supply the reference frequency. It is optimized for accuracy and programmability while providing several power-saving configurations that accommodate different operating conditions. The internal relaxation oscillator has little temperature and voltage variability. To optimize power, the internal relaxation oscillator supports a run state (8 MHz), standby state (400 kHz), and a power-down state.

During a boot or reset sequence, the relaxation oscillator is enabled by default (the PRECS bit in the PLLCR word is set to 0). Application code can then also switch to the external clock source and power down the internal oscillator, if desired. If a changeover between internal and external clock sources is required at power-on, ensure that the clock source is not switched until the desired external clock source is enabled and stable.

To compensate for variances in the device manufacturing process, the accuracy of the relaxation oscillator can be incrementally adjusted to within + 0.078% of 8 MHz by trimming an internal capacitor. Bits 0–9 of the oscillator control (OSCTL) register allow you to set an additional offset (trim) to this preset value to increase or decrease capacitance. Each unit added or subtracted changes the output frequency by about 0.078% of 8 MHz, allowing incremental adjustment until the desired frequency accuracy is achieved.

The center frequency of the internal oscillator is calibrated at the factory to 8 MHz, and the TRIM value is stored in the flash information block and loaded to the HFM IFR option register 0 at reset. When using the relaxation oscillator, the boot code should read the HFM IFR option register 0 and set this value as OSCTL TRIM. For further information, refer to the device's reference manual.

5.4.2 Crystal Oscillator/Ceramic Resonator

The internal crystal oscillator circuit is designed to interface with a parallel-resonant crystal resonator in the frequency range, specified for the external crystal, of 4 MHz to 16 MHz. A ceramic resonator can be substituted for the 4 MHz to 16 MHz range. When used to supply a source to the internal PLL, the recommended crystal/resonator is in the 8 MHz to 16 MHz range to optimize PLL performance. Oscillator circuits appear in Figure 9 and Figure 10. Follow the crystal supplier's recommendations

when selecting a crystal, because crystal parameters determine the component values required to provide maximum stability and reliable startup. The load capacitance values used in the oscillator circuit design should include all stray layout capacitances. The crystal and associated components should be mounted as near as possible to the EXTAL and XTAL pins to minimize output distortion and startup stabilization time. When using low-frequency, low-power mode, the only external component is the crystal itself. In the other oscillator modes, load capacitors (C_x, C_y) and feedback resistor (R_F) are required. In addition, a series resistor (R_S) may be used in high-gain modes. Recommended component values appear in Table 27.

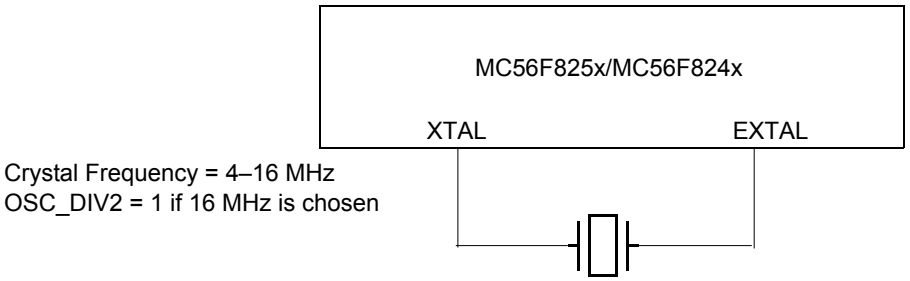


Figure 9. Typical Crystal Oscillator Circuit without Frequency Compensation Capacitor

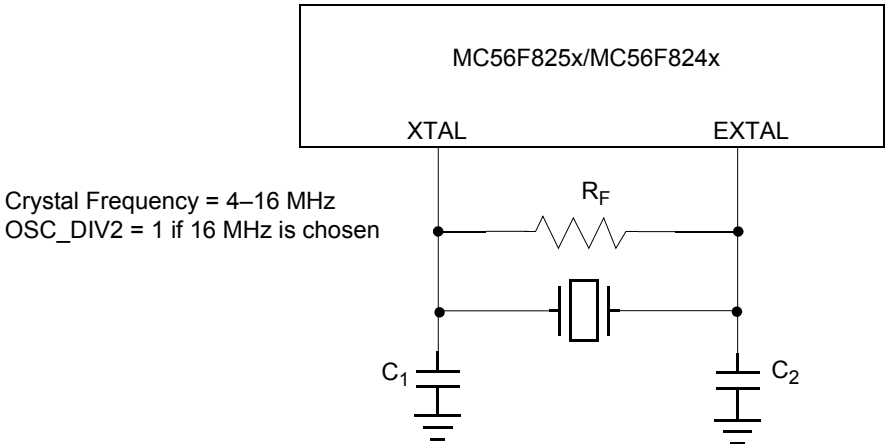


Figure 10. Typical Crystal or Ceramic Resonator Circuit

5.4.3 Alternate External Clock Input

The recommended method of connecting an external clock appears in Figure 11. The external clock source is connected to the CLKIN pin while:

- both the EXT_SEL bit and the CLK_MODE bit in the OSCTL register are set, and
- corresponding bits in the GPIOB_PER register in the GPIO module and the GPS_C0 bit in the GPS0 register in the system integration module (SIM) are set to the correct values.

The external clock input must be generated using a relatively low-impedance driver with a maximum frequency not greater than 120 MHz.

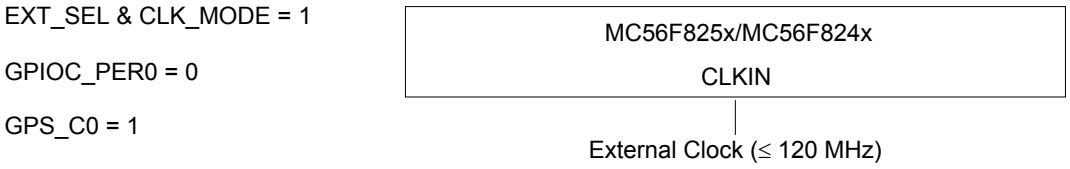


Figure 11. Connecting an External Clock Signal Using GPIO

5.5 Interrupt Controller

The MC56F825x/MC56F824x interrupt controller (INTC) module arbitrates the various interrupt requests (IRQs). When an interrupt of sufficient priority exists, the INTC signals to the 56800E core and provides the address to which to jump to service the interrupt.

The interrupt controller contains registers that allow each of the 66 interrupt sources to be set to one of three priority levels (excluding certain interrupt sources that have fixed priority) or to be disabled. Next, all interrupt requests of a given level are priority encoded to determine the lowest numeric value of the active interrupt requests for that level. Within a given priority level, the lowest vector number is the highest priority, and the highest vector number is the lowest priority.

Any two interrupt sources can be assigned to faster interrupts. Fast interrupts are described in the *DSP56800E Reference Manual*. The interrupt controller recognizes fast interrupts before the core does.

A fast interrupt is defined by:

1. Setting the priority of the interrupt as level 2 with the appropriate field in the Interrupt Priority Register (IPR) registers
2. Setting the Fast Interrupt Match (FIM*n*) register to the appropriate vector number
3. Setting the Fast Interrupt Vector Address Low (FIVAL*n)* and Fast Interrupt Vector Address High (FIVAH*n)* registers with the address of the code for the fast interrupt

When an interrupt occurs, its vector number is compared with the FIM0 and FIM1 register values. If a match occurs, and it is a level 2 interrupt, the INTC handles it as a Fast Interrupt. The INTC takes the vector address from the appropriate FIVAL*n* and FIVAH*n* registers, instead of generating an address that is an offset from the VBA.

The core then fetches the instruction from the indicated vector address instead of jumping to the vector table. If the instruction is not a JSR, the core starts its fast interrupt handling. Refer to section 9.3.3.3 of *DSP56800E 16-Bit Core Reference Manual* for details.

Table 48 on page 85 provides the MC56F825x/MC56F824x's interrupt table contents and interrupt priority structure.

5.6 System Integration Module (SIM)

The SIM module consists of the glue logic that ties together the system-on-a-chip. It controls distribution of resets and clocks and provides a number of control features, including pin muxing control, inter-module connection control (such as connecting comparator output to eFlexPWM fault input), individual peripheral enabling/disabling, clock rate control for quad timers and SCIs, enabling peripheral operation in stop mode, and port configuration overwrite protection. For more information, refer to the device's reference manual.

The SIM is responsible for the following functions:

- Chip reset sequencing
- Core and peripheral clock control and distribution
- Stop/wait mode control
- System status control
- Registers containing the JTAG ID of the chip
- Controls for programmable peripheral and GPIO connections

- Peripheral clocks for Quad Timers and SCIs with a high-speed (2x) option
- Power-saving clock gating for peripherals
- Controls for enabling/disabling functions of large regulator standby mode with write protection capability
- Allowing selected peripherals to run in stop mode to generate stop recovery interrupts
- Controls for programmable peripheral and GPIO connections
- Software chip reset
- I/O short address base location control
- Peripheral protection control to provide runaway code protection for safety-critical applications
- Controls for output of internal clock sources to CLKO pin
- Four general-purpose software control registers that are reset only at power-on
- Peripheral stop mode clocking control

5.7 Inter-Module Connections

The operations between on-chip peripherals can be synchronized or cascaded through internal module connections to support particular applications. Examples include synchronization between ADC sampling and PWM waveform generation for a power conversion application, and synchronization between timer pulse outputs and DAC waveform generation for a printer application. The user can program the internal Crossbar Switch or Comparator input multiplexes to connect one on-chip peripheral's outputs to other peripherals' inputs.

5.7.1 Comparator Connections

The MC56F825x/MC56F824x includes three high-speed comparators. Each comparator input has a 4-to-1 input mux, allowing it to sample a variety of analog sources. Some of these inputs share package pins with the on-chip ADCs; see Table 5 on page 18.

Each comparator is paired with a dedicated, programmable, 5-bit on-chip voltage reference DAC (VREF_DAC). Optionally, an on-chip 12-bit DAC can be internally fed to each comparator's positive input 1 (CMPn_P1) or negative input 3 (CMPn_M3). In addition, all three comparators' positive input 3 (CMPn_P3) can be connected together to package pin CMP_REF. Other inputs can be routed to package pins when the corresponding pin is configured for peripheral mode in the GPIO module.

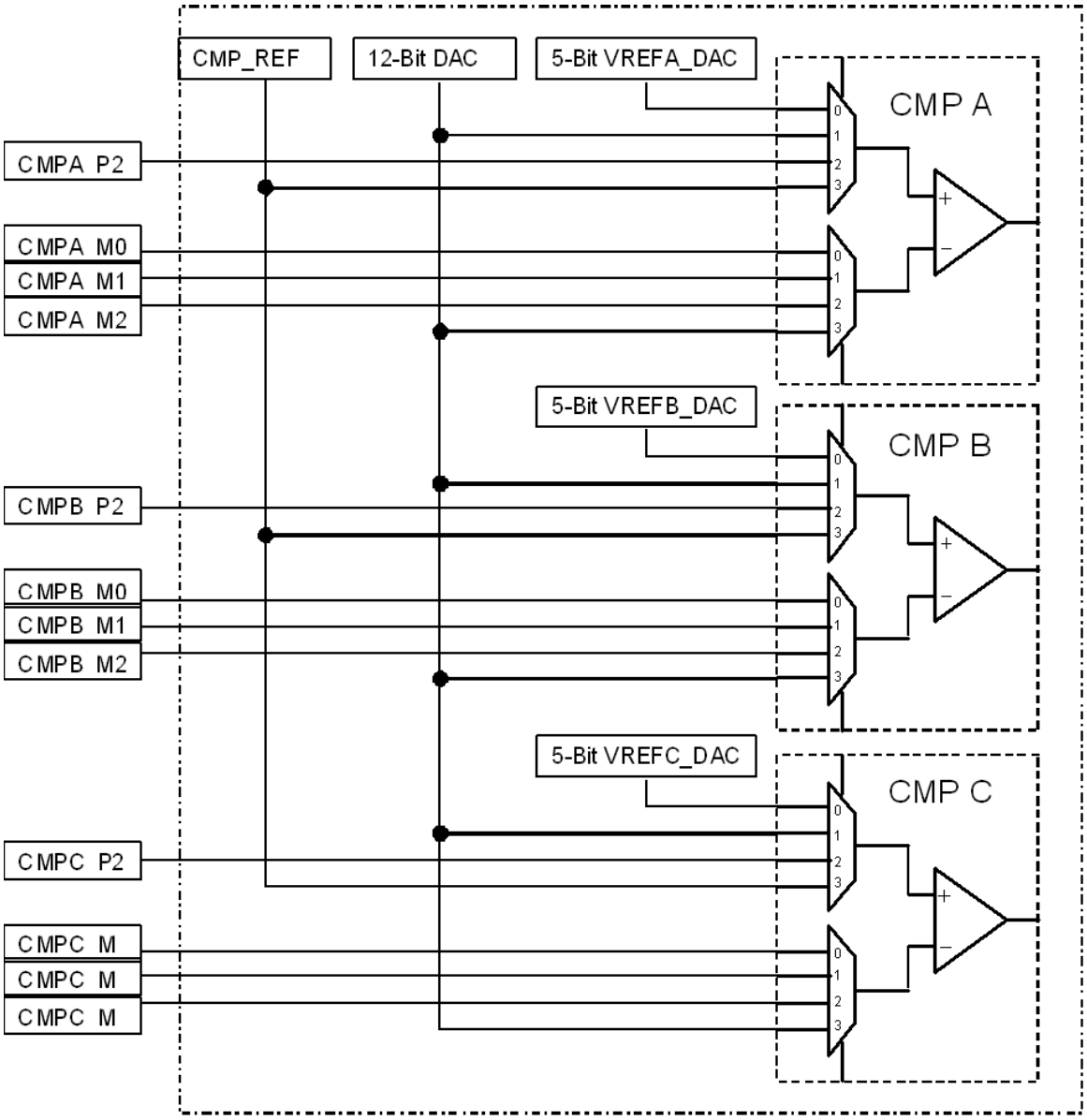


Figure 12. On-Chip Comparator Connections

Table 14. Connections by Comparator Inputs

Comparator Input	Comparator A	Comparator B	Comparator B
P0 (from internal)	5-bit VREFA_DAC	5-bit VREFB_DAC	5-bit VREFC_DAC
P1 (from internal)	12-bit DAC	12-bit DAC	12-bit DAC
P2 (from package pin)	CMPA_P2	CMPB_P2	CMPC_P2
P3 (from package pin)	CMP_REF	CMP_REF	CMP_REF

Table 14. Connections by Comparator Inputs (continued)

Comparator Input	Comparator A	Comparator B	Comparator B
M0 (from package pin)	CMPA_M0	CMPB_M0	CMPC_M0
M1 (from package pin)	CMPA_M1	CMPB_M1	CMPC_M1
M2 (from package pin)	CMPA_M2	CMPB_M2	CMPC_M2
M3 (from internal)	12-bit DAC	12-bit DAC	12-bit DAC

5.7.2 Crossbar Switch Connections

The Crossbar Switch module provides a generic mechanism for making connections between on-chip peripherals as well as between peripherals and pins. It provides a purely combinational path from input to output. The module groups 30 identical multiplexes with 22 shared inputs. All Crossbar control registers that are used to select one of the 22 input signals to output are write protected. Control of the write protection setting is in the SIM_PROT register.

In general, the crossbar module connects the Enhanced Flex PWM, ADC, Quad Timers, and comparators together, which allows synchronization between PWM pulse generation and ADC sampling. In addition, several crossbar inputs and outputs are routed to package pins. For example, the user can define an XB_INn pin as a PWM fault protection input that is routed to the PWM module through the crossbar, increasing the flexibility of pin use and reducing the complexity of PCB layout.

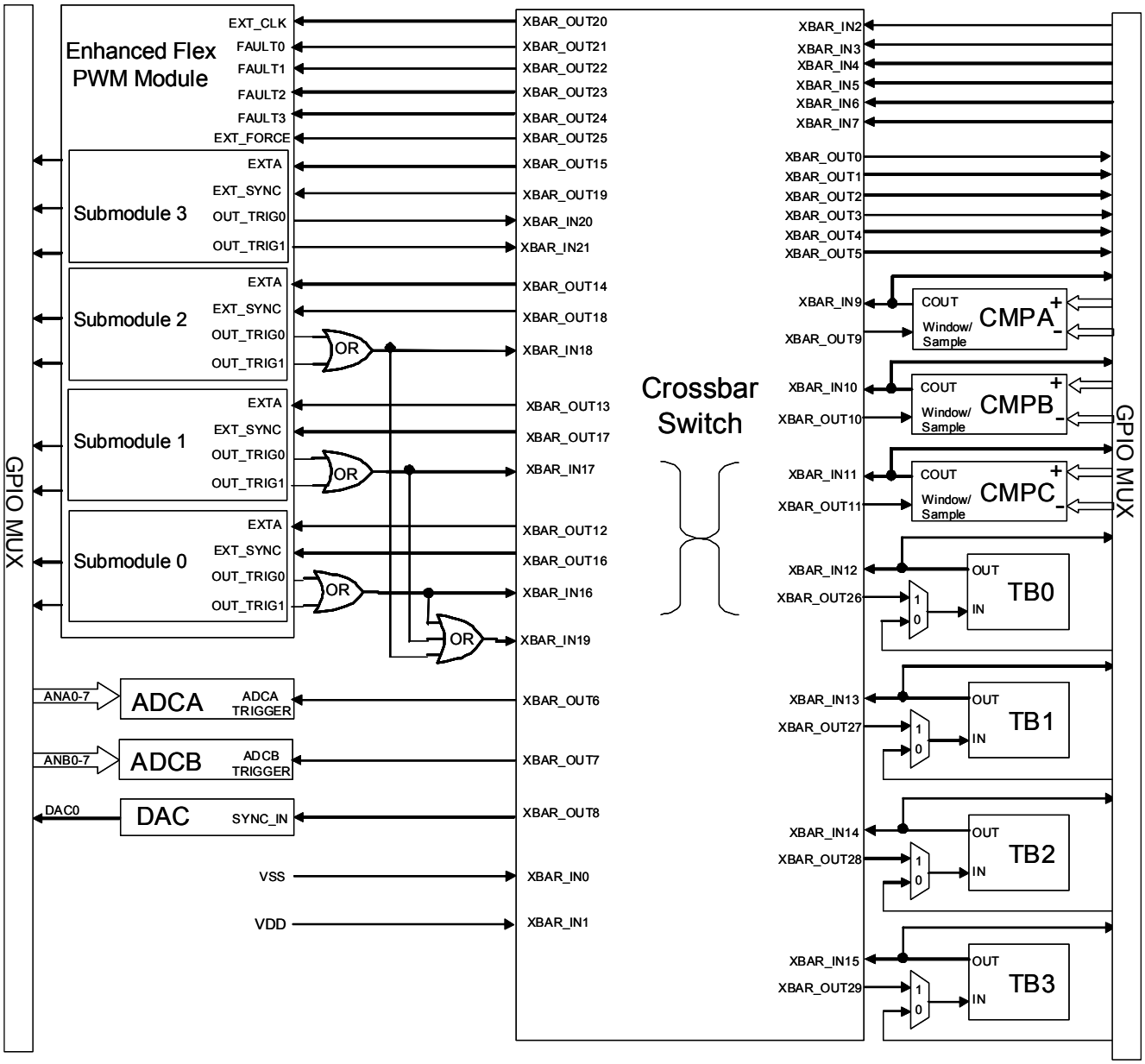


Figure 13. Crossbar Switch Connections

5.7.2.1 Crossbar Switch Inputs

Table 15 lists the signal assignments of Crossbar Switch inputs.

Table 15. Crossbar Input Signal Assignments

XBAR_INn	Input from	Function
XBAR_IN0	Logic Zero	V_{SS}
XBAR_IN1	Logic One	V_{DD}
XBAR_IN2	XB_IN2	Package pin
XBAR_IN3	XB_IN3	Package pin
XBAR_IN4	XB_IN4	Package pin
XBAR_IN5	XB_IN5	Package pin
XBAR_IN6	XB_IN6	Package pin
XBAR_IN7	XB_IN7	Package pin
XBAR_IN8	Unused	
XBAR_IN9	CMPA_OUT	Comparator A Output
XBAR_IN10	CMPB_OUT	Comparator B Output
XBAR_IN11	CMPC_OUT	Comparator C Output
XBAR_IN12	TB0	Quad Timer B0 Output
XBAR_IN13	TB1	Quad Timer B1 Output
XBAR_IN14	TB2	Quad Timer B2 Output
XBAR_IN15	TB3	Quad Timer B3 Output
XBAR_IN16	PWM0_TRIG_COMB	eFlexPWM submodule 0: PWM0_OUT_TRIG0 or PWM0_OUT_TRIG1
XBAR_IN17	PWM1_TRIG_COMB	eFlexPWM submodule 1: PWM1_OUT_TRIG0 or PWM1_OUT_TRIG1
XBAR_IN18	PWM2_TRIG_COMB	eFlexPWM submodule 2: PWM2_OUT_TRIG0 or PWM2_OUT_TRIG1
XBAR_IN19	PWM[012]_TRIG_COMB	eFlexPWM submodule 0, 1, or 2; PWM0_TRIG_COMB or PWM1_TRIG_COMB or PWM2_TRIG_COMB
XBAR_IN20	PWM3_TRIG0	eFlexPWM submodule 3: PWM3_OUT_TRIG0
XBAR_IN21	PWM3_TRIG1	eFlexPWM submodule 3: PWM3_OUT_TRIG1

5.7.2.2 Crossbar Switch Outputs

Table 16 lists the signal assignments of Crossbar Switch outputs.

Table 16. Crossbar Output Signal Assignments

XBAR_OUTn	Output to	Function
XBAR_OUT0	XB_OUT0	Package pin
XBAR_OUT1	XB_OUT1	Package pin
XBAR_OUT2	XB_OUT2	Package pin
XBAR_OUT3	XB_OUT3	Package pin
XBAR_OUT4	XB_OUT4	Package pin
XBAR_OUT5	XB_OUT5	Package pin
XBAR_OUT6	ADCA	ADCA Trigger

Table 16. Crossbar Output Signal Assignments (continued)

XBAR_OUTn	Output to	Function
XBAR_OUT7	ADCB	ADCB Trigger
XBAR_OUT8	DAC	12-bit DAC SYNC_IN
XBAR_OUT9	CMPA	Comparator A Window/Sample
XBAR_OUT10	CMPB	Comparator B Window/Sample
XBAR_OUT11	CMPC	Comparator C Window/Sample
XBAR_OUT12	PWM0 EXTA	eFlexPWM submodule 0 Alternate Control signal
XBAR_OUT13	PWM1 EXTA	eFlexPWM submodule 1 Alternate Control signal
XBAR_OUT14	PWM2 EXTA	eFlexPWM submodule 2 Alternate Control signal
XBAR_OUT15	PWM3 EXTA	eFlexPWM submodule 3 Alternate Control signal
XBAR_OUT16	PWM0 EXT_SYNC	eFlexPWM submodule 0 External Synchronization signal
XBAR_OUT17	PWM1 EXT_SYNC	eFlexPWM submodule 1 External Synchronization signal
XBAR_OUT18	PWM2 EXT_SYNC	eFlexPWM submodule 2 External Synchronization signal
XBAR_OUT19	PWM3 EXT_SYNC	eFlexPWM submodule 3 External Synchronization signal
XBAR_OUT20	PWM EXT_CLK	eFlexPWM External Clock signal
XBAR_OUT21	PWM FAULT0	eFlexPWM Module FAULT0
XBAR_OUT22	PWM FAULT1	eFlexPWM Module FAULT1
XBAR_OUT23	PWM FAULT2	eFlexPWM Module FAULT2
XBAR_OUT24	PWM FAULT3	eFlexPWM Module FAULT3
XBAR_OUT25	PWM FORCE	eFlexPWM External Output Force signal
XBAR_OUT26	TB0	Quad Timer B0 Input when SIM_GPS3[12] is set
XBAR_OUT27	TB1	Quad Timer B1 Input when SIM_GPS3[13] is set
XBAR_OUT28	TB2	Quad Timer B2 Input when SIM_GPS3[14] is set
XBAR_OUT29	TB3	Quad Timer B3 Input when SIM_GPS3[15] is set

5.7.3 Interconnection of PWM Module and ADC Module

In addition to how PWM0_EXTA, PWM1_EXTA, PWM2_EXTA, and PWM3_EXTA connect to crossbar outputs, the ADC conversion high/low limit compare results of sample0, sample1, and sample2 are used to drive PWM0_EXTB, PWM1_EXTB, and PWM2_EXTB, respectively. PWM3_EXTB is permanently tied to GND.

State of PWM0_EXTB:

- If the ADC conversion result in SAMPLE0 is greater than the value programmed into the high limit register 0, PWM0_EXTB is driven low.
- If the ADC conversion result in SAMPLE0 is less than the value programmed into the low limit register 0, PWM0_EXTB is driven high.

State of PWM1_EXTB:

- If the ADC conversion result in SAMPLE1 is greater than the value programmed into the high limit register 1, PWM1_EXTB is driven low.

- If the ADC conversion result in SAMPLE1 is less than the value programmed into the low limit register 1, PWM1_EXTB is driven high.

State of PWM2_EXTB:

- If the ADC conversion result in SAMPLE2 is greater than the value programmed into the high limit register 2, PWM2_EXTB is driven low.
- If the ADC conversion result in SAMPLE2 is less than the value programmed into the low limit register 2, PWM2_EXTB is driven high.

5.8 Joint Test Action Group (JTAG)/Enhanced On-Chip Emulator (EOnCE)

The 56800E family includes extensive integrated support for application software development and real-time debugging. Two modules, the Enhanced On-Chip Emulation (EOnCE) module and the core test access port (TAP, commonly called the JTAG port), work together to provide these capabilities. Both are accessed through a common 4-pin JTAG/EOnCE interface. These modules allow you to insert the MC56F825x/MC56F824x into a target system while retaining debug control. This capability is especially important for devices without an external bus, because it eliminates the need for a costly cable to bring out the footprint of the chip, as is required by a traditional emulator system.

The 56800E's EOnCE module is a Freescale-designed module for developing and debugging application software used with the chip. This module allows non-intrusive interaction with the CPU and is accessible through the pins of the JTAG interface or by software program control of the 56800E core. Among the many features of the EOnCE module is support, in real-time program execution, for data communication between the controller and the host software development and debug systems. Other features allow for hardware breakpoints, the monitoring and tracking of program execution, and the ability to examine and modify the contents of registers, memory, and on-chip peripherals, all in a special debug environment. No user-accessible resources must be sacrificed to perform debugging operations.

The 56800E's JTAG port provides an interface for the EOnCE module to the JTAG pins. The Joint Test Action Group (JTAG) boundary scan is an IEEE 1149.1 standard methodology enabling access to test features using a test access port (TAP). A JTAG boundary scan consists of a TAP controller and boundary scan registers. Contact your Freescale sales representative or authorized distributor for device-specific BSDL information.

NOTE

In normal operation, an external pullup on the TMS pin is highly recommend to place the JTAG state machine in reset state (if this pin is not configured as GPIO).

6 Security Features

The MC56F825x/MC56F824x offers security features intended to prevent unauthorized users from gaining access to and reading the contents of the flash memory (FM) array. The MC56F825x/MC56F824x's flash memory security consists of several hardware interlocks.

After flash memory security is set, the application software can allow an authorized user to access on-chip memory by including a user-defined software subroutine that reads and transfers the contents of internal memory via peripherals. This application software can communicate over a serial port, for example, to validate the authenticity of the requested access and then to grant it until the next device reset. The system designer must use discretion when deciding whether to support this type of "back door" access technique.

6.1 Operation with Security Enabled

After you have programmed flash with the application code, or as part of programming the flash with the application code, you can secure the MC56F825x/MC56F824x by programming the values 1 and 0 into bits 1 and 0, respectively, of program memory location 0x00_7FF7. The CodeWarrior IDE menu flash lock command can also accomplish this task. The nonvolatile security

word ensures that the device remains secure after the next reset (caused, for example, by the device powering down). Refer to the flash memory section of the device's reference manual for details.

When flash security mode is enabled, the MC56F825x/MC56F824x disables the core's EOnCE debug capabilities. Normal program execution is otherwise unaffected.

6.2 Flash Access Lock and Unlock Mechanisms

Several methods effectively lock or unlock the on-chip flash.

6.2.1 Disabling EOnCE Access

You can read on-chip flash by issuing commands across the EOnCE port, which is the debug interface for the 56800E core. The TCK, TMS, TDO, and TDI pins compose a JTAG interface onto which the EOnCE port functionality is mapped. When the device boots, the chip-level JTAG port is active and provides the chip's boundary scan capability and access to the ID register. However, proper implementation of flash security blocks any attempt to access the internal flash memory via the EOnCE port when security is enabled. This protection is effective when the device comes out of reset, even prior to the execution of any code at startup.

6.2.2 Flash Lockout Recovery Using JTAG

If the device is secured, one lockout recovery mechanism is the complete erasure of the internal flash contents, including the configuration field. The erasure disables security by clearing the protection register. This approach does not compromise security. The entire contents of your secured code stored in flash are erased before the next reset or power-up sequence, when security becomes disabled.

To start the lockout recovery sequence via JTAG, first shift the JTAG public instruction (LOCKOUT_RECOVERY) into the chip-level TAP controller's instruction register. Then shift the clock divider value into the corresponding 7-bit data register. Finally, the TAP controller must enter the RUN-TEST/IDLE state for the lockout sequence to commence. The controller must remain in this state until the erase sequence is complete. Refer to the device's reference manual for details, or contact Freescale.

NOTE

After completion of the lockout recovery sequence, you must reset the JTAG TAP controller and the device to return to normal unsecured operation. A power-on reset resets both.

6.2.3 Flash Lockout Recovery Using CodeWarrior

You can use CodeWarrior to unlock a device by selecting the following items in the indicated sequence:

1. Debug menu
2. DSP56800E
3. Unlock Flash

You can accomplish the same task with another CodeWarrior mechanism that uses the device's memory configuration file: the command "Unlock_Flash_on_Connect 1" in the .cfg file.

This lockout recovery mechanism completely erases the internal flash contents, including the configuration field, thereby disabling security (the protection register is cleared).

6.2.4 Flash Lockout Recovery without Mass Erase

6.2.4.1 Without Presenting Back Door Access Keys to the Flash Unit

A user can unsecure a secured device by programming the word 0x0000 into program flash location 0x00 7FF7. After completing the programming, the JTAG TAP controller and the device must be reset to return to normal unsecured operation.

The user is responsible for directing the device to invoke the flash programming subroutine to reprogram the word 0x0000 into program flash location 0x00 7FF7. You can do so, for example, by toggling a specific pin or downloading a user-defined key through serial interfaces.

NOTE

Flash contents can be programmed only from ones to zeroes.

6.2.4.2 Presenting Back Door Access Key to the Flash Unit

The user can temporarily bypass security through a “back door” access scheme, using a four-word key to temporarily unlock the flash. “Back door” access requires support from the embedded software. This software would typically permit an external user to enter the four-word code through one of the communications interfaces and then use it to attempt the unlock sequence. If the input matches the four-word code stored at location 0x00 7FFC–0x00 7FFF in the flash memory, the device immediately becomes unsecured (at runtime) and internal memory is accessible via the JTAG/EOnCE port. Refer to the device’s reference manual for details. The key must be entered in four consecutive accesses to the flash, so this routine should be designed to run in RAM.

6.3 Product Analysis

To analyze a product’s failures in the field, the recommended method of unsecuring a secured device appears in Section 6.2.4.2, “Presenting Back Door Access Key to the Flash Unit.” The customer must supply technical-support details about the protocol to access the subroutines in flash memory. An alternative method for performing analysis on a secured device is to mass-erase and reprogram the flash memory with the original code, but also to modify or not program the security word.

7 Specifications

7.1 General Characteristics

The MC56F825x/MC56F824x is fabricated in high-density, low-power, low-leakage CMOS process with 5 V–tolerant, TTL-compatible digital inputs. The term *5 V–tolerant* refers to the capability of an I/O pin, built on a 3.3 V–compatible process technology, to withstand a voltage up to 5.5 V without damaging the device. Many systems have a mixture of devices designed for 3.3 V and 5 V power supplies. In such systems, a bus may carry both 3.3 V–compatible and 5 V–compatible I/O voltage levels (a standard 3.3 V I/O is designed to receive a maximum voltage of 3.3 V ± 10% during normal operation without causing damage). This 5 V–tolerant capability therefore combines the power savings of 3.3 V I/O levels with the ability to receive 5 V levels without damage.

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

7.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed.

CAUTION

Stress beyond the limits specified in Table 17 may affect device reliability or cause permanent damage to the device.

Unless otherwise stated, all specifications within this section apply over the ambient temperature range (–40 ºC to +105 ºC for V temperature devices or –40 ºC to +125 ºC for M temperature devices) over the following supply ranges:
$V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0$ V to 3.6 V, CL $\leq$ 50 pF, $f_{OP} = 60$ MHz.

For functional operating conditions, refer to the remaining tables in the section.

Table 17. Absolute Maximum Ratings (V_{SS} = 0 V, V_{SSA} = 0 V)

Characteristic		Symbol	Notes	Min	Max	Unit
Supply Voltage Range		V_{DD}		–0.3	4.0	V
Analog Supply Voltage Range		V_{DDA}		–0.3	4.0	V
ADC High Voltage Reference		V_{REFHx}		–0.3	4.0	V
Voltage difference V_{DD} to V_{DDA}		ΔV_{DD}		–0.3	0.3	V
Voltage difference V_{SS} to V_{SSA}		ΔV_{SS}		–0.3	0.3	V
Digital Input Voltage Range		V_{IN}	Pin Groups 1, 2	–0.3	6.0	V
Oscillator Voltage Range		V_{OSC}	Pin Group 4	–0.4	4.0	V
Analog Input Voltage Range		V_{INA}	Pin Group 3	–0.3	4.0	V
Input clamp current, per pin (V_{IN} < 0)[1]		V_{IC}		—	-20.0	mA
Output clamp current, per pin (V_O < 0)[1]		V_{OC}		—	-20.0	mA
Output Voltage Range (Normal Push-Pull mode)		V_{OUT}	Pin Group 1	–0.3	4.0	V
Output Voltage Range (Open Drain mode)		V_{OUTOD}	Pin Group 2	–0.3	6.0	V
DAC Output Voltage Range		V_{OUT_DAC}	Pin Group 5	–0.3	4.0	V
Ambient Temperature	Industrial V	T_A		–40	105	°C
	Industrial M	T_A		–40	125	°C
Junction Temperature		T_J		—	150	°C
Storage Temperature Range (Extended Industrial)		T_{STG}		–55	150	°C

1 Continuous clamp current per pin is –2.0 mA.

Default Mode

Pin Group 1: GPIO, TDI, TDO, TMS, TCK
Pin Group 2: $\overline{\text{RESET}}$, GPIOA7
Pin Group 3: ADC and Comparator Analog Inputs
Pin Group 4: XTAL, EXTAL
Pin Group 5: DAC analog output

7.3 ESD Protection and Latch-up Immunity

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, use normal handling precautions to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing conforms with AEC-Q100 Stress Test Qualification. During device qualification, ESD stresses are performed for the human body model (HBM), the machine model (MM), and the charge device model (CDM).

All latch-up testing conforms with AEC-Q100 Stress Test Qualification.

A device is defined as a failure if, after exposure to ESD pulses, the device no longer meets the device specification. Comprehensive DC parametric and functional testing is performed according to the applicable device specification at room temperature and then at hot temperature, unless specified otherwise in the device specification.

Table 18. MC56F825x/MC56F824x ESD/Latch-up Protection

Characteristic [1]	Min	Typ	Max	Unit
ESD for Human Body Model (HBM)	2000	—	—	V
ESD for Machine Model (MM)	200	—	—	V
ESD for Charge Device Model (CDM)	750	—	—	V
Latch-up current at T_A = 85 °C (I_{LAT})	± 100			mA

[1] Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions, unless otherwise noted

7.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the device design. To account for $P_{I/O}$ in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} is very small.

Table 19. 44LQFP Package Thermal Characteristics

Characteristic	Comments	Symbol	Value (LQFP)	Unit
Junction to ambient Natural convection	Single layer board (1s)	$R_{\theta JA}$	70	°C/W
Junction to ambient Natural convection	Four layer board (2s2p)	$R_{\theta JMA}$	48	°C/W
Junction to ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	57	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	42	°C/W
Junction to board		$R_{\theta JB}$	30	°C/W
Junction to case		$R_{\theta JC}$	13	°C/W
Junction to package top	Natural convection	Ψ_{JT}	2	°C/W

Table 20. 48LQFP Package Thermal Characteristics

Characteristic	Comments	Symbol	Value (LQFP)	Unit
Junction to ambient Natural convection	Single layer board (1s)	$R_{\theta JA}$	67	°C/W
Junction to ambient Natural convection	Four layer board (2s2p)	$R_{\theta JMA}$	48	°C/W
Junction to ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	60	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	44	°C/W
Junction to board		$R_{\theta JB}$	24	°C/W
Junction to case		$R_{\theta JC}$	15	°C/W
Junction to package top	Natural Convection	Ψ_{JT}	2	°C/W

Table 21. 64LQFP Package Thermal Characteristics

Characteristic	Comments	Symbol	Value (LQFP)	Unit
Junction to ambient Natural convection	Single layer board (1s)	$R_{\theta JA}$	67	°C/W
Junction to ambient Natural convection	Four layer board (2s2p)	$R_{\theta JMA}$	48	°C/W
Junction to ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	55	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	42	°C/W
Junction to board		$R_{\theta JB}$	31	°C/W
Junction to case		$R_{\theta JC}$	14	°C/W
Junction to package top	Natural convection	Ψ_{JT}	3	°C/W

NOTE

Junction-to-ambient thermal resistance determined per JEDEC JESD51–3 and JESD51–6. Thermal test board meets JEDEC specification for this package.

Junction-to-board thermal resistance determined per JEDEC JESD51–8. Thermal test board meets JEDEC specification for the specified package.

Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51–2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

See Section 8.1, "Thermal Design Considerations," for more detail on thermal design considerations.

7.5 Recommended Operating Conditions

This section contains information about recommended operating conditions.

Table 22. Recommended Operating Conditions (V_{REFLx} = 0 V, V_{SSA} = 0 V, V_{SS} = 0 V)

Characteristic		Symbol	Notes	Min	Typ	Max	Unit
Supply voltage		V_{DD}, V_{DDA}		3	3.3	3.6	V
ADC Reference Voltage High		V_{REFHx}		3.0		V_{DDA}	V
Voltage difference V_{DD} to V_{DDA}		ΔV_{DD}		–0.1	0	0.1	V
Voltage difference V_{SS} to V_{SSA}		ΔV_{SS}		–0.1	0	0.1	V
Device Clock Frequency Using relaxation oscillator Using external clock source		FSYSCLK		 0.001 0		 60 60	MHz
Input Voltage High (digital inputs)		V_{IH}	Pin Groups 1, 2	2.0		5.5	V
Input Voltage Low (digital inputs)		V_{IL}	Pin Groups 1, 2	–0.3		0.8	V
Oscillator Input Voltage High XTAL driven by an external clock source		V_{IHOSC}	Pin Group 4	2.0		V_{DD} + 0.3	V
Oscillator Input Voltage Low		V_{ILOSC}	Pin Group 4	–0.3		0.8	V
DAC Output Load Resistance		R_{LD}	Pin Group 5	3K			Ω
DAC Output Load Capacitance		C_{LD}	Pin Group 5			400	pf
Output Source Current High at V_{OH} min.)[1] When programmed for low drive strength When programmed for high drive strength		I_{OH}	 Pin Group 1 Pin Group 1	 — —		 -4 -8	mA
Output Source Current Low (at V_{OL} max.)[1] When programmed for low drive strength When programmed for high drive strength		I_{OL}	 Pin Groups 1, 2 Pin Groups 1, 2	 — —		 4 8	mA
Ambient Operating Temperature	Industrial V	T_A		–40		105	°C
	Industrial M	T_A		–40		125	°C
Flash Endurance (Program Erase Cycles)		N_F	T_A = -40°C to 125°C	10,000		—	cycles
Flash Data Retention		T_R	T_J <= 85°C avg	15		—	years

Table 22. Recommended Operating Conditions (continued) (V_{REFLx} = 0 V, V_{SSA} = 0 V, V_{SS} = 0 V)

Characteristic	Symbol	Notes	Min	Typ	Max	Unit
Flash Data Retention with <100 Program/Erase Cycles	t_{FLRET}	T_J <= 85°C avg	20	—	—	years

1 Total chip source or sink current cannot exceed 75 mA

Default Mode
Pin Group 1: GPIO, TDI, TDO, TMS, TCK
Pin Group 2: $\overline{\text{RESET}}$, GPIOA7
Pin Group 3: ADC and Comparator Analog Inputs
Pin Group 4: XTAL, EXTAL
Pin Group 5: DAC analog output

7.6 DC Electrical Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 23. DC Electrical Characteristics at Recommended Operating Conditions

Characteristic	Symbol	Notes	Min	Typ	Max	Unit	Test Conditions
Output Voltage High	V_{OH}	Pin Group 1	2.4	—	—	V	$I_{OH} = I_{OHmax}$
Output Voltage Low	V_{OL}	Pin Groups 1, 2	—	—	0.4	V	$I_{OL} = I_{OLmax}$
Digital Input Current High (a) pull-up enabled or disabled	I_{IH}	Pin Groups 1, 2	—	0	+/- 2.5	µA	V_{IN} = 2.4 V to 5.5 V
Comparator Input Current High	I_{IHC}	Pin Group 3	—	0	+/- 2	µA	$V_{IN} = V_{DDA}$
Oscillator Input Current High	I_{IHOSC}	Pin Group 3	—	0	+/- 2	µA	$V_{IN} = V_{DDA}$
Digital Input Current Low[1] pull-up enabled pull-up disabled	I_{IL}	Pin Groups 1, 2	-15 —	-30 0	-60 +/- 2.5	µA	V_{IN} = 0 V
Internal Pull-Up Resistance	$R_{Pull-Up}$		60	110	220	kΩ	—
Comparator Input Current Low	I_{ILC}	Pin Group 3	—	0	+/- 2	µA	V_{IN} = 0 V
Oscillator Input Current Low	I_{ILOSC}	Pin Group 3	—	0	+/- 2	µA	V_{IN} = 0 V
DAC Output Voltage Range	V_{DAC}	Pin Group 5	Typically V_{SSA} + 40 mV	—	Typically V_{DDA} – 40 mV	V	—
Output Current [1] High Impedance State	I_{OZ}	Pin Groups 1, 2	—	0	+/- 2.5	µA	—
Schmitt Trigger Input Hysteresis	V_{HYS}	Pin Groups 1, 2	—	0.35	—	V	—
Input Capacitance	C_{IN}		—	10	—	pF	—
Output Capacitance	C_{OUT}		—	10	—	pF	—

[1] See Figure 14.

Default Mode

Pin Group 1: GPIO, TDI, TDO, TMS, TCK
Pin Group 2: $\overline{\text{RESET}}$, GPIOA7
Pin Group 3: ADC and Comparator Analog Inputs
Pin Group 4: XTAL, EXTAL
Pin Group 5: DAC Analog Output

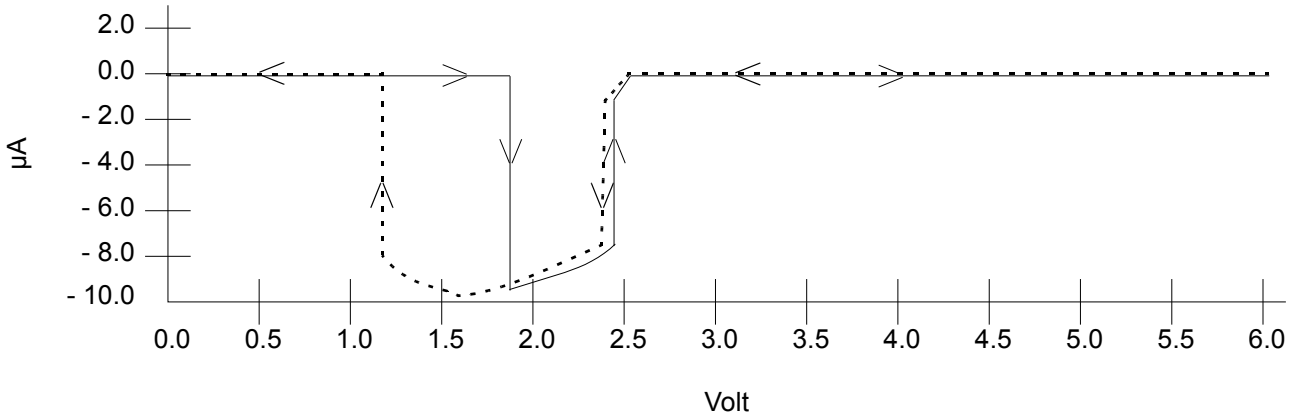


Figure 14. I_{IN}/I_{OZ} versus V_{IN} (Typical; Pull-Up Disabled)

7.7 Supply Current Characteristics

The following table specifies supply current characteristics.

Table 24. Current Consumption

Mode	Conditions	Typical @ 3.3 V 25°C (mA)		Maximum @ 3.6 V 105 °C (V temperature) 125 °C (M temperature) (mA)	
		I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}
RUN	60 MHz device clock Relaxation oscillator on PLL powered on Continuous MAC instructions with fetches from program flash memory All peripheral modules enabled; TMRs and SCIs using 1X Clock ADC/DAC powered on and clocked Comparator powered on	92	38	97	44
WAIT	60 MHz device clock Relaxation oscillator on PLL powered on Processor core in WAIT state All peripheral modules enabled; TMRs and SCIs using 1X Clock ADC/DAC/comparator powered off	49	4.5	53	5.5
STOP	4 MHz device clock Relaxation oscillator on PLL powered off Processor core in STOP state All peripheral module and core clocks are off ADC/DAC/comparator powered off	8.0	3.6	9.2	4.9
STANDBY > STOP	100 kHz device clock Relaxation oscillator in standby mode PLL powered off Processor core in STOP state All peripheral module and core clocks are off ADC/DAC/comparator powered off Voltage regulator in standby mode	0.76	0	3.0	0
POWERDOWN	Device clock is off Relaxation oscillator powered off PLL powered off Processor core in STOP state All peripheral module and core clocks are off ADC /DAC/comparator powered off Voltage regulator in standby mode	0.66	0	2.0	0

1 No output switching
All ports configured as inputs
All inputs low
No DC loads

7.8 Power-On Reset, Low Voltage Detection Specification

Table 25. Power-On Reset and Low-Voltage Detection Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Low-Voltage Interrupt for 3.3 V supply[1]	V_{LVI27}	2.6	2.7	2.8	V
Low-Voltage Interrupt for 2.5 V supply[2]	V_{LVI21}	—	2.18	—	V
Low-Voltage Interrupt Recovery Hysteresis	V_{EIH}	—	50	—	mV
Power-On Reset Threshold[3]	POR	2.6	2.7	2.8	V
Brown-Out Reset Threshold[4]	BOR	—	1.8	1.9	V

1 When V_{DD} drops below LVI27, an interrupt is generated.
2 When V_{DD} drops below LVI21, an interrupt is generated.
3 While power is ramping up, this signal remains active for as long as the internal 2.5 V is below 2.18 V or the 3.3 V V_{DD} voltage is below 2.7 V, no matter how long the ramp-up rate is. The internally regulated voltage is typically 100 mV less than V_{DD} during ramp-up until 2.5 V is reached, at which time it self-regulates.
4 Brown-Out Reset occurs whenever the internally regulated 2.5 V digital supply drops below 1.8 V.

7.9 Voltage Regulator Specifications

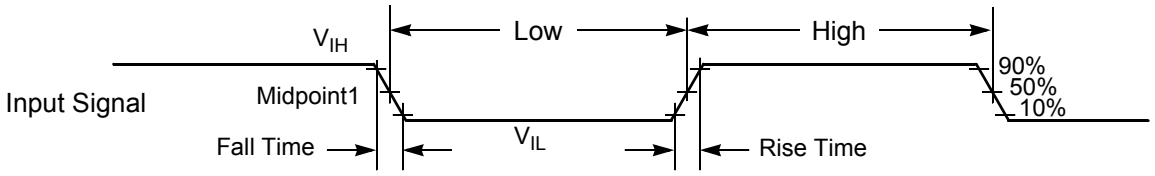
The MC56F825x/MC56F824x has two on-chip regulators. One supplies the PLL, crystal oscillator, NanoEdge placement PWM, and relaxation oscillator. It has no external pins and therefore has no external characteristics that must be guaranteed (other than proper operation of the device). The second regulator supplies approximately 2.5 V to the MC56F825x/MC56F824x's core logic. For proper operation, this regulator requires an external capacitor of 2.2 µF or greater. Ceramic and tantalum capacitors tend to provide better performance tolerances. The output voltage can be measured directly on the V_{CAP} pin. The specifications for this regulator appear in Table 26.

Table 26. Regulator Parameters

Characteristic	Symbol	Min	Typical	Max	Unit
Short Circuit Current	I_{SS}	—	900	1300	mA
Short Circuit Tolerance (V_{CAP} shorted to ground)	T_{RSC}	—	—	30	minutes

7.10 AC Electrical Characteristics

Tests are conducted using the input levels specified in Table 23. Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured between the 10% and 90% points, as shown in Figure 15.



The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

Figure 15. Input Signal Measurement References

Figure 16 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state
- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

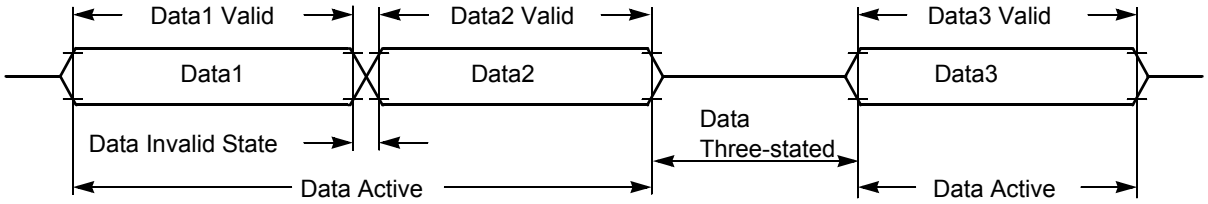


Figure 16. Signal States

7.11 Enhanced Flex PWM Characteristics

Table 27. Enhanced Flex PWM Timing Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
NanoEdge Placement (NEP) step size[1 2 3]	—	—	521	—	ps
Delay for fault input activating to PWM output deactivated	—	1	—		ns

1 Required: IP bus clock is between 50 MHz and ~60 Mhz in NanoEdge Placement mode.

2 NanoEdge Placement step size is a function of clock frequency only. Temperature and voltage variations do not affect NanoEdge Placement step size.

3 In NanoEdge Placement mode, the minimum pulse edge-to-edge cannot be less than 4 PWM clock cycles.

7.12 Flash Memory Characteristics

Table 28. Flash Timing Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Program time[1]	tprog	20	—	40	µs
Erase time [2]	terase	20	—	—	ms
Mass erase time	tme	100	—	—	ms

1 Additional overhead is part of the programming sequence. Refer to the device's reference manual for details.

2 Specifies page erase time. There are 1024 bytes per page in the program flash memory.

7.13 External Clock Operation Timing

Table 29. External Clock Operation Timing Requirements[1]

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation (external clock driver)[2]	f_{osc}	—	—	120	MHz
Clock pulse width[3]	t_{PW}	6.25	—	—	ns

Table 29. External Clock Operation Timing Requirements[1] (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
External clock input rise time[4]	t_{rise}	—	—	3	ns
External clock input fall time[5]	t_{fall}	—	—	3	ns
Input high voltage overdrive by an external clock	V_{ih}	$0.85V_{DD}$	—	—	V
Input high voltage overdrive by an external clock	V_{il}	—	—	$0.3V_{DD}$	V

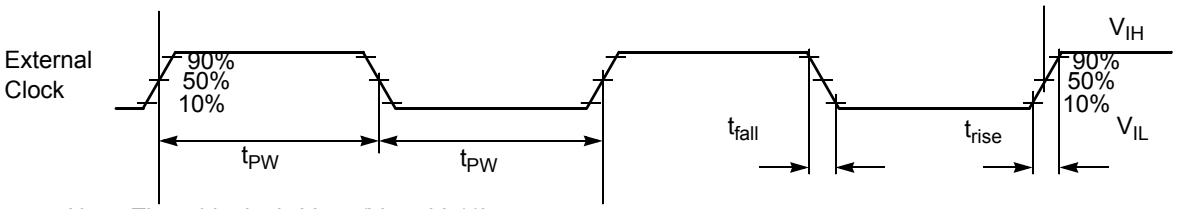
1 Parameters listed are guaranteed by design.

2 See Figure 17 for details on using the recommended connection of an external clock driver.

3 The chip may not function if the high or low pulse width is smaller than 6.25 ns.

4 External clock input rise time is measured from 10% to 90%.

5 External clock input fall time is measured from 90% to 10%.



Note: The midpoint is $V_{IL} + (V_{IH} – V_{IL})/2$.

Figure 17. External Clock Timing

7.14 Phase Locked Loop Timing

Table 30. Phase Locked Loop Timing

Characteristic	Symbol	Min	Typ	Max	Unit
PLL input reference frequency[1]	f_{ref}	4	8	8	MHz
PLL output frequency[2]	f_{op}	120	—	240	MHz
PLL lock time[3 4]	t_{plls}	—	40	100	µs
Accumulated jitter using an 8 MHz external crystal as the PLL source[5]	J_A	—	—	TBD	%
Cycle-to-cycle jitter	$t_{jitterpll}$	—	350	—	ps

1 An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 8 MHz input.

2 The core system clock operates at 1/6 of the PLL output frequency.

3 This is the time required after the PLL is enabled to ensure reliable operation.

4 From powerdown to powerup state at 60 MHz system clock state.

5 This is measured on the CLKO signal (programmed as system clock) over 264 system clocks at 60 MHz system clock frequency and using an 8 MHz oscillator frequency.

7.15 External Crystal or Resonator Requirement

Table 31. Crystal or Resonator Requirement

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation	f_{XOSC}	4	8	16	MHz

7.16 Relaxation Oscillator Timing

Table 32. Relaxation Oscillator Timing

Characteristic	Symbol	Minimum	Typical	Maximum	Unit
Relaxation oscillator output frequency[1] Normal Mode Standby Mode	f_{op}	—	 8.05 400	—	 MHz kHz
Relaxation oscillator stabilization time[2]	t_{roscs}	—	1	3	ms
Cycle-to-cycle jitter. This is measured on the CLKO signal (programmed prescaler_clock) over 264 clocks[3]	$t_{jitterosc}$	—	400	—	ps
Variation over temperature –40°C to 150°C[4]		—	+1.5 to –1.5	+3.0 to –3.0	%
Variation over temperature 0°C to 105°C[4]		—	0 to +1	+2.0 to –2.0	%

1 Output frequency after factory trim.

2 This is the time required from standby to normal mode transition.

3 J_A is required to meet QSCI requirements.

4 See Figure 18.

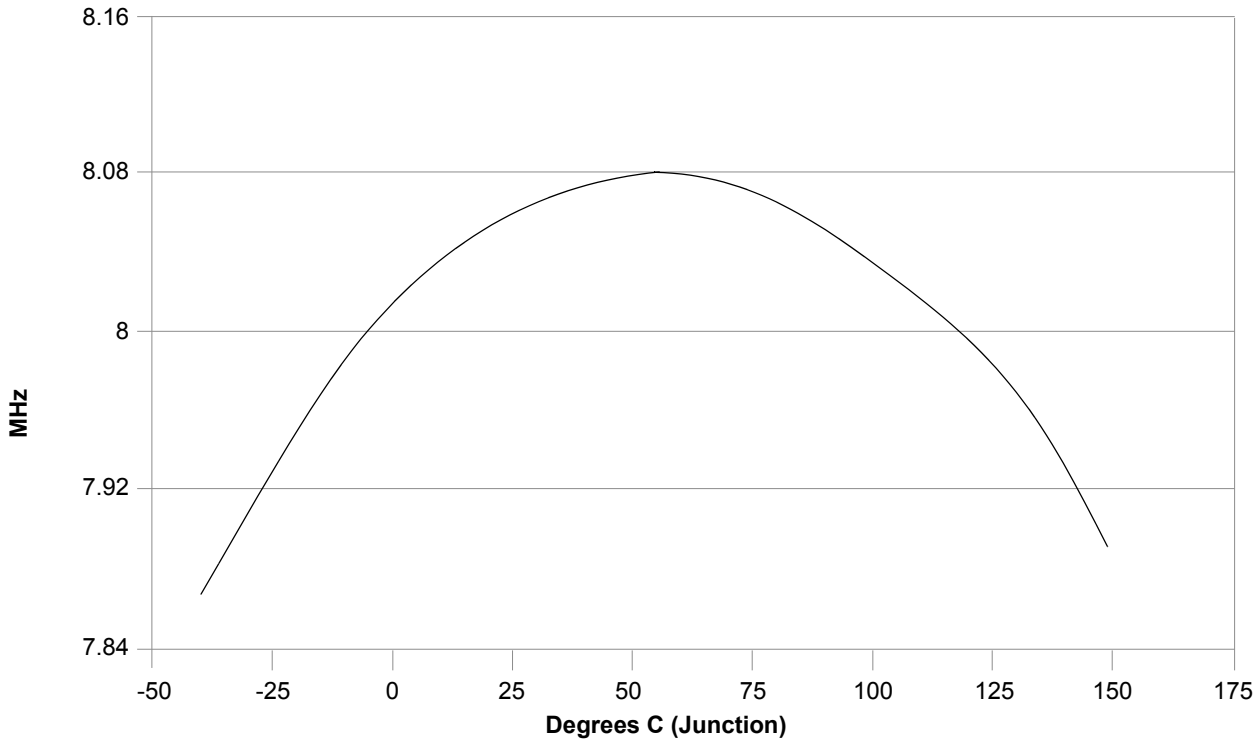


Figure 18. Relaxation Oscillator Temperature Variation (Typical) After Trim

7.17 Reset, Stop, Wait, Mode Select, and Interrupt Timing

NOTE

All address and data buses described here are internal.

Table 33. Reset, Stop, Wait, Mode Select, and Interrupt Timing[1,2]

Characteristic	Symbol	Typical Min	Typical Max	Unit	See Figure
Minimum $\overline{\text{RESET}}$ Assertion Duration [3]	t_{RA}	4T	—	ns	—
Minimum GPIO pin Assertion for Interrupt	t_{IW}	2T	—	ns	Figure 19
$\overline{\text{RESET}}$ deassertion to First Address Fetch	t_{RDA}	$96T_{OSC}$ + 64T	$97T_{OSC}$ + 65T	ns	—
Delay from Interrupt Assertion to Fetch of first instruction (exiting Stop)	t_{IF}	—	6T	ns	—

1 In the formulas, T = system clock cycle and T_{osc} = oscillator clock cycle. For an operating frequency of 32 MHz, T = 31.25 ns. At 4 MHz (used coming out of reset and stop modes), T = 250 ns.

2 Parameters listed are guaranteed by design.

3 This minimum number guarantees that a reliable reset occurs.

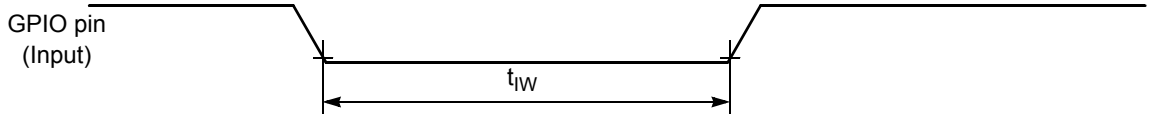


Figure 19. GPIO Interrupt Timing (Negative Edge-Sensitive)

7.18 Queued Serial Peripheral Interface (SPI) Timing

Table 34. SPI Timing[1]

Characteristic	Symbol	Min	Max	Unit	Refer to
Cycle time Master Slave	t_C	 125 62.5	 — —	 ns ns	Figure 20, Figure 21, Figure 22, Figure 23
Enable lead time Master Slave	t_{ELD}	 — 31	 — —	 ns ns	Figure 23
Enable lag time Master Slave	t_{ELG}	 — 125	 — —	 ns ns	Figure 23
Clock (SCK) high time Master Slave	t_{CH}	 50 31	 — —	 ns ns	Figure 20, Figure 21, Figure 22, Figure 23
Clock (SCK) low time Master Slave	t_{CL}	 50 31	 — —	 ns ns	Figure 23

Table 34. SPI Timing[1] (continued)

Characteristic	Symbol	Min	Max	Unit	Refer to
Data set-up time required for inputs Master Slave	t_{DS}	 20 0	 — —	 ns ns	Figure 20, Figure 21, Figure 22, Figure 23
Data hold time required for inputs Master Slave	t_{DH}	 0 2	 — —	 ns ns	Figure 20, Figure 21, Figure 22, Figure 23
Access time (time to data active from high-impedance state) Slave	t_A	 4.8	 15	 ns	Figure 23
Disable time (hold time to high-impedance state) Slave	t_D	 3.7	 15.2	 ns	Figure 23
Data valid for outputs Master Slave (after enable edge)	t_{DV}	 — —	 4.5 20.4	 ns ns	Figure 20, Figure 21, Figure 22, Figure 23
Data invalid Master Slave	t_{DI}	 0 0	 — —	 ns ns	Figure 20, Figure 21, Figure 22, Figure 23
Rise time Master Slave	t_R	 — —	 11.5 10.0	 ns ns	Figure 20, Figure 21, Figure 22, Figure 23
Fall time Master Slave	t_F	 — —	 9.7 9.0	 ns ns	Figure 20, Figure 21, Figure 22, Figure 23

1 Parameters listed are guaranteed by design.

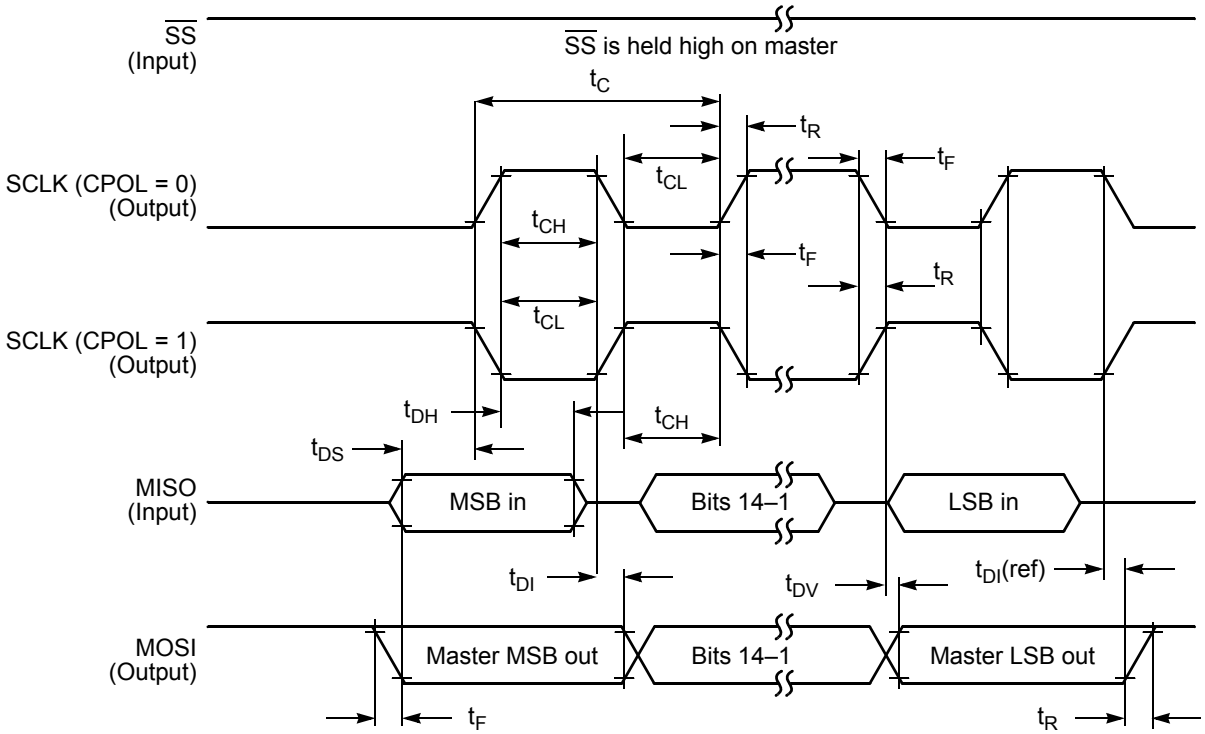


Figure 20. SPI Master Timing (CPHA = 0)

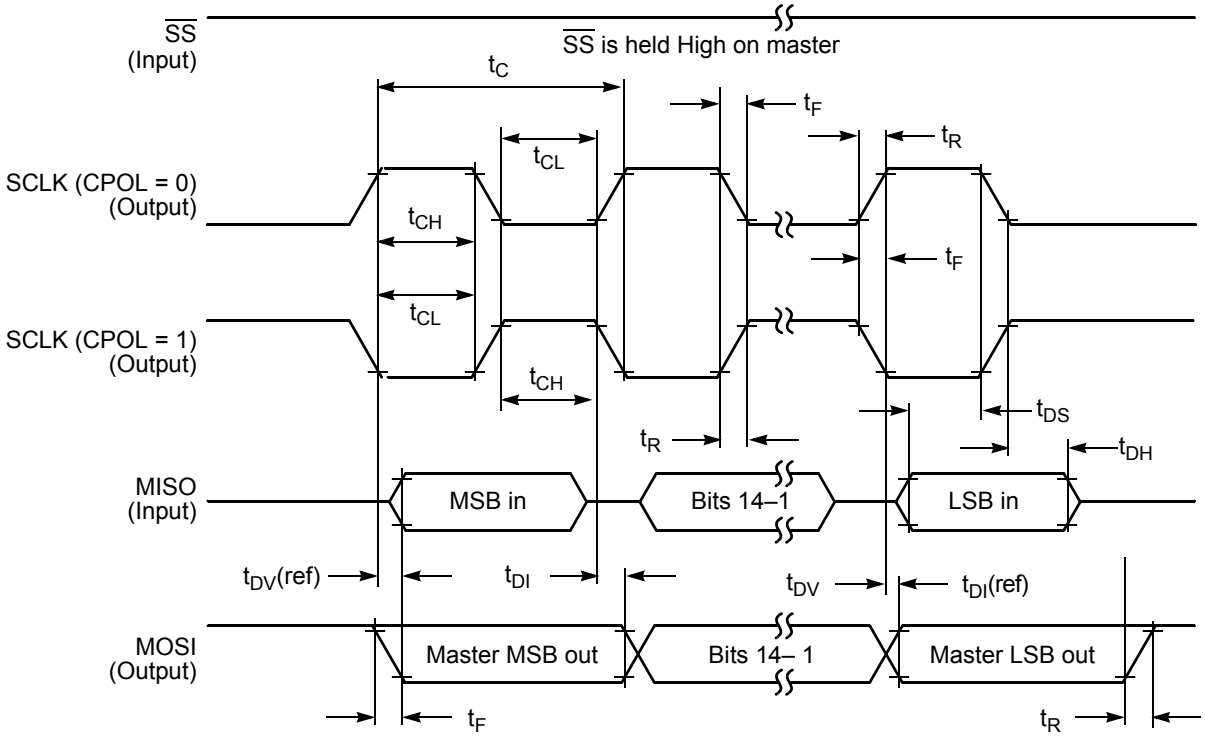


Figure 21. SPI Master Timing (CPHA = 1)

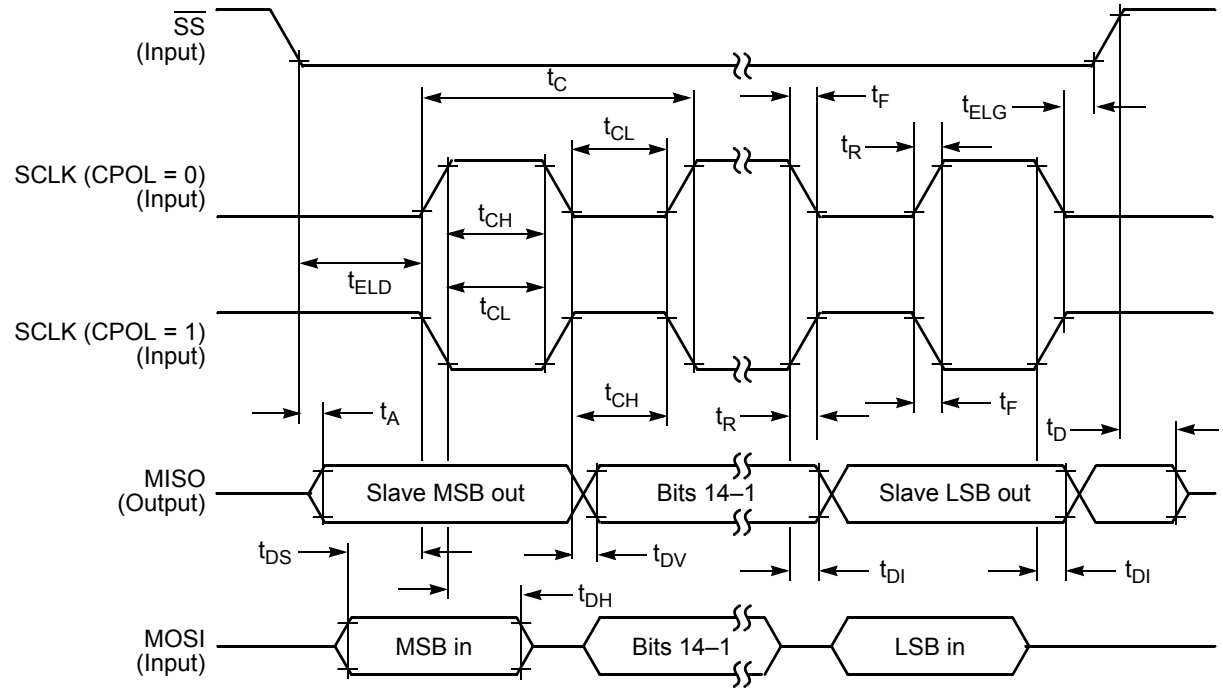


Figure 22. SPI Slave Timing (CPHA = 0)

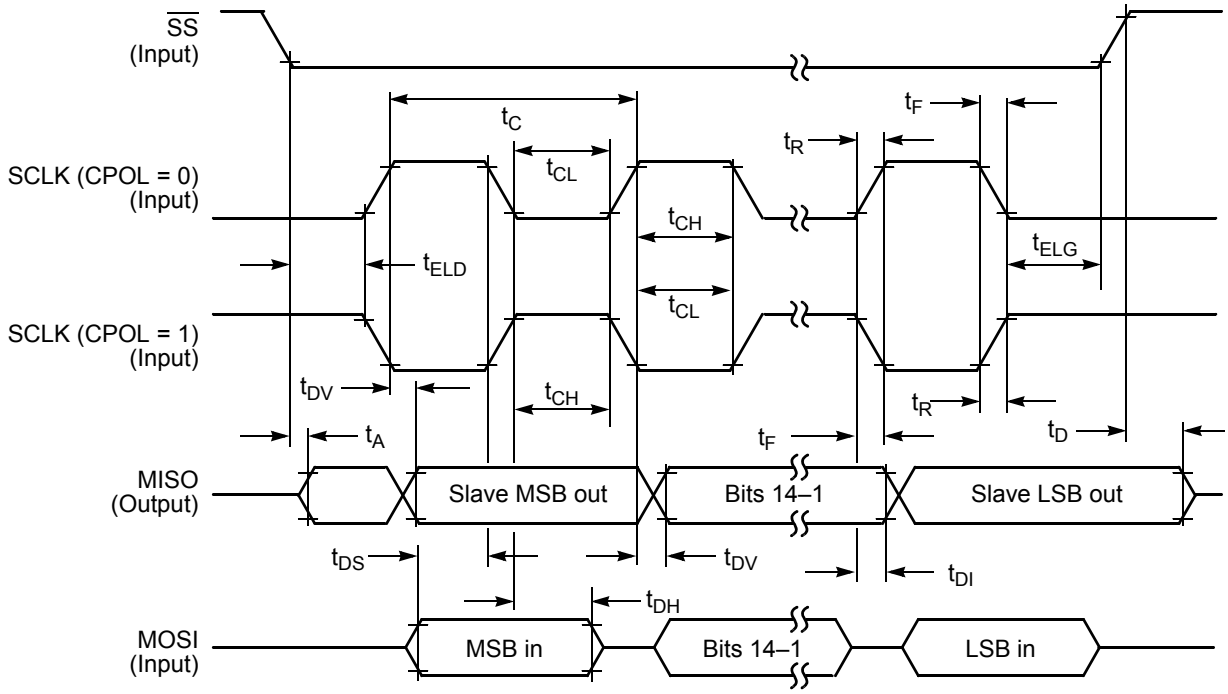


Figure 23. SPI Slave Timing (CPHA = 1)

7.19 Queued Serial Communication Interface (SCI) Timing

Table 35. SCI Timing[1]

Characteristic	Symbol	Min	Max	Unit	See Figure
Baud rate[2]	BR	—	(f_{MAX}/16)	Mbps	—
RXD pulse width	RXD_{PW}	0.965/BR	1.04/BR	ns	Figure 24
TXD pulse width	TXD_{PW}	0.965/BR	1.04/BR	ns	Figure 25
LIN Slave Mode					
Deviation of slave node clock from nominal clock rate before synchronization	$F_{TOL_UNSYNCH}$	–14	14	%	—
Deviation of slave node clock relative to the master node clock after synchronization	F_{TOL_SYNCH}	–2	2	%	—
Minimum break character length	T_{BREAK}	13	—	Master node bit periods	—
		11	—	Slave node bit periods	—

1 Parameters listed are guaranteed by design.

2 f_{MAX} is the frequency of operation of the SCI in MHz, which can be selected system clock (max. 60 MHz) or 2x system clock (max. 120 MHz) for the MC56F825x/MC56F824x device.

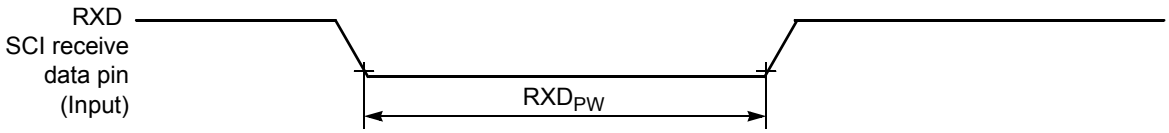


Figure 24. RXD Pulse Width

Figure 25. TXD Pulse Width

7.20 Freescale's Scalable Controller Area Network (MSCAN)

Table 36. MSCAN Timing

Characteristic	Symbol	Min	Max	Unit
Baud Rate	BR_{CAN}	—	1	Mbps
Bus Wake-up detection	T_{WAKEUP}	T_{IPBUS}	—	µs

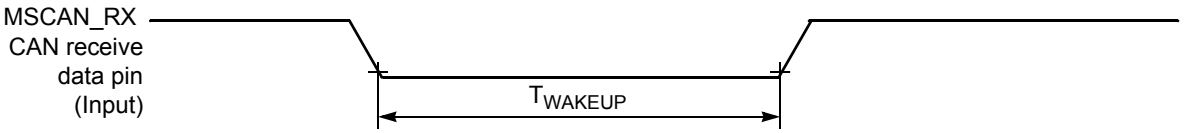


Figure 26. Bus Wake-up Detection

7.21 Inter-Integrated Circuit Interface (I^2C) Timing

Table 37. I^2C Timing

Characteristic	Symbol	Standard Mode		Unit
		Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{HD;\ STA}$	4.0	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	—	µs
Set-up time for a repeated START condition	$t_{SU;\ STA}$	4.7	—	µs
Data hold time for I^2C bus devices	$t_{HD;\ DAT}$	0[1]	3.45[2]	µs
Data set-up time	$t_{SU;\ DAT}$	250[3]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	ns
Fall time of SDA and SCL signals	t_f	—	300	ns
Set-up time for STOP condition	$t_{SU;\ STO}$	4.0	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	ns

1 The master mode I^2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, a negative hold time can result, depending on the edge rates of the SDA and SCL lines.

2 The maximum $t_{HD;\ DAT}$ must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

3 A Fast mode I^2C bus device can be used in a Standard mode I^2C bus system, but the requirement $t_{SU;\ DAT}$ > = 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\ DAT}$ = 1000 + 250 = 1250 ns (according to the Standard mode I^2C bus specification) before the SCL line is released.

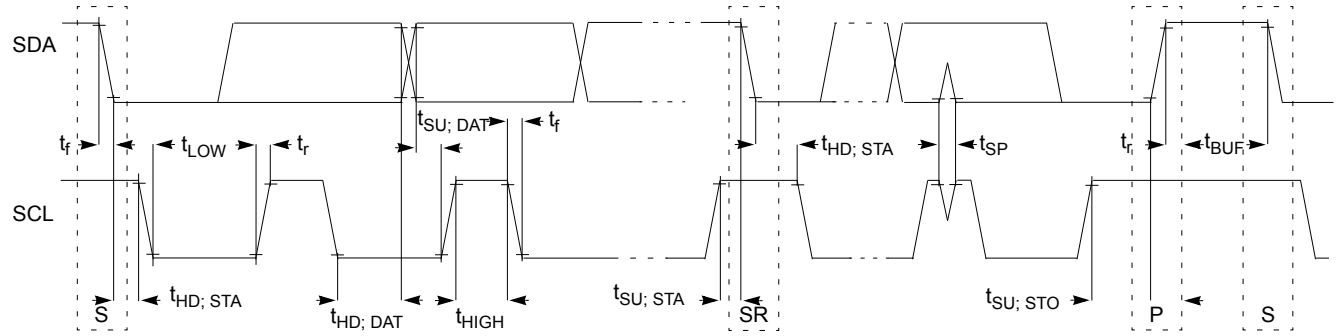


Figure 27. Timing Definition for Standard Mode Devices on the I^2C Bus

7.22 JTAG Timing

Table 38. JTAG Timing

Characteristic	Symbol	Min	Max	Unit	See Figure
TCK frequency of operation[1]	f_{OP}	DC	SYS_CLK/8	MHz	Figure 28
TCK clock pulse width	t_{PW}	50	—	ns	Figure 28
TMS, TDI data set-up time	t_{DS}	5	—	ns	Figure 29
TMS, TDI data hold time	t_{DH}	5	—	ns	Figure 29
TCK low to TDO data valid	t_{DV}	—	30	ns	Figure 29
TCK low to TDO tri-state	t_{TS}	—	30	ns	Figure 29

1 TCK frequency of operation must be less than 1/8 the processor rate.

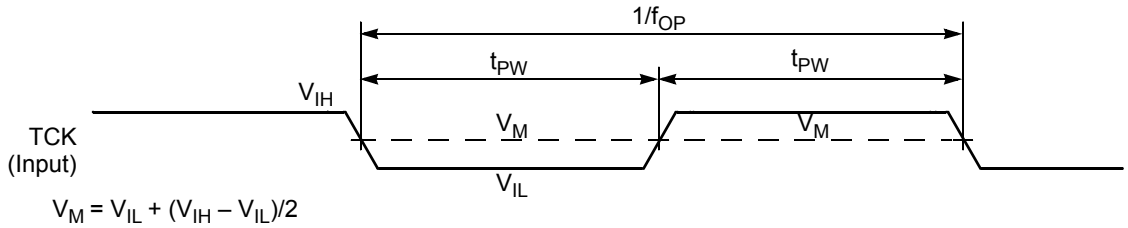


Figure 28. Test Clock Input Timing Diagram

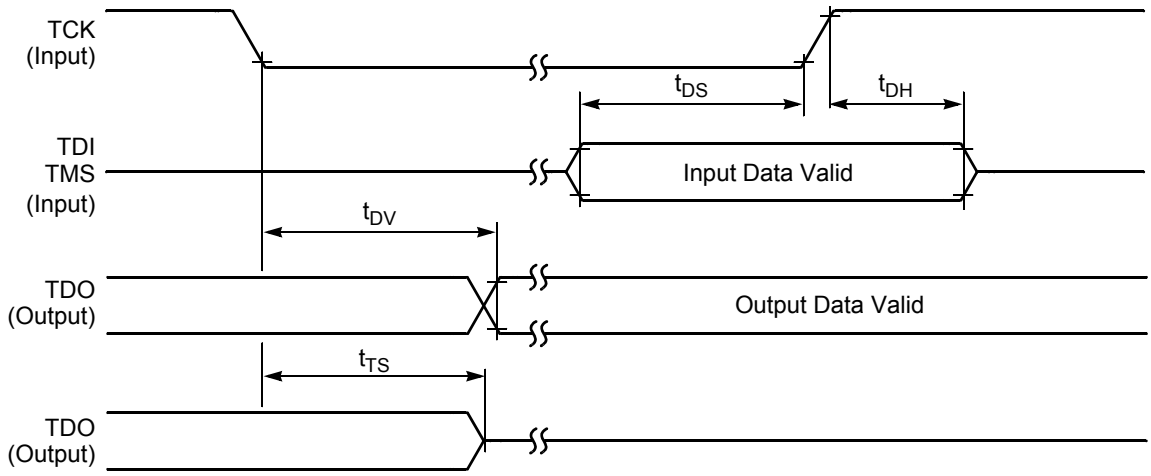


Figure 29. Test Access Port Timing Diagram

7.23 Quad Timer Timing

Table 39. Timer Timing[1, 2]

Characteristic	Symbol	Min	Max	Unit	See Figure
Timer input period	P_{IN}	2T + 6	—	ns	Figure 30
Timer input high/low period	P_{INHL}	1T + 3	—	ns	Figure 30
Timer output period	P_{OUT}	125	—	ns	Figure 30
Timer output high/low period	P_{OUTHL}	50	—	ns	Figure 30

1 In the formulas listed, T = the clock cycle. For 32 MHz operation, T = 31.25 ns.

2. Parameters listed are guaranteed by design.

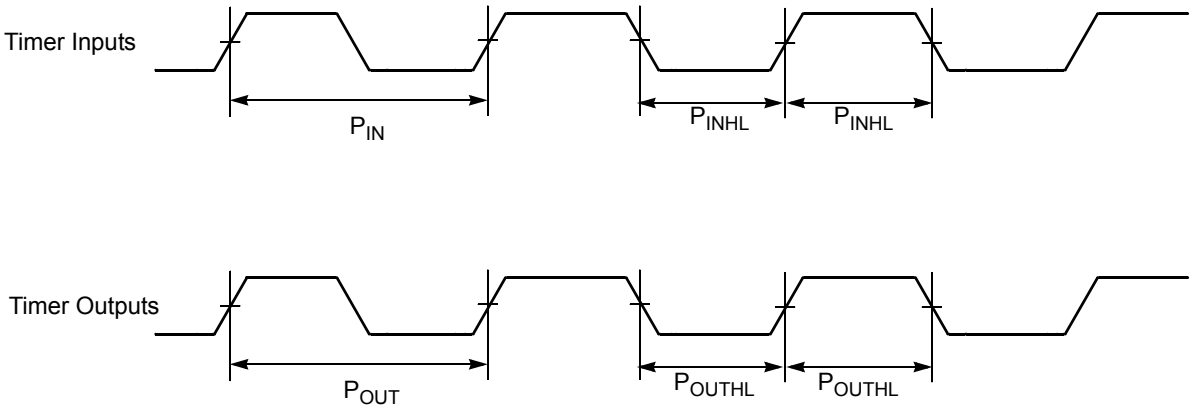


Figure 30. Timer Timing

7.24 COP Specifications

Table 40. COP Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Oscillator output frequency	LPFosc	500	1000	1500	Hz
Oscillator current consumption in partial power down mode	IDD		TBD		nA

7.25 Analog-to-Digital Converter (ADC) Parameters

Table 41. ADC Parameters[1]

Parameter	Symbol	Min	Typ	Max	Unit
DC Specifications					
Resolution	R_{ES}	12	—	12	Bits
ADC internal clock	f_{ADIC}	0.1	—	15	MHz
Conversion range	R_{AD}	V_{REFL}	—	V_{REFH}	V
ADC and VREF power-up time[2](from power down mode)	t_{ADPU}	—	13	—	t_{AIC} cycles[3]
VREF power-up time (from low power mode)	t_{REFPU}	—	6	—	t_{AIC} cycles[3]
ADC RUN current (Speed Control setting) at 100 kHz ADC clock (Standby Mode) at ADC clock ≤ 5 MHz (00) at 5 MHz < ADC clock ≤ 12 MHz (01) at 12 MHz < ADC clock ≤ 15 MHz (10)	I_{ADRUN}	 — — — —	 0.6 10 17 27	 — — — —	mA
Conversion time	t_{ADC}	—	6	—	t_{AIC} cycles[3]
Sample time	t_{ADS}	—	1	—	t_{AIC} cycles[3]
Accuracy (DC or absolute) (gain of 1x, 2x, 4x and f_{ADC} ≤ 10 MHz) (all data in single-ended mode)[4]					
Integral non-linearity[5] (Full input signal range)	INL	—	+/- 3	+/- 6	LSB[6]
Differential non-linearity[5]	DNL	—	+/- 0.6	+/- 1	LSB[5]
Monotonicity	GUARANTEED				
Offset Voltage Internal Ref	V_{OFFSET}	—	+/- 8	+/- 15	mV
Offset Voltage External Ref	V_{OFFSET}	—	+/- 8	+/- 15	mV
Gain Error (transfer gain)	E_{GAIN}	—	0.995 to 1.005	1.01 to 0.99	—
ADC Inputs[7] (Pin Group 3)					
Input voltage (external reference)	V_{ADIN}	V_{REFL}	—	V_{REFH}	V
Input voltage (internal reference)	V_{ADIN}	V_{SSA}	—	V_{DDA}	V
Input leakage	I_{IA}	—	0	+/- 2	µA
V_{REFH} current	I_{VREFH}	—	0.001	—	µA
Input injection current[8], per pin	I_{ADI}	—	—	3	mA
Input capacitance	C_{ADI}	—	See Figure 31	—	pF

Table 41. ADC Parameters[1] (continued)

Parameter	Symbol	Min	Typ	Max	Unit
Input impedance	X_{IN}	—	See Figure 31	—	Ohms
AC Specifications[9] (gain of 1x, 2x, 4x and $f_{ADC} \leq$ 10 MHz)[4]					
Signal-to-noise ratio	SNR	—	59		dB
Total Harmonic Distortion	THD	—	64		dB
Spurious Free Dynamic Range	SFDR	—	65		dB
Signal-to-noise plus distortion	SINAD	—	59		dB
Effective Number Of Bits	ENOB	—	9.5		Bits

1 All measurements were made at V_{DD} = 3.3V, V_{REFH} = 3.3V, and V_{REFL} = ground
2 Includes power-up of ADC and V_{REF}
3 ADC clock cycles
4 Speed register setting must be 00 for ADC clock ≤ 5 MHz, 01 for 5 MHz < ADC clock ≤ 12 MHz, and 10 for ADC clock > 12 MHz
5 INL and DNL measured from V_{IN} = V_{REFL} to V_{IN} = V_{REFH}
6 LSB = Least Significant Bit = 0.806 mV at x1 gain
7 Pin groups are detailed following Table 17.
8 The current that can be injected or sourced from an unselected ADC signal input without affecting the performance of the ADC
9 ADC PGA gain is x1

7.25.1 Equivalent Circuit for ADC Inputs

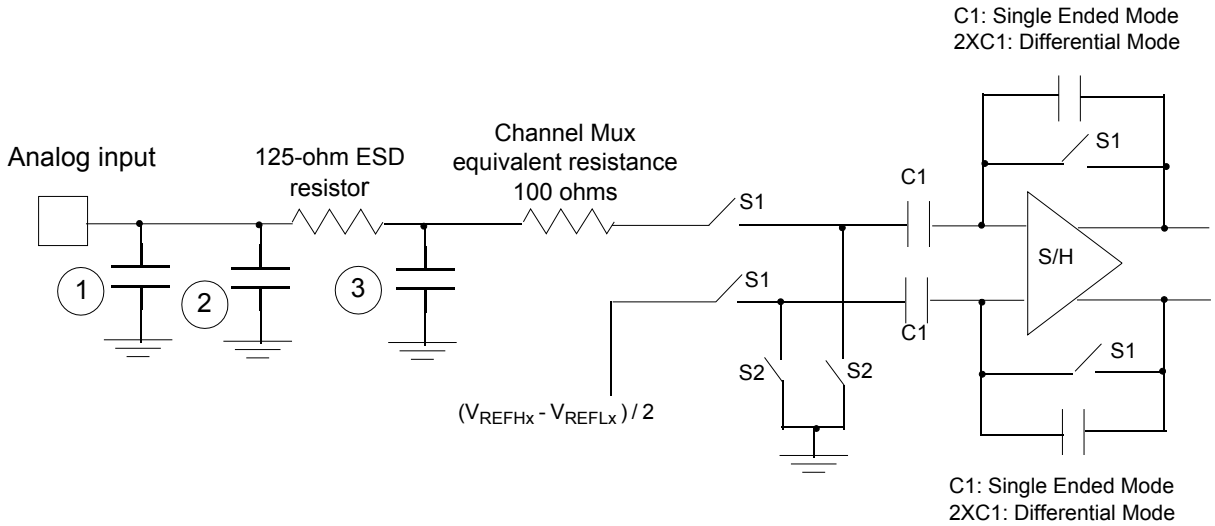
Figure 31 illustrates the ADC input circuit during sample and hold. S1 and S2 are always opened/closed at non-overlapping phases and operate at the ADC clock frequency. Equivalent input impedance, when the input is selected, is as follows:

$$(2 \times k / ADCClockRate \times C_{gain}) + 100 \text{ ohms} + 125 \text{ ohms} \qquad \textit{Eqn. 1}$$

where k =

- 1 for first sample
- 6 for subsequent samples

and C_{gain} is as described in note 4 below.



1. Parasitic capacitance due to package, pin-to-pin, and pin-to-package base coupling: 1.8 pF

2. Parasitic capacitance due to the chip bond pad, ESD protection devices, and signal routing: 2.04 pF
3. 8 pF noise damping capacitor
4. Sampling capacitor at the sample and hold circuit. Capacitor C1 is normally disconnected from the input and is only connected to it at sampling time: C_{gain} = 1.4 pF for x1 gain, 2.8 pF for x2 gain, and 5.6 pF for x4 gain.
5. S1 and S2 switch phases are non-overlapping and operate at the ADC clock frequency.

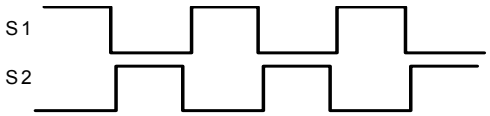


Figure 31. Equivalent Circuit for A/D Loading

7.26 Digital-to-Analog Converter (DAC) Parameters

Table 42. DAC Parameters

Parameter	Conditions/Comments	Symbol	Min	Typ	Max	Unit
DC Specifications						
Resolution			12	—	12	bits
Settling time	At output load R_{LD} = 3 KΩ C_{LD} = 400 pf		TBD	—	2	µS
Power-up time	Time from release of PWRDWN signal until DACOUT signal is valid	t_{DAPU}	—	—	11	µS
Accuracy						
Integral non-linearity[1]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	INL	—	+/- 3	+/- 8.0	LSB[2]
Differential non-linearity[1]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	DNL	—	+/- 0.8	+/- 1.0	LSB[2]
Monotonicity	> 6 sigma monotonicity, < 3.4 ppm non-monotonicity		guaranteed			—
Offset error[1]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	V_{OFFSET}	—	+/- 25	+/- 40	mV
Gain error[1]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	E_{GAIN}	—	+/- .5	+/- 1.5	%
DAC Output						
Output voltage range	Within 40 mV of either V_{REFLX} or V_{REFHX}	V_{OUT}	V_{REFLX} +0.04V	—	V_{REFHX} - 0.04V	V
AC Specifications						
Signal-to-noise ratio		SNR	—	TBD	—	dB
Spurious free dynamic range		SFDR	—	TBD	—	dB
Effective number of bits		ENOB	—	—	—	Bits

1 No guaranteed specification within 5% of V_{DDA} or V_{SSA}
2 LSB = 0.806 mV

7.27 5-Bit Digital-to-Analog Converter (DAC) Parameters

Table 43. 5-Bit DAC Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Reference Inputs	Vin	V_{DDA}	—	V_{DDA}	mV
Setup Delay	t_{PRGST}	TBD	TBD	TBD	ns
Step size	V_{STEP}	3Vin/128	Vin/32	5Vin/128	V
Output Range	V_{DACOUT}	Vin/32	—	Vin	ns

7.28 HSCMP Specifications

Table 44. HSCMP Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Analog input voltage	V_{AIN}	V_{SSA} – 0.01	—	V_{DDA} + 0.01	V
Analog input offset voltage[1]	V_{AIO}	—	—	40	mV
Analog comparator hysteresis[2]	V_H	—	1 to 16	—	mV
Propagation Delay, high speed mode (EN=1, PMODE=1),	t_{DHSN}[3]	—	70	140	ns
Propagation Delay, Low Speed Mode (EN=1, PMODE=0),	t_{AINIT}[4]	—	400	600	ns

1 Offset when the degree of hysteresis is set to its minimum value.
2 The range of hysteresis is based on simulation only. This range varies from part to part.
3 Measured with an input waveform that switches 30 mV above and below the reference, to the CMPO output pin. V_{DDA} > $V_{LVI_WARNING}$ => LVI_WARNING NOT ASSERTED.
4 Measured with an input waveform that switches 30 mV above and below the reference, to the CMPO output pin. V_{DDA} > $V_{LVI_WARNING}$ => LVI_WARNING NOT ASSERTED.

7.29 Optimize Power Consumption

See Section 7.7, "Supply Current Characteristics," for a list of I_{DD} requirements for the MC56F825x/MC56F824x. This section provides additional details for optimizing power consumption for a given application.

Power consumption is given by the following equation:

Total power = A: internal [static] component
+B: internal [state-dependent] component
+C: internal [dynamic] component
+D: external [dynamic] component
+E: external [static] component

A, the internal [static] component, consists of the DC bias currents for the oscillator, leakage currents, PLL, and voltage references. These sources operate independently of processor state or operating frequency.

B, the internal [state-dependent] component, reflects the supply current required by certain on-chip resources only when those resources are in use. These resources include RAM, flash memory, and the ADCs.

C, the internal [dynamic] component, is classic $C*V^2*F$ CMOS power dissipation corresponding to the 56800E core and standard cell logic.

D, the external [dynamic] component, reflects power dissipated on-chip as a result of capacitive loading on the external pins of the chip. This component is also commonly described as $C*V^2*F$, although simulations on two of the I/O cell types used on the 56800E reveal that the power-versus-load curve does have a non-zero Y-intercept.

Table 45. I/O Loading Coefficients at 10 MHz

	Intercept	Slope
8 mA drive	1.3	0.11 mW/pF
4 mA drive	1.15 mW	0.11 mW/pF

Power due to capacitive loading on output pins is (first order) a function of the capacitive load and frequency at which the outputs change. Table 45 provides coefficients for calculating power dissipated in the I/O cells as a function of capacitive load. In these cases, Equation 2 applies.

$$TotalPower = \Sigma((\text{Intercept} + \text{Slope}*C_{load})*\text{frequency}/10\ \text{MHz}) \qquad \textit{Eqn. 2}$$

where:

— Summation is performed over all output pins with capacitive loads.
— Total power is expressed in mW.
— C_{load} is expressed in pF.

Because of the low duty cycle on most device pins, power dissipation due to capacitive loads was found to be fairly low when averaged over a period of time.

E, the external [static] component, reflects the effects of placing resistive loads on the outputs of the device. Total all V^2/R or IV to arrive at the resistive load contribution to power. Assume V = 0.5 for the purposes of these rough calculations. For instance, if there is a total of nine PWM outputs driving 10 mA into LEDs, then P = 8*0.5*0.01 = 40 mW.

In previous discussions, power consumption due to parasites associated with pure input pins is ignored and assumed to be negligible.

8 Design Considerations

8.1 Thermal Design Considerations

An estimation of the chip junction temperature, T_J, can be obtained from Equation 3.

$$T_J = T_A + (R_{\theta JA} \times P_D) \qquad \textit{Eqn. 3}$$

where:

T_A = Ambient temperature for the package (^oC)
$R_{\theta JA}$ = Junction-to-ambient thermal resistance ($^oC/W$)
P_D = Power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single-layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which

value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low-power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance.

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \qquad \textit{Eqn. 4}$$

where:

$R_{\theta JA}$ = Package junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = Package junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = Package case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be adjusted. You control the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, you can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the thermal characterization parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case. Refer to Equation 5.

$$T_J = T_T + (\Psi_{JT} \times P_D) \qquad \textit{Eqn. 5}$$

where:

T_T = Thermocouple temperature on top of package (^{O}C)

Ψ_{JT} = Thermal characterization parameter (^{O}C/W)

P_D = Power dissipation in package (W)

The thermal characterization parameter is measured per JESD51–2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

8.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation of the MC56F825x/MC56F824x:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the MC56F825x/MC56F824x and from the board ground to each V_{SS} (GND) pin.
- The minimum bypass requirement is to place 0.01–0.1 µF capacitors positioned as near as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA}. Ceramic and tantalum capacitors tend to provide better tolerances.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are as short as possible.
- Bypass the V_{DD} and V_{SS} with approximately 100 µF, plus the number of 0.1 µF ceramic capacitors.
- PCB trace lengths should be minimal for high-frequency signals.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and V_{SS} circuits.
- Take special care to minimize noise levels on the V_{REF}, V_{DDA}, and V_{SSA} pins.
- Using separate power planes for V_{DD} and V_{DDA} and separate ground planes for V_{SS} and V_{SSA} is recommended. Connect the separate analog and digital power and ground planes as near as possible to power supply outputs. If an analog circuit and digital circuit are powered by the same power supply, you should connect a small inductor or ferrite bead in serial with V_{DDA} and V_{SSA} traces.
- Physically separate analog components from noisy digital components by ground planes. Do not place an analog trace in parallel with digital traces. Place an analog ground trace around an analog signal trace to isolate it from digital traces.
- Because the flash memory is programmed through the JTAG/EOnCE port, SPI, SCI, or I^2C, the designer should provide an interface to this port if in-circuit flash programming is desired.
- If desired, connect an external RC circuit to the $\overline{\text{RESET}}$ pin. The resistor value should be in the range of 4.7 kΩ to 10 kΩ; the capacitor value should be in the range of 0.22 µF to 4.7 µF.
- Configuring the $\overline{\text{RESET}}$ pin to GPIO output in normal operation in a high-noise environment may help to improve the performance of noise transient immunity.
- Add a 2.2 kΩ external pullup on the TMS pin of the JTAG port to keep EOnCE in a restate during normal operation if a JTAG converter is not present.
- During reset and after reset but before I/O initialization, all I/O pins are at input state with internal pullup enabled. The typical value of internal pullup is around 110 kΩ. These internal pullups can be disabled by software.
- To eliminate PCB trace impedance effect, each ADC input should have an RC filter of no less than 33 pF 10 Ω.
- External clamp diodes on analog input pins are recommended.

9 Ordering Information

Table 46 lists the pertinent information needed to place an order. Consult a Freescale Semiconductor sales office or authorized distributor to determine availability and to order devices.

Table 46. MC56F825x/MC56F824x Ordering Information

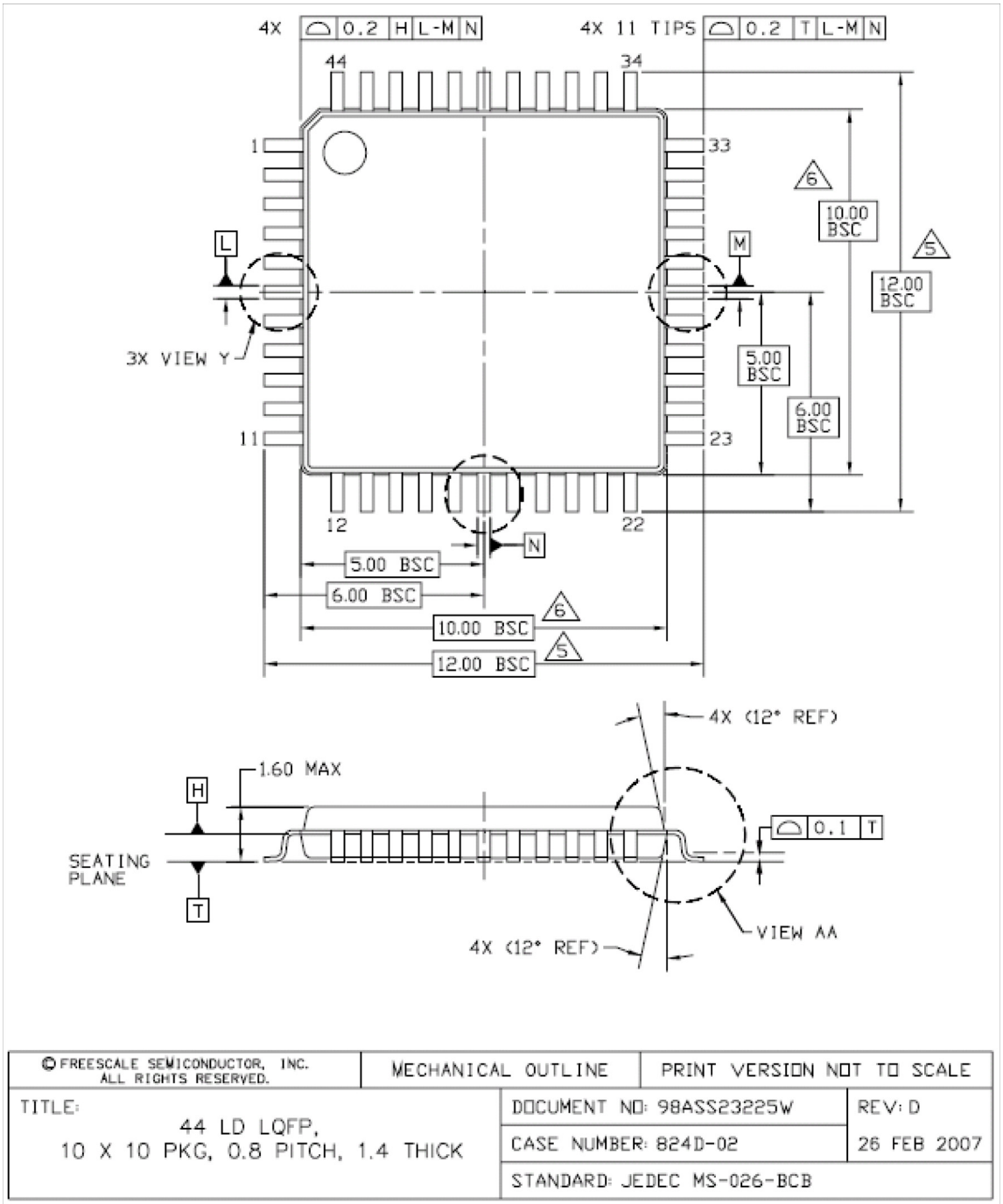
Device	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Ambient Temperature Range	Order Number[1]
MC56F8245	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	44	60	–40° to + 105° C –40° to + 125° C	MC56F8245VLD MC56F8245MLD
MC56F8246	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	48	60	–40° to + 105° C –40° to + 125° C	MC56F8246VLF MC56F8246MLF
MC56F8247	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	64	60	–40° to + 105° C –40° to + 125° C	MC56F8247VLH MC56F8247MLH
MC56F8255	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	44	60	–40° to + 105° C –40° to + 125° C	MC56F8255VLD MC56F8255MLD
MC56F8256	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	48	60	–40° to + 105° C –40° to + 125° C	MC56F8256VLF MC56F8256MLF
MC56F8257	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	64	60	–40° to + 105° C –40° to + 125° C	MC56F8257VLH MC56F8257MLH

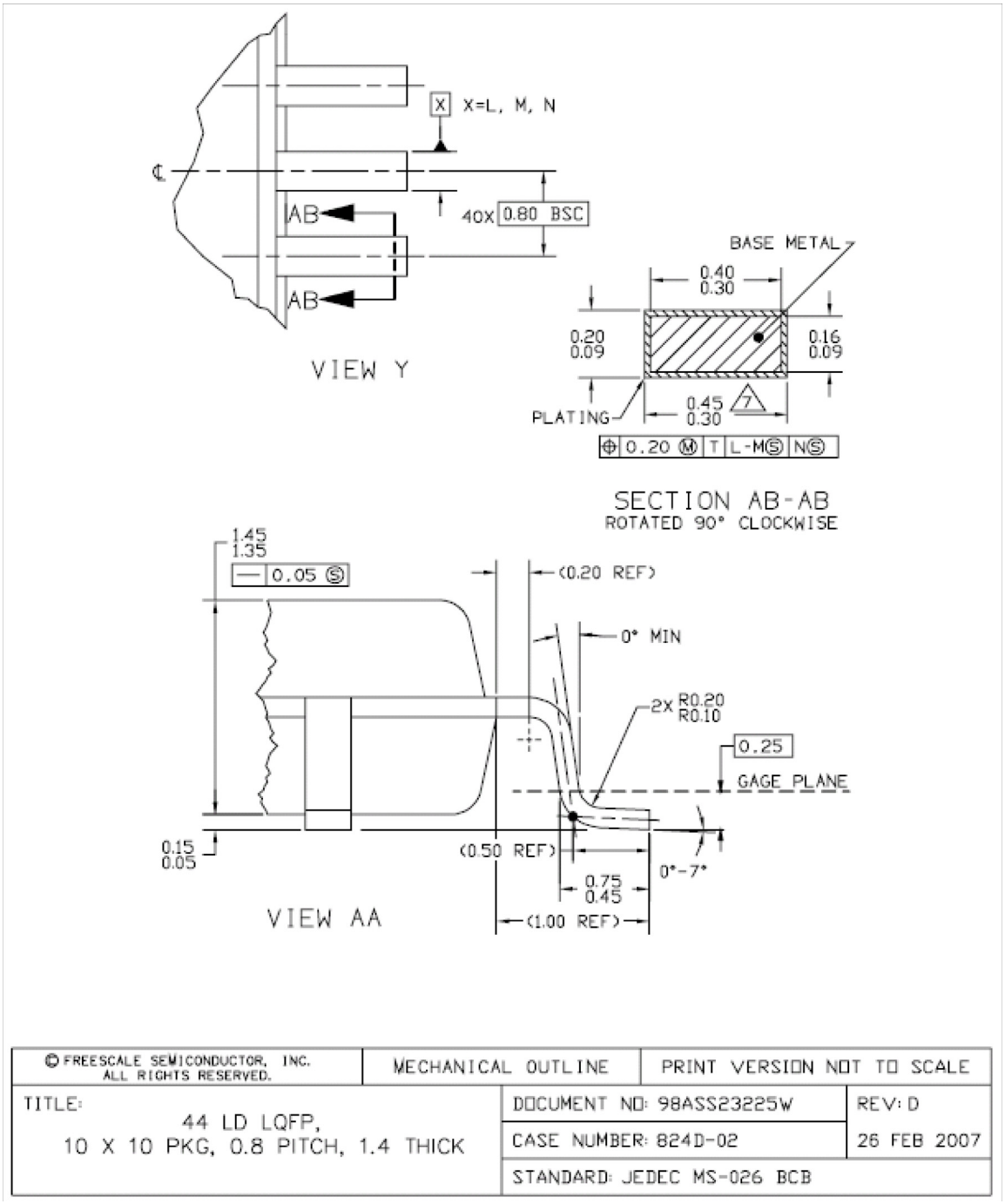
[1] All of the packages are RoHS compliant.

10 Package Mechanical Outline Drawings

To ensure you have the latest version of a package drawing, go to www.freescale.com and perform a keyword search for the drawing's document number (shown in the following sections for each package).

10.1 44-pin LQFP





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TITLE: 44 LD LQFP, 10 X 10 PKG, 0.8 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23225W	REV: D
	CASE NUMBER: 824D-02	26 FEB 2007
	STANDARD: JEDEC MS-026 BCB	

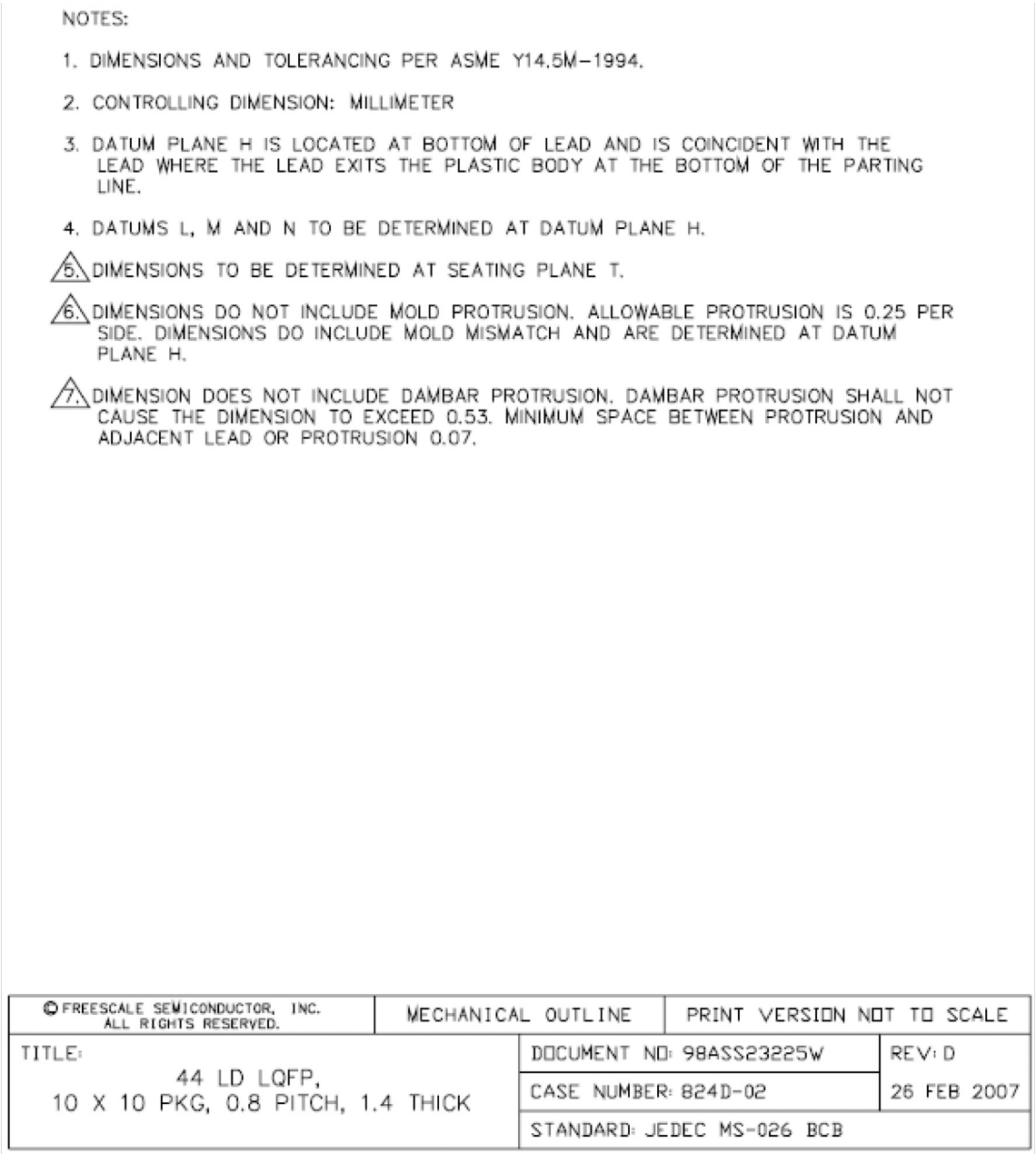
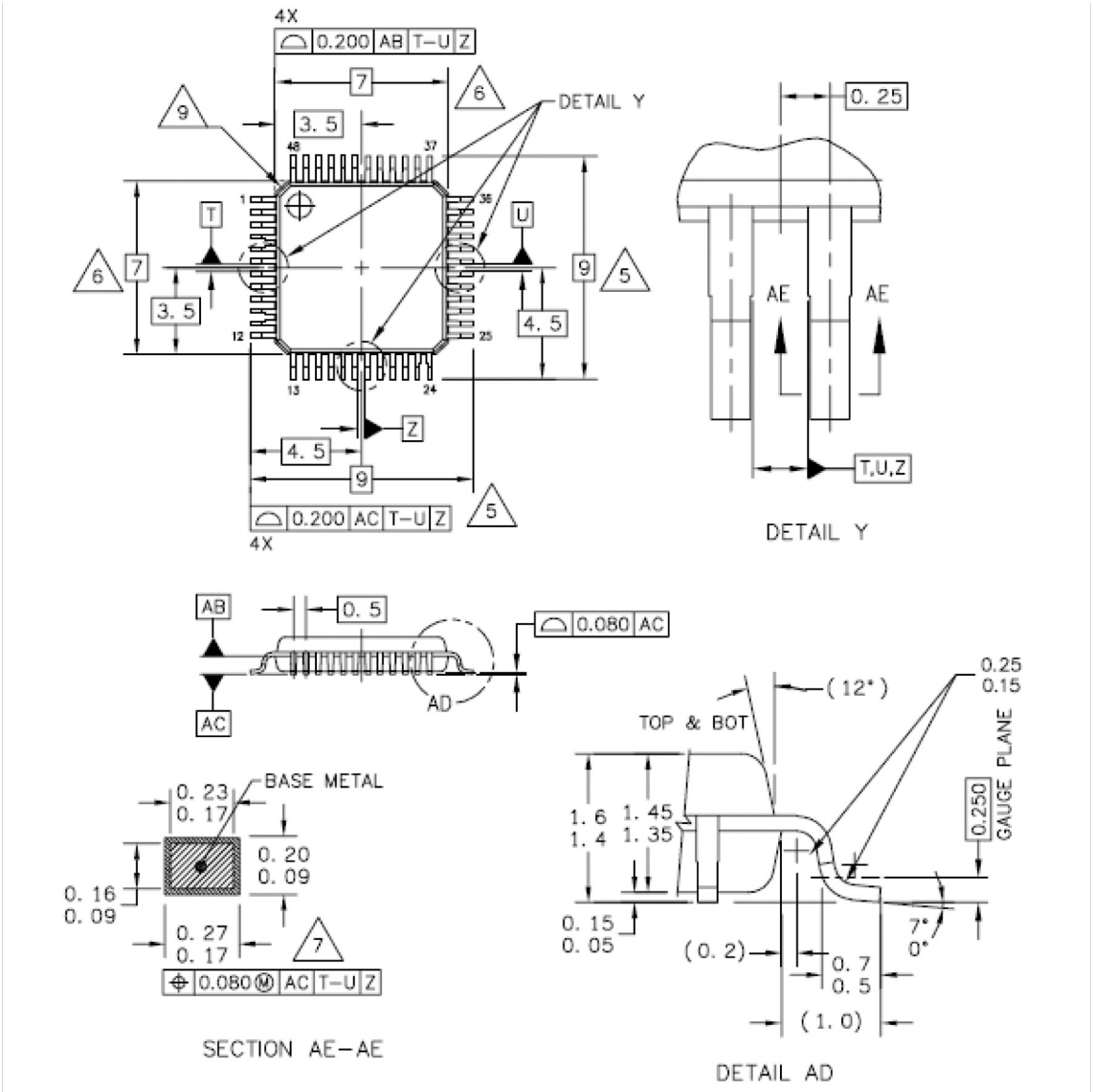


Figure 32. 56F8245 and 56F8255 44-Pin LQFP Mechanical Information

10.2 48-pin LQFP



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TITLE: LQFP, 48 LEAD, 0.50 PITCH (7.0 X 7.0 X 1.4)	DOCUMENT NO: 98ASH00962A	REV: G
	CASE NUMBER: 932-03	14 APR 2005
	STANDARD: JEDEC MS-026-BBC	

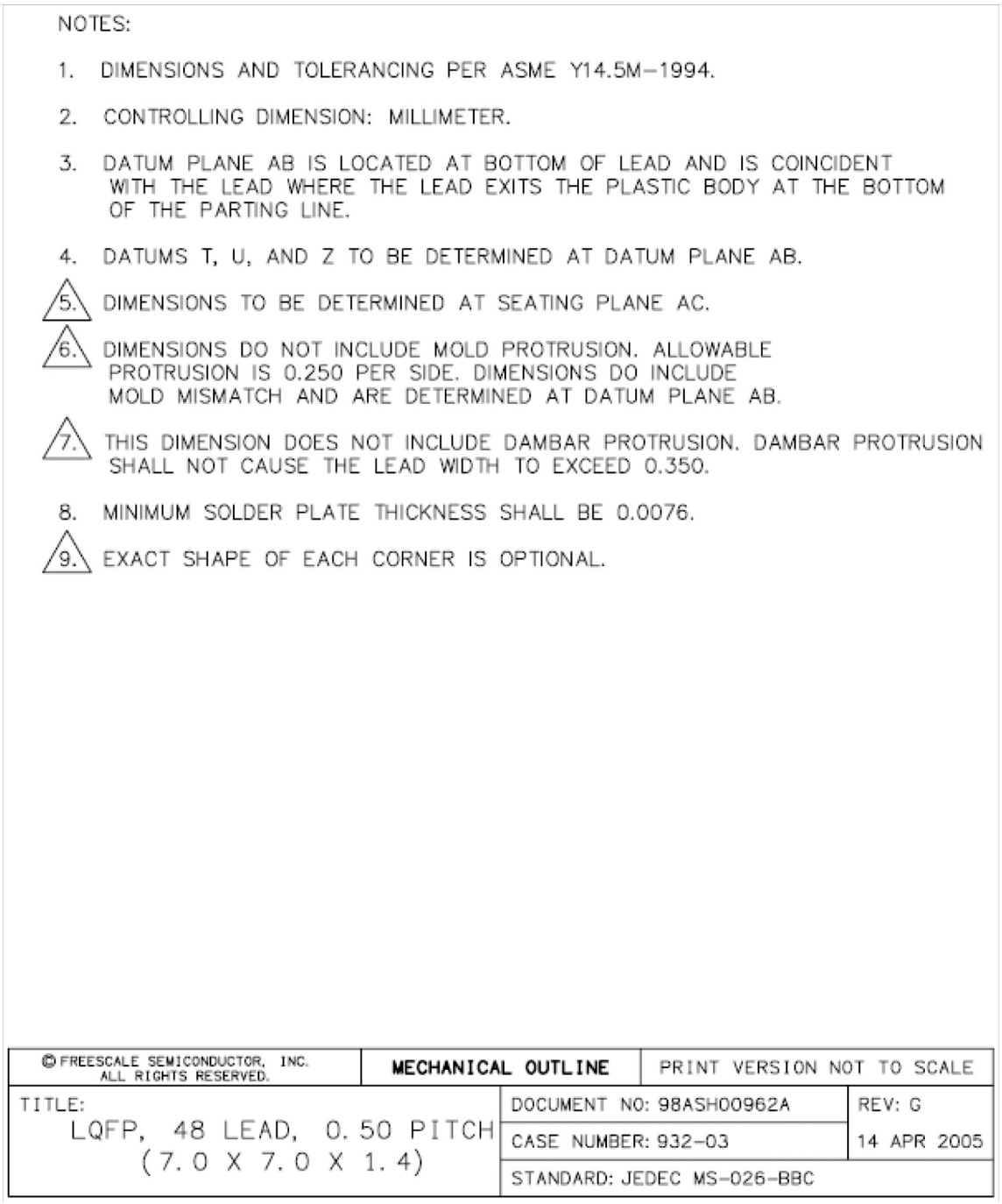
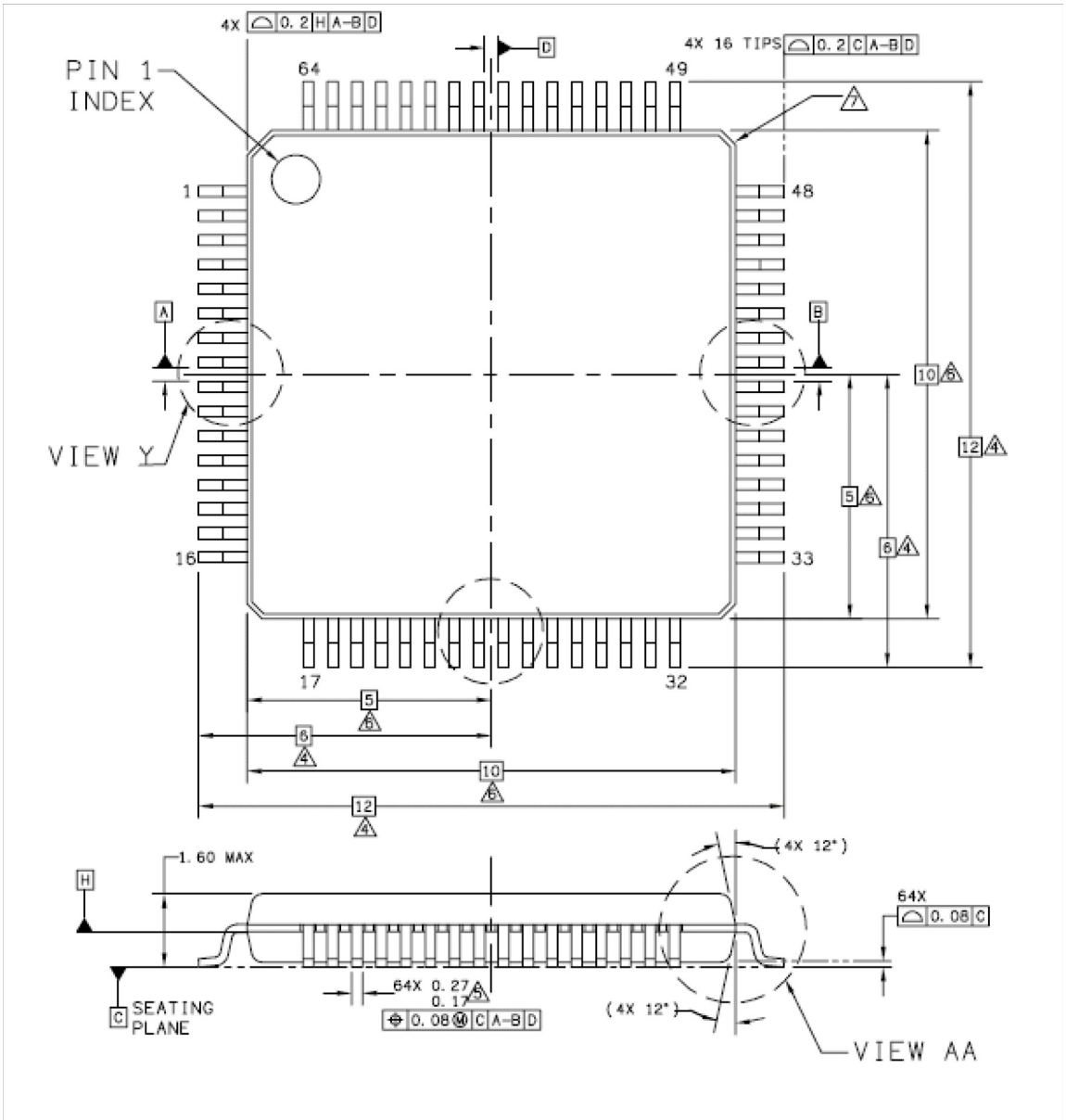


Figure 33. 56F8246 and 56F8256 48-Pin LQFP Mechanical Information

10.3 64-pin LQFP



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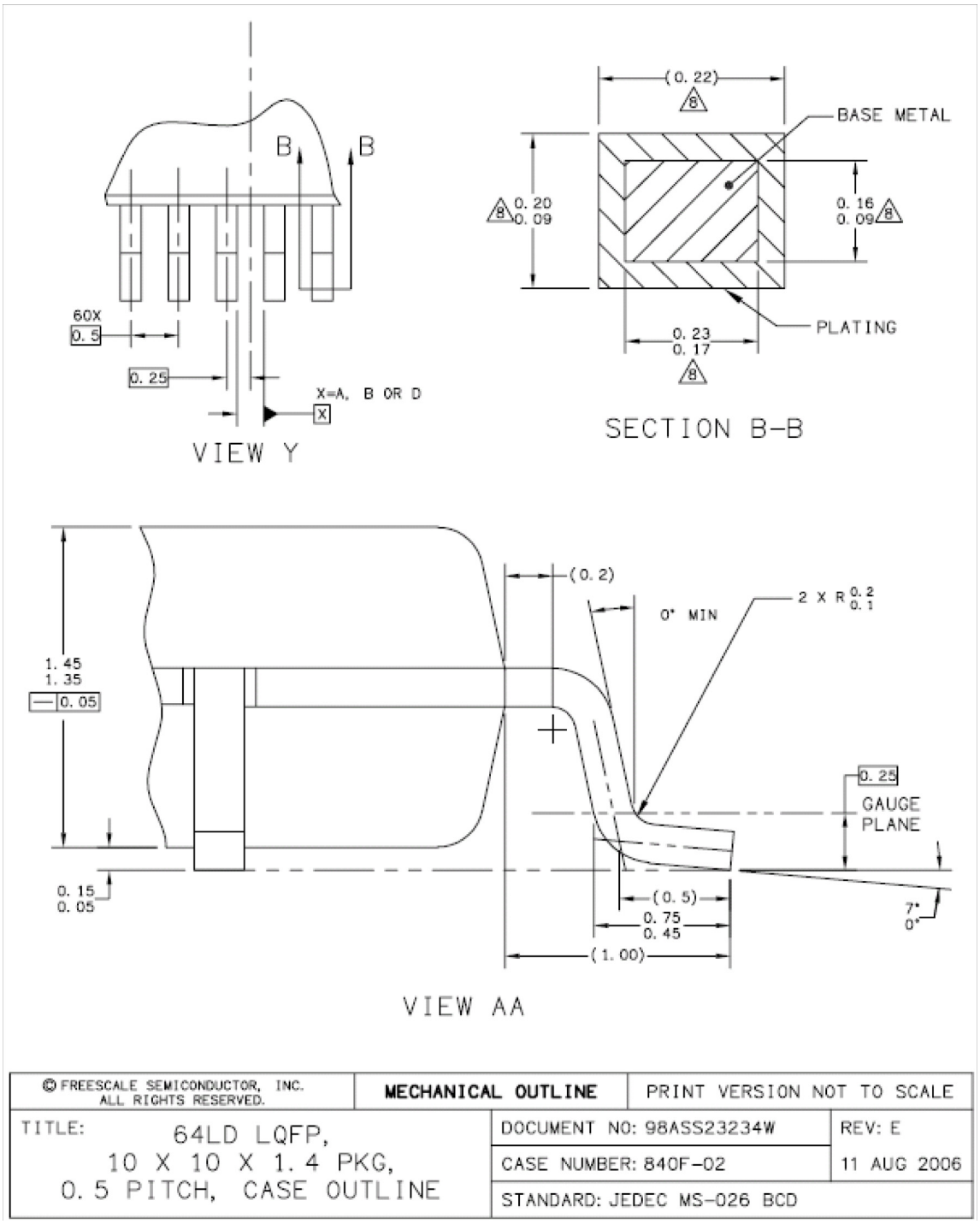
TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASS23234W	REV: E
	CASE NUMBER: 840F-02	11 AUG 2006
	STANDARD: JEDEC MS-026 BCD	


B
B
60X
0.5
0.25
X=A, B OR D
X
VIEW Y
(0.22)
B
BASE METAL
0.20
0.09
B
0.16
0.09
B
PLATING
0.23
0.17
B
SECTION B-B
1.45
1.35
0.05
(0.2)
0° MIN
2 X R 0.2 0.1
0.25
GAUGE
PLANE
0.15
0.05
(0.5)
0.75
0.45
(1.00)
7°
0°
VIEW AA
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MECHANICAL OUTLINE
PRINT VERSION NOT TO SCALE
TITLE:
64LD LQFP,
10 X 10 X 1.4 PKG,
0.5 PITCH, CASE OUTLINE
DOCUMENT NO: 98ASS23234W
REV: E
CASE NUMBER: 840F-02
11 AUG 2006
STANDARD: JEDEC MS-026 BCD

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.

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TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASS23234W	REV: E
	CASE NUMBER: 840F–02	11 AUG 2006
	STANDARD: JEDEC MS–026 BCD	

Figure 34. 56F8247 and 56F8257 64-Pin LQFP Mechanical Information

11 Revision History

Table 47 summarizes changes to the document since the release of the previous version.

Table 47. Revision History

Revision	Date	Description
Rev. 3	2011-04-22	Table 46 on page 75: Added “M” orderable part numbers Table 24 on page 55: Updated data for run, wait, and stop modes, and added data for standby and powerdown modes Table 23 on page 54: Added minimum and maximum values for Internal Pull-Up Resistance Renumbered sections: Section 9 (was 8.3), Section 10 (was 9), Section 11 (was 10)
Rev. 4	2014-06-13	Table 17 on page 49: Added data about junction temperature. Added data about M temperature grade devices to operating temperature range information. Operating temperature range information that was present in previous revision is unchanged but now refers to V temperature grade devices. Changes were made at these locations: Table 1 on page 3; Section 2.1.2, “Operation Range” on page 4; Table 17 on page 49; Table 22 on page 52; Table 24 on page 55.

Appendix A
Interrupt Vector Table

Table 48 provides the MC56F825x/MC56F824x's reset and interrupt priority structure, including on-chip peripherals. The table is organized with higher-priority vectors at the top and lower-priority interrupts lower in the table. As indicated, the priority of an interrupt can be assigned to different levels, allowing some control over interrupt priorities. All level 3 interrupts are serviced before level 2 and so on. For a selected priority level, the lowest vector number has the highest priority.

The location of the vector table is determined by the vector base address (VBA). See the device's reference manual for details.

By default, the chip reset address and COP reset address correspond to vector 0 and 1 of the interrupt vector table. In these cases, the first two locations in the vector table must contain branch or JMP instructions. All other entries must contain JSR instructions.

Table 48. Interrupt Vector Table Contents[1]

Peripheral	Vector Number	Priority Level	Vector Base Address +	Interrupt Function
Core			P:0x00	Reserved for Reset Overlay[2]
Core			P:0x02	Reserved for COP Reset Overlay
Core	2	3	P:0x04	Illegal Instruction
Core	3	3	P:0x06	SW Interrupt 3
Core	4	3	P:0x08	HW Stack Overflow
Core	5	3	P:0x0A	Misaligned Long Word Access
Core	6	1–3	P:0x0C	EOnCE Step Counter
Core	7	1–3	P:0x0E	EOnCE Breakpoint Unit
Core	8	1–3	P:0x10	EOnCE Trace Buffer
Core	9	1–3	P:0x12	EOnCE Transmit Register Empty
Core	10	1–3	P:0x14	EOnCE Receive Register Full
Core	11	2	P:0x16	SW Interrupt 2
Core	12	1	P:0x18	SW Interrupt 1
Core	13	0	P:0x1A	SW Interrupt 0
PS	14	1–3	P:0x1C	Low-Voltage Interrupt
OCCS	15	1–3	P:0x1E	Phase-Locked Loop Loss of Locks and Loss of Clock
TMRB3	16	0–2	P:0x20	Quad Timer B, Channel 3 Interrupt
TMRB2	17	0–2	P:0x22	Quad Timer B, Channel 2Interrupt
TMRB1	18	0–2	P:0x24	Quad Timer B, Channel 1Interrupt
TMRB0	19	0–2	P:0x26	Quad Timer B, Channel 0 Interrupt
ADCB_CC	20	0–2	P:0x28	ADCB Conversion Complete Interrupt
ADCA_CC	21	0–2	P:0x2A	ADCA Conversion Complete Interrupt
ADC_Err	22	0–2	P:0x2C	ADC Zero crossing, Low limit, and high limit interrupt
CAN	23	0–2	P:0x2E	CAN Transmit Interrupt
CAN	24	0–2	P:0x30	CAN Receive Interrupt

Table 48. Interrupt Vector Table Contents[1] (continued)

Peripheral	Vector Number	Priority Level	Vector Base Address +	Interrupt Function
CAN	25	0–2	P:0x32	CAN Error Interrupt
CAN	26	0–2	P:0x34	CAN Wake-Up Interrupt
QSCI1	27	0–2	P:0x36	QSCI1 Receiver Overrun/Errors
QSCI1	28	0–2	P:0x38	QSCI1 Receiver Full
QSCI1	29	0–2	P:0x3A	QSCI1 Transmitter Idle
QSCI1	30	0–2	P:0x3C	QSCI1 Transmitter Empty
QSCI0	31	0–2	P:0x3E	QSCI0 Receiver Overrun/Errors
QSCI0	32	0–2	P:0x40	QSCI0 Receiver Full
QSCI0	33	0–2	P:0x42	QSCI0 Transmitter Idle
QSCI0	34	0–2	P:0x44	QSCI0 Transmitter Empty
QSPI	35	0–2	P:0x46	SPI Transmitter Empty
QSPI	36	0–2	P:0x48	SPI Receiver Full
I^2C1	37	0–2	P:0x4A	I^2C1 Interrupt
I^2C0	38	0 -2	P:0x4C	I^2C0 Interrupt
TMRA3	39	0 -2	P:0x4E	Quad Timer A, Channel 3 Interrupt
TMRA2	40	0 -2	P:0x50	Quad Timer A, Channel 2 Interrupt
TMRA1	41	0 -2	P:0x52	Quad Timer A, Channel 1 Interrupt
TMRA0	42	0 -2	P:0x54	Quad Timer A, Channel 0 Interrupt
eFlexPWM	43	0 -2	P:0x56	PWM Fault
eFlexPWM	44	0 -2	P:0x58	PWM Reload Error
eFlexPWM	45	0 -2	P:0x5A	PWM Sub-Module 3 Reload
eFlexPWM	46	0 -2	P:0x5C	PWM Sub-Module 3 input capture
eFlexPWM	47	0 -2	P:0x5E	PWM Sub-Module 3 Compare
eFlexPWM	48	0 -2	P:0x60	PWM Sub-Module 2 Reload
eFlexPWM	49	0 -2	P:0x62	PWM Sub-Module 2 Compare
eFlexPWM	50	0 -2	P:0x64	PWM Sub-Module 1 Reload
eFlexPWM	51	0 -2	P:0x66	PWM Sub-Module 1 Compare
eFlexPWM	52	0 -2	P:0x68	PWM Sub-Module 0 Reload
eFlexPWM	53	0 -2	P:0x6A	PWM Sub-Module 0Compare
FM	54	0 -2	P:0x6C	Flash Memory Access Error
FM	55	0 -2	P:0x6E	Flash Memory Programming Command Complete
FM	56	0 -2	P:0x70	Flash Memory Buffer Empty Request
CMPC	57	0–2	P:0x72	Comparator C Rising/Falling Flag
CMPB	58	0–2	P:0x74	Comparator B Rising/Falling Flag

Table 48. Interrupt Vector Table Contents[1] (continued)

Peripheral	Vector Number	Priority Level	Vector Base Address +	Interrupt Function
CMPA	59	0–2	P:0x76	Comparator A Rising/Falling Flag
GPIOF	60	0–2	P:0x78	GPIOF Interrupt
GPIOE	61	0–2	P:0x7A	GPIOE Interrupt
GPIOD	62	0–2	P:0x7C	GPIOD Interrupt
GPIOC	63	0–2	P:0x7E	GPIOC Interrupt
GPIOB	64	0–2	P:0x80	GPIOB Interrupt
GPIOA	65	0–2	P:0x82	GPIOA Interrupt
SWILP	66	-1	P:0x84	SW Interrupt Low Priority

1 Two words are allocated for each entry in the vector table. This does not allow the full address range to be referenced from the vector table, providing only 19 bits of address.

2 If the VBA is set to the reset value, the first two locations of the vector table overlay the chip reset addresses because the reset address would match the base of this vector table.

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