THE DATASHEET OF

MC34844AEP

Document Number: MC34844
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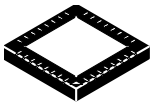
10 Channel LED Backlight Driver with Integrated Power Supply

34844

LED DRIVER



EP SUFFIX (PB-FREE)
98ASA10800D
32-PIN QFN-EP

The 34844 is a SMARTMOS high efficiency, LED driver for use in backlighting LCD displays from 10" to 20"+. Operating from supplies of 7.0 to 28 V, the MC34844 is capable of driving up to 160 LEDs in 10 parallel strings. Current in the 10 strings is matched to within ±2%, and can be programmed via the I^2C/SM Bus interface.

The 34844 also includes a Pulse Width Monitor (PWM) generator for LED dimming. The LEDs can be dimmed to one of 256 levels, programmed through the I^2C/SM Bus interface. Up to 65,000:1 (256:1 PWM, 256:1 Current DAC) dimming ratio.

The integrated boost converter generates the minimum output voltage required to keep all LEDs illuminated with the selected current, providing the highest efficiency possible.

The 34844 has an integrated boost self-clock at a default frequency of 600 kHz, but may be programmed via I^2C to 150/300/600/1200 kHz. The PWM frequency can be set from 100 Hz to 25 kHz, or can be synchronized to an external input. If not synchronized to another source, the internal PWM rate outputs on the CK pin. This enables multiple devices to be synchronized together.

The 34844 has a default boost frequency of 320 kHz, but may be programmed via I^2C to 160/320/650/1300 kHz. The PWM frequency can be set from 110 Hz to 27 kHz, or can be synchronized to an external input. If not synchronized to another source, the internal PWM rate outputs on the CK pin. This enables multiple devices to be synchronized together.

The 34844 also supports optical/temperature closed loop operation and features LED overtemperature protection, LED short protection, and LED open circuit protection. The IC includes overvoltage protection, overcurrent protection, and undervoltage lockout.

Features

- Input voltage of 7.0 to 28 V
- 2.5 A integrated boost FET
- Up to 80 mA on the 34844 LED current per channel
- 90% efficiency (DC:DC)
- I^2C/SM Bus interface
- 10 channel current mirror with ±2.0% current matching
- Boost output voltage up to 60V, with Dynamic Headroom Control (DHC)
- PWM frequency programmable or synchronizable from 110 to 27,000 Hz
- 32-Ld 5x5x1.0 mm TQFN Package

Applications

- Monitors and HDTV - up to 42 inch
- Personal Computer Notebooks
- GPS Screens
- Small screen Televisions

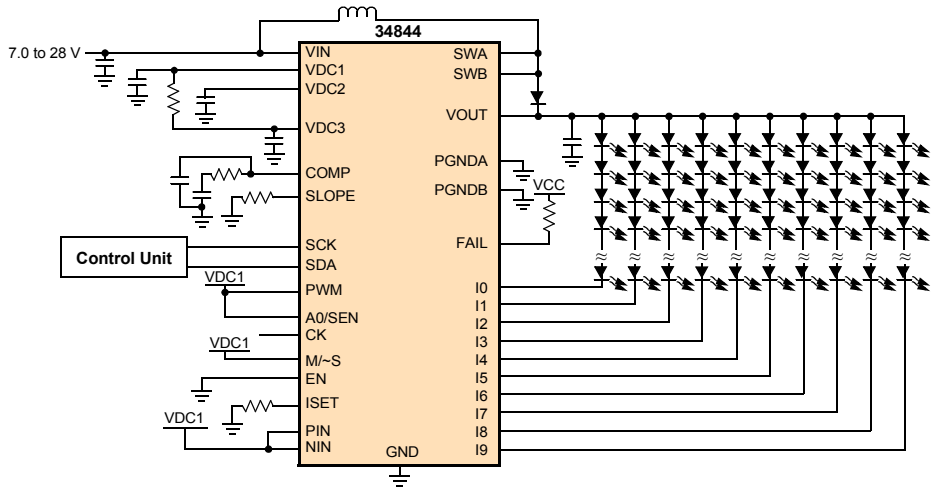


Figure 1. MC34844 Simplified Application Diagram (SM Bus Mode)

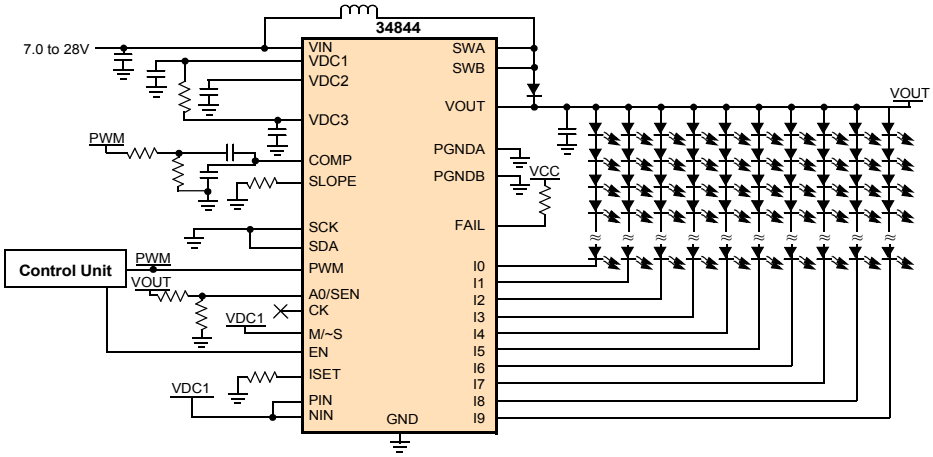


Figure 2. MC34844 Simplified Application Diagram (Manual Mode)

ORDERABLE PARTS

This section describes the part numbers available to be purchased along with their differences. Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to http://www.freescale.com and perform a part number search for the following device numbers.

Table 1. Orderable Part Variations

Part Number	Notes	Temperature (T_A)	Package
MC34844AEP	(1)	-40 to 105 °C	32 QFN-EP

Notes:
1. To order parts in Tape & Reel, add the R2 suffix to the part number.

INTERNAL BLOCK DIAGRAM

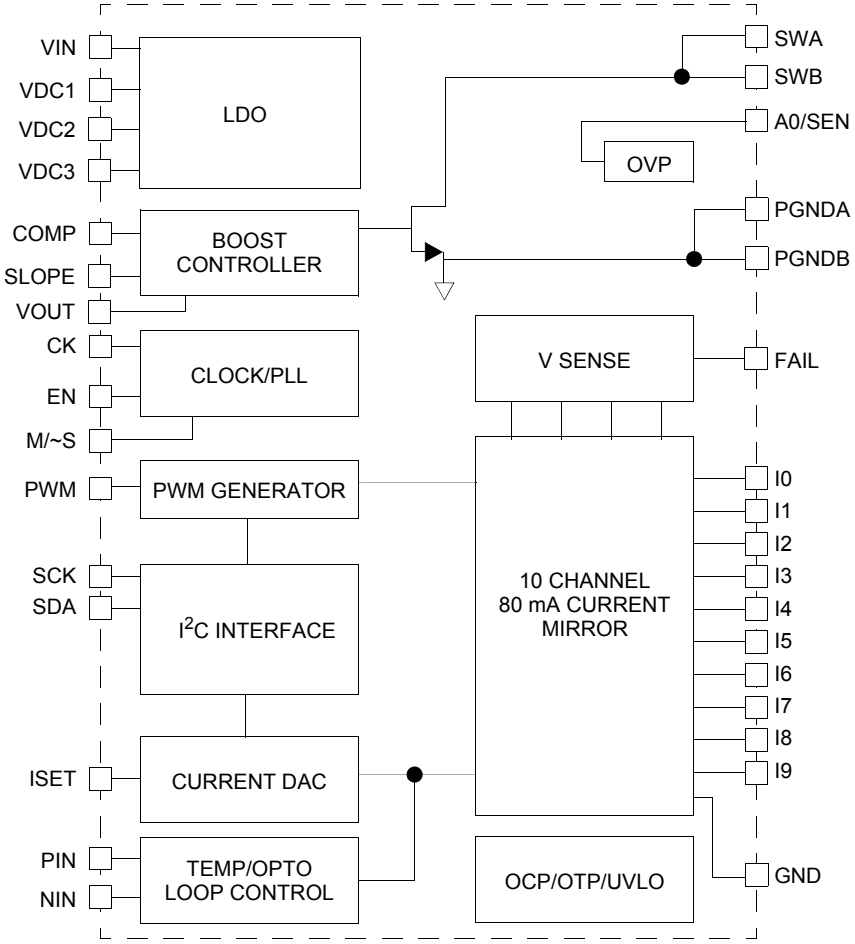


Figure 3. 34844 Simplified Internal Block Diagram

PIN CONNECTIONS

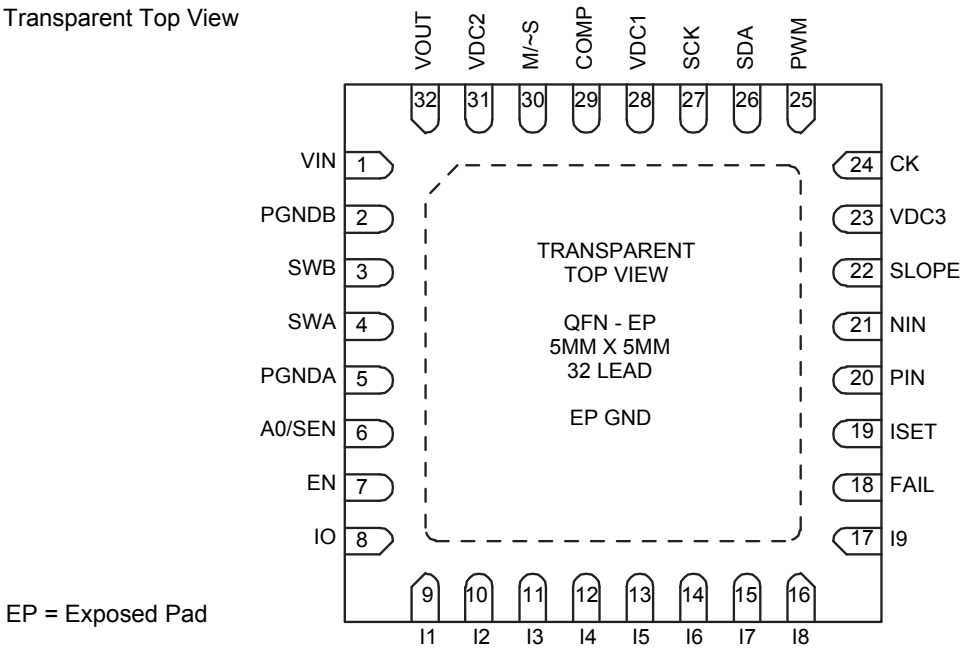


Figure 4. 34844 Pin Connections

A functional description of each pin can be found in the Functional Pin Description section beginning on page 13.

Table 2. 34844 Pin Definitions

Pin Number	Pin Name	Pin Function	Formal Name	Definition
1	VIN	Power	Input voltage	Input supply
2	PGNDB	Power	Power Ground	Power ground
3	SWB	Input	Switch node B	Boost switch connection B
4	SWA	Input	Switch node A	Boost switch connection A
5	PGNDA	Power	Power Ground	Power ground
6	A0/SEN	Input	Device Select	Address select, device select pin or OVP HW control
7	EN	Input	Enable	Enable pin (active high, internal pull-up)
8 - 17	I0-I9	Input	LED Channel	LED string connections
18	FAIL	Open Drain	Fault detection	Fault detected pin (open drain): No Failure = low-impedance Failure = high-impedance
19	ISET	Passive	Current set	LED current setting resistor
20	PIN	Input	Positive current scale	Positive input analog current control
21	NIN	Input	Negative current scale	Negative input analog current control
22	SLOPE	Passive	Boost Slope	Boost slope compensation setting resistor
23	VDC3	Output	Internal Regulator 3	Decoupling capacitor for internal phase locked loop power
24	CK	Input/Output	Clock signal	Clock synchronization pin (input for M/~S = low - internal pull-up, output for M/~S = high)
25	PWM	Input	External PWM	External PWM input (internal pull-down)

Table 2. 34844 Pin Definitions (continued)

Pin Number	Pin Name	Pin Function	Formal Name	Definition
26	SDA	Bidirectional	I^2C data	I^2C data line
27	SCK	Bidirectional	I^2C clock	I^2C clock line
28	VDC1	Output	Internal Regulator 1	Decoupling capacitor for internal logic rail
29	COMP	Passive	Compensation pin	Boost converter type compensation pin
30	M/~S	Input	Master/Slave selector	Selects Master mode (1) or Slave mode (0)
31	VDC2	Output	Internal Regulator 2	Decoupling capacitor for internal regulator
32	VOUT	Input	Voltage Output	Boost output voltage sense pin
EP	GND	-	Ground	Ground reference for all internal circuits other than boost FET

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 3. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
ELECTRICAL RATINGS				
V_{MAX}	Maximum Pin Voltages A0/SEN I0, I1, I2, I3, I4, I5, I6, I7, I8, I9 EN, VIN SWA, SWB, VOUT FAIL, PIN, NIN, ISET, M/~S, CK, PWM	 7.0 45 30 65 6.0	V	(5)
I_{MAX}	Maximum LED Current	85	mA	
V_{ESD}	ESD Voltage Human Body Model (HBM) Machine Model (MM)	 ±2000 ±200	V	(2)
THERMAL RATINGS				
T_A	Ambient Temperature Range	-40 to 105	°C	
$T_{\theta JA}$	Junction to Ambient Temperature	32	°C/W	(3)
$T_{\theta JC}$	Junction to Case Temperature	3.5	°C/W	(3)
T_J	Maximum junction temperature	150	°C	
TSTO	Storage temperature range	-40 to 150	°C	
T_{PPRT}	Peak Package Reflow Temperature During Reflow	260	°C	(4)
	Power Dissipation TA = 25 °C TA = 70 °C TA = 85 °C TA = 105 °C	 3.9 2.5 2.0 1.4	W	

Notes

2. ESD testing is performed in accordance with the Human Body Model (HBM) (AEC-Q100-2), and the Machine Model (MM) (AEC-Q100-003), R_{ZAP} = 0 Ω
3. Per JEDEC51 Standard for Multilayer PCB
4. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
5. 45 V is the Maximum allowable voltage on all LED channels in off-state.

STATIC AND DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Static and Dynamic Electrical Characteristics

Characteristics noted under conditions V_{IN} = 12 V, V_{OUT} = 42 V, PWM = VDC1, M/~S = VDC1, PIN & NIN = VDC1, -40°C ≤ T_A ≤ 105°C, PGND = 0 V, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
SUPPLY						
V_{IN}	Supply Voltage	7.0	12	28	V	(8)
$I_{SHUTDOWN}$	Supply Current when Shutdown Mode Manual: PWM = Low, EN = Low, SCK & SDA=Low SM Bus: EN bit = 0, SCK & SDA=Low, EN pin= Low I^2C: SETI2Cbit=1, CLRI2C=0, EN bit= 0, EN pin = Low	 - -	 2.0 17	 - -	µA	
I_{SLEEP}	Supply Current when Sleep Mode SM-Bus: EN = low, SCK & SDA = Active, SETI2C bit = 0, EN bit = 0 I^2C: EN = High, SETI^{2}C bit = 1, CLRI^{2}C bit = 0, EN bit = 0	-	4.0	-	mA	
$I_{OPERATIONAL}$	Supply Current when Operational Mode Manual: EN = High, SCK & SDA =Low, PWM = Low, SM-Bus: EN = Low, SCK & SDA = Active, EN bit = 1, PWM = Low I^2C: EN = High, SETI^{2}C bit = 1, CLRI^{2}C bit = 0, EN bit = 1, PWM = Low	-	13.0	-	mA	
UVLO	Undervoltage Lockout (V_{IN} Rising)	5.4	6.0	6.4	V	
$UVLO_{HYST}$	Undervoltage Hysteresis (V_{IN} Falling)	-	300	-	mV	
V_{DC1}	VDC1 Voltage C_{VDC1} = 2.2 µF	2.3	2.5	2.75	V	(6)
V_{DC2}	VDC2 Voltage C_{VDC2} = 2.2 µF	5.5	6.0	6.5	V	(6)
V_{DC3}	VDC3 Voltage C_{VDC3} = 2.2 µF	2.3	2.5	2.75	V	(6)
BOOST						
V_{OUT1} V_{OUT2}	Output Voltage Range VIN = 7.0 V VIN = 28 V	 8.0 32	 - -	 28 60	V	(7) (8)
I_{FET}	Boost Switch Current Limit	2.3	2.5	2.7	A	
t_{BOOST_TIME}	Boost Switch Current Limit Timeout	-	10	-	ms	
$R_{DS(ON)}$	$R_{DS(ON)}$ of Internal FET (I_{DRAIN}= 1.0 A)(	-	250	500	mΩ	
I_{BOOST_LEAK}	Boost Switch Off-state Leakage Current $V_{SWA,SWB}$ = 65 V	-	-	10	mA	
$VOUT_{LEAK}$	Feedback pin Off-state Leakage Current (V_{OUT} = 65 V)	-	500	700	mA	
EFF_{BOOST}	Peak Boost Efficiency	-	90	-	%	(8)
I_{OUT}/V_{IN}	Line Regulation - VIN = 7.0 to 28 V	-0.2	-	0.2	%/V	(8)
I_{OUT}/V_{LED}	Load Regulation - VLED = 8.0 to 65 V (all Channels)	-0.2	-	0.2	%/V	(8)

Notes
6. This output is for internal use only and not to be used for other purposes. A 1.0 kΩ resistor between the VDC3 and VDC1 pin is recommended for <-20 °C operation.
7. Minimum and Maximum output voltages are dependent on Min/Max duty cycle and current limit condition.
8. Guaranteed by design

Table 4. Static and Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions V_{IN} = 12 V, V_{OUT} = 42 V, PWM = VDC1, M/~S = VDC1, PIN & NIN = VDC1, -40°C ≤ T_A ≤ 105°C, PGND = 0 V, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
BOOST (CONTINUED)						
V_{SLOPE}	Slope compensation voltage ramp - R_{SLOPE} = 68 kΩ	-	0.49	-	V/µs	
A_{CSA}	Current Sense Amplifier Gain	-	9.0	-		
R_{SENSE}	Current Sense Resistor	-	22	-	mΩ	
G_M	OTA Transconductance	-	200	-	µS	
I_{SS}	Transconductance Sink and Source Current Capability	-	100	-	µA	
FAIL PIN						
I_{FAIL_LEAK}	Off-state Leakage Current - V_{FAIL} = 5.5 V	-	-	50	µA	
V_{OL}	On-state Voltage Drop - I_{SINK} = 4.0 mA	-	-	0.4	V	
LED CHANNELS						
I_{SINK}	Sink Current ICHx Register = 255, PIN&NIN = Disabled, T_A=25 °C RISET=3.48 kΩ, 0.1%	78.4	80	81.6	mA	
V_{MIN}	Regulated minimum voltage across drivers, Pulse Width > 400 ns	625	700	775	mV	
I_{MATCH}	Current Matching Accuracy	-2.0	-	2.0	%	
V_{SET}	I_{SET} Pin Voltage RISET=3.48 kΩ, 0.1%	2.007	2.048	2.069	V	
$ILED_{RES}$	LED Current Amplitude Resolution 1.0 mA ≤ I_{LED} ≤ 80 mA	-	1.5	-	%	
I_{CH_LEAK}	Off-state Leakage Current, All channels - (V_{CH} = 45 V)	-	-	10	µA	
PIN INPUT						
V_{PIN_DIS}	Voltage to Disable PIN mode	2.2	-	-	V	
I_{PIN}	PIN Bias Current PIN = V_{SET}	-2.0	-	2.0	µA	
I_{DIM_PIN}	Analog Dimming Current, ICHx Register = 255, RISET=3.48 kΩ 0.1% PIN = V_{SET}/2 PIN = V_{SET}	 36 76	 40 80	 44 84	mA	
NIN INPUT						
V_{NIN_DIS}	Voltage to Disable NIN mode	2.2	-	-	V	
I_{NIN}	NIN Bias Current NIN = V_{SET}	-2.0	-	2.0	µA	
I_{DIM_NIN}	Analog Dimming Current ICHx Register = 255, RISET=3.48 kΩ 0.1% NIN = V_{SET}/2 NIN = 0 V	 36 76	 40 80	 44 84	mA	

Table 4. Static and Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions V_{IN} = 12 V, V_{OUT} = 42 V, PWM = VDC1, M/~S = VDC1, PIN & NIN = VDC1, -40°C ≤ T_A ≤ 105°C, PGND = 0 V, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
OVER-TEMPERATURE PROTECTION						
O_{TT}	Over-temperature Threshold Rising Hysteresis	150 -	165 25	175 -	°C	(9)
I^2C/SM BUS PHYSICAL LAYER [SCK, SDA]						
ADR_{I2C}	I^2C Address	-	1110110	-	Binary	
ADR_{SMB}	SM-Bus Address	-	1110110	-	Binary	
V_{ILI}	Input Low Voltage	-0.3	-	0.8	V	
V_{IHI}	Input High Voltage	2.1	-	5.5	V	
V_{HYSI}	Input Hysteresis	-	0.3	-	V	
V_{OLI}	Output Low Voltage Sink Current ≤ 4.0 mA	-	-	0.4	V	
I_{INI}	Input Current	-5.0	-	5.0	µA	
C_{INI}	Input Capacitance	-	-	10	ρF	(9)
LOGIC INPUTS / OUTPUTS (CK, M/~S, PWM, A0/SEN, EN)						
V_{ILL}	Input Low Voltage	-0.3	-	0.5	V	
V_{IHL}	Input High Voltage	1.5	-	5.5	V	
V_{HYSL}	Input Hysteresis	-	0.1	-	V	
V_{ILL}	Input Low Voltage (EN)	-0.3	-	0.5	V	
V_{IHL}	Input High Voltage (EN)	2.1	-	28	V	
V_{OLL}	Output Low Voltage (CK) I_{SINK} ≤ 2.0 mA	-	-	0.45	V	
V_{OHL}	Output High Voltage (CK) I_{SOURCE} ≤ 2.0 mA	2.2	-	5.5	V	
IIIL	Input Current	-5.0	-	5.0	µA	
C_{INI}	Input Capacitance	-	-	5.0	ρF	(9)
OVER-VOLTAGE PROTECTION						
Over-voltage Clamp - OVP Register Table:						
OVP_{FH}	OVP = Fh (Default)	60.5	62.5	64.5	V	
OVP_{EH}	OVP = Eh	56.5	58	60	V	
OVP_{DH}	OVP = Dh	53	54	56	V	
OVP_{CH}	OVP = Ch	49	51	52.5	V	
OVP_{BH}	OVP = Bh	45	47	48.5	V	
OVP_{AH}	OVP = Ah	41	43	44.5	V	
OVP_{9H}	OVP = 9h	38	39	40.5	V	
OVP_{8H}	OVP = 8h	34	36	37.5	V	
OVP_{7H}	OVP = 7h	30.5	32	33.5	V	

Notes
9. Guaranteed by design

Table 4. Static and Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions V_{IN} = 12 V, V_{OUT} = 42 V, PWM = VDC1, M/~S = VDC1, PIN & NIN = VDC1, -40°C ≤ T_A ≤ 105°C, PGND = 0 V, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
OVER-VOLTAGE PROTECTION (CONTINUED)						
Over-voltage Clamp - OVP Register Table:						
OVP_{6H}	OVP = 6h	26	28	30	V	
OVP_{5H}	OVP = 5h	23	24	25	V	
OVP_{HW}	Over-voltage threshold, Set by Hardware, Voltage at A0/SEN	6.15	6.5	6.85	V	
I_{SINK_OVP}	A0/SEN Sink Current, T_A=25°C	70	100	130	µA	
BOOST						
f_{SW0}	Switching Frequency (BST [1:0]=0)	0.14	0.16	0.18	MHz	
f_{SW1}	Switching Frequency (BST [1:0]=1) (Default)	0.29	0.32	0.35	MHz	
f_{SW2}	Switching Frequency (BST [1:0]=2)	0.59	0.65	0.72	MHz	
f_{SW3}	Switching Frequency (BST [1:0]=3)	1.17	1.30	1.42	MHz	
f_{SW}	Boost Switching Frequency	0.29	0.32	0.35	MHz	
D_{MIN}	Minimum Duty Cycle	-	10	15	%	
D_{MAX}	Maximum Duty Cycle	80	85	-	%	
t_{SS}	Soft Start Period	-	6.5	-	ms	
t_{TR}	Boost Switch Rise Time	-	15	-	ns	(10)
t_F	Boost Switch Fall Time	-	25	-	ns	(10)
PWM GENERATOR						
$fPWM_S$	PWM Frequency Range M/~S = Low (Slave Mode)	110	-	27000	Hz	(10)
$fPWM_M$	PWM Frequency, M/~S = High (Master Mode) FPWM Register = 768 FPWM Register = 192,000	 25000 103	 27000 110	 29000 112	Hz	
t_{fPWM}	PWM dimming resolution	-	0.39	-	%	
PWM PIN (DIRECT PWM CONTROL)						
t_{PWM_IN}	Input PWM Pin Minimum Pulse	150	-	-	ns	(10)
fPWM	Input PWM Frequency Range	110	-	27000	Hz	
PHASE LOCK LOOP						
fCK_S	CK Slave Mode Frequency Lock Range, M/~S = Low (Slave Mode)	110	-	27000	Hz	(11)
fCK_{S_JITTER}	CK Slave Mode Input Jitter, M/~S = Low (Slave Mode)	-	-	0.1	%	(10)
T_{S_ACQ}	Slave Mode Acquisition Time, M/~S = Low (Slave Mode) $FPWM_S$=27 kHz $FPWM_S$=110 Hz	 - -	 50 2000	 - -	ms	
fCK_{MASTER}	CK Frequency (Master Mode) FPWM Register = 768 FPWM Register = 192,000	 25000 103	 27000 110	 29000 112	Hz	

Notes

10. Guaranteed by design
11. Special considerations should be made for frequencies between 110 Hz to 1.0 KHz. Please refer to Functional Device Operation for further details.

Table 4. Static and Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions V_{IN} = 12 V, V_{OUT} = 42 V, PWM = VDC1, M/~S = VDC1, PIN & NIN = VDC1, -40°C ≤ T_A ≤ 105°C, PGND = 0 V, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Unit	Notes
I^2C/SM BUS PHYSICAL LAYER [SCK, SDA]						
f_{SCK}	Interface Frequency Range			400	kHz	
t_{RST}	SM Bus Power-on-Reset Time	-	100	-	ms	
$t_{SHUTDOWN}$	SM Bus Shut down mode Timeout	-	30	-	ms	
t_F	Output fall time 10 ρF ≤ C_L ≤ 400 ρF	40	-	160	ns	(12)
t_R	Output rise time 10 ρF≤C_L≤400 ρF	20	-	80	ns	(12)
LOGIC OUTPUT (CK)						
t_R/t_F	Output Rise and Fall time C_L≤100 ρF	-	25	-	ns	
LED CHANNELS						
t_R/t_F	Channels Rise and Fall Time	-	23	50	ns	(12)

Notes

12. Guaranteed by design

FUNCTIONAL DESCRIPTION

INTRODUCTION

LED backlighting is very popular for small and medium LCDs, due to some advantages over other backlighting schemes, such as the widely used cold cathode fluorescent lamp (CCFL). The advantages of LED backlighting are low cost, long life, immunity to vibration, low operational voltage, and precise control over its intensity. However, there is an important drawback of this method. It requires more power than most of the other methods, and this is a major problem if the LCD size is large enough.

To address the power consumption problem, solid state optoelectronics technologies are evolving to create brighter LEDs with lower power consumption. These new technologies together with highly efficient power management LED drivers are turning LEDs, a more suitable solution for backlighting of almost any size of LCD panel, with really conservative power consumption.

One of the most common schemes for backlighting with LED is the one known as “Array backlighting”. This creates a matrix of LEDs all over the LCD surface, using defraction and diffused layers to produce an homogenous and even light at the LCD surface. Each row or column is formed by a number of LEDs in series, forcing a single current to flow through all LEDs in each string.

Using a current control driver, per row or column, helps the system to maintain a constant current flowing through each line, keeping a steady amount of light even with the presence of line or load variations. They can also be use as a light intensity control by increasing or decreasing the amount of current flowing through each LED string.

To achieve enough voltage to drive a number of LEDs in series, a boost converter is implemented to produce a higher voltage from a smaller one, which is typically used by the logical blocks to do their function. The 34844 implements a single channel boost converter together with 10 input channels, for driving up to 16 LEDs per string to create a matrix of more than 160 LEDs. Together with its 90% efficiency and I^2C programmable or external current control, among other features, makes the 34844 a perfect solution for backlighting small and medium size LCD panels, on low power portable and high definition devices.

FUNCTIONAL PIN DESCRIPTION

INPUT VOLTAGE SUPPLY (VIN)

IC Power input supply voltage, is used internally to produce internal voltage regulation (VDC1, VDC3) for logic functioning, and also as an input voltage for the boost regulator.

INTERNAL VOLTAGE REGULATOR 1 (VDC1)

This pin is for internal use only, and not to be used for other purposes. A capacitor of 2.2 μF should be connected between this pin and ground for decoupling purposes.

INTERNAL VOLTAGE REGULATOR 2 (VDC2)

This pin is for internal use only, and not to be used for other purposes. A capacitor of 2.2 μF should be connected between this pin and ground for decoupling purposes.

INTERNAL VOLTAGE REGULATOR 3 (VDC3)

This pin is for internal use only, and not to be used for other purposes. A capacitor of 2.2 μF should be connected between this pin and ground for decoupling purposes. A 1.0 kΩ resistor between the VDC3 and VDC1 pin is recommended for <-20 °C operation.

BOOST COMPENSATION PIN (COMP)

Passive terminal used to compensate the boost converter. Add a capacitor and a resistor in series to GND to stabilize the system.

IC ENABLE (EN)

The active high enable terminal is internally pulled high through pull-up resistors. Applying 0V to this terminal would stop the IC from working.

INPUT/OUTPUT CLOCK SIGNAL (CK)

This terminal can be used as an output clock signal (master mode), or input clock signal (slave mode), to synchronize more than one device.

MASTER/SLAVE MODE SELECTION (M/~S)

Setting this pin high puts the device into Master mode, producing an output synchronization clock at the CK terminal. Setting this pin low, puts the device in Slave mode, using the CK pin as an input clock.

EXTERNAL PWM INPUT (PWM)

This terminal is internally pulled down. An external PWM signal can be applied to modulate the LED channel directly in absence of an I^2C interface.

CLOCK I^2C SIGNAL (SCK)

Clock line for I^2C communication.

ADDRESS I^2C SIGNAL (SDA)

Address line for I^2C communication.

A0/SEN

Address select, device select pin, or hardware overvoltage protection (OVP) control.

CURRENT SET (ISET)

Each LED string can drive up to 50 mA. The maximum current can be set by using a resistor from this pin to GND.

POSITIVE CURRENT SCALING (PIN)

Positive current scaling factor for the external analog current control. Applying 0 V to this pin, scales the current to near 0%, and in the same way, applying V_{SET} (2.048 V Typ.), the scale factor is 100%. By applying a voltage higher than 2.2 V, the scaling factor is disabled, and the internal pull-ups are activated.

If PIN pin and NIN pin are used at the same time then by applying 0 V to the PIN pin and V_{SET} to NIN pin, scales the current to near 0%, and in the same way, applying V_{SET} to the PIN pin and 0 V to NIN pin, scales the current to 100%. By applying a voltage higher than 2.2 V, the scaling factor is disabled and the internal pull-ups are activated in both pins.

NEGATIVE CURRENT SCALING (NIN)

Negative current scaling factor for the external analog current control. Setting 0 V to this pin scales the current to 100%, in the same way, setting V_{SET} (2.048 V Typ.) the scale factor is near 0%. By applying a voltage higher than 2.2 V, the scaling factor is disabled and the internal pull-ups are activated.

If the PIN and NIN pin are used at the same time, then by applying 0 V to the PIN pin and V_{SET} to NIN pin, it scales the current to near 0%, and in the same way, applying V_{SET} to the PIN pin and 0 V to NIN pin, scales the current to 100%. By applying a voltage higher than 2.2 V, the scaling factor is disabled and the internal pull-ups are activated in both pins.

GROUND (GND)

Ground Reference for all internal circuits other than the Boost FET. The Exposed Pad (EP) should be used for thermal heat dissipation.

I0-I9

Current LED driver, each line has the capability of driving up to 50 mA.

FAULT DETECTION PIN (FAIL)

When a fault situation is detected, this pin goes into high-impedance.

BOOST SLOPE COMPENSATION SETTING RESISTOR (SLOPE)

The resistor to be used for the SLOPE depends on the Input and Output voltage difference as well as the inductor value. Use the formula shown in the Components Calculation section to calculate the value accordingly.

POWER GROUND TERMINALS (PGNDA, PGNDB)

Ground terminal for the internal Boost FET.

OUTPUT VOLTAGE SENSE TERMINAL (VOUT)

Input terminal to monitor the output voltage. It supplies the input voltage for the internal regulator 2 (VDC2).

SWITCHING NODE TERMINALS (SWA, SWB)

Switching node of boost converter.

FUNCTIONAL INTERNAL BLOCK DESCRIPTION

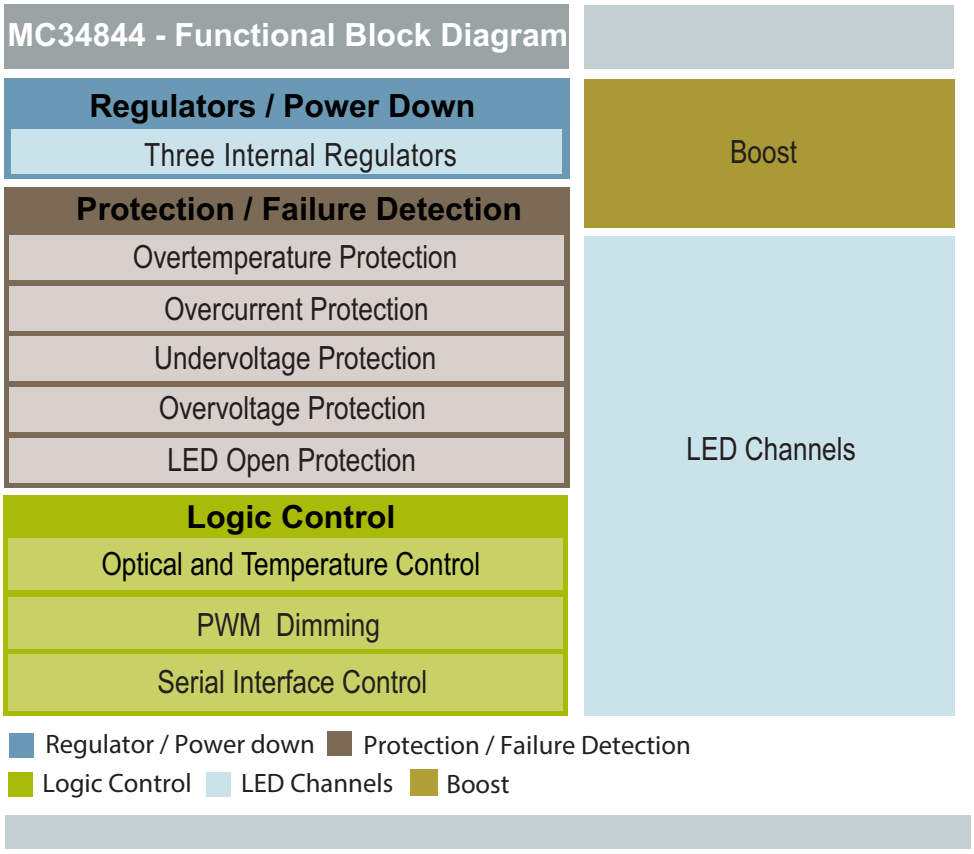


Figure 5. Functional Internal Block Diagram

REGULATORS

The 34844 is designed to operate from input voltages in the 7.0 to 28 V range. This is stepped down internally by LDOs to 2.5 V (VDC1 and VDC3) and 6 V (VDC3) for powering internal circuitry. If the input voltage falls below the UVLO threshold, the device automatically enters in shutdown mode.

Power UP Sequence:

The power up sequence for applying V_{IN}, with respect to the ENABLE and PWM signals is very important to assure a good performance of the part.

It is recommended to follow this sequence:

1. Apply V_{IN} first
2. Wait for a couple of milliseconds (~2.0 ms) to let the logic and internal regulators get settled
3. Take the EN pin high, or keep it low depending on the operating mode
4. Apply the PWM signal

Operating Modes:

The device can be operated by the EN pin and/or SDA/SCK bus lines, resulting in three distinct operation modes:

- Manual mode, there is no I^2C capability, the bus line pins must be tied low, and the EN pin controls the ON/OFF operation. To shutdown the part in Manual mode, first the PWM pin should be taken low followed by the EN pin. The part will not shutdown unless V_{OUT} collapses to a voltage below 30 V.
- SM Bus mode, EN pin must be tied low and the device is turned ON by any activity on the bus lines. The part shuts down if the bus lines are held low for more than 30 ms, the 30 ms watchdog timer can be disabled by I^2C (setting SETI2C bit high) or tying the EN pin high. In Sleep mode (EN bit=0) the device reduces the power consumption by leaving “alive” only the blocks required for I^2C communication.To shutdown the part in SM Bus mode, the EN bit should first be a '0', then the SCK and SDA should be taken low.

- I²C mode, has to be configured by I²C communication (SETI2C bit = 1) right after the IC is turned ON, it prevents the part from being turned ON/OFF by the bus. Sleep mode is also present and it is intended to save power, but still keep the IC prepared to communicate by I²C. By taking the EN bit low and then the EN pin low, the part enters into a shutdown mode.

Table 5. Operation Current Consumption Modes

MODE	EN Pin	SCK/SDA Pins	I²C Bit Command	Current Consumption Mode	Comments
Manual	Low	Low	N/A	Shutdown	PWM pin = Low
	High	Low	N/A	Operational	
SM Bus	Low	Low (> 27 ms)	EN bit = 0	Shutdown	
	Low	Active	EN bit = 0	Sleep	
	Low	Active	EN bit = 1	Operational	
I²C	Low	X	SETI2C bit = 1	I²C Low Power (Shutdown)	Part Doesn't Wake-up
			CLRI2C bit = 0		
			EN bit = 0		
	High	X	SETI2C bit = 1	Sleep	
			CLRI2C bit = 0		
			EN bit = 0		
	High	X	SETI2C bit = 1	Operational	
			CLRI2C bit = 0		
			EN bit = 1		

BOOST

The integrated boost converter operates in non-synchronous mode and integrates a 2.5 A FET. An integrated sense circuit is used to sense the voltage at the LED current mirror inputs and automatically sets the boost output voltage (DHC) to the minimum voltage needed to keep all LEDs biased with the required current. The DHC is designed to operate for pulse widths > 400 ns in the LED drivers.

If the pulse widths are shorter than specified, the DHC circuit will not operate and the voltage across the LED drivers increase to a value given by the OVP minus the total LED voltage in the LED string. Therefore it is imperative to select the proper OVP level to minimize power dissipation.

The user can program the boost frequency by I²C (BST[1:0]) only after the IC is powered up and before the boost circuit is turned ON for the first time (PWM pin low to high). This sequence avoids boost frequency to be changed inadvertently during operation. The first I²C command has to wait for 5.0 ms after the part is turned ON, to allow sufficient time for the device power up sequence to be completed.

Please follow this sequence to change the Boost frequency thru I²C:

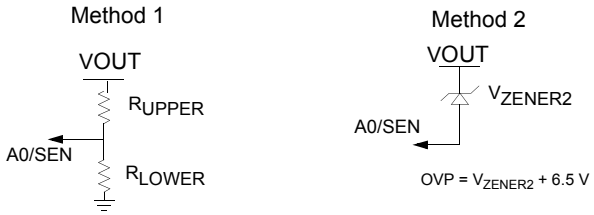
1. Take PWM pin low
2. Disable the part by software (EN bit = low)
3. Write the new Boost frequency data (BST[1:0])
4. Enable the part by software (EN bit = high)
5. Reconfigure all registers
6. Take PWM pin High

The boost controller has an integral track and hold amplifier with indefinite hold time capability, to enable immediate LED on cycles after extended off times. During extended off times, the external LEDs cool down from their normal quiescent operating temperature and thereby experience a forward voltage change, typically an increase in the forward voltage. This change can be significant for applications with a large number of series LEDs in a string operating at high current. If the boost controller did not track this increased change, the potential on the LED drivers would saturate for a few cycles once the LED channels are re-enabled.

HARDWARE AND SOFTWARE OVP:

The OVP value should be set to a higher value than the maximum LED voltage over the whole temperature range. A good practice is to set it 5.0 V or so above the max LED voltage.

The OVP can be set from 11 to 62 V, ~4.0 V spaced, using the I²C interface (OVP Register). If the I²C capability is not present, the OVP can be controlled either by a resistor divider connected from VOUT to GND, with its mid point tied to the A0/SEN pin, or by a zener diode from VOUT to the A0/SEN pin (threshold = 6.5 V). During an OVP condition, the output voltage goes to the OVP level, which is programmed via the I²C interface or settled by a resistor divider on A0/SEN pin, or by a zener diode. The formulas to calculate the hardware OVP using any of the two methods are as follows:



OVP = 6.5 V [(R_{UPPER} / R_{LOWER}) + 1] + (100E-6 x R_{UPPER})

OVERCURRENT PROTECTION (OCP)

The boost converter also features internal overcurrent protection (OCP) and has a user programmable overvoltage protection (OVP).

The OCP operates on a cycle by cycle basis. However, if the OCP condition remains for more than 10 ms then the device turns off the LED Drivers, the Boost goes to Sleep mode and the output FAULT pin goes into high-impedance. The device can only be restarted by recycling the enable or creating a Power On Reset (POR).

CURRENT MIRROR

The programmable current mirror matches the current in 10 LED strings to within 2%. The maximum current is set using a resistor to GND from the ISET pin. This can be scaled down using the I^2C interface to 255 levels.

Zero current is achieved by turning off the LED Driver by I^2C (registers CHENx = 0h) for a duty cycle from 0% to 99%, or by pulling PWM pin low regardless of the duty cycle.

I^2C capability allows the channels to be controlled individually or in parallel.

$$ISINK[A] = \frac{VSET[V] \times 136}{RISET[\Omega]} \times \frac{ICH[RegisterValue]}{255}$$

Current on LED Channel (PIN and NIN mode disabled) **Eqn. 1**

Default ICH[RegisterValue]=255

In the off state, the LEDs current is set to 0 and the boost converter stops switching.

This feature allows driving more than 80 mA of current by connecting the LED string to two or more LED channels in parallel. For example; if the application requires to drive a channels at 160 mA, then the bottom of each LED string should be connected to two channels to duplicate the current capability (Example: CH0+CH1 = 160 mA).

PWM GENERATOR

The PWM generator can operate in either master or slave modes, as set by the M/~S pin.

In master mode, the internal PWM generator frequency is programmed through the I^2C interface (registers FPWM). The default programmed value set the number of 27 kHz clocks (40 μs) in one PWM cycle. The 18-bit resolution allows minimum PWM frequencies of 110 Hz to be programmed. The resulting frequency is output on the CK pin.

$$FPWM[Hz] = \frac{20.736Mhz}{FPWM[RegisterValue]}$$

PWM Frequency **Eqn. 2**

In slave mode, the CK pin acts as an input. The internal digital PLL uses this frequency as the PWM frequency. By setting one device as master, and connecting the CK output to the input on a number of slave configured devices, all PWM frequencies are synchronized.

The duty cycle of the PWM waveform in both master and slave modes is set using a second register on the I^2C interface (register DPWM), and can be controlled from 100% duty cycle to 1/256 t_{PWM} = 0.39%. Zero percent of duty cycle is achieved by turning LED drivers off (register CHENx = 0h) or pulling PWM pin low.

An external PWM can also be used. The PWM input is 'AND'ed with the internal signal. By setting the serial interface to 100% duty cycle (default), the external pin has full control of the PWM duty cycle. This pin can also be used to modulate the LED at a lower frequency than the PWM dimming frequency (DHC Minimum pulse width = 400 ns).

POWER OFF AND POWER ON LED CHANNELS

The 34844 allows the user to Power OFF and Power ON any channel independently thru I2C/SM-BUS mode.

The POWER ON function reconnects the LED driver and the feedback circuit to the channel to allow functionality to that channel again.

On an opposite way when the channel is POWER OFF, the LED driver and feedback circuit are disconnected to the channels.

This function is very useful for applications where one or more channel has to be shutdown to avoid the output voltages goes to OVP during the start up of the part.

The sequence to make these functions work is the following:

To POWER ON LED channels:

1. Take PWM pin low
2. Set POWER ON bit high (MSB of Register 09)
3. Set high all Channels that should be power on by writing “1” on CHENx bits (Registers 08 & 09)
4. Clear POWER ON bit
5. Take PWM pin high

To POWER OFF LED channels:

1. Take PWM pin low
2. Set POWER OFF bit high (MSB of Register 08)
3. Clear all Channels that should be power off by writing “0” on CHENx bits (Registers 08 & 09)
4. Clear POWER OFF bit
5. Take PWM pin high

POWER ON bit and POWER OFF bits shouldn’t be set at the same time to avoid damage to the part.

POWER ON/OFF channels should be reconfigured every time the part recovered from a POR or shutdown condition. This also applies if the part is reenabled by software.

If the part is reenabled by software, it is recommended to take PWM pin low, reenable the part, then follow the corresponding sequence shown above.

DISABLING LED CHANNELS

The 34844 allows the user to enable and disable each of the 10 channels separately by writing the corresponding CHENx bit on Registers 08 and 09 thru I^2C.

Since the enable and disable functions reconnects the feedback circuit of the LED drivers, this shouldn’t be used on any channel that shuts down, because an open LED channel condition or because is was previously POWER OFF. This could cause instability issues, since the voltage on this open LED driver is not substantially above the DHC regulation voltage (0.75 V typ) and may interfere with the operation of the dynamic headroom control (DHC), leading to erratic output voltage regulation

FAIL PIN

If an LED fails to open in any of the LED strings, the voltage in that particular LED channel is close to ground and the LED open failure is detected. When this happens, a failure is registered, the FAIL pin is set to its high-impedance stage, and the channel is shutdown.

The FAIL pin cannot be cleared for Manual mode unless a complete power on reset is applied.

However for I^2C/SMBUS mode, the FAIL pin can be cleared by cycling the clear fail bit (CLRFAIL bit = 0 - 1 - 0). This allows the user to waive any known failure and set the device to able to detect any other failure during operation.

If the fail pin cannot be cleared by software, it indicates the failure is because of an overcurrent in the Boost. Since this is a critical failure, the only way to clear it is by releasing the part from the overcurrent condition and shutting down the part (Refer to Table 5)

If I^2C communication is not present, the FAIL condition should be reset by removing the failure and re-enabling the device thru the EN pin.

OPTICAL AND TEMPERATURE CONTROL LOOP

The 34844 supports both optical and temperature loop control.

The LED brightness can be adjusted for temperature loop control, depending on the temperature of the LEDs.

For optical loop control, the 34844 supports both optical closed loop backlight control, where the brightness of the backlight is maintained at a required level by adjusting the light output until the desired level is achieved, or with ambient light control, where the backlight brightness increases as ambient light increases.

Both temperature and optical loops are supported through the PIN and NIN pins. Each pin supports a 0 V to V_{SET} (2.048 V typ.) input range which affects the current through the LEDs. The PIN pin increases current as the voltage rises from 0 to V_{SET}. The NIN pin reduces current as the voltage rises from 0 - V_{SET}.

A 6.98 kΩ resistor or higher value must be used at the ISET pin if the part is configured to use PIN+NIN control loop functionality. The 80 mA maximum current is achieved at the higher allowed level of PIN/NIN pins, ensuring the maximum current of the LED Drivers are not exceeded.

The optical and temperature control loop can be disabled by the I^2C setting bits (PINEN & NINEN), or by tying PIN and NIN pins high (>2.2 V). The LED Driver maximum current is set to 80 mA by using a 3.48 kΩ resistor at the ISET pin.

$$IDIM[A] = ISINK[A] \times \frac{VPIN[V]}{2}$$

Current on LED Channel (PIN mode) **Eqn. 3**

$$IDIM[A] = ISINK[A] \times \frac{(VSET - VNIN)[V]}{2}$$

Current on LED Channel (NIN mode) **Eqn. 4**

$$IDIM[A] = ISINK[A] \times \frac{(VSET + VPIN - VNIN)[V]}{2}$$

Current on LED Channel (PIN+NIN mode) **Eqn. 5**

VPIN and VNIN is the voltage applied on PIN and NIN pins correspondingly.

For ISINK formula, refer to Equation 1.

LED FAILURE PROTECTION

Open LED Protection

If an LED fails open in any of the LED strings, the voltage on that channel is pulled close to zero, which causes the channel to be disabled. As a result, the boost output voltage goes to the OVP level and comes down to the regulation level, to continue powering the rest of the LED strings.

Short LED Protection

If an LED is shorted in any of the LED strings, the device continues to operate without interruption. However, if the shorted LED happens to be in the LED string with the highest forward voltage, the DHC circuit automatically regulates the output voltage with respect to the new highest LED voltage. If more LEDs are shorted in the same LED string, it may cause excessive power dissipation in the channel, which may cause the OTT circuit to trip completely shutting down the device.

OVERTEMPERATURE PROTECTION

The 34844 has an on-chip temperature sensor measuring die temperature. If the IC temperature exceeds the OTT threshold, the IC turns off all power sources inside the IC (LED drivers, boost and internal regulators) until the temperature falls below the falling OTT threshold. Once the chip is back on, it operates with the default configuration (refer to Table 7).

SERIAL INTERFACE CONTROL

The 34844 uses an I^2C interface capable of operating in standard (100 kHz) or fast (400 kHz) modes. The A0/SEN pin can be used as an address select pin to allow more than two devices in the system. The A0/SEN pin should be held low on all chips except the one to be addressed, where it is taken HIGH.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

NORMAL MODE

In normal operation, the 34844 is programed via I^2C to drive up to 50 mA of current through each one of the LED channels. The 34844 can be configured in master or slave mode as set by the M/~S pin.

In **Master mode**, the internal PWM generator frequency is programmed through the I^2C interface. The programmed value sets the number of 27 kHz clocks (37μs) in one PWM cycle. The 18-bit resolution allows minimum PWM frequencies of 110 Hz to be programmed. The resulting frequency is output on the CK pin.

In slave mode, the CK pin acts as an input. The internal digital PLL uses this frequency as the PWM frequency.

By setting one device as a master, and connecting the CK output to the input on a number of slave configured devices, all PWM frequencies are synchronized together. For this application A0/SEN pin indicates which device is enabled for I^2C control.

In **Slave mode**, an internal phase lock loop locks the internal PWM generator period to the period of the signal present at the CK pin. The PLL can lock to any frequency from 110 Hz to 27 KHz, provided the jitter is below 1000 ppm. At frequencies above 1.0 KHz, the PLL maintains the lock regardless of the transient power conditions imposed by the user (i.e. going from 0% duty cycle to 100% at 20 W LED display power). Below 1.0 kHz, thermal time constants on the die are such that the PLL may momentarily lose lock if the die temperature changes substantially during a large load power step. As explained further, this anomaly can be avoided by controlling the rate of change in PWM duty cycle.

To better understand this issue, consider the on chip PLL uses a VCO which is subject to thermal drift on the order of 1000 ppm/C. Furthermore, the thermal time constant of the chip is on the order of single digit milliseconds. Therefore, if a large power load step is imposed by the user (i.e. going from 0% duty cycle to 100% duty cycle with a load power of 20 W), the die experiences a large temperature wave gradient propagating across the chip surface, and thereby affects the instantaneous frequency of the VCO. As long as such changes are within the bandwidth of the PLL, the PLL is able to track and maintain lock. Exceeding this rate of change may cause the PLL to lose lock and the backlight is momentarily blanked until lock is reacquired.

At 110 Hz lock, the PLL has a bandwidth of approximately 10 Hz. This means that temperature changes on the order of 100 ms are tolerable without losing lock. Full load power changes on the order of 10 ms (i.e. 110 Hz PWM) are not tracked out and the PLL can momentarily lose lock. If this happens, as stated previously, the LED drivers are momentarily disabled until lock is reacquired. This is manifested as a perceivable short flash on the backlight immediately after the load change.

To avoid this problem, one can simply limit large instantaneous changes in die temperature by invoking only small power steps when raising or lowering the display power at low PWM frequencies. For example, to maintain lock while transitioning from 0% to 100% duty cycle at 20 W load power and a PWM frequency of 110 Hz would entail stepping the power at a rate not to exceed 1% per 10 ms. If a load of less than 20 W is used, the rate of rise can be increased. As the locked PWM frequency increases (i.e. use 600 Hz instead of 110 Hz), the step rate can be further increased to approximately 4% per 2.0 ms. The exact step rate to avoid loss of PLL lock is a function of essentially three things: (a) the composite thermal resistance of the user's PCB assembly, (b) the load power, and (c) the PWM frequency. For all cases below 1.0 KHz, simply using a rate of 1% duty cycle change per PWM period is adequate. If this is too slow, the value can be optimized experimentally once the hardware design is complete. At PWM rates above 1.0 KHz, it is not necessary to control the rate of change in PWM duty cycle.

It is important to point out when operating in the master mode, one does not need to concern themselves with loss of lock since the reference clock and the VCO clock are collocated on the die, and therefore experience the same thermal shift. Hence in master mode, once lock is initially acquired, it is not lost and no blanking of the display occurs.

The duty cycle of the PWM in both master and slave mode is set using a second register on the I^2C interface. An external PWM signal can also be applied in the PWM pin. This pin is AND'ed with the internal signal, giving the ability to control the duty cycle either via I^2C or externally by setting any of the 2 signals to 100% duty cycle.

MANUAL MODE

The 34844 can also be used in Manual mode without using the I^2C interface. By setting the pin M/~S High, the LED dimming is controlled by the external PWM signal. The overvoltage protection limit can be settled by a resistor divider or a zener diode on A0/SEN pin.

During manual mode, all internal Registers are in Default Configuration. Refer to Table 7. Under this configuration, the PIN and NIN pins are enabled to scale the current capability per string and may be disable by setting 2.2 V in the corresponding terminal.

In this mode, the device can also be enabled as follows:

- EN pin + PWM signal (Two Signals):

In this configuration, the PWM signal applied to PWM pin is in charge of controlling the LED dimming and a second signal enables or disables the chip through the EN pin.

- PWM Signal tied to SDA pin (Just ONE signal):

In this configuration, the PWM pin should be tied to the SDA pin. The PWM signal applied to PWM pin is in charge of controlling LED dimming and enabling the device every time the PWM is active. For this configuration the EN pin should be LOW.

I2C BUS SPECIFICATION

The 34844 is a unidirectional device that can only be written by an external control unit. Since the device is a 7 bit address device (1110110), the control unit needs to follow a specific data transfer format which is shown in Table 6.

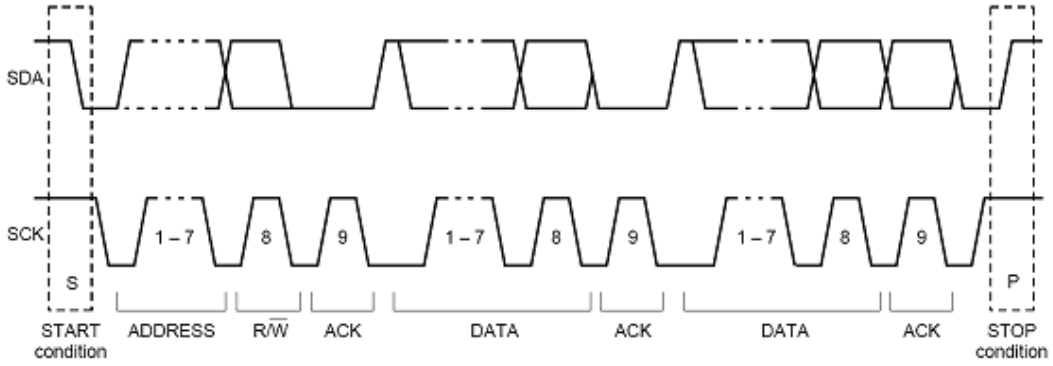


Figure 6. A Complete Data Transfer

For a complete data transfer, use this format in the following order:

1. START condition
2. 34844 device address and Write instruction (R/W = 0)
3. First data pack, it corresponds to the 34844 register needing to be written. (refer to Table 6)
4. Second data pack, it corresponds to the value which should be written to that register. (refer to Table 6)
5. STOP condition

I^2C variables description:

- START: this condition occurs when SDA changes from HIGH to LOW while SCK is HIGH.
- ACKNOWLEDGE: The acknowledge clock pulse is generated by the Master (Control Unit).
- The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse.The receiver (34844) must pull down the SDA line during this acknowledge pulse to indicate that the data was correctly written.
- Bits in the first byte: The first seven bits of the first bite make up the slave address. The eighth bit is the LSB (least significant bit), which determines the direction of the message (Write = 0)
  For the 34844 device, when an address is sent, each of the devices in a system compares the first seven bits after the START condition with its address. If they match, the device considers itself addressed by the control unit as a slave-receiver.
- STOP: this condition occurs when SDA changes from LOW to HIGH while SCK is HIGH

LOGIC COMMANDS AND REGISTERS

Table 6. Write Registers

reg / db	D7	D6	D5	D4	D3	D2	D1	D0
00	OVP3	OVP2	OVP1	OVP0		NINEN	PINEN	EN
01							CLRI2C	SETI2C
04			FPWM5	FPWM4	FPWM3	FPWM2	FPWM1	FPWM0
05			FPWM11	FPWM10	FPWM9	FPWM8	FPWM7	FPWM6
06			FPWM17	FPWM16	FPWM15	FPWM14	FPWM13	FPWM12
07	DPWM7	DPWM6	DPWM5	DPWM4	DPWM3	DPWM2	DPWM1	DPWM0
08	PWR_OFF			CHEN4	CHEN3	CHEN2	CHEN1	CHEN0
09	PWR_ON	CLRFAIL	ALL_OFF	CHEN9	CHEN8	CHEN7	CHEN6	CHEN5
14							BST1	BST0
F0	ICH0_7	ICH0_6	ICH0_5	ICH0_4	ICH0_3	ICH0_2	ICH0_1	ICH0_0
F1	ICH1_7	ICH1_6	ICH1_5	ICH1_4	ICH1_3	ICH1_2	ICH1_1	ICH1_0
F2	ICH2_7	ICH2_6	ICH2_5	ICH2_4	ICH2_3	ICH2_2	ICH2_1	ICH2_0
F3	ICH3_7	ICH3_6	ICH3_5	ICH3_4	ICHG_3	ICH3_2	ICH3_1	ICH3_0
F4	ICH4_7	ICH4_6	ICH4_5	ICH4_4	ICH4_3	ICH4_2	ICH4_1	ICH4_0
F5	ICH5_7	ICH5_6	ICH5_5	ICH5_4	ICH5_3	ICH5_2	ICH5_1	ICH5_0
F6	ICH6_7	ICH6_6	ICH6_5	ICH6_4	ICH6_3	ICH6_2	ICH6_1	ICH6_0
F7	ICH7_7	ICH7_6	ICH7_5	ICH7_4	ICH7_3	ICH7_2	ICH7_1	ICH7_0
F8	ICH8_7	ICH8_6	ICH8_5	ICH8_4	ICH8_3	ICH8_2	ICH8_1	ICH8_0
F9	ICH9_7	ICH9_6	ICH9_5	ICH9_4	ICH9_3	ICH9_2	ICH9_1	ICH9_0
FA	ICHG_7	ICHG_6	ICHG_5	ICHG_4	ICHG_3	ICHG_2	ICHG_1	ICHG_0

All registers and POWER ON/OFF channels should be reconfigured every time the part gets recovered from a POR or shutdown condition.

The configuration sequence every time the part is power up should be as follows:

1. Take the PWM pin low
2. Power up the part
3. Configure all registers
4. Take the PWM pin High

For configuring the part once in operation it is recommended to follow this sequence:

1. Take the PWM pin low
2. Configure the registers
3. Take the PWM pin High

Special considerations should be taken for re-configuring POWER ON/OFF functions, please refer to the POWER OFF and POWER ON LED CHANNELS section.

Table 7. Register Description

Register Name	Default Value (Hex)	Description
EN	1	Chip Enable by software.
PINEN	1	PIN pin enable (0 = OFF, 1 = ON)
NINEN	1	NIN pin enable (0 = OFF, 1 = ON)
OVP[3:0]	F	OVP voltage
SETI2C	0	SET I^2C communication (Disable SM Bus mode)
CLRI2C	0	Clear set I^2C
FPWM[17:0]	300	PWM Frequency
DPWM[7:0]	FF	PWM Duty Cycle (FFh = 100%)
CHEN[9:0]	3FF	Channel Enable (0 = OFF, 1 = ON)
ALL_OFF	0	All 10 channels OFF at the same. To reactivate channels this bit should be clear.
CLRFAIL	0	Clear fail if channels are re-enable.
PWR_OFF	0	POWER OFF LED channels (0 = disable, 1 = enable)
PWR_ON	0	POWER ON LED channels (0 = disable, 1 = enable)
BST[1:0]	2	Boost Frequency (160, 320, 650, 1300 kHz) [0h = 160 Hz]
ICH#[7:0]	FF	Channel Current Program (FFh = Maximum Current)
ICHG[7:0]	FF	Global Current Program

Table 8. Overvoltage Protection

Register (hex)	OVP Value (vOLTS)
2	11
3	15
4	19
5	23
6	27
7	31
8	35
9	39
A	43
B	47
C	51
D	55
E	59
F	62

TYPICAL APPLICATIONS

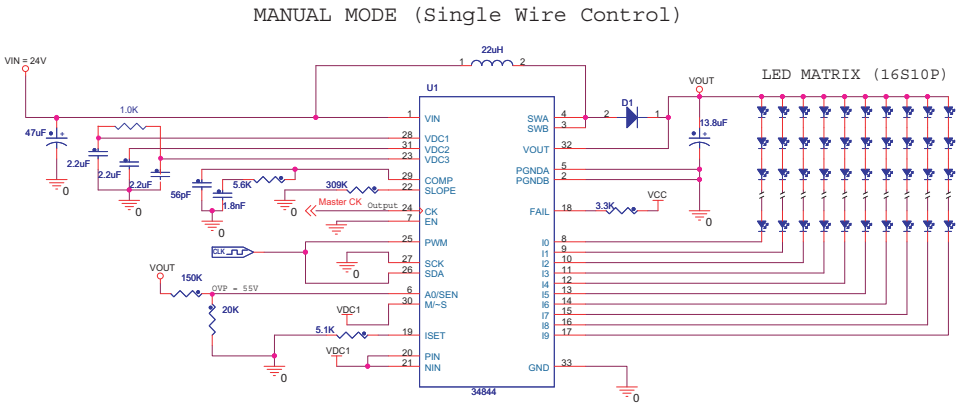


Figure 7. Manual Mode (Single Wire Control)
Conditions: V_{IN} = 24 V, V_{OUT} = 47 V, Load = 16S10P, I_{LED} = 60 mA, OVP = 53V, f_{SW} = 300 kHz

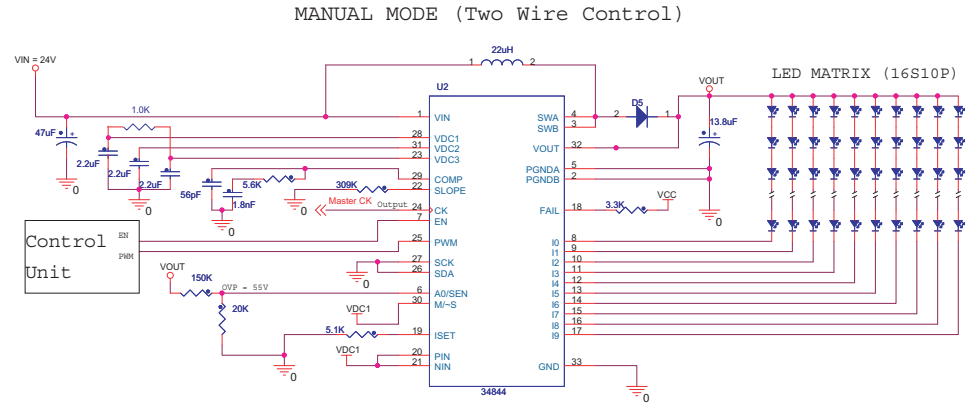


Figure 8. Manual Mode (Two Wire Control)
Conditions: V_{IN} = 24 V, V_{OUT} = 47 V, Load = 16S10P, I_{LED} = 60 mA, OVP = 53V, f_{SW} = 300 kHz

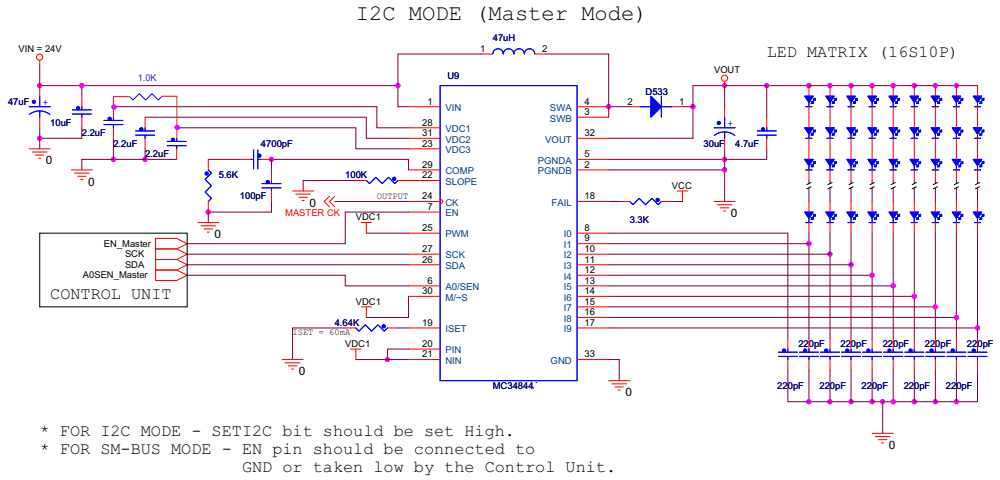


Figure 9. I²C (Master Mode)
Conditions: V_{IN} = 24 V, V_{OUT} = 47 V, Load = 16S10P, I_{LED} = 60 mA, OVP = 53V, f_{SW} = 300 kHz

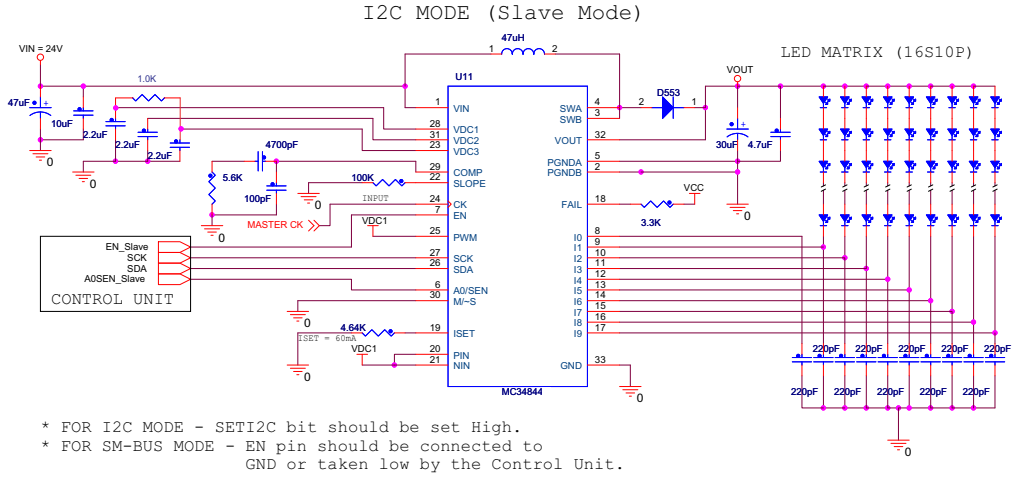


Figure 10. I²C (Slave Mode)
Conditions: V_{IN} = 24 V, V_{OUT} = 47 V, Load = 16S10P, I_{LED} = 60 mA, OVP = 53V, f_{SW} = 300 kHz

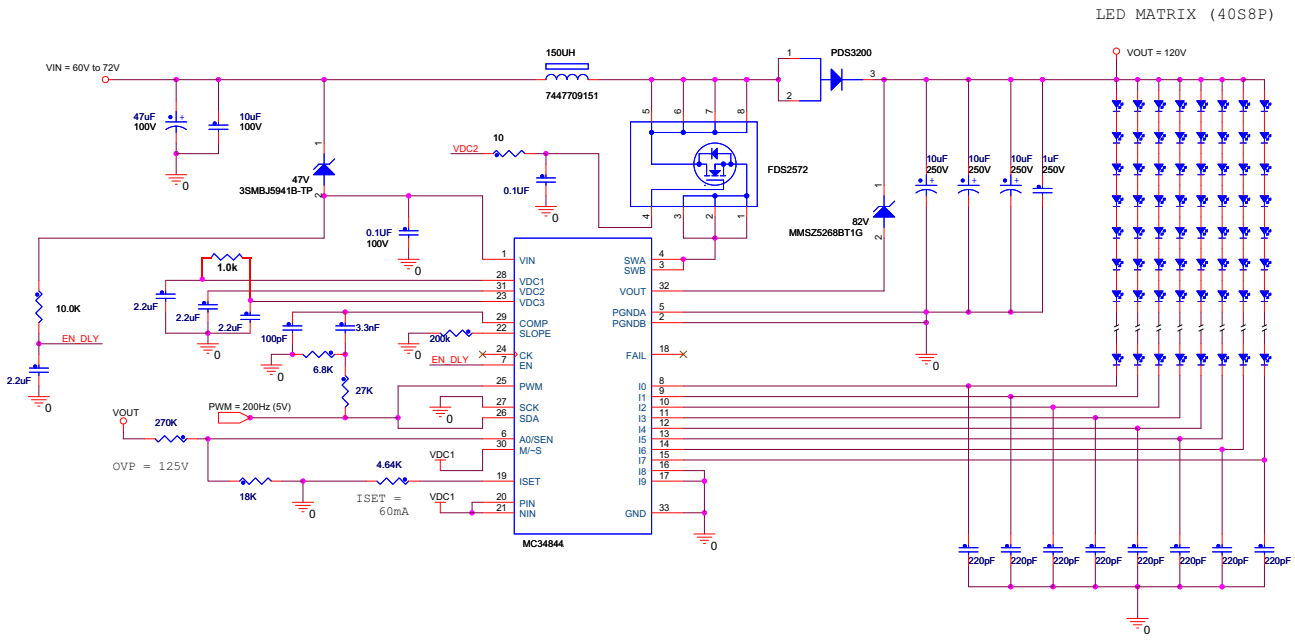


Figure 11. HIGH VOUT application (Manual Mode)
Conditions: V_{IN} = 60 to 72V, V_{OUT} = 120 V, Load = 40S8P, I_{LED} = 60 mA, OVP = 125 V, f_{SW} = 300 kHz

COMPONENTS CALCULATION

The following formulas are intended for the calculation of all external components related with the Boost converter and Network compensation. To calculate a Duty Cycle, the internal losses of the MOSFET and Diode should be taken into consideration.

$$D = \frac{Vout + V_D - Vin}{Vout + V_D - V_{SW}}$$

The average input current depends directly to the output current when the internal switch is off.

$$Iin_{avg} = \frac{Iout}{1 - D}$$

Inductor

For calculating the Inductor we should consider the losses of the internal switch and winding resistance of the inductor.

$$L = \frac{(Vin - V_{SW} - (Iin_{avg} \times rw)) \times D}{Iin_{avg} \times r \times F_{SW}}$$

It is important to look for an inductor rated at least for the maximum input current.

$$Iin_{max} = Iin_{avg} + \frac{Vin \times (Vout - Vin)}{2 \times L \times F_{SW} \times Vout}$$

Input Capacitor

The input capacitor should handle at least the following RMS current.

$$Irms_{Cin} = \left(\frac{Vin \times (Vout - Vin)}{2 \times L \times F_{SW} \times Vout}\right) \times 0.3$$

Output Capacitor

For the output capacitor selection the internal current sense gain (CSG) and the Transconductance should be taken in consideration. The CSG is the internal R_{SENSE} times the current sense amplifier gain (A_{CSA}).

$$CSG = A_{CSA} \times R_{Sense}$$

$$Cout = \frac{R_{Comp} \times 5 \times G_M \times Iout \times L}{(1 - D) \times Vout \times CSG}$$

The output voltage ripple (ΔV_{OUT}) depends on the ESR of the Output capacitor. For a low output voltage ripple, it is recommended to use Ceramic capacitors usually having very low ESR. Since ceramic capacitor are expensive, Electrolytic or Tantalum capacitors can be mixed with ceramic capacitors for an inexpensive solution.

$$ESR_{Cout} = \frac{Vout \times \Delta Vout \times F_{SW} \times L}{Vout \times (1 - D)}$$

The output capacitor should handle at least the following RMS current.

Network Compensation

Since this Boost converter is current controlled, Type II compensation is needed.

$$Irms_{Cout} = Iout \times \sqrt{\frac{D}{1 - D}}$$

To calculate the Network Compensation, first calculate all Boost Converter components.

For this type of compensation, push out the Right Half Plane Zero to higher frequencies where they can't significantly affect the overall loop.

$$f_{RHPZ} = \frac{Vout \times (1 - D)^2}{Iout \times 2 \times \pi \times L}$$

The Crossover frequency must be set much lower than the location of the Right half plane zero

$$f_{Cross} = \frac{f_{RHPZ}}{5}$$

Since the system has a fixed Slope, compensation set by R_{SLOPE}, R_{COMP} should be fixed for all configurations.

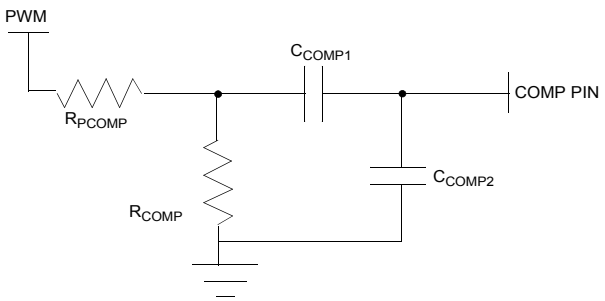
$$R_{Comp} = 5.6kohm$$

C_{COMP1} and C_{COMP2} should be calculated as follows:

$$C_{Comp1} = \frac{2}{f_{Cross} \times R_{Comp} \times \pi \times 2}$$

$$C_{Comp2} = \frac{G_M}{6.28 \times F_{SW}}$$

To improve the transient response of the boost, on the 34844, a resistor divider is implemented from the PWM pin to ground with a connection to the compensation network. This configuration should inject a 1.0 V signal to the COMP pin and the Thevenin-equivalent resistance of the divider is close to R_{COMP}, i.e. R_{COMP} = 6.8 k and R_{PCOMP}= 27 k for a 5.0 V PWM signal.



Slope Compensation

Slope Compensation can be expressed either in terms of Ampers/Second or as Volts/Second, through the use of the transfer resistance.

The following formula express the Slope Compensation in terms of V/μs:

$$V_{SLOPE} = \frac{(Vout - Vin) \times CSG}{L \times 2}$$

Where “L” is in μH

To have this slope compensation, the following resistor should be set.

$$R_{SLOPE} = \frac{33 \times 10^3}{V_{SLOPE} \times 5}$$

Variable Definition

D = Boost duty cycle

V_{OUT} = Output voltage

V_D = Diode forward voltage

V_{IN} = Input voltage

V_{SW} = V_{DROP} of internal switch

ΔV_{OUT} = Output voltage ripple ratio

IIN_{AVG} = Average input current

I_{OUT} = Output current

r = Input current ratio

IIN_{MAX} = Maximum input current

$IRMS_{CIN}$ = RMS current for input capacitor

$IRMS_{COUT}$ = RMS current for output capacitor

L = Inductor

R_W = Inductor winding DC resistance

f_{SW} = Boost switching frequency

CSG = Current sense gain = 0.2 V/A

A_{CSA} = Current sense amplifier gain = 9

R_{SENSE} = Current sense resistor = 22 mΩ

C_{OUT} = Output capacitor

R_{COMP} = Compensation resistor

G_M = OTA transconductance

ESR_{COUT} = ESR of output capacitor

f_{RHPZ} = Right half plane zero frequency

f_{CROSS} = Crossover frequency

C_{COMP1} = Compensation capacitor

C_{COMP2} = Shunt compensation capacitor

V_{SLOPE} = Slope compensation (V/μs)

R_{SLOPE} = External resistor for slope compensation

LAYOUT GUIDELINES

RECOMMENDED STACK-UP

Table 9 shows the recommended layer stack-up for the signals to have good shielding and Thermal Dissipation.

Table 9. Layer Stacking Recommendations

	Stack-Up
Layer 1 (Top)	Signal
Layer 2 (Inner 1)	Ground
Layer 3(Inner 2)	Signal
Layer 4 (Bottom)	Ground

DECOUPLING CAPS

It is recommended to place decoupling caps of 100 pf at the beginning and at the end of any power signal traces to filter high frequency noise. Decoupling caps of 100 pf should also be placed at the end of any long trace to cancel antenna effects. These caps should be located as closed as possible to the point to be decoupled and the connection to GND should be as short as possible.

SM-BUS/I^{2}C COMMUNICATION AND CLOCK SIGNALS (SDA, SCK AND CK)

To avoid contamination of these signals by nearby high power or high frequency signals, it is a good practice to shield them with ground planes placed on adjacent layers. Make sure the ground plane is uniform through the whole signal trace length.

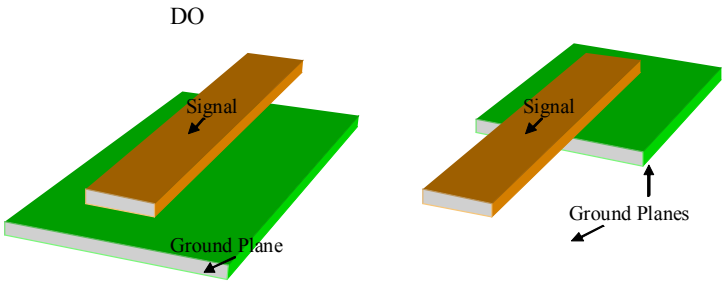


Figure 12. Recommended shielding for critical signals.

These signals should not run parallel to power signals or other clock signals in the same routing layer. If they have to cross or to be routed close to a power signal, it is a good practice to trace them perpendicularly or at 45° on a different layer to avoid coupling noise.

SWITCHING NODE (SWA & SWB)

The components associated to this node must be placed as close as possible to each other to keep the switching loop small enough so it does not contaminate other signals. However, care must be taken to ensure the copper traces used to connect these components together on this node, and are capable of handling the necessary current and voltage.

As a reference, a 10 mils trace with a thickness of 1.0 oz. of copper is capable of handling one ampere.

Traces for connecting the inductor, input and output caps should be as wide and short as possible to avoid adding inductance or resistance to the loop. The placement of these components should be selected far away from sensitive signals like compensation, feedback, and internal regulators to avoid power noise coupling.

COMPENSATION COMPONENTS

Components related with COMP pin need to be placed as close as possible to the pin.

FEEDBACK SIGNAL

The trace of the feedback signal (VOUT) should be routed perpendicularly or at 45° on a different layer to avoid coupling noise, preferably between ground or power planes.

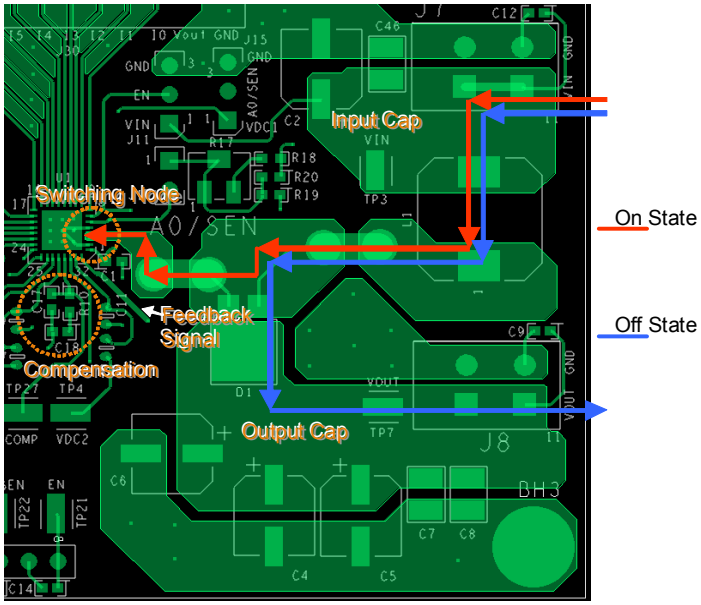


Figure 13. Feedback Signal Tracing

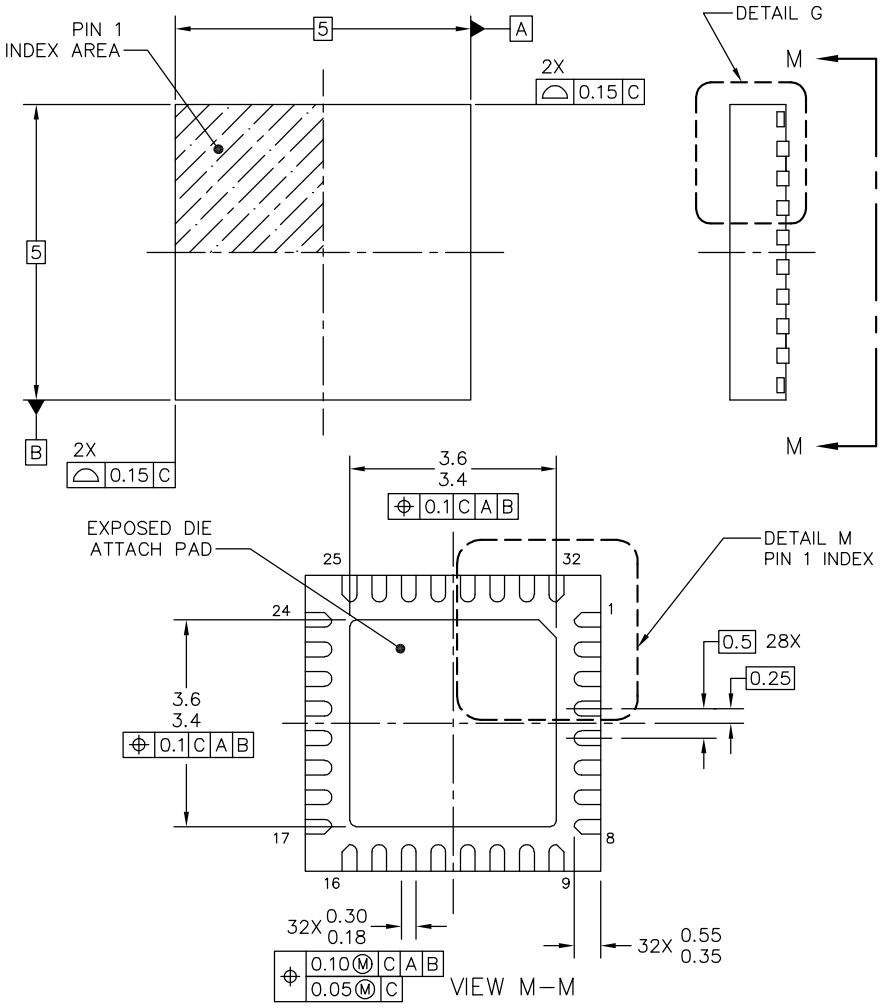
PACKAGING

PACKAGE MECHANICAL DIMENSIONS

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.freescale.com and perform a keyword search for the drawing's document number.

Table 10. Packaging Information

Package	Suffix	Package Outline Drawing Number
32-Pin LQFP-EP	EP	98ASA10800D



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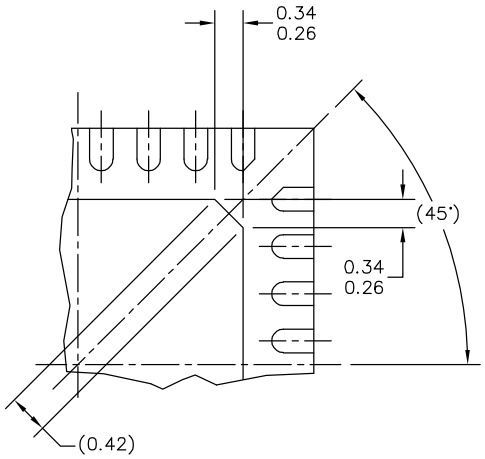
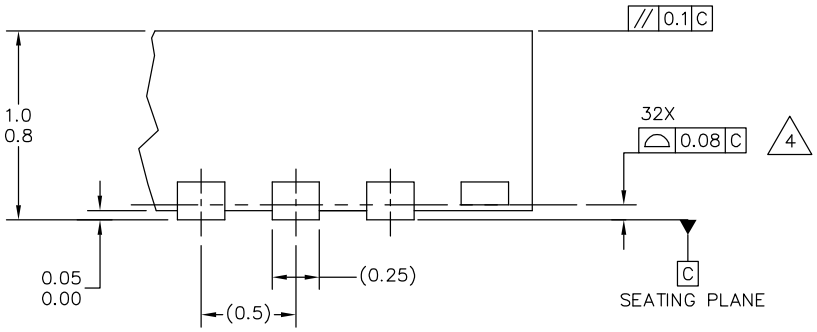
TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 32 TERMINAL, 0.50 PITCH (5 X 5 X 1) 3.5 X 3.5 EP, CASE OUTLINE	DOCUMENT NO: 98ASA10800D	REV: O
	CASE NUMBER: 1972–01	29 AUG 2007
	STANDARD: NON–JEDEC	



DETAIL M
PIN 1 BACKSIDE IDENTIFIER



DETAIL G
VIEW ROTATED 90°CW

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	CASE NUMBER: 1972-01	29 AUG 2007
	STANDARD: NON-JEDEC	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. RADIUS ON TERMINAL IS OPTIONAL.
4. COPLANARITY APPLIES TO LEADS, AND DIE ATTACH PAD.
5. MINIMUM METAL GAP SHOULD BE 0.2 MM.

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	CASE NUMBER: 1972–01	29 AUG 2007
	STANDARD: NON–JEDEC	

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
3.0	11/2008	• Initial Release
4.0	3/2009	• Added PWM Pin to Maximum Voltages in Maximum Rating Table. • Added Disabling LED Channels • Rewrote Fail Pin section • Added I2C Bus Specification
5.0	5/2009	• Corrected Compensation Components paragraph on page 32.
6.0	9/2009	• Added Part Number MC34844AEP/R2.
7.0	3/2010	• Combined Complete Data sheet for Part Numbers MC34844 and MC34844A to this data sheet.
8.0	7/2010	• Removed OVP=4h, OVP=3h and OVP=2h rows from Table 11. • PWM and CK Frequency range changed in Electrical Characteristics table.
9.0	3/2012	• Added resistor between VDC1 and VDC3 on the application drawings. Added to notes for VDC3 on pages 9, 14, 37, and 42.
10	8/2014	• Removed MC34844EP from the ordering information • Upgraded Freescale form and style to current standard • Updated back page

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