THE DATASHEET OF

MC33931VW

www.win-source.net 0086-755-83957316

MC33931

5.0 A throttle control H-bridge

Rev. 5.0 — 10 September 2018 Data sheet: technical data

1 General description

The 33931 is a monolithic H-bridge power IC in a robust thermally enhanced package. It is designed primarily for automotive electronic throttle control, but is applicable to any low voltage DC servo motor control application within the current and voltage limits stated in this specification. It meets the stringent requirements of automotive applications and is fully AEC-Q100 grade 1 qualified.

The 33931 H-bridge is able to control inductive loads with currents up to 5.0 A peak. RMS current capability is subject to the degree of heat sinking provided to the device package. Internal peak-current limiting (regulation) is activated at load currents above 6.5 A ± 1.5 A. Output loads can be pulse-width modulated at frequencies up to 11 kHz. A load current feedback feature provides a proportional (0.24 % of the load current) current output suitable for monitoring by a microcontroller's A/D input. A status flag output reports undervoltage, overcurrent and overtemperature fault conditions.

Two independent inputs provide polarity control of two half-bridge totem-pole outputs. The disable inputs are provided to force the H-bridge outputs to 3-state (high-impedance OFF state).

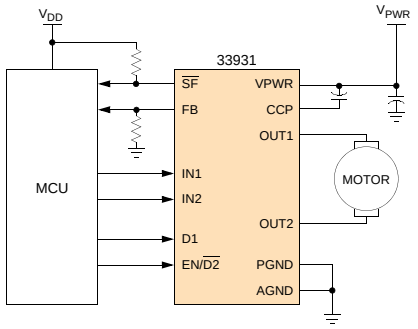


Figure 1. Simplified application diagram

2 Features and benefits

- 5.0 to 28 V continuous operation (transient operation from 5.0 to 40 V)
- 235 mΩ maximum $R_{DS(on)}$ @ T_J = 150 °C (each H-bridge MOSFET)
- 3.0 V and 5.0 V TTL / CMOS logic compatible inputs
- Overcurrent limiting (regulation) via internal constant-off-time PWM
- Output short-circuit protection (short to VPWR or GND)
- Temperature dependent current limit threshold reduction
- All inputs have an internal source/sink to define the default (floating input) state
- Sleep mode with current draw < 50 μA
- AEC-Q100 grade 1 qualified

3 Applications

- Electronic throttle control (ETC)
- Exhaust gas recirculation (EGR)
- Turbo flap control
- Industrial and medical pumps and motor control

4 Ordering information

Table 1. Ordering information

Type number [1]	Package			
	Name	Description	Operating temperature	Version
MC33931VW	HSOP44	HSOP44, plastic, thermal enhanced small outline package; 44 terminals; 0.65 mm pitch; 15.9 mm x 11 mm x 3 mm body	T_A = −40 °C to 125 °C	SOT1305-2
MC33931EK	HSOP32	HSOP32, plastic, heat sink, small outline; leaded package; 32 terminals; 0.65 mm pitch; 11 mm x 7.5 mm x 2.2 mm body		SOT1746-1

[1] To order parts in tape and reel, add the R2 suffix to the part number.

5 Block diagram

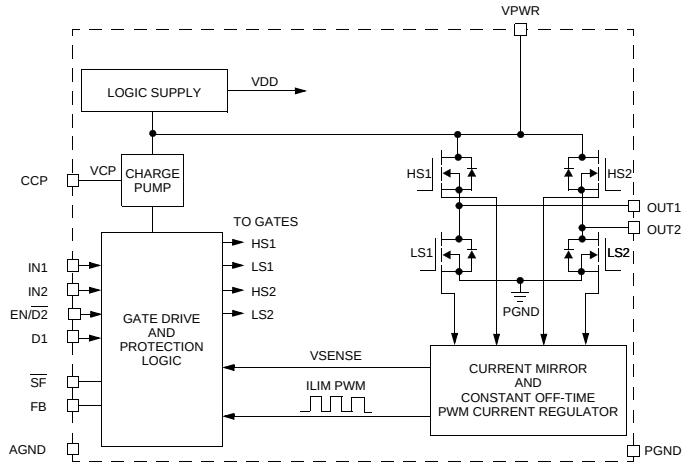


Figure 2. Block diagram

© NXP B.V. 2018. All rights reserved.

6 Pinning information

6.1 Pinning

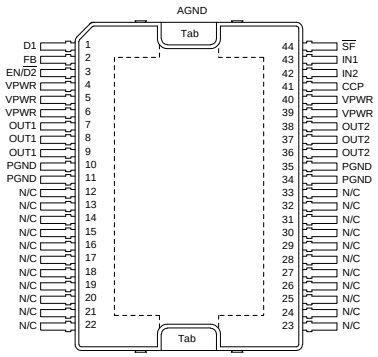


Figure 3. Pin configuration for HSOP44

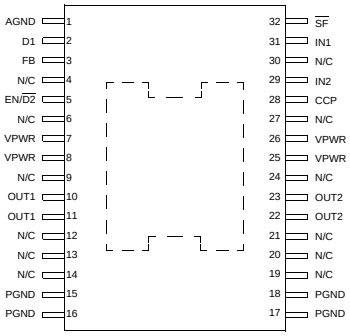


Figure 4. Pin configuration for HSOP32

6.2 Pin description

For functional description of each pin, see Section 7.2 "Functional pin description".

Table 2. Pin description

Symbol	Pin HSOP (VW)	Pin SOICW-EP (EK)	Function	Name	Description
D1	1	2	Logic input	Disable input 1 (active high)	When D1 is logic high, both OUT1 and OUT2 are 3-stated. Schmitt trigger input with ~80 µA source so default condition = disabled.
FB	2	3	Analog output	Feedback	The load current feedback output provides ground referenced 0.24 % of the high-side output current (tie to GND through a resistor if not used)
EN/$\overline{D2}$	3	5	Logic input	Enable input	When EN/$\overline{D2}$ is logic high, the H-bridge is operational. When EN/$\overline{D2}$ is logic low, the H-bridge outputs are 3-stated and placed in Sleep mode (logic input with ~ 80 µA sink so default condition = Sleep mode).
VPWR	4, 5, 6, 40, 39	7, 8, 25, 26	Power input	Positive power supply	These pins must be connected together physically as close as possible and directly soldered down to a wide, thick, low resistance supply plane on the PCB.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2018. All rights reserved.

Symbol	Pin HSOP (VW)	Pin SOICW-EP (EK)	Function	Name	Description
OUT1	7, 8, 9	10, 11	Power output	H-bridge output 1	Source of HS1 and drain of LS1
PGND	10, 11, 34, 35	15, 16, 17, 18	Power ground	Power ground	High-current power ground pins must be connected together physically as close as possible and directly soldered down to a wide, thick, low resistance ground plane on the PCB.
OUT2	36, 37, 38	22, 23	Power output	H-bridge output 2	Source of HS2 and drain of LS2
CCP	41	28	Analog output	Charge pump capacitor	External reservoir capacitor connection for the internal charge pump; connected to VPWR. Allowable values are 30 nF to 100 nF [1]
IN2	42	29	Logic input	Input 2	Logic input control of OUT2; e.g., when IN2 is logic high, OUT2 is set to VPWR, and when IN2 is logic low, OUT2 is set to PGND (Schmitt trigger input with ~ 80 µA source so default condition = OUT2 high)
IN1	43	31	Logic input	Input 1	Logic input control of OUT1; e.g., when IN1 is logic high, OUT1 is set to VPWR, and when IN1 is logic low, OUT1 is set to PGND (Schmitt trigger input with ~ 80 µA source so default condition = OUT1 high)
$\overline{SF}$	44	32	Logic output - open drain	Status flag (active low)	Open drain active low status flag output requires an external pull-up resistor to VDD. Maximum permissible load current < 0.5 mA. Maximum $V_{\overline{SF}LOW}$ < 0.4 V @ 0.3 mA. Maximum permissible pull-up voltage < 7.0 V.
AGND	TAB	1	Analog ground	Analog signal ground	The low-current analog signal ground must be connected to PGND via low-impedance path (<10 mΩ, 0 Hz to 20 kHz)
n.c.	12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33	4, 6, 9, 12, 13, 14, 19, 20, 21, 24, 27, 30	None	not connected	Pin is not used
EP	n.a.	EP	Thermal pad	Exposed pad	Exposed TAB is also the main heat sinking path for the device and must be connected to GND

[1] This capacitor is required for proper performance of the device.

7 Functional description

7.1 Introduction

Numerous protection and operational features (speed, torque, direction, dynamic breaking, PWM control and closed-loop control) make the 33931 a very attractive, cost-effective solution for controlling a broad range of small DC motors. The 33931 outputs are capable of supporting peak DC load currents of up to 5.0 A from a 28 V V_{PWR} source. An internal charge pump and gate drive circuitry are provided that can support external PWM frequencies up to 11 kHz.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2018. All rights reserved.

The 33931 has an analog feedback (current mirror) output pin (the FB pin) that provides a constant-current source ratioed to the active high-side MOSFETs' current. This can be used to provide real time monitoring of output current to facilitate closed-loop operation for motor speed/torque control, or for the detection of openload conditions.

Two independent inputs, IN1 and IN2, provide control of the two totem-pole half-bridge outputs. Two independent disable inputs, D1 and EN/$\overline{D2}$, provide the means to force the H-bridge outputs to a high-impedance state (all H-bridges switch off). The EN/$\overline{D2}$ pin also controls an enable function that allows the IC to be placed in a power conserving Sleep mode.

The 33931 has output current limiting (via constant OFF time PWM current regulation), output short-circuit detection with latch-off, and overtemperature detection with latch-off. Once the device is latched-off due to a fault condition, either of the disable inputs (D1 or EN/$\overline{D2}$), or V_{PWR} must be "toggled" to clear the status flag.

Current limiting (load current regulation) is accomplished by a constant OFF time PWM method using current limit threshold triggering. The current limiting scheme is unique in that it incorporates a junction temperature dependent current limit threshold. This means that the current limit threshold is reduced to around 4.2 A as the junction temperature increases above 160 °C. When the temperature is above 175 °C, overtemperature shutdown (latch-off) occurs. This combination of features allows the device to continue operating for short periods of time (< 30 seconds) with unexpected loads, while still retaining adequate protection for both the device and the load.

7.2 Functional pin description

7.2.1 Power ground and analog ground (PGND and AGND)

The power and analog ground pins should be connected together with a very low-impedance connection.

7.2.2 Positive power supply (VPWR)

VPWR pins are the power supply inputs to the device. All VPWR pins must be connected together on the printed circuit board with traces as short as possible, offering as low-impedance as possible between pins.

7.2.3 Status flag ($\overline{SF}$)

This pin is the device fault status output. This output is an active low open drain structure requiring a pull-up resistor to V_{DD}. The maximum V_{DD} is < 7.0 V. See Table 7 for the $\overline{SF}$ output status definition.

7.2.4 Input 1, 2 and Disable input 1 (IN1, IN2, and D1)

These pins are input control pins used to control the outputs. These pins are 3.0 V/ 5.0 V CMOS-compatible inputs with hysteresis. IN1 and IN2 independently control OUT1 and OUT2, respectively. D1 input is used to 3-state disable the H-bridge outputs.

When D1 is SET (D1 = logic high) in the disable state, outputs OUT1 and OUT2 are both 3-state disabled; however, the rest of the device circuitry is fully operational and the supply $I_{PWR(STANDBY)}$ current is reduced to a few mA. See Table 5.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2018. All rights reserved.

7.2.5 H-bridge output (OUT1, OUT2)

These pins are the outputs of the H-bridge with integrated freewheeling diodes. The bridge output is controlled using the IN1, IN2, D1, and EN/$\overline{D2}$ inputs. The outputs have PWM current limiting above the I_{LIM} threshold. The outputs also have thermal shutdown (3-state latch-off) with hysteresis as well as short-circuit latch-off protection.

A disable timer (time t_B) is incorporated to distinguish between load currents higher than the I_{LIM} threshold and short-circuit currents. This timer is activated at each output transition.

7.2.6 Charge pump capacitor (CCP)

This pin is the charge pump output pin and connection for the external charge pump reservoir capacitor. The allowable value is from 30 nF to 100 nF.

This capacitor must be connected from the CCP pin to the VPWR pin. The device cannot operate properly without the external reservoir capacitor.

7.2.7 Enable input/Disable input 2 (EN/$\overline{D2}$)

The EN/$\overline{D2}$ pin performs the same function as D1 pin, when it goes to a logic low, the outputs are immediately 3-stated. It is also used to place the device in a Sleep mode to consume low currents. When the EN/$\overline{D2}$ pin voltage is a logic Low state, the device is in the Sleep mode.

The device is enabled and fully operational when the EN pin voltage is logic high. An internal pull-down resistor maintains the device in Sleep mode in the event EN is driven through a high-impedance I/O or an unpowered microcontroller, or the EN/$\overline{D2}$ input is disconnected.

7.2.8 Feedback (FB)

The 33931 has a feedback output (FB) for real time monitoring of H-bridge high-side output currents to facilitate closed-loop operation for motor speed and torque control.

The FB pin provides current sensing feedback of the H-bridge high-side drivers. When running in the forward or reverse direction, a ground-referenced 0.24 % of load current is output to this pin. Through the use of an external resistor to ground, the proportional feedback current can be converted to a proportional voltage equivalent and the controlling microcontroller can read the current proportional voltage with its analog-to-digital converter (ADC). This is intended to provide the user with only first-order motor current feedback for motor torque control. The resistance range for the linear operation of the FB pin is $100\ \Omega < R_{FB} < 300\ \Omega$.

If PWM-ing is implemented using the disable pin input (only D1), a small filter capacitor (~1.0 μF) may be required in parallel with the R_{FB} resistor to ground for spike suppression.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2018. All rights reserved.

8 Maximum ratings

Table 3. Maximum ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device. These parameters are not production tested.

Symbol	Parameter		Value	Unit
Electrical ratings				
$V_{PWR(SS)}$ $V_{PWR(T)}$	Power supply voltage • Normal operation (steady-state) • Transient overvoltage	[1]	 −0.3 to 28 −0.3 to 40	V
V_{IN}	Logic input voltage	[2]	−0.3 to 7.0	V
$V_{\overline{SF}}$	$\overline{SF}$ output	[3]	−0.3 to 7.0	V
$I_{OUT(CONT)}$	Continuous output current	[4]	5.0	A
V_{ESD1} V_{ESD2}	ESD voltage • Human body model • Machine model • Charge device model – Corner pins – All other pins	[5]	 ± 2000 ± 200 ±750 ±500	V
T_{STG}	Storage temperature		−65 to 150	°C
T_A	Operational ambient temperature	[6]	−40 to 125	°C
T_J	Operation junction temperature	[6]	−40 to 150	°C
T_{PPRT}	Peak package reflow temperature during reflow	[7]	[8]	°C

[1] Device will survive repetitive transient overvoltage conditions for durations not to exceed 500 ms at duty cycle not to exceed 10 %. External protection is required to prevent device damage in case of a reverse battery condition.
[2] Exceeding the maximum input voltage on IN1, IN2, EN/$\overline{D2}$ or D1 may cause a malfunction or permanent damage to the device.
[3] Exceeding the pull-up resistor voltage on the open drain $\overline{SF}$ pin may cause permanent damage to the device.
[4] Continuous output current capability is dependent on sufficient package heat sinking to keep junction temperature ≤ 150 °C.
[5] ESD testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω), and the Charge Device Model (CDM), Robotic (C_{ZAP} = 4.0 pF).
[6] The limiting factor is junction temperature, taking into account the power dissipation, thermal resistance, and heat sinking provided. Brief non-repetitive excursions of junction temperature above 150 °C can be tolerated, provided the duration does not exceed 30 seconds maximum. Non-repetitive events are defined as not occurring more than once in 24 hours.
[7] Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
[8] NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), go to www.nxp.com, search by part number (remove prefixes/suffixes and enter the core ID) to view all orderable parts, and review parametrics.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2018. All rights reserved.

9 Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Approximate junction-to-case thermal resistance [1]	< 1.0	°C/W

[1] Exposed heat sink pad plus the power and ground pins comprise the main heat conduction paths. The actual $R_{\theta JB}$ (junction-to-PC board) values will vary depending on solder thickness and composition and copper trace thickness and area. Maximum current at maximum die temperature represents ~16 W of conduction loss heating in the diagonal pair of output MOSFETs. Therefore, the $R_{\theta JA}$ must be < 5.0 °C/W for maximum current at 70 °C ambient. Module thermal design must be planned accordingly.

10 Static characteristics

Table 5. Static characteristics

Characteristics noted under conditions 5.0 V ≤ V_{PWR} ≤ 28 V, −40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Unit
Power inputs (VPWR)					
	Operating voltage range [1] [2]				V
$V_{PWR(SS)}$	• Steady-state	5.0	—	28	
$V_{PWR(t)}$	• Transient (t < 500 ms)	—	—	40	
$I_{PWR(SLEEP)}$	Sleep state supply current [3] • EN/$\overline{D2}$ = Logic [0], IN1, IN2, D1 = Logic [1], and I_{OUT} = 0 A	—	—	50	µA
$I_{PWR(STANDBY)}$	Standby supply current (part enabled) • I_{OUT} = 0 A, V_{EN} = 5.0 V	—	—	20	mA
	Undervoltage lockout thresholds				
$V_{UVLO(ACTIVE)}$	• $V_{PWR(FALLING)}$	4.15	—	—	V
$V_{UVLO(INACTIVE)}$	• $V_{PWR(RISING)}$	—	—	5.0	V
$V_{UVLO(HYS)}$	• Hysteresis	150	200	350	mV
Charge pump					
$V_{CP} - V_{PWR}$	Charge pump voltage (CP capacitor = 33 nF), no PWM				V
	• V_{PWR} = 5.0 V	3.5	—	—	
	• V_{PWR} = 28 V	—	—	12	
$V_{CP} - V_{PWR}$	Charge pump voltage (CP capacitor = 33 nF), PWM = 11 kHz,				V
	• V_{PWR} = 5.0 V	3.5	—	—	
	• V_{PWR} = 28 V	—	—	12	
Control inputs					
V_I	Operating input voltage (IN1, IN2, D1, EN/$\overline{D2}$)	—	—	5.5	V
	Input voltage (IN1, IN2, D1, EN/$\overline{D2}$)				
V_{IH}	• Logic threshold high	2.0	—	—	V
V_{IL}	• Logic threshold low	—	—	1.0	V
V_{HYS}	• Hysteresis	250	400	—	mV
I_{IN}	Logic input currents, VPWR = 5.0 V				µA
	• Inputs EN/$\overline{D2}$ (internal pull-downs), V_{IH} = 5.0 V	20	80	200	
	• Inputs IN1, IN2, D1 (internal pull-ups), VIL = 0 V	−200	−80	−20	
Power outputs OUT1, OUT2					
$R_{DS(on)}$	Output-on resistance, I_{LOAD} = 3.0 A [4]				mΩ
	• V_{PWR} = 8.0 V, T_J = 25 °C	—	120	—	
	• V_{PWR} = 8.0 V, T_J = 150 °C	—	—	235	
	• V_{PWR} = 5.0 V, T_J = 150 °C	—	—	325	

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2018. All rights reserved.

Symbol	Parameter		Min	Typ	Max	Unit
I_{LIM}	Output current regulation threshold • $T_J < T_{FB}$ • $T_J \geq T_{FB}$ (foldback region - see Figure 10 and Figure 12)	[5]	 5.2 —	 6.5 4.2	 8.0 —	A
I_{SCH}	High-side short-circuit detection threshold (short-circuit to GND)	[5]	11	13	16	A
I_{SCL}	Low-side short-circuit detection threshold (short-circuit to V_{PWR})	[5]	9.0	11	14	A
$I_{OUTLEAK}$	Output leakage current, outputs off, V_{PWR} = 28 V • $V_{OUT} = V_{PWR}$ • V_{OUT} = Ground	[6]	 — −60	 — —	 100 —	μA
V_F	Output MOSFET body diode forward voltage drop • I_{OUT} = 3.0 A		 —	 —	 2.0	V
 T_{LIM} T_{HYS}	Overtemperature shutdown • Thermal limit at T_J • Hysteresis at T_J	[5]	 175 —	 — 12	 200 —	°C
T_{FB}	Current foldback at T_J	[5]	165	—	185	°C
T_{SEP}	Current foldback to thermal shutdown separation	[5]	10	—	15	°C
High-side current sense feedback						
I_{FB}	Feedback current (pin FB sourcing current) • IOUT = 0 mA • IOUT = 300 mA • IOUT = 500 mA • IOUT = 1.5 A • IOUT = 3.0 A • IOUT = 6.0 A	[7]	 0.0 0.0 0.35 2.86 5.71 11.43	 — 270 0.775 3.57 7.14 14.29	 50 750 1.56 4.28 8.57 17.15	 μA μA mA mA mA mA
Status flag [8]						
$I_{\overline{SF}LEAK}$	Status flag leakage current • $V_{\overline{SF}}$ = 5.0 V	[9]	 —	 —	 5.0	μA
$V_{\overline{SF}LOW}$	Status flag set voltage • $I_{\overline{SF}}$ = 300 μA	[10]	 —	 —	 0.4	V

[1] Device specifications are characterized over the range of 8.0 V ≤ V_{PWR} ≤ 28 V. Continuous operation above 28 V may degrade device reliability. Device is operational down to 5.0 V, but below 8.0 V the output resistance may increase by 50 percent.
[2] Device survives the transient overvoltage indicated for a maximum duration of 500 ms. Transient not to be repeated more than once every 10 seconds.
[3] $I_{PWR(SLEEP)}$ is with Sleep mode activated and EN/$\overline{D2}$, = logic [0], and IN1, IN2, D1 = logic [1] or with these inputs left floating.
[4] Output-on resistance as measured from output to VPWR and from output to GND.
[5] This parameter is guaranteed by design.
[6] Outputs switched OFF via D1 or EN/$\overline{D2}$.
[7] Accuracy is better than 20 % from 0.5 A to 6.0 A. Recommended terminating resistor value: R_{FB} = 270 Ω.
[8] Status flag output is an open drain output requiring a pull-up resistor to logic V_{DD}.
[9] Status flag leakage current is measured with status flag high and not set.
[10] Status flag set voltage measured with status flag low and set with $I_{\overline{FS}}$ = 300 μA. Maximum allowable sink current from this pin is <500 μA. Maximum allowable pull-up voltage < 7.0 V.

11 Dynamic characteristics

Table 6. Dynamic characteristics

Characteristics noted under conditions 5.0 V ≤ V_{PWR} ≤ 28 V, −40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Parameter		Min	Typ	Max	Unit
Timing characteristics						
f_{PWM}	PWM frequency	[1]	—	—	11	kHz
f_{MAX}	Maximum switching frequency during current limit regulation	[2]	—	—	20	kHz

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2018. All rights reserved.

Symbol	Parameter		Min	Typ	Max	Unit
t_{DON}	Output on delay • V_{PWR} = 14 V	[3]	— —	— —	18	µs
t_{DOFF}	Output off delay • V_{PWR} = 14 V	[3]	— —	— —	12	µs
t_A	I_{LIM} output constant-off time	[4] [5]	15	20.5	32	µs
t_B	I_{LIM} blanking time	[5] [6]	12	16.5	27	µs
$t_{DDISABLE}$	Disable delay time	[7]	—	—	8.0	µs
t_F, t_R	Output rise and fall time	[8]	1.5	3.0	8.0	µs
t_{FAULT}	Short-circuit/overtemperature turn-off (latch-off) time	[9] [10]	—	—	8.0	µs
t_{POD}	Power-on delay time	[10]	—	1.0	5.0	ms
t_{RR}	Output MOSFET body diode reverse recovery time	[10]	75	100	150	ns
f_{CP}	Charge pump operating frequency	[10]	—	7.0	—	MHz

[1] The maximum PWM frequency should be limited to frequencies < 11 kHz in order to allow the internal high-side driver circuitry time to fully enhance the high side MOSFETs.
[2] The internal current limit circuitry produces a constant-off-time pulse width modulation of the output current. The output load's inductance, capacitance, and resistance characteristics affect the total switching period (off-time + on-time), and thus the PWM frequency during current limit.
[3] Output delay is the time duration from 1.5 V on the IN1 or IN2 input signal to the 20 % or 80 % point (dependent on the transition direction) of the OUT1 or OUT2 signal. If the output is transitioning high-to-low, the delay is from 1.5 V on the input signal to the 80 % point of the output response signal. If the output is transitioning low-to-high, the delay is from 1.5 V on the input signal to the 20 % point of the output response signal. See Figure 5.
[4] The time during which the internal constant-off time PWM current regulation circuit has 3-stated the output bridge.
[5] Parameter is guaranteed by characterization
[6] The time during which the current regulation threshold is ignored so that the short-circuit detection threshold comparators may have time to act.
[7] Disable delay time measurement is defined in Figure 6.
[8] Rise time is from the 10 % to the 90 % level and fall time is from the 90 % to the 10 % level of the output signal with V_{PWR} = 14 V, R_{LOAD} = 3.0 Ω. See Figure 7.
[9] Load currents ramping up to the current regulation threshold become limited at the I_{LIM} value (see Figure 8). The short-circuit currents possess a di/dt that ramps up to the I_{SCH} or I_{SCL} threshold during the I_{LIM} blanking time, registering as a short-circuit event detection and causing the shutdown circuitry to force the output into an immediate 3-state latch-off (see Figure 9). Operation in current limit mode may cause junction temperatures to rise. Junction temperatures above ~160 °C causes the output current limit threshold to "foldback", or decrease, until ~175 °C is reached, after which the T_{LIM} thermal latch-off occurs. Permissible operation within this foldback region is limited to non-repetitive transient events of duration not to exceed 30 seconds (see Figure 10).
[10] Parameter is guaranteed by design.

12 Timing diagrams

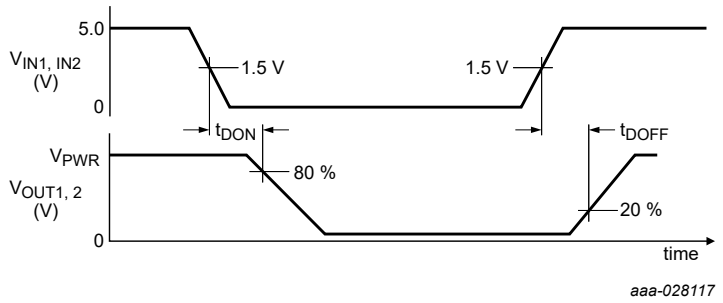


Figure 5. Output delay time

© NXP B.V. 2018. All rights reserved.

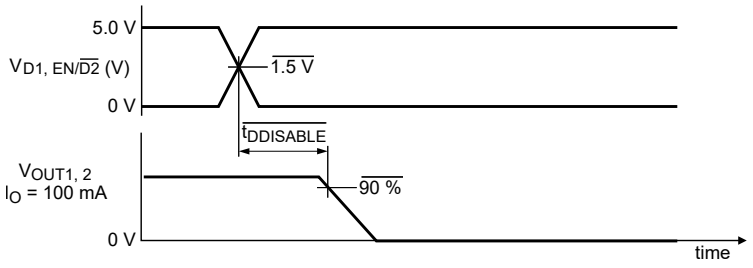


Figure 6. Disable delay time

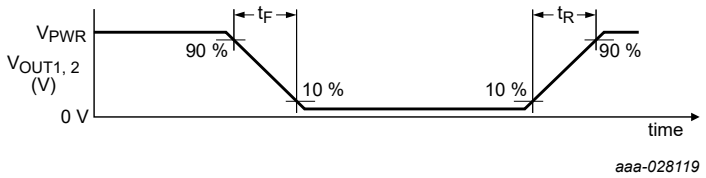


Figure 7. Output switching time

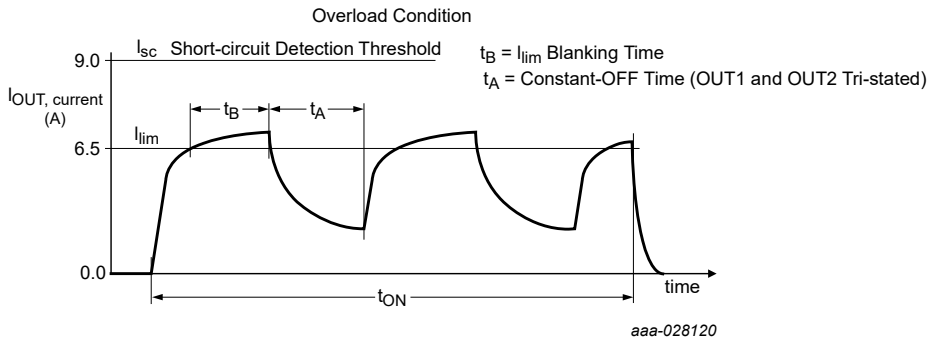


Figure 8. Current limit blanking time and constant-off time

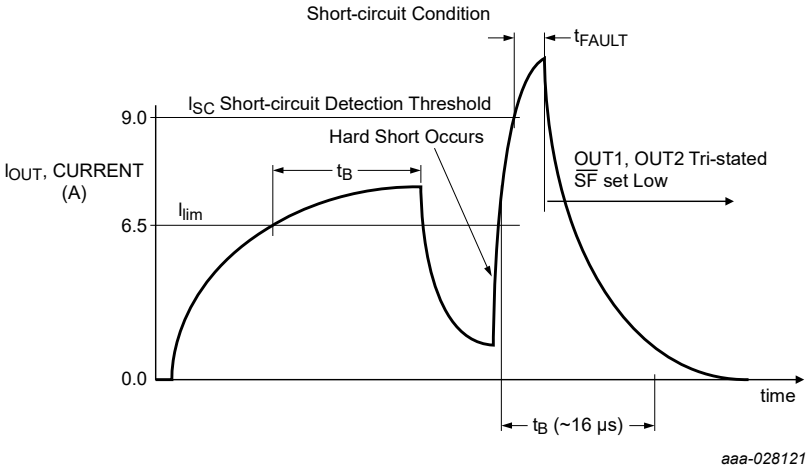


Figure 9. Short-circuit detection turn-off time t_{FAULT}

© NXP B.V. 2018. All rights reserved.

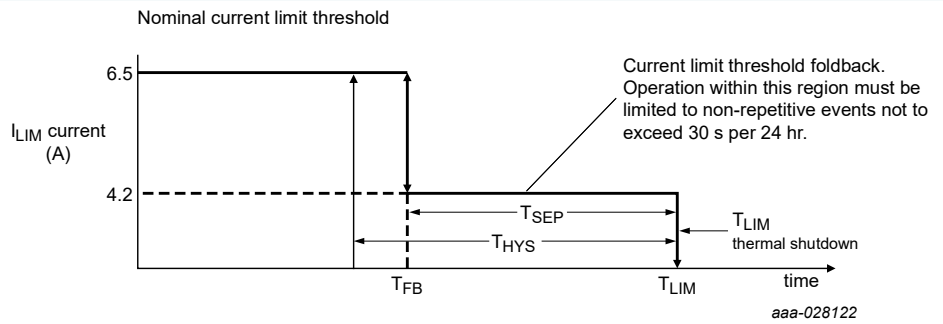


Figure 10. Output current limiting foldback region

13 Functional internal block description

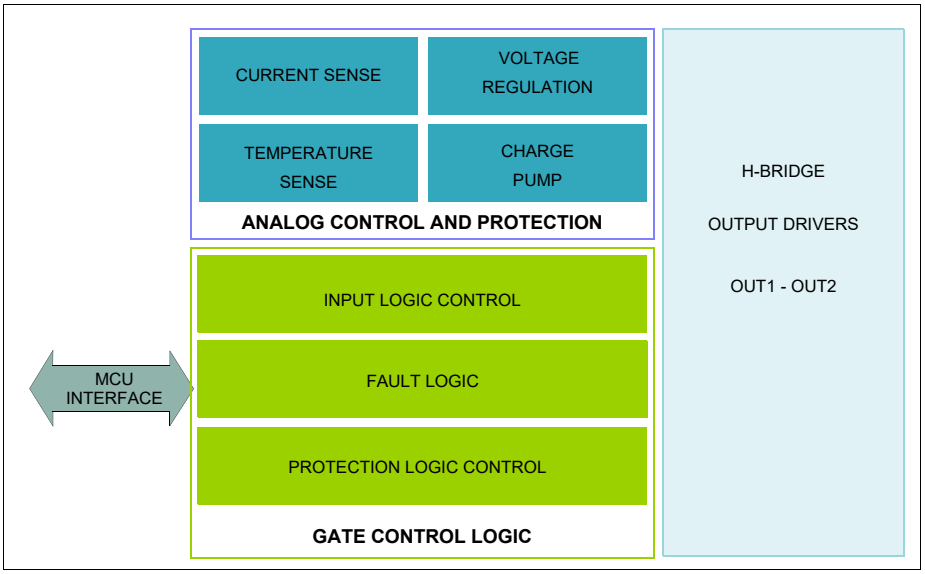


Figure 11. Functional internal block diagram

13.1 Analog control and protection circuitry

An on-chip voltage regulator supplies the internal logic. The charge pump provides gate drive for the H-bridge MOSFETs. The current and temperature sense circuitry provides detection and protection for the output drivers. Output undervoltage protection shuts down the MOSFETs.

13.2 Gate control logic

The 33931 is a monolithic H-bridge power IC designed primarily for any low-voltage DC servo motor control application within the current and voltage limits stated for the device. Two independent inputs provide polarity control of two half-bridge totem-pole outputs. Two independent disable inputs are provided to force the H-bridge outputs to 3-state (high-impedance OFF state).

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2018. All rights reserved.

13.3 H-bridge output drivers: OUT1 and OUT2

The H-bridge is the power output stage. The current flow from OUT1 to OUT2 is reversible and under full control of the user by way of the input control logic. The output stage is designed to produce full load control under all system conditions.

All protective and control features are integrated into the control and protection blocks. The sensors for current and temperature are integrated directly into the output MOSFET for maximum accuracy and dependability.

14 Functional device operation

14.1 Operational modes

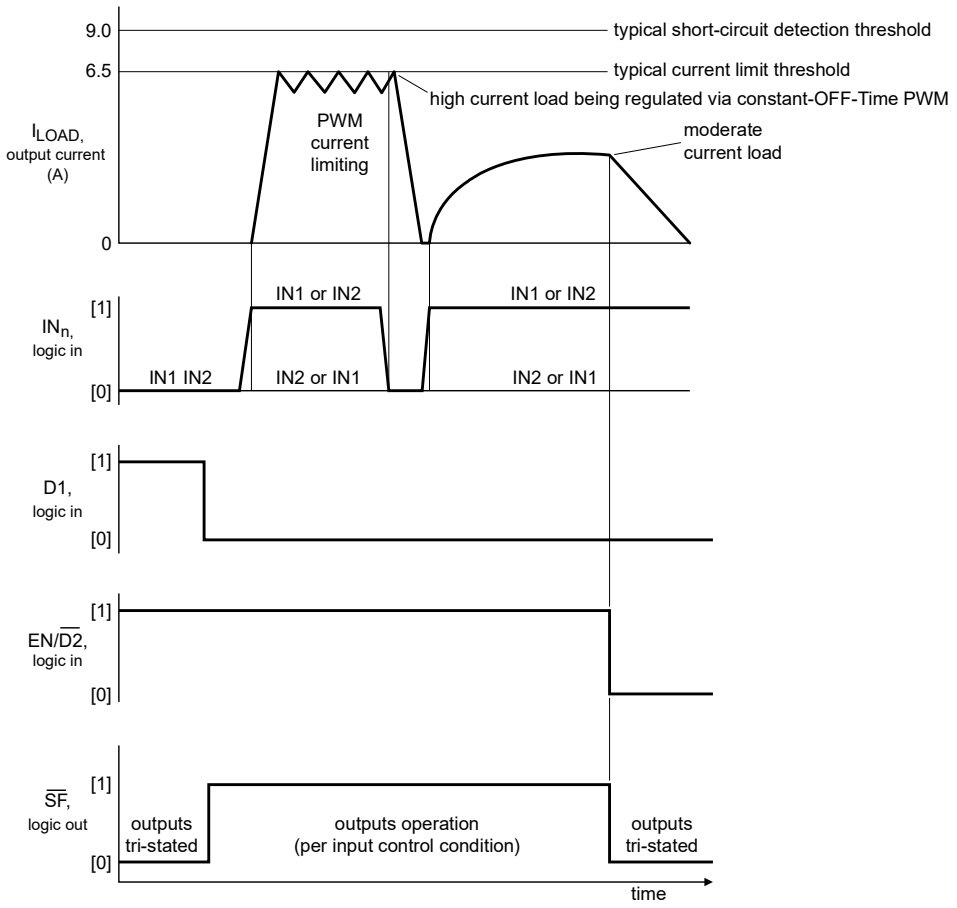


Figure 12. Operating states

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2018. All rights reserved.

14.2 Logic commands

Table 7. Truth table

The 3-state conditions and the status flag are reset using D1 or EN/$\overline{D2}$. The truth table uses the following notations: L = low, H = high, X = high or low, and Z = high-impedance.

Device state	Input conditions				Status	Outputs	
	EN/$\overline{D2}$	D1	IN1	IN2	$\overline{SF}$	OUT1	OUT2
Forward	H	L	H	L	H	H	L
Reverse	H	L	L	H	H	L	H
Freewheeling low	H	L	L	L	H	L	L
Freewheeling high	H	L	H	H	H	H	H
Disable 1 (D1)	H	H	X	X	L	Z	Z
IN1 disconnected	H	L	Z	X	H	H	X
IN2 disconnected	H	L	X	Z	H	X	H
D1 disconnected	H	Z	X	X	L	Z	Z
Undervoltage lockout [1]	H	X	X	X	L	Z	Z
Overtemperature [2]	H	X	X	X	L	Z	Z
Short-circuit [2]	H	X	X	X	L	Z	Z
Sleep mode EN/$\overline{D2}$	L	X	X	X	H	Z	Z
EN/$\overline{D2}$ disconnected	Z	X	X	X	H	Z	Z

[1] In the event of an undervoltage condition, the outputs 3-state and status flag are set to logic low. Upon undervoltage recovery, status flag is reset automatically or automatically cleared and the outputs are restored to their original operating condition.

[2] When a short-circuit or overtemperature condition is detected, the power outputs are 3-state latched-off, independent of the input signals, and the Status flag is latched to logic low. To reset from this condition requires the toggling of either D1, EN/$\overline{D2}$, or V_{PWR}.

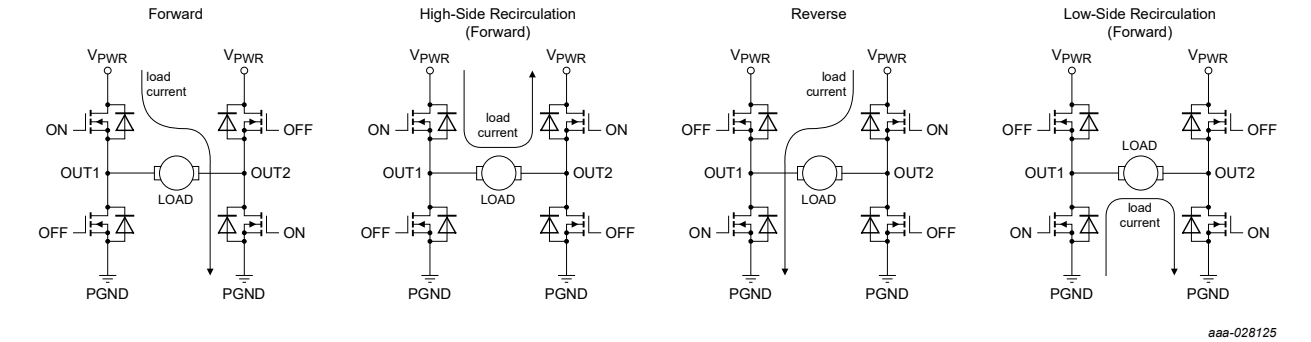


Figure 13. Power stage operation

14.3 Protection and diagnostic features

14.3.1 Short-circuit protection

If an output short-circuit condition is detected, the power outputs 3-state (latch-off) independent of the input (IN1 and IN2) states, and the fault status output flag ($\overline{SF}$) is set to logic low. If the D1 input changes from logic high to logic low, or if the EN/D2 input changes from logic low to logic high, the output bridge becomes operational again and the fault status flag resets (cleared) to a logic High state.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2018. All rights reserved.

The output stage always switches into the mode defined by the input pins (IN1, IN2, D1, and EN/$\overline{D2}$), provided the device junction temperature is within the specified operating temperature range.

14.3.2 Internal PWM current limiting

The maximum current flow under normal operating conditions should be less than 5.0 A. The instantaneous load currents will be limited to I_{LIM} via the internal PWM current limiting circuitry. When the I_{LIM} threshold current value is reached, the output stages are 3-stated for a fixed time (t_A) of 20 µs typical. Depending on the time constant associated with the load characteristics, the output current decreases during the 3-state duration until the next output ON cycle occurs.

The PWM current limit threshold value is dependent on the device junction temperature. When −40 °C < T_J < 160 °C, I_{LIM} is between the specified minimum/maximum values. When T_J exceeds 160 °C, the I_{LIM} threshold decreases to 4.2 A. Shortly above 175 °C, the device overtemperature circuit detects T_{LIM} and an overtemperature shutdown occurs. This feature implements a graceful degradation of operation before thermal shutdown occurs, thus allowing for intermittent unexpected mechanical loads on the motor's gear reduction train to be handled.

Important: *Die temperature excursions above 150 °C are permitted only for non-repetitive durations < 30 seconds. Provision must be made at the system level to prevent prolonged operation in the current-foldback region.*

14.3.3 Overtemperature shutdown and hysteresis

If an overtemperature condition occurs, the power outputs are 3-stated (latched-off), and the fault status flag ($\overline{SF}$) is set to a logic low.

To reset from this condition, D1 must change from a logic high to logic low, or EN/$\overline{D2}$ must change from a logic low to logic high. When reset, the output stage switches on again, provided the junction temperature is now below the overtemperature threshold limit minus the hysteresis.

Important: *Resetting from the fault condition clears the fault status flag. Powering down and powering up the device also resets the 33931 from the fault condition.*

14.3.4 Output avalanche protection

If VPWR becomes an open circuit, the outputs likely 3-state simultaneously due to the disable logic. This could result in an unclamped inductive discharge. The VPWR input to the 33931 should not exceed 40 V during this transient condition, to prevent electrical overstress of the output drivers. This can be accomplished with a zener clamp or MOV, and/or an appropriately valued input capacitor with sufficiently low ESR (see Figure 14).

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2018. All rights reserved.

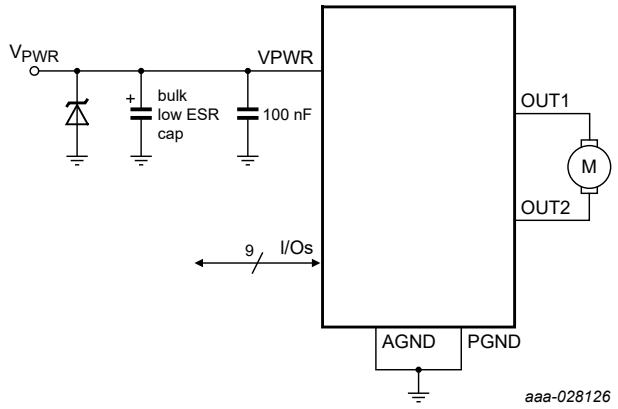


Figure 14. Avalanche protection

15 Application information

A typical application schematic is shown in Figure 15. For precision high current applications in harsh, noisy environments, the V_{PWR} bypass capacitor may need to be substantially larger.

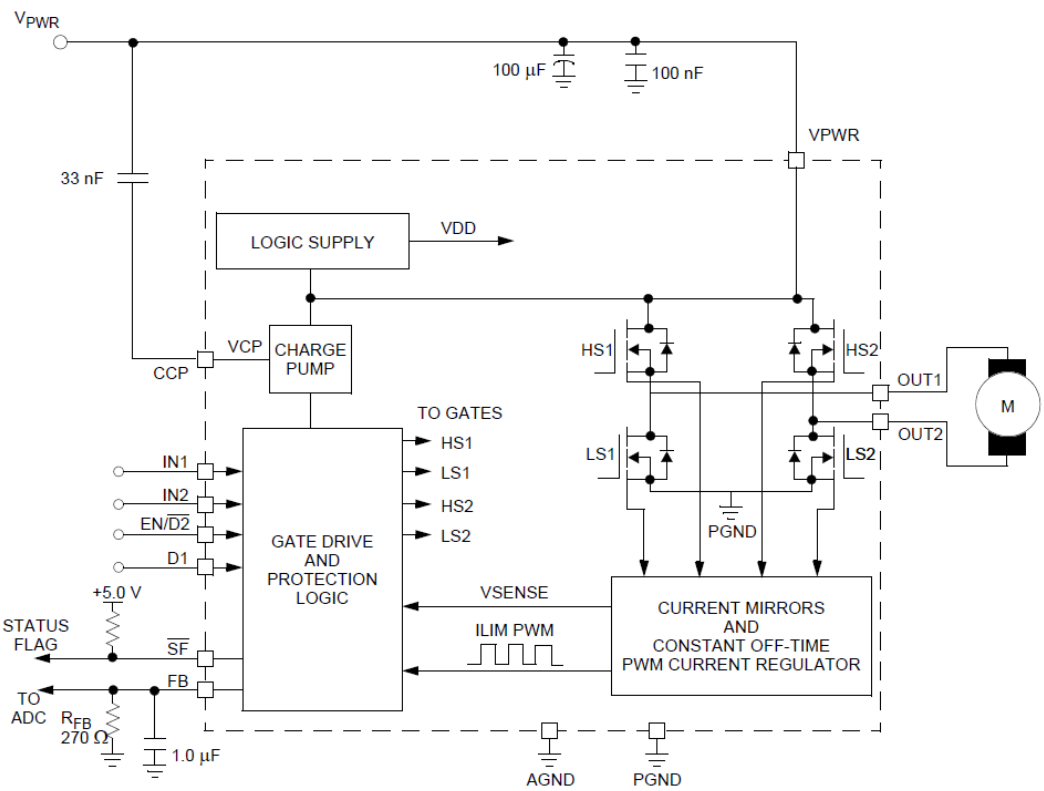


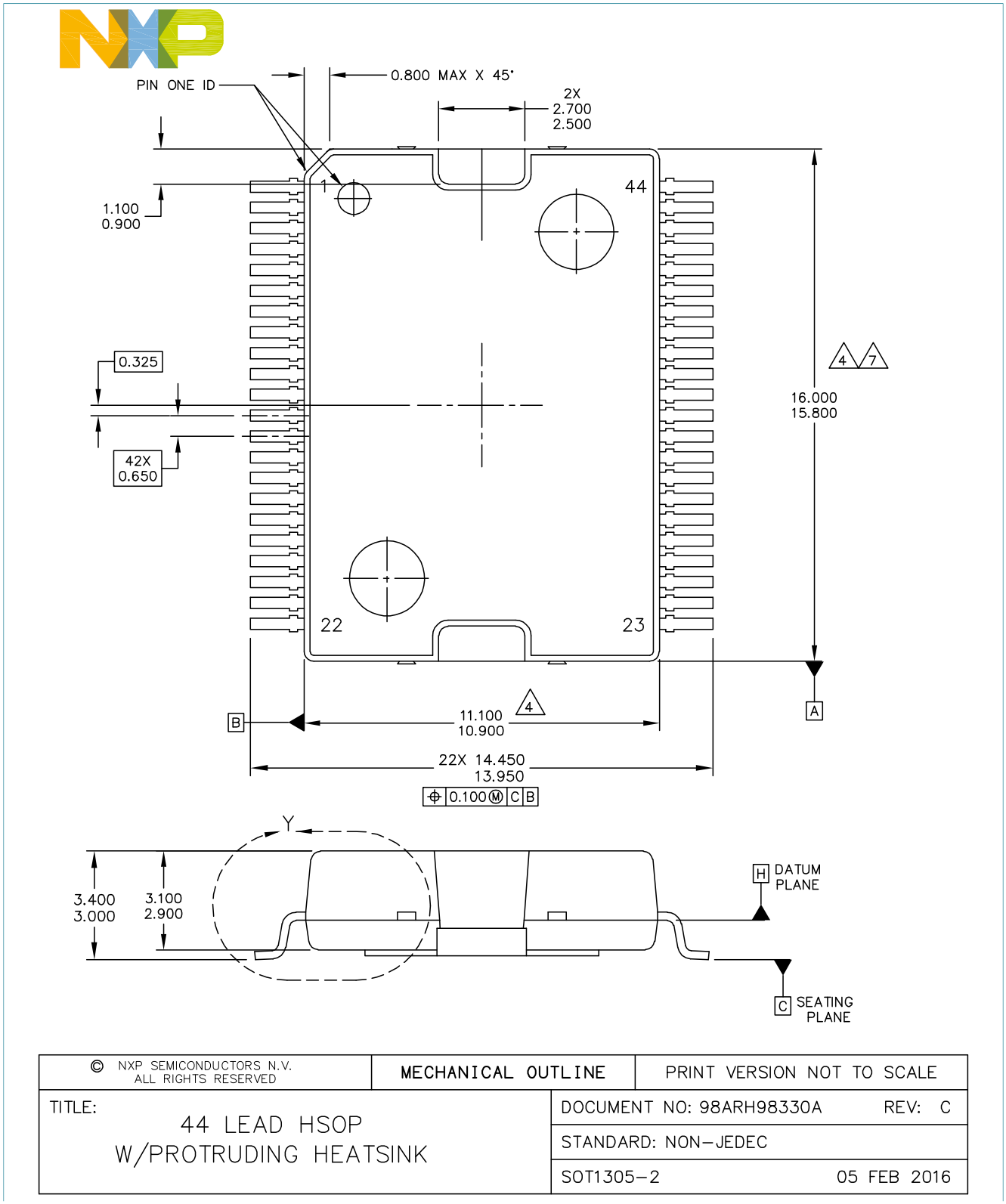
Figure 15. Typical application schematic

16 Package outline

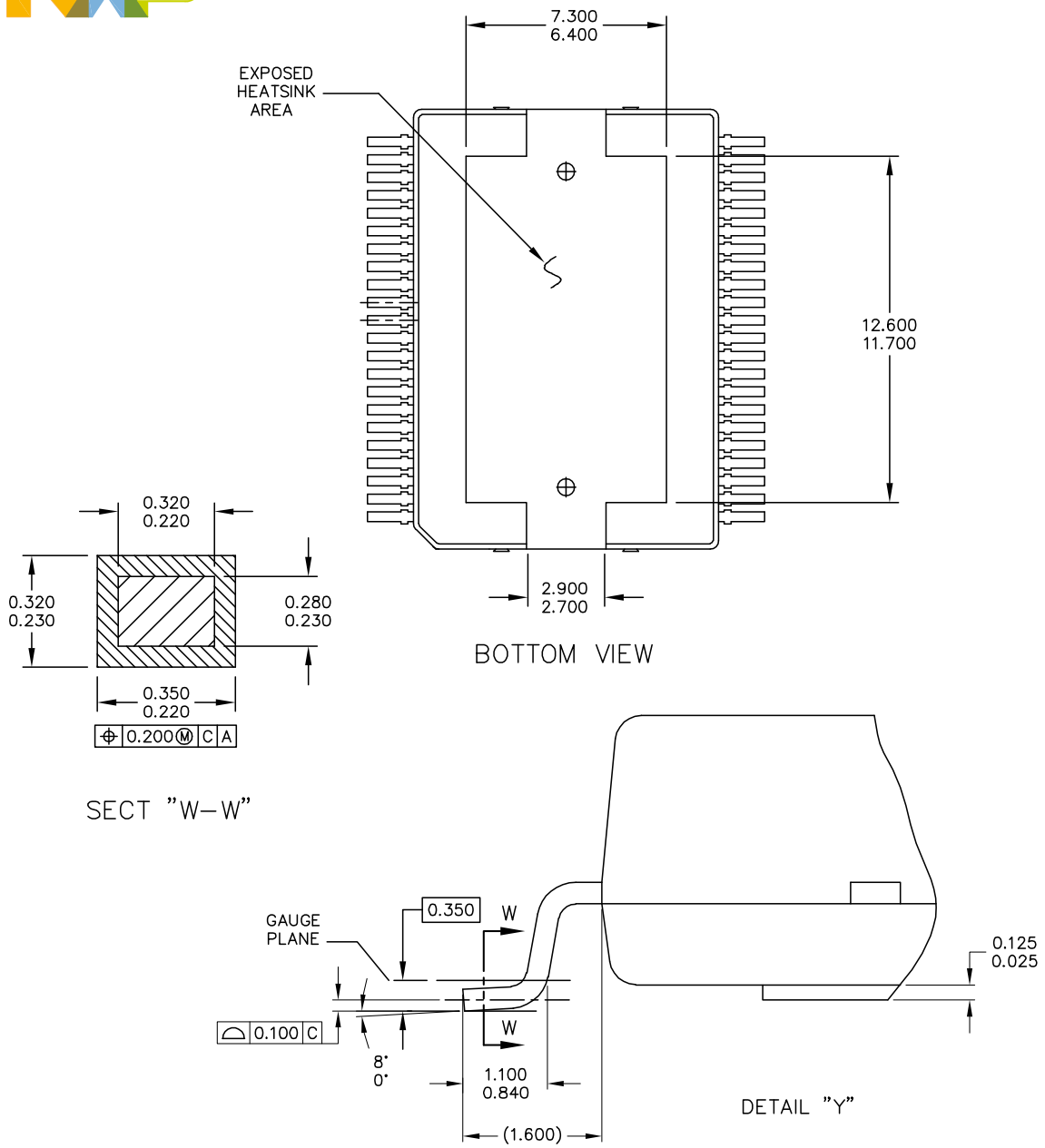
Note: *The most current package outline is available at* www.nxp.com.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2018. All rights reserved.



© NXP B.V. 2018. All rights reserved.



© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 44 LEAD HSOP W/PROTRUDING HEATSINK	DOCUMENT NO: 98ARH98330A	REV: C
	STANDARD: NON–JEDEC	
	SOT1305–2	05 FEB 2016

© NXP B.V. 2018. All rights reserved.

NOTES:

1. CONTROLLING DIMENSION: MILLIMETER

2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.

4. THIS DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.15 PER SIDE. THIS DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.

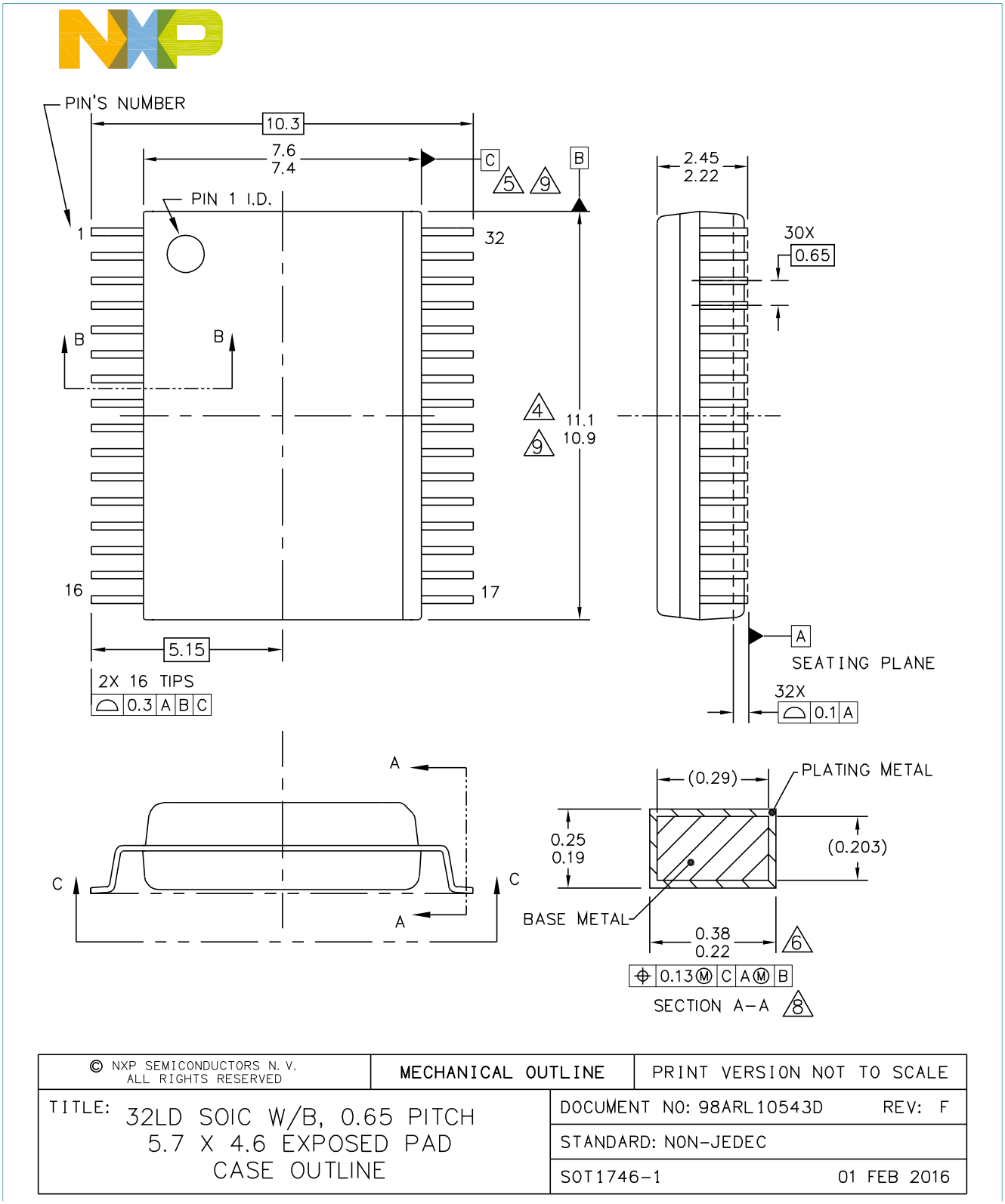
6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. THIS DIMENSIONS DOES NOT INCLUDE TIEBAR PROTRUSIONS. ALLOWABLE TIEBAR PROTRUSIONS ARE 0.15 PER SIDE.

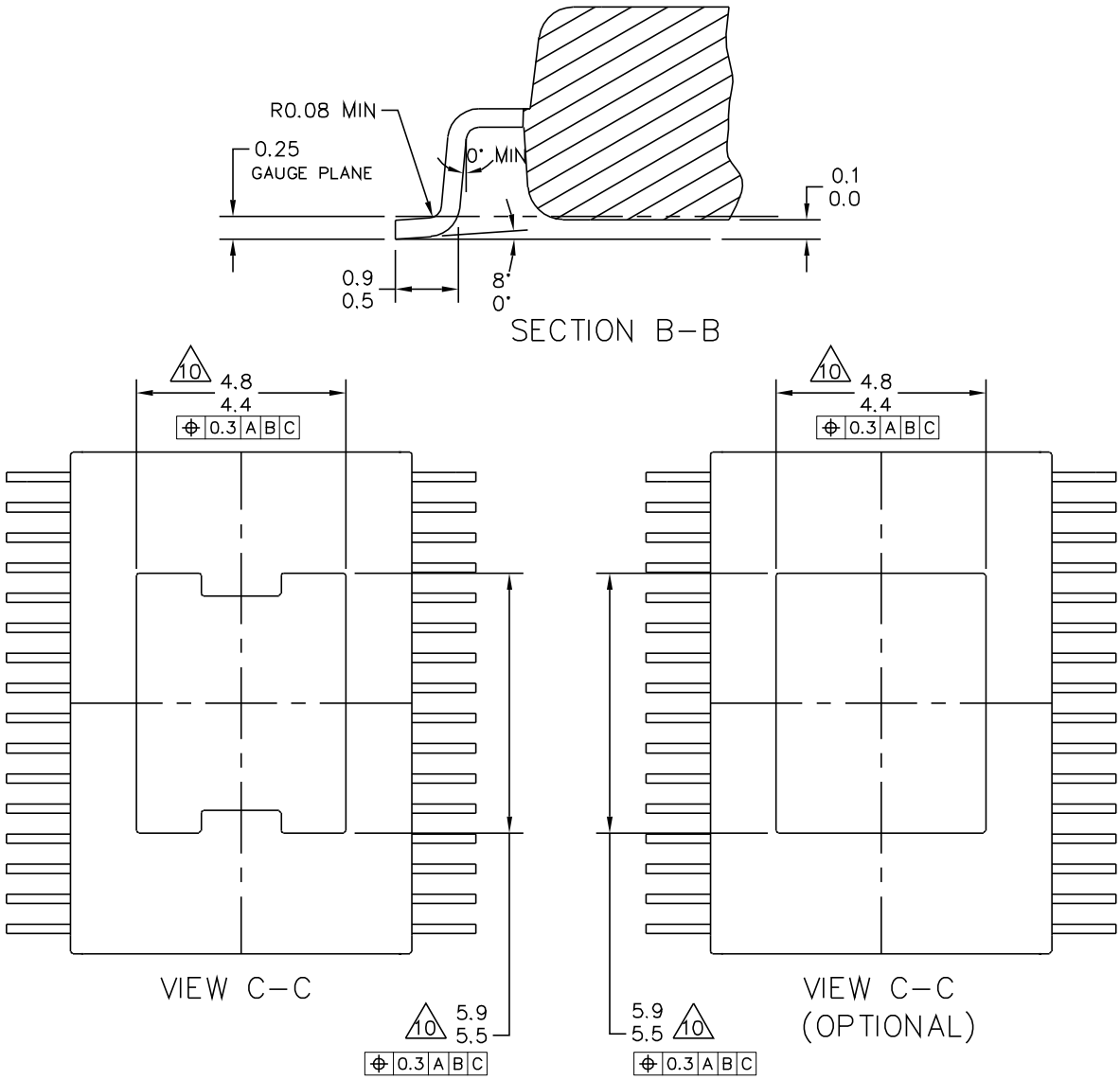
© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 44 LEAD HSOP W/PROTRUDING HEATSINK	DOCUMENT NO: 98ARH98330A	REV: C
	STANDARD: NON–JEDEC	
	SOT1305–2	05 FEB 2016

Figure 16. Package outline SOT1305-2 (HSOP44)

© NXP B.V. 2018. All rights reserved.



© NXP B.V. 2018. All rights reserved.



© NXP SEMICONDUCTORS N. V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 32LD SOIC W/B, 0.65 PITCH 5.7 X 4.6 EXPOSED PAD CASE OUTLINE	DOCUMENT NO: 98ARL10543D	REV: F
	STANDARD: NON-JEDEC	
	SOT1746-1	01 FEB 2016

© NXP B.V. 2018. All rights reserved.

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 mm.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.3 mm FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER–LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
10. THESE DIMENSIONS RANGES DEFINE THE PRIMARY KEEP–OUT AREA. MOLD LOCKING AND RESIN BLEED CONTROL FEATURES MAY BE VISIBLE AND THEY MAY EXTEND TO 0.9mm FROM MAXIMUM EXPOSED PAD SIZE

© NXP SEMICONDUCTORS N. V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 32LD SOIC W/B, 0.65 PITCH 5.7 X 4.6 EXPOSED PAD CASE OUTLINE	DOCUMENT NO: 98ARL10543D	REV: F
	STANDARD: NON-JEDEC	
	SOT1746-1	01 FEB 2016

Figure 17. Package outline SOT1746-1 (HSOP32)

© NXP B.V. 2018. All rights reserved.

17 Thermal addendum

17.1 Introduction

This thermal addendum is provided as a supplement to the MC33931 technical data sheet. The addendum provides thermal performance information that may be critical in the design and development of system applications. All electrical, application and packaging information is provided in the data sheet.

17.2 Packaging and thermal considerations

The 33931 is offered in a 32-pin SOICW-EP and a 44-pin HSOP single die package. There is a single heat source (P), a single junction temperature (T_J) and thermal resistance ($R_{\theta JA}$). This thermal addendum is specific to the 32-pin SOICW-EP package.

$\{T_J\} = [R_{\theta JA}] \cdot \{P\}$

The stated values are solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to, and will not predict the performance of a package in an application-specific environment.

Stated values were obtained by measurement and simulation according to the standards listed in Table 8.

Table 8. Thermal resistance data

Symbol	Parameter		Conditions	Value	Unit
$R_{\theta JA}$	Junction to Ambient Natural Convection	[1] [2]	Single Layer board (1s)	92	°C/W
$R_{\theta JA}$	Junction to Ambient Natural Convection	[1] [3]	Four layer board (2s2p)	26.6	°C/W
$R_{\theta JB}$	Junction to Board	[4]		7.0	°C/W
$R_{\theta JC}$(bottom)	Junction to Case (bottom / flag)	[5]		0.62	°C/W
$R_{\theta JC}$(top)	Junction to Case (top)	[6]		23.3	°C/W
Ψ_{JT}	Junction to Package Top	[7]	Natural Convection	2.7	°C/W

[1] Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
[2] Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
[3] Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
[4] Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
[5] Thermal resistance between the die and the case bottom / flag surface (simulated) (flag bottom side fixed to ambient temperature).
[6] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
[7] Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2018. All rights reserved.

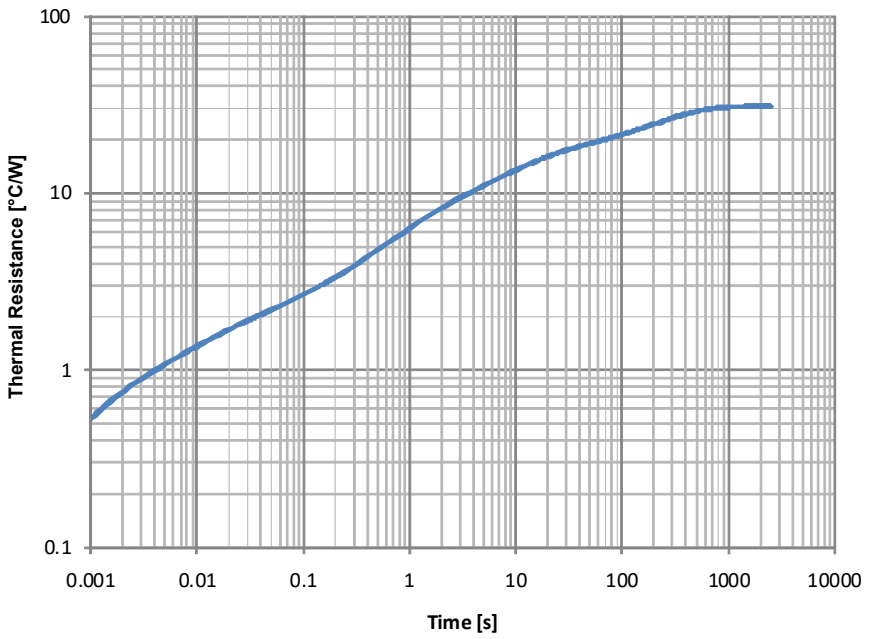


Figure 18. Transient thermal resistance $R_{\theta JA}$ MC33931EK on 2s2p test board

18 References

[1] **AN4146** — Thermal modeling and simulation of 12 V Gen3 eXtreme switch devices with SPICE
https://www.nxp.com/files-static/analog/doc/app_note/AN4146.pdf

[2] **BASICTHERMALWP** — Basic principles of thermal analysis for semiconductor systems
https://www.nxp.com/files-static/analog/doc/white_paper/BasicThermalWP.pdf

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2018. All rights reserved.

19 Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
MC33931 v.5.0	9/2018	Technical Data	-	DOC_ID v.4.0
Modifications	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. • Added AEC-Q100 grade 1 qualified to Section 1 and Section 2 • Updated package drawings to comply with the new identity guidelines of NXP Semiconductors (no technical change)			
MC33931 v.4.0	10/2012	Technical Data	-	DOC_ID v.3.0
Modifications	• PC33931EK changed to MC33931EK and released to production • Document level changed from Advance Information to Technical Data • Changed SOIC to SOICW-EP			
MC33931 v.3.0	6/2012	Advance information	-	DOC_ID v.2.0
Modifications	• Added PC33931EK to Table 1 • Added EK ordering and package information • Added thermal addendum and reference document sections • Minor corrections throughout the document			
MC33931 v.2.0	12/2008	Advance information	-	DOC_ID v.1.0
Modifications	• Updated Freescale form and style • Removed PC33931VW/R2 from the ordering information and added MC33931VW/R2 • Changed max $R_{DS(on)}$ from 225 to 235 mOhm in the document • Changed approximate Junction-to-Case Thermal Resistance and Peak Package Reflow Temperature in Table 4 • In Section 14.3.1, changed $\overline{D2}$ to EN/$\overline{D2}$			
MC33931 v.1.0	2/2008	Advance information	-	-

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2018. All rights reserved.

20 Legal information

20.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
[short] Data sheet: product preview	Development	This document contains certain information on a product under development. NXP reserves the right to change or discontinue this product without notice.
[short] Data sheet: advance information	Qualification	This document contains information on a new product. Specifications and information herein are subject to change without notice.
[short] Data sheet: technical data	Production	This document contains the product specification. NXP Semiconductors reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

20.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a technical data data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the technical data data sheet.

20.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

Suitability for use in automotive applications — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2018. All rights reserved.

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

20.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

SMARTMOS — is a trademark of NXP B.V.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2018. All rights reserved.

Tables

Tab. 1. Ordering information 2
Tab. 2. Pin description 3
Tab. 3. Maximum ratings 7
Tab. 4. Thermal characteristics 8
Tab. 5. Static characteristics 8
Tab. 6. Dynamic characteristics 9
Tab. 7. Truth table 14
Tab. 8. Thermal resistance data 23
Tab. 9. Revision history 25

Figures

Fig. 1. Simplified application diagram 1
Fig. 2. Block diagram 2
Fig. 3. Pin configuration for HSOP44 3
Fig. 4. Pin configuration for HSOP32 3
Fig. 5. Output delay time 10
Fig. 6. Disable delay time 11
Fig. 7. Output switching time 11
Fig. 8. Current limit blanking time and constant-off time 11
Fig. 9. Short-circuit detection turn-off time tFAULT 11
Fig. 10. Output current limiting foldback region 12
Fig. 11. Functional internal block diagram 12
Fig. 12. Operating states 13
Fig. 13. Power stage operation 14
Fig. 14. Avalanche protection 16
Fig. 15. Typical application schematic 16
Fig. 16. Package outline SOT1305-2 (HSOP44) 17
Fig. 17. Package outline SOT1746-1 (HSOP32) 20
Fig. 18. Transient thermal resistance RθJA MC33931EK on 2s2p test board 24

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2018. All rights reserved.

Contents

1 General description 1
2 Features and benefits 1
3 Applications 2
4 Ordering information 2
5 Block diagram 2
6 Pinning information 3
6.1 Pinning 3
6.2 Pin description 3
7 Functional description 4
7.1 Introduction 4
7.2 Functional pin description 5
7.2.1 Power ground and analog ground (PGND and AGND) 5
7.2.2 Positive power supply (VPWR) 5
7.2.3 Status flag (SF) 5
7.2.4 Input 1, 2 and Disable input 1 (IN1, IN2, and D1) 5
7.2.5 H-bridge output (OUT1, OUT2) 6
7.2.6 Charge pump capacitor (CCP) 6
7.2.7 Enable input/Disable input 2 (EN/D2) 6
7.2.8 Feedback (FB) 6
8 Maximum ratings 7
9 Thermal characteristics 8
10 Static characteristics 8
11 Dynamic characteristics 9
12 Timing diagrams 10
13 Functional internal block description 12
13.1 Analog control and protection circuitry 12
13.2 Gate control logic 12
13.3 H-bridge output drivers: OUT1 and OUT2 13
14 Functional device operation 13
14.1 Operational modes 13
14.2 Logic commands 14
14.3 Protection and diagnostic features 14
14.3.1 Short-circuit protection 14
14.3.2 Internal PWM current limiting 15
14.3.3 Overtemperature shutdown and hysteresis 15
14.3.4 Output avalanche protection 15
15 Application information 16
16 Package outline 16
17 Thermal addendum 23
17.1 Introduction 23
17.2 Packaging and thermal considerations 23
18 References 24
19 Revision history 25
20 Legal information 26

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2018. All rights reserved.

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 10 September 2018
Document identifier: MC33931

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View MC33931VW on WIN SOURCE
- Freescale Semiconductor - NXP Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management