THE DATASHEET OF

MC33926PNBR2

MC33926

5.0 A throttle control H-bridge

Rev. 16 — 19 February 2020 Data sheet: technical data

1 General description

The 33926 is a SMARTMOS monolithic H-bridge power IC designed primarily for automotive electronic throttle control, but is applicable to any low-voltage DC servo motor control application within the current and voltage limits stated in this specification. It meets the stringent requirements of automotive applications and is fully AEC-Q100 grade 1 qualified.

The 33926 is able to control inductive loads with currents up to 5.0 A peak. RMS current capability is subject to the degree of heatsinking provided to the device package. Internal peak-current limiting (regulation) is activated at load currents above 6.5 A ±1.5 A. Output loads can be pulse width modulated (PWM'ed) at frequencies up to 20 kHz. A load current feedback feature provides a proportional (0.24 % of the load current) current output suitable for monitoring by a microcontroller's A/D input. A status flag output reports undervoltage, overcurrent, and overtemperature fault conditions.

Two independent inputs provide polarity control of two half-bridge totem-pole outputs. Two independent disable inputs are provided to force the H-bridge outputs to tri-state (high-impedance off state). An inverted input changes the IN1 and IN2 inputs to low (true logic).

2 Simplified application diagram

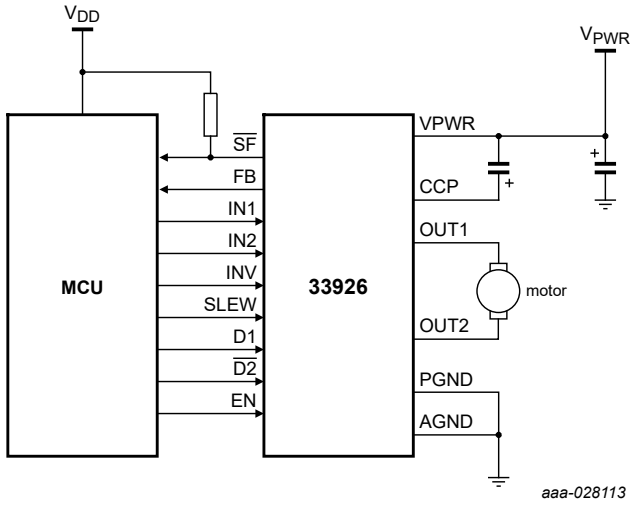


Figure 1. Simplified application diagram

3 Features and benefits

- 5.0 V to 28 V continuous operation (transient operation from 5.0 V to 40 V)

- 225 mΩ maximum $R_{DS(on)}$ at 150 °C (each H-bridge MOSFET)
- 3.0 V and 5.0 V TTL/CMOS logic compatible inputs
- Overcurrent limiting (regulation) via an internal constant-off-time PWM
- Output short-circuit protection (short to V_{PWR} or ground)
- Temperature dependent current limit threshold reduction
- All inputs have an internal source/sink to define the default (floating input) states
- Sleep mode with current draw < 50 µA (with inputs floating or set to match default logic states)
- AEC-Q100 grade 1 qualified

4 Applications

- Electronic throttle control (ETC)
- Exhaust gas recirculation (EGR)
- Turbo flap control
- Industrial and medical pumps and motor control

5 Ordering information

This section describes the part numbers available to be purchased along with their differences. Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to http://www.nxp.com and perform a part number search.

Table 1. Orderable parts

Part number [1]	Operating temperature	Package
MC33926PNB	T_A = −40 °C to 125 °C	32-pin PQFN
MC33926AES		28-pin HVQFN with inspectable fillets

[1] To order parts in tape and reel, add the R2 suffix to the part number.

6 Internal block diagram

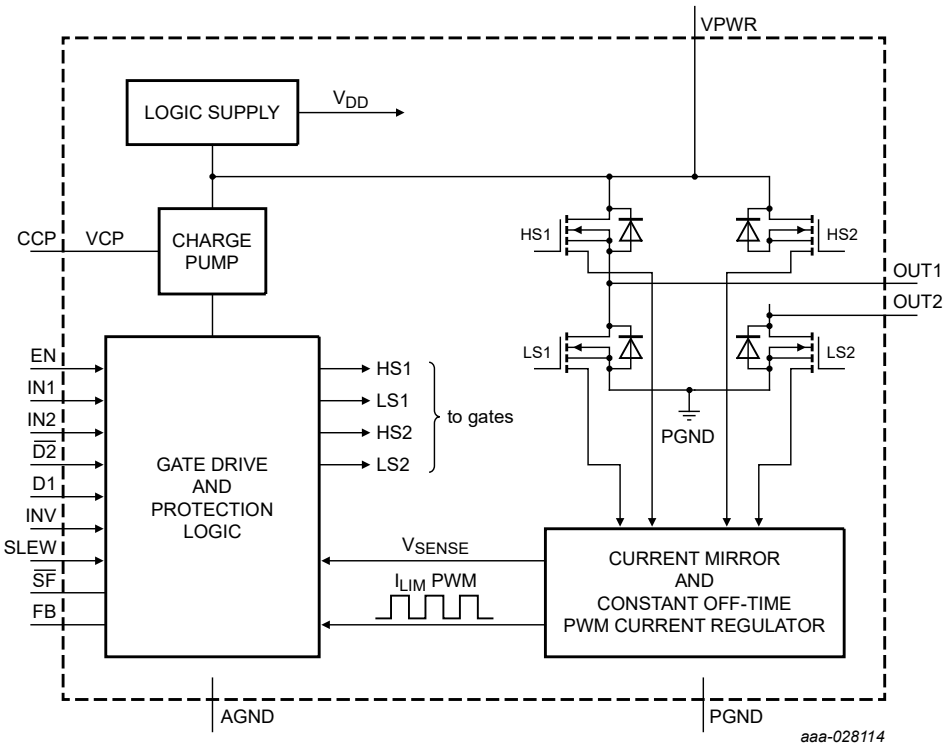
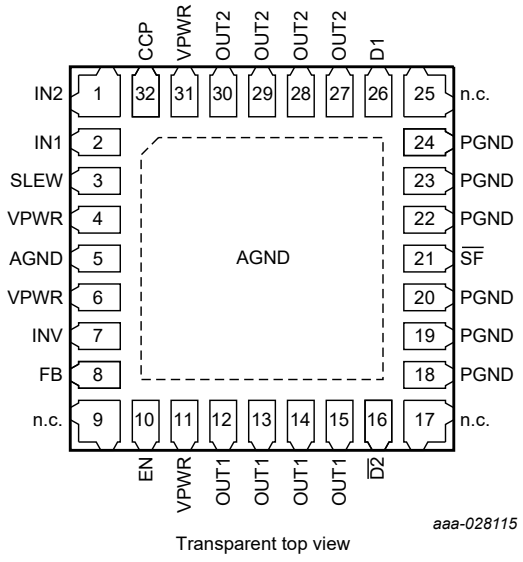


Figure 2. Internal block diagram

7 Pinning information

7.1 Pinning



Transparent top view

Figure 3. Pin configuration for 32-pin PQFN

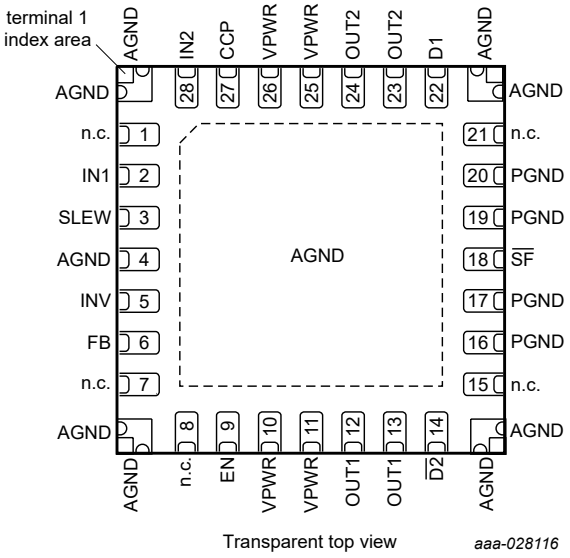


Figure 4. Pin configuration for 28-pin HVQFN

7.2 Pin description

For functional description of each pin see Section 9.2 "Functional pin description".

Table 2. Pin description

32-pin PQFN	28-pin QFN	Pin name	Pin function	Formal name	Definition
1	28	IN2	Logic input	Input 2	Logic input control of OUT2; example, when IN2 is logic high, OUT2 is set to V_{PWR}, and when IN2 is logic low, OUT2 is set to PGND (Schmitt trigger input with ~ 80 µA source so default condition = OUT2 high)
2	2	IN1	Logic input	Input 1	Logic input control of OUT1; example, when IN1 is logic high, OUT1 is set to V_{PWR}, and when IN1 is logic low, OUT1 is set to PGND (Schmitt trigger input with ~ 80 µA source so default condition = OUT1 high)
3	3	SLEW	Logic input	Slew rate	Logic input to select fast or slow slew rate (Schmitt trigger input with ~ 80 µA sink so default condition = slow)
4, 6, 11, 31	10, 11, 25, 26	VPWR	Power input	Positive power supply	These pins must be connected together physically as close as possible and directly soldered down to a wide, thick, low resistance supply plane on the PCB.
5, Exposed Pad	4, Exposed pad	AGND	Analog ground	Analog signal ground	The low current analog signal ground must be connected to PGND via low-impedance path (<<10 mΩ, 0 Hz to 20 kHz). Exposed copper pad is also the main heatsinking path for the device.
7	5	INV	Logic input	Input invert	Sets IN1 and IN2 to logic low = true (Schmitt trigger input with ~ 80 µA sink so default condition = non-inverted)
8	6	FB	Analog output	Feedback	Load current feedback output provides ground referenced 0.24 % of H-bridge high-side output current (tie pin to GND through a resistor if not used)
9, 17, 25	1, 7, 8, 15, 21	NC	—	No connect	No internal connection is made to this pin
10	9	EN	Logic input	Enable input	When EN is logic high, the device is operational. When EN is logic low, the device is placed in sleep mode (logic input with ~ 80 µA sink so default condition = sleep mode)

32-pin PQFN	28-pin QFN	Pin name	Pin function	Formal name	Definition
12, 13,14, 15	12, 13	OUT1	Power output	H-bridge output 1	Source of high-side MOSFET1 and drain of low-side MOSFET1
16	14	$\overline{D2}$	Logic input	Disable input 2 (active low)	When $\overline{D2}$ is logic low, both OUT1 and OUT2 are tri-stated (Schmitt trigger input with ~ 80 µA sink so default condition = disabled)
18 , 19, 20, 22 , 23, 24	16, 17, 19, 20	PGND	Power ground	Power ground	High-current power ground pins must be connected together physically as close as possible and directly soldered down to a wide, thick, low resistance ground plane on the PCB.
21	18	$\overline{SF}$	Logic output open drain	Status flag (active low)	Open drain active low status flag output (requires an external pull-up resistor to V_{DD}). Maximum permissible load current < 0.5 mA. Maximum V_{CESAT} < 0.4 V at 0.3 mA. Maximum permissible pull-up voltage < 7.0 V
26	22	D1	Logic input	Disable input 1 (active high)	When D1 is logic high, both OUT1 and OUT2 are tri-stated. Schmitt trigger input with ~ 80 µA source so default condition = disabled.
27, 28,29, 30	23, 24	OUT2	Power output	H-bridge output 2	Source of high-side MOSFET2 and drain of low-side MOSFET2
32	27	CCP	Analog output	Charge pump capacitor	External reservoir capacitor connection for internal charge pump; connected to VPWR. Allowable values are 30 nF to 100 nF. Note: This capacitor is required for the proper performance of the device.

8 General product characteristics

8.1 Maximum ratings

Table 3. Maximum ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device. These parameters are not production tested.

Symbol	Ratings	Value	Unit
Electrical ratings			
$V_{PWR(SS)}$ $V_{PWR(T)}$	Power supply voltage [1] • Normal operation (steady-state) • Transient overvoltage	 −0.3 to 28 −0.3 to 40	V
V_{IN}	Logic input voltage [2]	−0.3 to 7.0	V
V_{SFB}	$\overline{SF}$ output [3]	−0.3 to 7.0	V
$I_{OUT(CONT)}$	Continuous output current [4]	5.0	A
V_{ESD1} V_{ESD2}	ESD voltage [5] • Human body model • Machine model • Charge device model – Corner pins (1,9,17,25) - 32-pin PQFN – All other pins - 32-pin PQFN – All pins - 28-pin QFN	 ± 2000 ± 200 ±750 ±500 ±500	V

[1] Device will survive repetitive transient overvoltage conditions for durations not to exceed 500 ms at duty cycle not to exceed 10 %. External protection is required to prevent device damage in case of a reverse battery condition.
[2] Exceeding the maximum input voltage on IN1, IN2, EN, INV, SLEW, D1, or $\overline{D2}$ may cause a malfunction or permanent damage to the device.
[3] Exceeding the pull-up resistor voltage on the open drain SFB pin may cause permanent damage to the device.
[4] Continuous output current capability is dependent on sufficient package heatsinking to keep junction temperature ≤ 150 °C.
[5] ESD1 testing is performed in accordance with the human body model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), ESD2 testing is performed in accordance with the machine model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω), and the charge device model (CDM), robotic (C_{ZAP} = 4.0 pF).

8.2 Thermal characteristics

Table 4. Thermal ratings

Symbol	Ratings		Min.	Max.	Unit
Thermal ratings					
T_J	Operation junction temperature	[1]	−40	150	°C
T_A	Operational ambient temperature	[2]	−40	125	°C
T_{STG}	Storage temperature		−65	150	°C
T_{PPRT}	Peak package reflow temperature during reflow	[3] [4]	—	260	°C
MC33926PNB thermal resistance and package dissipation ratings					
$R_{\theta JA}$	Junction-to-ambient, single-layer board (1s)	[5] [6]	—	80.0	°C/W
$R_{\theta JA}$	Junction-to-ambient, four-layer board (2s2p)	[5] [7]	—	28.0	°C/W
$R_{\theta JB}$	Junction-to-board	[7] [8]	—	12.0	°C/W
$R_{\theta JC}$	Junction-to-case (bottom)	[9]	—	1.0	°C/W
MC33926AES thermal resistance and package dissipation ratings					
$R_{\theta JA}$	Junction-to-ambient, single-layer board (1s)	[5] [6]	—	89.5	°C/W
$R_{\theta JA}$	Junction-to-ambient, four-layer board (2s2p)	[5] [7]	—	31.9	°C/W
$R_{\theta JB}$	Junction-to-board	[7] [8]	—	11.9	°C/W
$R_{\theta JC}$	Junction-to-case (bottom)	[9]	—	0.53	°C/W
Ψ_{JT}	Junction-to-package top, natural convection	[10]	—	2.1	°C/W

[1] Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance. Junction temperature is a limiting factor, and module thermal design must be planned accordingly. Brief non-repetitive excursions of junction temperature above 150 °C can be tolerated, provided the duration does not exceed 30 seconds maximum. Non-repetitive events are defined as not occurring more than once in 24 hours.
[2] The circuit specification describes IC operation within the parametric operating range defined in the electrical characteristic table.
[3] Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
[4] NXP's package reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C for peak package reflow temperature and moisture sensitivity levels (MSL).
[5] Test procedure per JEDEC JESD51-2 at natural convection for horizontally-oriented board, still air condition.
[6] 1s thermal test board per JEDEC JESD51-3 and JESD51-5.
[7] 2s2p thermal test board per JEDEC JESD51-5 and JESD51-7.
[8] Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package. The actual RθJB (junction-to-board) values will vary depending on solder thickness and composition and copper trace thickness and area.
[9] Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
[10] Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

8.3 Static electrical characteristics

Table 5. Static electrical characteristics

Characteristics noted under conditions 5.0 V ≤ V_{PWR} ≤ 28 V, −40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic		Min.	Typ.	Max.	Unit
Power inputs (VPWR)						
	Operating voltage range	[1] [2]				V
$V_{PWR(SS)}$	• Steady-state		5.0	—	28	
$V_{PWR(T)}$	• Transient (t < 500 ms)		—	—	40	
$I_{PWR(SLEEP)}$	Sleep state supply current • EN, $\overline{D2}$, INV, SLEW = Logic [0], IN1, IN2, D1 = Logic [1], and I_{OUT} = 0 A	[3]	—	—	50	µA
$I_{PWR(STANDBY)}$	Standby supply current (part enabled) • I_{OUT} = 0 A, V_{EN} = 5.0 V		—	—	20	mA

Symbol	Characteristic	Min.	Typ.	Max.	Unit
	Undervoltage lockout thresholds				
$V_{UVLO(ACTIVE)}$	• $V_{PWR(FALLING)}$	4.15	—	—	V
$V_{UVLO(INACTIVE)}$	• $V_{PWR(RISING)}$	—	—	5.0	V
$V_{UVLO(HYS)}$	• Hysteresis	150	200	350	mV
Charge Pump					
$V_{CP} - V_{PWR}$	Charge pump voltage (CP capacitor = 33 nF)				V
	• V_{PWR} = 5.0 V	3.5	—	—	
	• V_{PWR} = 28 V	—	—	12	
Control inputs					
V_I	Operating input voltage (EN, IN1, IN2, D1, $\overline{D2}$, INV, SLEW)	—	—	5.5	V
	Input voltage (IN1, IN2, D1, $\overline{D2}$, INV, SLEW) [4]				
V_{IH}	• Logic threshold high	2.0	—	—	V
V_{IL}	• Logic threshold low	—	—	1.0	V
V_{HYS}	• Hysteresis	250	400	—	mV
V_{TH}	Input voltage (EN) threshold	1.0	—	2.0	V
I_{IN}	Logic input currents, V_{PWR} = 5.0 V				µA
	• Inputs EN, $\overline{D2}$, INV, SLEW (internal pull-downs), V_{IH} = 5.0 V	20	80	200	
	• Inputs IN1, IN2, D1 (internal pull-ups), VIL = 0 V	−200	−80	−20	
Power outputs OUT1, OUT2					
$R_{DS(on)}$	Output-on resistance, I_{LOAD} = 3.0 A [5]				mΩ
	• V_{PWR} = 8.0 V, T_J = 25 °C	—	120	—	
	• V_{PWR} = 8.0 V, T_J = 150 °C	—	—	225	
	• V_{PWR} = 5.0 V, T_J = 150 °C	—	—	325	
I_{LIM}	Output current regulation threshold [6]				A
	• $T_J < T_{FB}$	5.2	6.5	8.0	
	• $T_J \geq T_{FB}$ (foldback region - see Figure 10 and Figure 12)	—	4.2	—	
I_{SCH}	High-side short-circuit detection threshold (short-circuit to GND) [6]	11	13	16	A
I_{SCL}	Low-side short-circuit detection threshold (short-circuit to VPWR) [6]	9.0	11	14	A
$I_{OUTLEAK}$	Output leakage current, outputs off, V_{PWR} = 28 V [7]				µA
	• V_{OUT} = V_{PWR}	—	—	100	
	• V_{OUT} = Ground	−60	—	—	
V_F	Output MOSFET body diode forward voltage drop				V
	• I_{OUT} = 3.0 A	—	—	2.0	
	Overtemperature shutdown [6]				°C
T_{LIM}	• Thermal limit at T_J	175	—	200	
T_{HYS}	• Hysteresis at T_J	—	12	—	
T_{FB}	Current foldback at T_J [6]	165	—	185	°C
T_{SEP}	Current foldback to thermal shutdown separation [6]	10	—	15	°C
High-side current sense feedback					
	Feedback current (pin FB sourcing current) [8]				
	• IOUT = 0 mA	0.0	—	50	µA
	• IOUT = 300 mA	0.0	270	750	µA
I_{FB}	• IOUT = 500 mA	0.35	0.775	1.56	mA
	• IOUT = 1.5 A	2.86	3.57	4.28	mA
	• IOUT = 3.0 A	5.71	7.14	8.57	mA
	• IOUT = 6.0 A	11.43	14.29	17.15	mA
Status flag [9]					
	Status flag leakage current [10]				µA
$I_{\overline{SF}LEAK}$	• $V_{\overline{SF}}$ = 5.0 V	—	—	5.0	

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{SFLOW}	Status flag set voltage [11] • I_{SF} = 300 µA	—	—	0.4	V

[1] Device specifications are characterized over the range of 8.0 V ≤ V_{PWR} ≤ 28 V. Continuous operation above 28 V may degrade device reliability. Device is operational down to 5.0 V, but below 8.0 V the output resistance may increase by 50 percent.
[2] Device survives the transient overvoltage indicated for a maximum duration of 500 ms. Transient not to be repeated more than once every 10 seconds.
[3] $I_{PWR(SLEEP)}$ is with sleep mode activated and EN, $\overline{D2}$, INV, SLEW = logic [0], and IN1, IN2, D1 = logic [1] or with these inputs left floating.
[4] SLEW input voltage hysteresis is guaranteed by design.
[5] Output-on resistance as measured from output to VPWR and from output to GND.
[6] This parameter is guaranteed by design.
[7] Outputs switched OFF via D1 or $\overline{D2}$.
[8] Accuracy is better than 20 % from 0.5 A to 6.0 A. Recommended terminating resistor value: R_{FB} = 270 Ω.
[9] Status flag output is an open drain output requiring a pull-up resistor to logic V_{DD}.
[10] Status flag leakage current is measured with status flag high and not set.
[11] Status flag set voltage measured with status flag low and set with $I_{\overline{FS}}$ = 300 µA. Maximum allowable sink current from this pin is < | 500 µA | . Maximum allowable pull-up voltage < 7.0 V.

8.4 Dynamic electrical characteristics

Table 6. Dynamic electrical characteristics

Characteristics noted under conditions 5.0 V ≤ V_{PWR} ≤ 28 V, −40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit
Timing characteristics					
f_{PWM}	PWM frequency [1]	—	—	20	kHz
f_{MAX}	Maximum switching frequency during current limit regulation [2]	—	—	20	kHz
t_{DON}	Output on delay [3] • V_{PWR} = 14 V	——	——	18	µs
t_{DOFF}	Output off delay [3] • V_{PWR} = 14 V	——	——	12	µs
t_A	I_{LIM} output constant-off time [4]	15	20.5	32	µs
t_B	I_{LIM} blanking time [5]	12	16.5	27	µs
$t_{DDISABLE}$	Disable delay time [6]	—	—	8.0	µs
t_F, t_R	Output rise and fall time [7] • SLEW = Slow • SLEW = Fast	 1.5 0.2	 3.0 —	 6.0 1.45	µs
t_{FAULT}	Short-circuit/overtemperature turn-off (latch-off) time [8] [9]	—	—	8.0	µs
t_{POD}	Power-on delay time [9]	—	1.0	5.0	ms
t_{RR}	Output MOSFET body diode reverse recovery time [9]	75	100	150	ns
f_{CP}	Charge pump operating frequency [9]	—	7.0	—	MHz

[1] The maximum PWM frequency is obtained when the device is set to fast slew rate via the SLEW pin. PWM-ing when SLEW is set to slow should be limited to frequencies < 11 kHz to allow the internal high-side driver circuitry time to fully enhance the high-side MOSFETs.
[2] The internal current limit circuitry produces a constant-off-time pulse width modulation of the output current. The output load's inductance, capacitance, and resistance characteristics affect the total switching period (off-time + on-time), and thus the PWM frequency during current limit.
[3] Output delay is the time duration from 1.5 V on the IN1 or IN2 input signal to the 20 % or 80 % point (dependent on the transition direction) of the OUT1 or OUT2 signal. If the output is transitioning high-to-low, the delay is from 1.5 V on the input signal to the 80 % point of the output response signal. If the output is transitioning low-to-high, the delay is from 1.5 V on the input signal to the 20 % point of the output response signal. See Figure 5.
[4] The time during which the internal constant-off time PWM current regulation circuit has tri-stated the output bridge.
[5] The time during which the current regulation threshold is ignored so that the short-circuit detection threshold comparators may have time to act.
[6] Disable delay time measurement is defined in Figure 6.
[7] Rise time is from the 10 % to the 90 % level and fall time is from the 90 % to the 10 % level of the output signal with V_{PWR} = 14 V, R_{LOAD} = 3.0 Ω. See Figure 7.
[8] Load currents ramping up to the current regulation threshold become limited at the I_{LIM} value (see Figure 8). The short-circuit currents possess a di/dt that ramps up to the I_{SCH} or I_{SCL} threshold during the I_{LIM} blanking time, registering as a short-circuit event detection and causing the shutdown circuitry to force the output into an immediate tri-state latch-off (see Figure 9). Operation in current limit mode may cause junction temperatures to rise. Junction

temperatures above ~160 °C causes the output current limit threshold to “foldback”, or decrease, until ~175 °C is reached, after which the T_{LIM} thermal latch-off occurs. Permissible operation within this foldback region is limited to non-repetitive transient events of duration not to exceed 30 seconds (see Figure 10).

[9] Parameter is guaranteed by design.

8.5 Timing diagrams

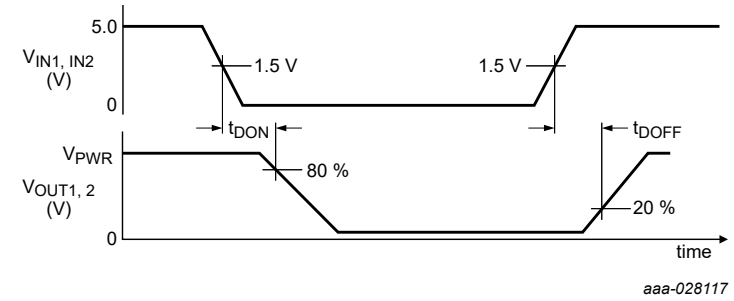


Figure 5. Output delay time

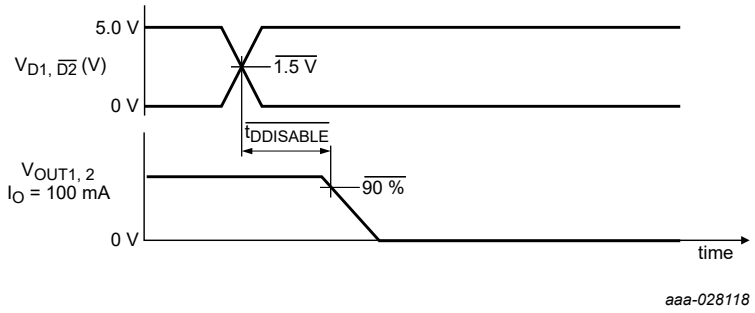


Figure 6. Disable delay time

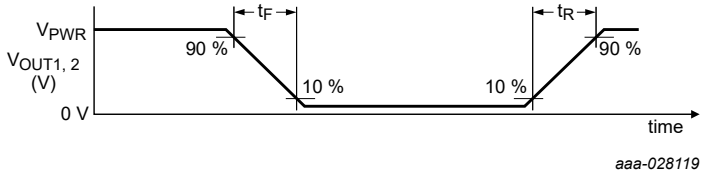


Figure 7. Output switching time

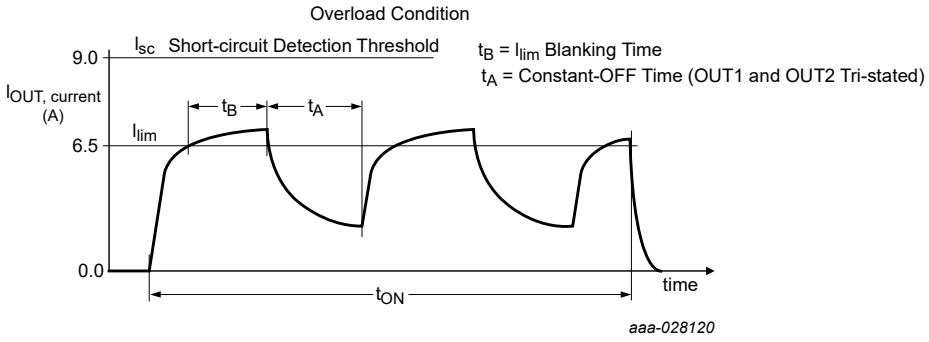


Figure 8. Current limit blanking time and constant-off time

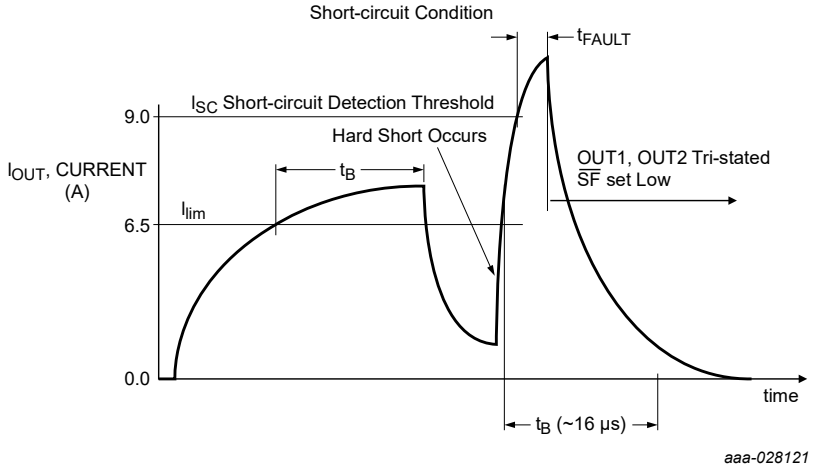


Figure 9. Short-circuit detection turn-off time t_{FAULT}

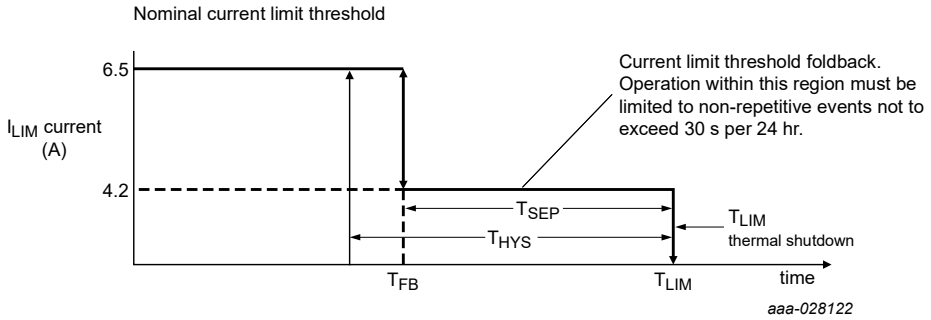


Figure 10. Output current limiting foldback region

9 Functional description

9.1 Introduction

Numerous protection and operational features (speed, torque, direction, dynamic breaking, PWM control, and closed-loop control) make the 33926 a very attractive, cost-effective solution for controlling a broad range of small DC motors. The 33926 outputs are capable of supporting peak DC load currents of up to 5.0 A from a 28 V_{PWR} source. An internal charge pump and gate drive circuitry are provided which can support external PWM frequencies up to 20 kHz.

The 33926 has an analog feedback (current mirror) output pin (the FB pin) providing a constant-current source ratioed to the active high-side MOSFETs' current. This can be used to provide "real time" monitoring of output current to facilitate closed-loop operation for motor speed/torque control, or for the detection of open load conditions.

Two independent inputs, IN1 and IN2, provide control of the two totem-pole half-bridge outputs. An input invert, INV, changes IN1 and IN2 to low = true logic. Two different output slew rates are selectable via the SLEW input. Two independent disable inputs, D1 and $\overline{D2}$, provide the means to force the H-bridge outputs to a high-impedance state (all H-bridge switches off). An EN pin controls an enable function allowing the IC to be placed in a power-conserving sleep mode.

The 33926 has output current limiting (via constant off-time PWM current regulation), output short-circuit detection with latch-off, and overtemperature detection with latch-off.

Once the device is latched-off due to a fault condition, either of the disable inputs (D1 or $\overline{D2}$), V_{PWR}, or EN must be "toggled" to clear the status flag.

Current limiting (load current regulation) is accomplished by a constant-off time PWM method using current limit threshold triggering. The current limiting scheme is unique in that it incorporates a junction temperature-dependent current limit threshold. This means the current limit threshold is "reduced to around 4.2 A" as the junction temperature increases above 160 °C. When the temperature is above 175 °C, overtemperature shutdown (latch-off) occurs. This combination of features allows the device to continue operating for short periods of time (< 30 seconds) with unexpected loads, while still retaining adequate protection for both the device and the load.

9.2 Functional pin description

9.2.1 Power ground and analog ground (PGND and AGND)

The power and analog ground pins should be connected together with a very low-impedance connection.

9.2.2 Positive power supply (VPWR)

VPWR pins are the power supply inputs to the device. All VPWR pins must be connected together on the printed circuit board with traces as short as possible, offering as low-impedance as possible between pins. Transients on V_{PWR} going below the undervoltage threshold result in the protection activating. It is essential to use an input filter capacitor of sufficient size and low ESR to sustain a V_{PWR} greater than V_{UVLO} when the load is switched (see Section 12 "Typical applications").

9.2.3 Status flag ($\overline{SF}$)

This pin is the device fault status output. This output is an active low open drain structure requiring a pull-up resistor to V_{DD}. The maximum V_{DD} is < 7.0 V. See Table 7 for the $\overline{SF}$ output status definition.

9.2.4 Input invert (INV)

The input invert control pin sets IN1 and IN2 to low = true. This is a Schmitt trigger input with ~80 µA sink; the default condition is non-inverted. If IN1 and IN2 are set so the current is being commanded to flow through the load attached between OUT1 and OUT2, changing the logic level at INV has the effect of reversing the direction of current commanded. Thus, the INV input may be used as a "forward/ reverse" command input. If both IN1 and IN2 are the same logic level, then changing the logic level at INV has the effect of changing the bridge's output from freewheeling high to freewheeling low or vice versa.

9.2.5 Slew rate (SLEW)

The SLEW pin is the logic input selecting fast or slow slew rates. It is a Schmitt trigger input with ~80 µA sink, so the default condition is slow. When SLEW is set to slow, PWM-ing should be limited to frequencies less than 11 kHz to allow the internal high-side driver circuitry time to fully enhance the high-side MOSFETs.

9.2.6 Input 1, 2 and disable input 1, 2 (IN1, IN2, and D1, $\overline{D2}$)

These pins are input control pins used to control the outputs, and are 3.0 V/ 5.0 V CMOS-compatible inputs with hysteresis. IN1 and IN2 independently control OUT1 and OUT2, respectively. D1 and $\overline{D2}$ are complementary inputs used to tri-state disable the H-bridge outputs.

When either D1 or $\overline{D2}$ is SET (D1 = logic high or $\overline{D2}$ = logic low) in the disable state, the outputs OUT1 and OUT2 are both tri-state disabled; however, the rest of the device circuitry is fully operational and the supply $I_{PWR(STANDBY)}$ current is reduced to a few mA. See Table 5.

9.2.7 H-bridge output (OUT1, OUT2)

These pins are the outputs of the H-bridge with integrated freewheeling diodes. The bridge output is controlled using the IN1, IN2, D1, and $\overline{D2}$ inputs. The outputs have PWM current limiting above the I_{LIM} threshold. The outputs also have thermal shutdown (tri-state latch-off) with hysteresis as well as short-circuit latch-off protection. A disable timer (time t_B) is incorporated to distinguish between load currents higher than the I_{LIM} threshold and short-circuit currents. This timer is activated at each output transition.

9.2.8 Charge pump capacitor (CCP)

This pin is the charge pump output pin and connection for the external charge pump reservoir capacitor. The allowable value is from 30 nF to 100 nF. This capacitor must be connected from the CCP pin to the VPWR pin. The device cannot operate properly without the external reservoir capacitor.

9.2.9 Enable input (EN)

The EN pin is used to place the device in a sleep mode so as to consume very low currents. When the EN pin voltage is a logic low state, the device is in sleep mode. The device is enabled and fully operational when the EN pin voltage is in logic high. An internal pull-down resistor maintains the device in sleep mode in the event EN is driven through a high-impedance I/O, or an unpowered microcontroller, or the EN input becomes disconnected.

9.2.10 Feedback (FB)

The 33926 has a feedback output (FB) for "real time" monitoring of H-bridge high-side output currents to facilitate closed-loop operation for motor speed and torque control.

The FB pin provides current sensing feedback of the H-bridge high-side drivers. When running in the forward or reverse direction, a ground-referenced 0.24 % of load current is output to this pin. Through the use of an external resistor to ground, the proportional feedback current can be converted to a proportional voltage equivalent and the controlling microcontroller can "read" the current proportional voltage with its analog-to-digital converter (ADC). This is intended to provide the user with only first-order motor current feedback for motor torque control. The resistance range for the linear operation of the FB pin is 100 Ω < R_{FB} < 300 Ω.

If PWM-ing is implemented using the disable pin inputs (either D1 or $\overline{D2}$), a small filter capacitor (~1.0 µF) may be required in parallel with the R_{FB} resistor to ground for spike suppression.

10 Functional internal block description

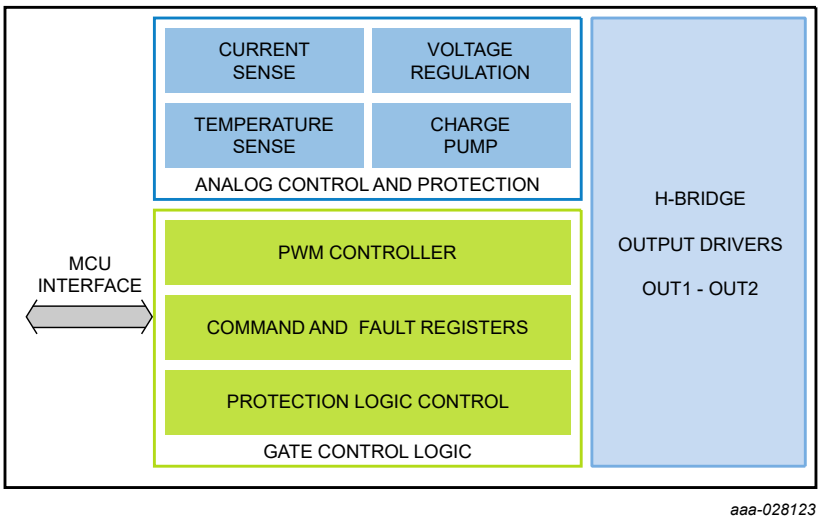


Figure 11. Functional internal block diagram

10.1 Analog control and protection circuitry

The on-chip voltage regulator supplies 3.3 V to the internal logic. The charge pump provides gate drive for the H-bridge MOSFETs. The current and temperature sense circuitry provides detection and protection for the output drivers. Output undervoltage protection shuts down the MOSFETS.

10.2 Gate control logic

The 33926 is a monolithic H-bridge power IC designed primarily for any low voltage DC servo motor control application within the current and voltage limits stated for the device. Two independent inputs provide polarity control of two half-bridge totem-pole outputs. Two independent disable inputs are provided to force the H-bridge outputs to tri-state (high-impedance off-state).

10.3 H-bridge output drivers: OUT1 and OUT2

The H-bridge is the power output stage. The current flow from OUT1 to OUT2 is reversible and under full control of the user by way of the input control logic. The output stage is designed to produce full load control under all system conditions. All protective and control features are integrated into the control and protection blocks. The sensors for current and temperature are integrated directly into the output MOSFET for maximum accuracy and dependability.

11 Functional device operation

11.1 Operational modes

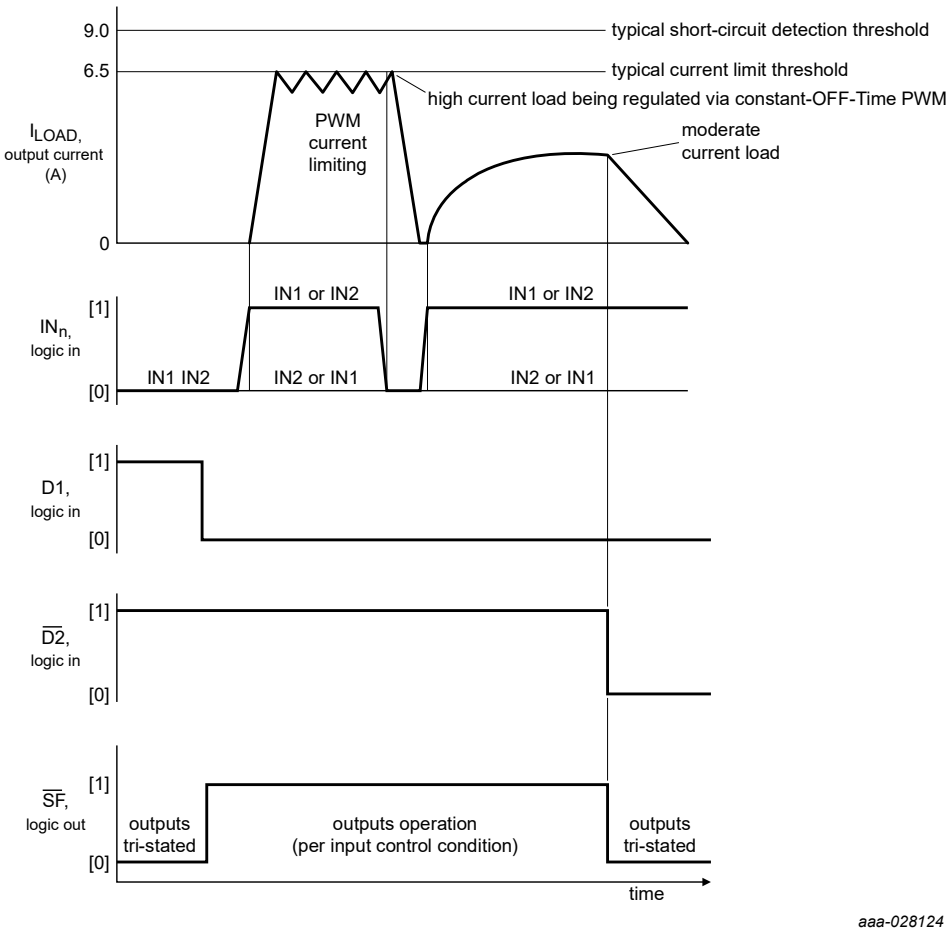


Figure 12. Operating states

11.2 Logic commands and registers

Table 7. Truth table

The tri-state conditions and the status flag are reset using D1 or $\overline{D2}$. The truth table uses the following notations: L = low, H = high, X = high or low, and Z = high-impedance. All output power transistors are switched off.

Device state	Input conditions					Status	Outputs	
	EN	D1	$\overline{D2}$	IN1	IN2	$\overline{SF}$	OUT1	OUT2
Forward	H	L	H	H	L	H	H	L
Reverse	H	L	H	L	H	H	L	H
Freewheeling low	H	L	H	L	L	H	L	L
Freewheeling high	H	L	H	H	H	H	H	H
Disable 1 (D1)	H	H	X	X	X	L	Z	Z
Disable 2 ($\overline{D2}$)	H	X	L	X	X	L	Z	Z
IN1 disconnected	H	L	H	Z	X	H	H	X
IN2 disconnected	H	L	H	X	Z	H	X	H
D1 disconnected	H	Z	X	X	X	L	Z	Z
$\overline{D2}$ disconnected	H	X	Z	X	X	L	Z	Z
Undervoltage lockout [1]	H	X	X	X	X	L	Z	Z
Overtemperature [2]	H	X	X	X	X	L	Z	Z
Short-circuit [2]	H	X	X	X	X	L	Z	Z
Sleep mode EN	L	X	X	X	X	H	Z	Z
EN disconnected	Z	X	X	X	X	H	Z	Z

[1] In the event of an undervoltage condition, the outputs tri-state and status flag are set to logic low. Upon undervoltage recovery, status flag is reset automatically or automatically cleared and the outputs are restored to their original operating condition.

[2] When a short-circuit or overtemperature condition is detected, the power outputs are tri-state latched-off, independent of the input signals, and the status flag is latched to logic low. To reset from this condition requires the toggling of either D1, $\overline{D2}$, EN, or V_{PWR}.

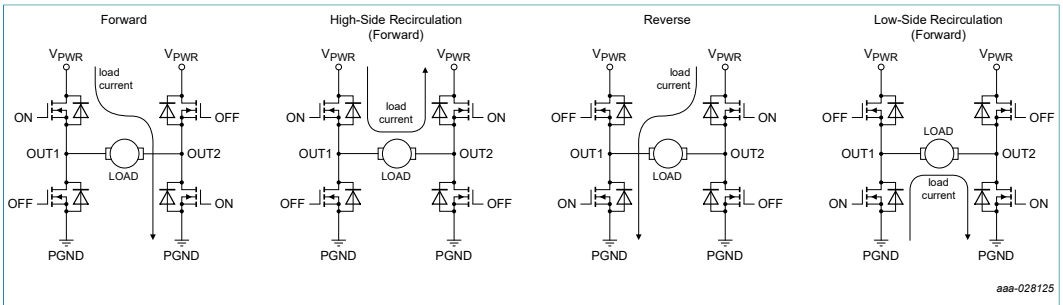


Figure 13. Power stage operation

11.3 Protection and diagnostic features

11.3.1 Short-circuit protection

If an output short-circuit condition is detected, the power outputs tri-state (latch-off) independent of the input (IN1 and IN2) states, and the fault status output flag ($\overline{SF}$) is set to a logic low. If the D1 input changes from a logic high to logic low, or if the $\overline{D2}$ input changes from a logic low to logic high, the output bridge becomes operational again, and the fault status flag resets (cleared) to a logic high state. The output stage always

switches into the mode defined by the input pins (IN1, IN2, D1, and $\overline{D2}$), provided the device junction temperature is within the specified operating temperature range.

11.3.2 Internal PWM current limiting

The maximum current flow under normal operating conditions should be less than 5.0 A. The instantaneous load currents are limited to I_{LIM} via the internal PWM current limiting circuitry. When the I_{LIM} threshold current value is reached, the output stages are tri-stated for a fixed time (T_A) of 20 µs, typical. Depending on the time constant associated with the load characteristics, the output current decreases during the tri-state duration until the next output on cycle occurs.

The PWM current limit threshold value is dependent on the device junction temperature. When −40 °C < T_J < 160 °C, I_{LIM} is between the specified minimum/maximum values. When T_J exceeds 160 °C, the I_{LIM} threshold decreases to 4.2 A. Shortly above 175 °C the device overtemperature circuit detects T_{LIM} and an overtemperature shutdown occurs. This feature implements a graceful degradation of operation before thermal shutdown occurs, thus allowing for intermittent unexpected mechanical loads on the motor's gear-reduction train to be handled.

Important:

Die temperature excursions above 150 °C are permitted only for non-repetitive durations < 30 seconds. Provision must be made at the system level to prevent prolonged operation in the current-foldback region.

11.3.3 Overtemperature shutdown and hysteresis

If an overtemperature condition occurs, the power outputs are tri-stated (latched-off), and the fault status flag ($\overline{SF}$) is set to a logic low.

To reset from this condition, D1 must change from a logic high to logic low, or $\overline{D2}$ must change from a logic low to logic high. When reset, the output stage switches on again, provided the junction temperature is now below the overtemperature threshold limit minus the hysteresis.

Important:

Resetting from the fault condition clears the fault status flag. Powering down and powering up the device also resets the 33926 from the fault condition.

11.3.4 Output avalanche protection

If VPWR becomes an open circuit, the outputs likely tri-states simultaneously due to the disable logic. This could result in an unclamped inductive discharge. The VPWR input to the 33926 should not exceed 40 V during this transient condition, to prevent electrical overstress of the output drivers. This can be accomplished with a zener clamp or MOV, and/or an appropriately valued input capacitor with sufficiently low ESR (see Figure 14).

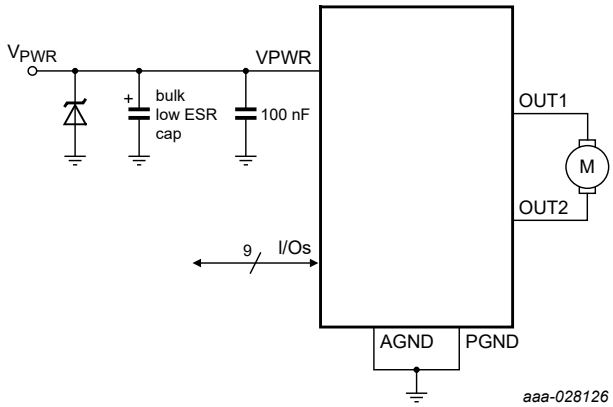


Figure 14. Avalanche protection

12 Typical applications

12.1 Introduction

A typical application schematic is shown in Figure 15. For precision high current applications in harsh, noisy environments, the V_{PWR} bypass capacitor may need to be substantially larger.

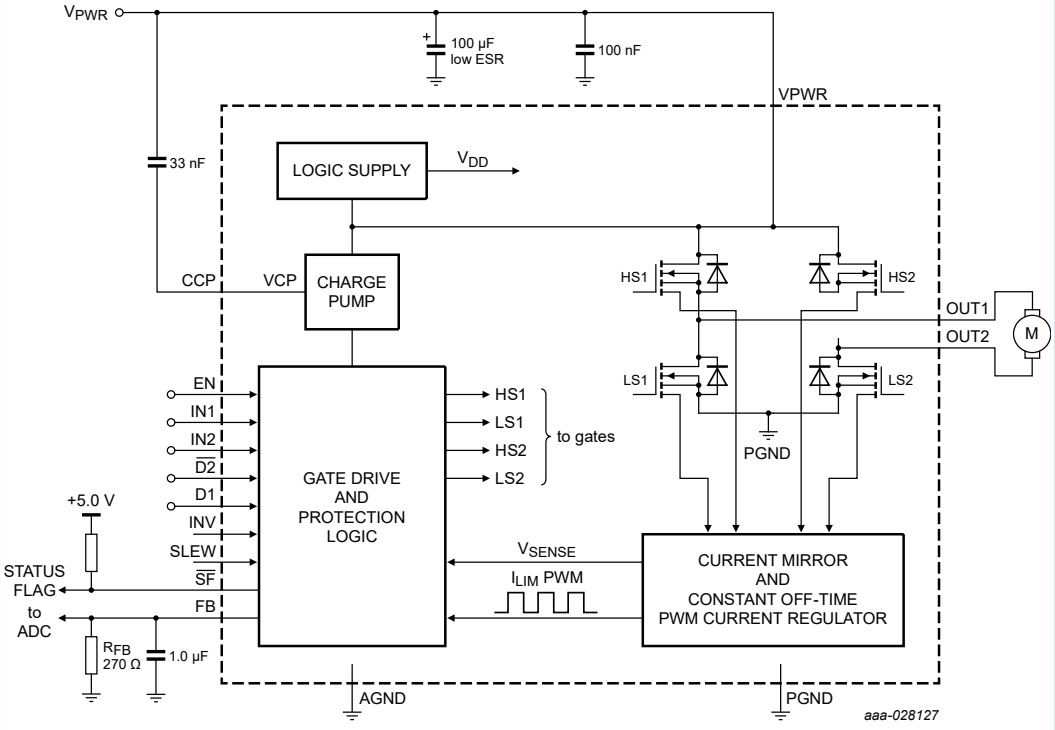


Figure 15. Typical application schematic

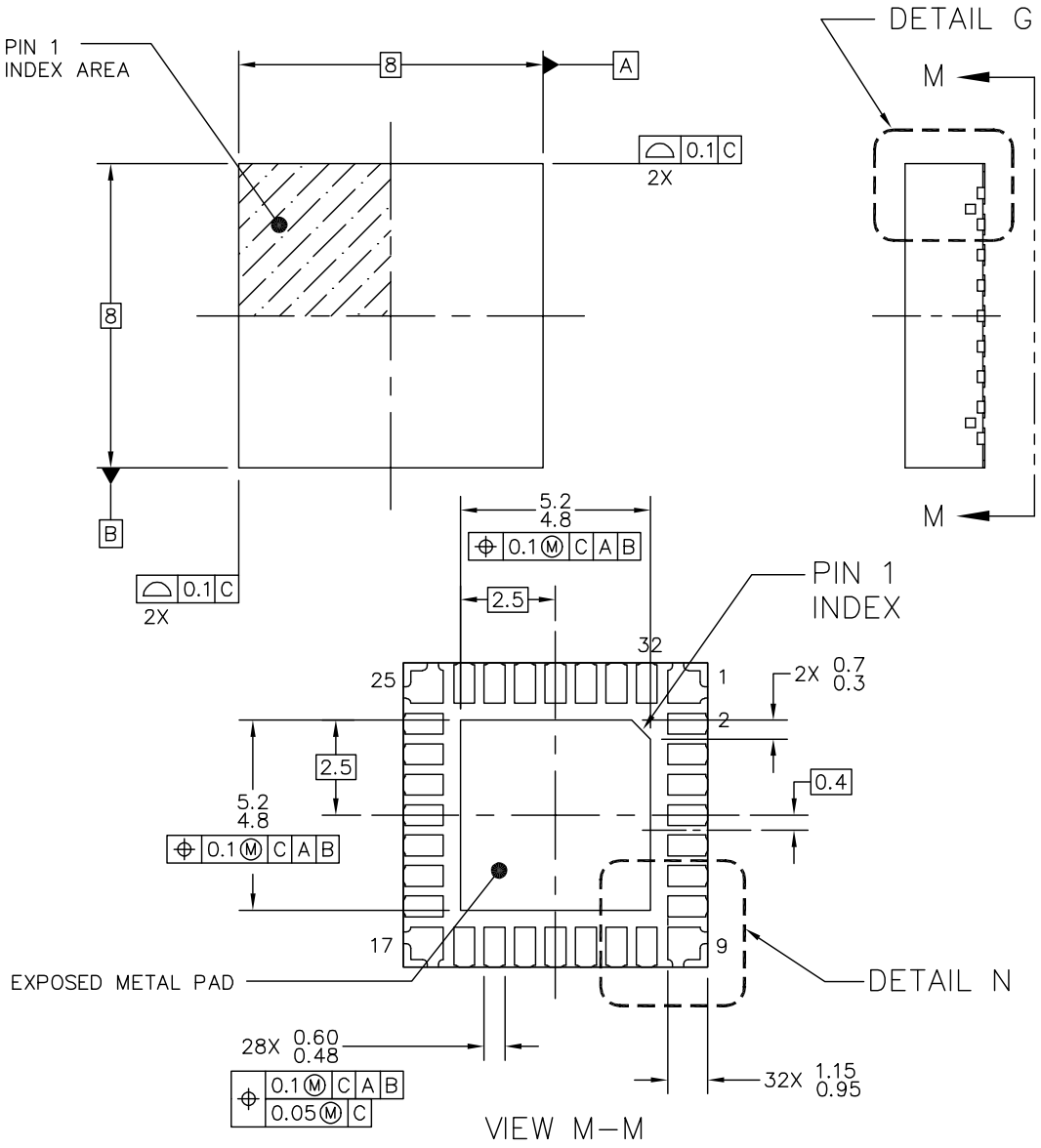
13 Packaging

13.1 Package mechanical dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number.

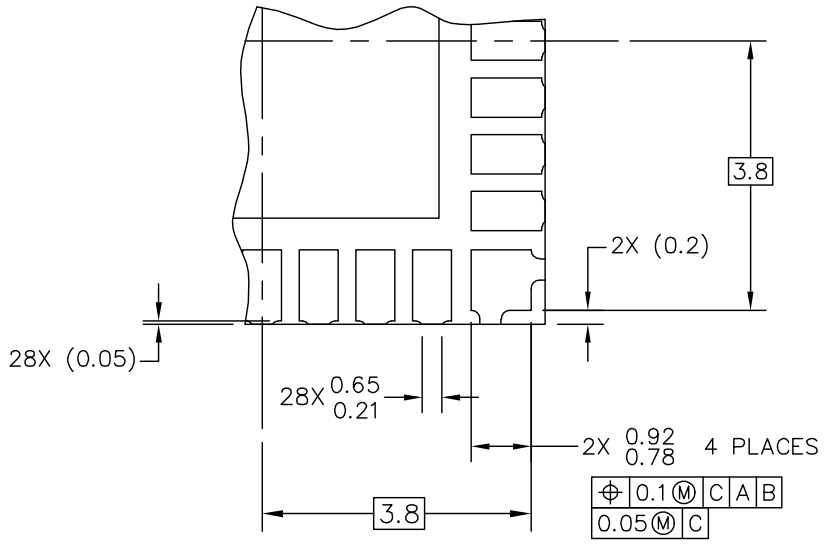
Table 8. Package outline

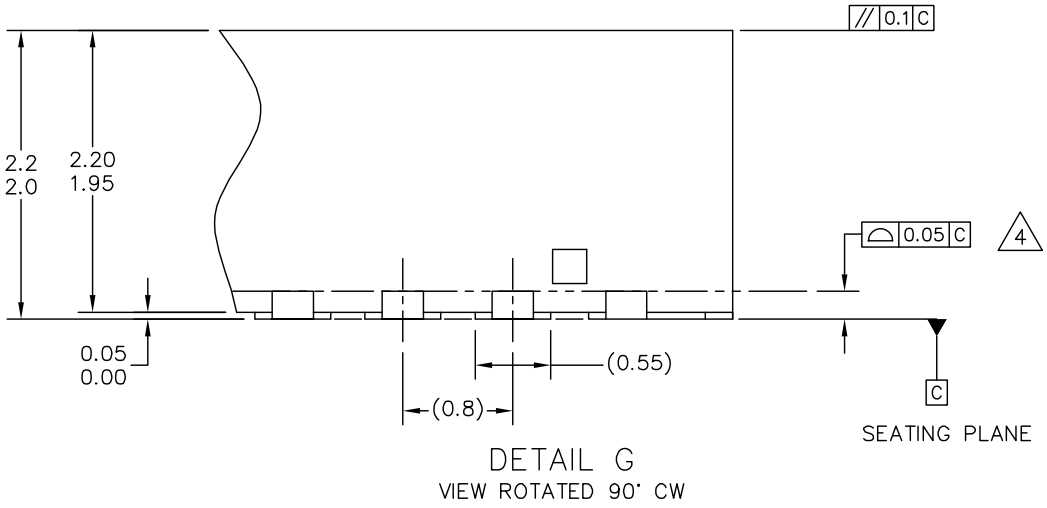
Package	Suffix	Package outline drawing number
32-pin PQFN	PNB	98ARL10579D
28-pin HVQFN	ES	98ASA00993D



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: POWER QUAD FLAT NON–LEADED PACKAGE (PWR QFN), 32 TERMINAL, 0.8 PITCH(8X8X2.1)	DOCUMENT NO: 98ARL10579D	REV: C
	CASE NUMBER: 1536–04	31 OCT 2006
	STANDARD: JEDEC MO–251A ADDB–1	

Figure 16. Package outline for 32-pin PQFN





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TITLE: POWER QUAD FLAT NON–LEADED PACKAGE (PWR QFN), 32 TERMINAL, 0.8 PITCH(8X8X2.1)	DOCUMENT NO: 98ARL10579D	REV: C
	CASE NUMBER: 1536–04	31 OCT 2006
	STANDARD: JEDEC MO–251A ADDB–1	

Figure 17. Package outline detail for 32-pin PQFN

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: F–PQFP–N.
4. COPLANARITY APPLIES TO LEADS AND CORNER LEADS.
5. MINIMUM METAL GAP SHOULD BE 0.25MM.

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TITLE: POWER QUAD FLAT NON–LEADED PACKAGE (PWR QFN), 32 TERMINAL, 0.8 PITCH(8X8X2.1)	DOCUMENT NO: 98ARL10579D	REV: C
	CASE NUMBER: 1536–04	31 OCT 2006
	STANDARD: JEDEC MO–251A ADDB–1	

Figure 18. Package outline notes for 32-pin PQFN

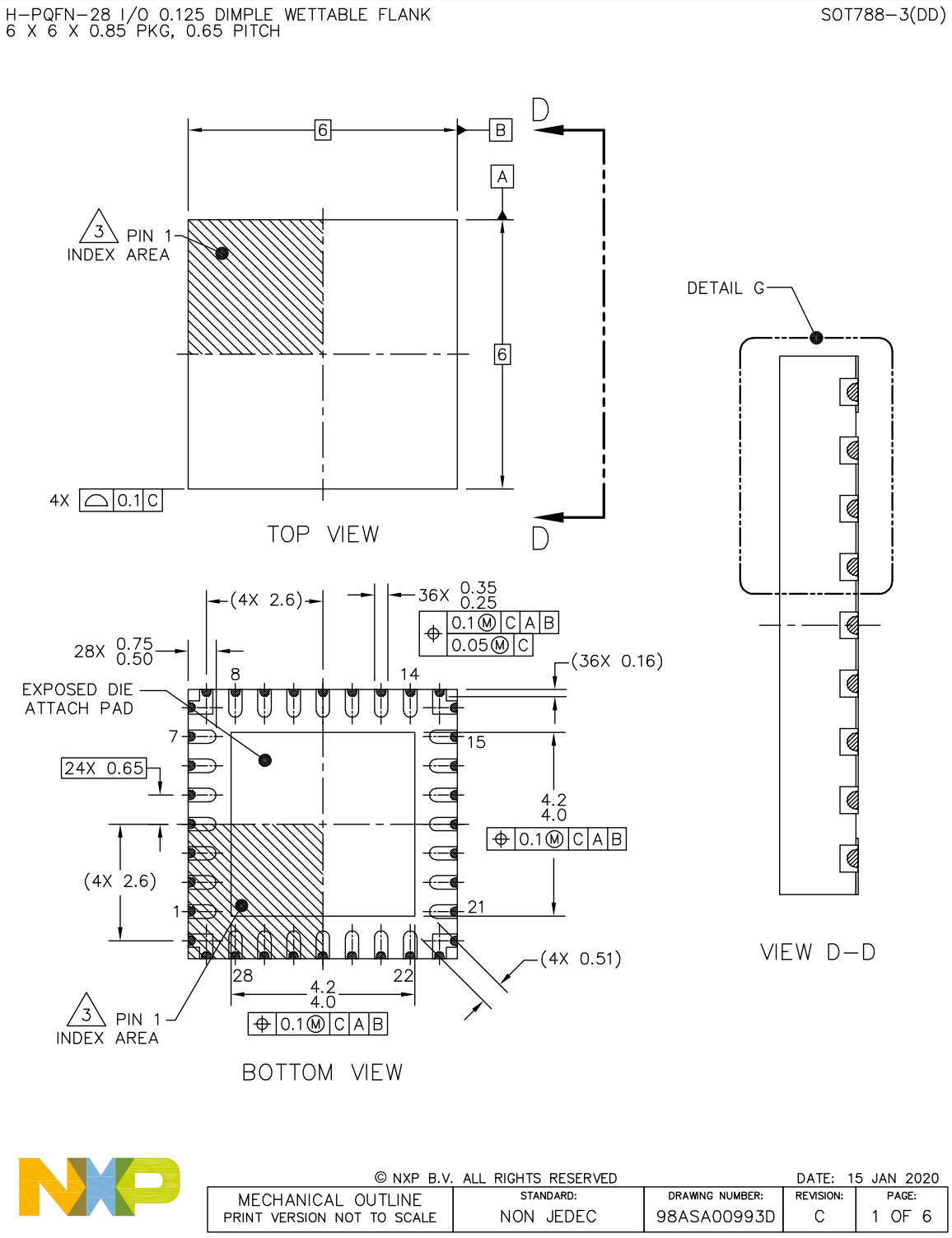
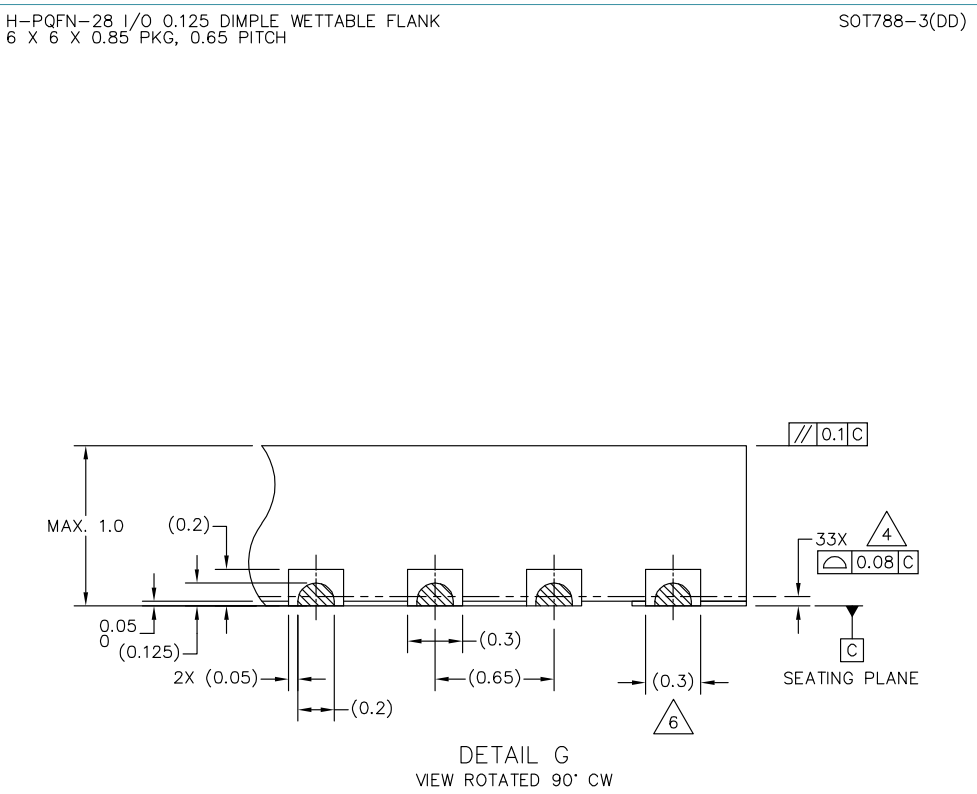


Figure 19. Package outline for 28-pin HVQFN



DATE: 15 JAN 2020

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA00993D	REVISION: C	PAGE: 2

Figure 20. Package outline detail for 28-pin HVQFN

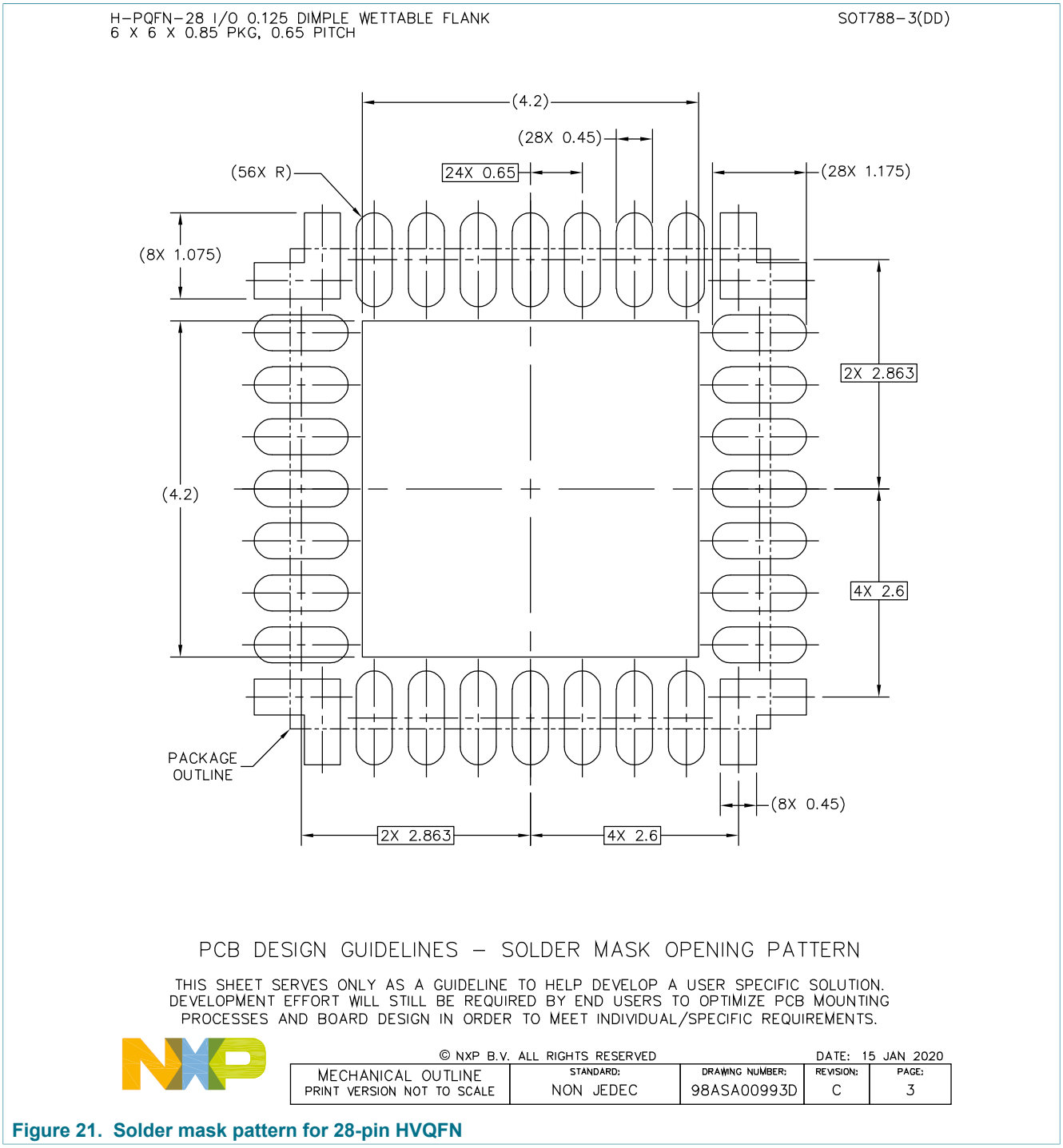


Figure 21. Solder mask pattern for 28-pin HVQFN

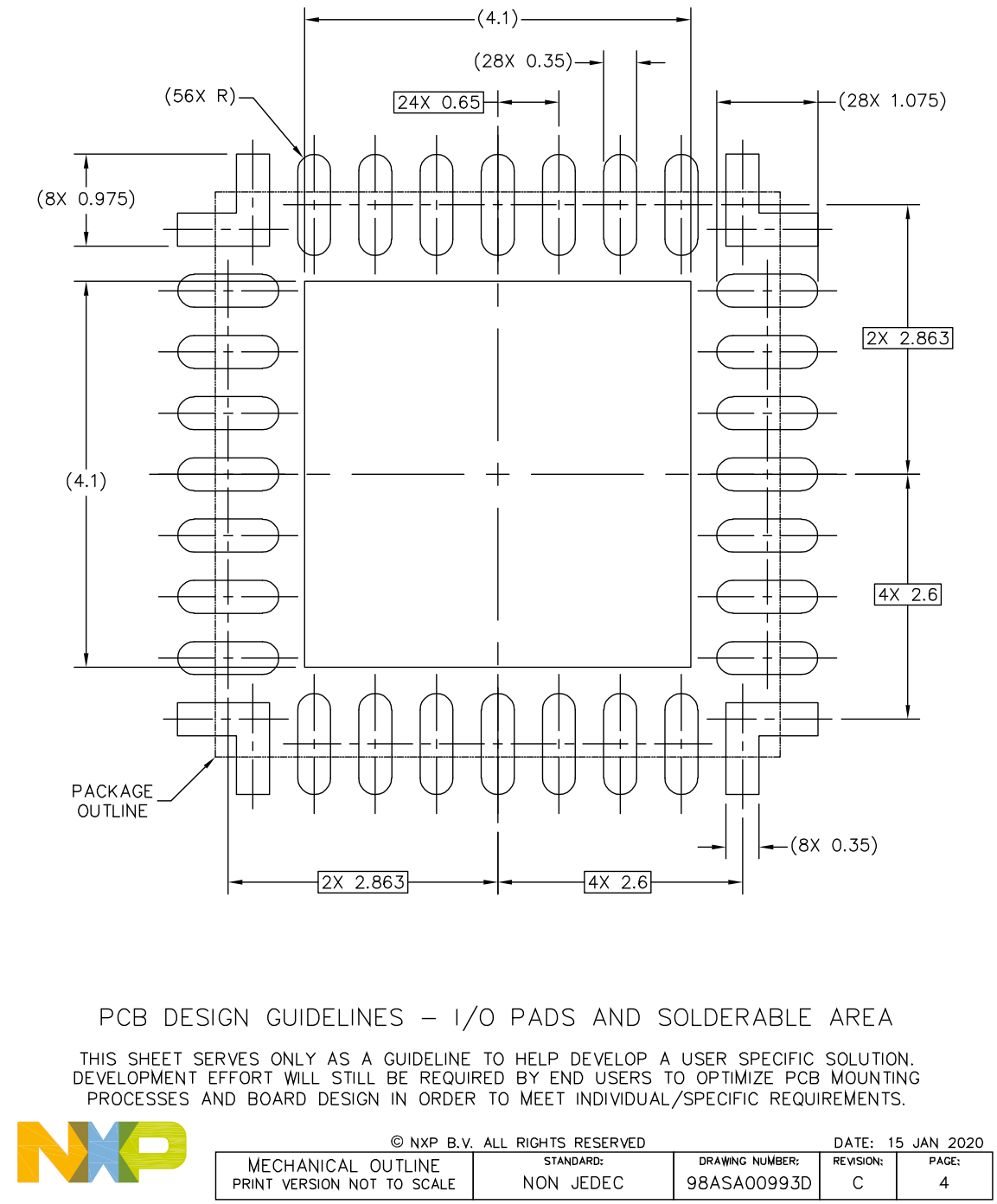


Figure 22. I/O pads and solderable areas for 28-pin HVQFN

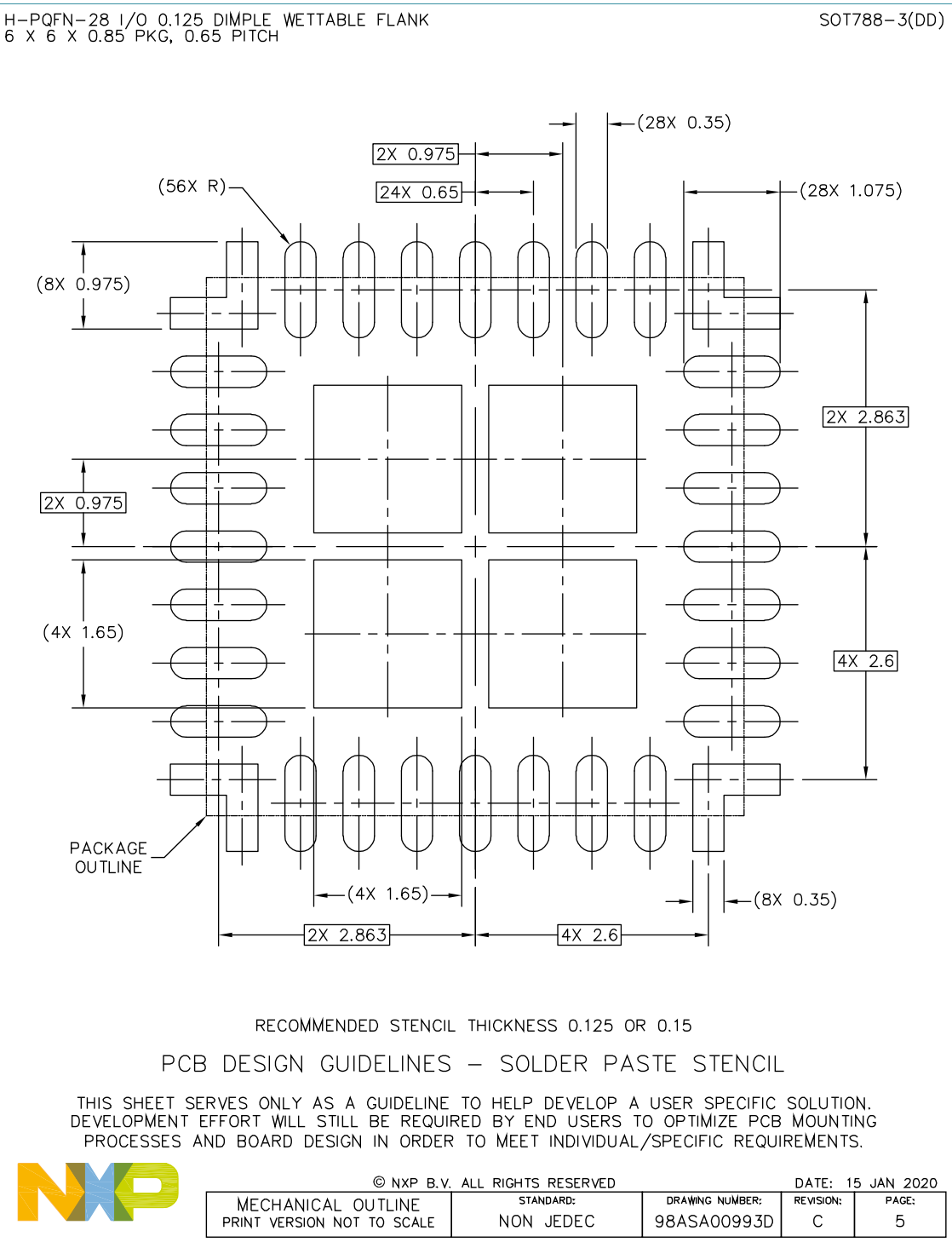


Figure 23. Solder paste stencil for 28-pin HVQFN

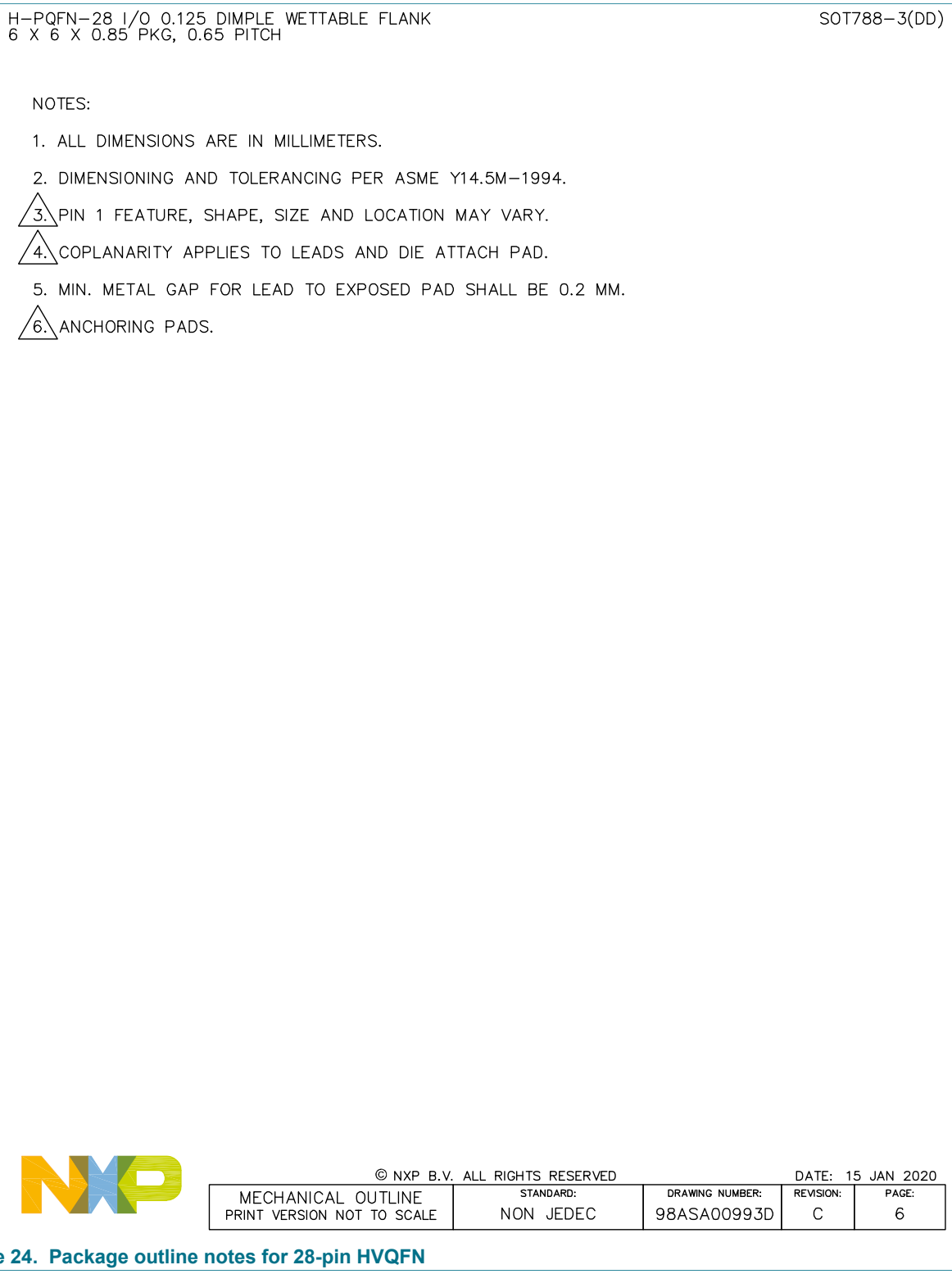


Figure 24. Package outline notes for 28-pin HVQFN

14 Additional documentation

14.1 Thermal addendum 32 PQFN only (Rev. 2.0)

14.1.1 Introduction

This thermal addendum is provided as a supplement to the 33926 technical data sheet. The addendum provides thermal performance information that may be critical in the design and development of system applications. All electrical, application, and packaging information is provided in the data sheet.

14.1.2 Packaging and thermal considerations

The 33926 is offered in a 32-pin PQFN, single die package. There is a single heat source (P), a single junction temperature (T_J), and thermal resistance ($R_{\theta JA}$).

$\{T_J\} = [R_{\theta JA}] \cdot \{P\}$

The stated values are solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to, and will not predict the performance of a package in an application-specific environment. Stated values were obtained by measurement and simulation according to the standards listed in Section 14.1.3 "Standards".

14.1.3 Standards

Table 9. Thermal performance comparison

Thermal resistance	[°C/W]
$R_{\theta JA}$ [1][2]	28
$R_{\theta JB}$ [2][3]	12
$R_{\theta JA}$ [1][4]	80
$R_{\theta JC}$ [5]	1.0

[1] Per JEDEC JESD51-2 at natural convection, still air condition.
[2] 2s2p thermal test board per JEDEC JESD51-5 and JESD51-7.
[3] Per JEDEC JESD51-8, with the board temperature on the center trace near the center lead.
[4] Single layer thermal test board per JEDEC JESD51-3 and JESD51-5.
[5] Thermal resistance between the die junction and the exposed pad surface; cold plate attached to the package bottom side, remaining surfaces insulated.

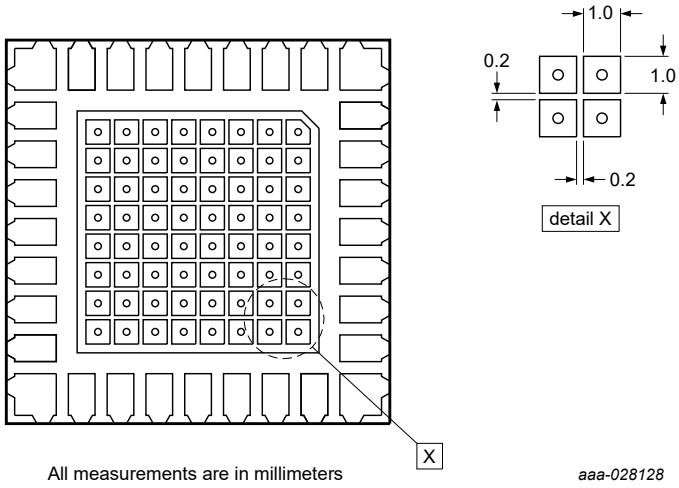


Figure 25. Surface mount for power PQFN with exposed pad

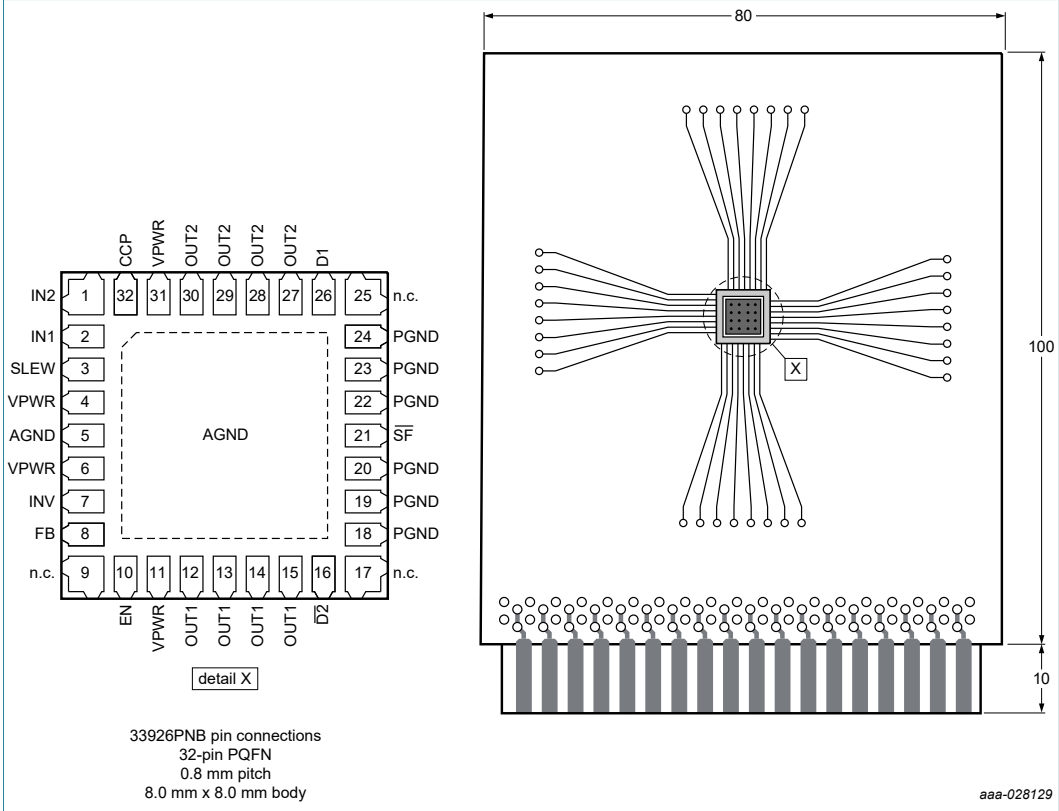


Figure 26. Thermal test board

14.1.4 Device on thermal test board

Material:	single layer printed circuit board FR4, 1.6 mm thickness Cu traces, 0.07 mm thickness
Outline:	80 mm x 100 mm board area, including edge connector for thermal testing
Area A:	Cu heat-spreading areas on board surface
Ambient conditions:	natural convection, still air

Table 10. Thermal resistance performance

A [mm^2]	$R_{\theta JA}$ [°C/W]
0	81
300	49
600	40

$R_{\theta JA}$ is the thermal resistance between die junction and ambient air.

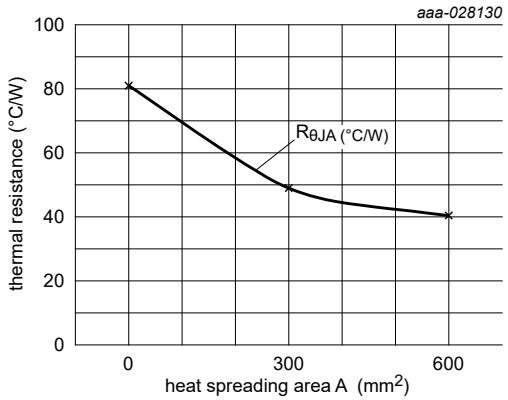


Figure 27. Device on thermal test board $R_{\theta JA}$

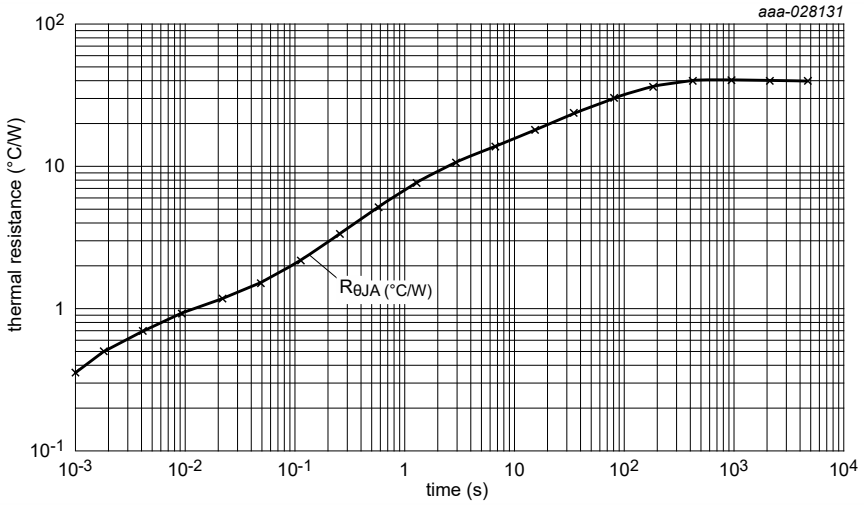


Figure 28. Transient thermal resistance $R_{\theta JA}$,1.0 W step response, device on thermal test board area A = 600 (mm^2)

15 Revision history

Revision	Date	Description of changes
1.0	3/2006	• Updated formatting and technical content throughout entire document
2.0	6/2007	• Updated formatting and technical content throughout entire document
3.0	10/2006	• Updated formatting and technical content throughout entire document
4.0	12/2006	• Updated formatting and technical content throughout entire document
5.0	2/2007	• Updated formatting and technical content throughout entire document
6.0	3/2007	• Changed Human Body Model, Charge Pump Voltage (CP Capacitor = 33 nF), No PWM and PWM = 20kHz, Slew Rate = Fast, Output Rise and Fall Time • Added second paragraph to Section 9.2.2 "Positive power supply (VPWR)" • Added “Low ESR” to 100 µF in Figure 15
7.0	6/2007	• Changed status to Advance Information
8.0	4/2009	• Minor corrections and clarifications
9.0	12/2009	• Changed minimum operating voltage range from 8.0 to 5.0
10	8/2014	• Updated the overall format to new standards with no change to document content • Added SMARTMOS to the page 1 description. Added application. Moved the ordering information to page 2 • Updated the back page
11	10/2017	• Updated document format • Added PC33926ES to ordering information table • Added pinout diagram for 28-pin HVQFN and updated pin definitions table • Added package drawing for 28-pin HVQFN
12	6/2018	• Deleted thermal ratings from Table 3 • Added Section 8.2
13	8/2018	• Added AEC-Q100 grade 1 qualified to Section 1 and Section 3
14	10/2019	• Section 7.1: updated Figure 4 • Table 4: updated max value for T_{PPRT} (replaced 250 by 260) • Section 13.1: updated package outline drawing (98ASA00993D)
15	10/2019	• Table 1: replaced PC33926ES by MC33926AES • Table 4: updated Ψ_{JT} value for MC33926AES (replaced 0.83 by 2.1)
16	2/2020	• Updated as per CIN 202002025I – Figure 4: updated 28-pin HVQFN pin configuration to indicate four corner pads as AGND – Section 13.1: added 28-pin HVQFN solder mask information

16 Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
[short] Data sheet: product preview	Development	This document contains certain information on a product under development. NXP reserves the right to change or discontinue this product without notice.
[short] Data sheet: advance information	Qualification	This document contains information on a new product. Specifications and information herein are subject to change without notice.
[short] Data sheet: technical data	Production	This document contains the product specification. NXP Semiconductors reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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