THE DATASHEET OF

MC33912BAC

NXP Semiconductors
Technical Data

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LIN system basis chip with dc motor pre-driver and current sense

33912

SYSTEM BASIS CHIP WITH LIN 2ND GENERATION

AC SUFFIX (Pb-FREE)
98ASH70029A
32-PIN LQFP

The 33912G5/BAC is a Serial Peripheral Interface (SPI) controlled System Basis Chip (SBC), combining many frequently used functions in an MCU based system, plus a Local Interconnect Network (LIN) transceiver. The 33912 has a 5.0 V, 50 mA/60 mA low dropout regulator with full protection and reporting features. The device provides full SPI readable diagnostics and a selectable timing watchdog for detecting errant operation. The LIN Protocol Specification 2.0 and 2.1 compliant LIN transceiver has waveshaping circuitry which can be disabled for higher data rates.

Two 50 mA/60 mA high-side switches and two 150 mA/160 mA low-side switches with output protection are available. All outputs can be pulse-width modulated (PWM). Four high voltage inputs are available for use in contact monitoring, or as external wake-up inputs. These inputs can be used as high voltage Analog Inputs. The voltage on these pins is divided by a selectable ratio and available via an analog multiplexer.

The 33912 has three main operating modes: Normal (all functions available), Sleep (V_{DD} off, wake-up via LIN, wake-up inputs (L1-L4), cyclic sense and forced wake-up), and Stop (V_{DD} on with limited current capability, wake-up via $\overline{CS}$, LIN bus, wake-up inputs, cyclic sense, forced wake-up and external reset).

The 33912 is compatible with LIN Protocol Specification 2.0, 2.1, and SAEJ2602-2. This device is powered using SMARTMOS technology.

Features

- Full-duplex SPI interface at frequencies up to 4.0 MHz
- LIN transceiver capable of up to 100 kbps with wave shaping
- Current sense module
- Four high voltage analog/logic Inputs
- Configurable window watchdog
- Switched/protected 5.0 V output (used for Hall sensors)
- Two 50 mA high-side and two 150 mA/160 mA low-side protected switches
- 5.0 V low drop regulator with fault detection and low voltage reset (LVR) circuitry

Applications

- Door module: window
- Lift, mirror, door lock, seat control switch
- Seat position motors, occupancy sensor
- Rain and light sensor, light control, sun roof
- Wiper, turning light, cruise control
- Climate: small motors, control panel
- Engine control: sensors, small motors

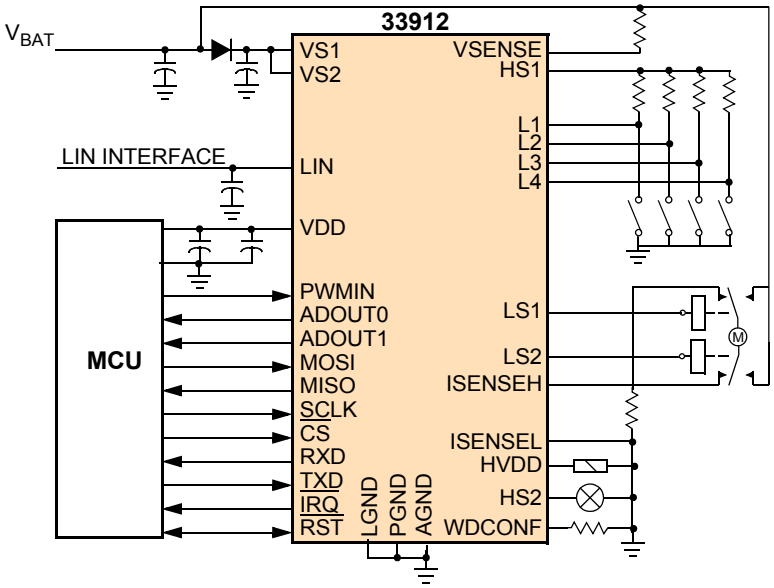


Figure 1. 33912 simplified application diagram

1 Orderable parts

The 33912G5 data sheet is within MC33912G5 product specifications, Pages 3 to 52
The 33912BAC data sheet is within MC33912BAC product specifications, Pages 53 to 103

Table 1. Orderable part variations

Part number [1]	Temperature (T_A)	Package	Generation	Changes
MC33912G5AC	-40 to 125 °C	32-LQFP	2.5	1. Increase ESD Gun IEC61000-4-2 (gun test contact with 150 pF, 330 ohm test conditions) performance to achieve ±6.0 kV min on the LIN pin. 2. Immunity against ISO7637 pulse 3b 3. Reduce EMC emission level on LIN 4. Improve EMC immunity against RF - target new specification including 3x68pF 5. Comply with J2602 conformance test
MC34912G5AC	-40 to 85 °C			
MC33912BAC	-40 to 125 °C		2.0	Initial release
MC34912BAC	-40 to 85 °C			

Notes
1. To order parts in Tape & Reel, add the R2 suffix to the part number.

2 MC33912G5 product specifications, Pages 3 to 52

3 Internal block diagram

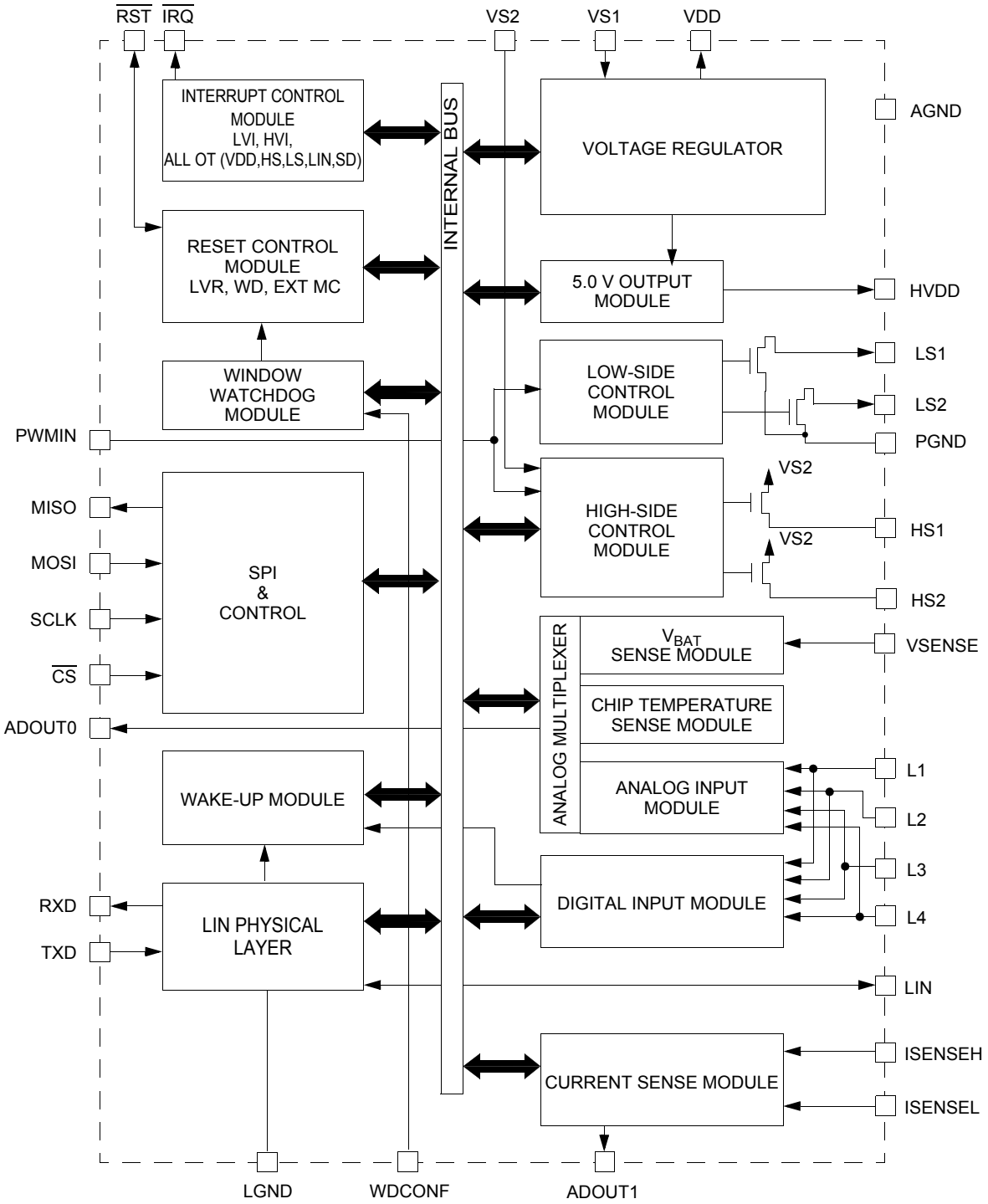


Figure 2. 33912 simplified internal block diagram

4 Pin connections

4.1 Pinout diagram

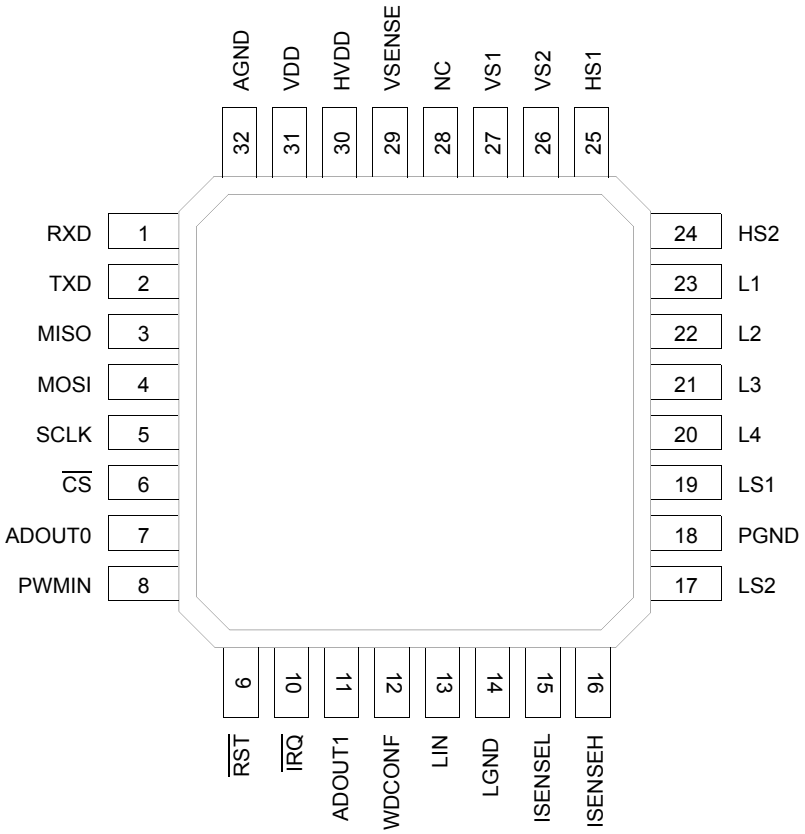


Figure 3. 33912 pin connections

A functional description of each pin can be found in the Functional pin description section beginning on page 23.

Table 2. 33912 pin definitions

Pin	Pin name	Formal name	Definition
1	RXD	Receiver Output	This pin is the receiver output of the LIN interface which reports the state of the bus voltage to the MCU interface.
2	TXD	Transmitter Input	This pin is the transmitter input of the LIN interface which controls the state of the bus output.
3	MISO	SPI Output	SPI (Serial Peripheral Interface) data output. When $\overline{CS}$ is high, pin is in the high-impedance state.
4	MOSI	SPI Input	SPI (Serial Peripheral Interface) data input.
5	SCLK	SPI Clock	SPI (Serial Peripheral Interface) clock Input.
6	CS	SPI Chip Select	SPI (Serial Peripheral Interface) chip select input pin. $\overline{CS}$ is active low.
7	ADOUT0	Analog Output Pin 0	Analog Multiplexer Output.
8	PWMIN	PWM Input	High-side and Low-side Pulse Width Modulation Input.
9	RST	Internal Reset I/O	Bidirectional Reset I/O pin - driven low when any internal reset source is asserted. $\overline{RST}$ is active low.

Table 2. 33912 pin definitions (continued)

Pin	Pin name	Formal name	Definition
10	IRQ	Internal Interrupt Output	Interrupt output pin, indicating wake-up events from Stop mode or events from Normal and Normal request modes. IRQ is active low.
11	ADOUT1	Analog Output Pin 1	Current sense analog output.
12	WDCONF	Watchdog Configuration Pin	This input pin is for configuration of the watchdog period and allows the disabling of the watchdog.
13	LIN	LIN Bus	This pin represents the single-wire bus transmitter and receiver.
14	LGND	LIN Ground Pin	This pin is the device LIN ground connection. It is internally connected to the PGND pin.
15 16	ISENSEL ISENSEH	Current Sense Pins	Current Sense differential inputs.
17 19	LS2 LS1	Low-side Outputs	Relay drivers low-side outputs.
18	PGND	Power Ground Pin	This pin is the device low-side ground connection. It is internally connected to the LGND pin.
20 21 22 23	L4 L3 L2 L1	Wake-up Inputs	These pins are the wake-up capable digital inputs[2]. In addition, all Lx inputs can be sensed analog via the analog multiplexer.
24 25	HS2 HS1	High-side Outputs	High-side switch outputs.
26 27	VS2 VS1	Power Supply Pin	These pins are device battery level power supply pins. VS2 is supplying the HSx drivers while VS1 supplies the remaining blocks.[3]
28	NC	Not Connected	This pin can be left open or connected to any potential ground or power supply.
29	VSENSE	Voltage Sense Pin	Battery voltage sense input.[4]
30	HVDD	Hall Sensor Supply Output	+5.0 V switchable supply output pin.[5]
31	VDD	Voltage Regulator Output	+5.0 V main voltage regulator output pin.[6]
32	AGND	Analog Ground Pin	This pin is the device analog ground connection.

Notes

2. When used as digital input, a series 33 kΩ resistor must be used to protect against automotive transients.
3. Reverse battery protection series diodes must be used externally to protect the internal circuitry.
4. This pin can be connected directly to the battery line for voltage measurements. The pin is self protected against reverse battery connections. It is strongly recommended to connect a 10 kΩ resistor in series with this pin for protection purposes.
5. External capacitor (1.0 µF < C < 10 µF; 0.1 Ω < ESR < 5.0 Ω) required.
6. External capacitor (2.0 µF < C < 100 µF; 0.1 Ω < ESR < 10 Ω) required.

5 Electrical characteristics

5.1 Maximum ratings

Table 3. Maximum ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
Electrical ratings				
$V_{SUP(SS)}$ $V_{SUP(PK)}$	Supply Voltage at VS1 and VS2 • Normal Operation (DC) • Transient Conditions (load dump)	 -0.3 to 27 -0.3 to 40	V	
V_{DD}	Supply Voltage at VDD	-0.3 to 5.5	V	
V_{IN} $V_{IN(IRQ)}$	Input / Output Pins Voltage • $\overline{CS}$, $\overline{RST}$, SCLK, PWMIN, ADOUT0, ADOUT1, MOSI, MISO, TXD, RXD, HVDD • Interrupt Pin ($\overline{IRQ}$)	-0.3 to V_{DD} +0.3 -0.3 to 11	V	(7) (8)
V_{HS}	HS1 and HS2 Pin Voltage (DC)	-0.3 to V_{SUP} +0.3	V	
V_{LS}	LS1 and LS2 Pin Voltage (DC)	-0.3 to 45	V	
V_{LxDC} V_{LxTR}	L1, L2, L3 and L4 Pin Voltage • Normal Operation with a series 33 k resistor (DC) • Transient input voltage with external component (according to ISO7637-2) (See Figure 5, page 19)	-18 to 40 ±100	V	
V_{ISENSE}	ISENSEH and ISENSEL Pin Voltage (DC)	-0.3 to 40	V	
V_{VSENSE}	VSENSE Pin Voltage (DC)	-27 to 40	V	
V_{BUSDC} V_{BUSTR}	LIN Pin Voltage • Normal Operation (DC) • Transient input voltage with external component (according to ISO7637-2) (See Figure 4, page 19)	-18 to 40 -150 to 100	V	
I_{VDD}	VDD output current	Internally Limited	A	

Notes

7. Exceeding voltage limits on specified pins may cause a malfunction or permanent damage to the device.
8. Extended voltage range for programming purpose only.

Table 3. Maximum ratings (continued)

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
	ESD Capability • AECQ100 • Human Body Model - JESD22/A114 (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω)			
V_{ESD1-1} V_{ESD1-2} V_{ESD1-3}	• LIN Pin • L1, L2, L3, and L4 • all other Pins	±8.0k ±6.0k ±2000		
	• Charge Device Model - JESD22/C101 (C_{ZAP} = 4.0 pF)			
V_{ESD2-1} V_{ESD2-2}	• Corner Pins (Pins 1, 8, 9, 16, 17, 24, 25 and 32) • All other Pins (Pins 2-7, 10-15, 18-23, 26-31)	±750 ±500		
	• According to LIN Conformance Test Specification / LIN EMC Test Specification, August 2004 (C_{ZAP} = 150 pF, R_{ZAP} = 330 Ω)		V	
	• Contact Discharge, Unpowered			
V_{ESD3-1} V_{ESD3-2} V_{ESD3-3} V_{ESD3-4}	• LIN pin with 220 pF • LIN pin without capacitor • VS1/VS2 (100 nF to ground) • Lx inputs (33 kΩ serial resistor)	±20k ±11k >±12k ±6000		
	• According to IEC 61000-4-2 (C_{ZAP} = 150 pF, R_{ZAP} = 330 Ω)			
	• Unpowered			
V_{ESD4-1} V_{ESD4-2} V_{ESD4-3}	• LIN pin with 220 pF and without capacitor • VS1/VS2 (100 nF to ground) • Lx inputs (33 kΩ serial resistor)	±8000 ±8000 ±8000		
Thermal ratings				
T_A	Operating Ambient Temperature 33912 34912	 -40 to 125 -40 to 85	°C	(9)
T_J	Operating Junction Temperature	-40 to 150	°C	
T_{STG}	Storage Temperature	-55 to 150	°C	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient Natural Convection, Single Layer board (1s) Natural Convection, Four Layer board (2s2p)	 85 56	°C/W	 (9), (10) (9), (11)
$R_{\theta JC}$	Thermal Resistance, Junction to Case	23	°C/W	(12)
T_{PPRT}	Peak Package Reflow Temperature During Reflow	Note 14	°C	(13), (14)

Notes

9. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
10. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
11. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
12. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
13. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
14. NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), go to www.NXP.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

5.2 Static electrical characteristics

Table 4. Static electrical characteristics

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33912 and -40 °C ≤ T_A ≤ 85 °C for the 34912, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Supply voltage range (VS1, VS2)						
V_{SUP}	Nominal Operating Voltage	5.5	–	18	V	
V_{SUPOP}	Functional Operating Voltage	–	–	27	V	(15)
V_{SUPLD}	Load Dump	–	–	40	V	
Supply current range (V_{SUP} = 13.5 V)						
I_{RUN}	Normal Mode (I_{OUT} at V_{DD} = 10 mA), LIN Recessive State	–	4.5	10	mA	(16)
I_{STOP}	Stop Mode, VDD ON with I_{OUT} = 100 µA, LIN Recessive State • 5.5 V < V_{SUP} < 12 V • V_{SUP} = 13.5 V • 13.5 V < V_{SUP} < 18 V	 – – –	 47 62 180	 80 90 400	µA	(16), (17), (18), (19)
I_{SLEEP}	Sleep Mode, VDD OFF, LIN Recessive State • 5.5 V < V_{SUP} < 12 V • V_{SUP} = 13.5 V • 13.5 V ≤ V_{SUP} < 18 V	 – – –	 27 33 160	 35 48 300	µA	(16), (18)
I_{CYCLIC}	Cyclic Sense Supply Current Adder	–	10	–	µA	(20)
Supply under/overvoltage detections						
$V_{BATFAIL}$ $V_{BATFAIL\_HYS}$	Power-On Reset (BATFAIL) • Threshold (measured on VS1) • Hysteresis (measured on VS1)	 1.5 –	 3.0 0.9	 3.9 –	V	(21), (20)
V_{SUV} V_{SUV_HYS}	V_{SUP} Undervoltage Detection (VSUV Flag) (Normal and Normal Request Modes, Interrupt Generated) • Threshold (measured on VS1) • Hysteresis (measured on VS1)	 5.55 –	 6.0 0.2	 6.6 –	V	
V_{SOV} V_{SOV_HYS}	V_{SUP} Overvoltage Detection (VSOV Flag) (Normal and Normal Request Modes, Interrupt Generated) • Threshold (measured on VS1) • Hysteresis (measured on VS1)	 18 –	 19.25 1.0	 20.5 –	V	

Notes

15. Device is fully functional. All features are operating.
16. Total current (I_{VS1} + I_{VS2}) measured at GND pins excluding all loads, cyclic sense disabled.
17. Total I_{DD} current (including loads) below 100 µA.
18. Stop and Sleep Modes current increases if V_{SUP} exceeds13.5 V.
19. This parameter is guaranteed after 90 ms.
20. This parameter is guaranteed by process monitoring but not production tested.
21. The Flag is set during power up sequence. To clear the flag, a SPI read must be performed.

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33912 and -40 °C ≤ T_A ≤ 85 °C for the 34912, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Voltage regulator (22) (VDD)						
V_{DDRUN}	Normal Mode Output Voltage • 1.0 mA < I_{VDD} < 50 mA; 5.5 V < V_{SUP} < 27 V	4.75	5.00	5.25	V	
I_{VDDRUN}	Normal Mode Output Current Limitation	60	110	200	mA	
V_{DDDROP}	Dropout Voltage • I_{VDD} = 50 mA	–	0.1	0.25	V	(23)
V_{DDSTOP}	Stop Mode Output Voltage • I_{VDD} < 5.0 mA	4.75	5.0	5.25	V	
$I_{VDDSTOP}$	Stop Mode Output Current Limitation	6.0	13	36	mA	
LR_{RUN} LR_{STOP}	Line Regulation • Normal Mode, 5.5 V < V_{SUP} < 18 V; I_{VDD} = 10 mA • Stop Mode, 5.5 V < V_{SUP} < 18 V; I_{VDD} = 1.0 mA	– –	– –	25 25	mV	
LD_{RUN} LD_{STOP}	Load Regulation • Normal Mode, 1.0 mA < I_{VDD} < 50 mA • Stop Mode, 0.1 mA < I_{VDD} < 5.0 mA	– –	– –	80 50	mV	
T_{PRE}	Overtemperature Prewarning (Junction) • Interrupt generated, VDDOT Bit Set	90	115	140	°C	(24)
T_{PRE_HYS}	Overtemperature Prewarning Hysteresis	–	13	–	°C	(24)
T_{SD}	Overtemperature Shutdown Temperature (Junction)	150	170	190	°C	(24)
T_{SD_HYS}	Overtemperature Shutdown Hysteresis	–	13	–	°C	(24)
Hall sensor supply output (25) (HVDD)						
H_{VDDACC}	V_{DD} Voltage matching H_{VDDACC} = (HVDD-VDD) / VDD * 100% • I_{HVDD} = 15 mA	-2.0	–	2.0	%	
I_{HVDD}	Current Limitation	20	35	50	mA	
$H_{VDDDROP}$	Dropout Voltage • I_{HVDD} = 15 mA; I_{VDD} = 5.0 mA	–	160	300	mV	
LR_{HVDD}	Line Regulation • I_{HVDD} = 5.0 mA; I_{VDD} = 5.0 mA	–	–	40	mV	
LD_{HVDD}	Load Regulation • 1.0 mA > I_{HVDD} > 15 mA; I_{VDD} = 5.0 mA	–	–	20	mV	

Notes

22. Specification with external capacitor 2.0 µF < C < 100 µF and 100 mΩ ≤ ESR ≤ 10 Ω.
23. Measured when voltage has dropped 250 mV below its nominal Value (5.0 V).
24. This parameter is guaranteed by process monitoring but not production tested.
25. Specification with external capacitor 1.0 µF < C < 10 µF and 100 mΩ ≤ ESR ≤ 10 Ω.

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33912 and -40 °C ≤ T_A ≤ 85 °C for the 34912, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
$\overline{RST}$ input/output pin ($\overline{RST}$)						
$V_{\overline{RST}TH}$	VDD Low Voltage Reset Threshold	4.3	4.5	4.7	V	
V_{OL}	Low-state Output Voltage • I_{OUT} = 1.5 mA; 3.5 V ≤ V_{SUP} ≤ 27 V	0.0	–	0.9	V	
I_{OH}	High-state Output Current (0 V < V_{OUT} < 3.5 V)	-150	-250	-350	µA	
I_{PD_MAX}	Pull-down Current Limitation (internally limited) V_{OUT} = V_{DD}	1.5	–	8.0	mA	
V_{IL}	Low-state Input Voltage	-0.3	–	0.3 x V_{DD}	V	
V_{IH}	High-state Input Voltage	0.7 x V_{DD}	–	V_{DD} +0.3	V	
MISO SPI output pin (MISO)						
V_{OL}	Low-state Output Voltage • I_{OUT} = 1.5 mA	0.0	–	1.0	V	
V_{OH}	High-state Output Voltage • I_{OUT} = -250 µA	V_{DD} -0.9	–	V_{DD}	V	
$I_{TRIMISO}$	Tri-state Leakage Current • 0 V ≤ V_{MISO} ≤ V_{DD}	-10	–	10	µA	
SPI input pins (MOSI, SCLK, $\overline{CS}$)						
V_{IL}	Low-state Input Voltage	-0.3	–	0.3 x V_{DD}	V	
V_{IH}	High-state Input Voltage	0.7 x V_{DD}	–	V_{DD} +0.3	V	
I_{IN}	MOSI, SCLK Input Current • 0 V ≤ V_{IN} ≤ V_{DD}	-10	–	10	µA	
$I_{PU\overline{CS}}$	$\overline{CS}$ Pull-up Current • 0 V < V_{IN} < 3.5 V	10	20	30	µA	
Interrupt output pin ($\overline{IRQ}$)						
V_{OL}	Low-state Output Voltage • I_{OUT} = 1.5 mA	0.0	–	0.8	V	
V_{OH}	High-state Output Voltage • I_{OUT} = -250 µA	V_{DD} -0.8	–	V_{DD}	V	
I_{OUT}	Leakage Current • V_{DD} ≤ V_{OUT} ≤ 10 V	–	–	2.0	mA	
Pulse width modulation input pin (PWMIN)						
V_{IL}	Low-state Input Voltage	-0.3	–	0.3 x V_{DD}	V	
V_{IH}	High-state Input Voltage	0.7 x V_{DD}	–	V_{DD} +0.3	V	
$I_{PUPWMIN}$	Pull-up current • 0 V < V_{IN} < 3.5 V	10	20	30	µA	

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33912 and -40 °C ≤ T_A ≤ 85 °C for the 34912, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
High-side outputs HS1 and HS2 Pins (HS1, HS2)						
$R_{DS(on)}$	Output Drain-to-Source On Resistance • T_J = 25 °C, I_{LOAD} = 50 mA; V_{SUP} > 9.0 V • T_J = 150 °C, I_{LOAD} = 50 mA; V_{SUP} > 9.0 V • T_J = 150 °C, I_{LOAD} = 30 mA; 5.5 V < V_{SUP} < 9.0 V	– – –	– – –	7.0 10 14	Ω	(26)
I_{LIMHSX}	Output Current Limitation • 0 V < V_{OUT} < V_{SUP} - 2.0 V	60	90	250	mA	(27)
I_{OLHSX}	Open Load Current Detection	–	5.0	7.5	mA	(28)
I_{LEAK}	Leakage Current • -0.2 V < V_{HSX} < V_{S2} + 0.2 V	–	–	10	µA	
V_{THSC}	Short-circuit Detection Threshold • 5.5 V < V_{SUP} < 27 V	V_{SUP} -2.0	–	–	V	(29)
T_{HSSD}	Overtemperature Shutdown	140	160	180	°C	(30), (34)
T_{HSSD_HYS}	Overtemperature Shutdown Hysteresis	–	10	–	°C	(34)
Low-side outputs LS1 and LS2 Pins (LS1, LS2)						
$R_{DS(on)}$	Output Drain-to-Source On Resistance • T_J = 25 °C, I_{LOAD} = 150 mA, V_{SUP} > 9.0 V • T_J = 125 °C, I_{LOAD} = 150 mA, V_{SUP} > 9.0 V • T_J = 125 °C, I_{LOAD} = 120 mA, 5.5 V < V_{SUP} < 9.0 V	– – –	– – –	2.5 4.5 10	Ω	
I_{LIMLSX}	Output Current Limitation • 2.0 V < V_{OUT} < V_{SUP}	160	275	350	mA	(31)
I_{OLLSX}	Open Load Current Detection	–	7.5	12	mA	(32)
I_{LEAK}	Leakage Current • -0.2 V < V_{OUT} < VS1	–	–	10	µA	
V_{CLAMP}	Active Output Energy Clamp • I_{OUT} = 150 mA	V_{SUP} +2.0	–	V_{SUP} +5.0	V	
V_{THSC}	Short-circuit Detection Threshold • 5.5 V < V_{SUP} < 27 V	2.0	–	–	V	(29)
T_{LSSD}	Overtemperature Shutdown	140	160	180	°C	(33), (34)
T_{LSSD_HYS}	Overtemperature Shutdown Hysteresis	–	10	–	°C	

Notes

26. This parameter is production tested up to T_A = 125 °C, and guaranteed by process monitoring up to T_J = 150 °C.
27. When overcurrent occurs, the corresponding high-side stays ON with limited current capability and the HSxCL flag is set in the HSSR.
28. When open load occurs, the flag (HSxOP) is set in the HSSR.
29. HS and LS automatically shutdown if HSOT or LSOT occurs or if the HVSE flag is enabled and an overvoltage occurs.
30. When overtemperature shutdown occurs, both high-sides are turned off. All flags in HSSR are set.
31. When overcurrent occurs, the corresponding low-side stays ON with limited current capability and the LSxCL flag is set in the LSSR.
32. When open load occurs, the flag (LSxOP) is set in the LSSR.
33. When overtemperature shutdown occurs, both low-sides are turned off. All flags in LSSR are set.
34. Guaranteed by characterization but not production tested

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33912 and -40 °C ≤ T_A ≤ 85 °C for the 34912, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
L1, L2, L3 and L4 input pins (L1, L2, L3, L4)						
V_{THL}	Low Detection Threshold • 5.5 V < V_{SUP} < 27 V	2.0	2.5	3.0	V	(35)
V_{THH}	High Detection Threshold • 5.5 V < V_{SUP} < 27 V	3.0	3.5	4.0	V	(35)
V_{HYS}	Hysteresis • 5.5 V < V_{SUP} < 27 V	0.4	0.8	1.4	V	(35)
I_{IN}	Input Current • -0.2 V < V_{IN} < VS1	-10	–	10	µA	(36)
R_{LXIN}	Analog Input Impedance	800	1300	2000	kΩ	(37)
$RATIO_{LX}$	Analog Input Divider Ratio ($RATIO_{Lx}$ = V_{Lx} / V_{ADOUT0}) • LXDS (Lx Divider Select) = 0 • LXDS (Lx Divider Select) = 1	 0.95 3.42	 1.0 3.6	 1.05 3.78		
$V_{RATIOLx-OFFSET}$	Analog Output offset Ratio • LXDS (Lx Divider Select) = 0 • LXDS (Lx Divider Select) = 1	 -80 -22	 6.0 2.0	 80 22	mV	
$LX_{MATCHING}$	Analog Inputs Matching • LXDS (Lx Divider Select) = 0 • LXDS (Lx Divider Select) = 1	 96 96	 100 100	 104 104	%	
Window watchdog configuration pin (WDCONF)(38)						
R_{EXT}	External Resistor Range	20	–	200	kΩ	
WD_{ACC}	Watchdog Period Accuracy with External Resistor (Excluding Resistor Accuracy)	-15	–	15	%	(39)
Analog multiplexer						
V_{ADOUT0_TEMP}	Temperature Sense Analog Output Voltage • T_A = -40 °C • T_A = 25 °C • T_A = 125 °C	 2.0 2.8 3.6	 - 3.0 -	 2.8 3.6 4.6	V	
V_{ADOUT0_25}	Temperature Sense Analog Output Voltage per characterization • T_A = 25 °C	3.1	3.15	3.2	V	(40)
S_{TTOV}	Internal Chip Temperature Sense Gain	9.0	10.5	12	mV/K	
S_{TTOV_3T}	Internal Chip Temperature Sense Gain per characterization at 3 temperatures. See Figure 16, Temperature sense gain	9.9	10.2	10.5	mV/K	(40)
$RATIO_{VSENSE}$	VSENSE Input Divider Ratio ($RATIO_{VSENSE}$ = V_{VSENSE} / V_{ADOUT0}) • 5.5 V < V_{SUP} < 27 V	5.0	5.25	5.5		
$RATIO_{VSENSECZ}$	VSENSE Input Divider Ratio (RATIOVSENSE=V_{SENSE}/V_{ADOUT0}) per characterization • 5.5 <V_{SUP}< 27 V	5.15	5.25	5.35		(40)

Notes

35. The unused Lx pins must be connected to ground.
36. Analog multiplexer input disconnected from Lx input pin.
37. Analog multiplexer input connected to Lx input pin.
38. For V_{SUP} 4.7 V to 18 V
39. Watchdog timing period calculation formula: t_{PWD} [ms] = [0.466 * (R_{EXT} - 20)] + 10 with (R_{EXT} in kΩ)
40. These limits have been defined after laboratory characterization on 3 lots and 30 samples. These tighten limits could not be guaranteed by production test.

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33912 and -40 °C ≤ T_A ≤ 85 °C for the 34912, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Analog multiplexer (continued)						
$OFFSET_{VSENSE}$	VSENSE Output Related Offset	-30	-10	30	mV	
$OFFSET_{VSENSE\_CZ}$	V_{SENSE} Output Related Offset per characterization	-30	-12.6	0	mV	(41)
Analog outputs (ADOUT0 and ADOUT1)						
V_{OUT_MAX}	Maximum Output Voltage • -5.0 mA < I_O < 5.0 mA	V_{DD} -0.35	–	V_{DD}	V	
V_{OUT_MIN}	Minimum Output Voltage • -5.0 mA < I_O < 5.0 mA	0.0	–	0.35	V	
Current sense amplifier (ISENSEH, ISENSEL)						
G	Gain • CSGS (Current Sense Gain Select) = 0 • CSGS (Current Sense Gain Select) = 1	 29 14	 30 14.5	 31 15		
DIFF	Differential Input Impedance • CSGS (Current Sense Gain Select) = 0 • CSGS (Current Sense Gain Select) = 1	 2.0 5.0	 10 20	 30 50	kΩ	
CM	Common Mode Input Impedance • CSGS (Current Sense Gain Select) = 0 • CSGS (Current Sense Gain Select) = 1	 100 100	 – –	 200 200	kΩ	
V_{IN}	ISENSEH, ISENSEL Input Voltage Range	-0.2	–	3.0	V	
V_{IN_OFFSET}	Input Offset Voltage • CSAZ (Current Sense Auto Zero) = 0 • CSAZ (Current Sense Auto Zero) = 1	 -15 -2.0	 – –	 15 2.0	mV	
RxD output pin (LIN physical layer) (RxD)						
V_{OL}	Low-state Output Voltage • I_{OUT} = 1.5 mA	0.0	–	0.8	V	
V_{OH}	High-state Output Voltage • I_{OUT} = -250 µA	V_{DD} -0.8	–	V_{DD}	V	
TXD input pin (LIN physical layer) (TXD)						
V_{IL}	Low-state Input Voltage	-0.3	–	0.3 x V_{DD}	V	
V_{IH}	High-state Input Voltage	0.7 x V_{DD}	–	V_{DD} +0.3	V	
I_{PUIN}	Pin Pull-up Current, 0 V < V_{IN} < 3.5 V	10	20	30	µA	
LIN physical layer with J2602 feature enabled (bit DIS_J2602 = 0)						
$V_{TH\_UNDER\_VOLTAGE}$	LIN Undervoltage threshold • Positive and Negative threshold (V_{THP}, V_{THN})	5.0	-	6.0	V	
V_{J2602_DEG}	Hysteresis (V_{THP} - V_{THN})	-	400	-	mV	

Notes

41. These limits have been defined after laboratory characterization on 3 lots and 30 samples. These tighten limits could not be guaranteed by production test.

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33912 and -40 °C ≤ T_A ≤ 85 °C for the 34912, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
LIN physical layer, transceiver (LIN)(42)						
V_{BAT}	Operating Voltage Range	8.0	-	18	V	
V_{SUP}	Supply Voltage Range	7.0	-	18	V	
$V_{SUP\_NON\_OP}$	Voltage Range within which the device is not destroyed	-0.3	-	40	V	
I_{BUS_LIM}	Current Limitation for Driver Dominant State • Driver ON, V_{BUS} = 18 V	40	90	200	mA	
$I_{BUS\_PAS\_DOM}$	Input Leakage Current at the receiver • Driver off; V_{BUS} = 0 V; V_{BAT} = 12 V	-1.0	–	–	mA	
$I_{BUS\_PAS\_REC}$	Leakage Output Current to GND • Driver Off; 8.0 V < V_{BAT} < 18 V; 8.0 V < V_{BUS} < 18 V; V_{BUS} ≥ V_{BAT}	–	–	20	µA	
$I_{BUS\_NO\_GND}$	Control unit disconnected from ground • GND_{DEVICE} = V_{SUP}; V_{BAT} = 12 V; 0 < V_{BUS} < 18 V	-1.0	–	1.0	mA	(43)
I_{BUSNO_BAT}	V_{BAT} Disconnected; V_{SUP_DEVICE} = GND; 0 V < V_{BUS} < 18 V	–	–	100	µA	(44)
V_{BUSDOM}	Receiver Dominant State	–	–	0.4	V_{SUP}	
V_{BUSREC}	Receiver Recessive State	0.6	–	–	V_{SUP}	
V_{BUS_CNT}	Receiver Threshold Center • (V_{TH_DOM} + V_{TH_REC})/2	0.475	0.5	0.525	V_{SUP}	
V_{HYS}	Receiver Threshold Hysteresis • (V_{TH_REC} - V_{TH_DOM})	–	–	0.175	V_{SUP}	
$V_{SERDIODE}$	Voltage Drop at the serial Diode in pull-up path	0.4		1.0	V	
V_{SHIFT_BAT}	VBAT_SHIFT	0		11.5%	V_{BAT}	
V_{SHIFT_GND}	GND_SHIFT	0		11.5%	V_{BAT}	
V_{BUSWU}	LIN Wake-up threshold from Stop or Sleep mode		5.3	5.8	V	(45)
R_{SLAVE}	LIN Pull-up Resistor to V_{SUP}	20	30	60	kΩ	
T_{LINSD}	Overtemperature Shutdown	140	160	180	°C	(46)
T_{LINSD_HYS}	Overtemperature Shutdown Hysteresis	–	10	–	°C	

Notes

42. Parameters guaranteed for 7.0 V ≤ V_{SUP} ≤ 18 V.
43. Loss of local ground must not affect communication in the residual network.
44. Node has to sustain the current which can flow under this condition. Bus must remain operational under this condition.
45. This parameter is 100% tested on an Automatic Tester. However, since it has not been monitored during reliability stresses, NXP does not guarantee this parameter during the product's life time.
46. When overtemperature shutdown occurs, the LIN bus goes in recessive state and the flag LINOT in LINSR is set.

5.3 Dynamic electrical characteristics

Table 5. Dynamic electrical characteristics

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33912 and -40 °C ≤ T_A ≤ 85 °C for the 34912, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
SPI interface timing (see Figure 13, page 22)						
f_{SPIOP}	SPI Operating Frequency	–	–	4.0	MHz	
t_{PSCLK}	SCLK Clock Period	250	–	N/A	ns	
t_{WSCLKH}	SCLK Clock High Time	110	–	N/A	ns	(47)
t_{WSCLKL}	SCLK Clock Low Time	110	–	N/A	ns	(47)
t_{LEAD}	Falling Edge of $\overline{CS}$ to Rising Edge of SCLK	100	–	N/A	ns	(47)
t_{LAG}	Falling Edge of SCLK to $\overline{CS}$ Rising Edge	100	–	N/A	ns	(47)
t_{SISU}	MOSI to Falling Edge of SCLK	40	–	N/A	ns	(47)
t_{SIH}	Falling Edge of SCLK to MOSI	40	–	N/A	ns	(47)
t_{RSO}	MISO Rise Time • C_L = 220 pF	–	40	–	ns	(47)
t_{FSO}	MISO Fall Time • C_L = 220 pF	–	40	–	ns	(47)
t_{SOEN} t_{SODIS}	Time from Falling or Rising Edges of $\overline{CS}$ to: - MISO Low-impedance - MISO High-impedance	 0.0 0.0	 – –	 50 50	ns	(47)
t_{VALID}	Time from Rising Edge of SCLK to MISO Data Valid • 0.2 x V_{DD} ≤ MISO ≥ 0.8 x V_{DD}, C_L = 100 pF	0.0	–	75	ns	(47)
$\overline{RST}$ output pin						
$t_{\overline{RST}}$	Reset Low-level Duration After V_{DD} High (see Figure 12, page 22)	0.65	1.0	1.35	ms	
$t_{\overline{RSTDF}}$	Reset Deglitch Filter Time	350	480	900	ns	
Window watchdog configuration pin (WDCONF)						
t_{PWD}	Watchdog Time Period • External Resistor R_{EXT} = 20 kΩ (1%) • External Resistor R_{EXT} = 200 kΩ (1%) • Without External Resistor R_{EXT} (WDCONF Pin Open)	 8.5 79 110	 10 94 150	 11.5 108 205	ms	(48)
Current sense amplifier(47)						
CMR	Common Mode Rejection Ratio	70	–	–	dB	
SVR	Supply Voltage Rejection Ratio	60	–	–	dB	(49)
GBP	Gain Bandwidth Product	0.75	3.0	–	MHz	
SR	Output Slew-Rate	0.5	–	–	V/µs	

Notes

47. This parameter is guaranteed by process monitoring but not production tested.
48. Watchdog timing period calculation formula: t_{PWD} [ms] = [0.466 * (R_{EXT} - 20)] + 10 with (R_{EXT} in kΩ)
49. Analog Outputs are supplied by V_{DD} and from 100 Hz to 4.0 kHz

Table 5. Dynamic electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33912 and -40 °C ≤ T_A ≤ 85 °C for the 34912, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
L1, L2, L3 and L4 inputs						
t_{WUF}	Lx Filter Time Deglitcher	8.0	20	38	µs	(50)
State machine timing						
t_{STOP}	Delay Between $\overline{CS}$ LOW-to-HIGH Transition (at End of SPI Stop Command) and Stop Mode Activation	–	–	5.0	µs	(50)
t_{NRTOUT}	Normal Request Mode Timeout (see Figure 12, page 22)	110	150	205	ms	
T_{ON}	Cyclic Sense ON Time from Stop and Sleep mode	130	200	270	µs	(51)
	Cyclic Sense Accuracy	-35		+35	%	(50)
t_{S-ON}	Delay Between the SPI Command and HS/LS Turn On • 9.0 V < V_{SUP} < 27 V	–	–	10	µs	(52)
t_{S-OFF}	Delay Between the SPI Command and HS/LS Turn Off • 9.0 V < V_{SUP} < 27 V	–	–	10	µs	(52)
t_{SNR2N}	Delay Between Normal Request and Normal mode After a Watchdog Trigger Command (Normal Request Mode)	–	–	10	µs	(50)
$t_{WU\overline{CS}}$ t_{WUSPI}	Delay Between $\overline{CS}$ Wake-up ($\overline{CS}$ LOW to HIGH) in Stop mode and: • Normal Request mode, VDD ON and $\overline{RST}$ HIGH • First Accepted SPI Command	9.0 90	15 —	80 N/A	µs	
$t_{2\overline{CS}}$	Minimum Time Between Rising and Falling Edge on the $\overline{CS}$	4.0	—	—	µs	
J2602 deglitcher						
t_{J2602_DEG}	V_{SUP} Deglitcher • (DIS_J2602 = 0)	35	50	70	µs	(53)
LIN physical layer: driver characteristics for normal slew rate - 20.0 kbit/sec according to lin physical layer specification (54), (55)						
D1	Duty Cycle 1: • $TH_{REC(MAX)}$ = 0.744 * V_{SUP} • $TH_{DOM(MAX)}$ = 0.581 * V_{SUP} • D1 = $t_{BUS\_REC(MIN)}$/(2 x t_{BIT}), t_{BIT} = 50 µs, 7.0 V ≤ V_{SUP} ≤ 18 V	0.396	—	—		
D2	Duty Cycle 2: • $TH_{REC(MIN)}$ = 0.422 * V_{SUP} • $TH_{DOM(MIN)}$ = 0.284 * V_{SUP} • D2 = $t_{BUS\_REC(MAX)}$/(2 x t_{BIT}), t_{BIT} = 50 µs, 7.6 V ≤ V_{SUP} ≤ 18 V	—	—	0.581		

Notes

50. This parameter is guaranteed by process monitoring but not production tested.
51. This parameter is 100% tested on an Automatic Tester. However, since it has not been monitored during reliability stresses, NXP does not guarantee this parameter during the product's life time.
52. Delay between turn on or off command (rising edge on $\overline{CS}$) and HS or LS ON or OFF, excluding rise or fall time due to external load.
53. This parameter has not been monitoring during operating life test.
54. Bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 kΩ, 6.8 nF / 660 Ω, 10 nF / 500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter.
55. See Figure 7, page 20.

Table 5. Dynamic electrical characteristics (continued)

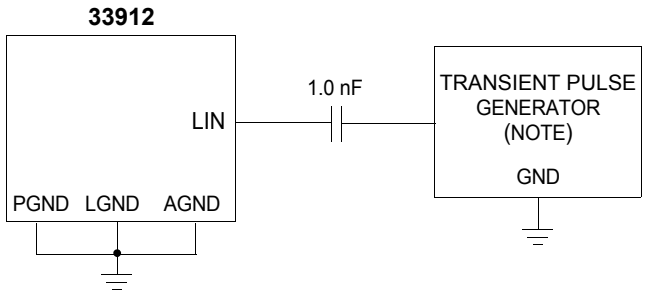
Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33912 and -40 °C ≤ T_A ≤ 85 °C for the 34912, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
LIN physical layer: driver characteristics for slow slew rate - 10.4 kbit/sec according to lin physical layer specification [56], [57]						
D3	Duty Cycle 3: • $TH_{REC(MAX)}$ = 0.778 * V_{SUP} • $TH_{DOM(MAX)}$ = 0.616 * V_{SUP} • D3 = $t_{BUS\_REC(MIN)}$/(2 x t_{BIT}), t_{BIT} = 96 µs, 7.0 V ≤ V_{SUP} ≤ 18 V	0.417	—	—		
D4	Duty Cycle 4: • $TH_{REC(MIN)}$ = 0.389 * V_{SUP} • $TH_{DOM(MIN)}$ = 0.251 * V_{SUP} • D4 = $t_{BUS\_REC(MAX)}$/(2 x t_{BIT}), t_{BIT} = 96 µs, 7.6 V ≤ V_{SUP} ≤ 18 V	—	—	0.590		
LIN physical layer: driver characteristics for fast slew rate						
SR_{FAST}	LIN Fast Slew Rate (Programming mode)	—	20	—	V/µs	
LIN physical layer: characteristics and wake-up timings [58]						
t_{REC_PD} t_{REC_SYM}	Propagation Delay and Symmetry • Propagation Delay of Receiver, t_{REC_PD} = MAX (t_{REC_PDR}, t_{REC_PDF}) • Symmetry of Receiver Propagation Delay, t_{REC_PDF} - t_{REC_PDR}	— -2.0	4.2 —	6.0 2.0	µs	[59]
t_{PROPWL}	Bus Wake-up Deglitcher (Sleep and Stop modes)	42	70	95	µs	[60], [64] [61]
t_{WAKE_SLEEP} t_{WAKE_STOP}	Bus Wake-Up Event Reported • From Sleep Mode • From Stop Mode	— 9.0	— 27	1500 35	µs	[62] [63]
t_{TXDDOM}	TXD Permanent Dominant State Delay	0.65	1.0	1.35	s	
Pulse width modulation input pin (PWMIN)						
f_{PWMIN}	PWMIN pin • Max. frequency to drive HS and LS output pins	-	10	-	kHz	[64]

Notes

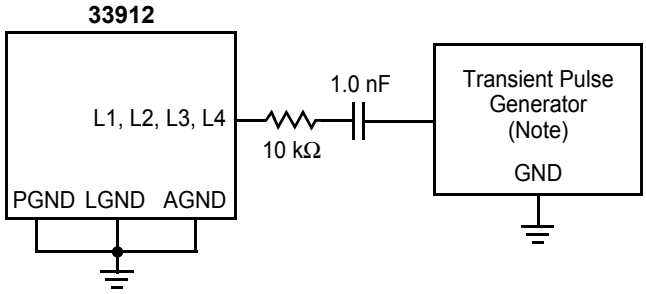
56. Bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 kΩ, 6.8 nF / 660 Ω, 10 nF / 500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 6, page 20.
57. See Figure 8, page 20.
58. V_{SUP} from 7.0 to 18 V, bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 kΩ, 6.8 nF / 660 Ω, 10 nF / 500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 6, page 20.
59. See Figure 9, page 21
60. See Figure 10, page 21 for Sleep and Figure 11, page 21 for Stop mode.
61. This parameter is tested on automatic tester but has not been monitoring during operating life test.
62. The measurement is done with 1.0 µF capacitor and 0mA current load on V_{DD}. The value takes into account the delay to charge the capacitor. The delay is measured between the bus wake-up threshold (V_{BUSWU}) rising edge of the LIN bus and when V_{DD} reaches 3.0 V. See Figure 10, page 21. The delay depends of the load and capacitor on V_{DD}.
63. In Stop mode, the delay is measured between the bus wake-up threshold (V_{BUSWU}) and the falling edge of the $\overline{IRQ}$ pin. See Figure 11, page 21.
64. This parameter is guaranteed by process monitoring but not production tested.

5.4 Timing diagrams



Note Waveform per ISO 7637-2. Test Pulses 1, 2, 3a, 3b.

Figure 4. Test circuit for transient test pulses (LIN)



Note Waveform per ISO 7637-2. Test Pulses 1, 2, 3a, 3b,.

Figure 5. Test circuit for transient test pulses (Lx)

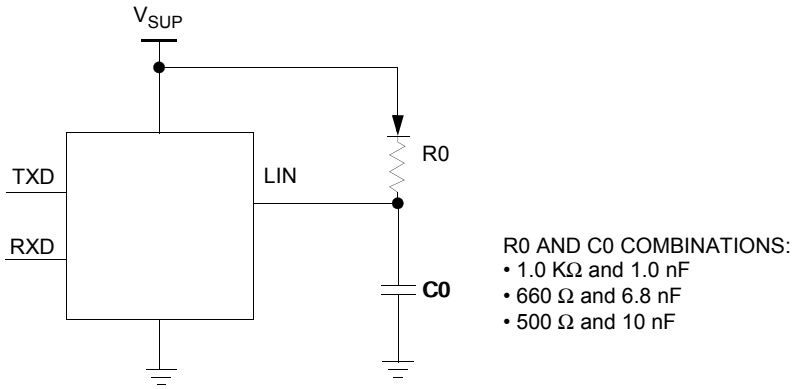


Figure 6. Test circuit for LIN timing measurements

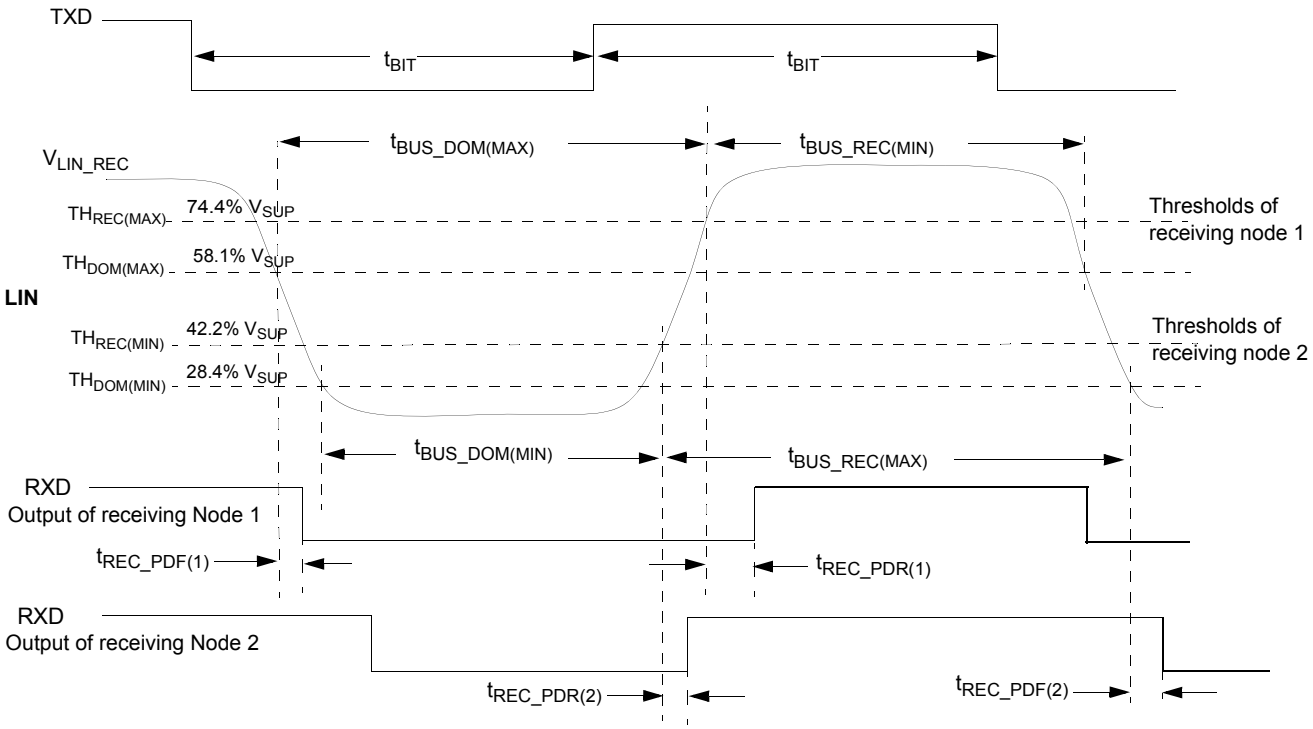


Figure 7. LIN timing measurements for normal slew rate

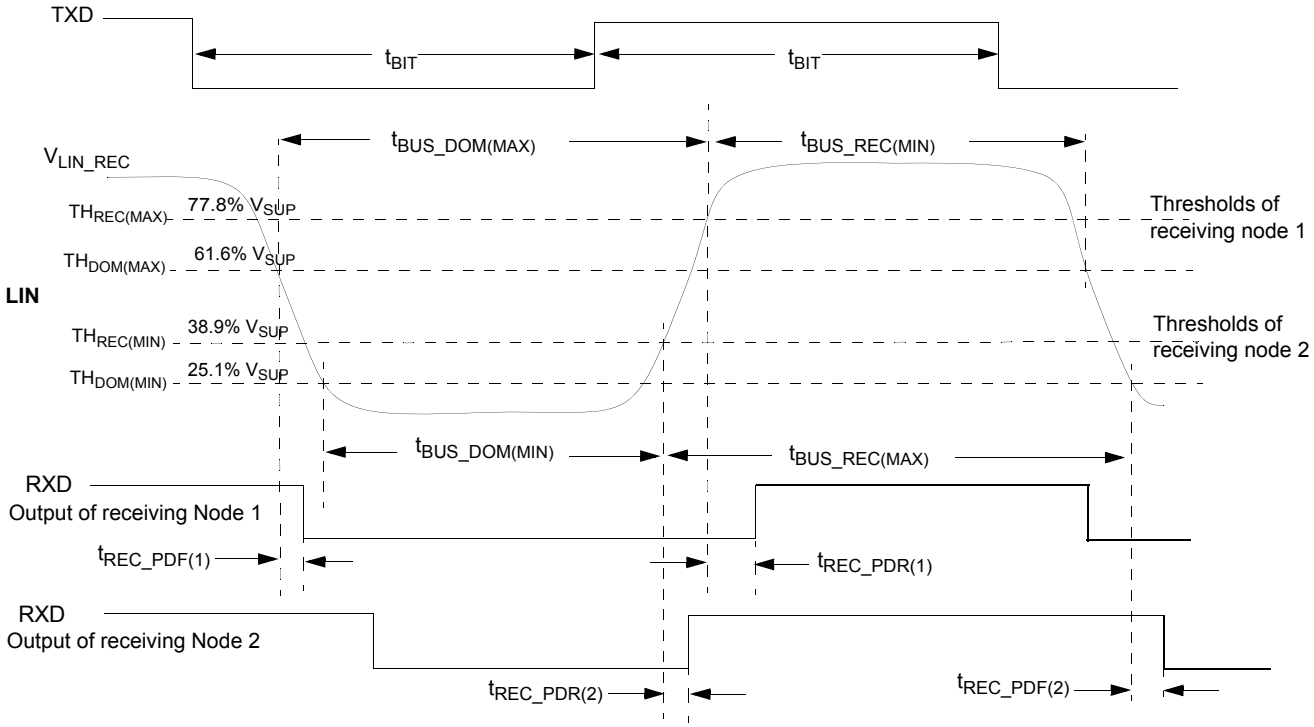


Figure 8. LIN timing measurements for slow slew rate

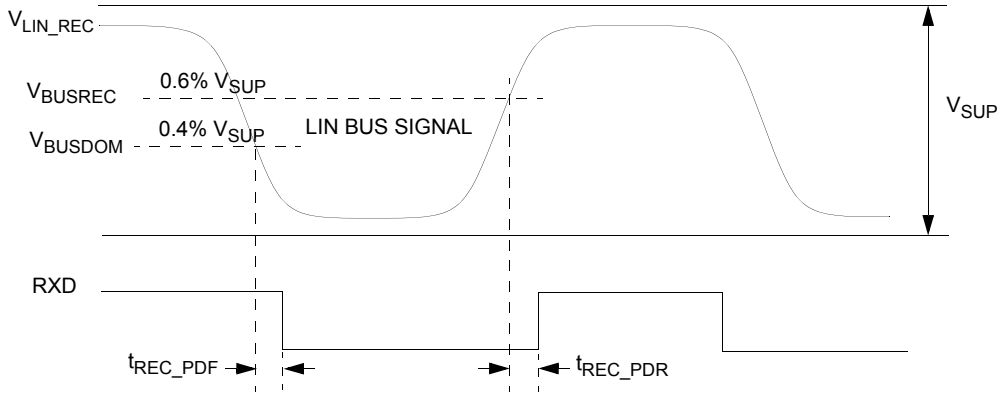


Figure 9. LIN receiver timing

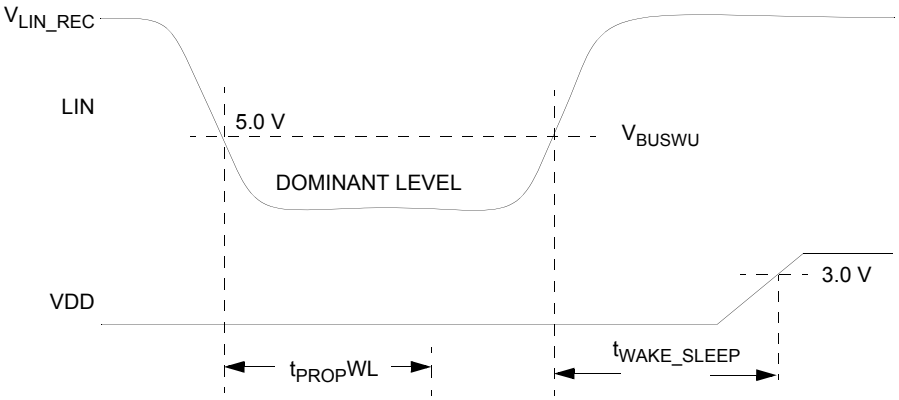


Figure 10. LIN wake-up sleep mode timing

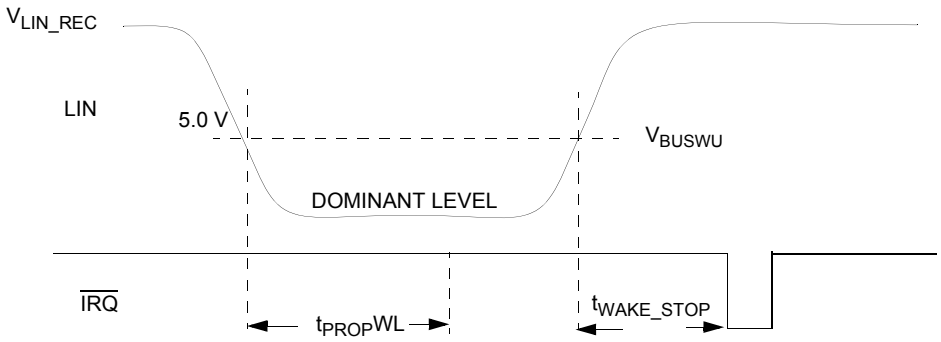


Figure 11. LIN wake-up stop mode timing

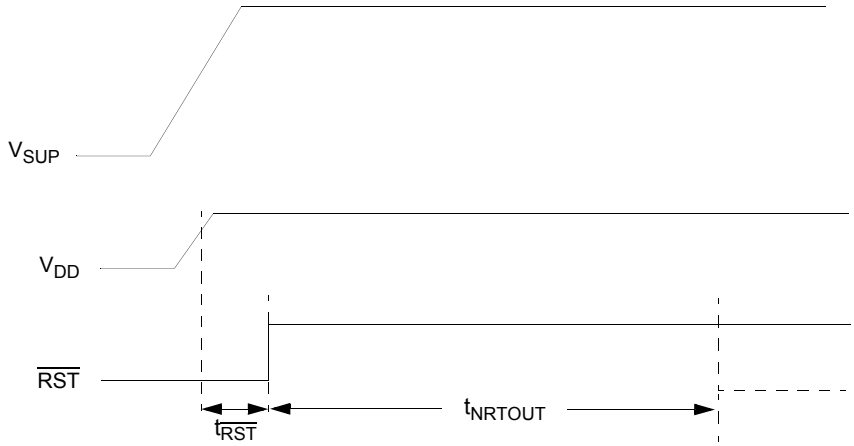


Figure 12. Power on reset and normal request timeout timing

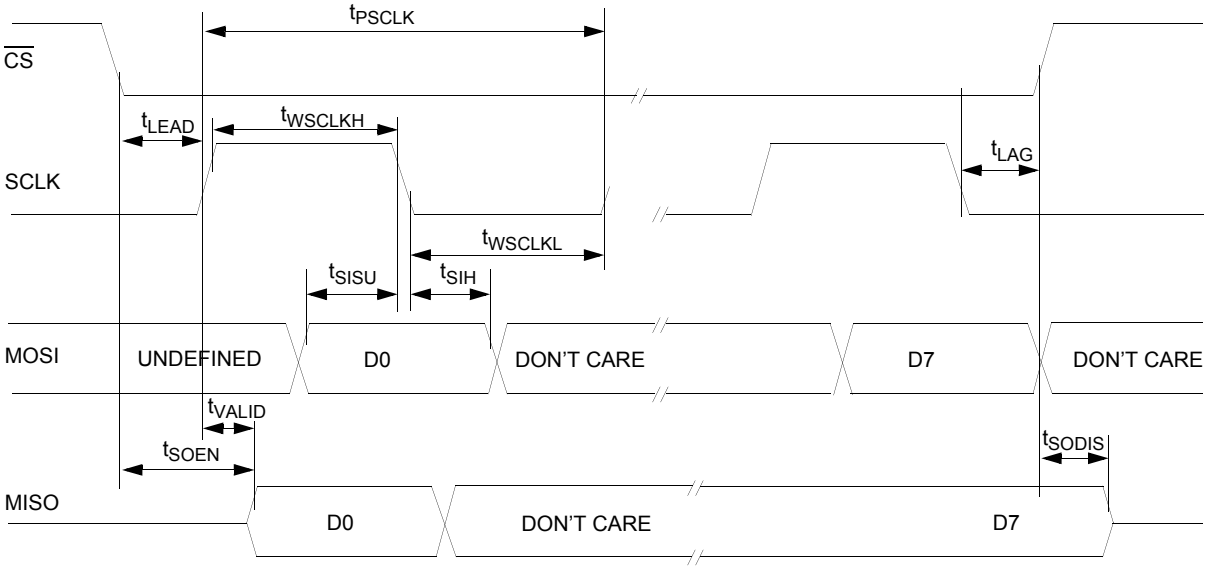


Figure 13. SPI timing characteristics

6 Functional description

6.1 Introduction

The 33912 was designed and developed as a highly integrated and cost-effective solution for automotive and industrial applications. For automotive body electronics, the 33912 is well suited to perform relay control in applications such as a window lift, sunroof, etc. via the LIN bus. Power switches are provided on the device configured as high-side and low-side outputs. Other ports are also provided, which include a current and voltage sense port, a Hall Sensor port supply, and four wake-up capable pins. An internal voltage regulator provides power to a MCU device.

Also included in this device is a LIN physical layer, which communicates using a single wire. This enables this device to be compatible with 3-wire bus systems, where one wire is used for communication, one for battery, and one for ground.

6.2 Functional pin description

See Figure 1, 33912 simplified application diagram, page 1, for a graphic representation of the various pins referred to in the following paragraphs. Also, see the pin diagram on page 5 for a description of the pin locations in the package.

6.2.1 Receiver output pin (RXD)

The RXD pin is a digital output. It is the receiver output of the LIN interface and reports the state of the bus voltage: RXD Low when LIN bus is dominant, RXD High when LIN bus is recessive.

6.2.2 Transmitter input pin (TXD)

The TXD pin is a digital input. It is the transmitter input of the LIN interface and controls the state of the bus output (dominant when TXD is Low, recessive when TXD is High). This pin has an internal pull-up to force recessive state in case the input is left floating.

6.2.3 Lin bus pin (LIN)

The LIN pin represents the single-wire bus transmitter and receiver. It is suited for automotive bus systems and is compliant to the LIN bus specification 2.0, 2.1, and SAE J2602-2. The LIN interface is only active during Normal Mode. See Table 6, Operating modes overview.

6.2.4 Serial data clock pin (SCLK)

The SCLK pin is the SPI clock input. MISO data changes on the positive transition of the SCLK. MOSI is sampled on the negative edge of the SCLK.

6.2.5 Master out slave in pin (MOSI)

The MOSI digital pin receives SPI data from the MCU. This data input is sampled on the negative edge of SCLK.

6.2.6 Master in slave out pin (MISO)

The MISO pin sends data to a SPI-enabled MCU. It is a digital tri-state output used to shift serial data to the microcontroller. Data on this output pin changes on the positive edge of the SCLK. When $\overline{CS}$ is High, this pin remains in the high-impedance state.

6.2.7 Chip select pin ($\overline{CS}$)

$\overline{CS}$ is an active low digital input. It must remain low during a valid SPI communication and allow for several devices to be connected in the same SPI bus without contention. A rising edge on $\overline{CS}$ signals the end of the transmission and the moment the data shifted in is latched. A valid transmission must consist of 8 bits only. While in STOP mode, a low-to-high level transition on this pin generates a wake-up condition for the 33912.

6.2.8 Analog multiplexer pin (ADOUT0)

The ADOUT0 pin can be configured via the SPI to allow the MCU A/D converter to read the several inputs of the Analog Multiplexer, including the VSENSE, L1, L2, L3, L4 input voltages, and the internal junction temperature.

6.2.9 Current sense amplifier pin (ADOUT1)

The ADOUT1 pin is an analog interface to the MCU A/D converter. It allows the MCU to read the output of the current sense amplifier.

6.2.10 PWM input control pin (PWMIN)

This digital input can control the high-sides and low-sides drivers in Normal Request and Normal mode. To enable PWM control, the MCU must perform a write operation to the High-side Control register (HSCR) or the Low-side Control register (LSCR). This pin has an internal 20 μA current pull-up.

6.2.11 Reset pin ($\overline{\text{RST}}$)

This bidirectional pin is used to reset the MCU in case the 33912 detects a reset condition, or to inform the 33912 the MCU has just been reset. After release of the $\overline{\text{RST}}$ pin, Normal Request mode is entered.

The $\overline{\text{RST}}$ pin is an active low filtered input and output formed by a weak pull-up and a switchable pull-down structure which allows this pin to be shorted either to V_{DD} or to GND during software development, without the risk of destroying the driver.

6.2.12 Interrupt pin ($\overline{\text{IRQ}}$)

The $\overline{\text{IRQ}}$ pin is a digital output used to signal events or faults to the MCU while in Normal and Normal Request mode or to signal a wake-up from Stop mode. This active low output transitions to high only after the interrupt is acknowledged by a SPI read of the respective status bits.

6.2.13 Watchdog configuration pin (WDCONF)

The WDCONF pin is the configuration pin for the internal watchdog. A resistor can be connected to this pin to configure the window watchdog period. When connected directly to ground, the watchdog is disabled. When this pin is left open, the watchdog period is fixed to its lower precision internal default value (150 ms typical).

6.2.14 Ground connection pins (AGND, PGND, LGND)

The AGND, PGND, and LGND pins are the Analog and Power ground pins. The AGND pin is the ground reference of the voltage regulator and the current sense module. The PGND and LGND pins are used for high current load return as in the relay-drivers and LIN interface pin.

Note: PGND, AGND, And LGND pins must be connected together.

6.2.15 Current sense amplifier input pins (ISENSEH and ISENSEL)

The ISENSEH and ISENSEL pins are the input pins of a ground compatible differential amplifier designed to be used to sense the voltage drop over a shunt resistor. The main purpose of this amplifier is to implement accurate current sensors. The gain of the differential amplifier can be set by the SPI.

6.2.16 Low-side pins (LS1 and LS2)

LS1 and LS2 are the low-side driver outputs. Those outputs are short-circuit protected and include active clamp circuitry to drive inductive loads. Due to the energy clamp voltage on this pin, it can raise above the battery level when switched off. The switches are controlled through the SPI and can be configured to respond to a signal applied to the PWMIN input pin. Both low-side switches are protected against overheating. In case of VS1 disconnection and the low-sides are still supplied by V_{BAT} through a load, both low-sides has a VDS voltage equal to the clamping value, as stated in the specification.

6.2.17 Digital/analog pins (L1, L2, L3, and L4)

The Lx pins are multi purpose inputs. They can be used as digital inputs, which can be sampled by reading the SPI and used for wake-up when 33912 is in Low-power mode or used as analog inputs for the analog multiplexer. When used to sense voltage outside the module, a 33 kΩ series resistor must be used on each input.

When used as wake-up inputs L1-L4 can be configured to operate in cyclic-sense mode. In this mode one or both of the high-side switches are configured to be periodically turned on and sample the wake-up inputs. If a state change is detected between two cycles a wake-up is initiated. The 33912 can also wake-up from Stop or Sleep by a simple state change on L1-L4.

When used as analog inputs, the voltage present on the Lx pins is scaled down by an selectable internal voltage divider and can be routed to the ADOUT0 output through the analog multiplexer. When an Lx input is not selected in the analog multiplexer, the voltage divider is disconnected from this input.

Note: If an Lx input is selected in the analog multiplexer, it is disabled as a digital input and remains disabled in Low-power mode. No wake-up feature is available in this condition.

6.2.18 High-side output pins (HS1 and HS2)

These two high-side switches are able to drive loads such as relays or lamps. Their structures are connected to the VS2 supply pin. The pins are short-circuit protected and both outputs are also protected against overheating. HS1 and HS2 are controlled by the SPI and can respond to a signal applied to the PWMIN input pin. HS1 and HS2 outputs can also be used during low-power mode for the cyclic-sense of the wake inputs.

6.2.19 Power supply pins (VS1 and VS2)

Those are the battery level voltage supply pins. In an application, VS1 and VS2 pins must be protected against reverse battery connection and negative transient voltages with external components. These pins sustain standard automotive voltage conditions such as a load dump at 40 V. The high-side switches (HS1 and HS2) are supplied by the VS2 pin. All other internal blocks are supplied by the VS1 pin.

6.2.20 Voltage sense pin (VSENSE)

This input can be connected directly to the battery line. It is protected against battery reverse connection. The voltage present in this input is scaled down by an internal voltage divider, and can be routed to the ADOUT0 output pin and used by the MCU to read the battery voltage. The ESD structure on this pin allows for excursion up to +40 V and down to -27 V, allowing this pin to be connected directly to the battery line. It is strongly recommended to connect a 10 kΩ resistor in series with this pin for protection purposes.

6.2.21 Hall sensor switchable supply pin (HVDD)

This pin provides a switchable supply for external hall sensors. While in Normal mode, this current limited output can be controlled through the SPI. The HVDD pin needs to be connected to an external capacitor to stabilize the regulated output voltage.

6.2.22 +5.0 V main regulator output pin (VDD)

An external capacitor has to be placed on the VDD pin to stabilize the regulated output voltage. The VDD pin is intended to supply a microcontroller. The pin is current limited against shorts to GND and overtemperature protected. During Stop mode, the voltage regulator does not operate with its full drive capabilities and the output current is limited. During Sleep mode, the regulator output is completely shutdown.

7 Functional device operations

7.1 Operational modes

7.1.1 Introduction

The 33912 offers three main operating modes: Normal (Run), Stop, and Sleep (Low-power). In Normal mode, the device is active and is operating under normal application conditions. The Stop and Sleep modes are low power modes with wake-up capabilities.

In Stop mode, the voltage regulator still supplies the MCU with V_{DD} (limited current capability), while in Sleep mode the voltage regulator is turned off (V_{DD} = 0 V). Wake-up from Stop mode is initiated by a wake-up interrupt. Wake-up from Sleep mode is done by a reset and the voltage regulator is turned back on.

The selection of the different modes is controlled by the MOD1:2 bits in the Mode Control register (MCR). Figure 14 describes how transitions are done between the different operating modes. Table 6, 28, gives an overview of the operating modes.

7.1.2 Reset mode

The 33912 enters the Reset mode after a power up. In this mode, the $\overline{RST}$ pin is low for 1.0 ms (typical value). After this delay, it enters the Normal Request mode and the $\overline{RST}$ pin is driven high. The Reset mode is entered if a reset condition occurs (V_{DD} low, watchdog trigger fail, after wake-up from Sleep mode, Normal Request mode timeout occurs).

7.1.3 Normal request mode

This is a temporary mode automatically accessed by the device after the Reset mode, or after a wake-up from Stop mode. In Normal Request mode, the VDD regulator is ON, the RESET pin is High, and the LIN is operating in RX Only mode.

As soon as the device enters in the Normal Request mode an internal timer is started for 150 ms (typical value). During these 150 ms, the MCU must configure the Timing Control register (TIMCR) and the Mode Control register (MCR) with MOD2 and MOD1 bits set = 0, to enter the Normal mode. If within the 150 ms timeout, the MCU does not command the 33912 to Normal mode, it enters in Reset mode. If the WDCONF pin is grounded in order to disable the watchdog function, it goes directly in Normal mode after the Reset mode.

7.1.4 Normal mode

In Normal mode, all 33912 functions are active and can be controlled by the SPI interface and the PWMIN pin. The VDD regulator is ON and delivers its full current capability. If an external resistor is connected between the WDCONF pin and the Ground, the window watchdog function is enabled. The wake-up inputs (L1-L4) can be read as digital inputs or have its voltage routed through the analog-multiplexer.

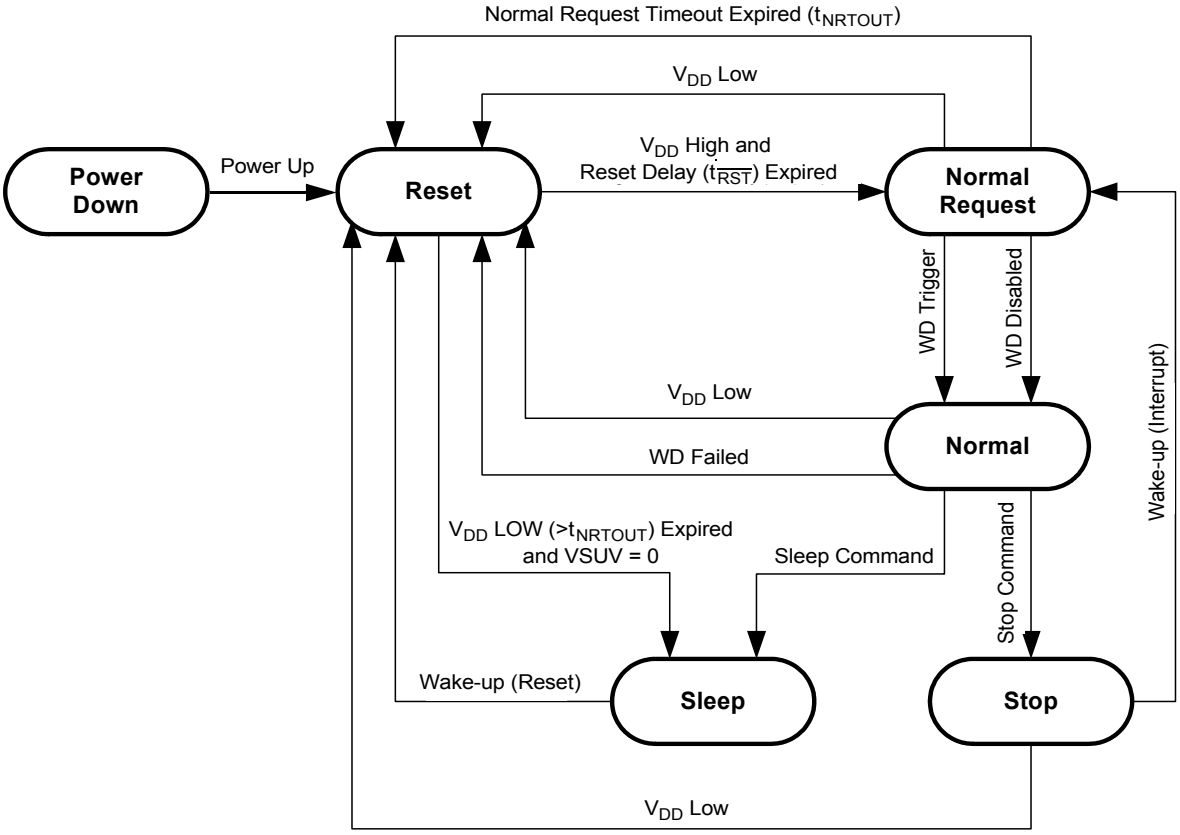
The LIN interface has slew rate and timing compatible with the LIN protocol specification 2.0, 2.1 and SAEJ2602. The LIN bus can transmit and receive information. The high-side and low-side switches are active and have PWM capability according to the SPI configuration. The interrupts are generated to report failures for V_{SUP} over/undervoltage, thermal shutdown, or thermal shutdown prewarning on the main regulator.

7.1.5 Sleep mode

The Sleep mode is a low power mode. From Normal mode, the device enters into Sleep mode by sending one SPI command through the Mode Control register (MCR), or (V_{DD} low > 150 ms) with V_{SUV} = 0. When in Reset mode, a V_{DD} undervoltage condition with no V_{SUP} undervoltage (V_{SUV} = 0) sends the device to Sleep mode. All blocks are in their lowest power consumption condition. Only some wake-up sources (wake-up inputs with or without cyclic sense, forced wake-up and LIN receiver) are active. The 5.0 V regulator is OFF. The internal low-power oscillator may be active if the IC is configured for cyclic-sense. In this condition, one of the high-side switches is turned on periodically and the wake-up inputs are sampled. Wake-up from Sleep mode is similar to a power-up. The device goes in Reset mode except the SPI reports the wake-up source and the BATFAIL flag is not set.

7.1.6 Stop mode

The Stop mode is the second Low-power mode, but in this case the 5.0 V regulator is ON with limited current drive capability. The application MCU is always supplied while the 33912 is operating in Stop mode. The device can enter into Stop mode only by sending the SPI command. When the application is in this mode, it can wake-up from the 33912 side (for example: cyclic sense, force wake-up, LIN bus, wake inputs) or the MCU side ($\overline{CS}$, $\overline{RST}$ pins). Wake-up from Stop mode transitions the 33912 to Normal Request mode and generates an interrupt except if the wake-up event is a low to high transition on the $\overline{CS}$ pin or comes from the $\overline{RST}$ pin.



Legend
WD: Watchdog
WD Disabled: Watchdog disabled (WDCONF pin connected to GND)
WD Trigger: Watchdog is triggered by a SPI command
WD Failed: No watchdog trigger or trigger occurs in closed window
Stop Command: Stop command sent via the SPI
Sleep Command: Sleep command sent via the SPI
Wake-up from Stop Mode: L1, L2, L3 or L4 state change, LIN bus wake-up, Periodic wake-up, $\overline{CS}$ rising edge wake-up or $\overline{RST}$ wake-up.
Wake-up from Sleep Mode: L1, L2, L3 or L4 state change, LIN bus wake-up, Periodic wake-up.

Figure 14. Operating modes and transitions

Table 6. Operating modes overview

Function	Reset mode	Normal request mode	Normal mode	Stop mode	Sleep mode
VDD	Full	Full	Full	Stop	-
HVDD	-	SPI[65]	SPI	-	-
LSx	-	SPI/PWM[66]	SPI/PWM	-	-
HSx	-	SPI/PWM[66]	SPI/PWM	Note[67]	Note[68]
Analog Mux	-	SPI	SPI	-	-
Lx	-	Inputs	Inputs	Wake-up	Wake-up
Current Sense	On	On	On	-	-
LIN	-	Rx-Only	Full/Rx-Only	Rx-Only/Wake-up	Wake-up
Watchdog	-	150 ms (typ.) timeout	On[69]/Off	-	-
Voltage Monitoring	V_{SUP}/V_{DD}	V_{SUP}/V_{DD}	V_{SUP}/V_{DD}	V_{DD}	-

Notes
65. Operation can be enabled/controlled by the SPI.
66. Operation can be controlled by the PWMIN input.
67. HSx switches can be configured for cyclic sense operation in Stop mode.
68. HSx switches can be configured for cyclic sense operation in Sleep mode.
69. Windowing operation when enabled by an external resistor.

7.1.7 Interrupts

Interrupts are used to signal a microcontroller peripheral needs to be serviced. The interrupts which can be generated, change according to the operating mode. While in Normal and Normal Request modes, the 33912 signals through interrupts special conditions which may require a MCU software action. Interrupts are not generated until all pending wake-up sources are read in the Interrupt Source register (ISR).

While in Stop mode, interrupts are used to signal wake-up events. Sleep mode does not use interrupts. Wake-up is performed by powering-up the MCU. In Normal and Normal Request mode the wake-up source can be read by the SPI. The interrupts are signaled to the MCU by a low logic level of the $\overline{IRQ}$ pin, which remains low until the interrupt is acknowledged by a SPI read command of the ISR register. The $\overline{IRQ}$ pin is then be driven high.

Interrupts are only asserted while in Normal, Normal Request and Stop mode. Interrupts are not generated while the $\overline{RST}$ pin is low. The following is a list of the interrupt sources in Normal and Normal Request modes. Some of these can be masked by writing to the SPI - Interrupt Mask register (IMR).

7.1.7.1 Low-voltage interrupt

Signals when the supply line (VS1) voltage drops below the VSUV threshold (V_{SUV}).

7.1.7.2 High-voltage interrupt

Signals when the supply line (VS1) voltage increases above the VSOV threshold (V_{SOV}).

7.1.7.3 Overtemperature prewarning

Signals when the 33912 temperature has reached the pre-shutdown warning threshold. It is used to warn the MCU an overtemperature shutdown in the main 5.0 V regulator is imminent.

7.1.7.4 LIN overtemperature shutdown / TXD stuck at dominant / RXD short-circuit

These signal fault conditions within the LIN interface causes the LIN driver to be disabled. In order to restart the operation, the fault must be removed and TXD must go recessive.

7.1.7.5 High-side overtemperature shutdown

Signals a shutdown in the high-side outputs.

7.1.7.6 Low-side overtemperature shutdown

Signals a shutdown in the low-side outputs.

7.1.8 Reset

To reset a MCU the 33912 drives the $\overline{RST}$ pin low for the time the reset condition lasts. After the reset source is removed, the state machine drives the $\overline{RST}$ output low for at least 1.0 ms (typical value) before driving it high. In the 33912, four main reset sources exist:

7.1.8.1 5.0 V regulator low-voltage reset ($V_{\overline{RSTTH}}$)

The 5.0 V regulator output V_{DD} is continuously monitored against brown outs. If the supply monitor detects the voltage at the VDD pin has dropped below the reset threshold $V_{\overline{RSTTH}}$, the 33912 issues a reset. In case of overtemperature, the voltage regulator is disabled and the voltage monitoring issues a VDDOT Flag independently of the V_{DD} voltage.

7.1.8.2 Window watchdog overflow

If the watchdog counter is not properly serviced while its window is open, the 33912 detects an MCU software run-away and resets the microcontroller.

7.1.8.3 Wake-up from sleep mode

During Sleep mode, the 5.0 V regulator is not active, hence all wake-up requests from Sleep mode require a power-up/reset sequence.

7.1.8.4 External reset

The 33912 has a bidirectional reset pin which drives the device to a safe state (same as Reset mode) for as long as this pin is held low. The $\overline{RST}$ pin must be held low long enough to pass the internal glitch filter and get recognized by the internal reset circuit. This functionality is also active in Stop mode. After the $\overline{RST}$ pin is released, there is no extra $t_{\overline{RST}}$ to be considered.

7.1.9 Wake-up capabilities

Once entered into one of the Low-power modes (Sleep or Stop) only wake-up sources can bring the device into Normal mode operation.

In Stop mode, a wake-up is signaled to the MCU as an interrupt, while in Sleep mode the wake-up is performed by activating the 5.0 V regulator and resetting the MCU. In both cases the MCU can detect the wake-up source by accessing the SPI registers and reading the Interrupt Source register. There is no specific SPI register bits to signal a $\overline{CS}$ wake-up or external reset. If necessary this condition is detected by excluding all other possible wake-up sources.

7.1.9.1 Wake-up from wake-up inputs (L1-L4) with cyclic sense disabled

The wake-up lines are dedicated to sense state changes of external switches and wake-up the MCU (in Sleep or Stop mode). In order to select and activate direct wake-up from Lx inputs, the Wake-up Control register (WUCR) must be configured with appropriate LxWE inputs enabled or disabled. The wake-up input's state is read through the Wake-up Status register (WUSR). Lx inputs are also used to perform cyclic-sense wake-up.

Note: Selecting an Lx input in the analog multiplexer before entering Low-power mode disables the wake-up capability of the Lx input

7.1.9.2 Wake-up from wake-up inputs (L1-L4) with cyclic sense timer enabled

The SBCLIN can wake-up at the end of a cyclic sense period if on one of the four wake-up input lines (L1-L4) a state change occurs. One or both HSx switch can be activated in Sleep or Stop modes from an internal timer. Cyclic sense and force wake-up are exclusive. If cyclic sense is enabled, the force wake-up can not be enabled. In order to select and activate the cyclic sense wake-up from Lx inputs, before entering in low power modes (Stop or Sleep modes), the following SPI set-up has to be performed:

In WUCR: select the Lx input to WU-enable.

In HSCR: enable the desired HSx.

- In TIMCR: select the CS/$\overline{WD}$ bit and determine the cyclic sense period with CYSTx bits.
- Perform Goto Sleep/Stop command.

7.1.9.3 Forced wake-up

The 33912 can wake-up automatically after a predetermined time spent in Sleep or Stop mode. Cyclic sense and Forced wake-up are exclusive. If Forced wake-up is enabled, the Cyclic Sense can not be enabled.

To determine the wake-up period, the following SPI set-up has to be sent before entering in low power modes:

- In TIMCR: select the CS/$\overline{WD}$ bit and determine the low power mode period with CYSTx bits.
- In HSCR: all HSx bits must be disabled.

7.1.9.4 $\overline{CS}$ wake-up

While in Stop mode, a rising edge on the $\overline{CS}$ causes a wake-up. The $\overline{CS}$ wake-up does not generate an interrupt, and is not reported in the SPI.

7.1.9.5 LIN wake-up

While in the low-power mode, the 33912 monitors the activity on the LIN bus. A dominant pulse larger than t_{PROPWL} followed by a dominant to recessive transition causes a LIN wake-up. This behavior protects the system from a short to ground bus condition. The bit RXONLY = 1 from LINCR register disables the LIN wake-up from Stop mode.

7.1.9.6 $\overline{RST}$ wake-up

While in Stop mode, the 33912 can wake-up when the $\overline{RST}$ pin is held low long enough to pass the internal glitch filter. The 33912 changes to Normal Request or Normal modes depending on the WDCONF pin configuration. The $\overline{RST}$ wake-up does not generate an interrupt and is not reported via the SPI.

From Stop mode, the following wake-up events can be configured:

- Wake-up from Lx inputs without cyclic sense
- Cyclic sense wake-up inputs
- Force wake-up
- $\overline{CS}$ wake-up
- LIN wake-up
- $\overline{RST}$ wake-up

From Sleep mode, the following wake-up events can be configured:

- Wake-up from Lx inputs without cyclic sense
- Cyclic sense wake-up inputs
- Force wake-up
- Lin wake-up

7.1.10 Window watchdog

The 33912 includes a configurable window watchdog which is active in Normal mode. The watchdog can be configured by an external resistor connected to the WDCONF pin. The resistor is used to achieve higher precision in the timebase used for the watchdog. SPI clears are performed by writing through the SPI in the MOD bits of the Mode Control register (MCR).

During the first half of the SPI timeout, watchdog clears are not allowed, but after the first half of the SPI timeout window, the clear operation opens. If a clear operation is performed outside the window, the 33912 resets the MCU, in the same way as when the watchdog overflows.

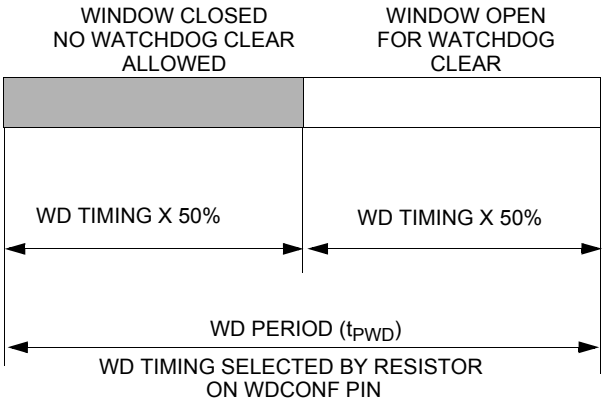


Figure 15. Window watchdog operation

To disable the watchdog function in Normal mode the user must connect the WDCONF pin to ground. This measure effectively disables Normal Request mode. The WDOFF bit in the Watchdog Status register (WDSR) is set. This condition is only detected during Reset mode.

If neither a resistor nor a connection to ground is detected, the watchdog falls back to the internal lower precision timebase of 150 ms (typ.) and signals the faulty condition through the Watchdog Status register (WDSR).

The watchdog timebase can be further divided by a prescaler which can be configured by the Timing Control register (TIMCR). During Normal Request mode, the window watchdog is not active but there is a 150 ms (typ.) timeout for leaving the Normal Request mode. In case of a timeout, the 33912 enters into Reset mode, resetting the microcontroller before entering again into Normal Request mode.

7.1.11 Faults detection management

The 33912 has the capability to detect faults like an over or undervoltage on VS1, TxD in permanent Dominant State, overtemperature on HS, LIN. It is able to take corrective actions accordingly. Most of faults are monitoring through SPI and the Interrupt pin. The microcontroller can also take actions. Table 7 summarizes all fault sources the device is able to detect with associated conditions. The status for a device recovery and the SPI or pins monitoring are also described.

Table 7. Fault detection management conditions

Block	Fault	Mode	Condition	Fallout	Recovery	Monitoring(71)	
						REG (Flag, Bit)	Interrupt
Power Supply	Battery Fail	All modes	V_{SUP}<3.0 V (typ) then power-up	-	Condition gone	VSR (BATFAIL, 0)	-
	V_{SUP} Overvoltage	Normal, Normal Request	V_{SUP} > 19.25 V (typ)	In Normal mode, HS and LS shutdown if bit HVSE=1 (reg MCR)	Condition gone, to re-enable HS or LS write to HSCR or LSCR registers	VSR (VSOV,3)	IRQ low + ISR (0101) (72)
	V_{SUP} Undervoltage		V_{SUP} < 6.0 V (typ)	-	Condition gone	VSR (VSUV,2)	IRQ low + ISR (0101)
	V_{DD} Undervoltage	All except Sleep	V_{DD} < 4.5 V (typ)	Reset (70)		-	-
	V_{DD} Overtemp Prewarning	All except Low Power modes	Temperature > 115 °C (typ)	-		VSR (VDDOT,1)	IRQ low + ISR (0101)
	V_{DD} Overtemperature		Temperature > 170 °C (typ)	VDD shutdown, Reset then Sleep		-	-
LIN	Rxd Pin Short-Circuit	Normal, Normal Request	RXD pin shorted to GND or 5.0 V	LIN trans shutdown	LIN transmitter re-enabled once the condition is gone and TXD is high	LINSR, (RXSHORT,3)	IRQ low + ISR (0100)(72)
	Txd Pin Permanent Dominant		TXD pin low for more than 1.0 s (typ)	LIN transmitter shutdown		LINSR (TXDOM,2)	
	Lin Driver Overtemperature		Temperature > 160 °C (typ)			LINSR (LINOT,1)	

Table 7. Fault detection management conditions

Block	Fault	Mode	Condition	Fallout	Recovery	Monitoring[71]	
						REG (Flag, Bit)	Interrupt
High-side	High-side Drivers Overtemperature	Normal, Normal Request	Temperature > 160 °C (typ)	Both HS thermal shutdown	Condition gone, to re-enable HS write to HSCR reg	All flags in HSSR are set	IRQ low + ISR (0010) [72]
	Hs1 Open Load Detection		Current through HSx < 5.0 mA (typ)	-	Condition gone	HSSR (HS1OP,1)	-
	Hs2 Open Load Detection					HSSR (HS2OP,3)	
	Hs1 Overcurrent		Current through HSx tends to rise above the current limit 60 mA (min)	HSx on with limited current capability 60 mA (min)		HSSR (HS1CL,0)	
	Hs2 Overcurrent					HSSR (HS2CL,2)	
Low-side	Low-side Drivers Overtemperature	Normal, Normal Request	Temperature > 160 °C (typ)	Both LS thermal shutdown	Condition gone, to re-enable LS write to LSCR reg	All flags in LSSR are set	IRQ low + ISR (0011) [72]
	Ls1 Open Load		Current through LSx < 7.5 mA (typ)	-	-	LSSR (LS1OP,1)	-
	Ls2 Open Load					LSSR (LS2OP,3)	
	Ls1 Overcurrent		Current through LSx tends to rise above the current limit 160 mA (min)	LSx on with limited current capability 160 mA (min)		LSSR (LS1CL,0)	
	Ls2 Overcurrent					LSSR (LS2CL,2)	
Watchdog	Normal Request Timeout Expired	Normal Request	The MCU did not command the device to Normal mode within the 150 ms timeout after reset	Reset	-	-	-
	Watchdog Timeout	Normal	WD timeout or WD clear within the window closed	Reset		WDSR (WDTO, 3)	
	Watchdog Error	Normal	WDCONF pin is floating	WD internal lower precision timebase 150 ms (typ)	Connect WDCONF to a resistor or to GND	WDSR (WDERR, 2)	

Notes

70. When in Reset mode a V_{DD} undervoltage condition combined with no V_{SUP} undervoltage (VSUV=0) sends the device to Sleep mode.
71. Registers to be read when back in Normal Request or Normal mode depending on the fault. Interrupts only generated in Normal, Normal Request and Stop modes
72. Unless masked, If masked IRQ remains high and the ISR flags are not set.

7.1.12 Temperature sense gain

The analog multiplexer can be configured via the SPI to allow the ADOUT0 pin to deliver the internal junction temperature of the device. Figure 16 illustrates the internal chip temp sense obtained per characterization at three temperatures with three different lots and 30 samples.

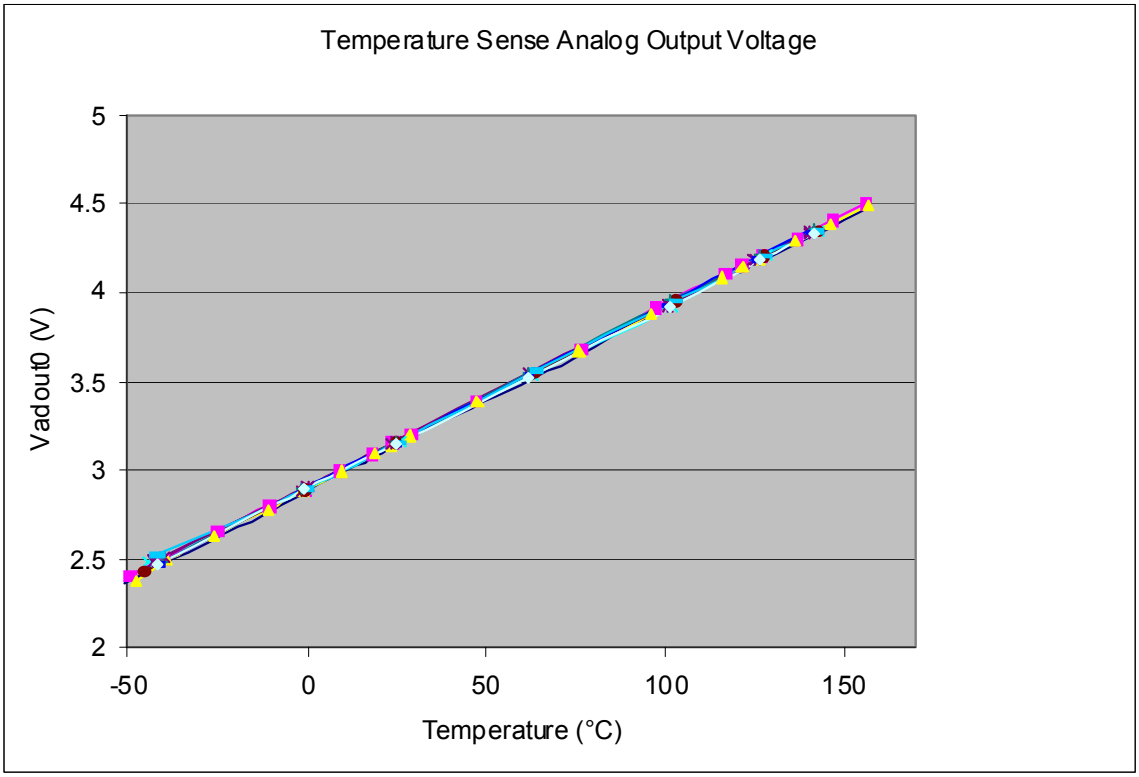


Figure 16. Temperature sense gain

7.1.13 High-side output pins HS1 and HS2

These outputs are two high-side drivers intended to drive small resistive loads or LEDs incorporating the following features:

- PWM capability (software maskable)
- Open load detection
- Current limitation
- Overtemperature shutdown (with maskable interrupt)
- High-voltage shutdown (software maskable)
- Cyclic sense

The high-side switches are controlled by the bits HS1:2 in the High-side Control register (HSCR).

7.1.13.1 PWM capability (direct access)

Each high-side driver offers additional (to the SPI control) direct control via the PWMIN pin. If both the bits HS1 and PWMHS1 are set in the High-side Control register (HSCR), then the HS1 driver is turned on if the PWMIN pin is high and turned of if the PWMIN pin is low. This applies to HS2 configuring HS2 and PWMHS2 bits.

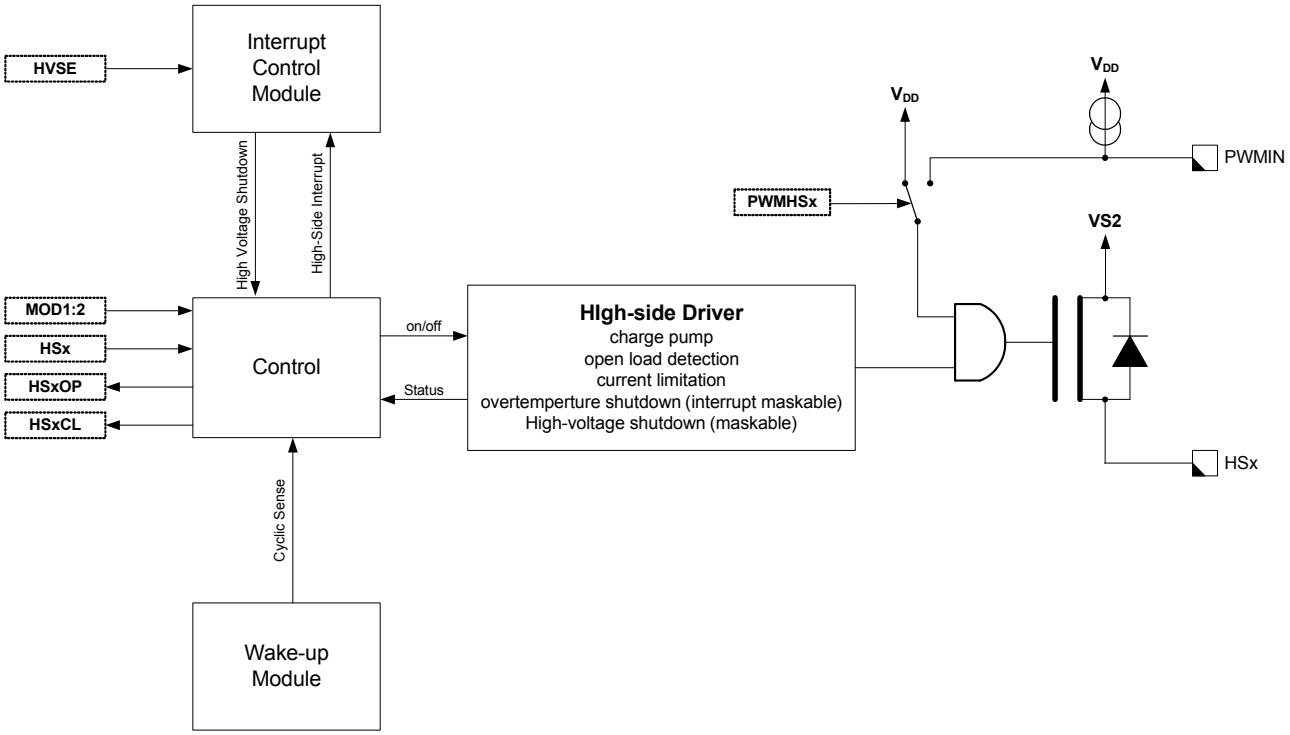


Figure 17. High-side drivers HS1 and HS2

7.1.13.2 Open load detection

Each high-side driver signals an open load condition if the current through the high-side is below the open load current threshold. The open load condition is indicated with the bits HS1OP and HS2OP in the High-side Status register (HSSR).

7.1.13.3 Current limitation

Each high-side driver has an output current limitation. In combination with the overtemperature shutdown the high-side drivers are protected against overcurrent and short-circuit failures. When the driver operates in the current limitation area, it is indicated with the bits HS1CL and HS2CL in the HSSR.

Note: If the driver is operating in current limitation mode, excessive power might be dissipated.

7.1.13.4 Overtemperature protection (HS interrupt)

Both high-side drivers are protected against overtemperature. In case of an overtemperature condition both high-side drivers are shutdown and the event is latched in the Interrupt Control Module. The shutdown is indicated as HS Interrupt in the Interrupt Source register (ISR).

A thermal shutdown of the high-side drivers is indicated by setting all HSxOP and HSxCL bits simultaneously. If the bit HSM is set in the Interrupt Mask register (IMR), then an interrupt (IRQ) is generated. A write to the high-side Control register (HSCR), when the overtemperature condition is gone, re-enables the high-side drivers.

7.1.13.5 High-voltage shutdown

In case of a high voltage condition and if the high voltage shutdown is enabled (bit HVSE in the Mode Control register (MCR) is set, both high-side drivers are shutdown. A write to the high-side Control register (HSCR), when the high voltage condition is gone, re-enables the high-side drivers.

7.1.13.6 Sleep and stop mode

The high-side drivers can be enabled to operate in Sleep and Stop mode for cyclic sensing. Also see Table 6, Operating modes overview.

7.1.14 Low-side output pins LS1 and LS2

These outputs are two low-side drivers intended to drive relays incorporating the following features:

- PWM capability (software maskable)
- Open load detection
- Current limitation
- Overtemperature shutdown (with maskable interrupt)
- Active clamp (for driving relays)
- High-voltage shutdown (software maskable)

The low-side switches are controlled by the bit LS1:2 in the Low-side Control register (LSCR). To protect the device against overvoltage when an inductive load (relay) is turned off. An active clamp re-enables the low-side FET if the voltage on the LS1 or LS2 pin exceeds a certain level.

7.1.14.1 PWM capability (direct access)

Each low-side driver offers additional (to the SPI control) direct control via the PWMIN pin. If both the bits LS1 and PWMLS1 are set in the Low-side Control register (LSCR), the LS1 driver is turned on if the PWMIN pin is high and turned off if the PWMIN pin is low. The same applies to the LS2 and PWMLS2 bits for the LS2 driver.

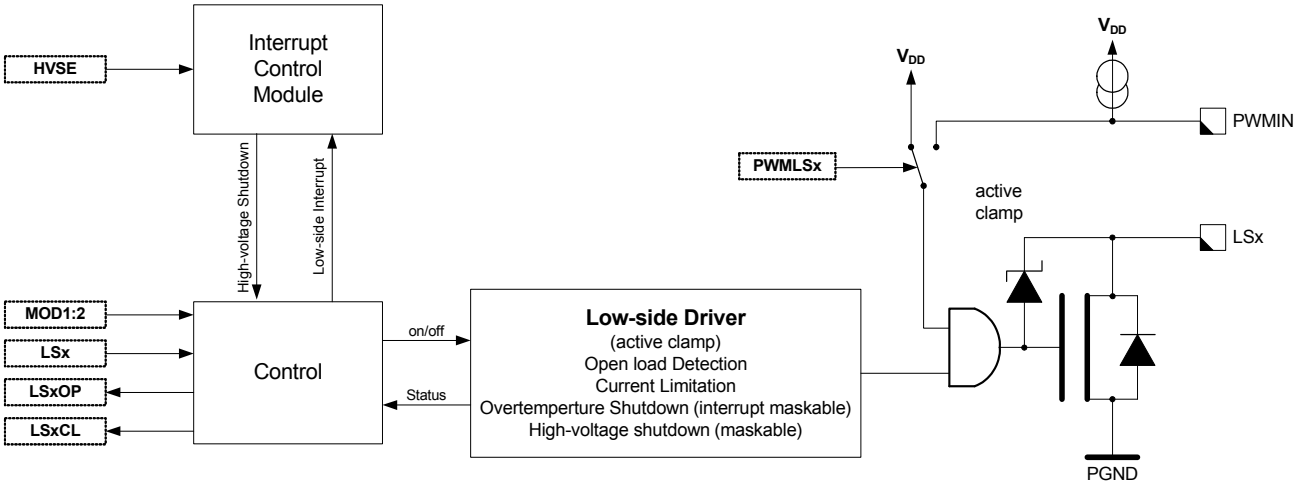


Figure 18. Low-side drivers LS1 and LS2

7.1.14.2 Open load detection

Each low-side driver signals an open load condition if the current through the low-side is below the open load current threshold. The open load condition is indicated with the bit LS1OP and LS2OP in the Low-side Status register (LSSR).

7.1.14.3 Current limitation

Each low-side driver has a current limitation. In combination with the overtemperature shutdown the low-side drivers are protected against overcurrent and short-circuit failures. When the drivers operate in current limitation, this is indicated with the bits LS1CL and LS2CL in the LSSR.

Note: If the drivers are operating in current limitation mode excessive power might be dissipated.

7.1.14.4 Overtemperature protection (LS interrupt)

Both low-side drivers are protected against overtemperature. In case of an overtemperature condition both low-side drivers are shutdown and the event is latched in the Interrupt Control Module. The shutdown is indicated as an LS Interrupt in the Interrupt Source register (ISR).

If the bit LSM is set in the Interrupt Mask register (IMR) then an Interrupt ($\overline{\text{IRQ}}$) is generated. A write to the Low-side Control register (LSCR), when the overtemperature condition is gone, re-enables the low-side drivers.

7.1.14.5 High-voltage shutdown

In case of a high-voltage condition and if the high-voltage shutdown is enabed (bit HVSE in the Mode Control register (MCR) is set) both low-sides drivers are shutdown. A write to the low-side Control register (LSCR), when the high-voltage condition is gone, re-enables the low-side drivers.

7.1.14.6 Sleep and stop mode

The low-side drivers are disabled in Sleep and Stop mode. Also see Table 6, Operating modes overview.

7.1.15 LIN physical layer

The LIN bus pin provides a physical layer for single-wire communication in automotive applications. The LIN physical layer is designed to meet the LIN physical layer specification and has the following features:

- LIN physical layer 2.0, 2.1 and SAEJ2602 compliant
- Slew rate selection
- Overtemperature shutdown
- Advanced diagnostics

The LIN driver is a low-side MOSFET with thermal shutdown. An internal pull-up resistor with a serial diode structure is integrated, so no external pull-up components are required for the application in a slave node. The fall time from dominant to recessive and the rise time from recessive to dominant is controlled. The symmetry between both slopes is guaranteed.

7.1.15.1 LIN pin

The LIN pin offers a high susceptibility immunity level from external disturbance, guaranteeing communication during external disturbance.

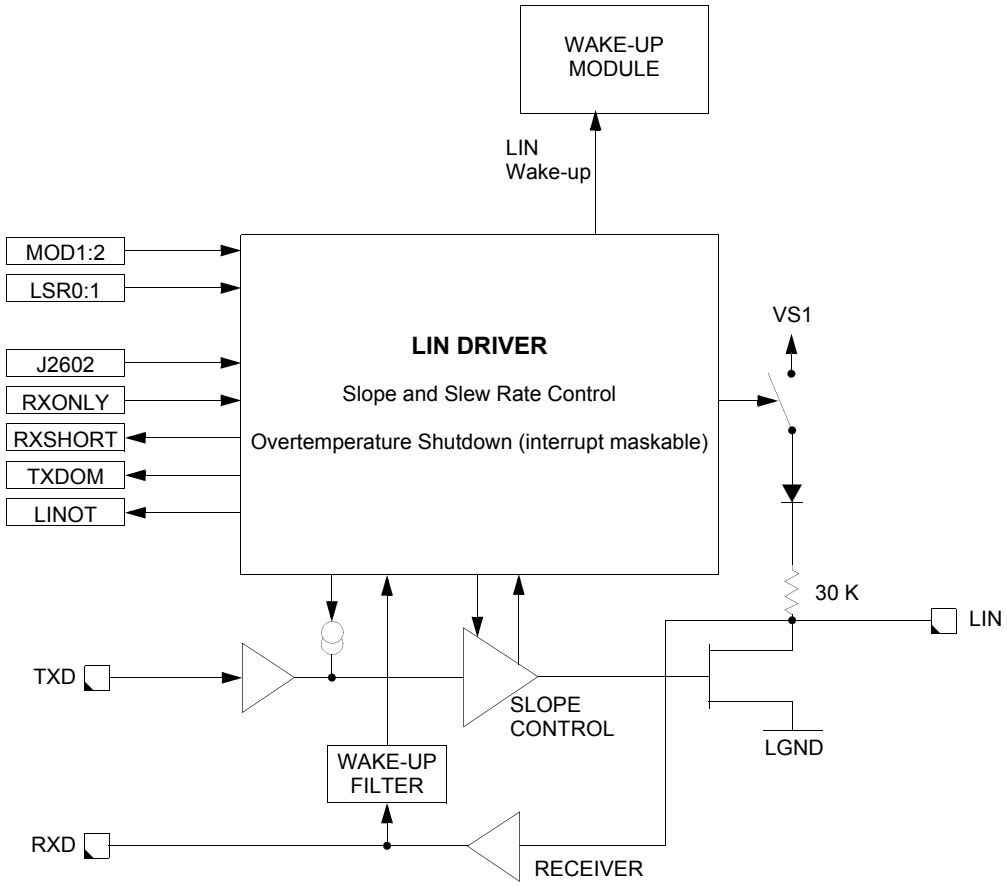


Figure 19. LIN interface

7.1.15.2 Slew rate selection

The slew rate can be selected for optimized operation at 10.4 and 20 kBit/s as well as a fast baud rate for test and programming. The slew rate can be adapted with the bits LSR1:0 in the LIN Control register (LINCR). The initial slew rate is optimized for 20 kBit/s.

7.1.15.3 J2602 conformance

To be compliant with the SAE J2602-2 specification, the J2602 feature has to be enabled in the LINCR register (bit DIS_J2602 sets to 0). The LIN transmitter is disabled in case of a V_{SUP} undervoltage condition occurs and TXD is in Recessive state: the LIN bus goes in Recessive state and RXD goes high. The LIN transmitter is not disabled if TXD is in Dominant state. A deglitcher on V_{SUP} (t_{J2602_DEG}) is implemented to avoid false switching.

If the (DIS_J2602) bit is set to 1, the J2602 feature is disabled and the communication TXD-LIN-RXD works for V_{SUP} down to 4.6 V (typical value) and then the communication is interrupted. The (DIS_J2602) bit is set per default to 0.

7.1.15.4 Overtemperature shutdown (LIN interrupt)

The output low-side FET is protected against overtemperature conditions. In case of an overtemperature condition, the transmitter is shutdown and the LINOT bit in the LIN Status register (LINSR) is set.

If the LINM bit is set in the Interrupt Mask register (IMR), an Interrupt $\overline{IRQ}$ is generated. The transmitter is automatically re-enabled once the condition is gone and TXD is high.

7.1.15.5 RXD short-circuit detection (LIN interrupt)

The LIN transceiver has a short-circuit detection for the RXD output pin. If the device transmits and in case of a short-circuit condition, either 5.0 V or Ground, the RXSHORT bit in the LIN Status register (LINSR) is set and the transmitter is shutdown.

If the LINM bit is set in the Interrupt Mask register (IMR), an Interrupt $\overline{IRQ}$ is generated. The transmitter is automatically re-enabled once the condition is gone (transition on RXD) and TXD is high. A read of the LIN Status register (LINSR) without the RXD pin short-circuit condition clears the bit RXSHORT.

7.1.15.6 TXD dominant detection (LIN interrupt)

The LIN transceiver monitors the TXD input pin to detect a stuck in dominant (0 V) condition. In case of a stuck condition (TXD pin 0 V for more than 1 second (typ.)), the transmitter is shutdown and the TXDOM bit in the LIN Status register (LINSR) is set.

If the LINM bit is set in the IMR, an Interrupt $\overline{IRQ}$ is generated. The transmitter is automatically re-enabled once TXD is high. A read of the LIN Status register (LINSR) with the TXD pin at 5.0 V clears the bit TXDOM.

7.1.15.7 LIN receiver operation only

While in Normal mode, the activation of the RXONLY bit disables the LIN TXD driver. In case of a LIN error condition, this bit is automatically set. If Stop mode is selected with this bit set, the LIN wake-up functionality is disabled and the RXD pin reflects the state of the LIN bus.

7.1.15.8 Stop mode and wake-up feature

During Stop mode operation, the transmitter of the physical layer is disabled. The receiver is still active and able to detect wake-up events on the LIN bus line. A dominant level longer than t_{PROPWL} followed by a rising edge generates a wake-up interrupt, and is reported in the Interrupt Source register (ISR). Also see Figure 11, page 21.

7.1.15.9 Sleep mode and wake-up feature

During Sleep mode operation, the transmitter of the physical layer is disabled. The receiver must be active to detect wake-up events on the LIN bus line. A dominant level longer than T_{PROPWL} followed by a rising edge generates a system wake-up (Reset), and is reported in the Interrupt Source register (ISR). Also see Figure 10, page 21.

7.2 Logic commands and registers

7.2.1 33912 SPI interface and configuration

The serial peripheral interface creates the communication link between a microcontroller (master) and the 33912. The interface consists of four pins (see Figure 20):

- $\overline{CS}$—Chip Select
- MOSI—Master-out Slave-in
- MISO—Master-in Slave-out
- SCLK—Serial Clock

A complete data transfer via the SPI consists of 1 byte. The master sends 4 bits of address (A3:A0) + 4 bits of control information (C3:C0) and the slave replies with 4 system status bits (VMS,LINS,HSS,LSS) + 4 bits of status information (S3:S0).

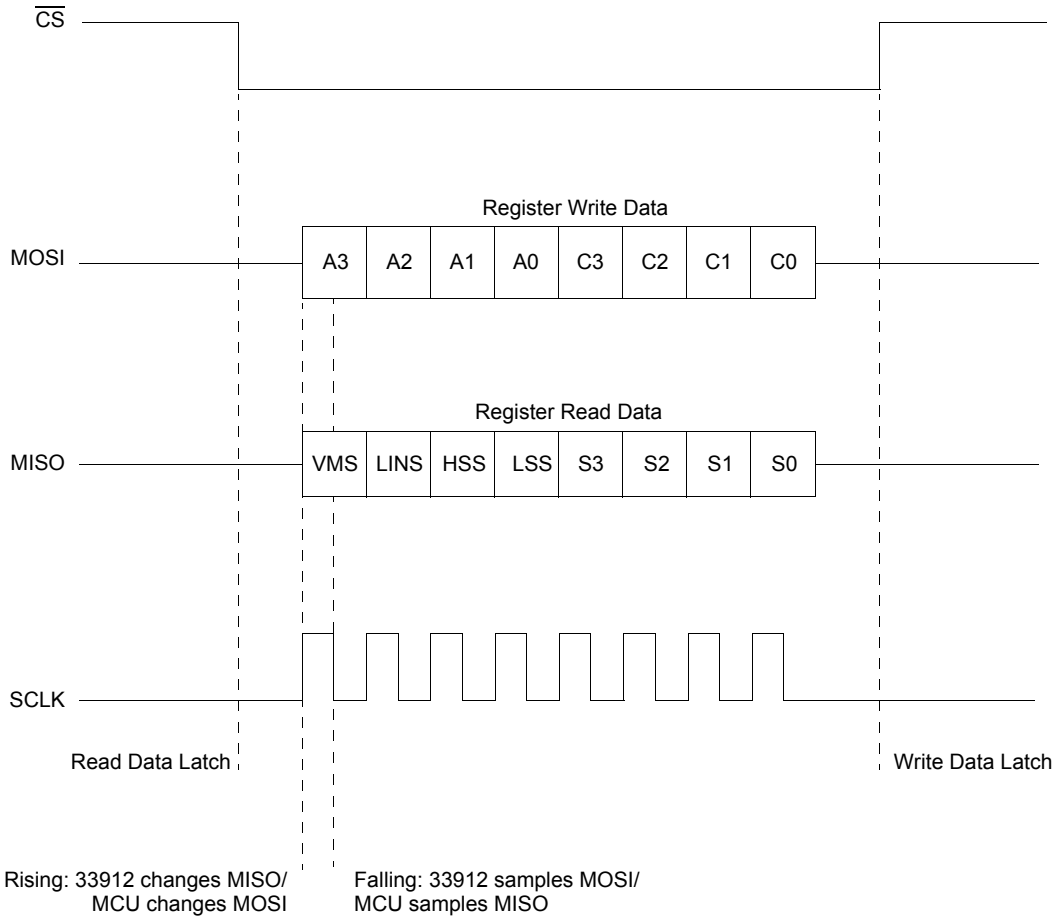


Figure 20. SPI protocol

During the inactive phase of the $\overline{CS}$ (HIGH), the new data transfer is prepared. The falling edge of the $\overline{CS}$ indicates the start of a new data transfer and puts the MISO in the low-impedance state and latches the analog status data (register read data).

With the rising edge of the SPI clock (SCLK), the data is moved to MISO/MOSI pins. With the falling edge of the SPI clock (SCLK), the data is sampled by the receiver. The data transfer is only valid if exactly 8 sample clock edges are present during the active (low) phase of $\overline{CS}$. The rising edge of the Chip Select $\overline{CS}$ indicates the end of the transfer and latches the write data (MOSI) into the register. The $\overline{CS}$ high forces MISO to the high-impedance state.

Register reset values are described along with the reset condition. Reset condition is the condition causing the bit to be set to its reset value. The main reset conditions are:

- Power-On Reset (POR): the level at which the logic is reset and BATFAIL flag sets.
- Reset mode
- Reset done by the $\overline{RST}$ pin (ext_reset)

7.3 SPI register overview

Table 8. System status register

Address(A3:A0)	Register Name / Read/Write Information		BIT			
			7	6	5	4
$0 - $F	SYSSR - System Status Register	R	VMS	LINS	HSS	LSS

Table 9 summarizes the SPI Register content for Control Information (C3:C0)=W and status information (S3:S0) = R.

Table 9. SPI register overview

Address(A3:A0)	Register name / read/write information		BIT			
			3	2	1	0
$0	MCR - Mode Control Register	W	HVSE	0	MOD2	MOD1
	VSR - Voltage Status Register	R	VSOV	VSUV	VDDOT	BATFAIL
$1	VSR - Voltage Status Register	R	VSOV	VSUV	VDDOT	BATFAIL
$2	WUCR - Wake-up Control Register	W	L4WE	L3WE	L2WE	L1WE
	WUSR - Wake-up Status Register	R	L4	L3	L2	L1
$3	WUSR - Wake-up Status Register	R	L4	L3	L2	L1
$4	LINCR - LIN Control Register	W	DIS_J2602	RXONLY	LSR1	LSR0
	LINSR - LIN Status Register	R	RXSHORT	TXDOM	LINOT	0
$5	LINSR - LIN Status Register	R	RXSHORT	TXDOM	LINOT	0
$6	HSCR - High-side Control Register	W	PWMHS2	PWMHS1	HS2	HS1
	HSSR - High-side Status Register	R	HS2OP	HS2CL	HS1OP	HS1CL
$7	HSSR - High-side Status Register	R	HS2OP	HS2CL	HS1OP	HS1CL
$8	LSCR - Low-side Control Register	W	PWMLS2	PWMLS1	LS2	LS1
	LSSR - Low-side Status Register	R	LS2OP	LS2CL	LS1OP	LS1CL
$9	LSSR - Low-side Status Register	R	LS2OP	LS2CL	LS1OP	LS1CL
$A	TIMCR - Timing Control Register	W	CS/$\overline{WD}$	WD2	WD1	WD0
				CYST2	CYST1	CYST0
	WDSR - Watchdog Status Register	R	WDTO	WDERR	WDOFF	WDWO
$B	WDSR - Watchdog Status Register	R	WDTO	WDERR	WDOFF	WDWO
$C	AMUXCR - Analog Multiplexer Control Register	W	LXDS	MX2	MX1	MX0
$D	CFR - Configuration Register	W	HVDD	CYSX8	CSAZ	CSGS
$E	IMR - Interrupt Mask Register	W	HSM	LSM	LINM	VMM
	ISR - Interrupt Source Register	R	ISR3	ISR2	ISR1	ISR0
$F	ISR - Interrupt Source Register	R	ISR3	ISR2	ISR1	ISR0

7.3.1 Register definitions

7.3.1.1 System status register - SYSSR

The System Status register (SYSSR) is always transferred with every SPI transmission and gives a quick system status overview. It summarizes the status of the Voltage Monitor Status (VMS), LIN Status (LINS), High-side Status (HSS), and the Low-side Status (LSS).

Table 10. System status register

	S7	S6	S5	S4
Read	VMS	LINS	HSS	LSS

7.3.1.1.1 VMS - voltage monitor status

This read-only bit indicates one or more bits in the VSR are set.

1 = Voltage Monitor bit set

0 = None

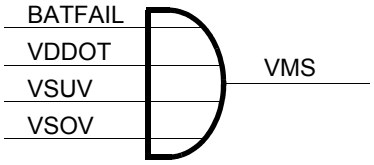


Figure 21. Voltage monitor status

7.3.1.1.2 LINS - LIN status

This read-only bit indicates one or more bits in the LINSR are set.

1 = LIN Status bit set

0 = None

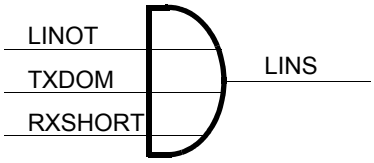


Figure 22. LIN status

7.3.1.1.3 HSS - high-side switch status

This read-only bit indicates one or more bits in the HSSR are set.

1 = High-side Status bit set

0 = None

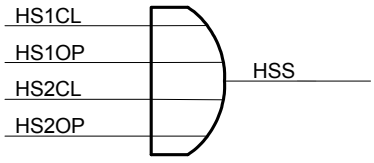


Figure 23. High-side status

7.3.1.1.4 LSS - low-side switch status

This read-only bit indicates one or more bits in the LSSR are set.
1 = Low-side Status bit set
0 = None

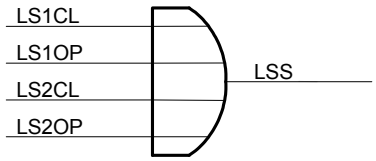


Figure 24. Low-side status

7.3.1.2 Mode control register - MCR

The Mode Control register (MCR) allows switching between the operation modes and to configure the 33912. Writing the MCR returns the VSR.

Table 11. Mode control register - $0

	C3	C2	C1	C0
Write	HVSE	0	MOD2	MOD1
Reset Value	1	0	-	-
Reset Condition	POR	POR	-	-

7.3.1.2.1 HVSE - high-voltage shutdown enable

This write-only bit enables/disables automatic shutdown of the high-side and the low-side drivers during a high-voltage VSOV condition.
1 = automatic shutdown enabled
0 = automatic shutdown disabled

7.3.1.2.2 MOD2, MOD1 - mode control bits

These write-only bits select the operating mode and allow clearing the watchdog in accordance with Table 9 Mode Control Bits.

Table 12. Mode control bits

MOD2	MOD1	Description
0	0	Normal Mode
0	1	Stop Mode
1	0	Sleep Mode
1	1	Normal Mode + Watchdog Clear

7.3.1.3 Voltage status register - VSR

Returns the status of the several voltage monitors. This register is also returned when writing to the Mode Control register (MCR).

Table 13. Voltage status register - $0/$1

	S3	S2	S1	S0
Read	VSOV	VSUV	VDDOT	BATFAIL

7.3.1.3.1 VSOV - V_{SUP} overvoltage

This read-only bit indicates an overvoltage condition on the VS1 pin.

1 = Overvoltage condition.

0 = Normal condition.

7.3.1.3.2 VSUV - V_{SUP} undervoltage

This read-only bit indicates an undervoltage condition on the VS1 pin.

1 = Undervoltage condition

0 = Normal condition

7.3.1.3.3 VDDOT - main voltage regulator overtemperature warning

This read-only bit indicates the main voltage regulator temperature reached the Overtemperature Prewarning threshold.

1 = Overtemperature Prewarning

0 = Normal

7.3.1.3.4 BATFAIL - battery fail flag

This read-only bit is set during power-up and indicates the 33912 had a Power-On-Reset (POR). Any access to the MCR or VSR clears the BATFAIL flag.

1 = POR Reset has occurred

0 = POR Reset has not occurred

7.3.1.4 Wake-up control register - WUCR

This register is used to control the digital wake-up inputs. Writing the WUCR returns the Wake-up Status register (WUSR).

Table 14. Wake-up control register - $2

	C3	C2	C1	C0
Write	L4WE	L3WE	L2WE	L1WE
Reset Value	1	1	1	1
Reset Condition	POR, Reset mode or ext_reset			

7.3.1.4.1 LxWE - wake-up input x enable

This write-only bit enables/disables which Lx inputs are enabled. In Stop and Sleep mode the LxWE bit determines which wake inputs are active for wake-up. If one of the Lx inputs is selected on the analog multiplexer, the corresponding LxWE is masked to 0.

1 = Wake-up Input x enabled

0 = Wake-up Input x disabled

7.3.1.5 Wake-up status register - WUSR

This register is used to monitor the digital wake-up inputs and is also returned when writing to the WUCR.

Table 15. Wake-up status register - $2/$3

	S3	S2	S1	S0
Read	L4	L3	L2	L1

7.3.1.5.1 Lx - wake-up input x

This read-only bit indicates the status of the corresponding Lx input. If the Lx input is not enabled, then the according Wake-up status returns 0. After a wake-up from Stop or Sleep mode these bits also allow to determine which input has caused the wake-up, by first reading the Interrupt Status register (ISR) and then reading the WUSR. The source of the wake-up is only reported on the first WUCR or WUSR access.

1 = Lx pin high, or Lx is the source of the wake-up

0 = Lx pin low, disabled or selected as an analog input

7.3.1.6 LIN control register - LINCR

This register controls the LIN physical interface block. Writing the LIN Control register (LINCR) returns the LIN Status register (LINSR).

Table 16. LIN control register - $4

	C3	C2	C1	C0
Write	DIS_J2602	RXONLY	LSR1	LSR0
Reset Value	0	0	0	0
Reset Condition	POR	POR, Reset mode, ext_reset or LIN failure gone*	POR	

* LIN failure gone: if LIN failure (overtemp, TXD/RXD short) was set, the flag resets automatically when the failure is gone.

7.3.1.6.1 J2602 - LIN dominant voltage select

This write-only bit controls the J2602 circuitry. If the circuitry is enabled (bit sets to 0), the TXD-LIN-RXD communication works down to the battery undervoltage condition is detected. Below, the bus is in recessive state. If the circuitry is disabled (bit sets to 1), the communication TXD-LIN-RXD works down to 4.6 V (typical value).

0 = Enabled J2602 feature

1 = Disabled J2602 feature

7.3.1.6.2 RXONLY - LIN receiver operation only

This write-only bit controls the behavior of the LIN transmitter. In Normal mode, the activation of the RXONLY bit disables the LIN transmitter. In case of a LIN error condition, this bit is automatically set. In Stop mode this bit disables the LIN wake-up functionality, and the RXD pin reflects the state of the LIN bus.

1 = only LIN receiver active (Normal mode) or LIN wake-up disabled (Stop mode)

0 = LIN fully enabled

7.3.1.6.3 LSRx - LIN slew rate

This write-only bit controls the LIN driver slew-rate in accordance with Table 17.

Table 17. LIN slew rate control

LSR1	LSR0	Description
0	0	Normal Slew Rate (up to 20 kb/s)
0	1	Slow Slew Rate (up to 10 kb/s)
1	0	Fast Slew Rate (up to 100 kb/s)
1	1	Reserved

7.3.1.7 LIN status register - LINSR

This register returns the status of the LIN physical interface block and is also returned when writing to the LINCR.

Table 18. LIN status register - $4/$5

	S3	S2	S1	S0
Read	RXSHORT	TXDOM	LINOT	0

7.3.1.7.1 RXSHORT - RXD pin short-circuit

This read-only bit indicates a short-circuit condition on the RXD pin (shorted either to 5.0 V or to Ground). The short-circuit delay must be a worst case of 8µs to be detected and to shutdown the driver. To clear this bit, it must be read after the condition is gone (transition detected on RXD pin). The LIN driver is automatically re-enabled once the condition is gone and TXD is high.

1 = RXD short-circuit condition

0 = None

7.3.1.7.2 TXDOM - TXD permanent dominant

This read-only bit signals the detection of a TXD pin stuck at dominant (Ground) condition and the resultant shutdown in the LIN transmitter. This condition is detected after the TXD pin remains in dominant state for more than 1 second (typical value).

To clear this bit, it must be read after TXD has gone high. The LIN driver is automatically re-enabled once TXD goes High.

1 = TXD stuck at dominant fault detected

0 = None

7.3.1.7.3 LINOT - LIN driver overtemperature

This read-only bit signals the LIN transceiver was shutdown due to overtemperature. The transmitter is automatically re-enabled after the overtemperature condition is gone and TXD is high. The LINOT bit is cleared after a SPI read once the condition is gone.

1 = LIN overtemperature shutdown

0 = None

7.3.1.8 High-side control register - HSCR

This register controls the operation of the high-side drivers. Writing to this register returns the high-side Status register (HSSR).

Table 19. High-side control register - $6

	C3	C2	C1	C0
Write	PWMHS2	PWMHS1	HS2	HS1
Reset Value	0	0	0	0
Reset Condition	POR		POR, Reset mode, ext_reset, HSx overtemp or (VSOV & HVSE)	

7.3.1.8.1 PWMHSx - PWM input control enable

This write-only bit enables/disables the PWMIN input pin to control the respective high-side switch. The corresponding high-side switch must be enabled (HSx bit).

1 = PWMIN input controls HSx output

0 = HSx is controlled only by the SPI

7.3.1.8.2 HSx - HSx switch control.

This write-only bit enables/disables the corresponding high-side switch.

1 = HSx switch on

0 = HSx switch off

7.3.1.9 High-side status register - HSSR

This register returns the status of the high-side switches and is also returned when writing to the HSCR.

Table 20. High-side status register - $6/$7

	S3	S2	S1	S0
Read	HS2OP	HS2CL	HS1OP	HS1CL

7.3.1.9.1 High-side thermal shutdown

A thermal shutdown of the high-side drivers is indicated by setting all HSxOP and HSxCL bits simultaneously.

7.3.1.9.2 HSxOP - high-side switch open load detection

This read-only bit signals the high-side switches are conducting current below a certain threshold indicating possible load disconnection.

1 = HSx Open Load detected (or thermal shutdown)

0 = Normal

7.3.1.9.3 HSxCL - high-side current limitation

This read-only bit indicates the respective high-side switch is operating in current limitation mode.

1 = HSx in current limitation (or thermal shutdown)

0 = Normal

7.3.1.10 Low-side control register - LSCR

This register controls the operation of the low-side drivers. Writing the low-side Control register (LSCR) also returns the low-side Status register (LSSR).

Table 21. Low-side control register - $8

	C3	C2	C1	C0
Write	PWMLS2	PWMLS1	LS2	LS1
Reset Value	0	0	0	0
Reset Condition	POR		POR, Reset mode, ext_reset, LSx overtemp or (VSOV & HVSE)	

7.3.1.10.1 PWMLx - PWM input control enable

This write-only bit enables/disables the PWMIN input pin to control the respective low-side switch. The corresponding low-side switch must be enabled (LSx bit).

1 = PWMIN input controls LSx

0 = LSx is controlled only by the SPI

7.3.1.10.2 LSx - LSx switch control

This write-only bit enables/disables the corresponding low-side switch.

1 = LSx switch on

0 = LSx switch off

7.3.1.11 Low-side status register - LSSR

This register returns the status of the low-side switches and is also returned when writing to the LSCR.

Table 22. Low-side status register - $8/$9

	C3	C2	C1	C0
Read	LS2OP	LS2CL	LS1OP	LS1CL

7.3.1.11.1 Low-side thermal shutdown

A thermal shutdown of the low-side drivers is indicated by setting all LSxOP and LSxCL bits simultaneously.

7.3.1.11.2 LSxOP - low-side switch open load detection

This read-only bit signals the low-side switches are conducting current below a certain threshold indicating possible load disconnection.
1 = LSx Open Load detected (or thermal shutdown)
0 = Normal

7.3.1.11.3 LSxCL - low-side current limitation

This read-only bit indicates the respective low-side switch is operating in current limitation mode.
1 = LSx in current limitation (or thermal shutdown)
0 = Normal

7.3.1.12 Timing control register - TIMCR

This register allows to configure the watchdog, the cyclic sense and Forced Wake-up periods. Writing to the Timing Control register (TIMCR) also returns the Watchdog Status register (WDSR).

Table 23. Timing control register - $A

	C3	C2	C1	C0
Write	CS/$\overline{WD}$	WD2	WD1	WD0
		CYST2	CYST1	CYST0
Reset Value	-	0	0	0
Reset Condition	-	POR		

7.3.1.12.1 CS/$\overline{WD}$ - cyclic sense or watchdog prescaler select

This write-only bit selects which prescaler is being written to, the Cyclic Sense/Forced Wake-up prescaler or the Watchdog prescaler.
1 = Cyclic Sense/Forced Wake-up Prescaler selected
0 = Watchdog Prescaler select

7.3.1.12.2 WDx - watchdog prescaler

This write-only bits selects the divider for the watchdog prescaler and therefore selects the watchdog period in accordance with Table 24. This configuration is valid only if windowing watchdog is active.

Table 24. Watchdog prescaler

WD2	WD1	WD0	Prescaler divider
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	6
1	0	0	8
1	0	1	10
1	1	0	12
1	1	1	14

7.3.1.12.3 CYSTx - cyclic sense period prescaler select

This write-only bits selects the interval for the wake-up cyclic sensing together with the bit CYSX8 in the Configuration register (CFR) (see page 49). This option is only active if one of the high-side switches is enabled when entering in Stop or Sleep mode. Otherwise, a timed wake-up is performed after the period shown in Table 25.

Table 25. Cyclic sense and force wake up interval

CYSX8[73]	CYST2	CYST1	CYST0	Interval
X	0	0	0	No cyclic sense[74]
0	0	0	1	20 ms
0	0	1	0	40 ms
0	0	1	1	60 ms
0	1	0	0	80 ms
0	1	0	1	100 ms
0	1	1	0	120 ms
0	1	1	1	140 ms
1	0	0	1	160 ms
1	0	1	0	320 ms
1	0	1	1	480 ms
1	1	0	0	640 ms
1	1	0	1	800 ms
1	1	1	0	960 ms
1	1	1	1	1120 ms

Notes
73. bit CYSX8 is located in Configuration register (CFR)
74. No Cyclic Sense and no Force Wake-up available.

7.3.1.13 Watchdog status register - WDSR

This register returns the Watchdog status information and is also returned when writing to the TIMCR.

Table 26. Watchdog status register - $A/$B

	S3	S2	S1	S0
Read	WDTO	WDERR	WDOFF	WDWO

7.3.1.13.1 WDTO - watchdog timeout

This read-only bit signals the last reset was caused by either a watchdog timeout or by an attempt to clear the Watchdog within the window closed. Any access to this register or the Timing Control register (TIMCR) clears the WDTO bit.

1 = Last reset caused by watchdog timeout

0 = None

7.3.1.13.2 WDERR - watchdog error

This read-only bit signals the detection of a missing watchdog resistor. In this condition the watchdog is using the internal, lower precision timebase. The Windowing function is disabled.

1 = WDCONF pin resistor missing

0 = WDCONF pin resistor not floating

7.3.1.13.3 WDOFF - watchdog off

This read-only bit signals the watchdog pin connected to Ground and therefore disabled. In this case watchdog timeouts are disabled and the device automatically enters Normal mode out of Reset. This might be necessary for software debugging and for programming the Flash memory.

1 = Watchdog is disabled

0 = Watchdog is enabled

7.3.1.13.4 WDWO - watchdog window open

This read-only bit signals when the watchdog window is open for clears. The purpose of this bit is for testing. Should be ignored in case WDERR is High.

1 = Watchdog window open

0 = Watchdog window closed

7.3.1.14 Analog multiplexer control register - MUXCR

This register controls the analog multiplexer and selects the divider ration for the Lx input divider.

Table 27. Analog multiplexer control register -$C

	C3	C2	C1	C0
Write	LXDS	MX2	MX1	MX0
Reset Value	1	0	0	0
Reset Condition	POR	POR, Reset mode or ext_reset		

7.3.1.14.1 LXDS - Lx analog input divider select

This write-only bit selects the resistor divider for the Lx analog inputs. Voltage is internally clamped to VDD.

0 = Lx Analog divider: 1

1 = Lx Analog divider: 3.6 (typ.)

7.3.1.15 MXx - analog multiplexer input select

These write-only bits selects which analog input is multiplexed to the ADOUT0 pin according to Table 28.
When disabled or when in Stop or Sleep mode, the output buffer is not powered and the ADOUT0 output is left floating to achieve lower current consumption.

Table 28. Analog multiplexer channel select

MX2	MX1	MX0	Meaning
0	0	0	Disabled
0	0	1	Reserved
0	1	0	Die Temperature Sensor(75)
0	1	1	VSENSE input
1	0	0	L1 input
1	0	1	L2 input
1	1	0	L3 input
1	1	1	L4 input

Notes
75. Accessing the Die Temperature Sensor directly from the Disabled state is not recommended. If this transition must be performed and to avoid the intermediate state, wait at least 1.0 ms, then start the die temp measurement.
Possible access is Disabled ⟶ Vsense input ⟶ Die Temperature Sensor.

7.3.1.16 Configuration register - CFR

This register controls the Hall Sensor Supply enable/disable, the cyclic sense timing multiplier, enables/disables the Current Sense Auto-zero function and selects the gain for the current sense amplifier.

Table 29. Configuration register - $D

	C3	C2	C1	C0
Write	HVDD	CYSX8	CSAZ	CSGS
Reset Value	0	0	0	0
Reset Condition	POR, Reset mode or ext_reset	POR	POR	POR

7.3.1.16.1 HVDD - hall sensor supply enable

This write-only bit enables/disables the state of the hall sensor supply.
1 = HVDD on
0 = HVDD off

7.3.1.16.2 CYSX8 - cyclic sense timing x 8

This write-only bit influences the cyclic sense and Forced Wake-up period as shown in Table .
1 = Multiplier enabled
0 = None

7.3.1.16.3 CSAZ - current sense auto-zero function enable

This write-only bit enables/disables the circuitry to lower the offset voltage of the current sense amplifier.
1 = Auto-zero function enabled
0 = Auto-zero function disabled

7.3.1.16.4 CSGS - current sense amplifier gain select

This write-only bit selects the gain of the current sense amplifier.

1 = 14.5 (typ.)

0 = 30 (typ.)

7.3.1.17 Interrupt mask register - IMR

This register allows masking of some of the interrupt sources. No interrupt is generated to the MCU and no flag is set in the ISR register. The 5.0 V Regulator overtemperature prewarning interrupt and undervoltage (V_{SUV}) interrupts can not be masked and always causes an interrupt. Writing to the IMR returns the ISR.

Table 30. Interrupt mask register - $E

	C3	C2	C1	C0
Write	HSM	LSM	LINM	VMM
Reset Value	1	1	1	1
Reset Condition	POR			

7.3.1.17.1 HSM - high-side interrupt mask

This write-only bit enables/disables interrupts generated in the high-side block.

1 = HS Interrupts Enabled

0 = HS Interrupts Disabled

7.3.1.17.2 LSM - low-side interrupt mask

This write-only bit enables/disables interrupts generated in the low-side block.

1 = LS Interrupts Enabled

0 = LS Interrupts Disabled

7.3.1.17.3 LINM - LIN interrupts mask

This write-only bit enables/disables interrupts generated in the LIN block.

1 = LIN Interrupts Enabled

0 = LIN Interrupts Disabled

7.3.1.17.4 VMM - voltage monitor interrupt mask

This write-only bit enables/disables interrupts generated in the Voltage Monitor block. The only maskable interrupt in the Voltage Monitor block is the V_{SUP} overvoltage interrupt.

1 = Interrupts Enabled

0 = Interrupts Disabled

7.3.1.18 Interrupt source register - ISR

This register allows the MCU to determine the source of the last interrupt or wake-up respectively. A read of the register acknowledges the interrupt and leads IRQ pin to high, in case there are no other pending interrupts. If there are pending interrupts, IRQ is driven high for 10 µs and then be driven low again. This register is also returned when writing to the Interrupt Mask register (IMR).

Table 31. Interrupt source register - $E/$F

	S3	S2	S1	S0
Read	ISR3	ISR2	ISR1	ISR0

7.3.1.18.1 ISRx - interrupt source register

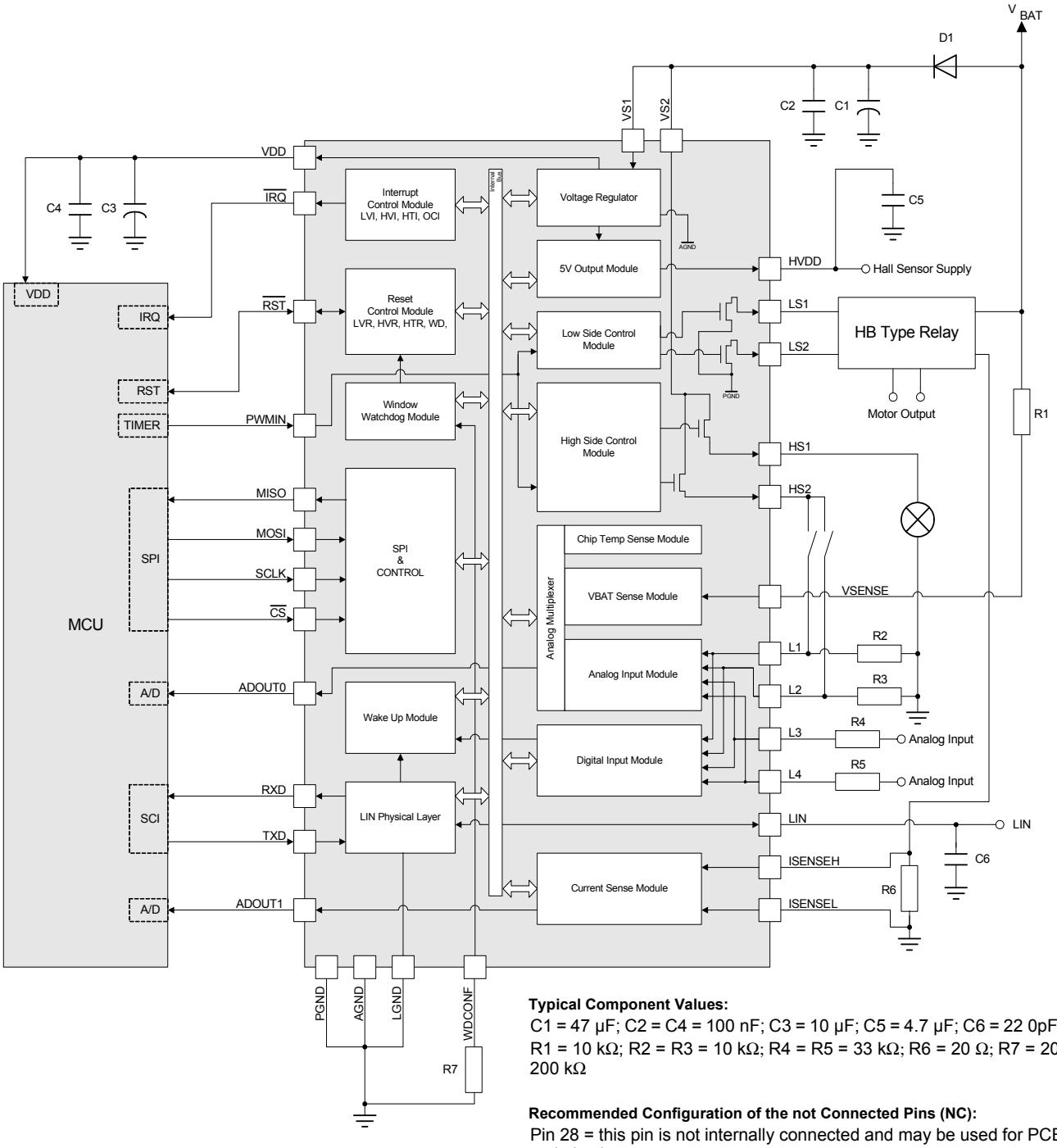
These read-only bits indicate the interrupt source following Table 32. If no interrupt is pending then all bits are 0. If more than one interrupt is pending, the interrupt sources are handled sequentially multiplex.

Table 32. Interrupt sources

				Interrupt source		Priority
ISR3	**ISR2**	**ISR1**	**ISR0**	**none maskable**	**maskable**	
0	0	0	0	no interrupt	no interrupt	none
0	0	0	1	Lx Wake-up from Stop and Sleep mode	-	highest
0	0	1	0	-	HS Interrupt (Overtemperature)	
0	0	1	1	-	LS Interrupt (Overtemperature)	
0	1	0	0	LIN Wake-up	LIN Interrupt (RXSHORT, TXDOM, LIN OT)	
0	1	0	1	Voltage Monitor Interrupt (Low Voltage and VDD overtemperature)	Voltage Monitor Interrupt (High Voltage)	
0	1	1	0	Forced Wake-up	-	lowest

8 Typical application

The 33912 can be configured in several applications. The figure below shows the 33912 in the typical Slave Node Application.



Typical Component Values:
C1 = 47 µF; C2 = C4 = 100 nF; C3 = 10 µF; C5 = 4.7 µF; C6 = 22 0pF or 68 pF
R1 = 10 kΩ; R2 = R3 = 10 kΩ; R4 = R5 = 33 kΩ; R6 = 20 Ω; R7 = 20 kΩ-200 kΩ

Recommended Configuration of the not Connected Pins (NC):
Pin 28 = this pin is not internally connected and may be used for PCB routing optimization.

9 MC33912BAC product specifications, Pages 53 to 103

10 Internal block diagram

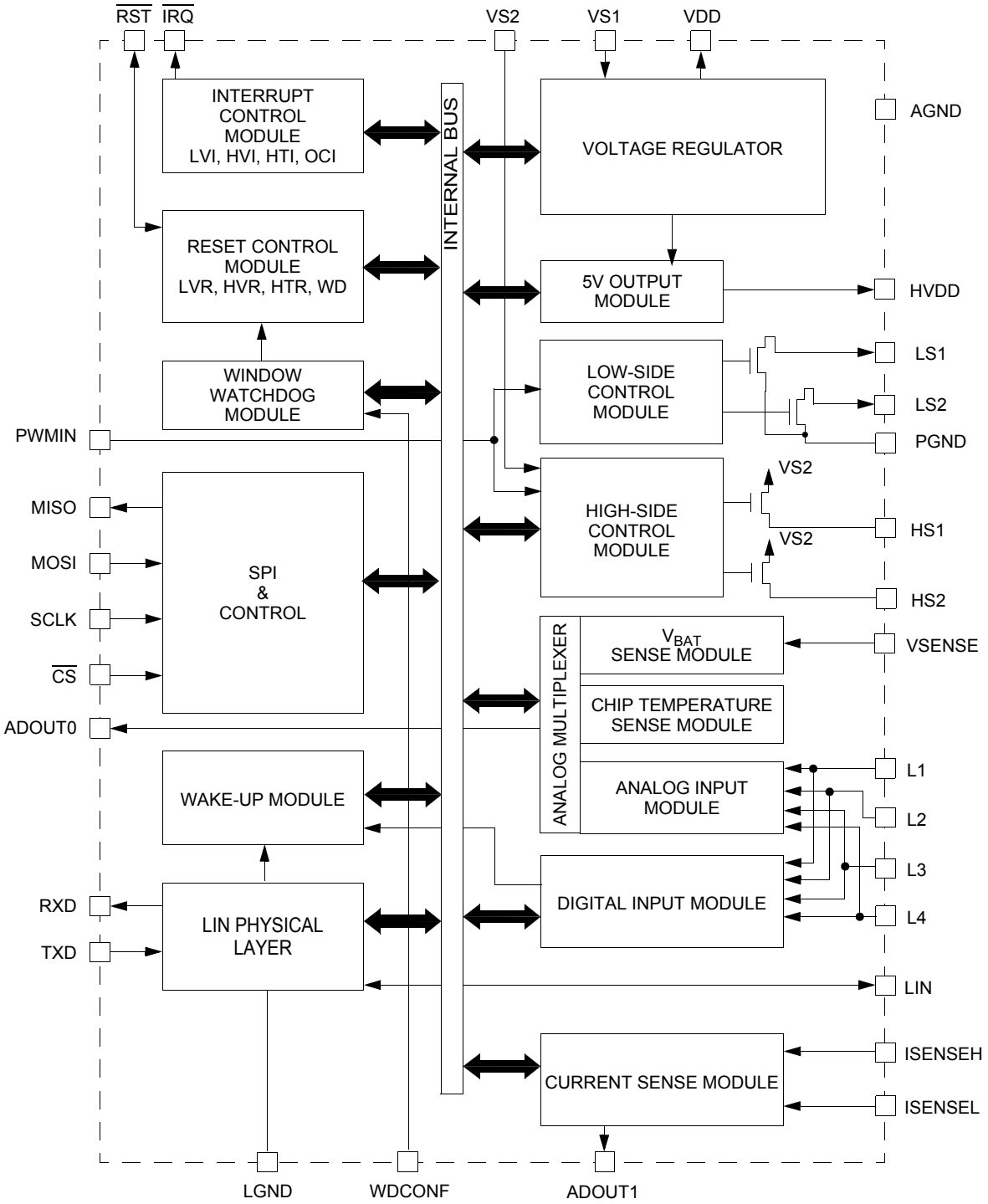


Figure 25. 33912 simplified internal block diagram

11 Pin connections

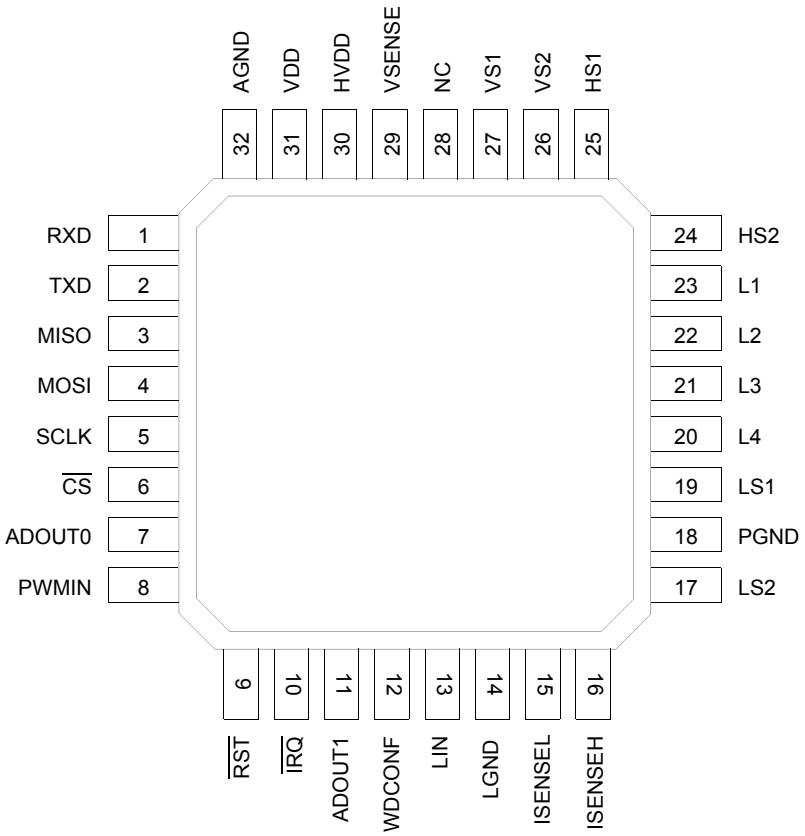


Figure 26. 33912 pin connections

A functional description of each pin can be found in the Functional pin description on page 73.

Table 33. 33912 pin definitions

Pin	Pin name	Formal name	Definition
1	RXD	Receiver Output	This pin is the receiver output of the LIN interface which reports the state of the bus voltage to the MCU interface.
2	TXD	Transmitter Input	This pin is the transmitter input of the LIN interface which controls the state of the bus output.
3	MISO	SPI Output	SPI (Serial Peripheral Interface) data output. When $\overline{CS}$ is high, pin is in the high-impedance state.
4	MOSI	SPI Input	SPI (Serial Peripheral Interface) data input.
5	SCLK	SPI Clock	SPI (Serial Peripheral Interface) clock Input.
6	CS	SPI Chip Select	SPI (Serial Peripheral Interface) chip select input pin. $\overline{CS}$ is active low.
7	ADOUT0	Analog Output Pin 0	Analog Multiplexer Output.
8	PWMIN	PWM Input	High-side and Low-side Pulse Width Modulation Input.
9	RST	Internal Reset I/O	Bidirectional Reset I/O pin - driven low when any internal reset source is asserted. $\overline{RST}$ is active low.
10	IRQ	Internal Interrupt Output	Interrupt output pin, indicating wake-up events from Stop mode or events from Normal and Normal request modes. $\overline{IRQ}$ is active low.
11	ADOUT1	Analog Output Pin 1	Current sense analog output.

Table 33. 33912 pin definitions (continued)

Pin	Pin name	Formal name	Definition
12	WDCONF	Watchdog Configuration Pin	This input pin is for configuration of the watchdog period and allows the disabling of the watchdog.
13	LIN	LIN Bus	This pin represents the single-wire bus transmitter and receiver.
14	LGND	LIN Ground Pin	This pin is the device LIN ground connection. It is internally connected to the PGND pin.
15 16	ISENSEL ISENSEH	Current Sense Pins	Current Sense differential inputs.
17 19	LS2 LS1	Low-side Outputs	Relay drivers low-side outputs.
18	PGND	Power Ground Pin	This pin is the device low-side ground connection. It is internally connected to the LGND pin.
20 21 22 23	L4 L3 L2 L1	Wake-up Inputs	These pins are the wake-up capable digital inputs[76]. In addition, all Lx inputs can be sensed analog via the analog multiplexer.
24 25	HS2 HS1	High-side Outputs	High-side switch outputs.
26 27	VS2 VS1	Power Supply Pin	These pins are device battery level power supply pins.VS2 is supplying the HSx drivers while VS1 supplies the remaining blocks.[77]
29	VSENSE	Voltage Sense Pin	Battery voltage sense input.[78]
30	HVDD	Hall Sensor Supply Output	+5.0 V switchable supply output pin.[79]
31	VDD	Voltage Regulator Output	+5.0 V main voltage regulator output pin.[80]
32	AGND	Analog Ground Pin	This pin is the device analog ground connection.

Notes

76. When used as digital input, a series 33 kΩ resistor must be used to protect against automotive transients.
77. Reverse battery protection series diodes must be used externally to protect the internal circuitry.
78. This pin can be connected directly to the battery line for voltage measurements. The pin is self protected against reverse battery connections. It is strongly recommended to connect a 10 kΩ resistor in series with this pin for protection purposes.
79. External capacitor (1.0 µF < C < 10 µF; 0.1 Ω < ESR < 5.0 Ω) required.
80. External capacitor (2.0 µF < C < 100 µF; 0.1 Ω < ESR < 10.0 Ω) required.

12 Electrical characteristics

12.1 Maximum ratings

Table 34. Maximum ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
Electrical ratings				
$V_{SUP(SS)}$ $V_{SUP(PK)}$	Supply Voltage at VS1 and VS2 • Normal Operation (DC) • Transient Conditions (load dump)	 -0.3 to 27 -0.3 to 40	V	
V_{DD}	Supply Voltage at VDD	-0.3 to 5.5	V	
V_{IN} $V_{IN(IRQ)}$	Input / Output Pins Voltage • $\overline{CS}$, $\overline{RST}$, SCLK, PWMIN, ADOUT0, ADOUT1, MOSI, MISO, TXD, RXD, HVDD • Interrupt Pin ($\overline{IRQ}$)	-0.3 to V_{DD} +0.3 -0.3 to 11	V	(81) (82)
V_{HS}	HS1 and HS2 Pin Voltage (DC)	-0.3 to V_{SUP} +0.3	V	
V_{LS}	LS1 and LS2 Pin Voltage (DC)	-0.3 to 45	V	
V_{LxDC} V_{LxTR}	L1, L2, L3 and L4 Pin Voltage • Normal Operation with a series 33 kΩ resistor (DC) • Transient input voltage with external component (according to ISO7637-2) (See Figure 28)	 -18 to 40 ±100	V	
V_{ISENSE}	ISENSEH and ISENSEL Pin Voltage (DC)	-0.3 to 40	V	
V_{VSENSE}	VSENSE Pin Voltage (DC)	-27 to 40	V	
V_{BUSDC} V_{BUSTR}	LIN Pin Voltage • Normal Operation (DC) • Transient input voltage with external component (according to ISO7637-2) (See Figure 27)	 -18 to 40 -150 to 100	V	
I_{VDD}	VDD output current	Internally Limited	A	
V_{ESD1-1} V_{ESD1-2} V_{ESD2} V_{ESD3-1} V_{ESD3-2}	ESD Voltage • Human Body Model - LIN Pin • Human Body Model - all other Pins • Machine Model • Charge Device Model • Corner Pins (Pins 1, 8, 9, 16, 17, 24, 25, and 32) • All other Pins (Pins 2-7, 10-15, 18-23, 26-31)	 ±8000 ±2000 ±150 ±750 ±500	V	(83)

Notes

81. Exceeding voltage limits on specified pins may cause a malfunction or permanent damage to the device.
82. Extended voltage range for programming purpose only.
83. Testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω) and the Charge Device Model, Robotic (C_{ZAP} = 4.0 pF).

Table 34. Maximum ratings (continued)

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
Thermal ratings				
T_A	Operating Ambient Temperature 33912 34912	 -40 to 125 -40 to 85	°C	(84)
T_J	Operating Junction Temperature	-40 to 150	°C	
T_{STG}	Storage Temperature	-55 to 150	°C	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient Natural Convection, Single Layer board (1s) Natural Convection, Four Layer board (2s2p)	 85 56	°C/W	 (85), (86) (85), (87)
$R_{\theta JC}$	Thermal Resistance, Junction to Case	23	°C/W	(88)
T_{PPRT}	Peak Package Reflow Temperature During Reflow	Note 90	°C	(89), (90)

Notes

84. The limiting factor is junction temperature; taking into account the power dissipation, thermal resistance, and heat sinking.
85. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
86. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
87. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
88. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
89. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
90. NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.NXP.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

12.2 Static electrical characteristics

Table 35. Static electrical characteristics

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33912 and -40 °C ≤ T_A ≤ 85 °C for the 34912, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Supply voltage range (VS1, VS2)						
V_{SUP}	Nominal Operating Voltage	5.5	–	18	V	
V_{SUPOP}	Functional Operating Voltage	–	–	27	V	(91)
V_{SUPLD}	Load Dump	–	–	40	V	
Supply current range (V_{SUP} = 13.5 V)						
I_{RUN}	Normal Mode (I_{OUT} at V_{DD} = 10 mA), LIN Recessive State	–	4.5	10	mA	(92)
I_{STOP}	Stop mode, VDD ON with I_{OUT} = 100 µA, LIN Recessive State • 5.5 V < V_{SUP} < 12 V • V_{SUP} = 13.5 V	 – –	 48 58	 80 90	µA	(92), (93), (94)
I_{SLEEP}	Sleep mode, VDD OFF, LIN Recessive State • 5.5 V < V_{SUP} < 12 V • 12 V ≤ V_{SUP} < 13.5 V	 – –	 27 37	 35 48	µA	(92), (94)
I_{CYCLIC}	Cyclic Sense Supply Current Adder(95)	–	10	–	µA	
Supply under/overvoltage detections						
$V_{BATFAIL}$ $V_{BATFAIL\_HYS}$	Power-On Reset (BATFAIL) • Threshold (measured on VS1) • Hysteresis (measured on VS1)	 1.5 –	 3.0 0.9	 3.9 –	V	(96) (95) (95)
V_{SUV} V_{SUV_HYS}	V_{SUP} Undervoltage Detection (VSUV Flag) (Normal and Normal Request modes, Interrupt Generated) • Threshold (measured on VS1) • Hysteresis (measured on VS1)	 5.55 –	 6.0 1.0	 6.6 –	V	
V_{SOV} V_{SOV_HYS}	V_{SUP} Overvoltage Detection (VSOV Flag) (Normal and Normal Request modes, Interrupt Generated) • Threshold (measured on VS1) • Hysteresis (measured on VS1)	 18 –	 19.25 1.0	 20.5 –	V	

Notes

91. Device is fully functional. All features are operating.
92. Total current (I_{VS1} + I_{VS2}) measured at GND pins excluding all loads, cyclic sense disabled.
93. Total I_{DD} current (including loads) below 100 µA.
94. Stop and Sleep modes current increases if V_{SUP} exceeds 13.5 V.
95. This parameter is guaranteed by process monitoring but not production tested.
96. The Flag is set during power up sequence. To clear the flag, a SPI read must be performed.

Table 35. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33912 and -40 °C ≤ T_A ≤ 85 °C for the 34912, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Voltage regulator[97] (VDD)						
V_{DDRUN}	Normal Mode Output Voltage • 1.0 mA < I_{VDD} < 50 mA; 5.5 V < V_{SUP} < 27 V	4.75	5.00	5.25	V	
I_{VDDRUN}	Normal Mode Output Current Limitation	60	110	200	mA	
V_{DDDROP}	Dropout Voltage • I_{VDD} = 50 mA	–	0.1	0.25	V	(98)
V_{DDSTOP}	Stop Mode Output Voltage • I_{VDD} < 5.0 mA	4.75	5.0	5.25	V	
$I_{VDDSTOP}$	Stop Mode Output Current Limitation	6.0	12	36	mA	
LR_{RUN} LR_{STOP}	Line Regulation • Normal mode, 5.5 V < V_{SUP} < 18 V; I_{VDD} = 10 mA • Stop mode, 5.5 V < V_{SUP} < 18 V; I_{VDD} = 1.0 mA	 – –	 20 5.0	 25 25	mV	
LD_{RUN} LD_{STOP}	Load Regulation • Normal mode, 1.0 mA < I_{VDD} < 50 mA • Stop mode, 0.1 mA < I_{VDD} < 5.0 mA	 – –	 15 10	 80 50	mV	
T_{PRE}	Overtemperature Prewarning (Junction) • Interrupt generated, VDDOT Bit Set	110	125	140	°C	(99)
T_{PRE_HYS}	Overtemperature Prewarning Hysteresis	–	10	–	°C	(99)
T_{SD}	Overtemperature Shutdown Temperature (Junction)	155	170	185	°C	(99)
T_{SD_HYS}	Overtemperature Shutdown Hysteresis	–	10	–	°C	(99)
Hall sensor supply output [100] (HVDD)						
H_{VDDACC}	V_{DD} Voltage matching H_{VDDACC} = (H_{VDD}-V_{DD}) / V_{DD} * 100% • I_{HVDD} = 15 mA	-2.0	–	2.0	%	
I_{HVDD}	Current Limitation	20	30	50	mA	
$H_{VDDDROP}$	Dropout Voltage • I_{HVDD} = 15 mA; I_{VDD} = 5.0 mA	–	160	300	mV	
LR_{HVDD}	Line Regulation • I_{HVDD} = 5.0 mA; I_{VDD} = 5.0 mA	–	25	40	mV	
LD_{HVDD}	Load Regulation • 1.0 mA > I_{HVDD} > 15 mA; I_{VDD} = 5.0 mA	–	10	20	mV	

Notes

97. Specification with external capacitor 2.0 µF < C < 100 µF and 100 mΩ ≤ ESR ≤ 10 Ω.
98. Measured when voltage has dropped 250 mV below its nominal Value (5.0 V).
99. This parameter is guaranteed by process monitoring but not production tested.
100. Specification with external capacitor 1.0 µF < C < 10 µF and 100 mΩ ≤ ESR ≤ 10 Ω.

Table 35. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33912 and -40 °C ≤ T_A ≤ 85 °C for the 34912, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
$\overline{RST}$ input/output pin ($\overline{RST}$)						
$V_{\overline{RST}TH}$	VDD Low Voltage Reset Threshold	4.3	4.5	4.7	V	
V_{OL}	Low-state Output Voltage • I_{OUT} = 1.5 mA; 3.5 V ≤ V_{SUP} ≤ 27 V	0.0	–	0.9	V	
I_{OH}	High-state Output Current (0 < V_{OUT} < 3.5 V)	-150	-250	-350	µA	
I_{PD_MAX}	Pull-down Current Limitation (internally limited) V_{OUT} = V_{DD}	1.5	–	8.0	mA	
V_{IL}	Low-state Input Voltage	-0.3	–	0.3 x V_{DD}	V	
V_{IH}	High-state Input Voltage	0.7 x V_{DD}	–	V_{DD} +0.3	V	
MISO SPI output pin (MISO)						
V_{OL}	Low-state Output Voltage • I_{OUT} = 1.5 mA	0.0	–	1.0	V	
V_{OH}	High-state Output Voltage • I_{OUT} = -250 µA	V_{DD} -0.9	–	V_{DD}	V	
$I_{TRIMISO}$	Tri-state Leakage Current • 0 V ≤ V_{MISO} ≤ V_{DD}	-10	–	10	µA	
SPI input pins (MOSI, SCLK, $\overline{CS}$)						
V_{IL}	Low-state Input Voltage	-0.3	–	0.3 x V_{DD}	V	
V_{IH}	High-state Input Voltage	0.7 x V_{DD}	–	V_{DD} +0.3	V	
I_{IN}	MOSI, SCLK Input Current • 0 V ≤ V_{IN} ≤ V_{DD}	-10	–	10	µA	
$I_{PU\overline{CS}}$	$\overline{CS}$ Pull-up Current • 0 V < V_{IN} < 3.5 V	10	20	30	µA	
Interrupt output pin ($\overline{IRQ}$)						
V_{OL}	Low-state Output Voltage • I_{OUT} = 1.5 mA	0.0	–	0.8	V	
V_{OH}	High-state Output Voltage • I_{OUT} = -250 µA	V_{DD} -0.8	–	V_{DD}	V	
V_{OH}	Leakage Current • V_{DD} ≤ V_{OUT} ≤ 10 V	–	–	2.0	mA	
Pulse width modulation input pin (PWMIN)						
V_{IL}	Low-state Input Voltage	-0.3	–	0.3 x V_{DD}	V	
V_{IH}	High-state Input Voltage	0.7 x V_{DD}	–	V_{DD} +0.3	V	
$I_{PUPWMIN}$	Pull-up current • 0 V < V_{IN} < 3.5 V	10	20	30	µA	

Table 35. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33912 and -40 °C ≤ T_A ≤ 85 °C for the 34912, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
High-side output HS1 and HS2 pins (HS1, HS2)						
$R_{DS(on)}$	Output Drain-to-Source On Resistance • T_J = 25 °C, I_{LOAD} = 50 mA; V_{SUP} > 9.0 V • T_J = 150 °C, I_{LOAD} = 50 mA; V_{SUP} > 9.0 V • T_J = 150 °C, I_{LOAD} = 30 mA; 5.5 V < V_{SUP} < 9.0 V	– – –	– – –	7.0 10 14	Ω	(101)
I_{LIMHSX}	Output Current Limitation • 0 V < V_{OUT} < V_{SUP} - 2.0 V	60	120	250	mA	(102)
I_{OLHSX}	Open Load Current Detection	–	5.0	7.5	mA	(103)
I_{LEAK}	Leakage Current • -0.2 V < V_{HSX} < V_{S2} + 0.2 V	–	–	10	µA	
V_{THSC}	Short-circuit Detection Threshold • 5.5 V < V_{SUP} < 27 V	V_{SUP} -2.0	–	–	V	(104)
T_{HSSD}	Overtemperature Shutdown	150	165	180	°C	(105), (106)
T_{HSSD_HYS}	Overtemperature Shutdown Hysteresis	–	10	–	°C	(106)
Low-side output LS1 and LS2 pins (LS1, LS2)						
$R_{DS(on)}$	Output Drain-to-Source On Resistance • T_J = 25 °C, I_{LOAD} = 150 mA, V_{SUP} > 9.0 V • T_J = 125 °C, I_{LOAD} = 150 mA, V_{SUP} > 9.0 V • T_J = 125 °C, I_{LOAD} = 120 mA, 5.5 V < V_{SUP} < 9.0 V	– – –	– – –	2.5 4.5 10	Ω	
I_{LIMLSX}	Output Current Limitation • 2.0 V < V_{OUT} < V_{SUP}	160	275	350	mA	(107)
I_{OLLSX}	Open Load Current Detection	–	8.0	12	mA	(108)
I_{LEAK}	Leakage Current • -0.2 V < V_{OUT} < VS1	–	–	10	µA	
V_{CLAMP}	Active Output Energy Clamp • I_{OUT} = 150 mA	V_{SUP} +2.0	–	V_{SUP} +5.0	V	
V_{THSC}	Short-circuit Detection Threshold • 5.5 V < V_{SUP} < 27 V	2.0	–	–	V	(109)
T_{LSSD}	Overtemperature Shutdown	150	165	180	°C	(110), (106)
T_{LSSD_HYS}	Overtemperature Shutdown Hysteresis	–	10	–	°C	(106)

Notes

101. This parameter is production tested up to T_A = 125 °C and guaranteed by process monitoring up to T_J = 150 °C.
102. When overcurrent occurs, the corresponding high-side stays ON with limited current capability and the HSxCL flag is set in the HSSR.
103. When open load occurs, the flag (HSxOP) is set in the HSSR.
104. When short-circuit occurs and if HVSE flag is enabled, both HS automatic shutdown.
105. When overtemperature shutdown occurs, both high-sides are turned off. All flags in HSSR are set.
106. Guaranteed by characterization but not production tested
107. When overcurrent occurs, the corresponding low-side stays ON with limited current capability and the LSxCL flag is set in the LSSR.
108. When open load occurs, the flag (LSxOP) is set in the LSSR.
109. When short-circuit occurs and if HVSE Flag is enabled, both LS automatic shutdown
110. When overtemperature shutdown occurs, both low-sides are turned off. All flags in LSSR are set.

Table 35. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33912 and -40 °C ≤ T_A ≤ 85 °C for the 34912, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
L1, L2, L3, and L4 input pins (L1, L2, L3, L4)						
V_{THL}	Low Detection Threshold • 5.5 V < V_{SUP} < 27 V	2.0	2.5	3.0	V	
V_{THH}	High Detection Threshold • 5.5 V < V_{SUP} < 27 V	3.0	3.5	4.0	V	
V_{HYS}	Hysteresis • 5.5 V < V_{SUP} < 27 V	0.5	1.0	1.5	V	
I_{IN}	Input Current • -0.2 V < V_{IN} < VS1	-10	–	10	µA	(111)
R_{LXIN}	Analog Input Impedance	800	1550	–	kΩ	(112)
$RATIO_{LX}$	Analog Input Divider Ratio ($RATIO_{Lx}$ = V_{Lx} / V_{ADOUT0}) • LXDS (Lx Divider Select) = 0 • LXDS (Lx Divider Select) = 1	 0.95 3.42	 1.0 3.6	 1.05 3.78		
$V_{RATIOLx-OFFSET}$	Analog Output offset Ratio • LXDS (Lx Divider Select) = 0 • LXDS (Lx Divider Select) = 1	 -80 -22	 0.0 0.0	 80 22	mV	
$LX_{MATCHING}$	Analog Inputs Matching • LXDS (Lx Divider Select) = 0 • LXDS (Lx Divider Select) = 1	 96 96	 100 100	 104 104	%	
Window watchdog configuration pin (WDCONF)						
R_{EXT}	External Resistor Range	20	–	200	kΩ	
WD_{ACC}	Watchdog Period Accuracy with External Resistor (Excluding Resistor Accuracy)	-15	–	15	%	(113)
Analog multiplexer						
S_{TTOV}	Internal Chip Temperature Sense Gain	–	10.5	–	mV/K	
$RATIO_{VSENSE}$	VSENSE Input Divider Ratio ($RATIO_{VSENSE}$ = V_{VSENSE} / V_{ADOUT0}) • 5.5 V < V_{SUP} < 27 V	5.0	5.25	5.5		
$OFFSET_{VSENSE}$	VSENSE Output Related Offset • -40 °C < T_A < -20 °C	-30 -45	– –	30 45	mV	
Analog outputs (ADOUT0 and ADOUT1)						
V_{OUT_MAX}	Maximum Output Voltage • -5.0 mA < I_O < 5.0 mA	V_{DD} -0.35	–	V_{DD}	V	
V_{OUT_MIN}	Minimum Output Voltage • -5.0 mA < I_O < 5.0 mA	0.0	–	0.35	V	

Notes

111. Analog multiplexer input disconnected from Lx input pin.
112. Analog multiplexer input connected to Lx input pin.
113. Watchdog timing period calculation formula: t_{PWD} [ms] = 0.466 * (R_{EXT} - 20) + 10 (R_{EXT} in kΩ)

Table 35. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33912 and -40 °C ≤ T_A ≤ 85 °C for the 34912, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Current sense amplifier (ISENSEH, ISENSEL)						
G	Gain • CSGS (Current Sense Gain Select) = 0 • CSGS (Current Sense Gain Select) = 1	 29 14	 30 14.5	 31 15		
DIFF	Differential Input Impedance • CSGS (Current Sense Gain Select) = 0 • CSGS (Current Sense Gain Select) = 1	 2.0 5.0	 10 20	 30 50	kΩ	
CM	Common Mode Input Impedance • CSGS (Current Sense Gain Select) = 0 • CSGS (Current Sense Gain Select) = 1	 75 75	 – –	 300 300	kΩ	
V_{IN}	ISENSEH, ISENSEL Input Voltage Range	-0.2	–	3.0	V	
V_{IN_OFFSET}	Input Offset Voltage • CSAZ (Current Sense Auto Zero) = 0 • CSAZ (Current Sense Auto Zero) = 1	 -15 -2.0	 – –	 15 2.0	mV	
RxD output pin (LIN physical layer) (RxD)						
V_{OL}	Low-state Output Voltage • I_{OUT} = 1.5 mA	0.0	–	0.8	V	
V_{OH}	High-state Output Voltage • I_{OUT} = -250 µA	V_{DD} -0.8	–	V_{DD}	V	
TXD input pin (LIN physical layer) (TXD)						
V_{IL}	Low-state Input Voltage	-0.3	–	0.3 x V_{DD}	V	
V_{IH}	High-state Input Voltage	0.7 x V_{DD}	–	V_{DD} +0.3	V	
I_{PUIN}	Pin Pull-up Current, 0 V < V_{IN} < 3.5 V	10	20	30	µA	

Table 35. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33912 and -40 °C ≤ T_A ≤ 85 °C for the 34912, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
LIN physical layer, transceiver (LIN)(114)						
I_{BUSLIM}	Output Current Limitation • Dominant State, V_{BUS} = 18 V	40	120	200	mA	
	Leakage Output Current to GND					
$I_{BUS\_PAS\_DOM}$	• Dominant State; V_{BUS} = 0 V; V_{BAT} = 12 V	-1.0	–	–	mA	
$I_{BUS\_PAS\_REC}$	• Recessive State; 8.0 V < V_{BAT} < 18 V; 8.0 V < V_{BUS} < 18 V; V_{BUS} ≥ V_{BAT}	–	–	20	µA	
$I_{BUS\_NO\_GND}$	• GND Disconnected; GND_{DEVICE} = V_{SUP}; V_{BAT} = 12 V; 0 < V_{BUS} < 18 V	-1.0	–	1.0	mA	
I_{BUS}	• V_{BAT} Disconnected; V_{SUP_DEVICE} = GND; 0 < V_{BUS} < 18 V	–	–	100	µA	
	Receiver Input Voltages					
V_{BUSDOM}	• Receiver Dominant State	–	–	0.4	V_{SUP}	
V_{BUSREC}	• Receiver Recessive State	0.6	–	–		
V_{BUS_CNT}	• Receiver Threshold Center (V_{TH_DOM} + V_{TH_REC})/2	0.475	0.5	0.525		
V_{HYS}	• Receiver Threshold Hysteresis (V_{TH_REC} - V_{TH_DOM})	–	–	0.175		
	LIN Transceiver Output Voltage					
V_{LIN_REC}	• Recessive State, TXD HIGH, I_{OUT} = 1.0 µA	V_{SUP} -1.0	–	–	V	
$V_{LIN\_DOM\_0}$	• Dominant State, TXD LOW, 500 Ω External Pull-up Resistor, LDVS = 0	–	1.1	1.4		
$V_{LIN\_DOM\_1}$	• Dominant State, TXD LOW, 500 Ω External Pull-up Resistor, LDVS = 1	–	1.7	2.0		
R_{SLAVE}	LIN Pull-up Resistor to V_{SUP}	20	30	60	kΩ	
T_{LINSD}	Overtemperature Shutdown	150	165	180	°C	(115)
T_{LINSD_HYS}	Overtemperature Shutdown Hysteresis	–	10	–	°C	

Notes

114. Parameters guaranteed for 7.0 V ≤ V_{SUP} ≤ 18 V.

115. When overtemperature shutdown occurs, the LIN bus goes in recessive state and the flag LINOT in LINSR is set.

12.3 Dynamic electrical characteristics

Table 36. Dynamic electrical characteristics

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33912 and -40 °C ≤ T_A ≤ 85 °C for the 34912, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
SPI interface timing (see Figure 36)						
f_{SPIOP}	SPI Operating Frequency	–	–	4.0	MHz	
t_{PSCLK}	SCLK Clock Period	250	–	N/A	ns	
t_{WSCLKH}	SCLK Clock High Time	110	–	N/A	ns	(116)
t_{WSCLKL}	SCLK Clock Low Time	110	–	N/A	ns	(116)
t_{LEAD}	Falling Edge of $\overline{CS}$ to Rising Edge of SCLK	100	–	N/A	ns	(116)
t_{LAG}	Falling Edge of SCLK to $\overline{CS}$ Rising Edge	100	–	N/A	ns	(116)
t_{SISU}	MOSI to Falling Edge of SCLK	40	–	N/A	ns	(116)
t_{SIH}	Falling Edge of SCLK to MOSI	40	–	N/A	ns	(116)
t_{RSO}	MISO Rise Time • C_L = 220 pF	–	40	–	ns	(116)
t_{FSO}	MISO Fall Time • C_L = 220 pF	–	40	–	ns	(116)
t_{SOEN} t_{SODIS}	Time from Falling or Rising Edges of $\overline{CS}$ to: • MISO Low-impedance • MISO High-impedance	 0.0 0.0	 – –	 50 50	ns	(116)
t_{VALID}	Time from Rising Edge of SCLK to MISO Data Valid(116) • 0.2 x V_{DD} ≤ MISO ≥ 0.8 x V_{DD}, C_L = 100 pF	0.0	–	75	ns	(116)
$\overline{RST}$ output pin						
$t_{\overline{RST}}$	Reset Low-level Duration After V_{DD} High (see Figure 35)	0.65	1.0	1.35	ms	
$t_{\overline{RSTDF}}$	Reset Deglitch Filter Time	350	600	900	ns	
Window watchdog configuration pin (WDCONF)						
t_{PWD}	Watchdog Time Period • External Resistor R_{EXT} = 20 kΩ (1%) • External Resistor R_{EXT} = 200 kΩ (1%) • Without External Resistor R_{EXT} (WDCONF Pin Open)	 8.5 79 110	 10 94 150	 11.5 108 205	ms	(117)
Current sense amplifier (116)						
CMR	Common Mode Rejection Ratio	70	–	–	dB	
SVR	Supply Voltage Rejection Ratio	60	–	–	dB	(118)
GBP	Gain Bandwidth Product	0.75	3.0	–	MHz	
SR	Output Slew-rate	0.5	–	–	V/µs	

Notes

116. This parameter is guaranteed by process monitoring but not production tested.
117. Watchdog timing period calculation formula: t_{PWD} [ms] = 0.466 * (R_{EXT} - 20) + 10 (R_{EXT} in kΩ)
118. Analog Outputs are supplied by V_{DD}

Table 36. Dynamic electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33912 and -40 °C ≤ T_A ≤ 85 °C for the 34912, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
L1, L2, L3, and L4 inputs						
t_{WUF}	Wake-up Filter Time	8.0	20	38	µs	
State machine timing						
t_{STOP}	Delay Between $\overline{CS}$ LOW-to-HIGH Transition (at End of SPI Stop Command) and Stop mode Activation	–	–	5.0	µs	(119)
t_{NRTOUT}	Normal Request Mode Timeout (see Figure 35)	110	150	205	ms	
$t_{S\text{-}ON}$	Delay Between SPI Command and HS/LS Turn On • 9.0 V < V_{SUP} < 27 V	–	–	10	µs	(120)
$t_{S\text{-}OFF}$	Delay Between SPI Command and HS/LS Turn Off • 9.0 V < V_{SUP} < 27 V	–	–	10	µs	(120)
t_{SNR2N}	Delay Between Normal Request and Normal Mode After a Watchdog Trigger Command (Normal Request Mode)	–	–	10	µs	(119)
$t_{WU\overline{CS}}$ t_{WUSPI}	Delay Between $\overline{CS}$ Wake-up ($\overline{CS}$ LOW to HIGH) in Stop mode and: • Normal Request mode, VDD ON and $\overline{RST}$ HIGH • First Accepted SPI Command	9.0 90	15 —	80 N/A	µs	
$t_{2\overline{CS}}$	Minimum Time Between Rising and Falling Edge on the $\overline{CS}$	4.0	—	—	µs	
LIN physical layer: driver characteristics for normal slew rate - 20.0 kBit/sec (121), (122)						
D1	Duty Cycle 1: D1 = $t_{BUS\_REC(MIN)}$/(2 x t_{BIT}), t_{BIT} = 50 µs • 7.0 V ≤ V_{SUP} ≤ 18 V	0.396	—	—		
D2	Duty Cycle 2: D2 = $t_{BUS\_REC(MAX)}$/(2 x t_{BIT}), t_{BIT} = 50 µs • 7.6 V ≤ V_{SUP} ≤ 18 V	—	—	0.581		
LIN physical layer: driver characteristics for slow slew rate - 10.4 kBit/sec (121), (123)						
D3	Duty Cycle 3: D3 = $t_{BUS\_REC(MIN)}$/(2 x t_{BIT}), t_{BIT} = 96 µs • 7.0 V ≤ V_{SUP} ≤ 18 V	0.417	—	—	µs	
D4	Duty Cycle 4: D4 = $t_{BUS\_REC(MAX)}$/(2 x t_{BIT}), t_{BIT} = 96µs • 7.6 V ≤ V_{SUP} ≤ 18 V	—	—	0.590	µs	

Notes

119. This parameter is guaranteed by process monitoring but not production tested.
120. Delay between turn on or off command (rising edge on $\overline{CS}$) and HS or LS ON or OFF, excluding rise or fall time due to external load.
121. Bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 kΩ, 6.8 nF / 660 Ω, 10 nF / 500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 29.
122. See Figure 30.
123. See Figure 31.

Table 36. Dynamic electrical characteristics (continued)

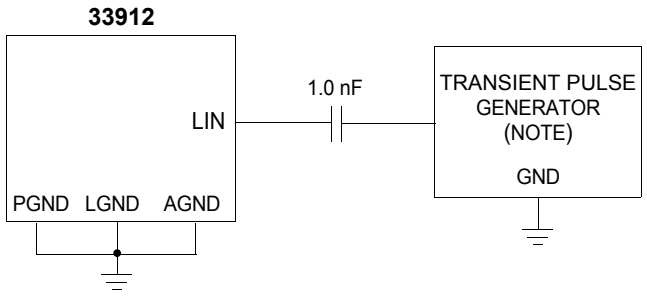
Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33912 and -40 °C ≤ T_A ≤ 85 °C for the 34912, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
LIN physical layer: driver characteristics for fast slew rate						
SR_{FAST}	LIN Fast Slew Rate (Programming mode)	—	20	—	V/µs	
LIN physical layer: characteristics and wake-up timings (124)						
t_{REC_PD} t_{REC_SYM}	Propagation Delay and Symmetry • Propagation Delay Receiver, t_{REC_PD} = MAX (t_{REC_PDR}, t_{REC_PDF}) • Symmetry of Receiver Propagation Delay t_{REC_PDF} - t_{REC_PDR}	— -2.0	3.0 —	6.0 2.0	µs	(125)
t_{PROPWL}	Bus Wake-up Deglitcher (Sleep and Stop modes)	42	70	95	µs	(126)
t_{WAKE} t_{WAKE}	Bus Wake-up Event Reported • From Sleep mode • From Stop mode	— 9.0	— 13	1500 17	µs	(127) (128)
t_{TXDDOM}	TXD Permanent Dominant State Delay	0.65	1.0	1.35	s	
Pulse width modulation input pin (PWMIN)						
f_{PWMIN}	PWMIN pin • Max. frequency to drive HS and LS output pins	-	10	-	kHz	(129)

Notes

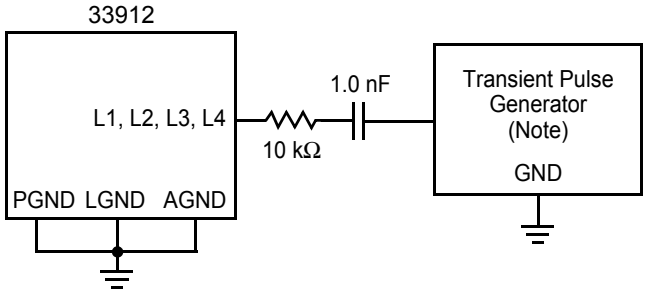
124. V_{SUP} from 7.0 V to 18 V, bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 kΩ, 6.8 nF / 660 Ω, 10 nF / 500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 29.
125. See Figure 32.
126. See Figure 33 for Sleep and Figure 34 for Stop mode.
127. The measurement is done with 1µF capacitor and 0 mA current load on V_{DD}. The value takes into account the delay to charge the capacitor. The delay is measured between the bus wake-up threshold (V_{BUSWU}) rising edge of the LIN bus and when V_{DD} reaches 3.0 V. See Figure 33. The delay depends of the load and capacitor on V_{DD}.
128. In Stop mode, the delay is measured between the bus wake-up threshold (V_{BUSWU}) and the falling edge of the $\overline{IRQ}$ pin. See Figure 34.
129. This parameter is guaranteed by process monitoring but not production tested.

12.4 Timing diagrams



Note Waveform per ISO 7637-2. Test Pulses 1, 2, 3a, 3b.

Figure 27. Test circuit for transient test pulses (LIN)



Note Waveform per ISO 7637-2. Test Pulses 1, 2, 3a, 3b,.

Figure 28. Test circuit for transient test pulses (Lx)

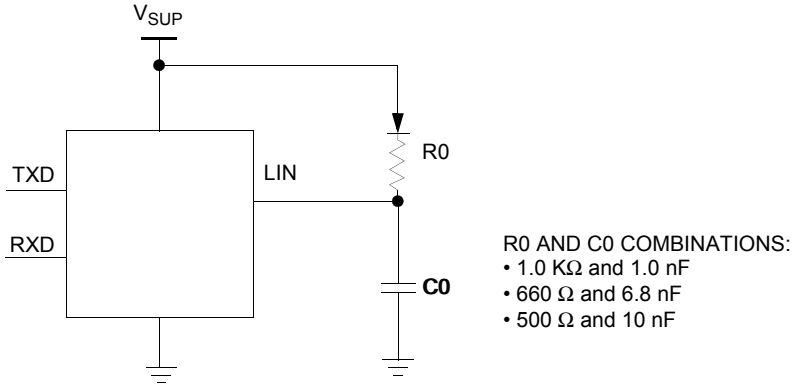


Figure 29. Test circuit for LIN timing measurements

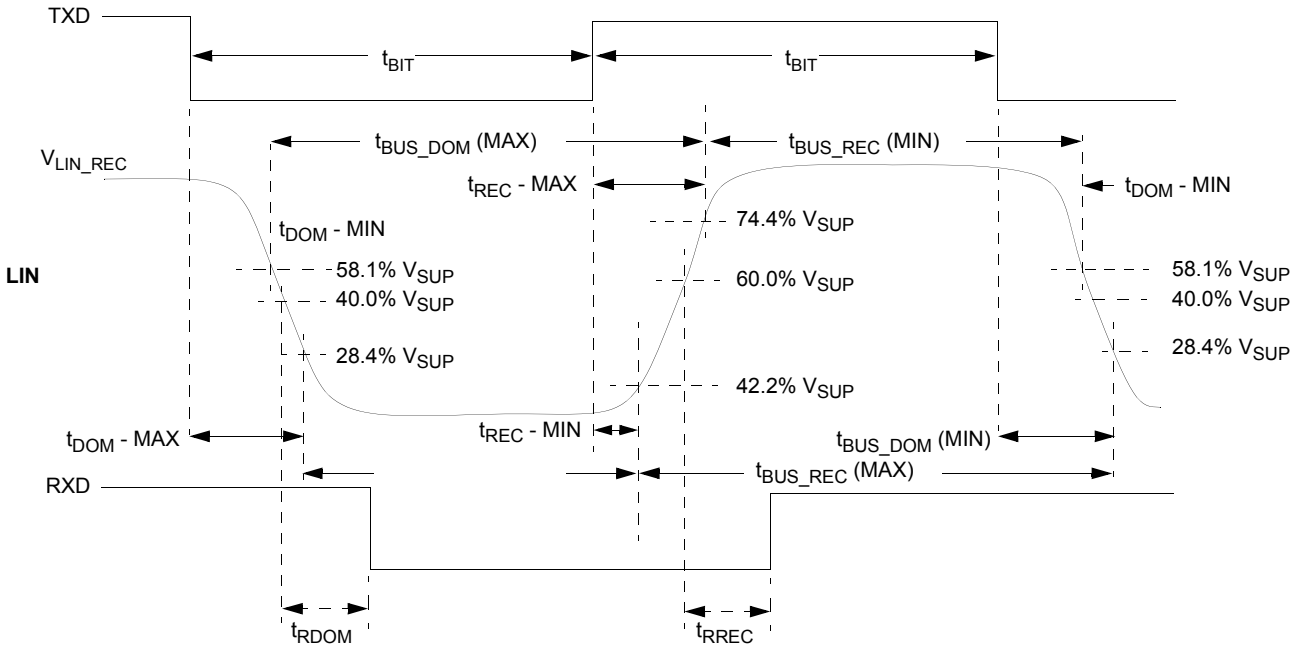


Figure 30. LIN timing measurements for normal slew rate

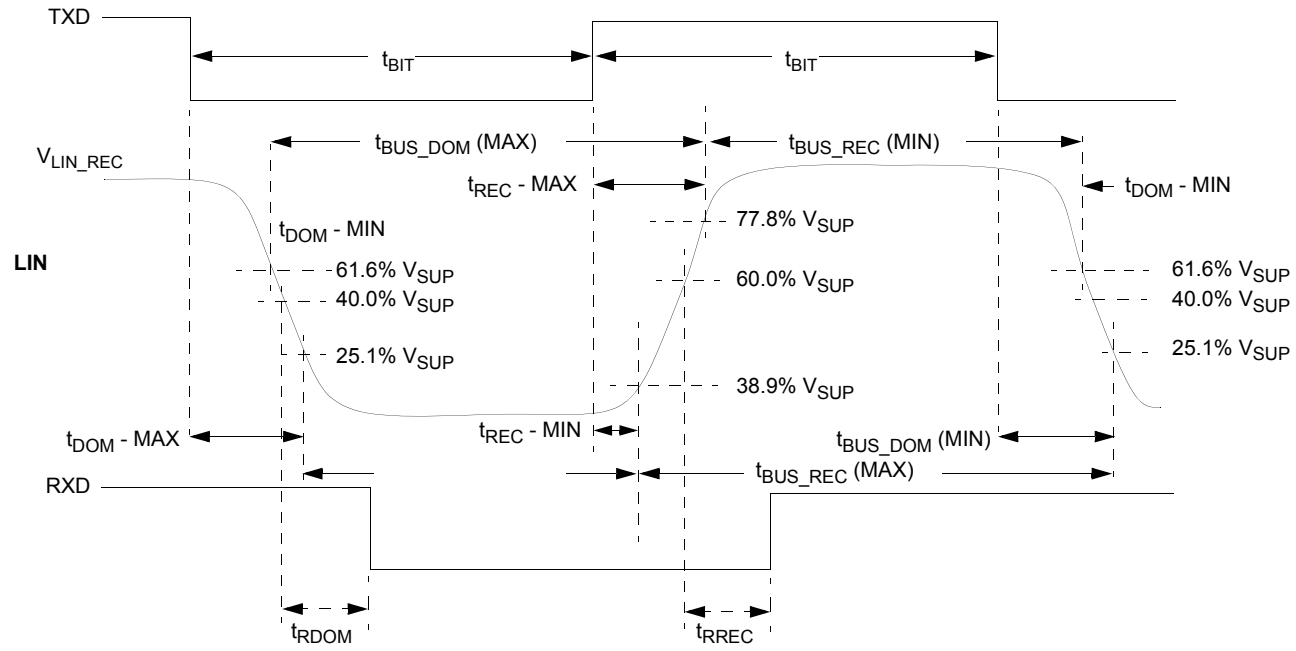


Figure 31. LIN timing measurements for slow slew rate

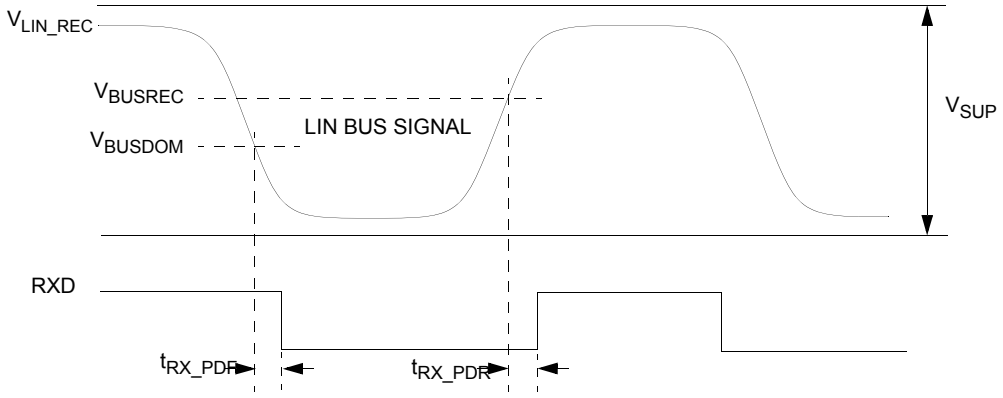


Figure 32. LIN receiver timing

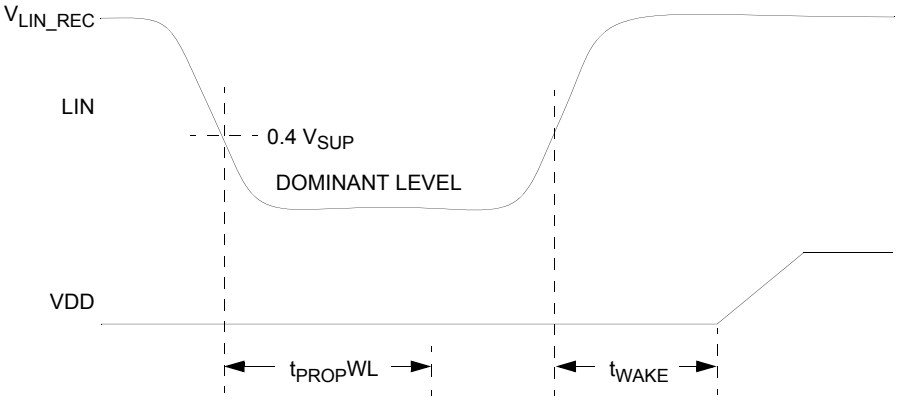


Figure 33. LIN wake-up sleep mode timing

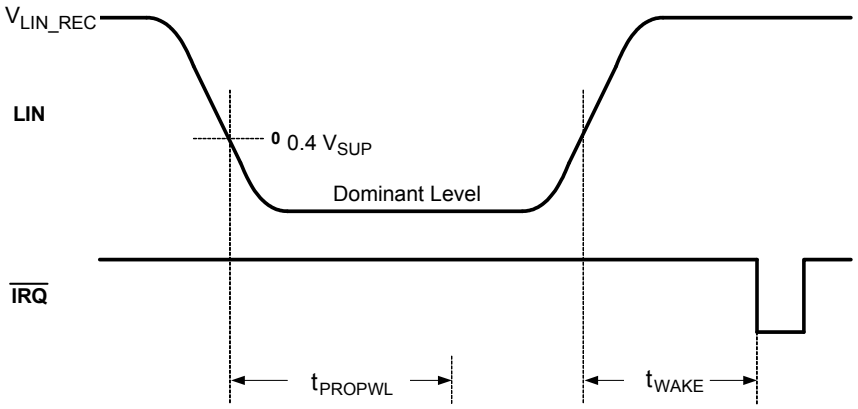


Figure 34. LIN wake-up stop mode timing

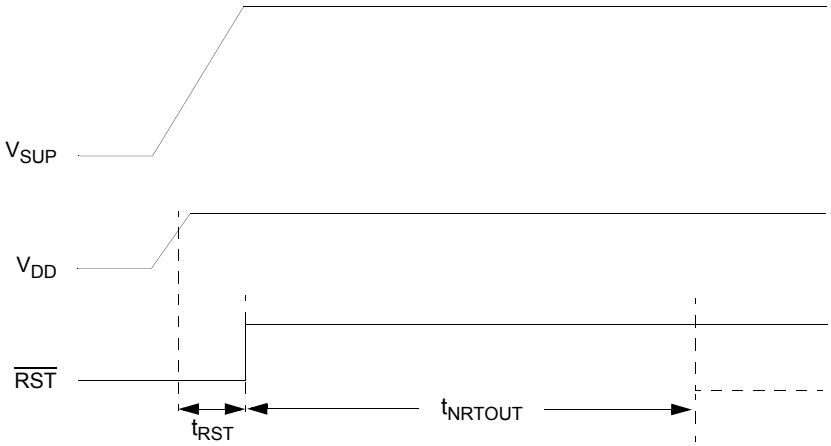


Figure 35. Power on reset and normal request timeout timing

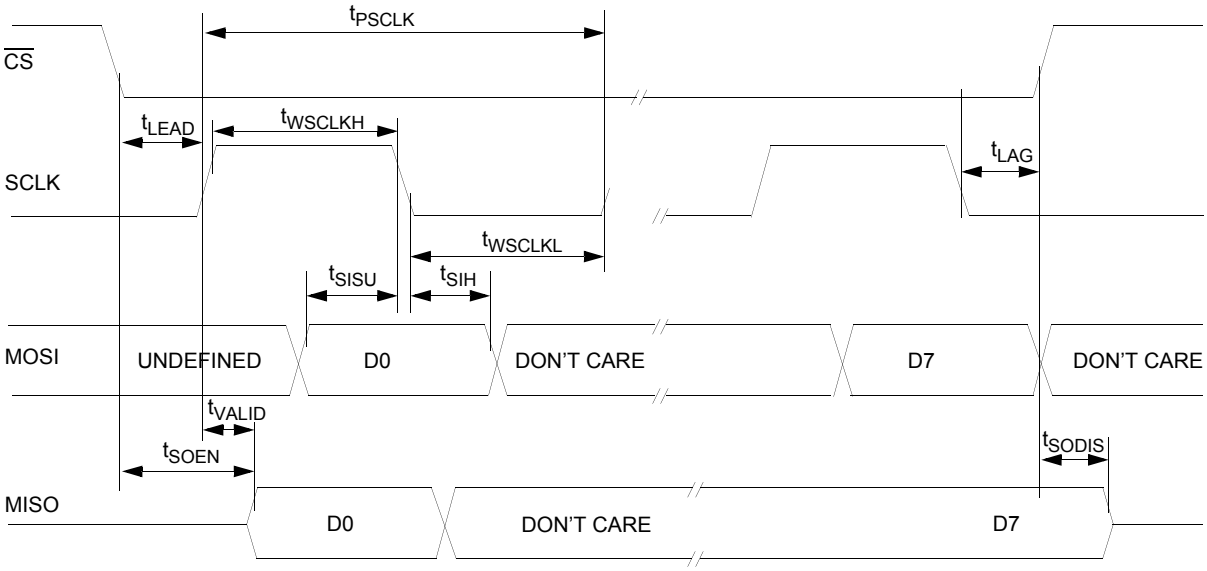


Figure 36. SPI timing characteristics

13 Functional description

13.1 Introduction

The 33912 was designed and developed as a highly integrated and cost-effective solution for automotive and industrial applications. The 33912 is well suited to perform relay control in applications like window lift, sunroof, etc. via LIN bus, for automotive body electronics.

Power switches are provided on the device configured as high-side and low-side outputs. Other ports are also provided, which include a current and voltage sense port, a Hall Sensor port supply, and four wake-up capable pins. An internal voltage regulator provides power to a MCU device.

Also included in this device is a LIN physical layer, which communicates using a single wire. This enables this device to be compatible with 3-wire bus systems, where one wire is used for communication, one for battery, and one for ground.

13.2 Functional pin description

See Figure 1, 33912 simplified application diagram, for a graphic representation of the various pins referred to in the following paragraphs. Also, see the pin diagram on page 55 for a description of the pin locations in the package.

13.2.1 Receiver output pin (RxD)

The RXD pin is a digital output. It is the receiver output of the LIN interface and reports the state of the bus voltage: RXD Low when LIN bus is dominant, RXD High when LIN bus is recessive.

13.2.2 Transmitter input pin (TXD)

The TXD pin is a digital input. It is the transmitter input of the LIN interface and controls the state of the bus output (dominant when TXD is Low, recessive when TXD is High). This pin has an internal pull-up to force recessive state in case the input is left floating.

13.2.3 LIN bus pin (LIN)

The LIN pin represents the single-wire bus transmitter and receiver. It is suited for automotive bus systems and is compliant to the LIN bus specification 2.0. The LIN interface is only active during Normal and Normal Request modes.

13.2.4 Serial data clock pin (SCLK)

The SCLK pin is the SPI clock input pin. MISO data changes on the negative transition of the SCLK. MOSI is sampled on the positive edge of the SCLK.

13.2.5 Master out slave in pin (MOSI)

The MOSI digital pin receives SPI data from the MCU. This data input is sampled on the positive edge of SCLK.

13.2.6 Master in slave out pin (MISO)

The MISO pin sends data to a SPI-enabled MCU. It is a digital tri-state output used to shift serial data to the microcontroller. Data on this output pin changes on the negative edge of the SCLK. When $\overline{CS}$ is High, this pin remains in high-impedance state.

13.2.7 Chip select pin ($\overline{CS}$)

$\overline{CS}$ is an active low digital input. It must remain low during a valid SPI communication and allow for several devices to be connected in the same SPI bus without contention. A rising edge on $\overline{CS}$ signals the end of the transmission and the moment the data shifted in is latched. A valid transmission must consist of 8 bits only. While in STOP mode, a low-to-high level transition on this pin generates a wake-up condition for the 33912.

13.2.8 Analog multiplexer pin (ADOUT0)

The ADOUT0 pin can be configured via the SPI to allow the MCU A/D converter to read the several inputs of the Analog Multiplexer, including the VSENSE, L1, L2, L3, L4 input voltages, and the internal junction temperature.

13.2.9 Current sense amplifier pin (ADOUT1)

The ADOUT1 pin is an analog interface to the MCU A/D converter. It allows the MCU to read the output of the current sense amplifier.

13.2.10 PWM input control pin (PWMIN)

This digital input can control the high-sides and low-sides drivers in Normal Request- and Normal mode. To enable PWM control, the MCU must perform a write operation to the High-side Control register (HSCR) or the Low-side Control register (LSCR). This pin has an internal 20 μA current pull-up.

13.2.11 Reset pin ($\overline{\text{RST}}$)

This bidirectional pin is used to reset the MCU in case the 33912 detects a reset condition, or to inform the 33912 the MCU has just been reset. After release of the $\overline{\text{RST}}$ pin, Normal Request mode is entered. The $\overline{\text{RST}}$ pin is an active low filtered input and output formed by a weak pull-up and a switchable pull-down structure which allows this pin to be shorted either to V_{DD} or to GND during software development, without the risk of destroying the driver.

13.2.12 Interrupt pin ($\overline{\text{IRQ}}$)

The $\overline{\text{IRQ}}$ pin is a digital output used to signal events or faults to the MCU while in Normal and Normal Request mode or to signal a wake-up from Stop mode. This active low output transitions to high only after the interrupt is acknowledged by a SPI read of the respective status bits.

13.2.13 Watchdog configuration pin (WDConf)

The WDCONF pin is the configuration pin for the internal watchdog. A resistor can be connected to this pin to configure the window watchdog period. When connected directly to ground, the watchdog is disabled. When this pin is left open, the watchdog period is fixed to its lower precision internal default value (150 ms typical).

13.2.14 Ground connection pins (AGND, PGND, LGND)

The AGND, PGND and LGND pins are the Analog and Power ground pins. The AGND pin is the ground reference of the voltage regulator and the current sense module. The PGND and LGND pins are used for high current load return as in the relay-drivers and LIN interface pin.

Note: PGND, AGND and LGND pins must be connected together.

13.2.15 Current sense amplifier input pins (ISENSEH and ISENSEL)

The ISENSEH and ISENSEL pins are the input pins of a ground compatible differential amplifier designed to be used to sense the voltage drop over a shunt resistor. The main purpose of this amplifier is to implement accurate current sensors. The gain of the differential amplifier can be set by the SPI.

13.2.16 Low-side pins (LS1 and LS2)

LS1 and LS2 are the low-side driver outputs. Those outputs are short-circuit protected and include active clamp circuitry to drive inductive loads. Due to the energy clamp voltage on this pin, it can raise above the battery level when switched off. The switches are controlled through the SPI and can be configured to respond to a signal applied to the PWMIN input pin. Both low-side switches are protected against overheating.

13.2.17Digital/analog pins (L1, L2, L3, and L4)

The Lx pins are multi purpose inputs. They can be used as digital inputs, which can be sampled by reading the SPI and used for wake-up when 33912 is in Low-power mode or used as analog inputs for the analog multiplexer. When used to sense voltage outside the module, a 33 kΩ series resistor must be used on each input.

When used as wake-up inputs L1-L4 can be configured to operate in cyclic-sense mode. In this mode one of the high-side switches is configured to be periodically turned on and sample the wake-up inputs. If a state change is detected between two cycles a wake-up is initiated. The 33912 can also wake-up from Stop or Sleep by a simple state change on L1-L4.

When used as analog inputs, the voltage present on the Lx pins is scaled down by an selectable internal voltage divider and can be routed to the ADOUT0 output through the analog multiplexer.

Note: If an Lx input is selected in the analog multiplexer, it is disabled as a digital input and remains disabled in low power mode. No wake-up feature is available in this condition.

When an Lx input is not selected in the analog multiplexer, the voltage divider is disconnected from this input.

13.2.18High-side output pins (HS1 and HS2)

These two high-side switches are able to drive loads such as relays or lamps. Their structures are connected to the VS2 supply pin. The pins are short-circuit protected and both outputs are also protected against overheating. HS1 and HS2 are controlled by the SPI and can respond to a signal applied to the PWMIN input pin. HS1 and HS2 outputs can also be used during Low-power mode for the cyclic-sense of the wake inputs.

13.2.19Power supply pins (VS1 and VS2)

Those are the battery level voltage supply pins. In an application, VS1 and VS2 pins must be protected against reverse battery connection and negative transient voltages with external components. These pins sustain standard automotive voltage conditions such as a load dump at 40 V. The high-side switches (HS1 and HS2) are supplied by the VS2 pin. All other internal blocks are supplied by VS1 pin.

13.2.20Voltage sense pin (VSENSE)

This input can be connected directly to the battery line. It is protected against battery reverse connection. The voltage present in this input is scaled down by an internal voltage divider, and can be routed to the ADOUT0 output pin and used by the MCU to read the battery voltage. The ESD structure on this pin allows for excursion up to +40 V and down to -27 V, allowing this pin to be connected directly to the battery line. It is strongly recommended to connect a 10 kΩ resistor in series with this pin for protection purposes.

13.2.21Hall sensor switchable supply pin (HVDD)

This pin provides a switchable supply for external hall sensors. While in Normal mode, this current limited output can be controlled through the SPI. The HVDD pin needs to be connected to an external capacitor to stabilize the regulated output voltage.

13.2.22+5.0 V main regulator output pin (VDD)

An external capacitor has to be placed on the VDD pin to stabilize the regulated output voltage. The VDD pin is intended to supply a microcontroller. The pin is current limited against shorts to GND and overtemperature protected. During Stop mode, the voltage regulator does not operate with its full drive capabilities and the output current is limited. During Sleep mode, the regulator output is completely shutdown.

13.3 Functional internal block description

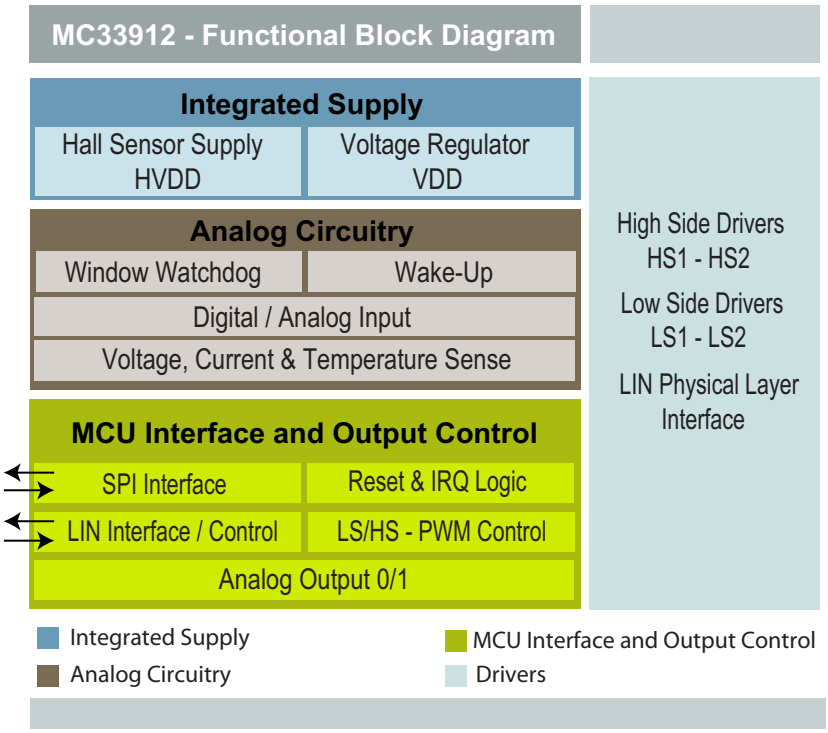


Figure 37. Functional internal block diagram

13.3.1 Analog circuitry

The 33912 is designed to operate under automotive operating conditions. A fully configurable window watchdog circuit resets the connected MCU in case of an overflow. Two low power modes are available with several different wake-up sources to reactivate the device. Four analog / digital inputs can be sensed or used as the wake-up source. The device is capable of sensing the supply voltage (VSENSE), the internal chip temperature (CTEMP) as well as the motor current using an external sense resistor.

13.3.2 High-side drivers

Two current and temperature protected high-side drivers with PWM capability are provided to drive small loads such as Status LEDs or small lamps. Both Drivers can be configured for periodic sense during Low-power modes.

13.3.3 Low-side drivers

Two current and temperature protected low-side drivers with PWM capability are provided to drive H-Bridge type relays for power motor applications

13.3.4 MCU interface

The 33912 provides its control and status information through a standard 8-Bit SPI interface. Critical system events such as Low- or High-voltage/Temperature conditions as well as overcurrent conditions in any of the driver stages can be reported to the connected MCU via IRQ or RST. Both low-side and both high-side driver outputs can be controlled via the SPI register as well as the PWMIN input. The integrated LIN physical layer interface can be configured via the SPI register and its communication is driven through the RXD and TXD device pins. All internal analog sources are multiplexed to the A_{DOUT} 0 pin. The current sense analog signal is directly routed through ADOUT1.

13.3.5 Voltage regulator outputs

Two independent voltage regulators are implemented on the 33912. The VDD main regulator output is designed to supply a MCU with a precise 5.0 V. The switchable HVDD output is dedicated to supply small peripherals as hall sensors.

13.3.6 LIN physical layer interface

The 33912 provides a LIN 2.0 compatible LIN physical layer interface with selectable slew rate and various diagnostic features.

14 Functional device operations

14.1 Operational modes

14.1.1 Introduction

The 33912 offers three main operating modes: Normal (Run), Stop, and Sleep (Low Power). In Normal mode, the device is active and is operating under normal application conditions. The Stop and Sleep modes are Low-power modes with wake-up capabilities.

In Stop mode, the voltage regulator still supplies the MCU with V_{DD} (limited current capability), while in Sleep mode the voltage regulator is turned off (V_{DD} = 0 V). Wake-up from Stop mode is initiated by a wake-up interrupt. Wake-up from Sleep mode is done by a reset and the voltage regulator is turned back on. The selection of the different modes is controlled by the MOD1:2 bits in the Mode Control register (MCR). Figure 38 describes how transitions are done between the different operating modes. Table 37 gives an overview of the operating modes.

14.1.2 Reset mode

The 33912 enters the Reset mode after a power up. In this mode, the $\overline{RST}$ pin is low for 1ms (typical value). After this delay, it enters the Normal Request mode and the $\overline{RST}$ pin is driven high. The Reset mode is entered if a reset condition occurs (V_{DD} low, watchdog trigger fail, after wake-up from Sleep mode, Normal Request mode timeout occurs).

14.1.3 Normal request mode

This is a temporary mode automatically accessed by the device after the Reset mode, or after a wake-up from Stop mode. In Normal Request mode, the VDD regulator is ON, the RESET pin is High, and the LIN is operating in RX Only mode.

As soon as the device enters in the Normal Request mode an internal timer is started for 150 ms (typical value). During these 150 ms, the MCU must configure the Timing Control register (TIMCR) and the Mode Control register (MCR) with MOD2 and MOD1 bits set = 0, to enter the Normal mode. If within the 150 ms timeout, the MCU does not command the 33912 to Normal mode, it enters in Reset mode. If the WDCONF pin is grounded, to disable the watchdog function, it goes directly in Normal mode after the Reset mode. If the WDCONF pin is open, the 33912 stays typically for 150 ms in Normal Request before entering in Normal mode.

14.1.4 Normal mode

In Normal mode, all 33912 functions are active and can be controlled by the SPI interface and the PWMIN pin. The VDD regulator is ON and delivers its full current capability. If an external resistor is connected between the WDCONF pin and the Ground, the window watchdog function is enabled.The wake-up inputs (L1-L4) can be read as digital inputs or have its voltage routed through the analog-multiplexer.

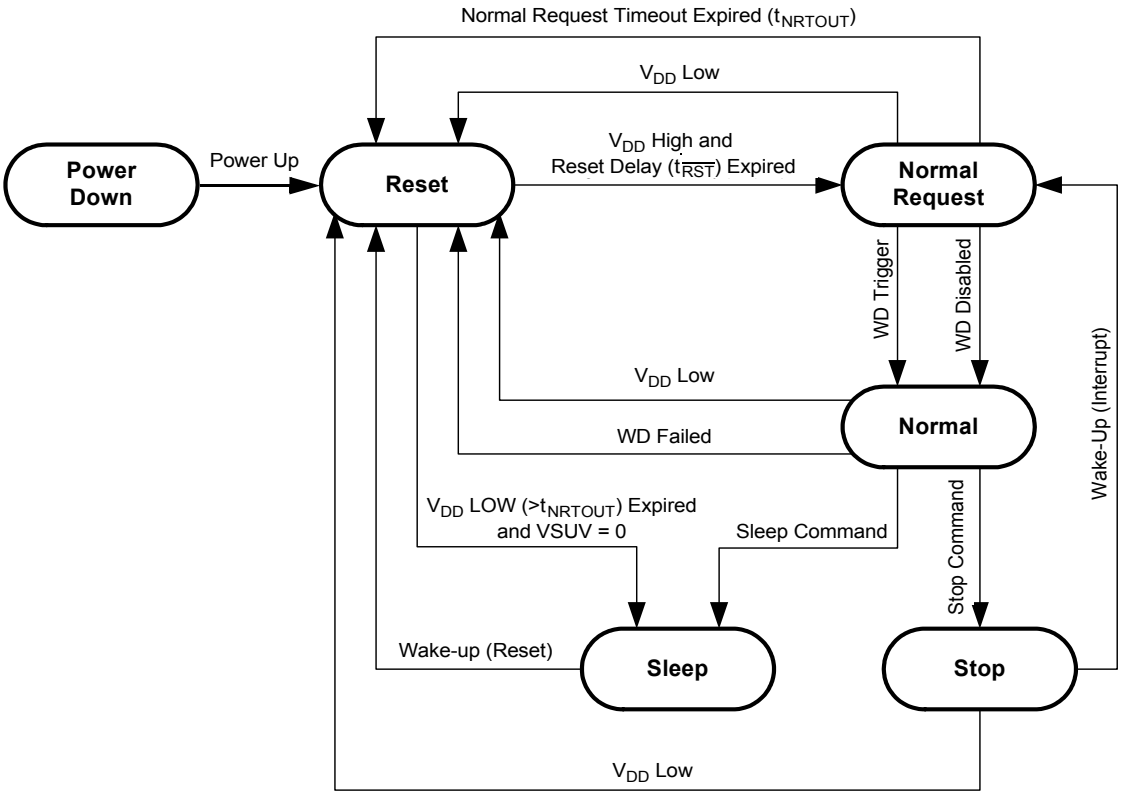
The LIN interface has slew rate and timing compatible with the LIN protocol specification 2.0. The LIN bus can transmit and receive information. The high-side and low-side switches are active and have PWM capability according to the SPI configuration. The interrupts are generated to report failures for V_{SUP} over/undervoltage, thermal shutdown, or thermal shutdown prewarning on the main regulator.

14.1.5 Sleep mode

The Sleep mode is a Low-power mode. From Normal mode, the device enters into Sleep mode by sending one SPI command through the Mode Control register (MCR). All blocks are in their lowest power consumption condition. Only some wake-up sources (wake-up inputs with or without cyclic sense, forced wake-up and LIN receiver) are active. The 5.0 V regulator is OFF. The internal low-power oscillator may be active if the IC is configured for cyclic-sense. In this condition, one of the high-side switches is turned on periodically and the wake-up inputs are sampled. Wake-up from Sleep mode is similar to a power-up. The device goes in Reset mode except the SPI reports the wake-up source and the BATFAIL flag is not set.

14.1.6 Stop mode

The Stop mode is the second Low-power mode, but in this case the 5.0 V regulator is ON with limited current drive capability. The application MCU is always supplied while the 33912 is operating in Stop mode. The device can enter into Stop mode only by sending the SPI command. When the application is in this mode, it can wake-up from the 33912 side (for example: cyclic sense, force wake-up, LIN bus, wake inputs) or the MCU side ($\overline{CS}$, $\overline{RST}$ pins). Wake-up from Stop mode transitions the 33912 to Normal Request mode and generates an interrupt except if the wake-up event is a low to high transition on the $\overline{CS}$ pin or comes from the $\overline{RST}$ pin.



Legend
WD: Watchdog
WD Disabled: Watchdog disabled (WDCONF pin connected to GND)
WD Trigger: Watchdog is triggered by a SPI command
WD Failed: No watchdog trigger or trigger occurs in closed window
Stop Command: Stop command sent via the SPI
Sleep Command: Sleep command sent via the SPI
Wake-Up from Stop Mode: L1, L2, L3 or L4 state change, LIN bus wake-up, Periodic wake-up, $\overline{CS}$ rising edge wake-up or $\overline{RST}$ wake-up.
Wake-Up from Sleep Mode: L1, L2, L3 or L4 state change, LIN bus wake-up, Periodic wake-up.

Figure 38. Operating modes and transitions

Table 37. Operating modes overview

Function	Reset mode	Normal request mode	Normal mode	Stop mode	Sleep mode
VDD	Full	Full	Full	Stop	-
HVDD	-	SPI[130]	SPI	-	-
LSx	-	SPI/PWM[131]	SPI/PWM	-	-
HSx	-	SPI/PWM[131]	SPI/PWM	Note[132]	Note[133]
Analog Mux	-	SPI	SPI	-	-
Lx	-	Inputs	Inputs	Wake-up	Wake-up
Current Sense	On	On	On	-	-
LIN	-	Rx-Only	Full/Rx-Only	Rx-Only/Wake-up	Wake-up
Watchdog	-	150 ms (typ.) timeout	On[134]/Off	-	-
VSENSE	On	On	On	VDD	-

Notes
130. Operation can be enabled/controlled by the SPI.
131. Operation can be controlled by the PWMIN input.
132. HSx switches can be configured for cyclic sense operation in Stop mode.
133. HSx switches can be configured for cyclic sense operation in Sleep mode.
134. Windowing operation when enabled by an external resistor.

14.1.7 Interrupts

Interrupts are used to signal a microcontroller peripheral needs to be serviced. The interrupts which can be generated, change according to the operating mode. While in Normal and Normal Request modes, the 33912 signals through interrupts special conditions which may require a MCU software action. Interrupts are not generated until all pending wake-up sources are read in the Interrupt Source register (ISR).

While in Stop mode, interrupts are used to signal wake-up events. Sleep mode does not use interrupts. Wake-up is performed by powering-up the MCU. In Normal and Normal Request mode the wake-up source can be read by the SPI. The interrupts are signaled to the MCU by a low logic level of the $\overline{\text{IRQ}}$ pin, which remains low until the interrupt is acknowledged by a SPI read. The $\overline{\text{IRQ}}$ pin then is driven high.

Interrupts are only asserted while in Normal, Normal Request and Stop mode. Interrupts are not generated while the $\overline{\text{RST}}$ pin is low. The following is a list of the interrupt sources in Normal and Normal Request modes. Some of these can be masked by writing to the SPI - Interrupt Mask register (IMR).

14.1.7.1 Low-voltage interrupt

Signals when the supply line (VS1) voltage drops below the VSUV threshold (V_{SUV}).

14.1.7.2 High-voltage interrupt

Signals when the supply line (VS1) voltage increases above the VSOV threshold (V_{SOV}).

14.1.7.3 Overtemperature prewarning

Signals when the 33912 temperature has reached the pre-shutdown warning threshold. It is used to warn the MCU an overtemperature shutdown in the main 5.0 V regulator is imminent.

14.1.7.4 LIN overcurrent shutdown/overtemperature shutdown/TXD stuck at dominant/ RXD short-circuit

These signal fault conditions within the LIN interface causes the LIN driver to be disabled, except for the LIN overcurrent condition. The fault must be removed and must be acknowledged by reading the SPI to restart the operation. The LINOC bit functionality in the LIN Status register (LINSR) is to indicate an LIN overcurrent has occurred and the driver remains enabled.

14.1.7.5 High-side overtemperature shutdown

Signals a shutdown in the high-side outputs.

14.1.7.6 Low-side overtemperature shutdown

Signals a shutdown in the low-side outputs.

14.1.8 Reset

To reset a MCU the 33912 drives the $\overline{RST}$ pin low for the time the reset condition lasts. After the reset source is removed, the state machine drives the $\overline{RST}$ output low for at least 1.0 ms (typical value) before driving it high. In the 33912, four main reset sources exist:

14.1.8.1 5.0 V regulator low-voltage-reset ($V_{\overline{RSTTH}}$)

The 5.0 V regulator output V_{DD} is continuously monitored against brown outs. If the supply monitor detects the voltage at the VDD pin has dropped below the reset threshold $V_{\overline{RSTTH}}$, the 33912 issues a reset. In case of an overtemperature, the voltage regulator is disabled and the voltage monitoring issues a VDDOT Flag independently of the V_{DD} voltage.

14.1.8.2 Window watchdog overflow

If the watchdog counter is not properly serviced while its window is open, the 33912 detects an MCU software run-away and resets the microcontroller.

14.1.8.3 Wake-up from sleep mode

During Sleep mode, the 5.0 V regulator is not active, hence all wake-up requests from Sleep mode require a power-up/reset sequence.

14.1.8.4 External reset

The 33912 has a bidirectional reset pin which drives the device to a safe state (same as Reset mode) for as long as this pin is held low. The $\overline{RST}$ pin must be held low long enough to pass the internal glitch filter and get recognized by the internal reset circuit. This functionality is also active in Stop mode. After the $\overline{RST}$ pin is released, there is no extra $t_{\overline{RST}}$ to be considered.

14.1.9 Wake-up capabilities

Once entered into one of the Low-power modes (Sleep or Stop) only wake-up sources can bring the device into Normal mode operation. In Stop mode, a wake-up is signaled to the MCU as an interrupt, while in Sleep mode the wake-up is performed by activating the 5.0 V regulator and resetting the MCU. In both cases, the MCU can detect the wake-up source by accessing the SPI registers. There is no specific SPI register bit to signal a $\overline{CS}$ wake-up or external reset. If necessary, this condition is detected by excluding all other possible wake-up sources.

14.1.9.1 Wake-up from wake-up inputs (L1-L4) with cyclic sense disabled

The wake-up lines are dedicated to sense state changes of external switches and wake-up the MCU (in Sleep or Stop mode). To select and activate direct wake-up from Lx inputs, the Wake-up Control register (WUCR) must be configured with appropriate LxWE inputs enabled or disabled. The wake-up input's state is read through the Wake-up Status register (WUSR). Lx inputs are also used to perform cyclic-sense wake-up.

Note: Selecting an Lx input in the analog multiplexer before entering low power mode disables the wake-up capability of the Lx input

14.1.9.2 Wake-up from wake-up inputs (L1-L4) with cyclic sense timer enabled

The SBCLIN can wake-up at the end of a cyclic sense period if on one of the four wake-up input lines (L1-L4) a state change occurs. The HSx switch is activated in Sleep or Stop modes from an internal timer. Cyclic sense and force wake-up are exclusive. If cyclic sense is enabled, the force wake-up can not be enabled. In order to select and activate the cyclic sense wake-up from Lx inputs, before entering in low power modes (Stop or Sleep modes), the following SPI set-up has to be performed:

In WUCR: select the Lx input to WU-enable.

In HSCR: enable the desired HSx.

- In TIMCR: select the CS/$\overline{WD}$ bit and determine the cyclic sense period with CYSTx bits.
- Perform Goto Sleep/Stop command.

14.1.9.3 Forced wake-up

The 33912 can wake-up automatically after a predetermined time spent in Sleep or Stop mode. Cyclic sense and Forced wake-up are exclusive. If Forced wake-up is enabled, the Cyclic Sense can not be enabled.

To determine the wake-up period, the following SPI set-up has to be sent before entering in Low-power modes:

- In TIMCR: select the CS/$\overline{WD}$ bit and determine the Low-power mode period with CYSTx bits.
- In HSCR: all HSx bits must be disabled.

14.1.9.4 $\overline{CS}$ wake-up

While in Stop mode, a rising edge on the $\overline{CS}$ causes a wake-up. The $\overline{CS}$ wake-up does not generate an interrupt, and is not reported on the SPI.

14.1.9.5 LIN wake-up

While in the Low-power mode, the 33912 monitors the activity on the LIN bus. A dominant pulse larger than t_{PROPWL} followed by a dominant to recessive transition causes a LIN wake-up. This behavior protects the system from a short to ground bus condition.

14.1.9.6 $\overline{RST}$ wake-up

While in Stop mode, the 33912 can wake-up when the $\overline{RST}$ pin is held low long enough to pass the internal glitch filter. The 33912 then changes to Normal Request or Normal modes depending on the WDCONF pin configuration. The $\overline{RST}$ wake-up does not generate an interrupt and is not reported via the SPI.

From Stop mode, the following wake-up events can be configured:

- Wake-up from Lx inputs without cyclic sense
- Cyclic sense wake-up inputs
- Force wake-up
- $\overline{CS}$ wake-up
- LIN wake-up
- $\overline{RST}$ wake-up

From Sleep mode, the following wake-up events can be configured:

- Wake-up from Lx inputs without cyclic sense
- Cyclic sense wake-up inputs
- Force wake-up
- LIN wake-up

14.1.10Window watchdog

The 33912 includes a configurable window watchdog which is active in Normal mode. The watchdog can be configured by an external resistor connected to the WDCONF pin. The resistor is used to achieve higher precision in the timebase used for the watchdog. SPI clears are performed by writing through the SPI in the MOD bits of the Mode Control register (MCR).

During the first half of the SPI timeout, watchdog clears are not allowed, but after the first half of the SPI timeout window, the clear operation opens. If a clear operation is performed outside the window, the 33912 resets the MCU, in the same way as when the watchdog overflows.

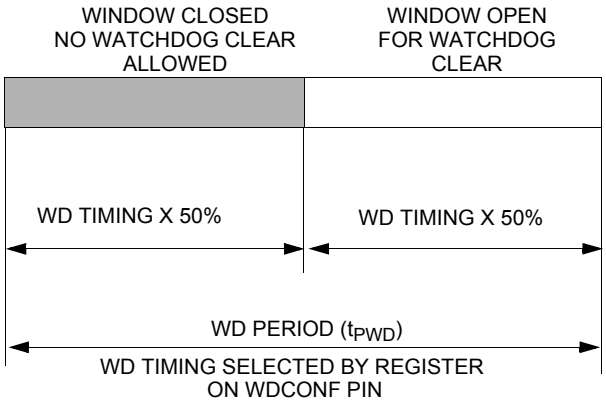


Figure 39. Window watchdog operation

To disable the watchdog function in Normal mode the user must connect the WDCONF pin to ground. This measure effectively disables Normal Request mode. The WDOFF bit in the Watchdog Status register (WDSR) is set. This condition is only detected during Reset mode.

If neither a resistor nor a connection to ground is detected, the watchdog falls back to the internal lower precision timebase of 150 ms (typ.) and signals the faulty condition through the Watchdog Status register (WDSR).

The watchdog timebase can be further divided by a prescaler which can be configured by the Timing Control register (TIMCR). During Normal Request mode, the window watchdog is not active but there is a 150 ms (typ.) timeout for leaving the Normal Request mode. In case of a timeout, the 33912 enters into Reset mode, resetting the microcontroller before entering again into Normal Request mode.

14.1.11 High-side output pins HS1 and HS2

These outputs are two high-side drivers intended to drive small resistive loads or LEDs incorporating the following features:

- PWM capability (software maskable)
- Open load detection
- Current limitation
- Overtemperature shutdown (with maskable interrupt)
- High-voltage shutdown (software maskable)
- Cyclic sense

The high-side switches are controlled by the bits HS1:2 in the high-side Control register (HSCR).

14.1.11.1 PWM capability (direct access)

Each high-side driver offers additional (to the SPI control) direct control via the PWMIN pin. If both the bits HS1 and PWMHS1 are set in the High-side Control register (HSCR), then the HS1 driver is turned on if the PWMIN pin is high and turned of if the PWMIN pin is low. This applies to HS2 configuring HS2 and PWMHS2 bits.

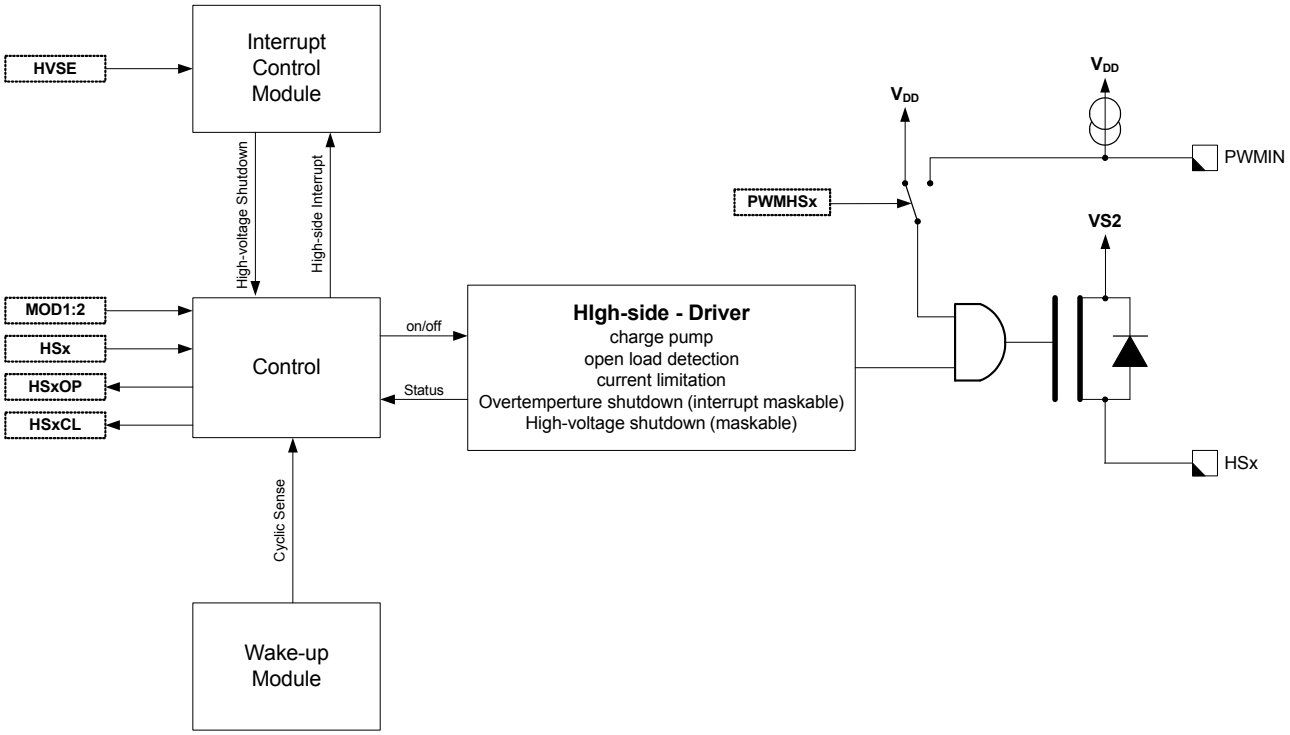


Figure 40. High-side drivers HS1 and HS2

14.1.11.2 Open load detection

Each high-side driver signals an open load condition if the current through the high-side is below the open load current threshold. The open load condition is indicated with the bits HS1OP and HS2OP in the High-side Status register (HSSR).

14.1.11.3 Current limitation

Each high-side driver has an output current limitation. In combination with the overtemperature shutdown the high-side drivers are protected against overcurrent and short-circuit failures. When the driver operates in the current limitation area, it is indicated with the bits HS1CL and HS2CL in the HSSR.

Note: If the driver is operating in current limitation mode, excessive power might be dissipated.

14.1.11.4 Overtemperature protection (HS interrupt)

Both high-side drivers are protected against overtemperature. In case of an overtemperature condition both high-side drivers are shutdown and the event is latched in the Interrupt Control Module. The shutdown is indicated as HS Interrupt in the Interrupt Source register (ISR). A thermal shutdown of the high-side drivers is indicated by setting all HSxOP and HSxCL bits simultaneously. If the bit HSM is set in the Interrupt Mask register (IMR), then an interrupt ($\overline{IRQ}$) is generated. A write to the High-side Control register (HSCR), when the overtemperature condition is gone, re-enables the high-side drivers.

14.1.11.5 High-voltage shutdown

In case of a high-voltage condition and if the high-voltage shutdown is enabled (bit HVSE in the Mode Control register (MCR) is set), both high-side drivers are shutdown. A write to the High-side Control register (HSCR), when the high-voltage condition is gone, re-enables the high-side drivers.

14.1.11.6 Sleep and stop mode

The high-side drivers can be enabled to operate in Sleep and Stop mode for cyclic sensing. Also see Table 37.

14.1.12Low-side output pins (LS1 and LS2)

These outputs are two low-side drivers intended to drive relays incorporating the following features:

- PWM capability (software maskable)
- Open load detection
- Current limitation
- Overtemperature shutdown (with maskable interrupt)
- Active clamp (for driving relays)
- High-voltage shutdown (software maskable)

The low-side switches are controlled by the bit LS1:2 in the Low-side Control register (LSCR). To protect the device against overvoltage when an inductive load (relay) is turned off. An active clamp re-enables the low-side FET if the voltage on the LS1 or LS2 pin exceeds a certain level.

14.1.12.1 PWM capability (direct access)

Each low-side driver offers additional (to the SPI control) direct control via the PWMIN pin. If both the bits LS1 and PWMLS1 are set in the Low-side Control register (LSCR), then the LS1 driver is turned on if the PWMIN pin is high and turned off if the PWMIN pin is low. The same applies to the LS2 and PWMLS2 bits for the LS2 driver.

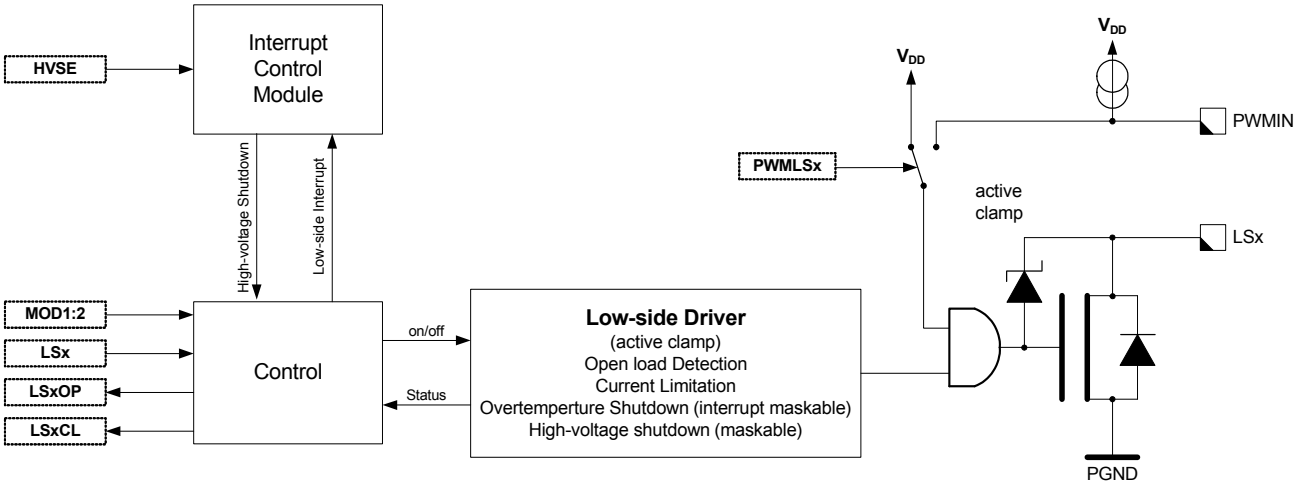


Figure 41. Low-side drivers LS1 and LS2

14.1.12.2 Open load detection

Each low-side driver signals an open load condition if the current through the low-side is below the open load current threshold. The open load condition is indicated with the bit LS1OP and LS2OP in the Low-side Status register (LSSR).

14.1.12.3 Current limitation

Each low-side driver has a current limitation. In combination with the overtemperature shutdown the low-side drivers are protected against overcurrent and short-circuit failures. When the drivers operate in current limitation, this is indicated with the bits LS1CL and LS2CL in the LSSR.

Note: If the drivers are operating in current limitation mode excessive power might be dissipated.

14.1.12.4 Overtemperature protection (LS interrupt)

Both low-side drivers are protected against overtemperature. In case of an overtemperature condition both low-side drivers are shutdown and the event is latched in the Interrupt Control Module. The shutdown is indicated as an LS Interrupt in the Interrupt Source register (ISR). If the bit LSM is set in the Interrupt Mask register (IMR) than an Interrupt ($\overline{IRQ}$) is generated. A write to the Low-side Control register (LSCR), when the overtemperature condition is gone, re-enables the low-side drivers.

14.1.12.5 High-voltage shutdown

In case of a high-voltage condition and if the high-voltage shutdown is enabed (bit HVSE in the Mode Control register (MCR) is set) both low-sides drivers are shutdown. A write to the Low-side Control register (LSCR), when the high-voltage condition is gone, re-enables the low-side drivers.

14.1.12.6 Sleep and stop mode

The low-side drivers are disabled in Sleep and Stop mode. Also see Table 37.

14.1.13LIN physical layer

The LIN bus pin provides a physical layer for single-wire communication in automotive applications. The LIN physical layer is designed to meet the LIN physical layer specification and has the following features:

- LIN physical layer 2.0 compliant
- Slew rate selection
- Overcurrent shutdown
- Overtemperature shutdown
- LIN pull-up disable in Stop and Sleep modes
- Advanced diagnostics
- LIN dominant voltage level selection

The LIN driver is a low-side MOSFET with overcurrent and thermal shutdown. An internal pull-up resistor with a serial diode structure is integrated, so no external pull-up components are required for the application in a slave node. The fall time from dominant to recessive and the rise time from recessive to dominant is controlled. The symmetry between both slopes is guaranteed.

14.1.13.1 LIN pin

The LIN pin offers a high susceptibility immunity level from external disturbance, guaranteeing communication during external disturbance.

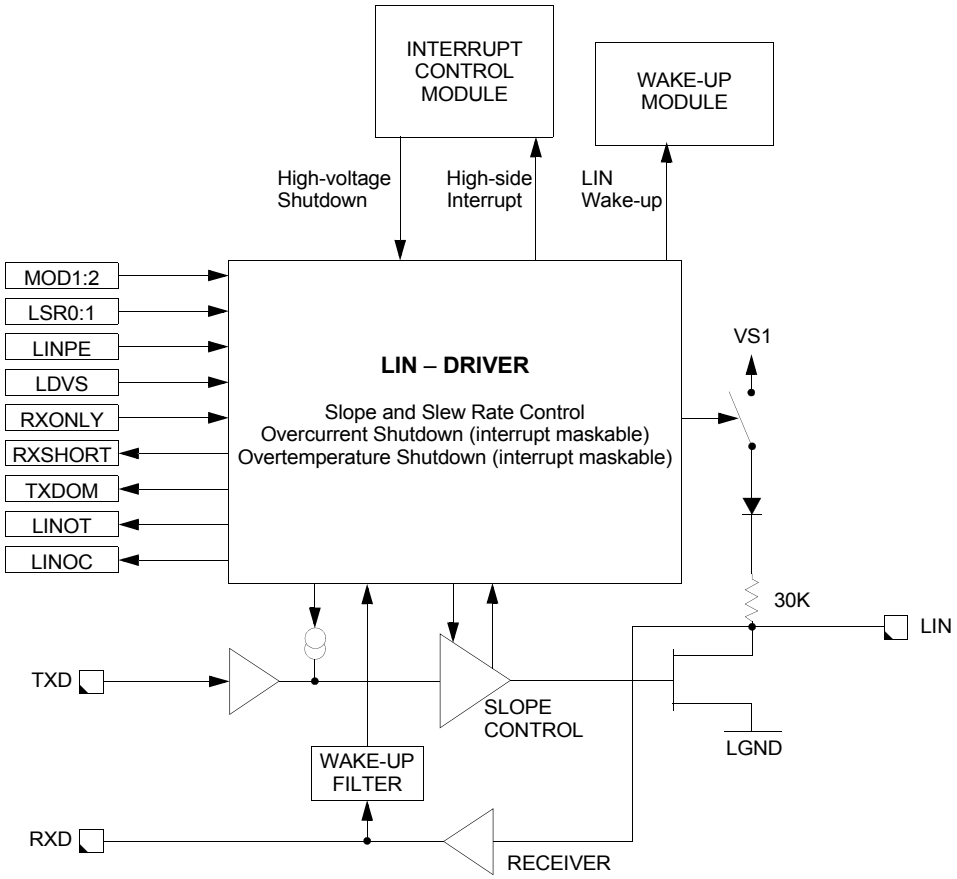


Figure 42. LIN interface

14.1.13.2 Slew rate selection

The slew rate can be selected for optimized operation at 10.4 and 20 kBit/s as well as a fast baud rate for test and programming. The slew rate can be adapted with the bits LSR 1:0 in the LIN Control register (LINCR). The initial slew rate is optimized for 20 kBit/s.

14.1.13.3 LIN pull-up disable in stop and sleep modes

In cases of a LIN bus short to GND or LIN bus leakage during Low-power mode, the internal pull-up resistor on the LIN pin can be disconnected by clearing the LINPE bit in the Mode Control register (MCR). The LINPE bit also changes the Bus wake-up threshold (V_{BUSWU}). This feature reduces the current consumption in STOP and SLEEP modes. It also improves performance and safe operation.

14.1.13.4 Current limit (LIN interrupt)

The output low-side FET is protected against overcurrent conditions. In case of an overcurrent condition (e.g. LIN bus short to V_{BAT}), the transmitter is not shutdown. The bit LINOC in the LIN Status register (LINSR) is set. If the LINM bit is set in the Interrupt Mask register (IMR), an Interrupt $\overline{IRQ}$ is generated.

14.1.13.5 Overtemperature shutdown (LIN interrupt)

The output low-side FET is protected against overtemperature conditions. In case of an overtemperature condition, the transmitter is shutdown and the LINOT bit in the LIN Status register (LINSR) is set. If the LINM bit is set in the Interrupt Mask register (IMR), an Interrupt $\overline{IRQ}$ is generated. The transmitter is automatically re-enabled once the condition is gone and TXD is high. A read of the LIN Status register (LINSR) with the TXD pin high, re-enables the transmitter.

14.1.13.6 RXD short-circuit detection (LIN interrupt)

The LIN transceiver has a short-circuit detection for the RXD output pin. In cases of a short-circuit condition, either 5.0 V or Ground, the RXSHORT bit in the LIN Status register (LINSR) is set and the transmitter is shutdown. If the LINM bit is set in the Interrupt Mask register (IMR), an Interrupt IRQ is generated. The transmitter automatically re-enables once the condition is gone (transition on RXD) and TXD is high. A read of the LIN Status register (LINSR) without the RXD pin short-circuit condition clears the bit RXSHORT.

14.1.13.7 TXD dominant detection (LIN interrupt)

The LIN transceiver monitors the TXD input pin to detect a stuck in dominant (0V) condition. In case of a stuck condition (TXD pin 0 V for more than 1 second (typ.)), the transmitter is shutdown and the TXDOM bit in the LIN Status register (LINSR) is set. If the LINM bit is set in the IMR, an Interrupt IRQ is generated. The transmitter automatically re-enables once TXD is high. A read of the LIN Status register (LINSR) with the TXD pin at 5.0 V clears the bit TXDOM.

14.1.13.8 LIN dominant voltage level selection

The LIN dominant voltage level can be selected by the bit LDVS in the LIN Control register (LINCR).

14.1.13.9 LIN receiver operation only

While in Normal mode, the activation of the RXONLY bit disables the LIN TXD driver. If case of a LIN error condition, this bit is automatically set. If a Low-power mode is selected with this bit set, the LIN wake-up functionality is disabled, then in STOP mode, the RXD pin reflects the state of the LIN bus.

14.1.13.10 Stop mode and wake-up feature

During Stop mode operation, the transmitter of the physical layer is disabled. If the LIN-PU bit was set in the Stop mode sequence, the internal pull-up resistor is disconnected from VSUP and a small current source keeps the LIN pin in the recessive state. The receiver is still active and able to detect wake-up events on the LIN bus line. A dominant level longer than t_{PROPWL} followed by a rising edge generates a wake-up interrupt, and is reported in the Interrupt Source register (ISR). Also see Figure 34.

14.1.13.11 Sleep mode and wake-up feature

During Sleep mode operation, the transmitter of the physical layer is disabled. If the LIN-PU bit was set in the Sleep mode sequence, the internal pull-up resistor is disconnected from VSUP and a small current source keeps the LIN pin in recessive state. The receiver must be active to detect wake-up events on the LIN bus line. A dominant level longer than t_{PROPWL} followed by a rising edge generates a system wake-up (Reset), and is reported in the Interrupt Source register (ISR). Also see Figure 33.

14.2 Logic commands and registers

14.2.1 33912 SPI interface and configuration

The serial peripheral interface creates the communication link between a microcontroller (master) and the 33912. The interface consists of four pins (see Figure 43):

- $\overline{CS}$—Chip Select
- MOSI—Master-Out Slave-In
- MISO—Master-In Slave-Out
- SCLK—Serial Clock

A complete data transfer via the SPI consists of 1 byte. The master sends 4 bits of address (A3:A0) + 4 bits of control information (C3:C0) and the slave replies with 4 system status bits (VMS,LINS,HSS,LSS) + 4 bits of status information (S3:S0).

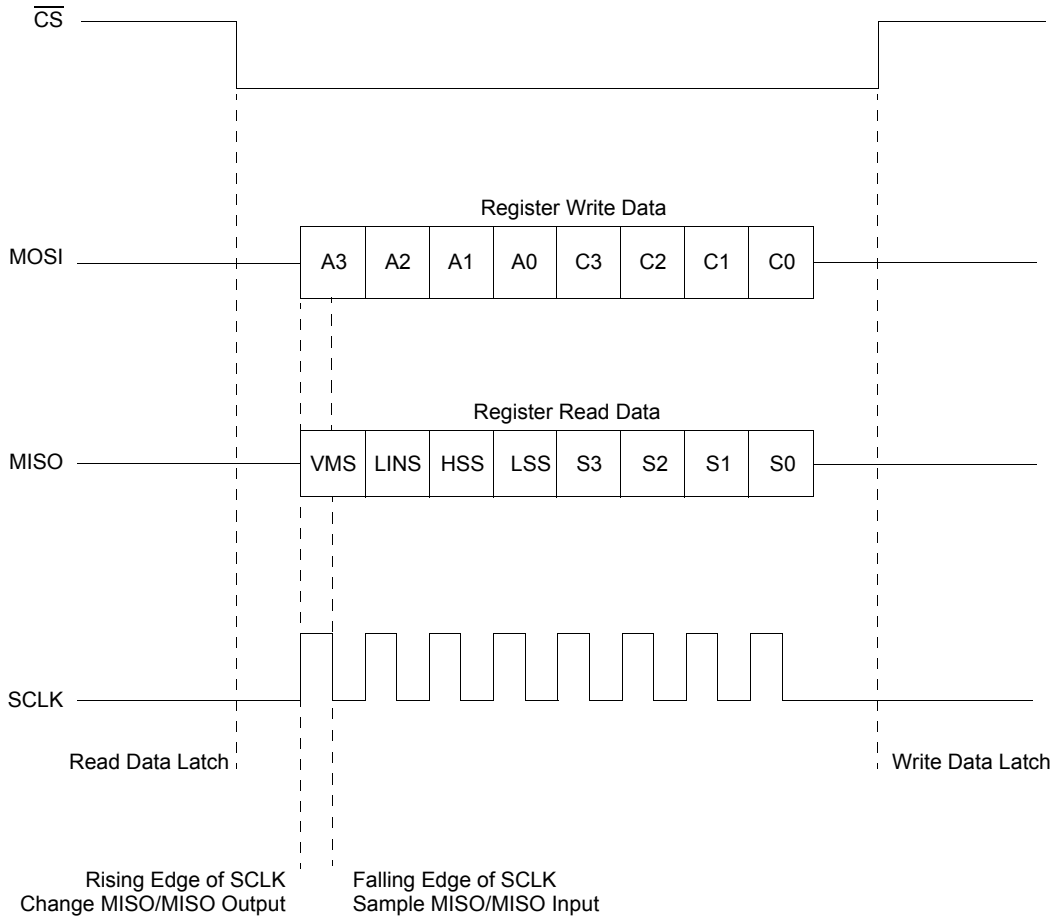


Figure 43. SPI protocol

During the inactive phase of the $\overline{CS}$ (HIGH), the new data transfer is prepared. The falling edge of the $\overline{CS}$ indicates the start of a new data transfer and puts the MISO in the low-impedance state and latches the analog status data (register read data). With the rising edge of the SPI clock (SCLK), the data is moved to MISO/MOSI pins. With the falling edge of the SPI clock (SCLK), the data is sampled by the receiver.

The data transfer is only valid if exactly 8 sample clock edges are present during the active (low) phase of $\overline{CS}$. The rising edge of the Chip Select $\overline{CS}$ indicates the end of the transfer and latches the write data (MOSI) into the register. The $\overline{CS}$ high forces MISO to the high-impedance state. Register reset values are described along with the reset condition. Reset condition is the condition causing the bit to be set to its reset value. The main reset conditions are:

- Power-On Reset (POR): the level at which the logic is reset and BATFAIL flag sets.
- Reset mode
- Reset done by the $\overline{RST}$ pin (ext_reset)

14.3 SPI register overview

Table 38. System status register

Address(A3:A0)	Register name / read/write information		BIT			
			7	6	5	4
$0 - $F	SYSSR - System Status Register	R	VMS	LINS	HSS	LSS

Table 39 summarizes the SPI register content for Control Information (C3:C0)=W and status information (S3:S0) = R.

Table 39. SPI register overview

Address(A3:A0)	Register name / read/write information		BIT			
			3	2	1	0
$0	MCR - Mode Control Register	W	HVSE	LINPE	MOD2	MOD1
	VSR - Voltage Status Register	R	VSOV	VSUV	VDDOT	BATFAIL
$1	VSR - Voltage Status Register	R	VSOV	VSUV	VDDOT	BATFAIL
$2	WUCR - Wake-up Control Register	W	L4WE	L3WE	L2WE	L1WE
	WUSR - Wake-up Status Register	R	L4	L3	L2	L1
$3	WUSR - Wake-up Status Register	R	L4	L3	L2	L1
$4	LINCR - LIN Control Register	W	LDVS	RXONLY	LSR1	LSR0
	LINSR - LIN Status Register	R	RXSHORT	TXDOM	LINOT	LINOC
$5	LINSR - LIN Status Register	R	RXSHORT	TXDOM	LINOT	LINOC
$6	HSCR - High-side Control Register	W	PWMHS2	PWMHS1	HS2	HS1
	HSSR - High-side Status Register	R	HS2OP	HS2CL	HS1OP	HS1CL
$7	HSSR - High-side Status Register	R	HS2OP	HS2CL	HS1OP	HS1CL
$8	LSCR - Low-side Control Register	W	PWMLS2	PWMLS1	LS2	LS1
	LSSR - Low-side Status Register	R	LS2OP	LS2CL	LS1OP	LS1CL
$9	LSSR - Low-side Status Register	R	LS2OP	LS2CL	LS1OP	LS1CL
$A	TIMCR - Timing Control Register	W	CS/$\overline{WD}$	WD2	WD1	WD0
				CYST2	CYST1	CYST0
	WDSR - Watchdog Status Register	R	WDTO	WDERR	WDOFF	WDWO
$B	WDSR - Watchdog Status Register	R	WDTO	WDERR	WDOFF	WDWO
$C	AMUXCR - Analog Multiplexer Control Register	W	LXDS	MX2	MX1	MX0
$D	CFR - Configuration Register	W	HVDD	CYSX8	CSAZ	CSGS
$E	IMR - Interrupt Mask Register	W	HSM	LSM	LINM	VMM
	ISR - Interrupt Source Register	R	ISR3	ISR2	ISR1	ISR0
$F	ISR - Interrupt Source Register	R	ISR3	ISR2	ISR1	ISR0

14.3.1 Register definitions

14.3.1.1 System status register - SYSSR

The System Status register (SYSSR) is always transferred with every SPI transmission and gives a quick system status overview. It summarizes the status of the Voltage Status register (VSR), LIN Status register (LINSR), High-side Status register (HSSR), and the Low-side Status register (LSSR).

Table 40. System status register

	S7	S6	S5	S4
Read	VMS	LINS	HSS	LSS

14.3.1.1.1 VMS - voltage monitor status

This read-only bit indicates one or more bits in the VSR are set.

1 = Voltage Monitor bit set

0 = None

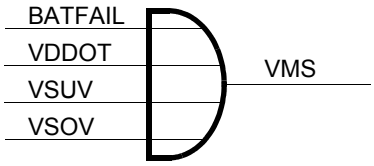


Figure 44. Voltage monitor status

14.3.1.1.2 LINS - LIN status

This read-only bit indicates one or more bits in the LINSR are set.

1 = LIN Status bit set

0 = None

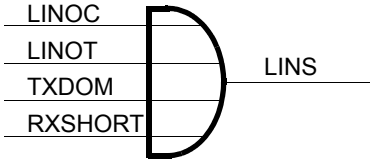


Figure 45. LIN status

14.3.1.1.3 HSS - high-side switch status

This read-only bit indicates one or more bits in the HSSR are set.

1 = High-side Status bit set

0 = None

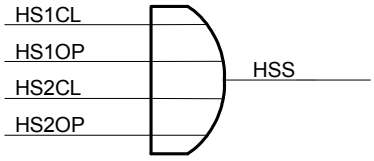


Figure 46. High-side status

14.3.1.1.4 LSS - low-side switch status

This read-only bit indicates one or more bits in the LSSR are set.

1 = Low-side Status bit set

0 = None

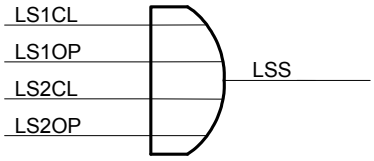


Figure 47. Low-side status

14.3.1.2 Mode control register - MCR

The Mode Control register (MCR) allows switching between the operation modes and to configure the 33912. Writing the MCR returns the VSR.

Table 41. Mode control register - $0

	C3	C2	C1	C0
Write	HVSE	LINPE	MOD2	MOD1
Reset Value	1	1	-	-
Reset Condition	POR	POR	-	-

14.3.1.2.1 HVSE - high-voltage shutdown enable

This write-only bit enables/disables automatic shutdown of the high-side and the low-side drivers during a high-voltage VSOV condition.

1 = automatic shutdown enabled

0 = automatic shutdown disabled

14.3.1.2.2 LINPE - LIN pull-up enable.

This write-only bit enables/disables the 30 kΩ LIN pull-up resistor in STOP and SLEEP modes. This bit also controls the LIN bus wake-up threshold.

1 = LIN pull-up resistor enabled

0 = LIN pull-up resistor disabled

14.3.1.2.3 MOD2, MOD1 - mode control bits

These write-only bits select the operating mode and allow clearing the watchdog in accordance with Table 85 Mode Control Bits.

Table 42. Mode control bits

MOD2	MOD1	Description
0	0	Normal Mode
0	1	Stop Mode
1	0	Sleep Mode
1	1	Normal Mode + Watchdog Clear

14.3.1.3 Voltage status register - VSR

Returns the status of the several voltage monitors. This register is also returned when writing to the Mode Control register (MCR).

Table 43. Voltage status register - $0/$1

	S3	S2	S1	S0
Read	VSOV	VSUV	VDDOT	BATFAIL

14.3.1.3.1 VSOV - V_{SUP} overvoltage

This read-only bit indicates an overvoltage condition on the VS1 pin.
1 = Overvoltage condition.
0 = Normal condition.

14.3.1.3.2 VSUV - V_{SUP} undervoltage

This read-only bit indicates an undervoltage condition on the VS1 pin.
1 = Undervoltage condition.
0 = Normal condition.

14.3.1.3.3 VDDOT - main voltage regulator overtemperature warning

This read-only bit indicates the main voltage regulator temperature reached the Overtemperature Prewarning threshold.
1 = Overtemperature Prewarning
0 = Normal

14.3.1.3.4 BATFAIL - battery fail flag

This read-only bit is set during power-up and indicates the 33912 had a Power-On-Reset (POR).
Any access to the MCR or VSR clears the BATFAIL flag.
1 = POR Reset has occurred
0 = POR Reset has not occurred

14.3.1.4 Wake-up control register - WUCR

This register is used to control the digital wake-up inputs. Writing the WUCR returns the Wake-up Status register (WUSR).

Table 44. Wake-up control register - $2

	C3	C2	C1	C0
Write	L4WE	L3WE	L2WE	L1WE
Reset Value	1	1	1	1
Reset Condition	POR, Reset mode or ext_reset			

14.3.1.4.1 LxWE - wake-up input x enable

This write-only bit enables/disables which Lx inputs are enabled. In Stop and Sleep mode the LxWE bit determines which wake inputs are active for wake-up. If one of the Lx inputs is selected on the analog multiplexer, the corresponding LxWE is masked to 0.

1 = Wake-up Input x enabled.

0 = Wake-up Input x disabled.

14.3.1.5 Wake-up status register - WUSR

This register is used to monitor the digital wake-up inputs and is also returned when writing to the WUCR.

Table 45. Wake-up status register - $2/$3

	S3	S2	S1	S0
Read	L4	L3	L2	L1

14.3.1.5.1 Lx - wake-up input x

This read-only bit indicates the status of the corresponding Lx input. If the Lx input is not enabled, then the according Wake-up status returns 0. After a wake-up from Stop or Sleep mode these bits also allow to determine which input has caused the wake-up, by first reading the Interrupt Status register (ISR) and then reading the WUSR.

1 = Lx Wake-up.

0 = Lx Wake-up disabled or selected as analog input.

14.3.1.6 LIN control register - LINCR

This register controls the LIN physical interface block. Writing the LIN Control register (LINCR) returns the LIN Status register (LINSR).

Table 46. LIN control register - $4

	C3	C2	C1	C0
Write	LDVS	RXONLY	LSR1	LSR0
Reset Value	0	0	0	0
Reset Condition	POR, Reset mode or ext_reset	POR, Reset mode, ext_reset or LIN failure gone*	POR	

* LIN failure gone: if LIN failure (overtemp, TXD/RXD short) was set, the flag resets automatically when the failure is gone.

14.3.1.6.1 LDVS - LIN dominant voltage select

This write-only bit controls the LIN Dominant voltage:

1 = LIN Dominant Voltage = $V_{LIN\_DOM\_1}$ (1.7V typ)

0 = LIN Dominant Voltage = $V_{LIN\_DOM\_0}$ (1.1V typ)

14.3.1.6.2 RXONLY - LIN receiver operation only

This write-only bit controls the behavior of the LIN transmitter. In Normal mode, the activation of the RXONLY bit disables the LIN transmitter. In case of a LIN error condition, this bit automatically sets. In Stop mode this bit disables the LIN wake-up functionality, and the RXD pin reflects the state of the LIN bus.

1 = only LIN receiver active (Normal mode) or LIN wake-up disabled (Stop mode).

0 = LIN fully enabled.

14.3.1.6.3 LSRx - LIN slew rate

This write-only bit controls the LIN driver slew-rate in accordance with Table 47.

Table 47. LIN slew rate control

LSR1	LSR0	Description
0	0	Normal Slew Rate (up to 20 kb/s)
0	1	Slow Slew Rate (up to 10 kb/s)
1	0	Fast Slew Rate (up to 100 kb/s)
1	1	Reserved

14.3.1.7 LIN status register - LINSR

This register returns the status of the LIN physical interface block and is also returned when writing to the LINCR.

Table 48. LIN status register - $4/$5

	S3	S2	S1	S0
Read	RXSHORT	TXDOM	LINOT	LINOC

14.3.1.7.1 RXSHORT - RXD pin short-circuit

This read-only bit indicates a short-circuit condition on the RXD pin (shorted either to 5.0 V or to Ground). The short-circuit delay must be a worst case of 8.0 µs to be detected and to shutdown the driver. To clear this bit, it must be read after the condition is gone (transition detected on RXD pin). The LIN driver automatically re-enables once the condition is gone.

1 = RXD short-circuit condition.

0 = None.

14.3.1.7.2 TXDOM - TXD permanent dominant

This read-only bit signals the detection of a TXD pin stuck at dominant (Ground) condition and the resultant shutdown in the LIN transmitter. This condition is detected after the TXD pin remains in dominant state for more than 1 second (typical value). To clear this bit, it must be read after TXD has gone high. The LIN driver automatically re-enables once TXD goes High.

1 = TXD stuck at dominant fault detected.

0 = None.

14.3.1.7.3 LINOT - LIN driver overtemperature shutdown

This read-only bit signals the LIN transceiver was shutdown due to overtemperature. The transmitter automatically re-enables after the overtemperature condition is gone and TXD is high. The LINOT bit clears after a SPI read once the condition is gone.

1 = LIN overtemperature shutdown

0 = None

14.3.1.7.4 LINOC - LIN driver overcurrent shutdown

This read-only bit signals an overcurrent condition occurred on the LIN pin. The LIN driver is not shutdown but an $\overline{\text{IRQ}}$ is generated. To clear this bit, it must be read after the condition is gone.

1 = LIN overcurrent shutdown

0 = None

14.3.1.8 High-side control register - HSCR

This register controls the operation of the high-side drivers. Writing to this register returns the High-side Status register (HSSR).

Table 49. High-side control register - $6

	C3	C2	C1	C0
Write	PWMHS2	PWMHS1	HS2	HS1
Reset Value	0	0	0	0
Reset Condition	POR		POR, Reset mode, ext_reset, HSx overtemp or (VSOV & HVSE)	

14.3.1.8.1 PWMHSx - PWM input control enable

This write-only bit enables/disables the PWMIN input pin to control the respective high-side switch. The corresponding high-side switch must be enabled (HSx bit).

1 = PWMIN input controls HSx output.

0 = HSx is controlled only by the SPI.

14.3.1.8.2 HSx - HSx switch control

This write-only bit enables/disables the corresponding high-side switch.

1 = HSx switch on.

0 = HSx switch off.

14.3.1.9 High-side status register - HSSR

This register returns the status of the high-side switches and is also returned when writing to the HSCR.

Table 50. High-side status register - $6/$7

	S3	S2	S1	S0
Read	HS2OP	HS2CL	HS1OP	HS1CL

14.3.1.9.1 High-side thermal shutdown

A thermal shutdown of the high-side drivers is indicated by setting all HSxOP and HSxCL bits simultaneously.

14.3.1.9.2 HSxOP - high-side switch open load detection

This read-only bit signals the high-side switches are conducting current below a certain threshold indicating possible load disconnection.

1 = HSx Open Load detected (or thermal shutdown)

0 = Normal

14.3.1.9.3 HSxCL - high-side current limitation

This read-only bit indicates the respective high-side switch is operating in current limitation mode.

1 = HSx in current limitation (or thermal shutdown)

0 = Normal

14.3.1.10 Low-side control register - LSCR

This register controls the operation of the low-side drivers. Writing the Low-side Control register (LSCR) also returns the Low-side Status register (LSSR).

Table 51. Low-side control register - $8

	C3	C2	C1	C0
Write	PWMLS2	PWMLS1	LS2	LS1
Reset Value	0	0	0	0
Reset Condition	POR		POR, Reset mode, ext_reset, LSx overtemp or (VSOV & HVSE)	

14.3.1.10.1 PWMLx - PWM input control enable

This write-only bit enables/disables the PWMIN input pin to control the respective low-side switch. The corresponding low-side switch must be enabled (LSx bit).

1 = PWMIN input controls LSx.

0 = LSx is controlled only by the SPI.

14.3.1.10.2 LSx - LSx switch control

This write-only bit enables/disables the corresponding low-side switch.

1 = LSx switch on.

0 = LSx switch off.

14.3.1.11 Low-side status register - LSSR

This register returns the status of the low-side switches and is also returned when writing to the LSCR.

Table 52. Low-side status register - $8/$9

	C3	C2	C1	C0
Read	LS2OP	LS2CL	LS1OP	LS1CL

14.3.1.11.1 Low-side thermal shutdown

A thermal shutdown of the low-side drivers is indicated by setting all LSxOP and LSxCL bits simultaneously.

14.3.1.11.2 LSxOP - low-side switch open load detection

This read-only bit signals the low-side switches are conducting current below a certain threshold indicating possible load disconnection.

1 = LSx Open Load detected (or thermal shutdown)

0 = Normal

14.3.1.11.3 LSxCL - low-side current limitation

This read-only bit indicates the respective low-side switch is operating in current limitation mode.

1 = LSx in current limitation (or thermal shutdown)

0 = Normal

14.3.1.12 Timing control register - TIMCR

This register is a double purpose register which allows to configure the watchdog and the cyclic sense periods. Writing to the Timing Control register (TIMCR) also returns the Watchdog Status register (WDSR).

Table 53. Timing control register - $A

	C3	C2	C1	C0
Write	CS/$\overline{WD}$	WD2	WD1	WD0
		CYST2	CYST1	CYST0
Reset Value	-	0	0	0
Reset Condition	-	POR		

14.3.1.12.1 CS/$\overline{WD}$ - cyclic sense or watchdog prescaler select

This write-only bit selects which prescaler is being written to, the Cyclic Sense prescaler or the Watchdog prescaler.

1 = Cyclic Sense Prescaler selected

0 = Watchdog Prescaler select

14.3.1.12.2 WDx - watchdog prescaler

This write-only bits selects the divider for the watchdog prescaler and therefore selects the watchdog period in accordance with Table 54. This configuration is valid only if windowing watchdog is active.

Table 54. Watchdog prescaler

WD2	WD1	WD0	Prescaler divider
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	6
1	0	0	8
1	0	1	10
1	1	0	12
1	1	1	14

14.3.1.12.3 CYSTx - cyclic sense period prescaler select

This write-only bits selects the interval for the wake-up cyclic sensing together with the bit CYSX8 in the Configuration register (CFR) (see Configuration register - CFR). This option is only active if one of the high-side switches is enabled when entering in Stop or Sleep mode. Otherwise a timed wake-up is performed after the period shown in Table 55.

Table 55. Cyclic sense interval

CYSX8[135]	CYST2	CYST1	CYST0	Interval
X	0	0	0	No cyclic sense
0	0	0	1	20 ms
0	0	1	0	40 ms
0	0	1	1	60 ms
0	1	0	0	80 ms
0	1	0	1	100 ms
0	1	1	0	120 ms
0	1	1	1	140 ms
1	0	0	1	160 ms

Table 55. Cyclic sense interval (continued)

CYSX8[135]	CYST2	CYST1	CYST0	Interval
1	0	1	0	320 ms
1	0	1	1	480 ms
1	1	0	0	640 ms
1	1	0	1	800 ms
1	1	1	0	960 ms
1	1	1	1	1120 ms

Notes

135. bit CYSX8 is located in Configuration register (CFR)

14.3.1.13 Watchdog status register - WDSR

This register returns the Watchdog status information and is also returned when writing to the TIMCR.

Table 56. Watchdog status register - $A/$B

	S3	S2	S1	S0
Read	WDTO	WDERR	WDOFF	WDWO

14.3.1.13.1 WDTO - watchdog timeout

This read-only bit signals the last reset was caused by either a watchdog timeout or by an attempt to clear the Watchdog within the window closed. Any access to this register or the Timing Control register (TIMCR) clears the WDTO bit.

1 = Last reset caused by watchdog timeout

0 = None

14.3.1.13.2 WDERR - watchdog error

This read-only bit signals the detection of a missing watchdog resistor. In this condition the watchdog is using the internal, lower precision timebase. The Windowing function is disabled.

1 = WDCONF pin resistor missing

0 = WDCONF pin resistor not floating

14.3.1.13.3 WDOFF - watchdog off

This read-only bit signals the watchdog pin connected to Ground and therefore disabled. In this case watchdog timeouts are disabled and the device automatically enters Normal mode out of Reset. This might be necessary for software debugging and for programming the Flash memory.

1 = Watchdog is disabled

0 = Watchdog is enabled

14.3.1.13.4 WDWO - watchdog window open

This read-only bit signals when the watchdog window is open for clears. The purpose of this bit is for testing. Should be ignored if WDERR is High.

1 = Watchdog window open

0 = Watchdog window closed

14.3.1.14 Analog multiplexer control register - MUXCR

This register controls the analog multiplexer and selects the divider ration for the Lx input divider.

Table 57. Analog multiplexer control register -$C

	C3	C2	C1	C0
Write	LXDS	MX2	MX1	MX0
Reset Value	1	0	0	0
Reset Condition	POR	POR, Reset mode or ext_reset		

14.3.1.14.1 LXDS - Lx analog input divider select

This write-only bit selects the resistor divider for the Lx analog inputs. Voltage is internally clamped to VDD.

0 = Lx Analog divider: 1

1 = Lx Analog divider: 3.6 (typ.)

14.3.1.15 MXx - analog multiplexer input select

These write-only bits selects which analog input is multiplexed to the ADOUT0 pin according to Table 58. When disabled or when in Stop or Sleep mode, the output buffer is not powered and the ADOUT0 output is left floating to achieve lower current consumption.

Table 58. Analog multiplexer channel select

MX2	MX1	MX0	Meaning
0	0	0	Disabled
0	0	1	Reserved
0	1	0	Die Temperature Sensor
0	1	1	VSENSE input
1	0	0	L1 input
1	0	1	L2 input
1	1	0	L3 input
1	1	1	L4 input

14.3.1.16 Configuration register - CFR

This register controls the Hall Sensor Supply enable/disable, the cyclic sense timing multiplier, enables/disables the Current Sense Auto-zero function and selects the gain for the current sense amplifier.

Table 59. Configuration register - $D

	C3	C2	C1	C0
Write	HVDD	CYSX8	CSAZ	CSGS
Reset Value	0	0	0	0
Reset Condition	POR, Reset mode or ext_reset	POR	POR	POR

14.3.1.16.1 HVDD - Hall sensor supply enable

This write-only bit enables/disables the state of the hall sensor supply.
1 = HVDD on
0 = HVDD off

14.3.1.16.2 CYSX8 - cyclic sense timing x 8

This write-only bit influences the cyclic sense period as shown in Table 55.
1 = Multiplier enabled
0 = None

14.3.1.16.3 CSAZ - current sense auto-zero function enable

This write-only bit enables/disables the circuitry to lower the offset voltage of the current sense amplifier.
1 = Auto-zero function enabled
0 = Auto-zero function disabled

14.3.1.16.4 CSGS - current sense amplifier gain select

This write-only bit selects the gain of the current sense amplifier.
1 = 14.5 (typ.)
0 = 30 (typ.)

14.3.1.17 Interrupt mask register - IMR

This register allows masking of some of the interrupt sources. The respective flags within the Interrupt Source register (ISR) continues to work but does not generate interrupts to the MCU. The 5.0 V Regulator overtemperature prewarning interrupt and undervoltage (VSUV) interrupts can not be masked and always causes an interrupt. Writing to the IMR returns the ISR.

Table 60. Interrupt mask register - $E

	C3	C2	C1	C0
Write	HSM	LSM	LINM	VMM
Reset Value	1	1	1	1
Reset Condition	POR			

14.3.1.17.1 HSM - high-side interrupt mask

This write-only bit enables/disables interrupts generated in the high-side block.
1 = HS Interrupts Enabled
0 = HS Interrupts Disabled

14.3.1.17.2 LSM - low-side interrupt mask

This write-only bit enables/disables interrupts generated in the low-side block.
1 = LS Interrupts Enabled
0 = LS Interrupts Disabled

14.3.1.17.3 LINM - LIN interrupts mask

This write-only bit enables/disables interrupts generated in the LIN block.
1 = LIN Interrupts Enabled
0 = LIN Interrupts Disabled

14.3.1.17.4 VMM - voltage monitor interrupt mask

This write-only bit enables/disables interrupts generated in the Voltage Monitor block. The only maskable interrupt in the Voltage Monitor Block is the V_{SUP} overvoltage interrupt.

1 = Interrupts Enabled

0 = Interrupts Disabled

14.3.1.18 Interrupt source register - ISR

This register allows the MCU to determine the source of the last interrupt or wake-up respectively. A read of the register acknowledges the interrupt and leads $\overline{IRQ}$ pin to high, in case there are no other pending interrupts. If there are pending interrupts, $\overline{IRQ}$ is driven high for 10 µs and then be driven low again. This register is also returned when writing to the Interrupt Mask register (IMR).

Table 61. Interrupt source register - $E/$F

	S3	S2	S1	S0
Read	ISR3	ISR2	ISR1	ISR0

14.3.1.18.1 ISRx - interrupt source register

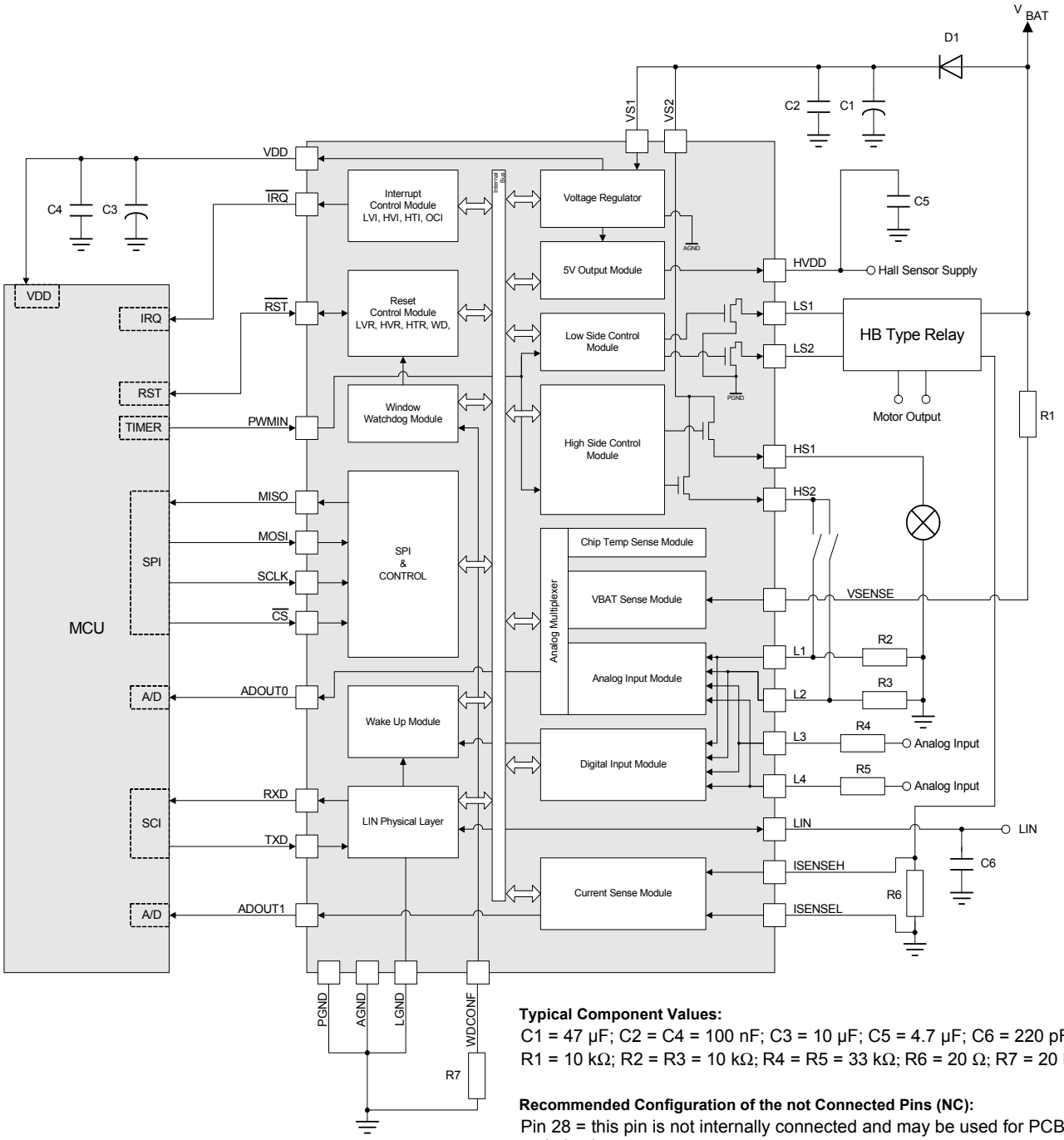
These read-only bits indicate the interrupt source following Table 62. If no interrupt is pending then all bits are 0. If more than one interrupt is pending, the interrupt sources are handled sequentially multiplex.

Table 62. Interrupt sources

ISR3	ISR2	ISR1	ISR0	Interrupt source		Priority
				none maskable	maskable	
0	0	0	0	no interrupt	no interrupt	none
0	0	0	1		Lx Wake-up from Stop mode	highest
0	0	1	0	-	HS Interrupt (Overtemperature)	
0	0	1	1	-	LS Interrupt (Overtemperature)	
0	1	0	0		LIN Interrupt (RXSHORT, TXDOM, LIN OT, LIN OC) or LIN Wake-up	
0	1	0	1	Voltage Monitor Interrupt (Low-voltage and VDD overtemperature)	Voltage Monitor Interrupt (High-voltage)	
0	1	1	0	-	Forced Wake-up	lowest

15 Typical application

The 33912 can be configured in several applications. The figure below shows the 33912 in the typical Slave Node Application.



Typical Component Values:

C1 = 47 µF; C2 = C4 = 100 nF; C3 = 10 µF; C5 = 4.7 µF; C6 = 220 pF

R1 = 10 kΩ; R2 = R3 = 10 kΩ; R4 = R5 = 33 kΩ; R6 = 20 Ω; R7 = 20 kΩ-200 kΩ

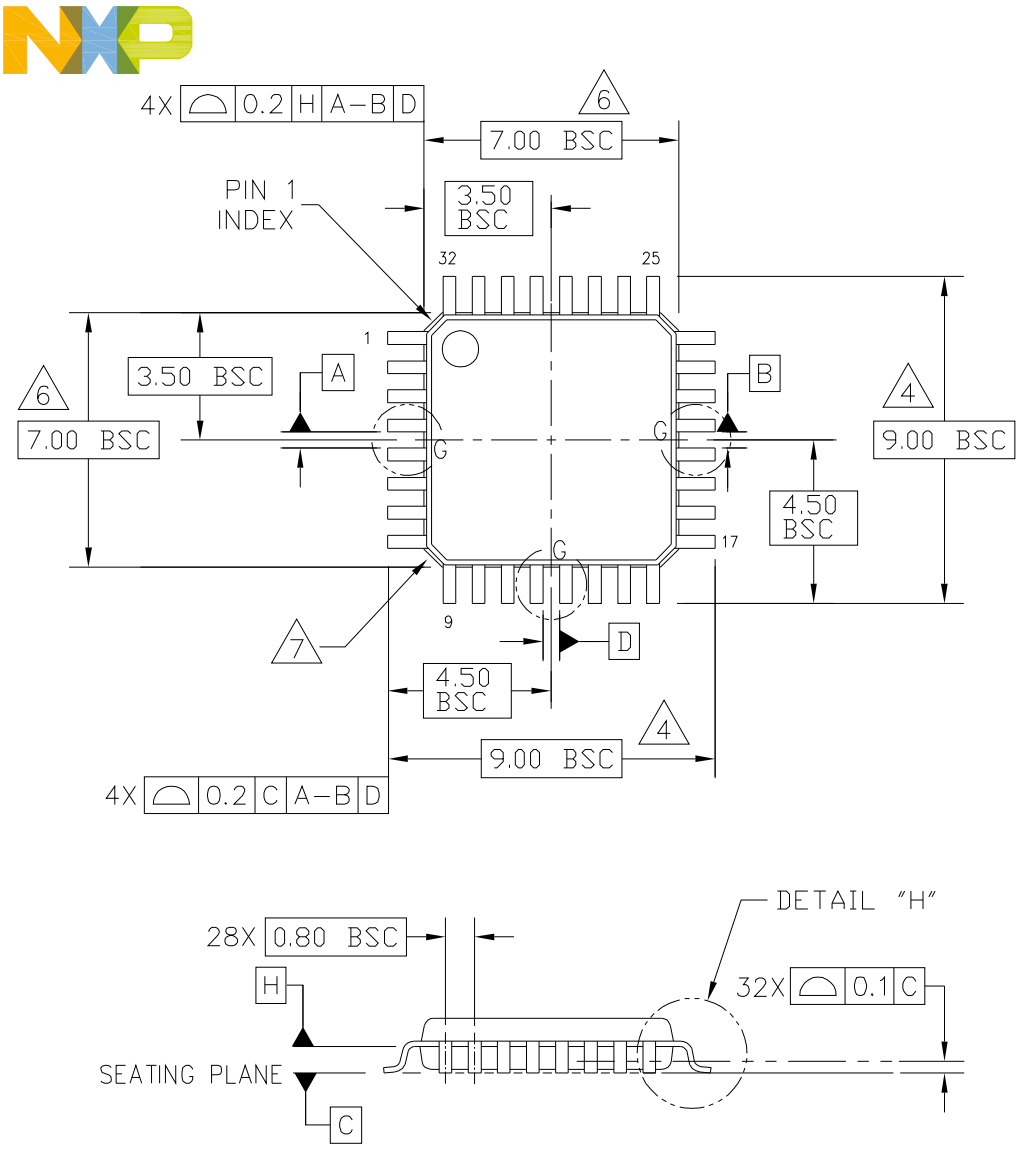
Recommended Configuration of the not Connected Pins (NC):

Pin 28 = this pin is not internally connected and may be used for PCB routing optimization.

16 Packaging

16.1 Package dimensions

Important For the most current revision of the package, visit www.nxp.com and select Documentation, then under Available Documentation column select Packaging Information.



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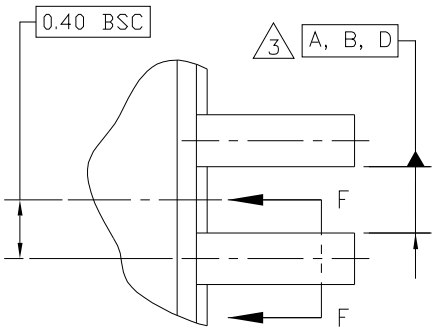
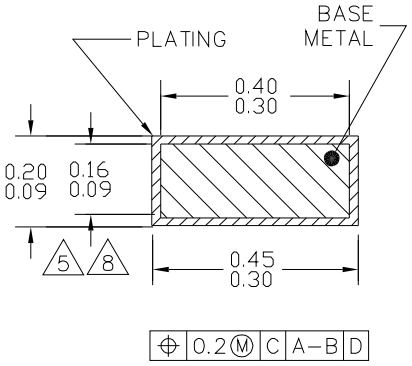
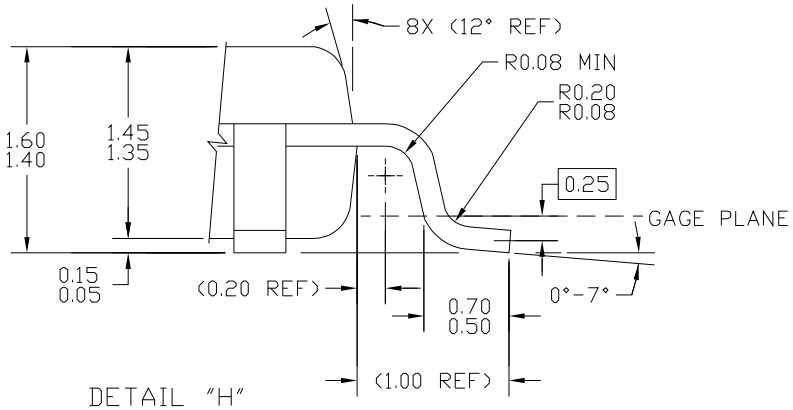
TITLE: LOW PROFILE QUAD FLAT PACK (LQFP) 32 LEAD, 0.8 PITCH (7 X 7 X 1.4)	DOCUMENT NO: 98ASH70029A	REV: F
	STANDARD: JEDEC MS-026 BBA	
	SOT358-3	01 APR 2016



DETAIL G



SECTION F–F
ROTATED 90°CW
32 PLACES



DETAIL "H"

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NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5–1994.

3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.

4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE DATUM C.

5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07 MM.

6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.

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	STANDARD: JEDEC MS-026 BBA	
	SOT358-3	01 APR 2016

17 Revision history

Table 63. Revision history

Revision	Date	Description of changes
1.0	5/2007	• Initial Release
2.0	9/2007	• Several textual corrections • Page 11: “Analog Output offset Ratio” (LXDS=1) changed to “Analog Output offset” +/-22mV • Page 11: VSENSE Input Divider Ratio adjusted to 5,0/5,25/5,5 • Page 12: Common mode input impedance corrected to 75kΩ • Page 13/15: LIN PHYSICAL LAYER parameters adjusted to final LIN specification release
3.0	9/2007	• Revision number incremented at engineering request.
4.0	2/2008	• Changed Functional Block Diagram on page 24. • This Data Sheet and previous versions cover Part Numbers MC33912BAC and MC34912BAC. Future revisions do not cover these Part Numbers.
5.0	10/2008	• Datasheet updated according to the Pass1.2 silicon version electrical parameters • Add Maximum Rating on $I_{BUS\_NO\_GND}$ parameter • Added L1, L2, L3, and L4, Temperature Sense Analog Output Voltage per characterization, Internal Chip Temperature Sense Gain per characterization at 3 temperatures. See Figure 16, Temperature sense gain, VSENSE Input Divider Ratio (RATIOVSENSE=VSENSE/VADOUT0) per characterization, and VSENSE Output Related Offset per characterization parameters • Added Temperature sense gain section • Minor corrections to ESD Capability, (19), Cyclic Sense ON Time from Stop and Sleep mode, Lin bus pin (LIN), Serial data clock pin (SCLK), Master out slave in pin (MOSI), Master in slave out pin (MISO), Low-side pins (LS1 and LS2), Digital/analog pins (L1, L2, L3, and L4), Normal request mode, Sleep mode, LIN overtemperature shutdown / TXD stuck at dominant / RXD short-circuit, Fault detection management conditions, LIN physical layer, LIN interface, Overtemperature shutdown (LIN interrupt), LIN receiver operation only, SPI protocol, Lx - wake-up input x, LIN control register - LINCR, and RXSHORT - RXD pin short-circuit • This data sheet does not contain electrical parameters for MC33912BAC and MC34912BAC (see revision 4.0). • Updated Freescale form and style
6.0	2/2009	• Added explanation for pins Not Connected (NC). • This data sheet does not contain electrical parameters for MC33912BAC and MC34912BAC (see revision 4.0).
7.0	3/2009	• Changed VBAT_SHIFT and GND_SHIFT maximum from 10% to 11.5% for both parameters on page 14. • This data sheet does not contain electrical parameters for MC33912BAC and MC34912BAC (see revision 4.0).
8.0	3/2010	• Combined Complete Data sheet for Part Numbers MC33912BAC and MC34912BAC to the back of this data sheet. • Changed ESD Voltage for Machine Model from ±200 to ±150
9.0	2/2014	• No technical changes. Revised back page. Updated document properties. Added SMARTMOS sentence to last paragraph.
10.0	9/2015	• Added (75) to Table 28 • Updated template form and style.
	8/2016	• Updated to NXP document form and style

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