THE DATASHEET OF

MC33879EKR2

www.win-source.net 0086-755-83957316

MC33879

Configurable Octal Serial Switch with Open Load Detect Current Disable

Rev. 12.1 — 11 May 2023 **Product data sheet**

1 General description

The 33879 device is an 8-output hardware configurable, high-side/low-side switch with 16-bit serial input control using the Serial Peripheral Interface (SPI). Two of the outputs may be controlled directly via a microcontroller for pulse-width modulation (PWM) applications. The 33879 incorporates SMARTMOS technology, with CMOS logic, bipolar/MOS analog circuitry, and DMOS power MOSFETs. The 33879 controls various inductive, incandescent, or LED loads by directly interfacing with a microcontroller. The circuit's innovative monitoring and protection features include very low standby currents, cascade fault reporting, internal +45 V clamp voltage for low-side configuration, –20 V high-side configuration, output specific diagnostics, and independent overtemperature protection.

2 Features and benefits

- Designed to operate at 5.5 V < VPWR < 27.5 V
- 16-bit SPI for control and fault reporting, 3.3 V / 5.0 V compatible
- Outputs are current limited (0.6 A to 1.2 A) to drive incandescent lamps
- Output voltage clamp, + 45 V (low side) and –20 V (high side) during inductive switching
- On/Off control of open load detect current (LED application)
- Internal reverse battery protection on VPWR
- Loss of ground or supply will not energize loads or damage IC
- Maximum 5.0 µA IPWR standby current at 13 V VPWR
- RDS(ON) of 0.75 Ω at 25 °C typical
- Short-circuit detect and current limit with automatic retry
- Independent overtemperature protection

3 Ordering information

Table 1. Orderable Part Variations

Type number[1]	Package		
	Name	Description	Version
MC33879TEK	HSOP32	EK suffix (PB-free) HSOP32, plastic, thermal enhanced small outline package; 32 terminals; 0.65 mm pitch; 7.5 mm x 11 mm x 2.22 mm body –40 to 125 °C	SOT1746-1
MC33879APEK			
MC33879BPEK			

[1] To order parts in tape & reel, add R2 to the end of the part number.

Table 2. Device variations

Symbol	Characteristic	Min	Typ	Max	Unit
V_{PWR}	V_{PWR} Supply Voltage				V
	33879	–16	—	40	
	33879A and 33879B	–16	—	45	
$I_{OUT(FLT-TH)}$	Output Fault Detection Current @ Threshold, High-side Configuration Outputs Programmed OFF				µA
	33879	35	55	90	
	33879A and 33879B	35	55	150	
I_{OCO}	Output OFF Open Load Detection Current, High-side Configuration VDRAIN = 16 V, VSOURCE = 0 V, Outputs Programmed OFF, VPWR = 16 V				µA
	33879	65	100	160	
	33879A and 33879B	60	100	190	
I_{OCO}	Output OFF Open Load Detection Current, Low-side Configuration VDRAIN = 16 V, VSOURCE = 0 V, Outputs Programmed OFF, VPWR =16 V				µA
	33879	40	75	135	
	33879A and 33879B	40	75	150	
I_{EN}	EN Pull-down Current EN = 5.0 V				µA
	33879	20	45	100	
	33879A and 33879B	20	45	110	
$V_{OUT(FLT-TH)}$	Output Fault Detection Voltage Threshold Outputs Programmed OFF				V
	33879	2.5	4.0	4.5	
	33879A and 33879B	2.5	4.0	5.0	
$I_{OUT(FLT-TH)}$	Output Fault Detection Current @ Threshold, Low-side Configuration Outputs Programmed OFF				µA
	33879	20	30	60	
	33879A and 33879B	20	30	115	

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4 Internal block diagram

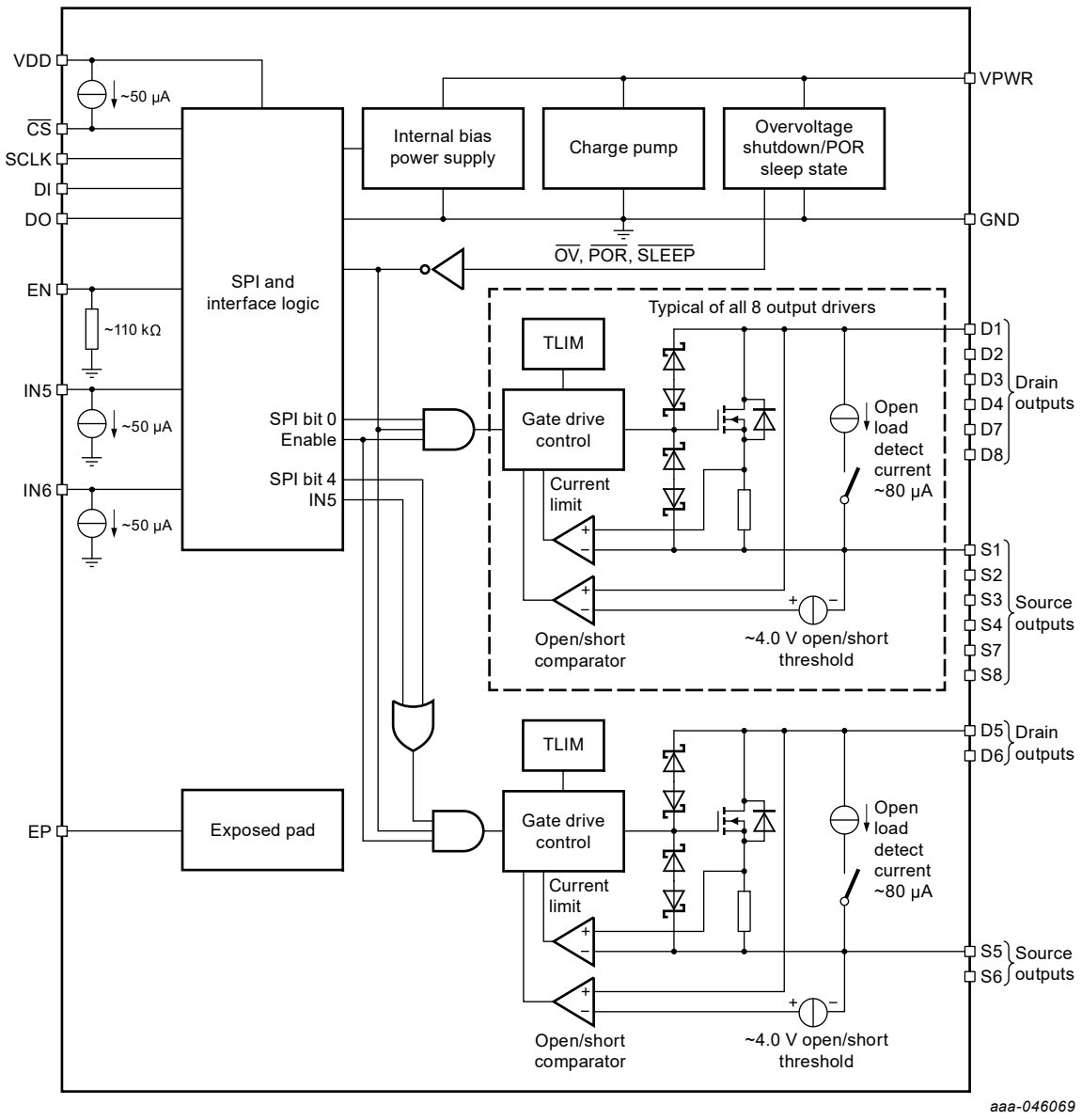

Figure 1. 33879 Simplified Internal Block Diagram

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5 Applications

- Solenoids
- Relays
- Actuators
- Stepper motors
- Brush DC motors
- Incandescent lamps

6 Simplified application diagram

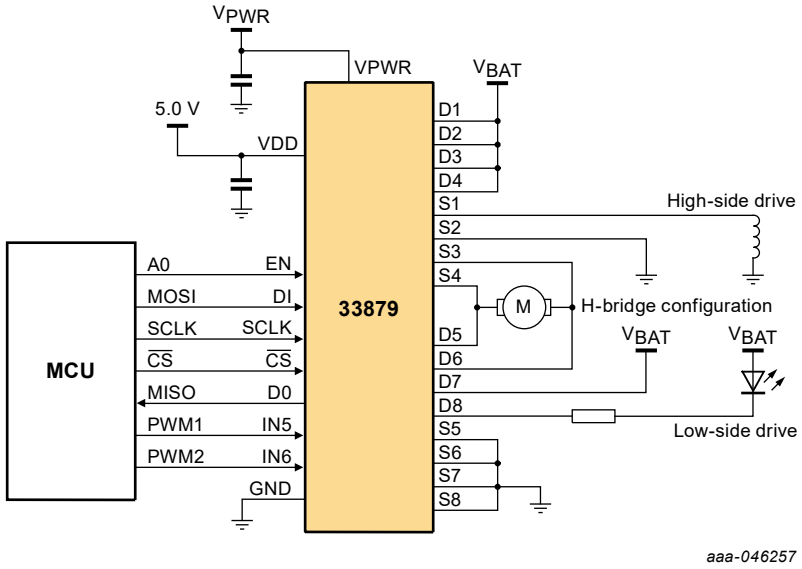

Figure 2. 33879 Simplified application diagram

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7 Pin connections

7.1 Pin diagram

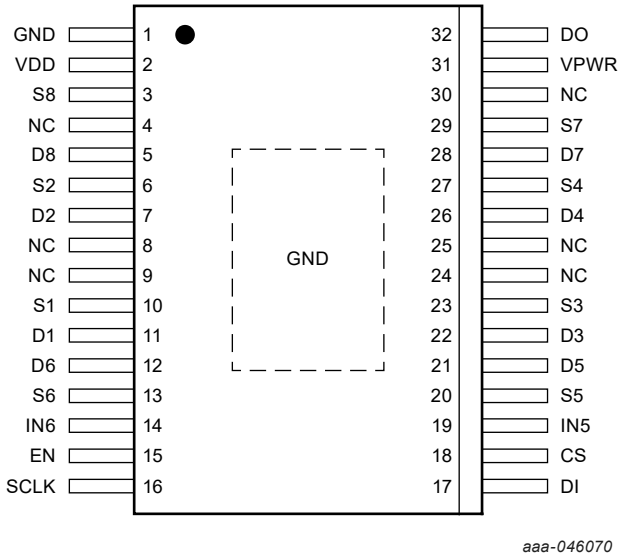

Figure 3. Pin diagram

7.2 Pin definitions

Table 3. Pin definitions

Number	Name	Function	Formal name	Definition
1	GND	Ground	Ground	Digital ground.
2	VDD	Input	Logic Supply Voltage	Logic supply for SPI interface. With VDD low the device is in Sleep mode.
3	S8	Output	Source Output 8	Output 8 MOSFET source pin.
4, 8, 9, 24, 25, 30	NC	No Connection	Not Connected	No internal connection to this pin.
5	D8	Output	Drain Output 8	Output 8 MOSFET drain pin.
6	S2	Output	Source Output 2	Output 2 MOSFET source pin.
7	D2	Output	Drain Output 2	Output 2 MOSFET drain pin.
10	S1	Output	Source Output 1	Output 1 MOSFET source pin.
11	D1	Output	Drain Output 1	Output 1 MOSFET drain pin.
12	D6	Output	Drain Output 6	Output 6 MOSFET drain pin.
13	S6	Output	Source Output 6	Output 6 MOSFET source pin.
14	IN6	Input	Command Input 6	PWM direct control input pin for output 6. IN6 is “OR” with SPI bit.
15	EN	Input	Enable Input	IC Enable. Active high. With EN low, the device is in Sleep mode.
16	SCLK	Clock	SPI Clock	SPI control clock input pin.
17	DI	Input	Serial Data Input	SPI control data input pin from MCU to the 33879. Logic [1] activates output.
18	CS	Input	SPI Chip Select	SPI control chip select input pin from MCU to the 33879. Logic [0] allows data to be transferred in.
19	IN5	Input	Command Input 5	PWM direct control input pin for output 5. IN5 is “OR” with SPI bit.

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Table 3. Pin definitions...*continued*

Number	Name	Function	Formal name	Definition
20	S5	Output	Source Output 5	Output 5 MOSFET source pin.
21	D5	Output	Drain Output 5	Output 5 MOSFET drain pin.
22	D3	Output	Drain Output 3	Output 3 MOSFET drain pin.
23	S3	Output	Source Output 3	Output 3 MOSFET source pin.
26	D4	Output	Drain Output 4	Output 4 MOSFET drain pin.
27	S4	Output	Source Output 4	Output 4 MOSFET source pin.
28	D7	Output	Drain Output 7	Output 7 MOSFET drain pin.
29	S7	Output	Source Output 7	Output 7 MOSFET source pin.
31	VPWR	Input	Battery Input	Power supply pin to the 33879. VPWR has internal reverse battery protection.
32	DO	Output	Serial Data Output	SPI control data output pin from the 33879 to the MCU. DO=0 no fault, DO=1 specific output has fault.
33	EP	Ground	Exposed Pad	Device performs as specified with the Exposed Pad un-terminated (floating) however, it is recommended the exposed pad be terminated to pin 1 (GND) and system ground.

8 Electrical characteristics

8.1 Maximum ratings

Table 4. Maximum ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (rating)	Min	Max	Unit
Electrical ratings				
V_{DD}	VDD Supply Voltage [1]	−0.3	7.0	V_{DC}
—	CS, DI, DO, SCLK, IN5, IN6, and EN [1]	−0.3	7.0	V_{DC}
V_{PWR}	V_{PWR} Supply Voltage [1]			V_{DC}
	33879	−16	40	
	33879A and 33879B	−16	45	
E_{CLAMP}	Output Clamp Energy [2]	50	50	mJ
	ESD Voltage [3]			V
V_{ESD1}	Human Body Model 33879	–450	+450	V
V_{ESD2}	Machine Model 33879	–100	+100	V
V_{ESD1}	Human Body Model 33879A and 33879B	–2000	+2000	V
V_{ESD2}	Machine Model 33879A and 33879B	–200	+200	V
Thermal ratings				
	Operating Temperature			
T_A	Ambient	−40	125	°C
T_J	Junction	–40	150	°C
T_C	Case	−40	125	°C

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Table 4. Maximum ratings*...continued*

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (rating)	Min	Max	Unit
T_{STG}	Storage Temperature	–55	150	°C
P_D	Power Dissipation [4]	—	1.7	W
	Thermal Resistance			
$R_{\theta JA}$	Junction to Ambient	—	71	°C/W
$R_{\theta JC}$	Between the Die and the Exposed Die Pad	—	1.2	°C/W
T_{PPRT}	Peak Package Reflow Temperature During Reflow [5] [6]	—	—	°C

[1] Exceeding these limits may cause malfunction or permanent damage to the device.
[2] Maximum output clamp energy capability at 150°C junction temperature using single non-repetitive pulse method with I = 350 mA.
[3] ESD1 testing is performed in accordance with the Human Body Model (CZAP = 100 pF, RZAP = 1500 Ω), ESD2 testing is performed in accordance with the Machine Model (CZAP = 200 pF, RZAP = 0 Ω).
[4] Maximum power dissipation at TA = 25 °C with no heatsink used.
[5] Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
[6] NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.nxp.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

8.2 Static electrical characteristics

Table 5. Static electrical characteristics

Characteristics noted under conditions 3.1 V ≤ VDD ≤ 5.5 V, 5.5 V ≤ VPWR ≤ 18 V, -40 °C ≤ TC ≤ 125 °C, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with VPWR = 13 V, TA = 25 °C.

Symbol	Description (rating)	Min	Typ	Max	Unit
Power input					
$V_{PWR(FO)}$	Supply Voltage Range				
	Fully Operational 33879	5.5	—	26.5	V
	33879A and 33879B	5.5	—	27.5	
$I_{PWR(ON)}$	Supply current	—	14	24	mA
$I_{PWR(SS)}$	Sleep State Supply Current				µA
	V_{DD} or EN ≤ 0.8 V, V_{PWR} = 13 V	—	2.0	5.0	
$I_{VDD(SS)}$	Sleep State Supply Current				µA
	EN ≤ 0.8 V, V_{DD} = 5.5 V	—	2.0	5.0	
$V_{PWR(OV)}$	VPWR Overvoltage Shutdown Threshold Voltage				
	33879	27	28.5	32	V
	33879A and 33879B	28	30	33	
$V_{PWR(OV-HYS)}$	V_{PWR} Overvoltage Shutdown Hysteresis Voltage	0.2	1.5	2.5	V
$V_{PWR(UV)}$	V_{PWR} Undervoltage Shutdown Threshold Voltage	3.0	4.0	5.0	V
$V_{PWR(UV-HYS)}$	V_{PWR} Undervoltage Shutdown Hysteresis Voltage	300	500	700	mV
V_{DD}	Logic Supply Voltage	3.1	—	5.5	V
I_{DD}	Logic Supply Current	250	400	700	µA
$V_{DD(SS)}$	Logic Supply Sleep State Threshold Voltage	0.8	2.5	3.0	V

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Table 5. Static electrical characteristics...*continued*

Characteristics noted under conditions 3.1 V ≤ VDD ≤ 5.5 V, 5.5 V ≤ VPWR ≤ 18 V, -40 °C ≤ TC ≤ 125 °C, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with VPWR = 13 V, TA = 25 °C.

Symbol	Description (rating)	Min	Typ	Max	Unit
Power output					
RDS(on)	Drain-to-Source ON Resistance (I_{OUT} = 0.350 A, V_{PWR} = 13 V)				Ω
	T_J = 125°C	—	—	1.4	
	T_J = 25°C	—	0.75	—	
	T_J = -40°C	—	—	—	
$I_{OUT(LIM)}$	Output Self Limiting Current High-side and Low-side Configurations	0.6	—	1.2	A
$V_{OUT(FLT-TH)}$	Output Fault Detection Voltage Threshold Outputs Programmed OFF [1]				V
	33879	2.5	4.0	4.5	
	33879A and 33879B	2.5	4.0	5.0	
$I_{OUT(FLT-TH)}$	Output Fault Detection Current @ Threshold, High-side Configuration Outputs Programmed OFF				µA
	33879	35	55	90	
	33879A and 33879B	35	55	150	
$I_{OUT(FLT-TH)}$	Output Fault Detection Current @ Threshold, Low-side Configuration Outputs Programmed OFF				µA
	33879	20	30	60	
	33879A and 33879B	20	30	115	
I_{OCO}	Output OFF Open Load Detection Current, High-side Configuration				µA
	V_{DRAIN} = 16 V, V_{SOURCE} = 0 V, Outputs Programmed OFF, V_{PWR} = 16 V				
	33879	65	100	160	
	33879A and 33879B	60	100	190	
I_{OCO}	Output OFF Open Load Detection Current, Low-side Configuration				µA
	V_{DRAIN} = 16 V, V_{SOURCE} = 0 V, Outputs Programmed OFF, V_{PWR} =16 V				
	33879	40	75	135	
	33879A and 33879B	40	75	150	
$V_{OC(LSD)}$	Output Clamp Voltage Low-side Drive				V
	I_D = 10 mA	40	45	55	
$V_{OC(HSD)}$	Output Clamp Voltage High-side Drive				V
	I_S = -10 mA	–15	–20	–25	
$I_{OUT(LKG)}$	Output Leakage Current High-side and Low-side Configurations				µA
	V_{DD} = 0 V, V_{DRAIN} = 16 V, V_{SOURCE} = 0 V	—	—	5.0	
$I_{OUT(LKG)}$	Output Leakage Current Low-side Configuration				µA
	V_{DD} = 5.0 V, V_{DRAIN} = 16 V, V_{SOURCE} = 0 V, Open Load Detection Current Disabled	—	—	5.0	
$I_{OUT(LKG)}$	Output Leakage Current High-side Configuration				µA
	V_{DD} = 5.0 V, V_{DRAIN} = 16 V, V_{SOURCE} = 0 V, Open Load Detection Current Disabled	—	—	20	
T_{LIM}	Overtemperature Shutdown [2]	155	—	185	°C
$T_{LIM(HYS)}$	Overtemperature Shutdown Hysteresis [2]	5.0	10	15	°C

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Table 5. Static electrical characteristics...*continued*

Characteristics noted under conditions 3.1 V ≤ VDD ≤ 5.5 V, 5.5 V ≤ VPWR ≤ 18 V, -40 °C ≤ TC ≤ 125 °C, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with VPWR = 13 V, TA = 25 °C.

Symbol	Description (rating)	Min	Typ	Max	Unit
Digital interface					
V_{IH}	Input Logic High-voltage Thresholds [3]	0.7 V_{DD}	—	V_{DD} + 0.3	V
V_{IL}	Input Logic Low-voltage Thresholds [3]	GND – 0.3	—	0.2 V_{DD}	V
I_{IN5}, I_{IN6}, I_{EN}	IN5, IN6, EN Input Logic Current				µA
	IN5, IN6, EN = 0 V	–10	—	10	
IIN5, IIN6	IN5, IN6 Pull-down Current				µA
	0.8 to 5.0 V	30	45	100	
I_{EN}	EN Pull-down Current, EN = 5.0 V				µA
	33879	20	45	100	
	33879A and 33879B	20	45	110	
I_{SCK}, I_{DI}, I_{TRI-DO}	SCLK, DI Input, Tri-state DO Output				µA
	0 to 5.0 V	–10	—	10	
I_{CS}	$\overline{CS}$ Input Current				µA
	$\overline{CS}$ = V_{DD}	–10	—	10	
I_{CS}	$\overline{CS}$ Pull-up Current				µA
	$\overline{CS}$ = 0 V	–30	—	–100	
$I_{CS(LKG)}$	$\overline{CS}$ Leakage Current to V_{DD}				µA
	$\overline{CS}$ = 5.0 V, V_{DD} = 0 V	—	—	10	
V_{DOHIGH}	DO High State Output Voltage				V
	$I_{DO-HIGH}$ = –1.6 mA	V_{DD} - 0.4	—	V_{DD}	
V_{DOLOW}	DO Low State Output Voltage				V
	I_{DO-LOW} = 1.6 mA	—	—	0.4	
C_{IN}	Input Capacitance on SCLK, DI, Tri-state DO, IN5, IN6, EN [2]	—	—	20	pF

[1] Output fault detection thresholds with outputs programmed OFF. Output fault detect thresholds are the same for output open and shorts
[2] This parameter is guaranteed by design; however, it is not production tested.
[3] Upper and lower logic threshold voltage levels apply to DI, CS, SCLK, IN5, IN6, and EN.

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8.3 Dynamic electrical characteristics

Table 6. Dynamic electrical characteristics

Characteristics noted under conditions 3.1 V ≤ VDD ≤ 5.5 V, 5.5 V ≤ VPWR ≤ 18 V, -40 °C ≤ TC ≤ 125 °C, unless otherwise noted. Where applicable, typical values reflect the parameter's approximate average value with VPWR = 13 V, TA = 25 °C.

Symbol	Description (rating)	Min	Typ	Max	Unit
Power output timing					
$t_{SR(RISE)}$	Output Slew Rate Low-side Configuration [1] R_{LOAD} = 620 Ω, CL = 200 pF	0.1	0.5	1.0	V/µs
$t_{SR(FALL)}$	Output Slew Rate Low-side Configuration [1] R_{LOAD} = 620 Ω, C_L = 200 pF	0.1	0.5	1.0	V/µs
$t_{SR(RISE)}$	Output Rise Time High-side Configuration [1] R_{LOAD} = 620 Ω, C_L = 200 pF	0.1	0.3	1.0	V/µs
$t_{SR(FALL)}$	Output Fall Time High-side Configuration [1] R_{LOAD} = 620 Ω, C_L = 200 pF	0.1	0.3	1.0	V/µs
$t_{DLY(ON)}$	Output Turn ON Delay Time, High-side and Low-side Configuration [2]	1.0	15	50	µs
$t_{DLY(OFF)}$	Output Turn OFF Delay Time, High-side and Low-side Configuration [2]	1.0	30	100	µs
t_{FAULT}	Output Fault Delay Time [3]	100	—	300	µs
t_{POR}	Power-ON Reset Delay Delay Time Required from Rising Edge of EN and V_{DD} to SPI Active	100	—	—	µs
t_{RESET}	Low-State Duration on V_{DD} or EN for Reset V_{DD} or EN ≤ 0.2 V	100	—	—	µs
Digital interface timing					
f_{SPI}	Recommended Frequency of SPI Operation [4]	—	4.0	—	MHz
t_{LEAD}	Falling Edge of $\overline{CS}$ to Rising Edge of SCLK (Required Setup Time)	100	—	—	ns
t_{LAG}	Falling Edge of SCLK to Rising Edge of $\overline{CS}$ (Required Setup Time)	50	—	—	ns
$t_{DI(SU)}$	DI to Falling Edge of SCLK (Required Setup Time)	16	—	—	ns
$t_{DI(HOLD)}$	Falling Edge of SCLK to DI (Required Hold Time)	20	—	—	ns
$t_{R(DI)}$	DI, $\overline{CS}$, SCLK Signal Rise Time [5]	—	5.0	—	ns
$t_{F(DI)}$	DI, $\overline{CS}$, SCLK Signal Fall Time [5]	—	5.0	—	ns
$t_{DO(EN)}$	Time from Falling Edge of $\overline{CS}$ to DO Low-impedance [6]	—	—	55	ns
$t_{DO(DIS)}$	Time from Rising Edge of $\overline{CS}$ to DO High-impedance [7]	—	—	55	ns
t_{VALID}	Time from Rising Edge of SCLK to DO Data Valid [8]	—	25	55	ns

[1] Output slew rate respectively measured across a 620 Ω resistive load at 10 to 90 percent and 90 to 10 percent voltage points. CL capacitor is connected from Drain or Source output to Ground.
[2] Output turn ON and OFF delay time measured from 50 percent rising edge of CS to the beginning of the 10 and 90 percent transition points.
[3] Duration of fault before fault bit is set. Duration between access times must be greater than 300 µs to read faults.
[4] This parameter is guaranteed by design. Production test equipment uses 4.16 MHz, 5.5 V/3.1 V SPI interface.
[5] Rise and Fall time of incoming DI, $\overline{CS}$, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
[6] Time required for output status data to be available for use at DO pin.
[7] Time required for output status data to be terminated at DO pin.
[8] Time required to obtain valid data out from DO following the rise of SCLK.

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8.4 Timing diagrams

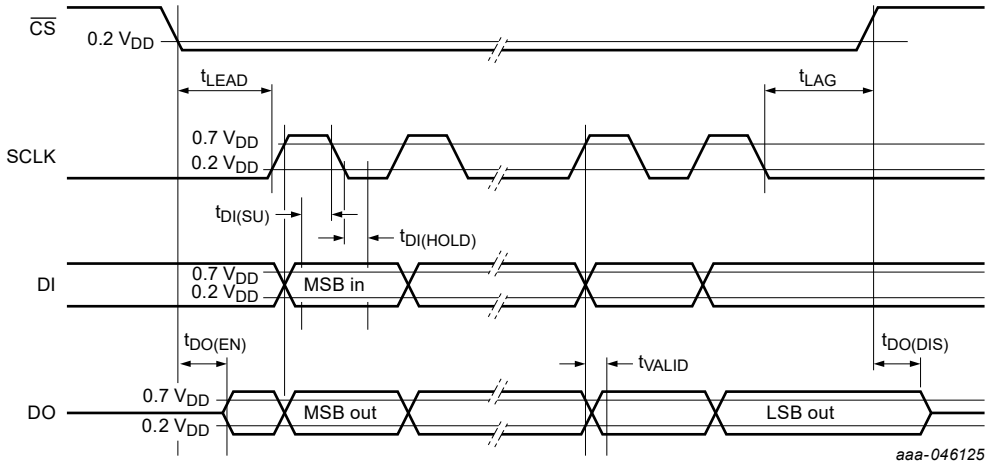

Figure 4. SPI timing diagram

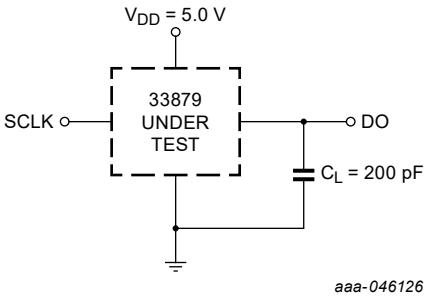

Figure 5. Valid Data Delay Time and Valid Time Test Circuit

Note: *CL represents the total capacitance of the test fixture and probe*

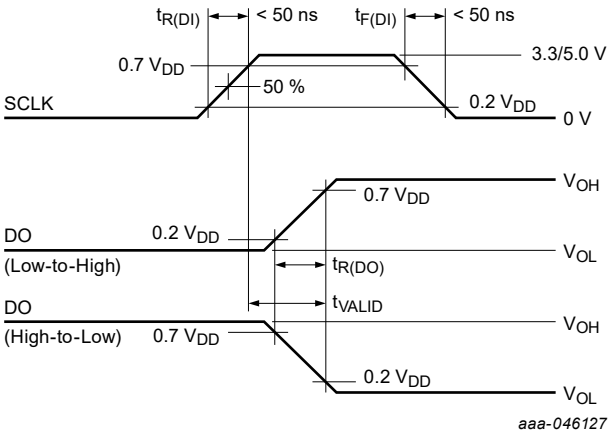

Figure 6. Valid data delay time and valid time waveforms

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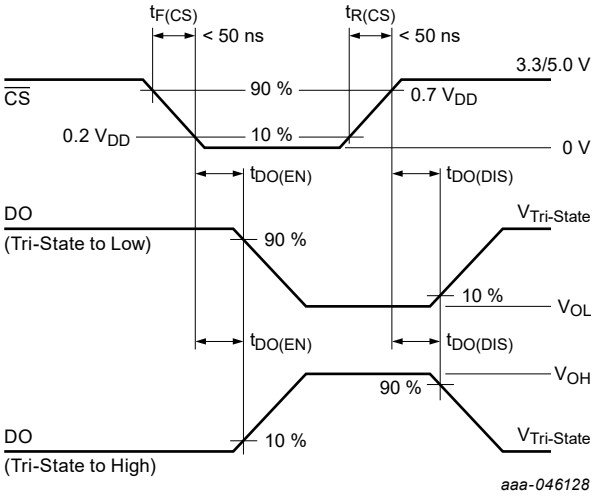

Figure 7. Enable and disable time waveforms

8.5 Typical electrical characteristics

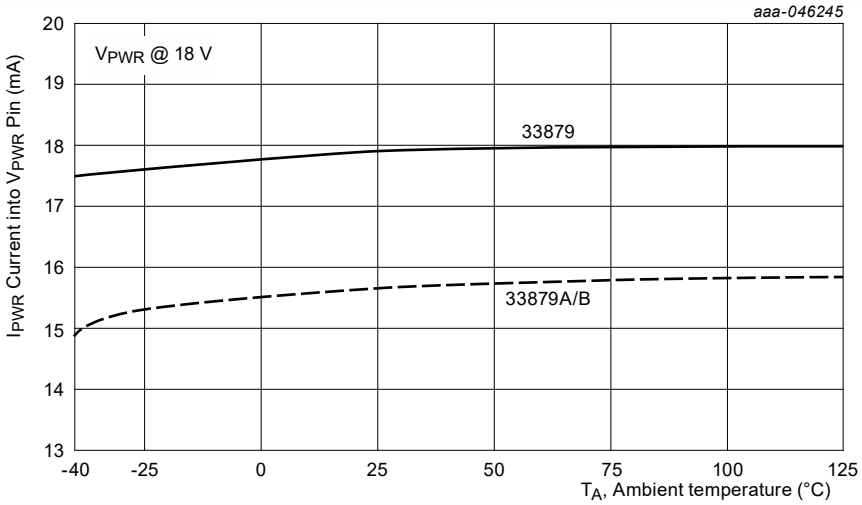

Figure 8. I_{PWR} vs. Temperature

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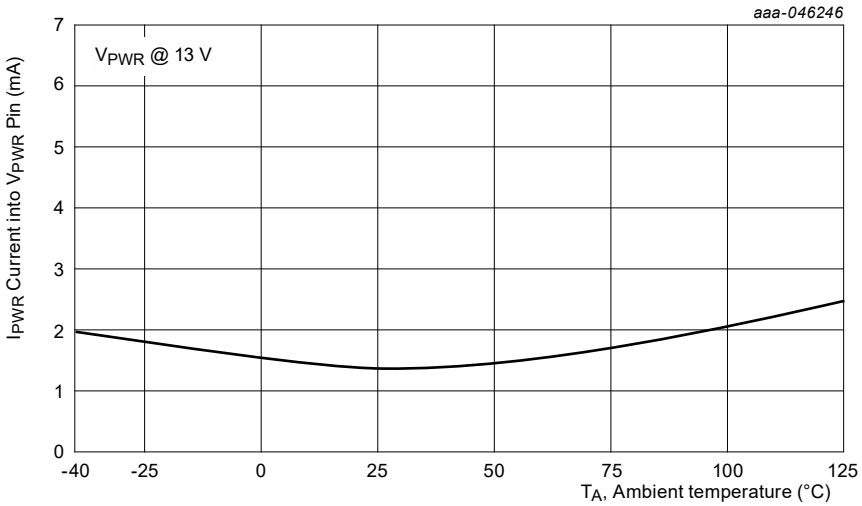

Figure 9. Sleep State I_{PWR} vs. Temperature

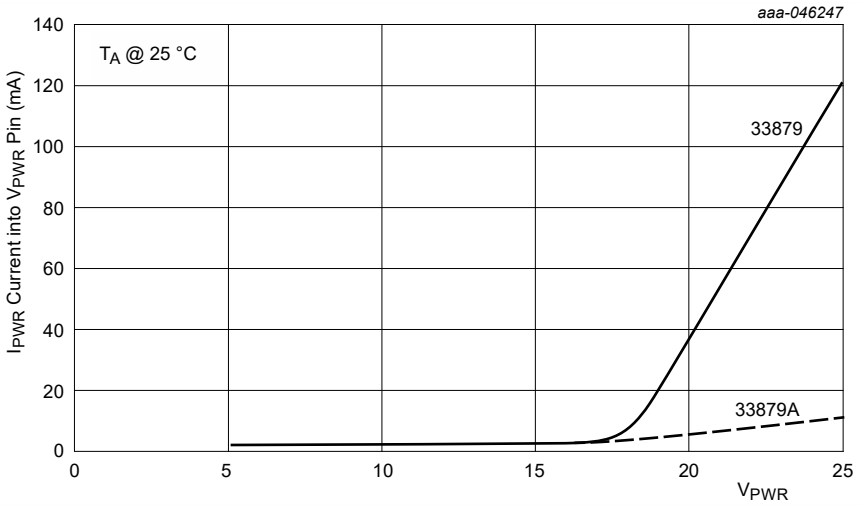

Figure 10. Sleep State I_{PWR} vs. V_{PWR}

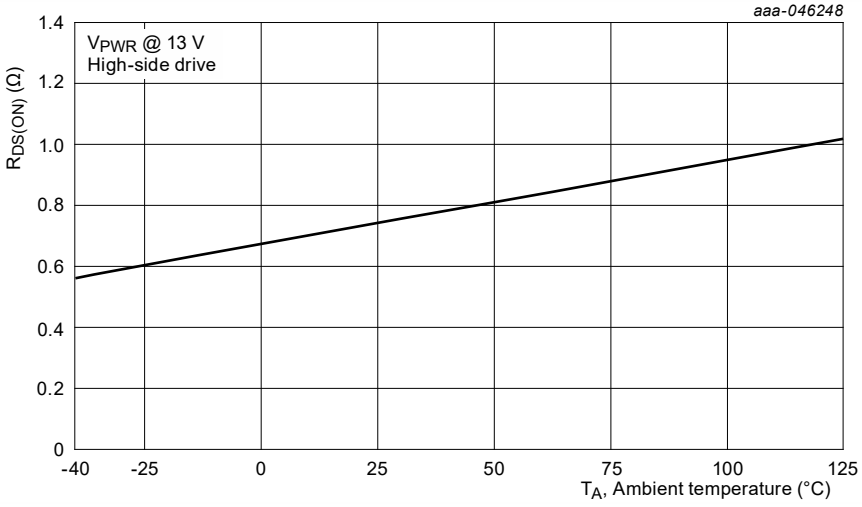

Figure 11. $R_{DS(ON)}$ vs. Temperature at 350 mA

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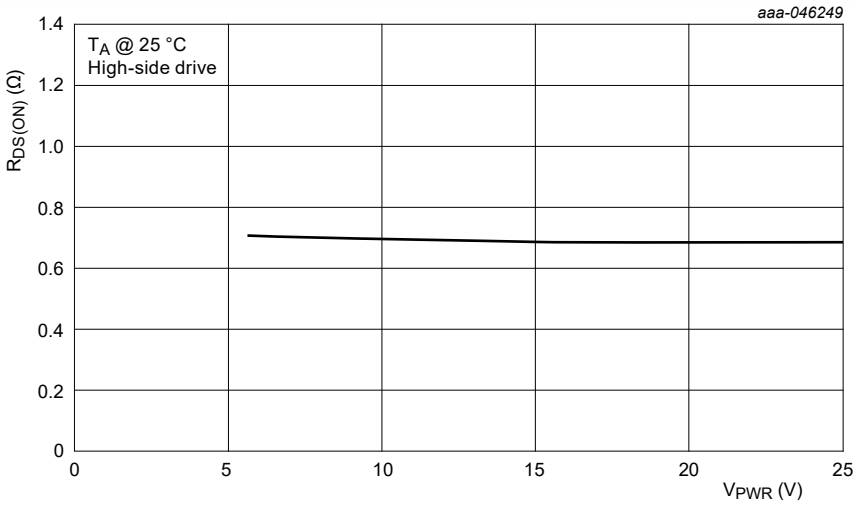

Figure 12. $R_{DS(ON)}$ vs. V_{PWR} at 350 mA

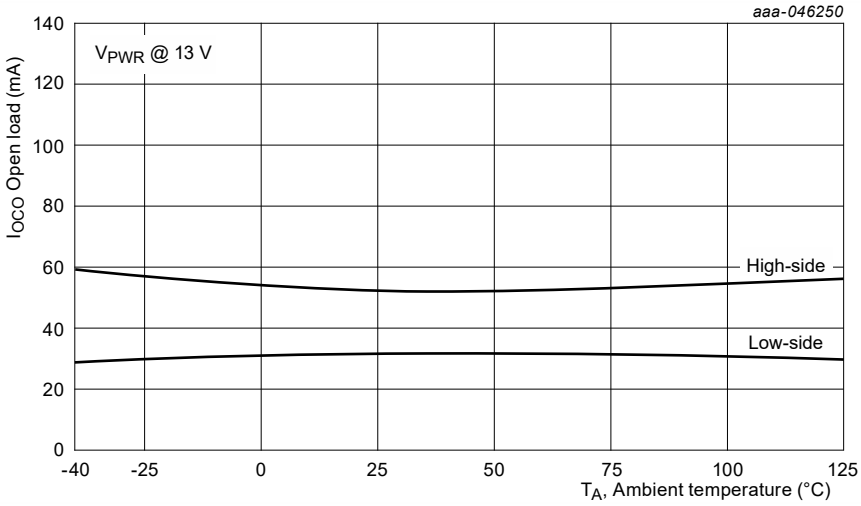

Figure 13. Open Load Detection Current at Threshold

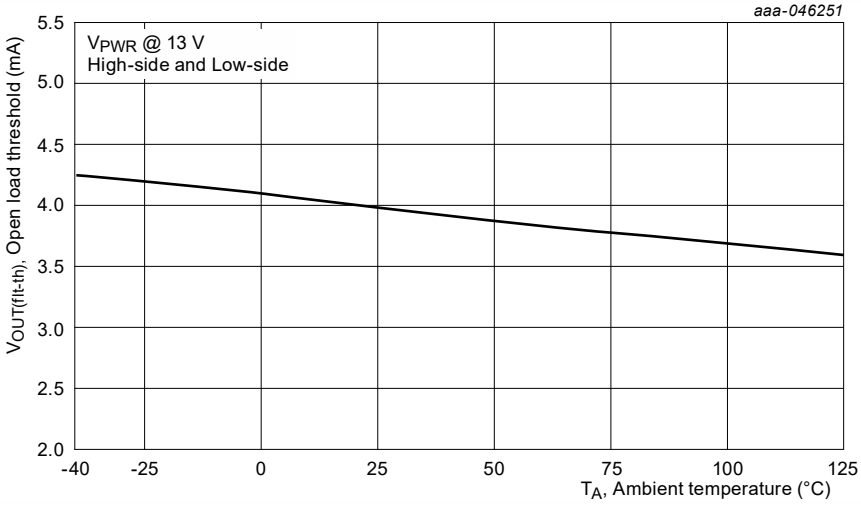

Figure 14. Open Load Detection Threshold vs. Temperature

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9 Functional description

9.1 Functional pin description

9.1.1 $\overline{CS}$ Pin

The system MCU selects the 33879 with which to communicate through the use of the chip select $\overline{CS}$ pin. Logic low on $\overline{CS}$ enables the data output (DO) driver and allows data to be transferred from the MCU to the 33879 and vice versa. Data clocked into the 33879 is acted upon on the rising edge of $\overline{CS}$. To avoid any spurious data, it is essential the high-to-low transition of the $\overline{CS}$ signal occur only when the SPI clock (SCLK) is in a logic low state.

9.1.2 SCLK Pin

The SCLK pin clocks the internal shift registers of the 33879. The serial data input (DI) pin is latched into the input shift register on the falling edge of the SCLK. The serial data output (DO) pin shifts data out of the shift register on the rising edge of the SCLK signal. False clocking of the shift register must be avoided to ensure validity of data. It is essential the SCLK pin be in a logic low state when the $\overline{CS}$ pin makes any transition. For this reason, it is recommended the SCLK pin is commanded to a logic low state when the device is not accessed ($\overline{CS}$ in logic high state). With $\overline{CS}$ in a logic high state, signals present on SCLK and DI are ignored and the DO output is in tri-state.

9.1.3 DI Pin

The DI pin is used for serial instruction data input. DI information is latched into the input register on the falling edge of SCLK. A logic high state present on DI programs a specific output on. The specific output turns on with the rising edge of the CS signal. Conversely, a logic low state present on the DI pin programs the output off. The specific output turns off with the rising edge of the CS signal. To program the eight outputs and open load detection current on or off, send the DI data beginning with the open load detection current bits, followed by output eight, output seven, and so on to output one. For each falling edge of the SCLK while CS is logic low, a data bit instruction (on or off) is loaded into the shift register per the data bit DI state. Sixteen bits of entered information is required to fill the input shift register.

9.1.4 DO Pin

The DO pin is the output from the shift register. The DO pin remains tri-state until the CS pin is in a logic low state. All faults on the 33879 device are reported as logic [1] through the DO data pin. Regardless of the configuration of the driver, open loads and shorted loads are reported as logic [1]. Conversely, normal operating outputs with non-faulted loads are reported as logic [0]. Outputs programmed with open load detection current disabled report logic [0] in the off state. The first eight positive transitions of SCLK report logic [0] followed by the status of the eight output drivers. The DI/DO shifting of data follows a first-in, first-out protocol with both input and output words transferring the most significant bit (MSB) first.

9.1.5 EN Pin

The EN pin on the 33879 enables the device. With the EN pin high, output drivers may be activated and open/short fault detection performed and reported. With the EN pin low, all outputs become inactive, open load detection current is disabled, and the device enters Sleep mode. The 33879 performs Power-ON Reset on the rising edge of the enable signal.

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9.1.6 IN5 and IN6 Pins

The IN5 and IN6 command inputs allow outputs five and six to be used in PWM applications. The IN5 and IN6 pins are OR-ed with the serial peripheral interface (SPI) command input bits. For SPI control of outputs five and six, the IN5 and IN6 pins should be grounded or held low by the microprocessor. When using IN5 or IN6 to PWM the output, the control SPI bit must be logic [0]. Maximum PWM frequency for each output is 2.0 kHz.

9.1.7 VDD Pin

The VDD input pin is used to determine logic levels on the microprocessor interface (SPI) pins. Current from VDD is used to drive the DO output and the pull-up current for $\overline{CS}$. V_{DD} must be applied for normal mode operation. The 33879 device performs Power-ON Reset with the application of V_{DD}.

9.1.8 VPWR Pin

The V_{PWR} pin is the battery input and Power-ON Reset to the 33879 IC. The VPWR pin has internal reverse battery protection. All internal logic current is provided from the VPWR pin. The 33879 performs Power-ON Reset with the application of V_{PWR}.

9.1.9 D1–D8 Pins

The D1 to D8 pins are the open-drain outputs of the 33879. For high-side drive configurations, the drain pins are connected to battery supply. In low-side drive configurations, the drain pins are connected to the low-side of the load. All outputs may be configured individually as desired. When configured as low-side drive, the 33879 limits the positive inductive transient to 45 V.

9.1.10 S1–S8 Pins

The S1 to S8 pins are the source outputs of the 33879. The source pins are connected directly to the load for high-side drive configurations. In low-side drive configurations, the source is connected to ground. All outputs may be configured individually as desired. When high-side drive is used, the 33879 will limit the negative inductive transient to negative 20 V.

9.1.11 Exposed Pad Pin

Device performs as specified with the Exposed Pad un-terminated (floating) however, it is recommended the Exposed Pad be terminated to pin 1 (GND) and system ground.

9.2 MCU Interface description

9.2.1 Introduction

The 33879 is an eight output hardware-configurable power switch with 16-bit serial control. A simplified internal block diagram of the 33879 is shown in Figure 2. The 33879 device uses high-efficiency up-drain power DMOS output transistors exhibiting low drain-to-source ON resistance (RDS(on) = 0.75 Ω at 25 °C typical) and dense CMOS control logic. All outputs have independent voltage clamps to provide fast inductive turn-off and transient protection.

In operation, the 33879 functions as an eight output serial switch, serving as an MCU bus expander and buffer with fault management and fault reporting features. In doing so, the device directly relieves the MCU of the fault management functions. This device directly interfaces to an MCU using a SPI for control and diagnostic readout. Figure 15 illustrates the basic SPI configuration between an MCU and one 33879.

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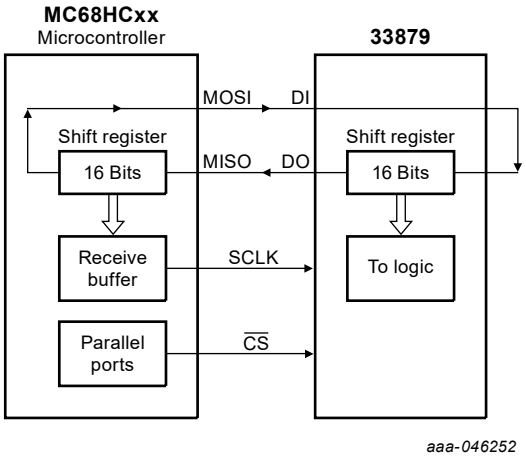

Figure 15. SPI Interface with microcontroller

All inputs are compatible with 5.0 V and 3.3 V CMOS logic levels and incorporate positive logic. When a SPI bit is programmed to a logic [0], the corresponding output is OFF. Conversely, when a SPI bit is programmed to logic [1] the output being controlled is ON. Diagnostics are treated in a similar manner. Outputs with a fault feed back (via DO) a logic [1] to the microcontroller, while normal operating outputs provide a logic [0].

Figure 16 illustrates the daisy chain configuration using the 33879. Data from the MCU is clocked daisy chain through each device while the CS bit is commanded low by the MCU. During each clock cycle, output status from the daisy chain is transferred to the MCU via the Master In Slave Out (MISO) line. On rising edge of CS, command data stored in the input register is then transferred to the output driver.

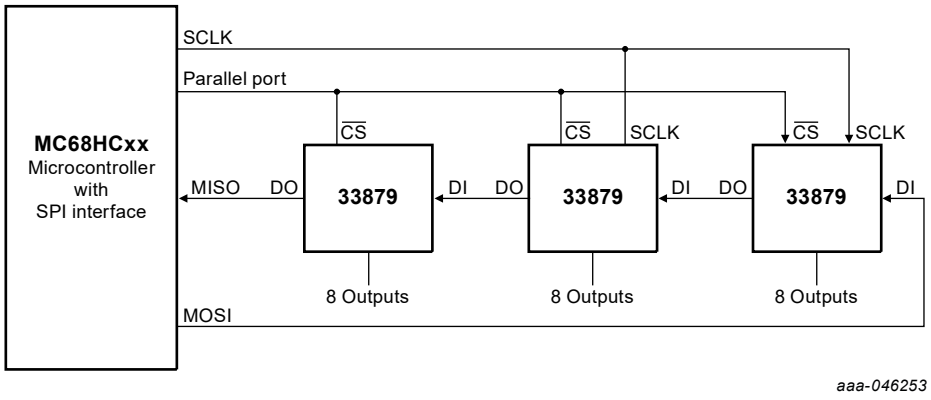

Figure 16. 33879 SPI System Daisy Chain

Multiple 33879 devices can be controlled in a parallel input fashion using the SPI. Figure 17 illustrates the control of 24 loads using three dedicated parallel MCU ports for chip select.

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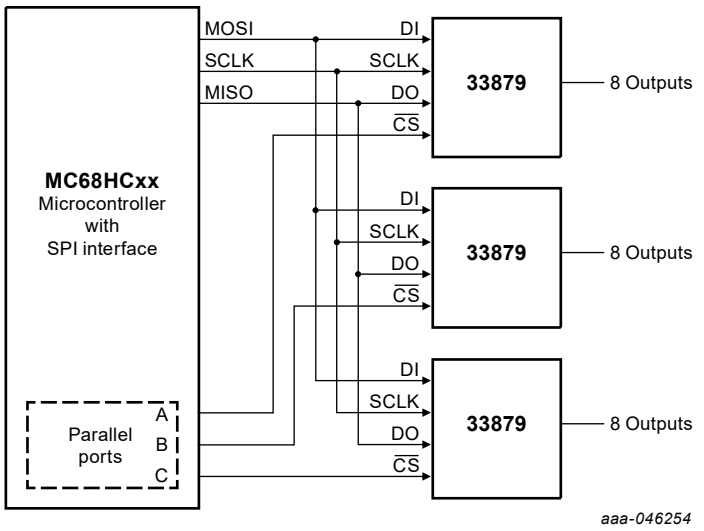

Figure 17. Parallel Input SPI Control

9.3 SPI Definition

A 16-bit command word is sent to the 33879 on each SPI communication and a 16-bit status word is received from the 33879. The MSB is sent and received first. As Table 7 shows, the Command Register defines the position and operation the 33879 performs on the rising edge of CS. The Fault Register, shown in Table 8, defines the previous state status of the output driver. Table 9 identifies the type of fault and the method by which the fault is communicated to the microprocessor.

Table 7. Command register definition

MSB															LSB
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
ON/ OFF Open Load Detect 8	ON/ OFF Open Load Detect 7	ON/ OFF Open Load Detect 6	ON/ OFF Open Load Detect 5	ON/ OFF Open Load Detect 4	ON/ OFF Open Load Detect 3	ON/ OFF Open Load Detect 2	ON/ OFF Open Load Detect 1	ON/ OFF OUT 8	ON/ OFF OUT 7	ON/ OFF OUT 6	ON/ OFF OUT 5	ON/ OFF OUT 4	ON/ OFF OUT 3	ON/ OFF OUT 2	ON/ OFF OUT 1

0 = Bits 0 to 7, Output commanded OFF.

0 = Bits 8 to 15, Open Load Detection Current OFF.

1 = Bits 0 to 7, Output commanded ON.

1 = Bits 8 to 15 Open Load Detection Current ON.

Table 8. Command register definition

MSB															LSB
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	0	0	0	0	0	0	0	OUT 8 Status	OUT 7 Status	OUT 6 Status	OUT 5 Status	OUT 4 Status	OUT 3 Status	OUT 2 Status	OUT 1 Status

0 = Bits 0 to 7, No Fault at Output.

1 = Bits 0 to 7, Output Short-to-Battery, Short-to-GND, Open Load, or TLIM.

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Bits 8 to 15 will always return “0”.

Table 9. Fault operation

Serial Output (DO) Pin Reports	
Overtemperature	Fault reported by serial output (DO) pin.
Overcurrent	DO pin reports short to battery/supply or overcurrent condition.
Output ON Open Load Fault	Not reported.
Output OFF Open Load Fault	DO pin reports output OFF open load condition only with Open Load Detection Current enabled.DO pin will report “0” for Output OFF Open Load Fault with Open Load Detection Current disabled.
Device Shutdowns	
Overvoltage	Total device shutdown at V_{PWR} = $V_{PWR(OV)}$ V. Resumes normal operation with proper voltage. All outputs assuming the previous state upon recovery from overvoltage.
Overtemperature	Only the output experiencing an overtemperature shuts down. Output assumes previous state upon recovery from overtemperature.

9.4 Device operation

9.4.1 Power supply

The 33879 device has been designed with ultra-low Sleep mode currents. The device may enter Sleep mode via the EN pin or the VDD pin. In the Sleep mode (EN or VDD ≤ 0.8 V), the current consumed by the VPWR pin is less than 5.0 µA. Placing the 33879 in Sleep mode resets the internal registers to the Power-ON Reset state. The reset state is defined as all outputs off and open load detection current disabled. To place the 33879 in the Sleep mode, either command all outputs off and apply logic low to the EN input pin or remove power from the VDD supply pin. Prior to removing V_{DD} from the device, it is recommended that all control inputs from the MCU be low.

9.4.2 Paralleling of outputs

Using MOSFETs as an output switch conveniently allows the paralleling of outputs for increased current capability. $R_{DS(on)}$ of MOSFETs have an inherent positive temperature coefficient providing balanced current sharing between outputs without destructive operation. This mode of operation may be desirable in the event the application requires lower power dissipation or the added capability of switching higher currents. Performance of parallel operation results in a corresponding decrease in $R_{DS(on)}$, while the output OFF open load detection currents and the output current limits increase correspondingly. Paralleling outputs from two or more different IC devices is possible, but not recommended.

9.4.3 Fault Logic Operation

Fault logic of the 33879 device has been greatly simplified over other devices using SPI communications. As command word one is being written into the shift register, a fault status word is being simultaneously written out and received by the MCU. Regardless of the configuration, with no outputs faulted and open load detection current enabled, all status bits being received by the MCU are zero. When outputs are faulted (off state open circuit or on state short-circuit/overtemperature), the status bits being received by the MCU are one. The distinction between open circuit fault and short/overtemperature is completed via the command word. For example, when a zero command bit is sent and a one fault is received in the following word, the fault is open/short-to-battery for high-side drive or open/short-to-ground for low-side drive. In the same manner, when a one command bit is sent and a one fault is received in the following word, the fault is a short-to-ground/

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overtemperature for high-side drive or short-to-battery/overtemperature for low-side drive. The timing between two write words must be greater than 300 µs to allow adequate time to sense and report the proper fault status.

9.4.4 SPI Integrity Check

Checking the integrity of the SPI communication with the initial power-up of the VDD and EN pins is recommended. After initial system start-up or reset, the MCU writes one 32-bit pattern to the 33879. The first 16 bits read by the MCU are 8 logic [0]s followed by the fault status of the outputs. The second 16 bits are the same bit pattern sent by the MCU. By the MCU receiving the same bit pattern it sent, bus integrity is confirmed. Note the second 16-bit pattern the MCU sends to the device is the command word and is transferred to the outputs with rising edge of CS. Important: A SCLK pulse count strategy has been implemented to ensure integrity of SPI communications. SPI messages consisting of 16 SCLK pulses and multiples of 8 clock pulses thereafter are acknowledged. SPI messages consisting of other than 16 + multiples of 8 SCLK pulses are ignored by the device.

9.4.5 Overtemperature Fault

Overtemperature detection and shutdown circuits are specifically incorporated for each individual output. The shutdown following an overtemperature condition is independent of the system clock or any other logic signal. Each independent output shuts down at 155 to 185 °C. When an output shuts down owing to an overtemperature fault, no other outputs are affected. The MCU recognizes the fault by a one in the fault status register. After the 33879 device has cooled below the switch point temperature and 15 °C hysteresis, the output activates unless otherwise told to shut down by the MCU via the SPI.

9.4.6 Overvoltage Fault

An overvoltage condition on the VPWR pin causes the device to shut down all outputs until the overvoltage condition is removed. When the overvoltage condition is removed, the outputs resume their previous state. This device does not detect an overvoltage on the VDD pin. The overvoltage threshold on the VPWR pin is specified as $V_{PWR(OV)}$ V, with 1.0 V typical hysteresis. A V_{PWR} overvoltage detection is global, causing all outputs to be turned OFF.

9.4.7 Output OFF Open Load Fault

An output OFF open load fault is the detection and reporting of an open load when the corresponding output is disabled (input bit programmed to a logic low state). The Output OFF Open Load fault is detected by comparing the drain-to-source voltage of the specific MOSFET output to an internally generated reference. Each output has one dedicated comparator for this purpose. An output OFF open load fault is indicated when the drain-to-source voltage is less than the output threshold voltage ($V_{OUT(FLT-TH)}$) of 2.5 to 4.0 V. Hence, the 33879 declares the load open in the OFF state when the output drain-to-source voltage is less than $V_{OUT(FLT-TH)}$.

This device has an internal 80 µA current source connected from drain to source of the output MOSFET. The current source may be programmed on or off via the SPI. The Power-ON Reset state for the current source is “off” and must be enabled via the SPI. To achieve low Sleep mode quiescent currents, the open load detection current source of each driver is switched off when VDD or EN is removed.

During output switching, especially with capacitive loads, a false output OFF open load fault may be triggered. To prevent this false fault from being reported, an internal fault filter of 100 µs to 300 µs is incorporated. A false fault reporting is a function of the load impedance, RDS(on), C_{OUT} of the MOSFET, as well as the supply voltage, V_{PWR}. The rising edge of $\overline{CS}$ triggers the built-in fault delay timer. The timer times out before the fault comparator is enabled and the fault is detected. Once the condition causing the open load fault is removed, the device resumes normal operation. The open load fault, however, is latched in the output DO register for the MCU to read.

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9.4.8 Shorted load fault

A shorted load (overcurrent) fault can be caused by any output being shorted directly to supply, or an output experiencing a current greater than the current limit. There are two safety circuits progressively in operation during load short conditions providing system protection:

- The device's output current is monitored in an analog fashion using SENSEFET approach and current limited.
- The device's output thermal limit is sensed and when attained causes only the specific faulted output to shutdown. The output remains off until cooled. The device then reasserts the output automatically. The cycle continues until fault is removed or the command bit instructs the output off. Shorted load faults are reported properly through the SPI regardless of open load detection current enable bits.

9.4.9 Undervoltage Shutdown

An undervoltage condition on VDD or VPWR results in the shutdown of all outputs. The V_{DD} undervoltage threshold is between 0.8 and 3.0 V. V_{PWR} undervoltage threshold is between 3.0 and 5.0 V. When the supplies fall below their respective thresholds, all outputs are turned OFF. As both supplies returns to normal levels, internal logic is reset and the device resumes normal operation.

9.4.10 Output voltage clamp

Each output of the 33879 incorporates an internal voltage clamp to provide fast turn-off and transient protection of each output. Each clamp independently limits the drain-to-source voltage to 45 V for low-side drive configurations and –20 V for high-side drive configurations. The total energy clamped (EJ) can be calculated by multiplying the current area under the current curve (I_A) times the clamp voltage (VCL). See Figure 18. Characterization of the output clamps, using a single pulse non-repetitive method at 0.35 A, indicates the maximum energy per output to be 50 mJ at 150°C junction temperature.

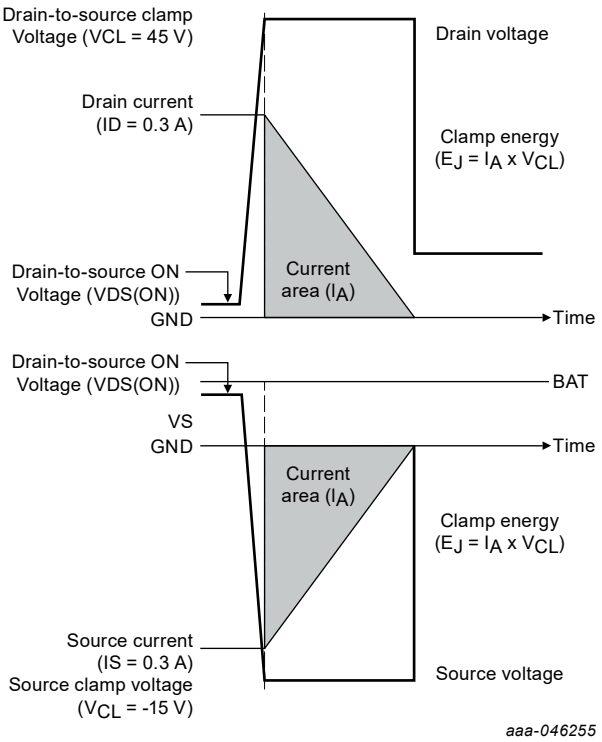

Figure 18. Output voltage clamping

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9.4.11 SPI configurations

The SPI configuration on the 33879 device is consistent with other devices in the Octal Serial Switch (OSS) family. This device may be used in serial SPI or parallel SPI with the 33298 and 33291. Different SPI configurations may be provided. For more information, contact NXP Analog Products Division or the local NXP representative.

9.4.12 Reverse battery

The 33879 has been designed with reverse battery protection on the VPWR pin. All outputs consist of a power MOSFET with an integral substrate diode. During the reverse battery condition, current flows through the load via the substrate diode. Under this circumstance, relays may energize and lamps turn on. Where load reverse battery protection is desired, a reverse battery blocking diode must be placed in series with the load.

10 Package Dimensions

Important: For the most current revision of the package, visit www.nxp.com and perform a keyword search using the “98ARL10543D” drawing number listed below. Dimensions shown are provided for reference ONLY.

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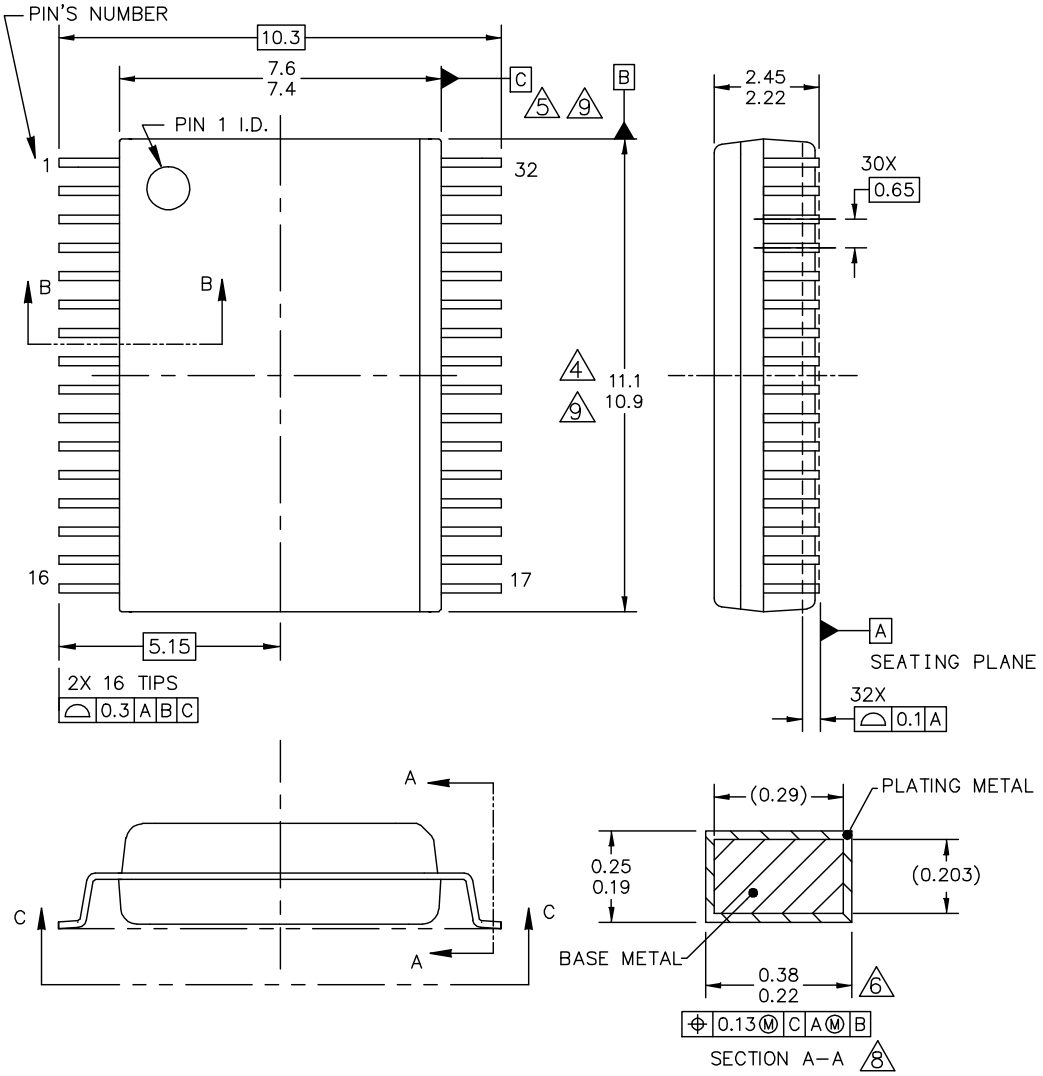

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	STANDARD: NON-JEDEC	
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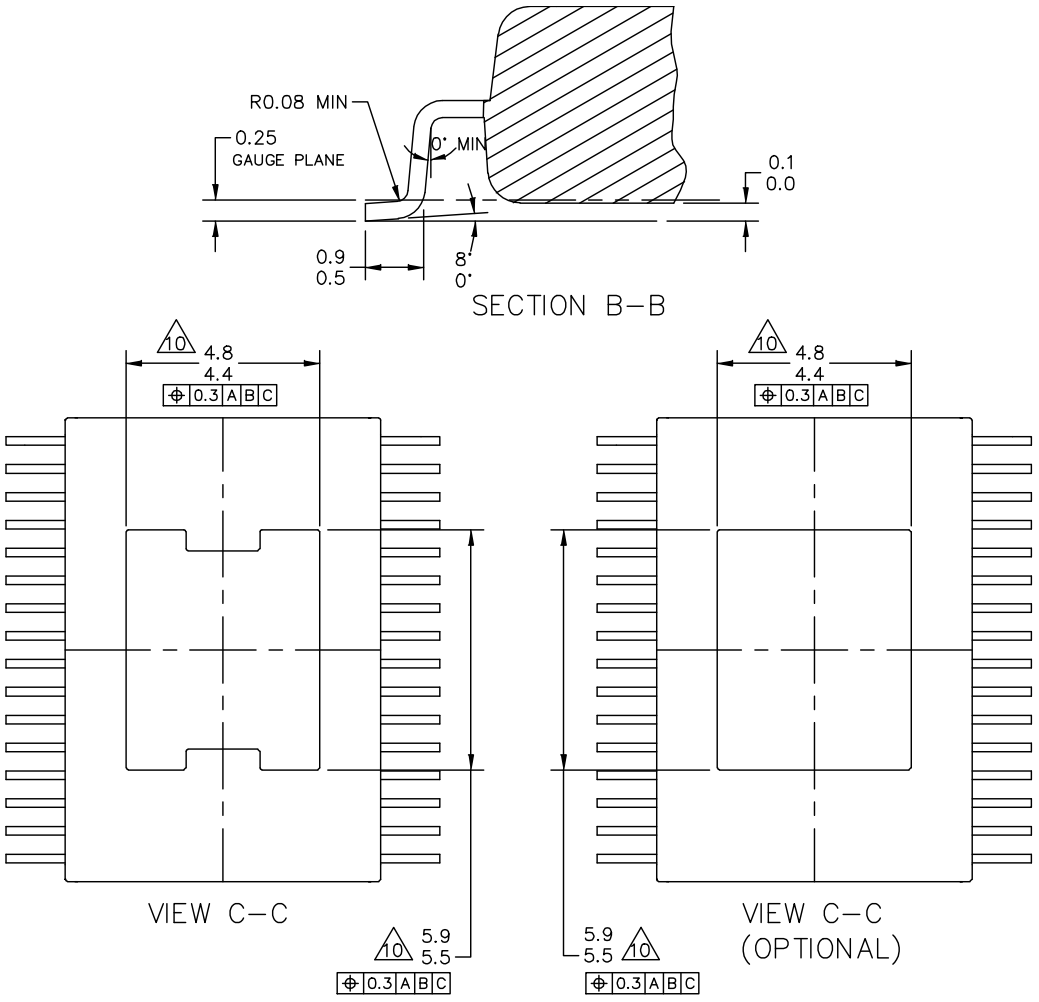

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NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 mm.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.3 mm FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER–LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
10. THESE DIMENSIONS RANGES DEFINE THE PRIMARY KEEP–OUT AREA. MOLD LOCKING AND RESIN BLEED CONTROL FEATURES MAY BE VISIBLE AND THEY MAY EXTEND TO 0.9mm FROM MAXIMUM EXPOSED PAD SIZE

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Figure 19. Package outline

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11 Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
MC33879 v.12.1	20230511	Product data sheet	202304027I	MC33879 v.12.0
Modifications	• Table 1: Changed part number to MC33879TEK from MC33879PEK			
MC33879 v.12.0	20220510	Product data sheet	202203027I	MC33879 v.11.0
MC33879 v.11.0	11/2015	Technical data sheet	-	MC33879 v.10.0
MC33879 v.10.0	6/2012	Technical data sheet	-	MC33879 v.9.0
MC33879 v.9.0	5/2012	Technical data sheet	-	MC33879 v.8.0
MC33879 v.8.0	10/2009	Technical data sheet	-	MC33879 v.7.0
MC33879 v.7.0	8/2008	Advance Information data sheet	-	MC33879 v.6.0
MC33879 v.6.0	6/2007	Advance Information data sheet	-	MC33879 v.5.0
MC33879 v.5.0	2/2006	Advance Information sheet	-	MC33879 v.4.0

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12 Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

12.2 Definitions

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