

MC14020B

14-Bit Binary Counter

The MC14020B 14-stage binary counter is constructed with MOS P-Channel and N-Channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 14 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency-dividing circuits.

Features

- Fully Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Buffered Outputs Available from stages 1 and 4 thru 14
- Common Reset Line
- Pin-for-Pin Replacement for CD4020B
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

| Symbol | Parameter | Value | Unit |
|-------------------|---|------------------------|-------------|
| V_{DD} | DC Supply Voltage Range | -0.5 to +18.0 | V |
| V_{in}, V_{out} | Input or Output Voltage Range (DC or Transient) | -0.5 to $V_{DD} + 0.5$ | V |
| I_{in}, I_{out} | Input or Output Current (DC or Transient) per Pin | ± 10 | mA |
| P_D | Power Dissipation, per Package (Note 1) | 500 | mW |
| T_A | Ambient Temperature Range | -55 to +125 | $^{\circ}C$ |
| T_{stg} | Storage Temperature Range | -65 to +150 | $^{\circ}C$ |
| T_L | Lead Temperature (8-Second Soldering) | 260 | $^{\circ}C$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Packages: -7.0 mW/ $^{\circ}C$ From 65 $^{\circ}C$ To 125 $^{\circ}C$

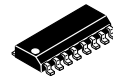
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



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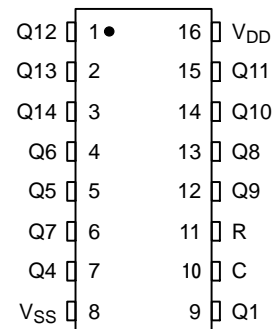


SOIC-16
D SUFFIX
CASE 751B

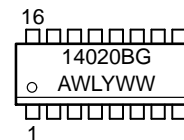


TSSOP-16
DT SUFFIX
CASE 948F

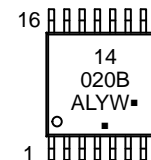
PIN ASSIGNMENT



MARKING DIAGRAMS



SOIC-16



TSSOP-16

- A = Assembly Location
- WL, L = Wafer Lot
- YY, Y = Year
- WW, W = Work Week
- G or ■ = Pb-Free Indicator

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

| Characteristic | Symbol | V _{DD} Vdc | -55°C | | 25°C | | | 125°C | | Unit | |
|---|-----------------|------------------------|---|-------|------|-----------------|-------|-------|-------|------|------|
| | | | Min | Max | Min | Typ (Note 2) | Max | Min | Max | | |
| Output Voltage V _{in} = V _{DD} or 0 | "0" Level | V _{OL} | 5.0 | - | 0.05 | - | 0 | 0.05 | - | 0.05 | Vdc |
| | | | 10 | - | 0.05 | - | 0 | 0.05 | - | 0.05 | |
| | | | 15 | - | 0.05 | - | 0 | 0.05 | - | 0.05 | |
| | "1" Level | V _{OH} | 5.0 | 4.95 | - | 4.95 | 5.0 | - | 4.95 | - | Vdc |
| | | | 10 | 9.95 | - | 9.95 | 10 | - | 9.95 | - | |
| | | | 15 | 14.95 | - | 14.95 | 15 | - | 14.95 | - | |
| Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc) | "0" Level | V _{IL} | 5.0 | - | 1.5 | - | 2.25 | 1.5 | - | 1.5 | Vdc |
| | | | 10 | - | 3.0 | - | 4.50 | 3.0 | - | 3.0 | |
| | | | 15 | - | 4.0 | - | 6.75 | 4.0 | - | 4.0 | |
| | "1" Level | V _{IH} | 5.0 | 3.5 | - | 3.5 | 2.75 | - | 3.5 | - | Vdc |
| | | | 10 | 7.0 | - | 7.0 | 5.50 | - | 7.0 | - | |
| | | | 15 | 11 | - | 11 | 8.25 | - | 11 | - | |
| Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) | Source | I _{OH} | 5.0 | -3.0 | - | -2.4 | -4.2 | - | -1.7 | - | mAdc |
| | | | 5.0 | -0.64 | - | -0.51 | -0.88 | - | -0.36 | - | |
| | | | 10 | -1.6 | - | -1.3 | -2.25 | - | -0.9 | - | |
| | | | 15 | -4.2 | - | -3.4 | -8.8 | - | -2.4 | - | |
| | Sink | I _{OL} | 5.0 | 0.64 | - | 0.51 | 0.88 | - | 0.36 | - | mAdc |
| | | | 10 | 1.6 | - | 1.3 | 2.25 | - | 0.9 | - | |
| 15 | | | 4.2 | - | 3.4 | 8.8 | - | 2.4 | - | | |
| Input Current | I _{in} | 15 | - | ±0.1 | - | ±0.00001 | ±0.1 | - | ±1.0 | µAdc | |
| Input Capacitance (V _{in} = 0) | C _{in} | - | - | - | - | 5.0 | 7.5 | - | - | pF | |
| Quiescent Current (Per Package) | I _{DD} | 5.0 | - | 5.0 | - | 0.005 | 5.0 | - | 150 | µAdc | |
| | | 10 | - | 10 | - | 0.010 | 10 | - | 300 | | |
| | | 15 | - | 20 | - | 0.015 | 20 | - | 600 | | |
| Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching) | I _T | 5.0 | I _T = (0.42 µA/kHz)f + I _{DD} | | | | | | | µAdc | |
| | | 10 | I _T = (0.85 µA/kHz)f + I _{DD} | | | | | | | | |
| | | 15 | I _T = (1.43 µA/kHz)f + I _{DD} | | | | | | | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
- The formulas given are for the typical characteristics only at 25°C.
- To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

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SWITCHING CHARACTERISTICS (Note 5) ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

| Characteristic | Symbol | V_{DD} Vdc | Min | Typ (Note 6) | Max | Unit |
|--|--------------------------|-----------------|--------------------|--------------------|----------------------|------|
| Output Rise and Fall Time t_{TLH} , $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ t_{TLH} , $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ t_{TLH} , $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$ | t_{TLH} , t_{THL} | 5.0 10 15 | – – – | 100 50 40 | 200 100 80 | ns |
| Propagation Delay Time Clock to Q1 t_{PHL} , $t_{PLH} = (1.7 \text{ ns/pF}) C_L + 175 \text{ ns}$ t_{PHL} , $t_{PLH} = (0.66 \text{ ns/pF}) C_L + 82 \text{ ns}$ t_{PHL} , $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 55 \text{ ns}$ | t_{PLH} , t_{PHL} | 5.0 10 15 | – – – | 260 115 80 | 520 230 160 | ns |
| Clock to Q14 t_{PHL} , $t_{PLH} = (1.7 \text{ ns/pF}) C_L + 1735 \text{ ns}$ t_{PHL} , $t_{PLH} = (0.66 \text{ ns/pF}) C_L + 772 \text{ ns}$ t_{PHL} , $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 535 \text{ ns}$ | | 5.0 10 15 | – – – | 1820 805 560 | 3900 1725 1200 | ns |
| Propagation Delay Time Reset to Q_n $t_{PHL} = (1.7 \text{ ns/pF}) C_L + 285 \text{ ns}$ $t_{PHL} = (0.66 \text{ ns/pF}) C_L + 122 \text{ ns}$ $t_{PHL} = (0.5 \text{ ns/pF}) C_L + 90 \text{ ns}$ | t_{PHL} | 5.0 10 15 | – – – | 370 155 115 | 740 310 230 | ns |
| Clock Pulse Width | t_{WH} | 5.0 10 15 | 500 165 125 | 140 55 38 | – – – | ns |
| Clock Pulse Frequency | f_{max} | 5.0 10 15 | 1.0 3.0 4.0 | 2.0 6.0 8.0 | – – – | MHz |
| Clock Rise and Fall Time | t_{TLH} , t_{THL} | 5.0 10 15 | No Limit | | | – |
| Reset Pulse Width | t_{WL} | 5.0 10 15 | 3000 550 420 | 320 120 80 | – – – | ns |
| Reset Recovery Time | t_{rec} | 5.0 10 15 | – – – | 65 25 15 | 130 50 30 | ns |

5. The formulas given are for the typical characteristics only at 25°C.

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

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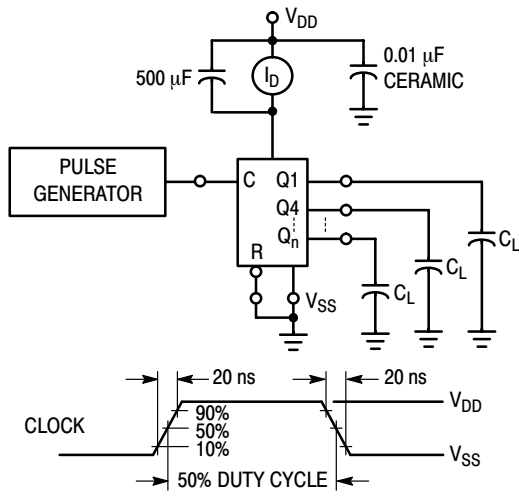


Figure 1. Power Dissipation Test Circuit and Waveform

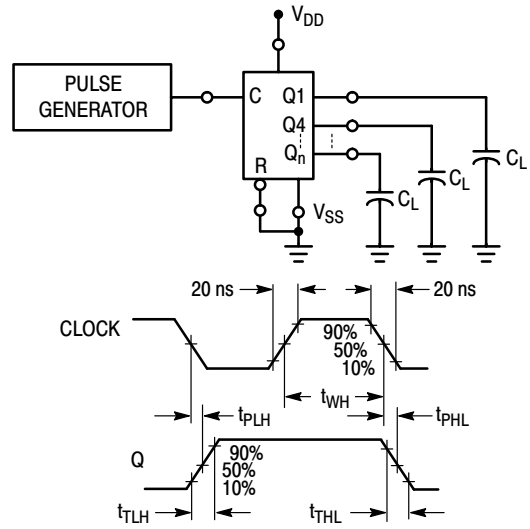


Figure 2. Switching Time Test Circuit and Waveforms

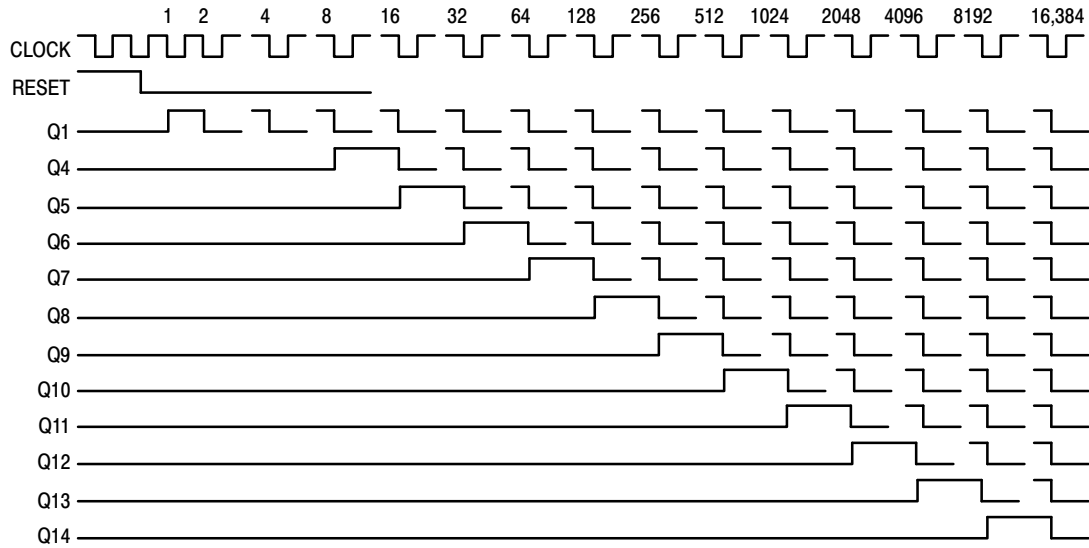
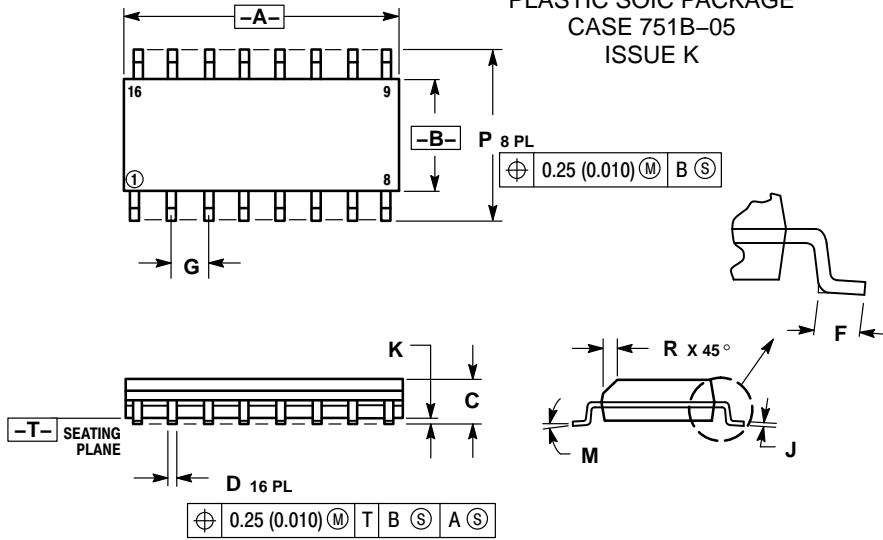


Figure 3. Timing Diagram

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PACKAGE DIMENSIONS

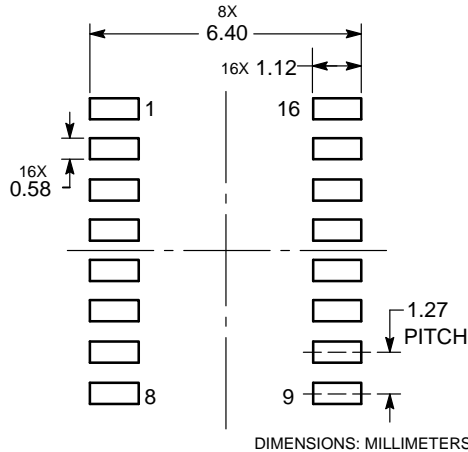
SOIC-16 D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE K



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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