



**THE DATASHEET OF
MC100LVEL11DR2G**



MC100LVEL11

3.3V ECL 1:2 Differential Fanout Buffer

Description

The MC100LVEL11 is a differential 1:2 fanout buffer. The device is functionally similar to the E111 device but with higher performance capabilities. Having within-device skews and output transition times significantly improved over the E111, the LVEL11 is ideally suited for those applications which require the ultimate in AC performance.

The differential inputs of the LVEL11 employ clamping circuitry to maintain stability under open input conditions. If the inputs are left open (pulled to V_{EE}) the Q outputs will go LOW.

Features

- 330 ps Propagation Delay
- 5 ps Skew Between Outputs
- High Bandwidth Output Transitions
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: $V_{CC} = 3.0\text{ V}$ to 3.8 V with $V_{EE} = 0\text{ V}$
- NECL Mode Operating Range: $V_{CC} = 0\text{ V}$ with $V_{EE} = -3.0\text{ V}$ to -3.8 V
- Internal Input Pulldown Resistors on D, Pullup and Pulldown Resistors on \bar{D}
- Q Output will Default LOW with Inputs Open or at V_{EE}
- These Devices are Pb-Free and are RoHS Compliant

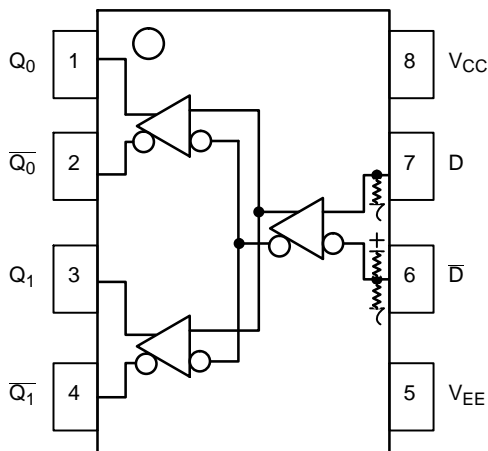


Figure 1. Logic Diagram and Pinout Assignment



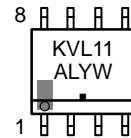
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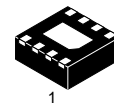
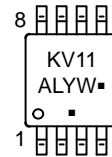
MARKING DIAGRAMS*



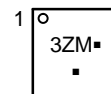
SOIC-8
D SUFFIX
CASE 751



TSSOP-8
DT SUFFIX
CASE 948R



DFN8
MN SUFFIX
CASE 506AA



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

MC100LVEL11

Table 1. PIN DESCRIPTION

| Pin | Function |
|---|--|
| Q0, $\overline{Q0}$; Q1, $\overline{Q1}$ | ECL Data Outputs |
| D, \overline{D} | ECL Data Inputs |
| V _{CC} | Positive Supply |
| V _{EE} | Negative Supply |
| EP | (DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open. |

Table 2. ATTRIBUTES

| Characteristics | Value |
|---|--|
| Internal Input Pulldown Resistor | 75 k Ω |
| Internal Input Pullup Resistor | 75 k Ω |
| ESD Protection | Human Body Model Machine Model Charge Device Model |
| | > 4 kV > 400 V > 2 kV |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) | |
| | SOIC-8 TSSOP-8 DFN8 |
| | Level 1 Level 3 Level 1 |
| Flammability Rating | Oxygen Index: 28 to 34 |
| | UL 94 V-0 @ 0.125 in |
| Transistor Count | 63 |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | |

1. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Units |
|------------------|--|--|--|-------------------|--------------|
| V _{CC} | PECL Mode Power Supply | V _{EE} = 0 V | | 8 to 0 | V |
| V _{EE} | NECL Mode Power Supply | V _{CC} = 0 V | | -8 to 0 | V |
| V _I | PECL Mode Input Voltage NECL Mode Input Voltage | V _{EE} = 0 V V _{CC} = 0 V | V _I ≤ V _{CC} V _I ≥ V _{EE} | 6 to 0 -6 to 0 | V |
| I _{out} | Output Current | Continuous Surge | | 50 100 | mA mA |
| T _A | Operating Temperature Range | | | -40 to +95 | °C |
| T _{stg} | Storage Temperature Range | | | -65 to +150 | °C |
| θ_{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lpfm 500 lpfm | SOIC-8 SOIC-8 | 190 130 | °C/W °C/W |
| θ_{JC} | Thermal Resistance (Junction-to-Case) | Standard Board | SOIC-8 | 41 to 44 ± 5% | °C/W |
| θ_{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lpfm 500 lpfm | TSSOP-8 TSSOP-8 | 185 140 | °C/W °C/W |
| θ_{JC} | Thermal Resistance (Junction-to-Case) | Standard Board | TSSOP-8 | 41 to 44 ± 5% | °C/W |
| θ_{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lpfm 500 lpfm | DFN8 DFN8 | 129 84 | °C/W °C/W |
| T _{sol} | Wave Solder | Pb-Free | <2 to 3 sec @ 260°C | 265 | °C |
| θ_{JC} | Thermal Resistance (Junction-to-Case) | (Note 2) | DFN8 | 35 to 40 | °C/W |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

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Table 4. LVPECL DC CHARACTERISTICS $V_{CC} = 3.3\text{ V}$; $V_{EE} = 0.0\text{ V}$ (Note 3)

| Symbol | Characteristic | -40°C | | | 25°C | | | 95°C | | | Unit |
|-------------|---|-----------|------|------|------|------|------|------|------|------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | | 24 | 28 | | 24 | 28 | | 25 | 30 | mA |
| V_{OH} | Output HIGH Voltage (Note 4) | 2215 | 2295 | 2420 | 2275 | 2345 | 2420 | 2275 | 2345 | 2420 | mV |
| V_{OL} | Output LOW Voltage (Note 4) | 1470 | 1605 | 1745 | 1490 | 1595 | 1680 | 1490 | 1595 | 1680 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | 2135 | | 2420 | 2135 | | 2420 | 2135 | | 2420 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | 1490 | | 1825 | 1490 | | 1825 | 1490 | | 1825 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential) (Note 8) $V_{pp} < 500\text{ mV}$ $V_{pp} \geq 500\text{ mV}$ | 1.2 | | 3.1 | 1.1 | | 3.1 | 1.1 | | 3.1 | V |
| | | 1.4 | | 3.1 | 1.3 | | 3.1 | 1.3 | | 3.1 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | D | 0.5 | | 0.5 | | | 0.5 | | | μA |
| | | \bar{D} | -600 | | -600 | | | -600 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

- Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $\pm 0.3\text{ V}$.
- Outputs are terminated through a $50\ \Omega$ resistor to $V_{CC} - 2.0\text{ V}$.
- V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{ppmin} and 1.0 V .

Table 5. LVNECL DC CHARACTERISTICS $V_{CC} = 0.0\text{ V}$; $V_{EE} = -3.3\text{ V}$ (Note 6)

| Symbol | Characteristic | -40°C | | | 25°C | | | 95°C | | | Unit |
|-------------|---|-----------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | | 24 | 28 | | 24 | 28 | | 25 | 30 | mA |
| V_{OH} | Output HIGH Voltage (Note 7) | -1085 | -1005 | -880 | -1025 | -955 | -880 | -1025 | -955 | -880 | mV |
| V_{OL} | Output LOW Voltage (Note 7) | -1830 | -1695 | -1555 | -1810 | -1705 | -1620 | -1810 | -1705 | -1620 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | -1165 | | -880 | -1165 | | -880 | -1165 | | -880 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | -1810 | | -1475 | -1810 | | -1475 | -1810 | | -1475 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential) (Note 8) $V_{pp} < 500\text{ mV}$ $V_{pp} \geq 500\text{ mV}$ | -2.1 | | -0.2 | -2.2 | | -0.2 | -2.2 | | -0.2 | V |
| | | -1.9 | | -0.2 | -2.0 | | -0.2 | -2.0 | | -0.2 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | D | 0.5 | | 0.5 | | | 0.5 | | | μA |
| | | \bar{D} | -600 | | -600 | | | -600 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

- Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $\pm 0.3\text{ V}$.
- Outputs are terminated through a $50\ \Omega$ resistor to $V_{CC} - 2.0\text{ V}$.
- V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{ppmin} and 1.0 V .

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Table 6. AC CHARACTERISTICS $V_{CC} = 3.3\text{ V}$; $V_{EE} = 0.0\text{ V}$ or $V_{CC} = 0.0\text{ V}$; $V_{EE} = -3.3\text{ V}$ (Note 9)

| Symbol | Characteristic | -40°C | | | 25°C | | | 95°C | | | Unit |
|------------------------|---|-------|---------|-----------------|------|---------|-----------------|------|---------|-----------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| f_{\max} | Maximum Toggle Frequency | | | | | 1.0 | | | | | GHz |
| t_{PLH} t_{PHL} | Propagation Delay to Output | 235 | | 385 | 255 | 330 | 405 | 285 | | 435 | ps |
| t_{SKEW} | Within-Device Skew (Note 10) Device-to-Device (Note 11) Duty Cycle Skew (Note 12) | | 5 10 | 20 150 20 | | 5 10 | 20 150 20 | | 5 10 | 20 150 20 | ps |
| t_{JITTER} | Random Clock Jitter (RMS) | | | | | 0.6 | | | | | ps |
| V_{PP} | Input Swing (Note 13) | 200 | | 1000 | 200 | | 1000 | 200 | | 1000 | mV |
| t_r t_f | Output Rise/Fall Times Q (20% – 80%) | 120 | | 320 | 120 | 220 | 320 | 120 | | 320 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

9. V_{EE} can vary $\pm 0.3\text{ V}$.

10. Within-device skew defined as identical transitions on similar paths through a device.

11. Device-to-device skew for identical transitions at identical V_{CC} levels.

12. Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.

13. $V_{PP}(\min)$ is the minimum input swing for which AC parameters guaranteed. The device will function properly with input swings below 200 mV, however, AC delays may move outside of the specified range. The device has a DC gain of ≈ 40 .

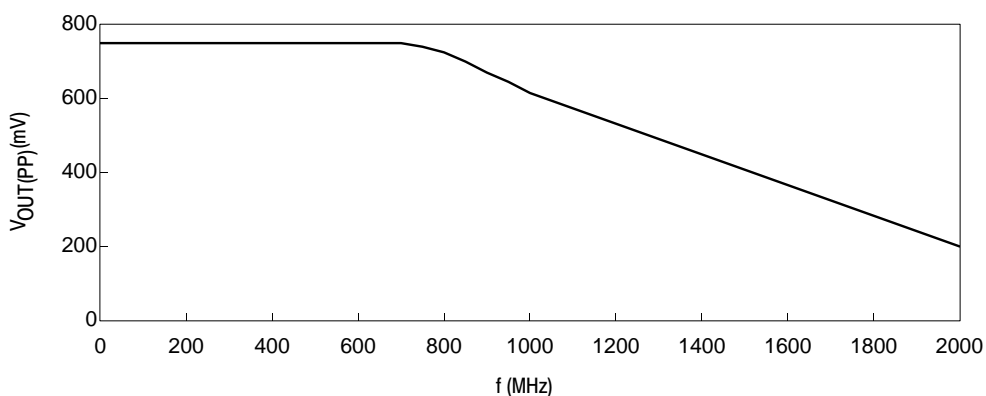


Figure 2. Output Swing versus Frequency

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ORDERING INFORMATION

| Device | Package | Shipping† |
|-------------------|----------------------|--------------------|
| MC100LEVEL11DG | SOIC-8 (Pb-Free) | 98 Units / Rail |
| MC100LEVEL11DR2G | SOIC-8 (Pb-Free) | 2500 / Tape & Reel |
| MC100LEVEL11DTG | TSSOP-8 (Pb-Free) | 100 Units / Rail |
| MC100LEVEL11DTR2G | TSSOP-8 (Pb-Free) | 2500 / Tape & Reel |
| MC100LEVEL11MNR4G | DFN8 (Pb-Free) | 1000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

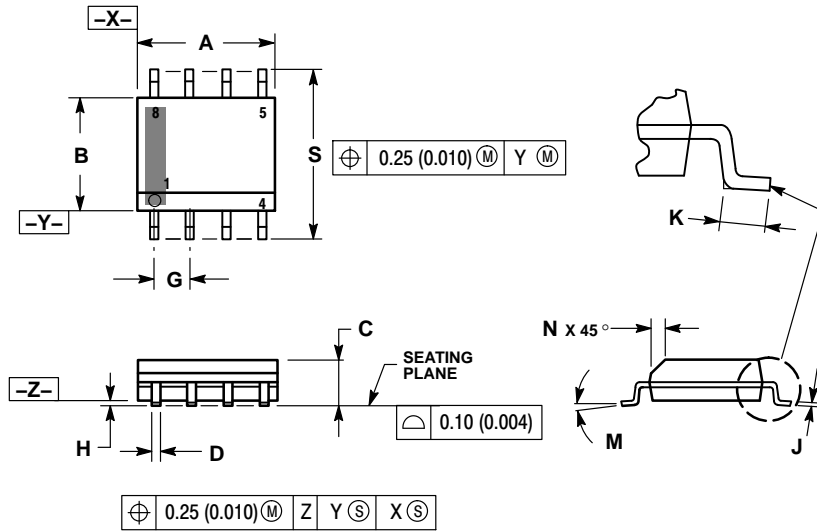
Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

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PACKAGE DIMENSIONS

SOIC-8 NB
CASE 751-07
ISSUE AK

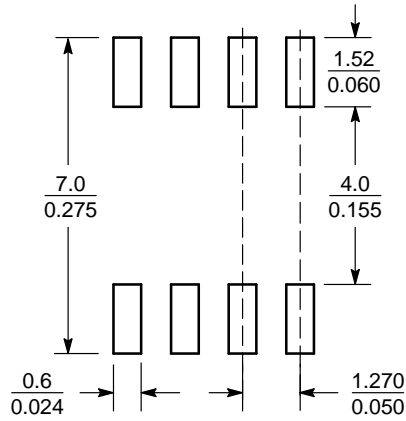


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

SOLDERING FOOTPRINT*



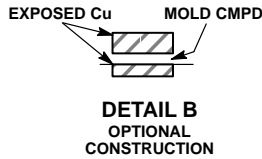
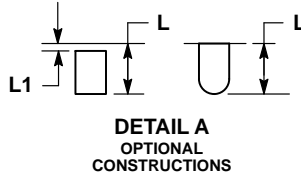
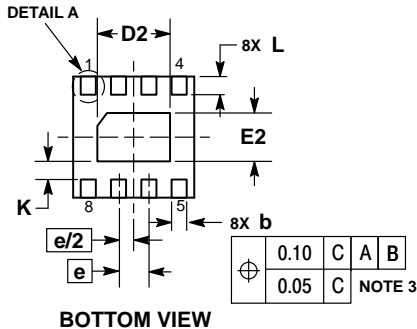
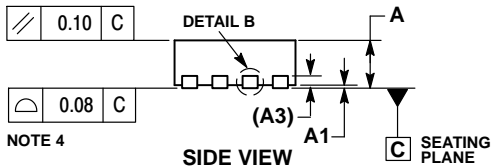
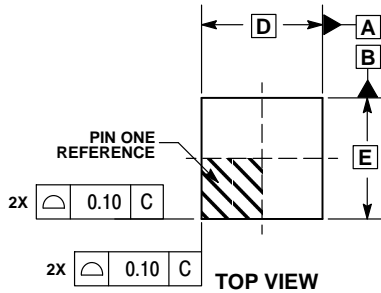
SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC100LVEL11

PACKAGE DIMENSIONS

DFN8 2x2, 0.5P
CASE 506AA
ISSUE E

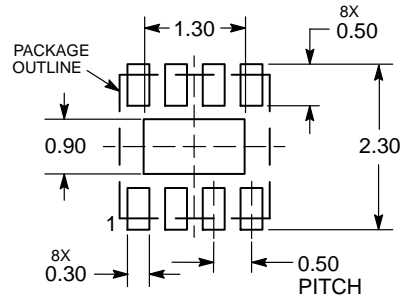


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.20 | 0.30 |
| D | 2.00 BSC | |
| D2 | 1.10 | 1.30 |
| E | 2.00 BSC | |
| E2 | 0.70 | 0.90 |
| e | 0.50 BSC | |
| K | 0.30 REF | |
| L | 0.25 | 0.35 |
| L1 | --- | 0.10 |


RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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