



**THE DATASHEET OF  
MB95F398HPMC-G-SNE2**





## MB95F394H/F396K/F398H/F394K/F396H/F398K

# CMOS F<sup>2</sup>MC-8FX MB95390H Series 8-bit Microcontrollers

MB95390H is a series of general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers of this series contain a variety of peripheral resources.

## Features

### F<sup>2</sup>MC-8FX CPU core

Instruction set optimized for controllers

- Multiplication and division instructions
- 16-bit arithmetic operations
- Bit test branch instructions
- Bit manipulation instructions, etc.

### Clock

- Selectable main clock source

Main OSC clock (up to 16.25 MHz, maximum machine clock frequency: 8.125 MHz)

External clock (up to 32.5 MHz, maximum machine clock frequency: 16.25 MHz)

Main CR clock (1/8/10/12.5 MHz  $\pm 2\%$  or  $\pm 2.5\%^*$ , maximum machine clock frequency: 12.5 MHz)

\*The main CR clock oscillation accuracy of a product in LQFP package (FPT-48P-M49 or FPT-52P-M02) is  $\pm 2\%$  and that of a product in QFN package (LCC-48P-M11) is  $\pm 2.5\%$ .

- Selectable subclock source

Sub-OSC clock (32.768 kHz)

External clock (32.768 kHz)

Sub-CR clock (Typ: 100 kHz, Min: 50 kHz, Max: 200 kHz)

### Timer

- 8/16-bit composite timer  $\times 2$  channels
- 8/16-bit PPG  $\times 3$  channels
- 16-bit PPG  $\times 1$  channel (can work independently or together with the multi-pulse generator)
- 16-bit reload timer  $\times 1$  channel (can work independently or together with the multi-pulse generator)
- Time-base timer  $\times 1$  channel
- Watch prescaler  $\times 1$  channel

### UART/SIO $\times 1$ channel

- Full duplex double buffer
- Capable of clock-asynchronous (UART) serial data transfer and clock-synchronous (SIO) serial data transfer

### I<sup>2</sup>C $\times 1$ channel

- Built-in wake-up function

### Multi-pulse generator (MPG) (for DC motor control) $\times 1$ channel

- 16-bit reload timer  $\times 1$  channel
- 16-bit PPG timer  $\times 1$  channel
- Waveform sequencer (including a 16-bit timer equipped with a buffer and a compare clear function)

### LIN-UART

- Full duplex double buffer
- Capable of clock-synchronous serial data transfer and clock-asynchronous serial data transfer

### External interrupt $\times 8$ channels

- Interrupt by edge detection (rising edge, falling edge, and both edges can be selected)
- Can be used to wake up the device from different low power consumption (standby) modes

### 8/10-bit A/D converter $\times 12$ channels

- 8-bit and 10-bit resolution can be chosen.

### Low power consumption (standby) modes

- Stop mode
- Sleep mode
- Watch mode
- Time-base timer mode

### I/O port

- MB95F394H/F396H/F398H (maximum no. of I/O ports: 44)  
General-purpose I/O ports (N-ch open drain)..... : 3  
General-purpose I/O ports (CMOS I/O)..... : 41
- MB95F394K/F396K/F398K (maximum no. of I/O ports: 45)  
General-purpose I/O ports (N-ch open drain)..... : 4  
General-purpose I/O ports (CMOS I/O)..... : 41

### **On-chip debug**

- 1-wire serial control
- Serial writing supported (asynchronous mode)

### **Hardware/software watchdog timer**

- Built-in hardware watchdog timer
- Built-in software watchdog timer

### **Low-voltage detection reset circuit**

- Built-in low-voltage detector

### **Clock supervisor counter**

- Built-in clock supervisor counter function

### **Programmable port input voltage level**

- CMOS input level / hysteresis input level

### **Dual operation Flash memory**

- The erase/write operation and the read operation can be executed in different banks (upper bank/lower bank) simultaneously.

### **Flash memory security function**

- Protects the content of the Flash memory

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**1. Product Line-up**

Part number	MB95F394H	MB95F396H	MB95F398H	MB95F394K	MB95F396K	MB95F398K
<b>Parameter</b>						
Type	Flash memory product					
Clock supervisor counter	It supervises the main clock oscillation.					
Program ROM capacity	20 Kbyte	36 Kbyte	60 Kbyte	20 Kbyte	36 Kbyte	60 Kbyte
RAM capacity	496 bytes	1008 bytes	2032 bytes	496 bytes	1008 bytes	2032 bytes
Low-voltage detection reset	No			Yes		
Reset input	Dedicated			Selected through software		
CPU functions	<ul style="list-style-type: none"> <li>• Number of basic instructions : 136</li> <li>• Instruction bit length : 8 bits</li> <li>• Instruction length : 1 to 3 bytes</li> <li>• Data bit length : 1, 8 and 16 bits</li> <li>• Minimum instruction execution time : 61.5 ns (with machine clock frequency = 16.25 MHz)</li> <li>• Interrupt processing time : 0.6 μs (with machine clock frequency = 16.25 MHz)</li> </ul>					
General-purpose I/O	<ul style="list-style-type: none"> <li>• I/O ports (Max) : 44</li> <li>• CMOS I/O : 41</li> <li>• N-ch open drain : 3</li> </ul>			<ul style="list-style-type: none"> <li>• I/O ports (Max) : 45</li> <li>• CMOS I/O : 41</li> <li>• N-ch open drain : 4</li> </ul>		
Time-base timer	Interval time: 0.256 ms to 8.3 s (with external clock frequency = 4 MHz)					
Hardware/software watchdog timer	<ul style="list-style-type: none"> <li>• Reset generation cycle               <ul style="list-style-type: none"> <li>- Main oscillation clock at 10 MHz: 105 ms (Min)</li> </ul> </li> <li>• The sub-CR clock can be used as the source clock of the hardware watchdog timer.</li> </ul>					
Wild register	It can be used to replace three bytes of data.					
LIN-UART	<ul style="list-style-type: none"> <li>• A wide range of communication speeds can be selected by a dedicated reload timer.</li> <li>• Clock-synchronous serial data transfer and clock-asynchronous serial data transfer is enabled.</li> <li>• The LIN function can be used as a LIN master or a LIN slave.</li> </ul>					
8/10-bit A/D converter	12 channels					
	8-bit resolution and 10-bit resolution can be chosen.					
8/16-bit composite timer	2 channels					
	<ul style="list-style-type: none"> <li>• The timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel".</li> <li>• It has the following functions: timer function, PWC function, PWM function and input capture function.</li> <li>• Count clock: it can be selected from internal clocks (seven types) and external clocks.</li> <li>• It can output square wave.</li> </ul>					
External interrupt	8 channels					
	<ul style="list-style-type: none"> <li>• Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.)</li> <li>• It can be used to wake up the device from different standby modes.</li> </ul>					
On-chip debug	<ul style="list-style-type: none"> <li>• 1-wire serial control</li> <li>• It supports serial writing. (asynchronous mode)</li> </ul>					

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Part number	MB95F394H	MB95F396H	MB95F398H	MB95F394K	MB95F396K	MB95F398K
Parameter						
UART/SIO	1 channel <ul style="list-style-type: none"> <li>Data transfer with UART/SIO is enabled.</li> <li>It has a full duplex double buffer, variable data length (5/6/7/8 bits), a built-in baud rate generator and an error detection function.</li> <li>It uses the NRZ type transfer format.</li> <li>LSB-first data transfer and MSB-first data transfer are available to use.</li> <li>Clock-asynchronous (UART) serial data transfer and clock-synchronous (SIO) serial data transfer is enabled.</li> </ul>					
I <sup>2</sup> C	1 channel <ul style="list-style-type: none"> <li>Master/slave transmission and receiving</li> <li>It has the following functions: bus error function, arbitration function, transmission direction detection function, wake-up function, and functions of generating and detecting repeated START conditions.</li> </ul>					
8/16-bit PPG	3 channels <ul style="list-style-type: none"> <li>Each channel of PPG can be used as two 8-bit PPG channels or a single 16-bit PPG channel.</li> <li>The counter operating clock can be selected from eight clock sources.</li> </ul>					
16-bit PPG	<ul style="list-style-type: none"> <li>PWM mode and one-shot mode are available to use.</li> <li>The counter operating clock can be selected from eight clock sources.</li> <li>It supports external trigger start.</li> <li>It can work independently or together with the multi-pulse generator.</li> </ul>					
16-bit reload timer	<ul style="list-style-type: none"> <li>Two clock modes and two counter operating modes are available to use.</li> <li>It can output square waveform.</li> <li>Count clock: it can be selected from internal clocks (seven types) and external clocks.</li> <li>Two counter operating modes: reload mode and one-shot mode</li> <li>It can work independently or together with the multi-pulse generator.</li> </ul>					
Multi-pulse generator (for DC motor control)	<ul style="list-style-type: none"> <li>16-bit PPG timer: 1 channel</li> <li>16-bit reload timer operations: toggle output, one-shot output</li> <li>Event counter: 1 channel</li> <li>Waveform sequencer (including a 16-bit timer equipped with a buffer and a compare clear function)</li> </ul>					
Watch prescaler	Eight different time intervals can be selected.					
Flash memory	<ul style="list-style-type: none"> <li>It supports automatic programming, Embedded Algorithm, and write/erase/erase-suspend/erase-resume commands.</li> <li>It has a flag indicating the completion of the operation of Embedded Algorithm.</li> <li>Number of write/erase cycles: 100000</li> <li>Data retention time: 20 years</li> <li>Flash security feature for protecting the content of the Flash memory</li> </ul>					
Standby mode	Sleep mode, stop mode, watch mode, time-base timer mode					
Package	FPT-48P-M49 FPT-52P-M02 LCC-48P-M11					

**2. Packages and Corresponding Products**

<b>Part number</b>	<b>MB95F394H</b>	<b>MB95F396H</b>	<b>MB95F398H</b>	<b>MB95F394K</b>	<b>MB95F396K</b>	<b>MB95F398K</b>
<b>Package</b>						
FPT-48P-M49	O	O	O	O	O	O
FPT-52P-M02	O	O	O	O	O	O
LCC-48P-M11	O	O	O	O	O	O

O: Available

### 3. Differences Among Products and Notes on Product Selection

#### ■ Current consumption

When using the on-chip debug function, take account of the current consumption of flash erase/write.

For details of current consumption, see “Electrical Characteristics”.

#### ■ Package

For details of information on each package, see “Packages and Corresponding Products” and “Package Dimension”.

#### ■ Operating voltage

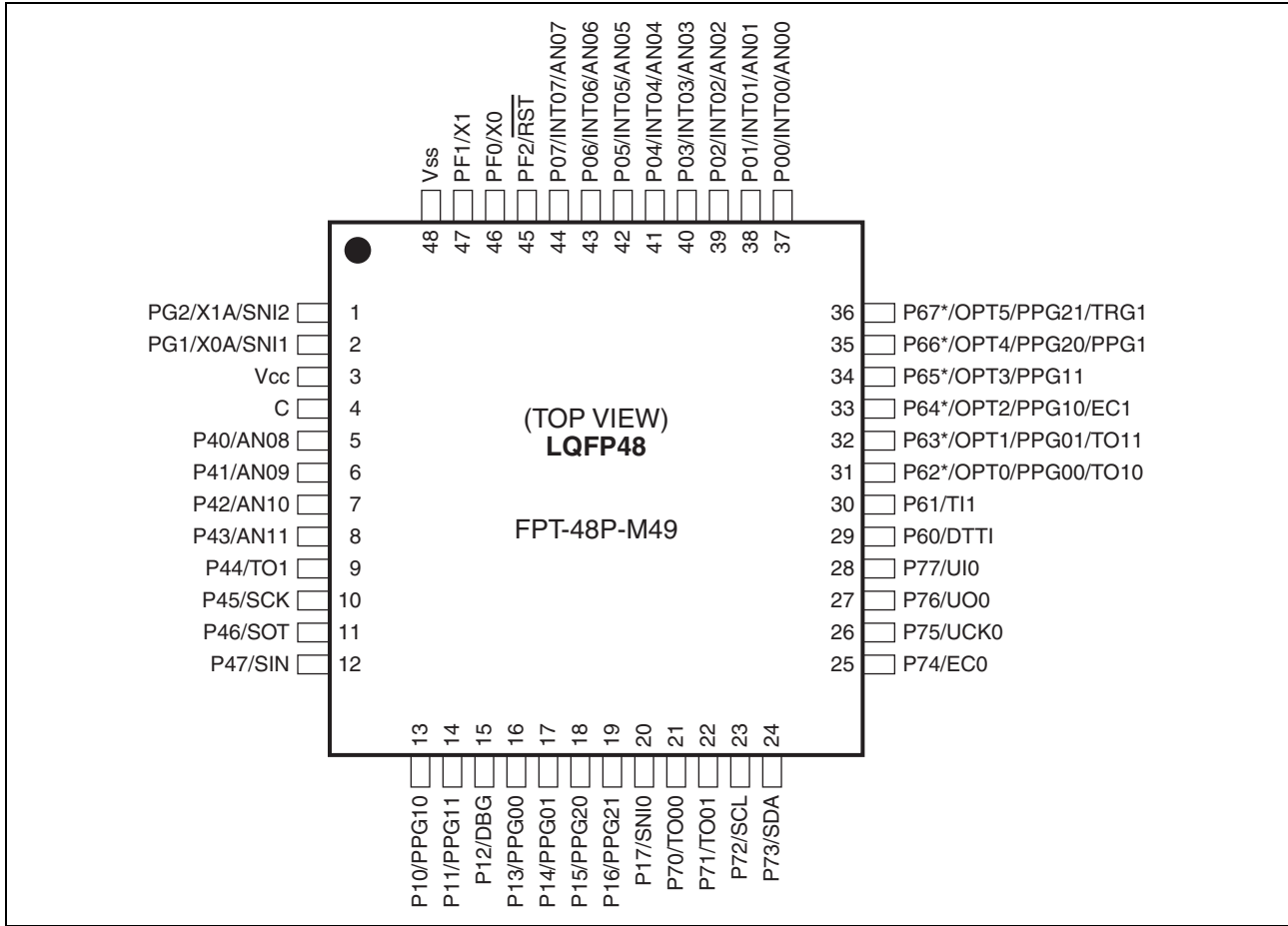
The operating voltage varies, depending on whether the on-chip debug function is used or not.

For details of the operating voltage, see “Electrical Characteristics”.

#### ■ On-chip debug function

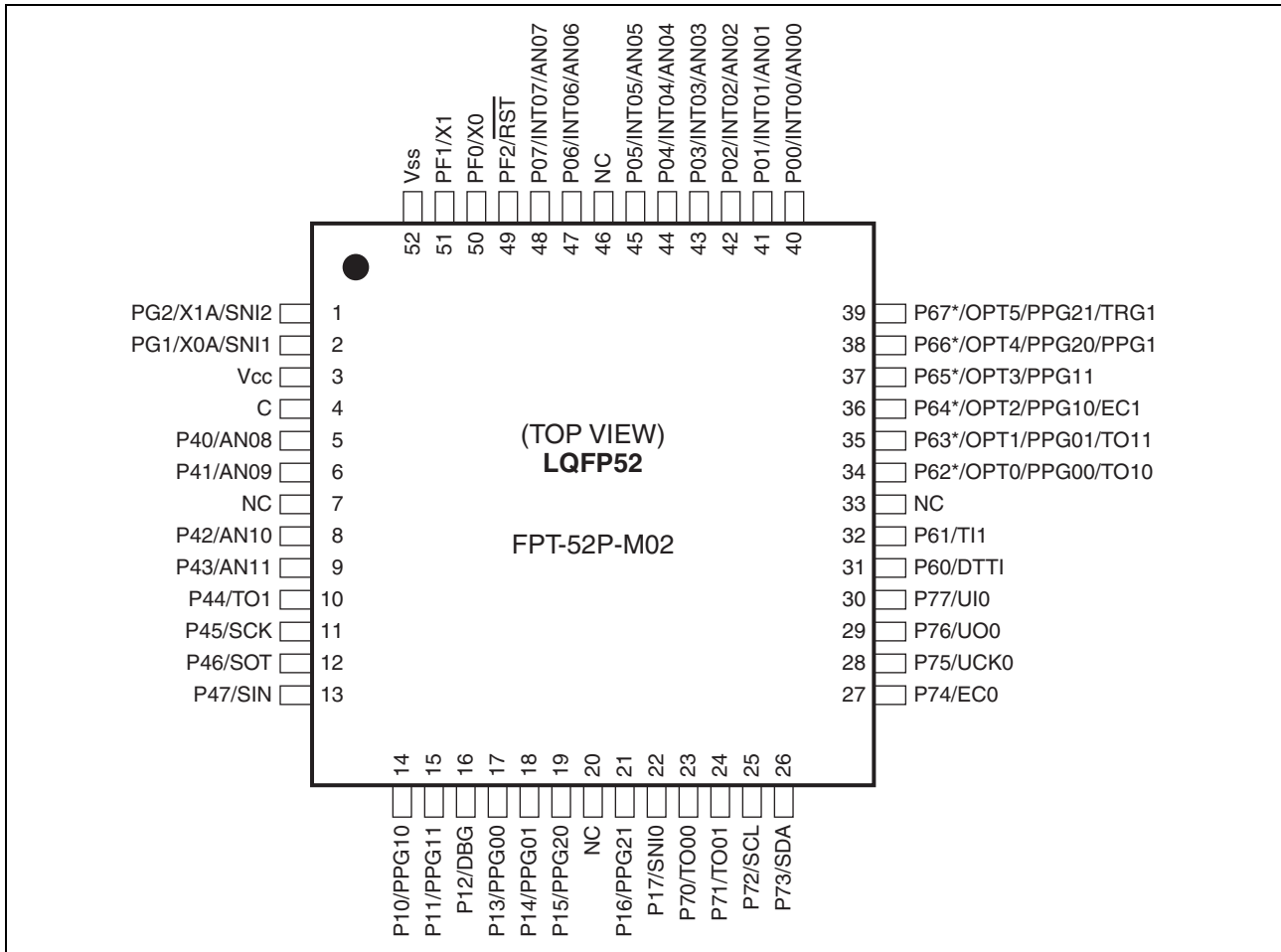
The on-chip debug function requires that  $V_{CC}$ ,  $V_{SS}$  and one serial wire be connected to an evaluation tool. For details of the connection method, refer to “CHAPTER 29 EXAMPLE OF SERIAL PROGRAMMING CONNECTION” in the hardware manual of the MB95390H Series.

**4. Pin Assignment**



\*: High-current pin (8 mA/12 mA)

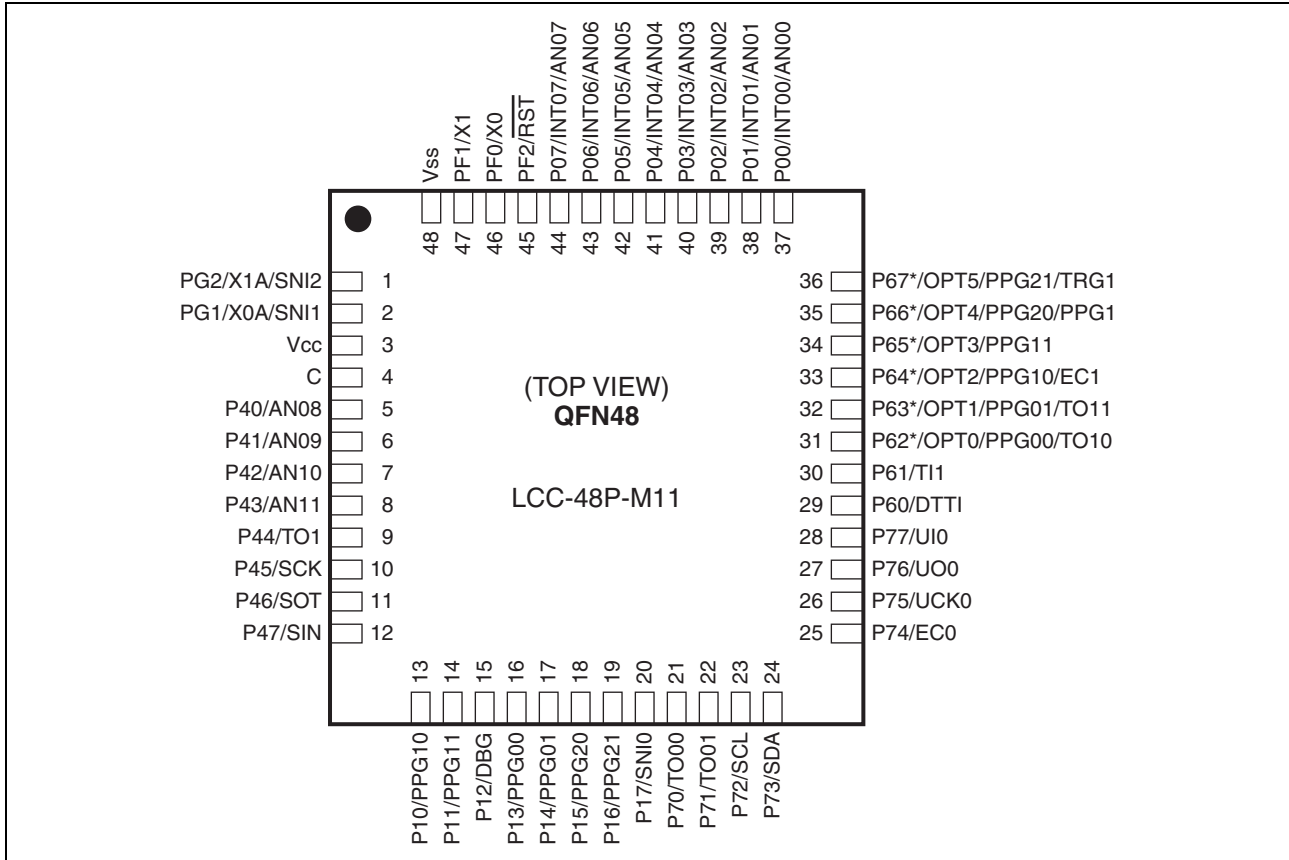
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\*: High-current pin (8 mA/12 mA)

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\*: High-current pin (8 mA/12 mA)

**5. Pin Functions**

Pin no.			Pin name	I/O circuit type*4	Function
LQFP48*1	QFN48*2	LQFP52*3			
1	1	1	PG2	C	General-purpose I/O port
			X1A		Subclock I/O oscillation pin
			SN12		Trigger input pin for the position detection function of the MPG waveform sequencer
2	2	2	PG1	C	General-purpose I/O port
			X0A		Subclock input oscillation pin
			SN11		Trigger input pin for the position detection function of the MPG waveform sequencer
3	3	3	V <sub>CC</sub>	—	Power supply pin
4	4	4	C	—	Capacitor connection pin
5	5	5	P40	K	General-purpose I/O port
			AN08		A/D converter analog input pin
6	6	6	P41	K	General-purpose I/O port
			AN09		A/D converter analog input pin
—	—	7	NC	—	It is an internally connected pin. Always leave it unconnected.
7	7	8	P42	K	General-purpose I/O port
			AN10		A/D converter analog input pin
8	8	9	P43	K	General-purpose I/O port
			AN11		A/D converter analog input pin
9	9	10	P44	G	General-purpose I/O port
			TO1		16-bit reload timer ch. 0 output pin
10	10	11	P45	G	General-purpose I/O port
			SCK		LIN-UART clock I/O pin
11	11	12	P46	G	General-purpose I/O port
			SOT		LIN-UART data output pin
12	12	13	P47	J	General-purpose I/O port
			SIN		LIN-UART data input pin
13	13	14	P10	G	General-purpose I/O port
			PPG10		8/16-bit PPG ch. 1 output pin
14	14	15	P11	G	General-purpose I/O port
			PPG11		8/16-bit PPG ch. 1 output pin
15	15	16	P12	H	General-purpose I/O port
			DBG		DBG input pin
16	16	17	P13	G	General-purpose I/O port
			PPG00		8/16-bit PPG ch. 0 output pin

*(Continued)*

Pin no.			Pin name	I/O circuit type*4	Function
LQFP48*1	QFN48*2	LQFP52*3			
17	17	18	P14	G	General-purpose I/O port
			PPG01		8/16-bit PPG ch. 0 output pin
18	18	19	P15	G	General-purpose I/O port
			PPG20		8/16-bit PPG ch. 2 output pin
—	—	20	NC	—	It is an internally connected pin. Always leave it unconnected.
19	19	21	P16	G	General-purpose I/O port
			PPG21		8/16-bit PPG ch. 2 output pin
20	20	22	P17	G	General-purpose I/O port
			SNi0		Trigger input pin for the position detection function of the MPG waveform sequencer
21	21	23	P70	G	General-purpose I/O port
			TO00		8/16-bit composite timer ch. 0 output pin
22	22	24	P71	G	General-purpose I/O port
			TO01		8/16-bit composite timer ch. 0 output pin
23	23	25	P72	I	General-purpose I/O port
			SCL		I <sup>2</sup> C clock I/O pin
24	24	26	P73	I	General-purpose I/O port
			SDA		I <sup>2</sup> C data I/O pin
25	25	27	P74	G	General-purpose I/O port
			EC0		8/16-bit composite timer ch. 0 clock input pin
26	26	28	P75	G	General-purpose I/O port
			UCK0		UART/SIO ch. 0 clock I/O pin
27	27	29	P76	G	General-purpose I/O port
			UO0		UART/SIO ch. 0 data output pin
28	28	30	P77	J	General-purpose I/O port
			UI0		UART/SIO ch. 0 data input pin
29	29	31	P60	G	General-purpose I/O port
			DTTI		MPG waveform sequencer input pin
30	30	32	P61	G	General-purpose I/O port
			TI1		16-bit reload timer ch. 0 input pin
—	—	33	NC	—	It is an internally connected pin. Always leave it unconnected.
31	31	34	P62	D	General-purpose I/O port High-current pin
			OPT0		MPG waveform sequencer output pin
			PPG00		8/16-bit PPG ch. 0 output pin
			TO10		8/16-bit composite timer ch. 1 output pin

*(Continued)*

Pin no.			Pin name	I/O circuit type*4	Function
LQFP48*1	QFN48*2	LQFP52*3			
32	32	35	P63	D	General-purpose I/O port High-current pin
			OPT1		MPG waveform sequencer output pin
			PPG01		8/16-bit PPG ch. 0 output pin
			TO11		8/16-bit composite timer ch. 1 output pin
33	33	36	P64	D	General-purpose I/O port High-current pin
			OPT2		MPG waveform sequencer output pin
			PPG10		8/16-bit PPG ch. 1 output pin
			EC1		8/16-bit composite timer ch. 1 clock input pin
34	34	37	P65	D	General-purpose I/O port High-current pin
			OPT3		MPG waveform sequencer output pin
			PPG11		8/16-bit PPG ch. 1 output pin
35	35	38	P66	D	General-purpose I/O port High-current pin
			OPT4		MPG waveform sequencer output pin
			PPG20		8/16-bit PPG ch. 2 output pin
			PPG1		16-bit PPG ch. 1 output pin
36	36	39	P67	D	General-purpose I/O port High-current pin
			OPT5		MPG waveform sequencer output pin
			PPG21		8/16-bit PPG ch. 2 output pin
			TRG1		16-bit PPG ch. 1 trigger input pin
37	37	40	P00	E	General-purpose I/O port
			INT00		External interrupt input pin
			AN00		A/D converter analog input pin
38	38	41	P01	E	General-purpose I/O port
			INT01		External interrupt input pin
			AN01		A/D converter analog input pin
39	39	42	P02	E	General-purpose I/O port
			INT02		External interrupt input pin
			AN02		A/D converter analog input pin
40	40	43	P03	E	General-purpose I/O port
			INT03		External interrupt input pin
			AN03		A/D converter analog input pin

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Pin no.			Pin name	I/O circuit type*4	Function
LQFP48*1	QFN48*2	LQFP52*3			
41	41	44	P04	E	General-purpose I/O port
			INT04		External interrupt input pin
			AN04		A/D converter analog input pin
42	42	45	P05	E	General-purpose I/O port
			INT05		External interrupt input pin
			AN05		A/D converter analog input pin
—	—	46	NC	—	It is an internally connected pin. Always leave it unconnected.
43	43	47	P06	E	General-purpose I/O port
			INT06		External interrupt input pin
			AN06		A/D converter analog input pin
44	44	48	P07	E	General-purpose I/O port
			INT07		External interrupt input pin
			AN07		A/D converter analog input pin
45	45	49	PF2	A	General-purpose I/O port
			$\overline{\text{RST}}$		Reset pin Dedicated reset pin in MB95F394H/F396H/F398H
46	46	50	PF0	B	General-purpose I/O port
			X0		Main clock I/O oscillation pin
47	47	51	PF1	B	General-purpose I/O port
			X1		Main clock I/O oscillation pin
48	48	52	V <sub>SS</sub>	—	Power supply pin (GND)

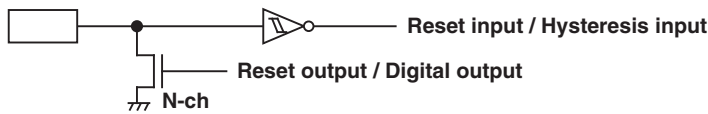
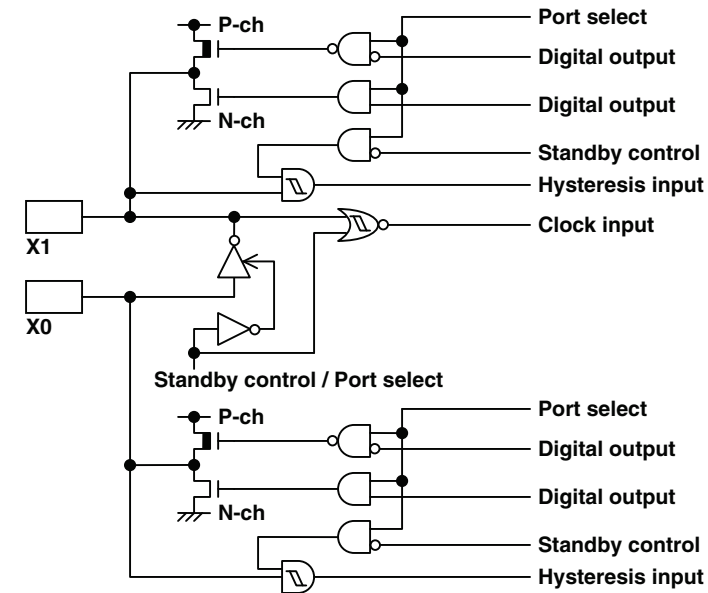
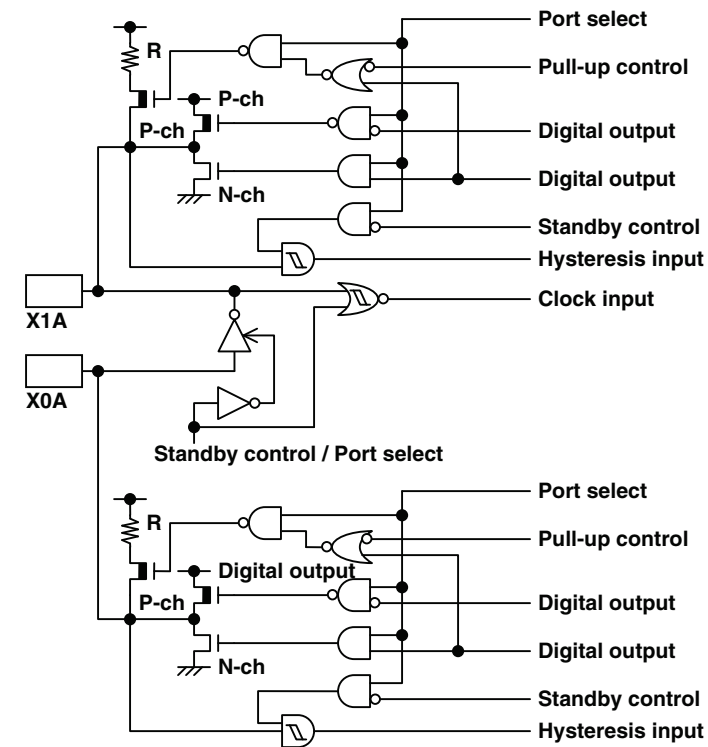
\*1: Package code: FPT-48P-M49

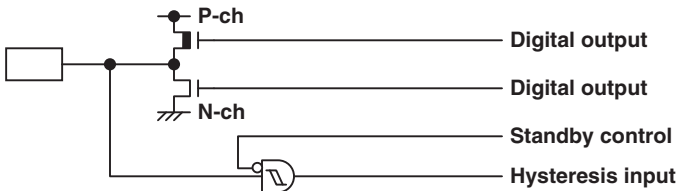
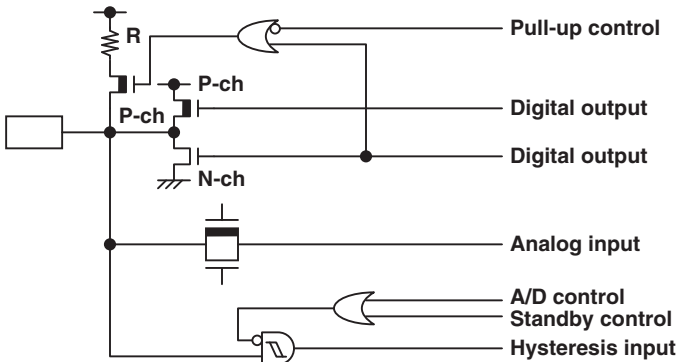
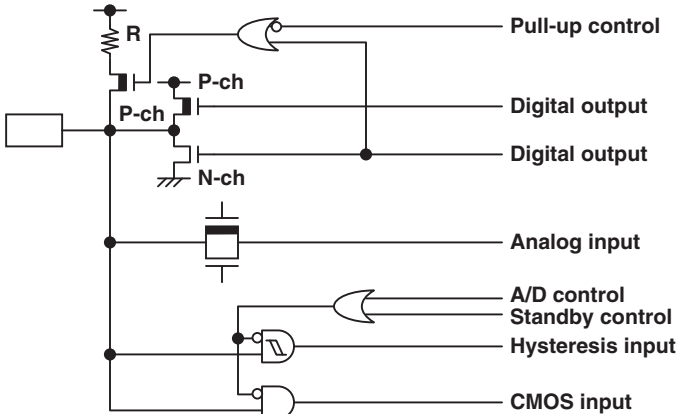
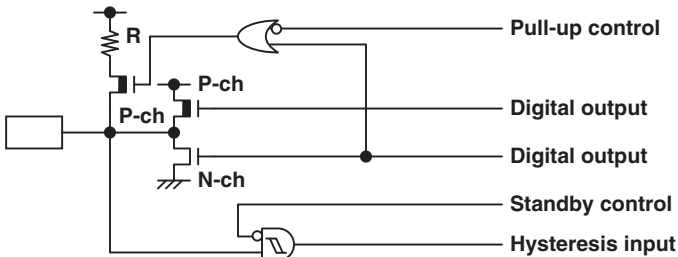
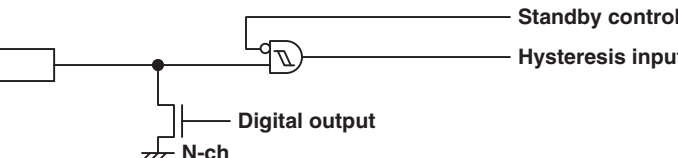
\*2: Package code: LCC-48P-M11

\*3: Package code: FPT-52P-M02

\*4: For the I/O circuit types, see "I/O Circuit Type".

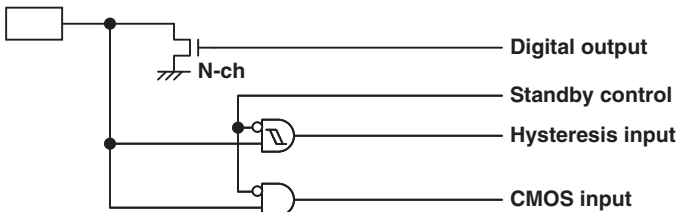
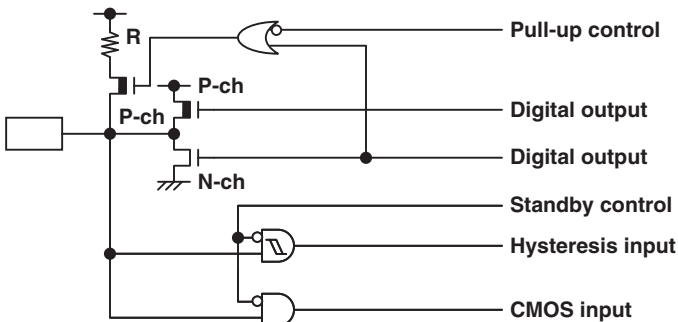
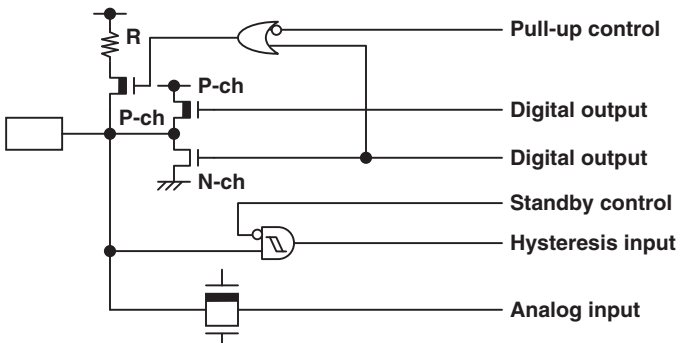
6. I/O Circuit Type

Type	Circuit	Remarks
A		<ul style="list-style-type: none"> <li>■ N-ch open drain output</li> <li>■ Hysteresis input</li> <li>■ Reset output</li> </ul>
B		<ul style="list-style-type: none"> <li>■ Oscillation circuit</li> <li>■ High-speed side</li> <li>■ Feedback resistance: approx. 1 MΩ</li> <li>■ CMOS output</li> <li>■ Hysteresis input</li> </ul>
C		<ul style="list-style-type: none"> <li>■ Oscillation circuit</li> <li>■ Low-speed side</li> <li>■ Feedback resistance: approx. 10 MΩ</li> <li>■ CMOS output</li> <li>■ Hysteresis input</li> <li>■ Pull-up control available</li> </ul>

Type	Circuit	Remarks
D		<ul style="list-style-type: none"> <li>■ CMOS output</li> <li>■ Hysteresis input</li> <li>■ High-current output</li> </ul>
E		<ul style="list-style-type: none"> <li>■ CMOS output</li> <li>■ Hysteresis input</li> <li>■ Pull-up control available</li> <li>■ Analog input</li> </ul>
F		<ul style="list-style-type: none"> <li>■ CMOS output</li> <li>■ Hysteresis input</li> <li>■ CMOS input</li> <li>■ Pull-up control available</li> <li>■ Analog input</li> </ul>
G		<ul style="list-style-type: none"> <li>■ CMOS output</li> <li>■ Hysteresis input</li> <li>■ Pull-up control available</li> </ul>
H		<ul style="list-style-type: none"> <li>■ N-ch open drain output</li> <li>■ Hysteresis input</li> </ul>

(Continued)

(Continued)

Type	Circuit	Remarks
I		<ul style="list-style-type: none"> <li>■ N-ch open drain output</li> <li>■ Hysteresis input</li> <li>■ CMOS input</li> </ul>
J		<ul style="list-style-type: none"> <li>■ CMOS output</li> <li>■ Hysteresis input</li> <li>■ CMOS input</li> <li>■ Pull-up control available</li> </ul>
K		<ul style="list-style-type: none"> <li>■ Hysteresis input</li> <li>■ CMOS output</li> <li>■ Pull-up control available</li> <li>■ Analog input</li> </ul>

## 7. Notes On Device Handling

### ■ Preventing latch-ups

When using the device, ensure that the voltage applied does not exceed the maximum voltage rating.

In a CMOS IC, if a voltage higher than  $V_{CC}$  or a voltage lower than  $V_{SS}$  is applied to an input/output pin that is neither a medium-withstand voltage pin nor a high-withstand voltage pin, or if a voltage out of the rating range of power supply voltage mentioned in "14.1 Absolute Maximum Ratings" of "Electrical Characteristics" is applied to the  $V_{CC}$  pin or the  $V_{SS}$  pin, a latch-up may occur.

When a latch-up occurs, power supply current increases significantly, which may cause a component to be thermally destroyed.

### ■ Stabilizing supply voltage

Supply voltage must be stabilized.

A malfunction may occur when power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the  $V_{CC}$  power supply voltage.

As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in  $V_{CC}$  ripple (p-p value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard  $V_{CC}$  value, and the transient fluctuation rate does not exceed 0.1 V/ms at a momentary fluctuation such as switching the power supply.

### ■ Notes on using the external clock

When an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from subclock mode or stop mode.

## 8. Pin Connection

### ■ Treatment of unused pins

If an unused input pin is left unconnected, a component may be permanently damaged due to malfunctions or latch-ups. Always pull up or pull down an unused input pin through a resistor of at least 2 k $\Omega$ . Set an unused input/output pin to the output state and leave it unconnected, or set it to the input state and treat it the same as an unused input pin. If there is an unused output pin, leave it unconnected.

## 9. Power supply pins

To reduce unnecessary electro-magnetic emission, prevent malfunctions of strobe signals due to an increase in the ground level, and conform to the total output current standard, always connect the  $V_{CC}$  pin and the  $V_{SS}$  pin to the power supply and ground outside the device. In addition, connect the current supply source to the  $V_{CC}$  pin and the  $V_{SS}$  pin with low impedance.

It is also advisable to connect a ceramic capacitor of approximately 0.1  $\mu$ F as a bypass capacitor between the  $V_{CC}$  pin and the  $V_{SS}$  pin at a location close to this device.

### ■ DBG pin

Connect the DBG pin directly to an external pull-up resistor.

To prevent the device from unintentionally entering the debug mode due to noise, minimize the distance between the DBG pin and the  $V_{CC}$  or  $V_{SS}$  pin when designing the layout of the printed circuit board.

The DBG pin should not stay at "L" level after power-on until the reset output is released.

### ■ $\overline{RST}$ pin

Connect the  $\overline{RST}$  pin directly to an external pull-up resistor.

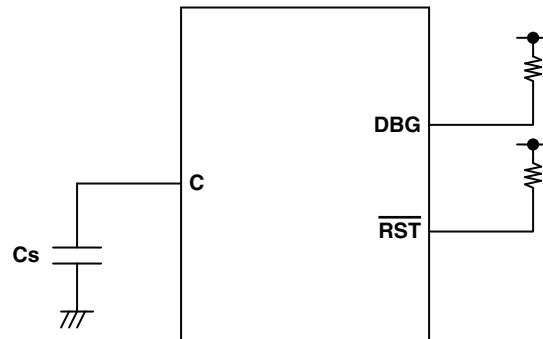
To prevent the device from unintentionally entering the reset mode due to noise, minimize the distance between the  $\overline{RST}$  pin and the  $V_{CC}$  or  $V_{SS}$  pin when designing the layout of the printed circuit board.

The  $\overline{RST}$ /PF2 pin functions as the reset input/output pin after power-on. In addition, the reset output of the  $\overline{RST}$ /PF2 pin can be enabled by the RSTOE bit in the SYSC register, and the reset input function and the general purpose I/O function can be selected by the RSTEN bit in the SYSC register.

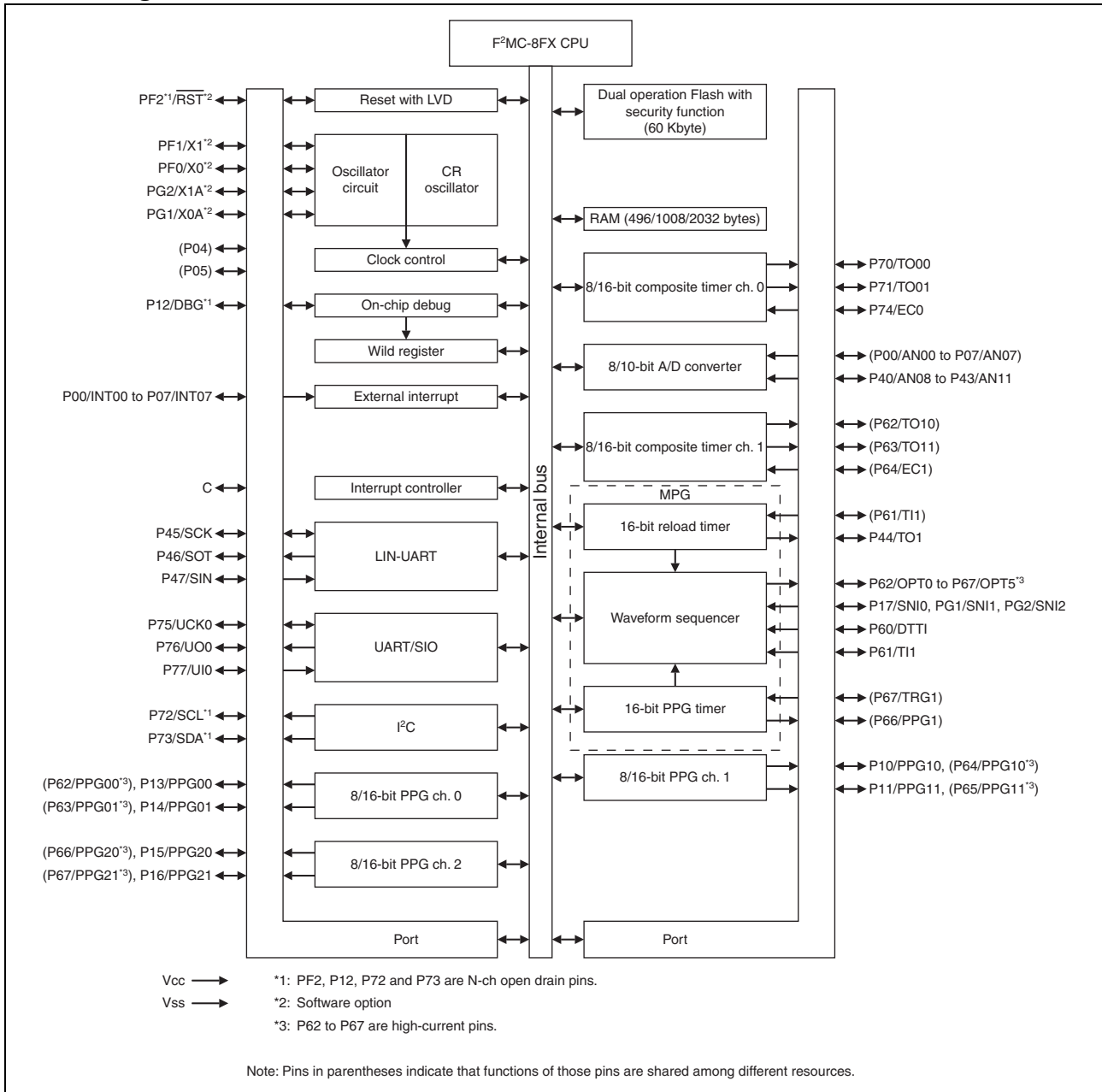
■ C pin

Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The bypass capacitor for the  $V_{CC}$  pin must have a capacitance larger than  $C_S$ . For the connection to a smoothing capacitor  $C_S$ , see the diagram below. To prevent the device from unintentionally entering a mode to which the device is not set to transit due to noise, minimize the distance between the C pin and  $C_S$  and the distance between  $C_S$  and the  $V_{SS}$  pin when designing the layout of a printed circuit board.

• DBG/ $\overline{RST}$ /C pins connection diagram



**10. Block Diagram**

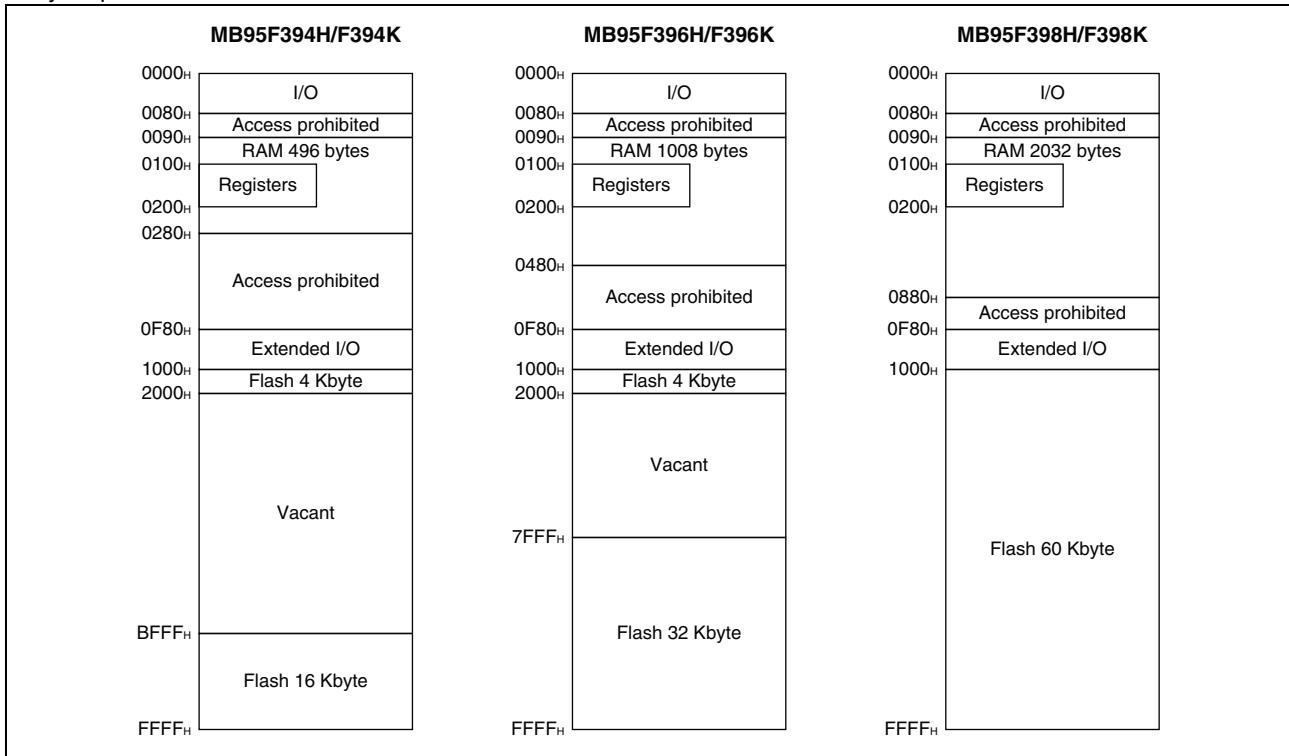


## 11. CPU Core

### ■ Memory Space

The memory space of the MB95390H Series is 64 Kbyte in size, and consists of an I/O area, a data area, and a program area. The memory space includes areas intended for specific purposes such as general-purpose registers and a vector table. The memory maps of the MB95390H Series are shown below.

### ■ Memory Maps



**12. I/O Map**

Address	Register abbreviation	Register name	R/W	Initial value
0000 <sub>H</sub>	PDR0	Port 0 data register	R/W	00000000 <sub>B</sub>
0001 <sub>H</sub>	DDR0	Port 0 direction register	R/W	00000000 <sub>B</sub>
0002 <sub>H</sub>	PDR1	Port 1 data register	R/W	00000000 <sub>B</sub>
0003 <sub>H</sub>	DDR1	Port 1 direction register	R/W	00000000 <sub>B</sub>
0004 <sub>H</sub>	—	(Disabled)	—	—
0005 <sub>H</sub>	WATR	Oscillation stabilization wait time setting register	R/W	11111111 <sub>B</sub>
0006 <sub>H</sub>	—	(Disabled)	—	—
0007 <sub>H</sub>	SYCC	System clock control register	R/W	0000X011 <sub>B</sub>
0008 <sub>H</sub>	STBC	Standby control register	R/W	0000XXX <sub>B</sub>
0009 <sub>H</sub>	RSRR	Reset source register	R/W	XXXXXXXX <sub>B</sub>
000A <sub>H</sub>	TBTC	Time-base timer control register	R/W	00000000 <sub>B</sub>
000B <sub>H</sub>	WPCR	Watch prescaler control register	R/W	00000000 <sub>B</sub>
000C <sub>H</sub>	WDTC	Watchdog timer control register	R/W	00XX0000 <sub>B</sub>
000D <sub>H</sub>	SYCC2	System clock control register 2	R/W	XX100011 <sub>B</sub>
000E <sub>H</sub> to 0011 <sub>H</sub>	—	(Disabled)	—	—
0012 <sub>H</sub>	PDR4	Port 4 data register	R/W	00000000 <sub>B</sub>
0013 <sub>H</sub>	PDR4	Port 4 direction register	R/W	00000000 <sub>B</sub>
0014 <sub>H</sub> , 0015 <sub>H</sub>	—	(Disabled)	—	—
0016 <sub>H</sub>	PDR6	Port 6 data register	R/W	00000000 <sub>B</sub>
0017 <sub>H</sub>	DDR6	Port 6 direction register	R/W	00000000 <sub>B</sub>
0018 <sub>H</sub>	DDR7	Port 7 data register	R/W	00000000 <sub>B</sub>
0019 <sub>H</sub>	DDR7	Port 7 direction register	R/W	00000000 <sub>B</sub>
001A <sub>H</sub> to 0027 <sub>H</sub>	—	(Disabled)	—	—
0028 <sub>H</sub>	PDRF	Port F data register	R/W	00000000 <sub>B</sub>
0029 <sub>H</sub>	DDRF	Port F direction register	R/W	00000000 <sub>B</sub>
002A <sub>H</sub>	PDRG	Port G data register	R/W	00000000 <sub>B</sub>
002B <sub>H</sub>	DDRG	Port G direction register	R/W	00000000 <sub>B</sub>
002C <sub>H</sub>	PUL0	Port 0 pull-up register	R/W	00000000 <sub>B</sub>
002D <sub>H</sub>	PUL1	Port 1 pull-up register	R/W	00000000 <sub>B</sub>
002E <sub>H</sub> , 002F <sub>H</sub>	—	(Disabled)	—	—
0030 <sub>H</sub>	PUL4	Port 4 pull-up register	R/W	00000000 <sub>B</sub>
0031 <sub>H</sub>	PUL6	Port 6 pull-up register	R/W	00000000 <sub>B</sub>
0032 <sub>H</sub>	PUL7	Port 7 pull-up register	R/W	00000000 <sub>B</sub>
0033 <sub>H</sub> , 0034 <sub>H</sub>	—	(Disabled)	—	—
0035 <sub>H</sub>	PULG	Port G pull-up register	R/W	00000000 <sub>B</sub>

*(Continued)*

Address	Register abbreviation	Register name	R/W	Initial value
0036 <sub>H</sub>	T01CR1	8/16-bit composite timer 01 status control register 1	R/W	00000000 <sub>B</sub>
0037 <sub>H</sub>	T00CR1	8/16-bit composite timer 00 status control register 1	R/W	00000000 <sub>B</sub>
0038 <sub>H</sub>	T11CR1	8/16-bit composite timer 11 status control register 1	R/W	00000000 <sub>B</sub>
0039 <sub>H</sub>	T10CR1	8/16-bit composite timer 10 status control register 1	R/W	00000000 <sub>B</sub>
003A <sub>H</sub>	PC01	8/16-bit PPG timer 01 control register	R/W	00000000 <sub>B</sub>
003B <sub>H</sub>	PC00	8/16-bit PPG timer 00 control register	R/W	00000000 <sub>B</sub>
003C <sub>H</sub>	PC11	8/16-bit PPG timer 11 control register	R/W	00000000 <sub>B</sub>
003D <sub>H</sub>	PC10	8/16-bit PPG timer 10 control register	R/W	00000000 <sub>B</sub>
003E <sub>H</sub>	PC21	8/16-bit PPG timer 21 control register	R/W	00000000 <sub>B</sub>
003F <sub>H</sub>	PC20	8/16-bit PPG timer 20 control register	R/W	00000000 <sub>B</sub>
0040 <sub>H</sub>	TMCSRH1	16-bit reload timer control status register upper	R/W	00000000 <sub>B</sub>
0041 <sub>H</sub>	TMCSRL1	16-bit reload timer control status register lower	R/W	00000000 <sub>B</sub>
0042 <sub>H</sub> , 0043 <sub>H</sub>	—	(Disabled)	—	—
0044 <sub>H</sub>	PCNTH1	16-bit PPG status control register upper	R/W	00000000 <sub>B</sub>
0045 <sub>H</sub>	PCNTL1	16-bit PPG status control register lower	R/W	00000000 <sub>B</sub>
0046 <sub>H</sub> , 0047 <sub>H</sub>	—	(Disabled)	—	—
0048 <sub>H</sub>	EIC00	External interrupt circuit control register ch. 0/ch. 1	R/W	00000000 <sub>B</sub>
0049 <sub>H</sub>	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	00000000 <sub>B</sub>
004A <sub>H</sub>	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	00000000 <sub>B</sub>
004B <sub>H</sub>	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	00000000 <sub>B</sub>
004C <sub>H</sub> to 004F <sub>H</sub>	—	(Disabled)	—	—
0050 <sub>H</sub>	SCR	LIN-UART serial control register	R/W	00000000 <sub>B</sub>
0051 <sub>H</sub>	SMR	LIN-UART serial mode register	R/W	00000000 <sub>B</sub>
0052 <sub>H</sub>	SSR	LIN-UART serial status register	R/W	00001000 <sub>B</sub>
0053 <sub>H</sub>	RDR/TDR	LIN-UART receive/transmit data register	R/W	00000000 <sub>B</sub>
0054 <sub>H</sub>	ESCR	LIN-UART extended status control register	R/W	00000100 <sub>B</sub>
0055 <sub>H</sub>	ECCR	LIN-UART extended communication control register	R/W	000000XX <sub>B</sub>
0056 <sub>H</sub>	SMC10	UART/SIO serial mode control register 1	R/W	00000000 <sub>B</sub>
0057 <sub>H</sub>	SMC20	UART/SIO serial mode control register 2	R/W	00100000 <sub>B</sub>
0058 <sub>H</sub>	SSR0	UART/SIO serial status and data register	R/W	00000001 <sub>B</sub>
0059 <sub>H</sub>	TDR0	UART/SIO serial output data register	R/W	00000000 <sub>B</sub>
005A <sub>H</sub>	RDR0	UART/SIO serial input data register	R	00000000 <sub>B</sub>
005B <sub>H</sub> to 005F <sub>H</sub>	—	(Disabled)	—	—

*(Continued)*

Address	Register abbreviation	Register name	R/W	Initial value
0060 <sub>H</sub>	IBCR00	I <sup>2</sup> C bus control register 0	R/W	00000000 <sub>B</sub>
0061 <sub>H</sub>	IBCR10	I <sup>2</sup> C bus control register 1	R/W	00000000 <sub>B</sub>
0062 <sub>H</sub>	IBCR0	I <sup>2</sup> C bus status register	R/W	00000000 <sub>B</sub>
0063 <sub>H</sub>	IDDR0	I <sup>2</sup> C data register	R/W	00000000 <sub>B</sub>
0064 <sub>H</sub>	IAAR0	I <sup>2</sup> C address register	R/W	00000000 <sub>B</sub>
0065 <sub>H</sub>	ICCR0	I <sup>2</sup> C clock control register	R/W	00000000 <sub>B</sub>
0066 <sub>H</sub>	OPCUR	Output control register (upper)	R/W	00000000 <sub>B</sub>
0067 <sub>H</sub>	OPCLR	Output control register (lower)	R/W	00000000 <sub>B</sub>
0068 <sub>H</sub>	IPCUR	Input control register (upper)	R/W	00000000 <sub>B</sub>
0069 <sub>H</sub>	IPCLR	Input control register (lower)	R/W	00000000 <sub>B</sub>
006A <sub>H</sub>	NCCR	Noise cancellation control register	R/W	00000000 <sub>B</sub>
006B <sub>H</sub>	TCSR	Timer control status register	R/W	00000000 <sub>B</sub>
006C <sub>H</sub>	ADC1	8/10-bit A/D converter control register 1	R/W	00000000 <sub>B</sub>
006D <sub>H</sub>	ADC2	8/10-bit A/D converter control register 2	R/W	00000000 <sub>B</sub>
006E <sub>H</sub>	ADDH	8/10-bit A/D converter data register (upper)	R/W	00000000 <sub>B</sub>
006F <sub>H</sub>	ADDL	8/10-bit A/D converter data register (lower)	R/W	00000000 <sub>B</sub>
0070 <sub>H</sub>	—	(Disabled)	—	—
0071 <sub>H</sub>	FSR2	Flash memory status register 2	R/W	00000000 <sub>B</sub>
0072 <sub>H</sub>	FSR	Flash memory status register	R/W	00X0000 <sub>B</sub>
0073 <sub>H</sub>	SWRE0	Flash memory sector write control register 0	R/W	00000000 <sub>B</sub>
0074 <sub>H</sub>	FSR3	Flash memory status register 3	R	00000000 <sub>B</sub>
0075 <sub>H</sub>	—	(Disabled)	—	—
0076 <sub>H</sub>	WREN	Wild register address compare enable register	R/W	00000000 <sub>B</sub>
0077 <sub>H</sub>	WROR	Wild register data test setting register	R/W	00000000 <sub>B</sub>
0078 <sub>H</sub>	—	Mirror of register bank pointer (RP) and mirror of direct bank pointer (DP)	—	—
0079 <sub>H</sub>	ILR0	Interrupt level setting register 0	R/W	11111111 <sub>B</sub>
007A <sub>H</sub>	ILR1	Interrupt level setting register 1	R/W	11111111 <sub>B</sub>
007B <sub>H</sub>	ILR2	Interrupt level setting register 2	R/W	11111111 <sub>B</sub>
007C <sub>H</sub>	ILR3	Interrupt level setting register 3	R/W	11111111 <sub>B</sub>
007D <sub>H</sub>	ILR4	Interrupt level setting register 4	R/W	11111111 <sub>B</sub>
007E <sub>H</sub>	ILR5	Interrupt level setting register 5	R/W	11111111 <sub>B</sub>
007F <sub>H</sub>	—	(Disabled)	—	—
0F80 <sub>H</sub>	WRARH0	Wild register address setting register (upper) ch. 0	R/W	00000000 <sub>B</sub>
0F81 <sub>H</sub>	WRARL0	Wild register address setting register (lower) ch. 0	R/W	00000000 <sub>B</sub>
0F82 <sub>H</sub>	WRDR0	Wild register data setting register ch. 0	R/W	00000000 <sub>B</sub>

*(Continued)*

Address	Register abbreviation	Register name	R/W	Initial value
0F83 <sub>H</sub>	WRARH1	Wild register address setting register (upper) ch. 1	R/W	00000000 <sub>B</sub>
0F84 <sub>H</sub>	WRARL1	Wild register address setting register (lower) ch. 1	R/W	00000000 <sub>B</sub>
0F85 <sub>H</sub>	WRDR1	Wild register data setting register ch. 1	R/W	00000000 <sub>B</sub>
0F86 <sub>H</sub>	WRARH2	Wild register address setting register (upper) ch. 2	R/W	00000000 <sub>B</sub>
0F87 <sub>H</sub>	WRARL2	Wild register address setting register (lower) ch. 2	R/W	00000000 <sub>B</sub>
0F88 <sub>H</sub>	WRDR2	Wild register data setting register ch. 2	R/W	00000000 <sub>B</sub>
0F89 <sub>H</sub> to 0F91 <sub>H</sub>	—	(Disabled)	—	—
0F92 <sub>H</sub>	T01CR0	8/16-bit composite timer 01 status control register 0	R/W	00000000 <sub>B</sub>
0F93 <sub>H</sub>	T00CR0	8/16-bit composite timer 00 status control register 0	R/W	00000000 <sub>B</sub>
0F94 <sub>H</sub>	T01DR	8/16-bit composite timer 01 data register	R/W	00000000 <sub>B</sub>
0F95 <sub>H</sub>	T00DR	8/16-bit composite timer 00 data register	R/W	00000000 <sub>B</sub>
0F96 <sub>H</sub>	TMCR0	8/16-bit composite timer 00/01 timer mode control register	R/W	00000000 <sub>B</sub>
0F97 <sub>H</sub>	T11CR0	8/16-bit composite timer 11 status control register 0	R/W	00000000 <sub>B</sub>
0F98 <sub>H</sub>	T10CR0	8/16-bit composite timer 10 status control register 0	R/W	00000000 <sub>B</sub>
0F99 <sub>H</sub>	T11DR	8/16-bit composite timer 11 data register	R/W	00000000 <sub>B</sub>
0F9A <sub>H</sub>	T10DR	8/16-bit composite timer 10 data register	R/W	00000000 <sub>B</sub>
0F9B <sub>H</sub>	TMCR1	8/16-bit composite timer 10/11 timer mode control register	R/W	00000000 <sub>B</sub>
0F9C <sub>H</sub>	PPS01	8/16-bit PPG01 cycle setting buffer register	R/W	11111111 <sub>B</sub>
0F9D <sub>H</sub>	PPS00	8/16-bit PPG00 cycle setting buffer register	R/W	11111111 <sub>B</sub>
0F9E <sub>H</sub>	PDS01	8/16-bit PPG01 duty setting buffer register	R/W	11111111 <sub>B</sub>
0F9F <sub>H</sub>	PDS00	8/16-bit PPG00 duty setting buffer register	R/W	11111111 <sub>B</sub>
0FA0 <sub>H</sub>	PPS11	8/16-bit PPG11 cycle setting buffer register	R/W	11111111 <sub>B</sub>
0FA1 <sub>H</sub>	PPS10	8/16-bit PPG10 cycle setting buffer register	R/W	11111111 <sub>B</sub>
0FA2 <sub>H</sub>	PDS11	8/16-bit PPG11 duty setting buffer register	R/W	11111111 <sub>B</sub>
0FA3 <sub>H</sub>	PDS10	8/16-bit PPG10 duty setting buffer register	R/W	11111111 <sub>B</sub>
0FA4 <sub>H</sub>	PPGS	8/16-bit PPG startup register	R/W	00000000 <sub>B</sub>
0FA5 <sub>H</sub>	REVC	8/16-bit PPG output reverse register	R/W	00000000 <sub>B</sub>
0FA6 <sub>H</sub>	PPS21	8/16-bit PPG21 cycle setting buffer register	R/W	11111111 <sub>B</sub>
0FA7 <sub>H</sub>	PPS20	8/16-bit PPG20 cycle setting buffer register	R/W	11111111 <sub>B</sub>
0FA8 <sub>H</sub>	TMRH1	16-bit reload timer timer register (upper)	R/W	00000000 <sub>B</sub>
	TMRLRH1	16-bit reload timer reload register (upper)		
0FA9 <sub>H</sub>	TMRL1	16-bit reload timer timer register (lower)	R/W	00000000 <sub>B</sub>
	TMRLRL1	16-bit reload timer reload register (lower)		
0FAA <sub>H</sub>	PDS21	8/16-bit PPG21 duty setting buffer register	R/W	11111111 <sub>B</sub>
0FAB <sub>H</sub>	PDS20	8/16-bit PPG20 duty setting buffer register	R/W	11111111 <sub>B</sub>

*(Continued)*

Address	Register abbreviation	Register name	R/W	Initial value
0FAC <sub>H</sub> to 0FAF <sub>H</sub>	—	(Disabled)	—	—
0FB0 <sub>H</sub>	PDCRH1	16-bit PPG down counter register (upper)	R	00000000 <sub>B</sub>
0FB1 <sub>H</sub>	PDCRL1	16-bit PPG down counter register (lower)	R	00000000 <sub>B</sub>
0FB2 <sub>H</sub>	PCSRH1	16-bit PPG cycle setting buffer register (upper)	R/W	11111111 <sub>B</sub>
0FB3 <sub>H</sub>	PC SRL1	16-bit PPG cycle setting buffer register (lower)	R/W	11111111 <sub>B</sub>
0FB4 <sub>H</sub>	PDUTH1	16-bit PPG duty setting buffer register (upper)	R/W	11111111 <sub>B</sub>
0FB5 <sub>H</sub>	PDUTL1	16-bit PPG duty setting buffer register (lower)	R/W	11111111 <sub>B</sub>
0FB6 <sub>H</sub> to 0FBB <sub>H</sub>	—	(Disabled)	—	—
0FBC <sub>H</sub>	BGR1	LIN-UART baud rate generator register 1	R/W	00000000 <sub>B</sub>
0FBD <sub>H</sub>	BGR0	LIN-UART baud rate generator register 0	R/W	00000000 <sub>B</sub>
0FBE <sub>H</sub>	PSSR0	UART/SIO prescaler select register	R/W	00000000 <sub>B</sub>
0FBF <sub>H</sub>	BRSR0	UART/SIO baud rate setting register	R/W	00000000 <sub>B</sub>
0FC0 <sub>H</sub> , 0FC1 <sub>H</sub>	—	(Disabled)	—	—
0FC2 <sub>H</sub>	AIDRH	A/D input disable register (upper)	R/W	00000000 <sub>B</sub>
0FC3 <sub>H</sub>	AIDRL	A/D input disable register (lower)	R/W	00000000 <sub>B</sub>
0FC4 <sub>H</sub>	OPDBRH0	Output data buffer register (upper) ch. 0	R/W	00000000 <sub>B</sub>
0FC5 <sub>H</sub>	OPDBRL0	Output data buffer register (lower) ch. 0	R/W	00000000 <sub>B</sub>
0FC6 <sub>H</sub>	OPDBRH1	Output data buffer register (upper) ch. 1	R/W	00000000 <sub>B</sub>
0FC7 <sub>H</sub>	OPDBRL1	Output data buffer register (lower) ch. 1	R/W	00000000 <sub>B</sub>
0FC8 <sub>H</sub>	OPDBRH2	Output data buffer register (upper) ch. 2	R/W	00000000 <sub>B</sub>
0FC9 <sub>H</sub>	OPDBRL2	Output data buffer register (lower) ch. 2	R/W	00000000 <sub>B</sub>
0FCA <sub>H</sub>	OPDBRH3	Output data buffer register (upper) ch. 3	R/W	00000000 <sub>B</sub>
0FCB <sub>H</sub>	OPDBRL3	Output data buffer register (lower) ch. 3	R/W	00000000 <sub>B</sub>
0FCC <sub>H</sub>	OPDBRH4	Output data buffer register (upper) ch. 4	R/W	00000000 <sub>B</sub>
0FCD <sub>H</sub>	OPDBRL4	Output data buffer register (lower) ch. 4	R/W	00000000 <sub>B</sub>
0FCE <sub>H</sub>	OPDBRH5	Output data buffer register (upper) ch. 5	R/W	00000000 <sub>B</sub>
0FCF <sub>H</sub>	OPDBRL5	Output data buffer register (lower) ch. 5	R/W	00000000 <sub>B</sub>
0FD0 <sub>H</sub>	OPDBRH6	Output data buffer register (upper) ch. 6	R/W	00000000 <sub>B</sub>
0FD1 <sub>H</sub>	OPDBRL6	Output data buffer register (lower) ch. 6	R/W	00000000 <sub>B</sub>
0FD2 <sub>H</sub>	OPDBRH7	Output data buffer register (upper) ch. 7	R/W	00000000 <sub>B</sub>
0FD3 <sub>H</sub>	OPDBRL7	Output data buffer register (lower) ch. 7	R/W	00000000 <sub>B</sub>
0FD4 <sub>H</sub>	OPDBRH8	Output data buffer register (upper) ch. 8	R/W	00000000 <sub>B</sub>
0FD5 <sub>H</sub>	OPDBRL8	Output data buffer register (lower) ch. 8	R/W	00000000 <sub>B</sub>
0FD6 <sub>H</sub>	OPDBRH9	Output data buffer register (upper) ch. 9	R/W	00000000 <sub>B</sub>
0FD7 <sub>H</sub>	OPDBRL9	Output data buffer register (lower) ch. 9	R/W	00000000 <sub>B</sub>
0FD8 <sub>H</sub>	OPDBRHA	Output data buffer register (upper) ch. A	R/W	00000000 <sub>B</sub>
0FD9 <sub>H</sub>	OPDBRLA	Output data buffer register (lower) ch. A	R/W	00000000 <sub>B</sub>

*(Continued)*

*(Continued)*

Address	Register abbreviation	Register name	R/W	Initial value
0FDA <sub>H</sub>	OPDBRHB	Output data buffer register (upper) ch. B	R/W	00000000 <sub>B</sub>
0FDB <sub>H</sub>	OPDBRLB	Output data buffer register (lower) ch. B	R/W	00000000 <sub>B</sub>
0FDC <sub>H</sub>	OPDUR	Output data register (upper)	R	0000XXXX <sub>B</sub>
0FDD <sub>H</sub>	OPDLR	Output data register (lower)	R	XXXXXXXX <sub>B</sub>
0FDE <sub>H</sub>	CPCUR	Compare clear register (upper)	R/W	XXXXXXXX <sub>B</sub>
0FDF <sub>H</sub>	CPCLR	Compare clear register (lower)	R/W	XXXXXXXX <sub>B</sub>
0FE0 <sub>H</sub> , 0FE1 <sub>H</sub>	—	(Disabled)	—	—
0FE2 <sub>H</sub>	TMBUR	Timer buffer register (upper)	R	XXXXXXXX <sub>B</sub>
0FE3 <sub>H</sub>	TMBLR	Timer buffer register (lower)	R	XXXXXXXX <sub>B</sub>
0FE4 <sub>H</sub>	CRTH	Main CR clock trimming register (upper)	R/W	0XXXXXXXX <sub>B</sub>
0FE5 <sub>H</sub>	CRTL	Main CR clock trimming register (lower)	R/W	00XXXXXXXX <sub>B</sub>
0FE6 <sub>H</sub> , 0FE7 <sub>H</sub>	—	(Disabled)	—	—
0FE8 <sub>H</sub>	SYSC	System configuration register	R/W	11000011 <sub>B</sub>
0FE9 <sub>H</sub>	CMCR	Clock monitoring control register	R/W	00000000 <sub>B</sub>
0FEA <sub>H</sub>	CMDR	Clock monitoring data register	R	00000000 <sub>B</sub>
0FEB <sub>H</sub>	WDTH	Watchdog timer selection ID register (upper)	R	XXXXXXXX <sub>B</sub>
0FEC <sub>H</sub>	WDTL	Watchdog timer selection ID register (lower)	R	XXXXXXXX <sub>B</sub>
0FED <sub>H</sub>	—	(Disabled)	—	—
0FEE <sub>H</sub>	ILSR	Input level select register	R/W	00000000 <sub>B</sub>
0FEF <sub>H</sub>	WICR	Interrupt pin control register	R/W	01000000 <sub>B</sub>
0FF0 <sub>H</sub> to 0FFF <sub>H</sub>	—	(Disabled)	—	—

**■ R/W access symbols**


- R/W : Readable / Writable
- R : Read only
- W : Write only

**■ Initial value symbols**

- 0 : The initial value of this bit is "0".
- 1 : The initial value of this bit is "1".
- X : The initial value of this bit is indeterminate.

**Note:** Do not write to an address that is "(Disabled)". If a "(Disabled)" address is read, an indeterminate value is returned.

**13. Interrupt Source Table**

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower		
External interrupt ch. 0, ch. 4	IRQ00	FFFA <sub>H</sub>	FFFB <sub>H</sub>	L00 [1:0]	<div style="text-align: center;">High</div>  <div style="text-align: center;">Low</div>
External interrupt ch. 1, ch. 5	IRQ01	FFF8 <sub>H</sub>	FFF9 <sub>H</sub>	L01 [1:0]	
External interrupt ch. 2, ch. 6	IRQ02	FFF6 <sub>H</sub>	FFF7 <sub>H</sub>	L02 [1:0]	
External interrupt ch. 3, ch. 7	IRQ03	FFF4 <sub>H</sub>	FFF5 <sub>H</sub>	L03 [1:0]	
UART/SIO ch. 0, MPG (DTTI)	IRQ04	FFF2 <sub>H</sub>	FFF3 <sub>H</sub>	L04 [1:0]	
8/16-bit composite timer ch. 0 (lower)	IRQ05	FFF0 <sub>H</sub>	FFF1 <sub>H</sub>	L05 [1:0]	
8/16-bit composite timer ch. 0 (upper)	IRQ06	FFEE <sub>H</sub>	FFEF <sub>H</sub>	L06 [1:0]	
LIN-UART (reception)	IRQ07	FFEC <sub>H</sub>	FFED <sub>H</sub>	L07 [1:0]	
LIN-UART (transmission)	IRQ08	FFEA <sub>H</sub>	FFEB <sub>H</sub>	L08 [1:0]	
8/16-bit PPG ch. 1 (lower)	IRQ09	FFE8 <sub>H</sub>	FFE9 <sub>H</sub>	L09 [1:0]	
8/16-bit PPG ch. 1 (upper)	IRQ10	FFE6 <sub>H</sub>	FFE7 <sub>H</sub>	L10 [1:0]	
8/16-bit PPG ch. 2 (upper)	IRQ11	FFE4 <sub>H</sub>	FFE5 <sub>H</sub>	L11 [1:0]	
8/16-bit PPG ch. 0 (upper)	IRQ12	FFE2 <sub>H</sub>	FFE3 <sub>H</sub>	L12 [1:0]	
8/16-bit PPG ch. 0 (lower)	IRQ13	FFE0 <sub>H</sub>	FFE1 <sub>H</sub>	L13 [1:0]	
8/16-bit composite timer ch. 1 (upper)	IRQ14	FFDE <sub>H</sub>	FFDF <sub>H</sub>	L14 [1:0]	
8/16-bit PPG ch. 2 (lower)	IRQ15	FFDC <sub>H</sub>	FFDD <sub>H</sub>	L15 [1:0]	
16-bit reload timer ch. 1, MPG (write timing/compare clear), I <sup>2</sup> C	IRQ16	FFDA <sub>H</sub>	FFDB <sub>H</sub>	L16 [1:0]	
16-bit PPG timer ch. 1, MPG (position detection/compare match)	IRQ17	FFD8 <sub>H</sub>	FFD9 <sub>H</sub>	L17 [1:0]	
8/10-bit A/D converter	IRQ18	FFD6 <sub>H</sub>	FFD7 <sub>H</sub>	L18 [1:0]	
Time-base timer	IRQ19	FFD4 <sub>H</sub>	FFD5 <sub>H</sub>	L19 [1:0]	
Watch prescaler	IRQ20	FFD2 <sub>H</sub>	FFD3 <sub>H</sub>	L20 [1:0]	
—	IRQ21	FFD0 <sub>H</sub>	FFD1 <sub>H</sub>	L21 [1:0]	
8/16-bit composite timer ch. 1 (lower)	IRQ22	FFCE <sub>H</sub>	FFCF <sub>H</sub>	L22 [1:0]	
Flash memory	IRQ23	FFCC <sub>H</sub>	FFCD <sub>H</sub>	L23 [1:0]	

## 14. Electrical Characteristics

### 14.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage* <sup>1</sup>	$V_{CC}$	$V_{SS} - 0.3$	$V_{SS} + 6$	V	
Input voltage* <sup>1</sup>	$V_I$	$V_{SS} - 0.3$	$V_{SS} + 6$	V	*2
Output voltage* <sup>1</sup>	$V_O$	$V_{SS} - 0.3$	$V_{SS} + 6$	V	*2
Maximum clamp current	$I_{CLAMP}$	-2	+2	mA	Applicable to specific pins* <sup>3</sup>
Total maximum clamp current	$\sum  I_{CLAMP} $	—	20	mA	Applicable to specific pins* <sup>3</sup>
"L" level maximum output current	$I_{OL1}$	—	15	mA	Other than P62 to P67
	$I_{OL2}$	—	15		P62 to P67
"L" level average current	$I_{OLAV1}$	—	4	mA	Other than P62 to P67 Average output current = operating current × operating ratio (1 pin)
	$I_{OLAV2}$	—	12		P62 to P67 Average output current = operating current × operating ratio (1 pin)
"L" level total maximum output current	$\sum I_{OL}$	—	100	mA	
"L" level total average output current	$\sum I_{OLAV}$	—	50	mA	Total average output current = operating current × operating ratio (Total number of pins)
"H" level maximum output current	$I_{OH1}$	—	-15	mA	Other than P12, P62 to P67, P72, P73 and PF2
	$I_{OH2}$	—	-15		P12, P62 to P67, P72, P73 and PF2
"H" level average current	$I_{OHAV1}$	—	-4	mA	Other than P12, P62 to P67, P72, P73 and PF2 Average output current = operating current × operating ratio (1 pin)
	$I_{OHAV2}$	—	-8		P12, P62 to P67, P72, P73 and PF2 Average output current = operating current × operating ratio (1 pin)
"H" level total maximum output current	$\sum I_{OH}$	—	-100	mA	
"H" level total average output current	$\sum I_{OHAV}$	—	-50	mA	Total average output current = operating current × operating ratio (Total number of pins)
Power consumption	$P_d$	—	320	mW	
Operating temperature	$T_A$	-40	+85	°C	
Storage temperature	$T_{stg}$	-55	+150	°C	

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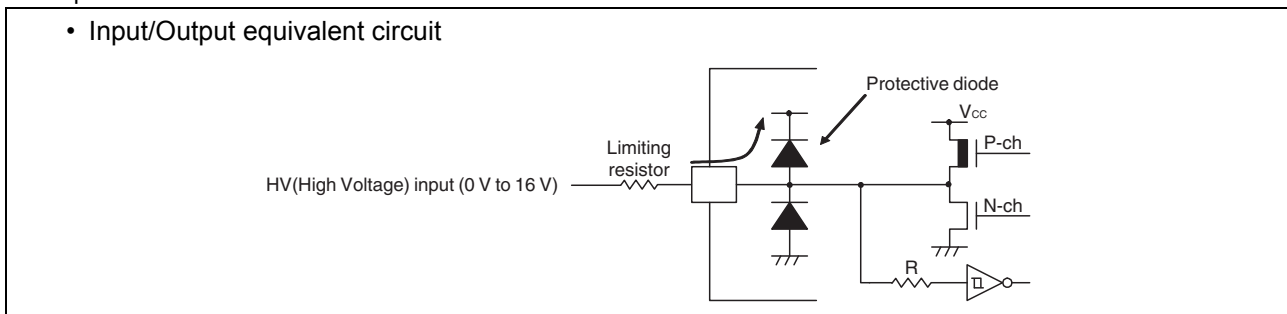
(Continued)

\*1: The parameter is based on  $V_{SS} = 0.0\text{ V}$ .

\*2:  $V_I$  and  $V_O$  must not exceed  $V_{CC} + 0.3\text{ V}$ .  $V_I$  must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the  $I_{CLAMP}$  rating is used instead of the  $V_I$  rating.

\*3: Applicable to the following pins: P00 to P07, P10, P11, P13 to P17, P40 to P47, P60 to P67, P70, P71, P74 to P77, PF0, PF1, PG1 and PG2

- Use under recommended operating conditions.
- Use with DC voltage (current).
- The HV (High Voltage) signal is an input signal exceeding the  $V_{CC}$  voltage. Always connect a limiting resistor between the HV (High Voltage) signal and the microcontroller before applying the HV (High Voltage) signal.
- The value of the limiting resistor should be set to a value at which the current to be input to the microcontroller pin when the HV (High Voltage) signal is input is below the standard value, irrespective of whether the current is transient current or stationary current.
- When the microcontroller drive current is low, such as in low power consumption modes, the HV (High Voltage) input potential may pass through the protective diode to increase the potential of the  $V_{CC}$  pin, affecting other devices.
- If the HV (High Voltage) signal is input when the microcontroller power supply is off (not fixed at 0 V), since power is supplied from the pins, incomplete operations may be executed.
- If the HV (High Voltage) input is input after power-on, since power is supplied from the pins, the voltage of power supply may not be sufficient to enable a power-on reset.
- Do not leave the HV (High Voltage) input pin unconnected.
- Example of a recommended circuit



**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

**14.2 Recommended Operating Conditions**

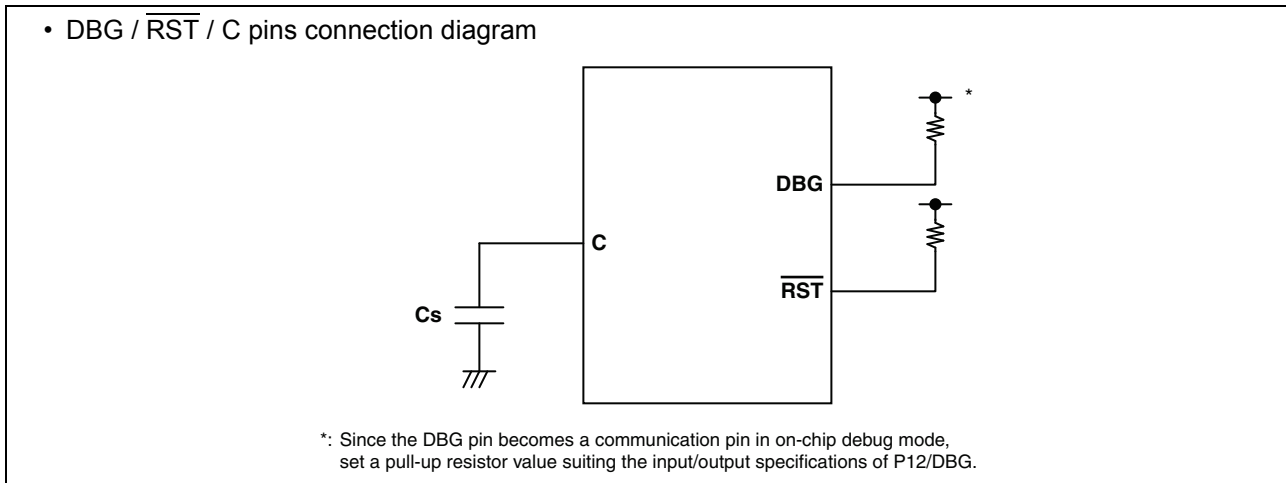
 (V<sub>SS</sub> = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks	
		Min	Max			
Power supply voltage	V <sub>CC</sub>	2.4*1*2	5.5*1	V	In normal operation	Other than on-chip debug mode
		2.3	5.5		Hold condition in stop mode	
		2.9	5.5		In normal operation	On-chip debug mode
		2.3	5.5		Hold condition in stop mode	
Smoothing capacitor	C <sub>S</sub>	0.022	1	μF	*3	
Operating temperature	T <sub>A</sub>	-40	+85	°C	Other than on-chip debug mode	
		+5	+35		On-chip debug mode	

\*1: The value varies depending on the operating frequency, the machine clock and the analog guaranteed range.

\*2: This value becomes 2.88 V when the low-voltage detection reset is used.

\*3: Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The bypass capacitor for the V<sub>CC</sub> pin must have a capacitance larger than C<sub>S</sub>. For the connection to a smoothing capacitor C<sub>S</sub>, see the diagram below. To prevent the device from unintentionally entering an unknown mode due to noise, minimize the distance between the C pin and C<sub>S</sub> and the distance between C<sub>S</sub> and the V<sub>SS</sub> pin when designing the layout of a printed circuit board.



**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

**14.3 DC Characteristics**
 $(V_{CC} = 5.0 V \pm 10\%, V_{SS} = 0.0 V, T_A = -40^\circ C \text{ to } +85^\circ C)$ 

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ <sup>*3</sup>	Max		
"H" level input voltage	$V_{IHI}$	P47, P72, P73, P77	*1	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	When CMOS input level (hysteresis input) is selected
	$V_{IHS}$	P00 to P07, P10 to P17, P40 to P47, P60 to P67, P70 to P77, PF0, PF1, PG1, PG2	*1	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Hysteresis input
	$V_{IHM}$	PF2	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	Hysteresis input
"L" level input voltage	$V_{IL}$	P47, P72, P73, P77	*1	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	When CMOS input level (hysteresis input) is selected
	$V_{ILS}$	P00 to P07, P10 to P17, P40 to P47, P60 to P67, P70 to P77, PF0, PF1, PG1, PG2	*1	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	Hysteresis input
	$V_{ILM}$	PF2	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	Hysteresis input
Open-drain output application voltage	$V_D$	P12, P72, P73, PF2	—	$V_{SS} - 0.3$	—	$V_{SS} + 5.5$	V	
"H" level output voltage	$V_{OH1}$	Output pins other than P12, P62 to P67, P72, P73, PF2	$I_{OH} = -4 \text{ mA}$	$V_{CC} - 0.5$	—	—	V	
	$V_{OH2}$	P62 to P67	$I_{OH} = -8 \text{ mA}$	$V_{CC} - 0.5$	—	—	V	
"L" level output voltage	$V_{OL1}$	Output pins other than P62 to P67	$I_{OL} = 4 \text{ mA}$	—	—	0.4	V	
	$V_{OL2}$	P62 to P67	$I_{OL} = 12 \text{ mA}$	—	—	0.4	V	
Input leak current (Hi-Z output leak current)	$I_{LI}$	All input pins	$0.0 V < V_I < V_{CC}$	-5	—	+5	$\mu A$	When pull-up resistance is disabled
Pull-up resistance	$R_{PULL}$	P00 to P07, P10, P11, P13 to P17, P40 to P47, P60, P61, P70, P71, P74 to P76, PG1, PG2	$V_I = 0 V$	25	50	100	$k\Omega$	When pull-up resistance is enabled

*(Continued)*

(V<sub>CC</sub> = 5.0 V±10%, V<sub>SS</sub> = 0.0 V, T<sub>A</sub> = -40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ <sup>*3</sup>	Max		
Input capacitance	C <sub>IN</sub>	Other than V <sub>CC</sub> and V <sub>SS</sub>	f = 1 MHz	—	5	15	pF	
Power supply current <sup>*2</sup>	I <sub>CC</sub>	V <sub>CC</sub> (External clock operation)	V <sub>CC</sub> = 5.5 V F <sub>CH</sub> = 32 MHz F <sub>MP</sub> = 16 MHz Main clock mode (divided by 2)	—	14.8	17	mA	Except during Flash memory writing and erasing
				—	33.5	39.5	mA	During Flash memory writing and erasing
				—	16.6	21	mA	At A/D conversion
	I <sub>CCS</sub>		V <sub>CC</sub> = 5.5 V F <sub>CH</sub> = 32 MHz F <sub>MP</sub> = 16 MHz Main sleep mode (divided by 2)	—	7	9	mA	
	I <sub>CCL</sub>		V <sub>CC</sub> = 5.5 V F <sub>CL</sub> = 32 kHz F <sub>MPL</sub> = 16 kHz Subclock mode (divided by 2) T <sub>A</sub> = +25°C	—	60	153	μA	
	I <sub>CCLS</sub>		V <sub>CC</sub> = 5.5 V F <sub>CL</sub> = 32 kHz F <sub>MPL</sub> = 16 kHz Subsleep mode (divided by 2) T <sub>A</sub> = +25°C	—	9.4	84	μA	
	I <sub>CCT</sub>		V <sub>CC</sub> = 5.5 V F <sub>CL</sub> = 32 kHz Watch mode Main stop mode T <sub>A</sub> = +25°C	—	4.3	30	μA	
	I <sub>CCMCR</sub>		V <sub>CC</sub>	V <sub>CC</sub> = 5.5 V F <sub>CRH</sub> = 12.5 MHz F <sub>MP</sub> = 12.5 MHz Main CR clock mode	—	11.8	13.2	mA
I <sub>CCSCR</sub>	V <sub>CC</sub>	V <sub>CC</sub> = 5.5 V Sub-CR clock mode (divided by 2) T <sub>A</sub> = +25°C	—	113	410	μA		

(Continued)

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 ( $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ <sup>*3</sup>	Max		
Power supply current <sup>*2</sup>	$I_{CCTS}$	$V_{CC}$ (External clock operation)	$V_{CC} = 5.5\text{ V}$ $F_{CH} = 32\text{ MHz}$ Time-base timer mode $T_A = +25^\circ\text{C}$	—	0.9	3	mA	
	$I_{CCH}$		$V_{CC} = 5.5\text{ V}$ Substop mode $T_A = +25^\circ\text{C}$	—	3.4	22.5	$\mu\text{A}$	
	$I_{LVD}$	$V_{CC}$	Current consumption for low-voltage detection circuit only	—	31	54	$\mu\text{A}$	
	$I_{CRH}$		Current consumption for the main CR oscillator	—	0.5	0.6	mA	
	$I_{CRL}$		Current consumption for the sub-CR oscillator oscillating at 100 kHz	—	20	72	$\mu\text{A}$	

\*1: The input levels of P47, P72, P73 and P77 can be switched between “CMOS input level” and “hysteresis input level”. The input level selection register (ILSR) is used to switch between the two input levels.

\*2: • The power supply current is determined by the external clock. When the low-voltage detection option is selected, the power-supply current will be the sum of adding the current consumption of the low-voltage detection circuit ( $I_{LVD}$ ) to one of the value from  $I_{CC}$  to  $I_{CCH}$ . In addition, when both the low-voltage detection option and the CR oscillator are selected, the power supply current will be the sum of adding up the current consumption of the low-voltage detection circuit, the current consumption of the CR oscillators ( $I_{CRH}$ ,  $I_{CRL}$ ) and a specified value. In on-chip debug mode, the CR oscillator ( $I_{CRH}$ ) and the low-voltage detection circuit are always enabled, and current consumption therefore increases accordingly.

• See "AC Characteristics: Clock Timing" for  $F_{CH}$  and  $F_{CL}$ .

• See "AC Characteristics: Source Clock/Machine Clock" for  $F_{MP}$  and  $F_{MPL}$ .

\*3:  $V_{CC} = 5.0\text{ V}$ ,  $T_A = 25^\circ\text{C}$

**14.4 AC Characteristics**
**14.4.1 Clock Timing**
 $(V_{CC} = 2.4\text{ V to } 5.5\text{ V}, V_{SS} = 0.0\text{ V}, T_A = -40^\circ\text{C to } +85^\circ\text{C})$ 

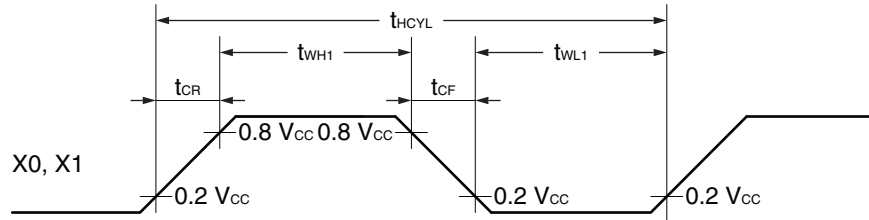
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks	
				Min	Typ	Max			
Clock frequency	F <sub>CH</sub>	X0, X1	—	1	—	16.25	MHz	When the main oscillation circuit is used	
		X0	X1: open	1	—	12	MHz	When the main external clock is used	
		X0, X1	*1	1	—	32.5	MHz	When the main external clock is used	
	F <sub>CRH</sub>	—	—	—	12.25	12.5	12.75	MHz	When the main CR clock is used*2
					9.80	10	10.20	MHz	
					7.84	8	8.16	MHz	
					0.98	1	1.02	MHz	
					12.18	12.5	12.82	MHz	When the main CR clock is used*3
					9.75	10	10.25	MHz	
					7.80	8	8.20	MHz	
					0.97	1	1.03	MHz	
	F <sub>CL</sub>	X0A, X1A	—	—	—	32.768	—	kHz	When the sub-oscillation circuit is used
—					32.768	—	kHz	When the sub-external clock is used	
F <sub>CRL</sub>	—	—	—	50	100	200	kHz	When the sub-CR clock is used	
Clock cycle time	t <sub>H CYL</sub>	X0, X1	—	61.5	—	1000	ns	When the main oscillation circuit is used	
		X0	X1: open	83.4	—	1000	ns	When the external clock is used	
		X0, X1	*1	30.8	—	1000	ns		
	t <sub>L CYL</sub>	X0A, X1A	—	—	30.5	—	μs	When the subclock is used	
Input clock pulse width	t <sub>WH1</sub>	X0	X1: open	33.4	—	—	ns	When the external clock is used, the duty ratio should range between 40% and 60%.	
	t <sub>WL1</sub>	X0, X1	*1	12.4	—	—	ns		
	t <sub>WH2</sub> t <sub>WL2</sub>	X0A	—	—	15.2	—	μs		
Input clock rise time and fall time	t <sub>CR</sub>	X0	X1: open	—	—	5	ns	When the external clock is used	
	t <sub>CF</sub>	X0, X1	*1	—	—	5	ns		
CR oscillation start time	t <sub>CRHWK</sub>	—	—	—	—	80	μs	When the main CR clock is used	
	t <sub>CRLWK</sub>	—	—	—	—	10	μs	When the sub-CR clock is used	

\*1: The external clock signal is input to X0 and the inverted external clock signal to X1.

\*2: These specifications are only applicable to a product in LQFP package (FPT-48P-M49 or FPT-52P-M02).

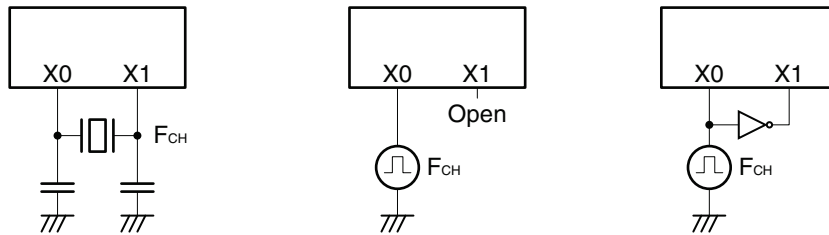
\*3: These specifications are only applicable to a product in QFN package (LCC-48P-M11).

- Input waveform generated when an external clock (main clock) is used

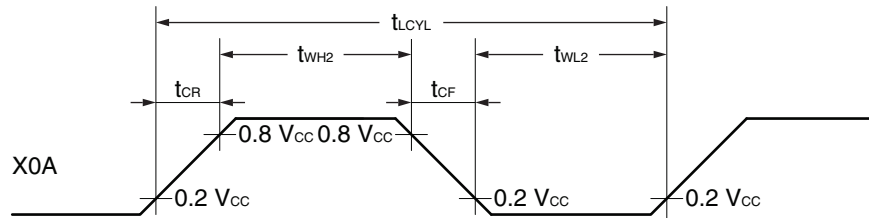


- Figure of main clock input port external connection

When a crystal oscillator or a ceramic oscillator is used      When the external clock is used (X1 is open)      When the external clock is used



- Input waveform generated when an external clock (subclock) is used



- Figure of subclock input port external connection

When a crystal oscillator or a ceramic oscillator is used      When the external clock is used



**14.4.2 Source Clock/Machine Clock**
 $(V_{CC} = 5.0 V \pm 10\%, V_{SS} = 0.0 V, T_A = -40^\circ C \text{ to } +85^\circ C)$ 

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Source clock cycle time*1	$t_{SCLK}$	—	61.5	—	2000	ns	When the main external clock is used Min: $F_{CH} = 32.5$ MHz, divided by 2 Max: $F_{CH} = 1$ MHz, divided by 2
			80	—	1000	ns	When the main CR clock is used Min: $F_{CRH} = 12.5$ MHz Max: $F_{CRH} = 1$ MHz
			—	61	—	$\mu s$	When the sub-oscillation clock is used $F_{CL} = 32.768$ kHz, divided by 2
			—	20	—	$\mu s$	When the sub-CR clock is used $F_{CRL} = 100$ kHz, divided by 2
Source clock frequency	$F_{SP}$	—	0.5	—	16.25	MHz	When the main oscillation clock is used
			1	—	12.5	MHz	When the main CR clock is used
	—		16.384	—	kHz	When the sub-oscillation clock is used	
	$F_{SPL}$		—	50	—	kHz	When the sub-CR clock is used $F_{CRL} = 100$ kHz, divided by 2
Machine clock cycle time*2 (minimum instruction execution time)	$t_{MCLK}$	—	61.5	—	32000	ns	When the main oscillation clock is used Min: $F_{SP} = 16.25$ MHz, no division Max: $F_{SP} = 0.5$ MHz, divided by 16
			80	—	16000	ns	When the main CR clock is used Min: $F_{SP} = 12.5$ MHz Max: $F_{SP} = 1$ MHz, divided by 16
			61	—	976.5	$\mu s$	When the sub-oscillation clock is used Min: $F_{SPL} = 16.384$ kHz, no division Max: $F_{SPL} = 16.384$ kHz, divided by 16
			20	—	320	$\mu s$	When the sub-CR clock is used Min: $F_{SPL} = 50$ kHz, no division Max: $F_{SPL} = 50$ kHz, divided by 16
Machine clock frequency	$F_{MP}$	—	0.031	—	16.25	MHz	When the main oscillation clock is used
			0.0625	—	12.5	MHz	When the main CR clock is used
	$F_{MPL}$		1.024	—	16.384	kHz	When the sub-oscillation clock is used
			3.125	—	50	kHz	When the sub-CR clock is used $F_{CRL} = 100$ kHz

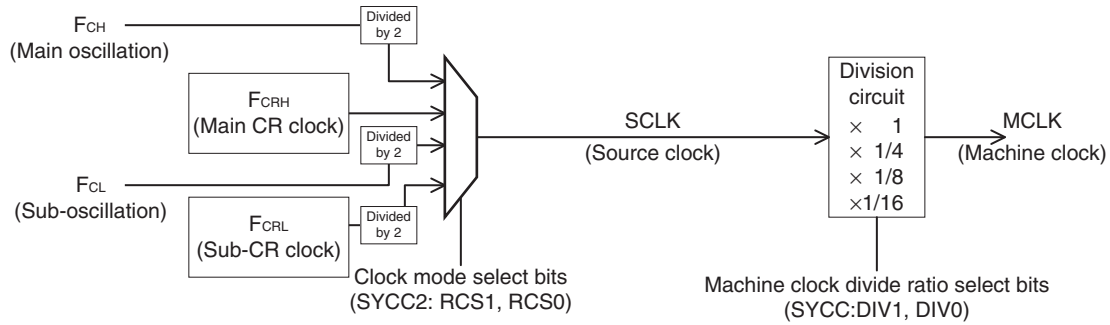
\*1: This is the clock before it is divided according to the division ratio set by the machine clock divide ratio select bits (SYCC:DIV1, DIV0). This source clock is divided to become a machine clock according to the divide ratio set by the machine clock divide ratio select bits (SYCC:DIV1, DIV0). In addition, a source clock can be selected from the following.

- Main clock divided by 2
- Main CR clock
- Subclock divided by 2
- Sub-CR clock divided by 2

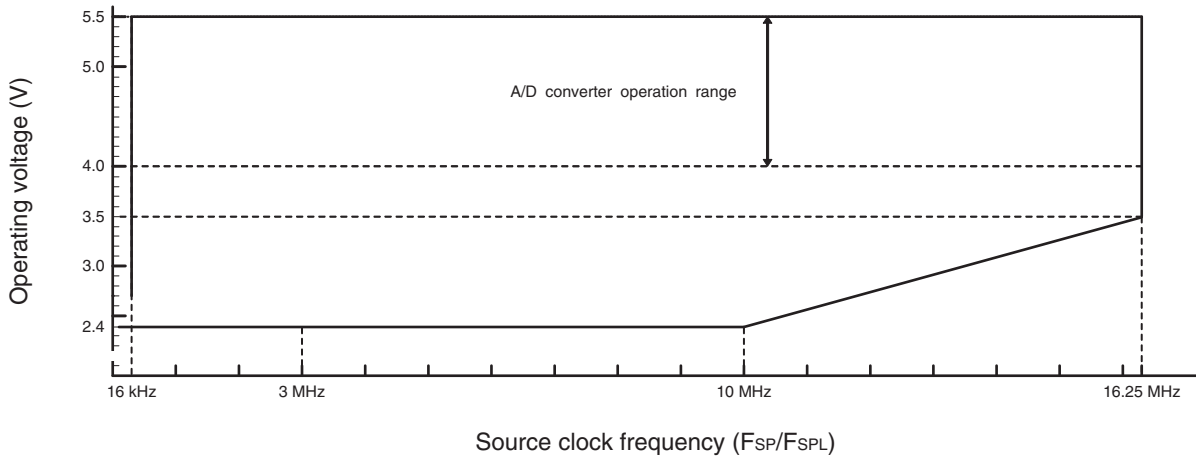
\*2: This is the operating clock of the microcontroller. A machine clock can be selected from the following.

- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

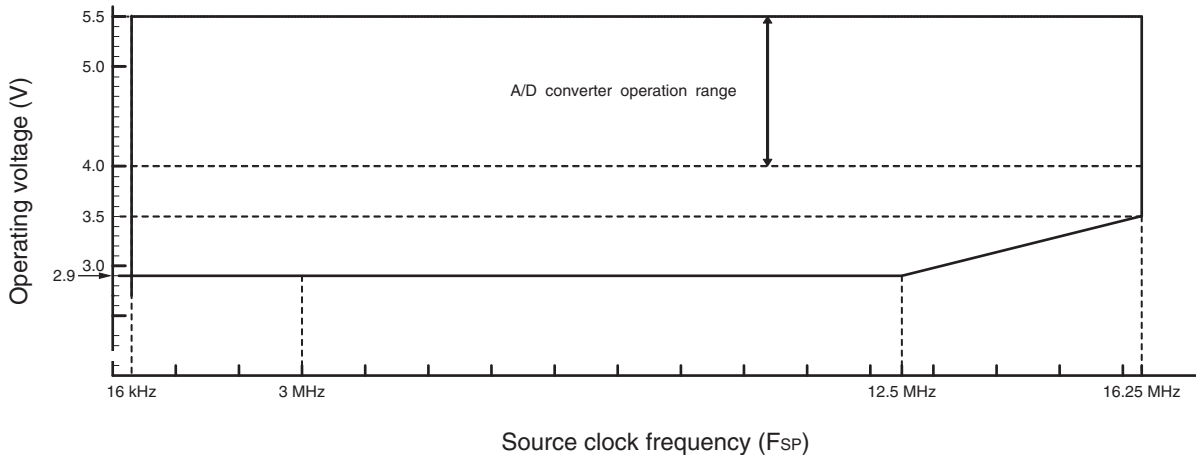
• Schematic diagram of the clock generation block



• Operating voltage - Operating frequency (When  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )  
MB95390H (without the on-chip debug function)



• Operating voltage - Operating frequency (When  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )  
MB95390H (with the on-chip debug function)



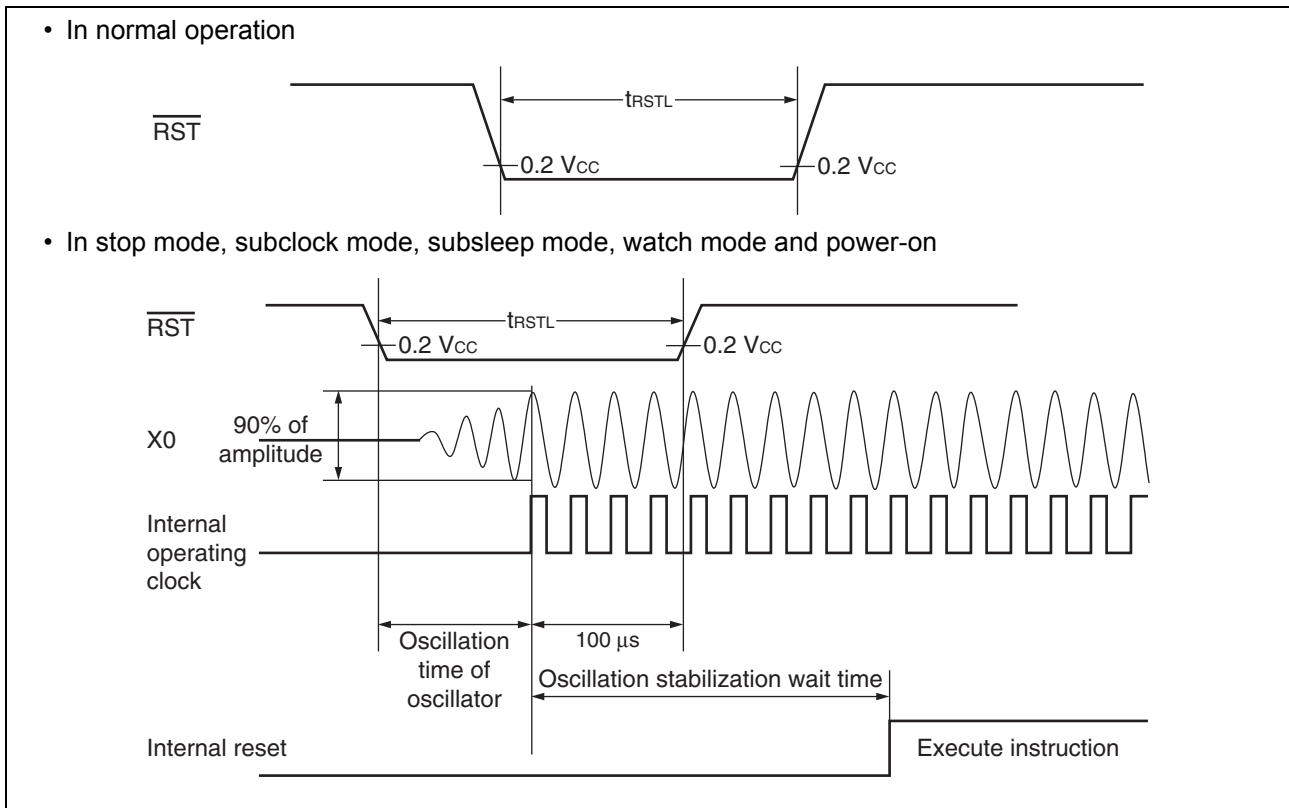
14.4.3 External Reset

( $V_{CC} = 5.0 V \pm 10\%$ ,  $V_{SS} = 0.0 V$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ )

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{RST}$ "L" level pulse width	$t_{RSTL}$	$2 t_{MCLK}^{*1}$	—	ns	In normal operation
		Oscillation time of the oscillator <sup>*2</sup> + 100	—	$\mu s$	In stop mode, subclock mode, subsleep mode, watch mode, and power-on
		100	—	$\mu s$	In time-base timer mode

\*1: See "Source Clock/Machine Clock" for  $t_{MCLK}$ .

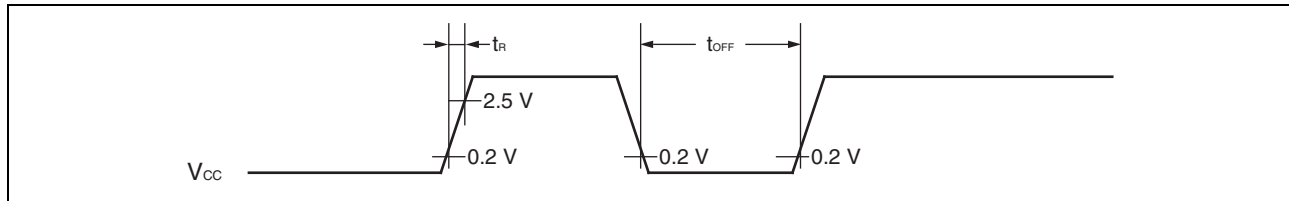
\*2: The oscillation time of an oscillator is the time for it to reach 90% of its amplitude. The crystal oscillator has an oscillation time of between several ms and tens of ms. The ceramic oscillator has an oscillation time of between hundreds of  $\mu s$  and several ms. The external clock has an oscillation time of 0 ms. The CR oscillator clock has an oscillation time of between several  $\mu s$  and several ms.



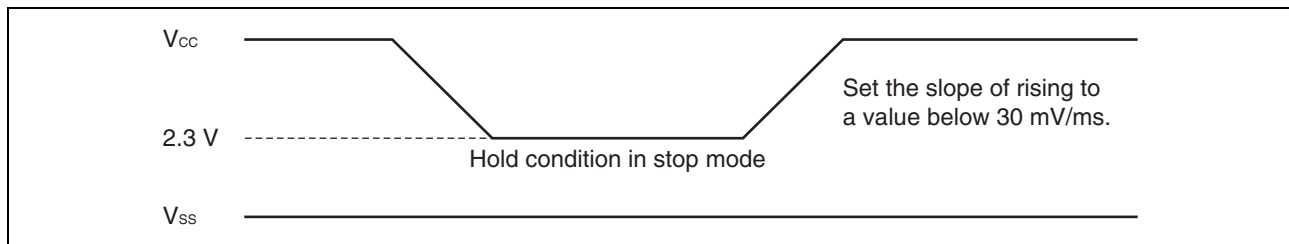
## 14.4.4 Power-on Reset

( $V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power supply rising time	$t_R$	—	—	50	ms	
Power supply cutoff time	$t_{OFF}$	—	1	—	ms	Wait time until power-on



**Note:** A sudden change of power supply voltage may activate the power-on reset function. When changing the power supply voltage during the operation, set the slope of rising to a value below within 30 mV/ms as shown below.

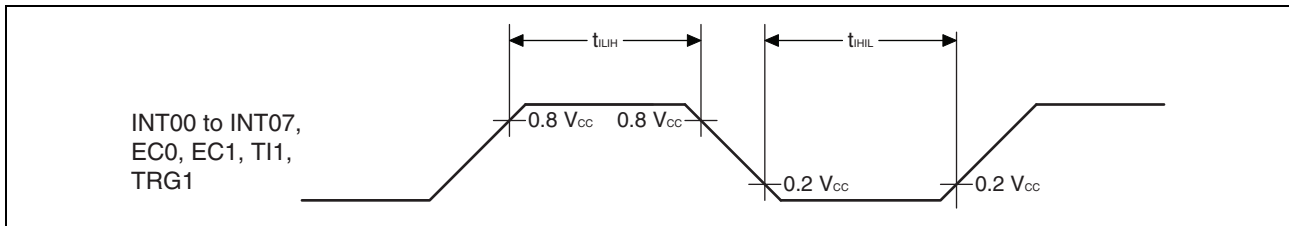


14.4.5 Peripheral Input Timing

( $V_{CC} = 5.0 V \pm 10\%$ ,  $V_{SS} = 0.0 V$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ )

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Peripheral input "H" pulse width	$t_{ILIH}$	INT00 to INT07, EC0, EC1, TI1, TRG1	$2 t_{MCLK}^*$	—	ns
Peripheral input "L" pulse width	$t_{IHIL}$		$2 t_{MCLK}^*$	—	ns

\*: See "Source Clock/Machine Clock" for  $t_{MCLK}$ .



**14.4.6 LIN-UART Timing**

Sampling is executed at the rising edge of the sampling clock\*1, and serial clock delay is disabled\*2.  
 (ESCR register: SCES bit = 0, ECCR register: SCDE bit = 0)

( $V_{CC} = 5.0 V \pm 10\%$ ,  $AV_{SS} = V_{SS} = 0.0 V$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ )

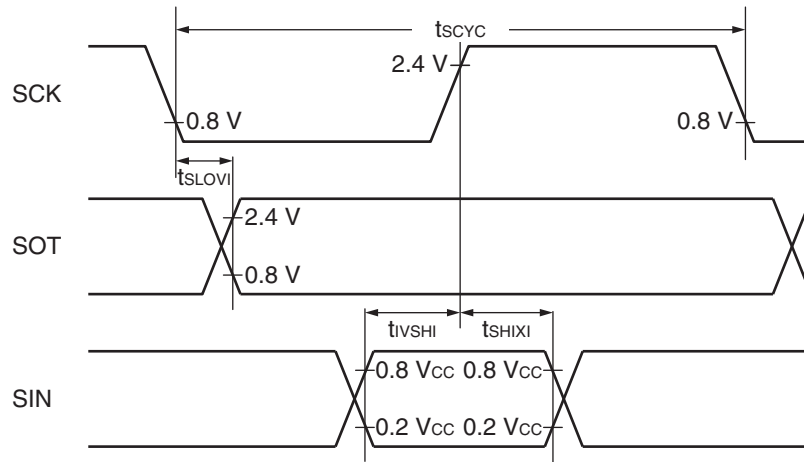
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCK	Internal clock operation output pin: $C_L = 80 \text{ pF} + 1 \text{ TTL}$	$5 t_{MCLK}^{*3}$	—	ns
SCK $\downarrow \rightarrow$ SOT delay time	$t_{SLOVI}$	SCK, SOT		-95	+95	ns
Valid SIN $\rightarrow$ SCK $\uparrow$	$t_{IVSHI}$	SCK, SIN		$t_{MCLK}^{*3} + 190$	—	ns
SCK $\uparrow \rightarrow$ valid SIN hold time	$t_{SHIXI}$	SCK, SIN		0	—	ns
Serial clock "L" pulse width	$t_{SLSH}$	SCK	External clock operation output pin: $C_L = 80 \text{ pF} + 1 \text{ TTL}$	$3 t_{MCLK}^{*3} - t_R$	—	ns
Serial clock "H" pulse width	$t_{SHSL}$	SCK		$t_{MCLK}^{*3} + 95$	—	ns
SCK $\downarrow \rightarrow$ SOT delay time	$t_{SLOVE}$	SCK, SOT		—	$2 t_{MCLK}^{*3} + 95$	ns
Valid SIN $\rightarrow$ SCK $\uparrow$	$t_{IVSHE}$	SCK, SIN		190	—	ns
SCK $\uparrow \rightarrow$ valid SIN hold time	$t_{SHIXE}$	SCK, SIN		$t_{MCLK}^{*3} + 95$	—	ns
SCK fall time	$t_F$	SCK		—	10	ns
SCK rise time	$t_R$	SCK		—	10	ns

\*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

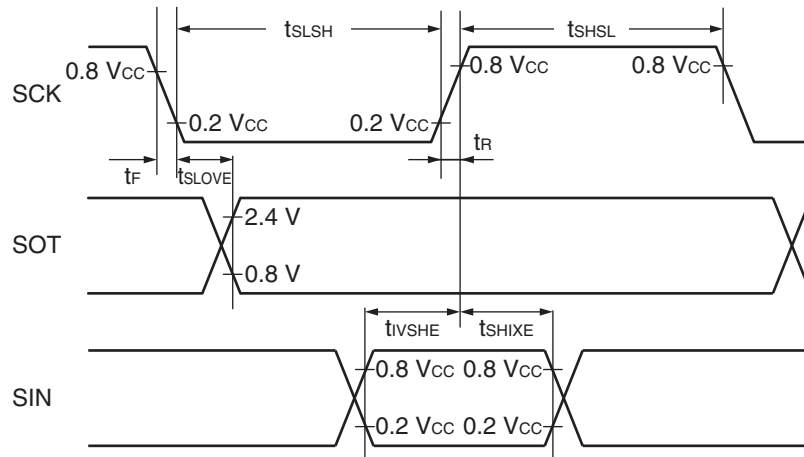
\*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

\*3: See "Source Clock/Machine Clock" for  $t_{MCLK}$ .

• Internal shift clock mode



• External shift clock mode



Sampling is executed at the falling edge of the sampling clock\*<sup>1</sup>, and serial clock delay is disabled\*<sup>2</sup>.  
 (ESCR register: SCES bit = 1, ECCR register: SCDE bit = 0)

(V<sub>CC</sub> = 5.0 V±10%, V<sub>SS</sub> = 0.0 V, T<sub>A</sub> = -40°C to +85°C)

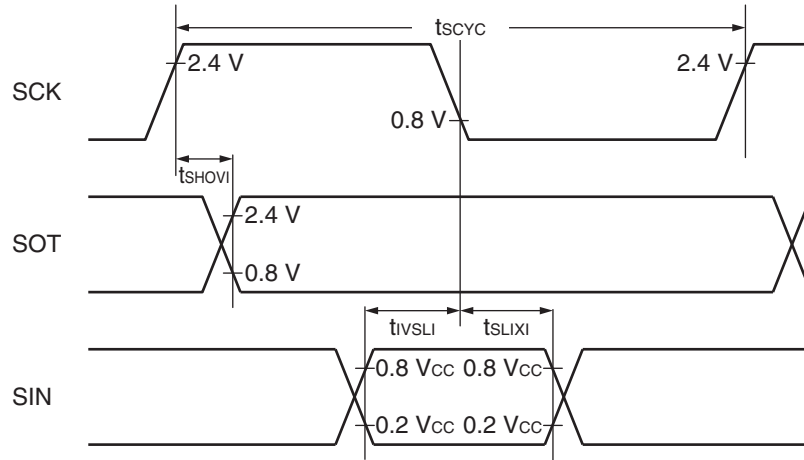
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t <sub>SCYC</sub>	SCK	Internal clock operation output pin: C <sub>L</sub> = 80 pF + 1 TTL	5 t <sub>MCLK</sub> <sup>*3</sup>	—	ns
SCK ↑ → SOT delay time	t <sub>SHOVI</sub>	SCK, SOT		-95	+95	ns
Valid SIN → SCK ↓	t <sub>IVSLI</sub>	SCK, SIN		t <sub>MCLK</sub> <sup>*3</sup> + 190	—	ns
SCK ↓ → valid SIN hold time	t <sub>SLIXI</sub>	SCK, SIN		0	—	ns
Serial clock "H" pulse width	t <sub>SHSL</sub>	SCK	External clock operation output pin: C <sub>L</sub> = 80 pF + 1 TTL	3 t <sub>MCLK</sub> <sup>*3</sup> - t <sub>R</sub>	—	ns
Serial clock "L" pulse width	t <sub>SLSH</sub>	SCK		t <sub>MCLK</sub> <sup>*3</sup> + 95	—	ns
SCK ↑ → SOT delay time	t <sub>SHOVE</sub>	SCK, SOT		—	2 t <sub>MCLK</sub> <sup>*3</sup> + 95	ns
Valid SIN → SCK ↓	t <sub>IVSLE</sub>	SCK, SIN		190	—	ns
SCK ↓ → valid SIN hold time	t <sub>SLIXE</sub>	SCK, SIN		t <sub>MCLK</sub> <sup>*3</sup> + 95	—	ns
SCK fall time	t <sub>F</sub>	SCK		—	10	ns
SCK rise time	t <sub>R</sub>	SCK		—	10	ns

\*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

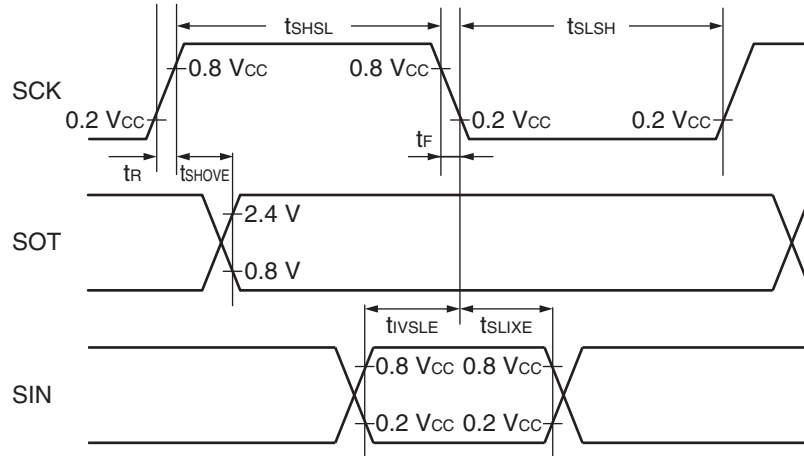
\*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

\*3: See "Source Clock/Machine Clock" for t<sub>MCLK</sub>.

• Internal shift clock mode



• External shift clock mode



Sampling is executed at the rising edge of the sampling clock\*<sup>1</sup>, and serial clock delay is enabled\*<sup>2</sup>.  
 (ESCR register: SCES bit = 0, ECCR register: SCDE bit = 1)

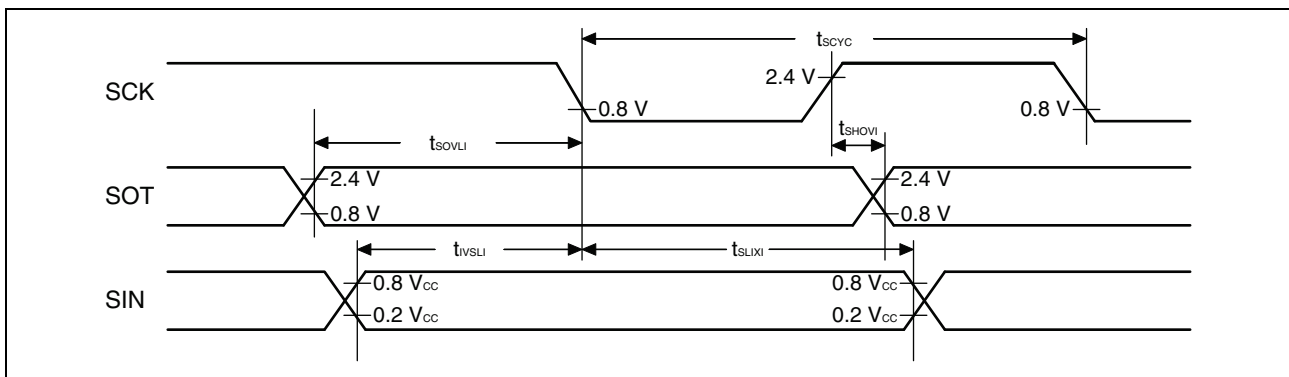
( $V_{CC} = 5.0 V \pm 10\%$ ,  $V_{SS} = 0.0 V$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ )

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCK	Internal clock operation output pin: $C_L = 80 \text{ pF} + 1 \text{ TTL}$	$5 t_{MCLK}^{*3}$	—	ns
SCK $\uparrow$ $\rightarrow$ SOT delay time	$t_{SHOVI}$	SCK, SOT		-95	+95	ns
Valid SIN $\rightarrow$ SCK $\downarrow$	$t_{VSLI}$	SCK, SIN		$t_{MCLK}^{*3} + 190$	—	ns
SCK $\downarrow$ $\rightarrow$ valid SIN hold time	$t_{SLIXI}$	SCK, SIN		0	—	ns
SOT $\rightarrow$ SCK $\downarrow$ delay time	$t_{SOVLI}$	SCK, SOT		—	$4 t_{MCLK}^{*3}$	ns

\*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

\*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

\*3: See "Source Clock/Machine Clock" for  $t_{MCLK}$ .



Sampling is executed at the falling edge of the sampling clock\*1, and serial clock delay is enabled\*2.  
 (ESCR register: SCES bit = 1, ECCR register: SCDE bit = 1)

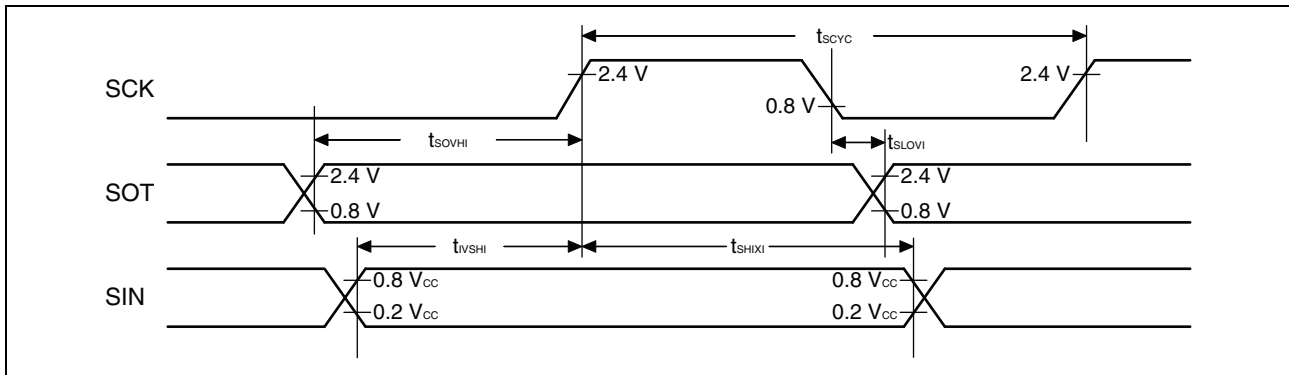
( $V_{CC} = 5.0 V \pm 10\%$ ,  $V_{SS} = 0.0 V$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ )

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCK	Internal clock operation output pin: $C_L = 80 \text{ pF} + 1 \text{ TTL}$	$5 t_{MCLK}^{*3}$	—	ns
SCK $\downarrow \rightarrow$ SOT delay time	$t_{SLOVI}$	SCK, SOT		-95	+95	ns
Valid SIN $\rightarrow$ SCK $\uparrow$	$t_{IVSHI}$	SCK, SIN		$t_{MCLK}^{*3} + 190$	—	ns
SCK $\uparrow \rightarrow$ valid SIN hold time	$t_{SHIXI}$	SCK, SIN		0	—	ns
SOT $\rightarrow$ SCK $\uparrow$ delay time	$t_{SOVHI}$	SCK, SOT		—	$4 t_{MCLK}^{*3}$	ns

\*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

\*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

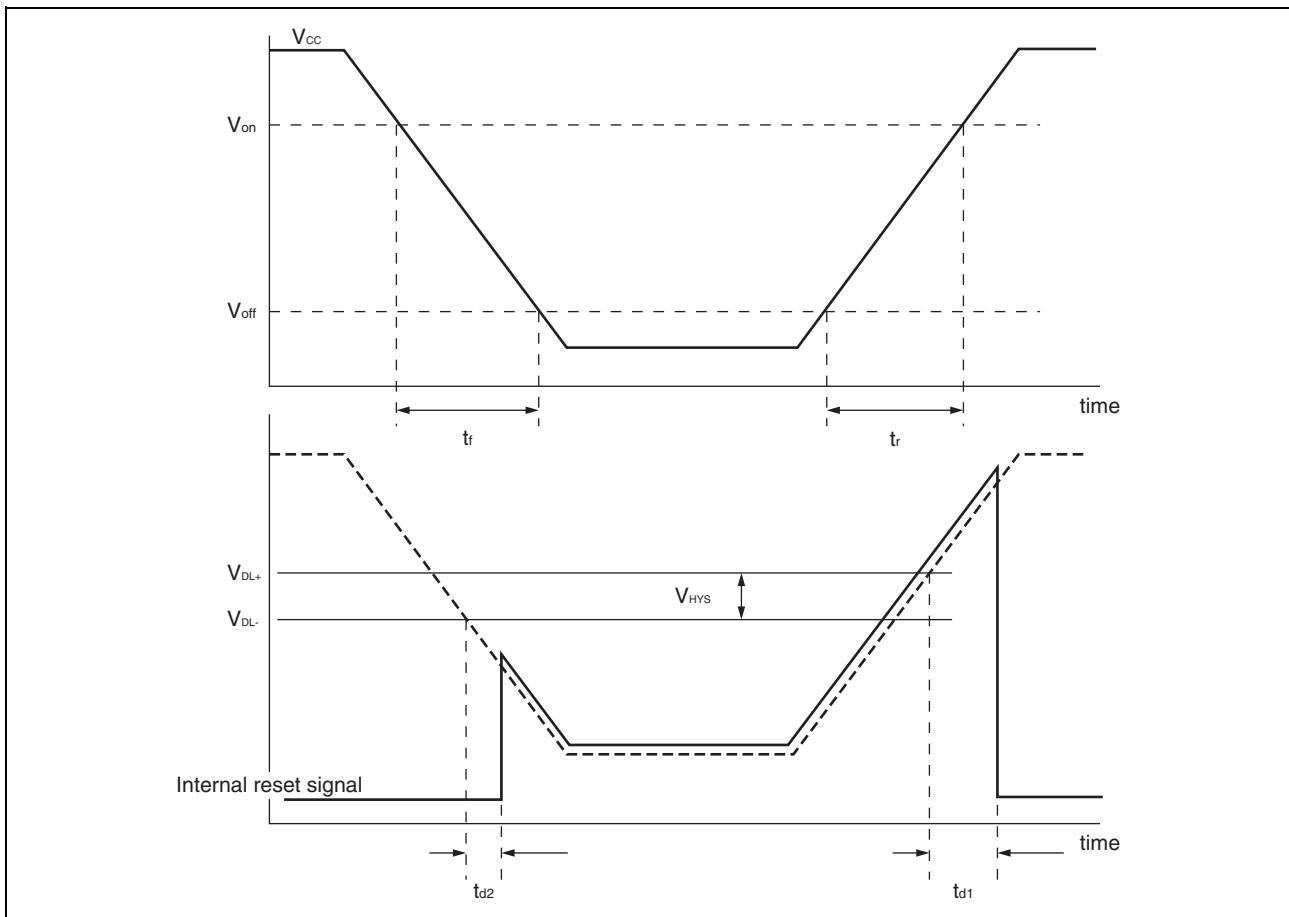
\*3: See "Source Clock/Machine Clock" for  $t_{MCLK}$ .



14.4.7 Low-voltage Detection

( $V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Release voltage	$V_{DL+}$	2.52	2.7	2.88	V	At power supply rise
Detection voltage	$V_{DL-}$	2.42	2.6	2.78	V	At power supply fall
Hysteresis width	$V_{HYS}$	70	100	—	mV	
Power supply start voltage	$V_{off}$	—	—	2.3	V	
Power supply end voltage	$V_{on}$	4.9	—	—	V	
Power supply voltage change time (at power supply rise)	$t_r$	3000	—	—	$\mu\text{s}$	Slope of power supply that the reset release signal generates within the rating ( $V_{DL+}$ )
Power supply voltage change time (at power supply fall)	$t_r$	300	—	—	$\mu\text{s}$	Slope of power supply that the reset detection signal generates within the rating ( $V_{DL-}$ )
Reset release delay time	$t_{d1}$	—	—	300	$\mu\text{s}$	
Reset detection delay time	$t_{d2}$	—	—	20	$\mu\text{s}$	



14.4.8 I<sup>2</sup>C Timing

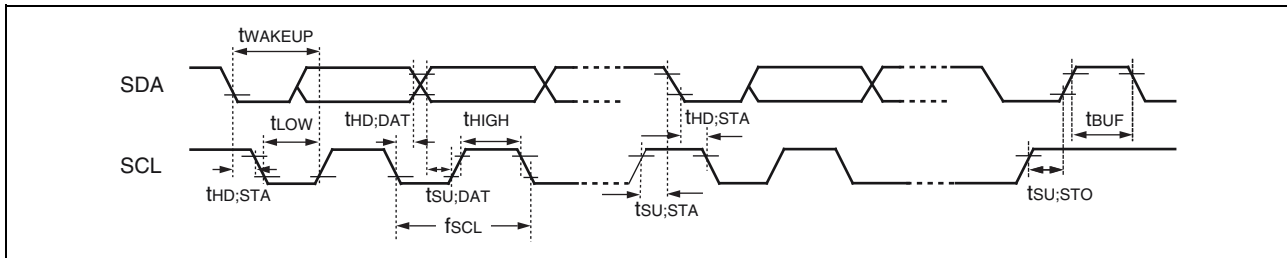
(V<sub>CC</sub> = 5.0 V±10%, AV<sub>SS</sub> = V<sub>SS</sub> = 0.0 V, T<sub>A</sub> = -40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value				Unit
				Standard-mode		Fast-mode		
				Min	Max	Min	Max	
SCL clock frequency	f <sub>SCL</sub>	SCL	R = 1.7 kΩ, C = 50 pF <sup>*1</sup>	0	100	0	400	kHz
(Repeated) START condition hold time SDA ↓ → SCL ↓	t <sub>HD;STA</sub>	SCL, SDA		4.0	—	0.6	—	μs
SCL clock "L" width	t <sub>LOW</sub>	SCL		4.7	—	1.3	—	μs
SCL clock "H" width	t <sub>HIGH</sub>	SCL		4.0	—	0.6	—	μs
(Repeated) START condition setup time SCL ↑ → SDA ↓	t <sub>SU;STA</sub>	SCL, SDA		4.7	—	0.6	—	μs
Data hold time SCL ↓ → SDA ↓↑	t <sub>HD;DAT</sub>	SCL, SDA		0	3.45 <sup>*2</sup>	0	0.9 <sup>*3</sup>	μs
Data setup time SDA ↓↑ → SCL ↑	t <sub>SU;DAT</sub>	SCL, SDA		0.25	—	0.1	—	μs
STOP condition setup time SCL ↑ → SDA ↑	t <sub>SU;STO</sub>	SCL, SDA		4	—	0.6	—	μs
Bus free time between STOP condition and START condition	t <sub>BUF</sub>	SCL, SDA		4.7	—	1.3	—	μs

\*1: R represents the pull-up resistor of the SCL and SDA lines, and C the load capacitor of the SCL and SDA lines.

\*2: The maximum t<sub>HD;DAT</sub> in the Standard-mode is applicable only when the time during which the device is holding the SCL signal at "L" (t<sub>LOW</sub>) does not extend.

\*3: A Fast-mode I<sup>2</sup>C-bus device can be used in a Standard-mode I<sup>2</sup>C-bus system, provided that the condition of t<sub>SU;DAT</sub> ≥ 250 ns is fulfilled.



(Continued)

$(V_{CC} = 5.0 V \pm 10\%, AV_{SS} = V_{SS} = 0.0 V, T_A = -40^\circ C \text{ to } +85^\circ C)$ 

Parameter	Symbol	Pin name	Condition	Value*2		Unit	Remarks
				Min	Max		
SCL clock "L" width	$t_{LOW}$	SCL	R = 1.7 k $\Omega$ , C = 50 pF*1	$(2 + nm/2)t_{MCLK} - 20$	—	ns	Master mode
SCL clock "H" width	$t_{HIGH}$	SCL		$(nm/2)t_{MCLK} - 20$	$(nm/2)t_{MCLK} + 20$	ns	Master mode
START condition hold time	$t_{HD;STA}$	SCL, SDA		$(-1 + nm/2)t_{MCLK} - 20$	$(-1 + nm)t_{MCLK} + 20$	ns	Master mode Maximum value is applied when m, n = 1, 8. Otherwise, the minimum value is applied.
STOP condition setup time	$t_{SU;STO}$	SCL, SDA		$(1 + nm/2)t_{MCLK} - 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Master mode
START condition setup time	$t_{SU;STA}$	SCL, SDA		$(1 + nm/2)t_{MCLK} - 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Master mode
Bus free time between STOP condition and START condition	$t_{BUF}$	SCL, SDA		$(2 nm + 4)t_{MCLK} - 20$	—	ns	
Data hold time	$t_{HD;DAT}$	SCL, SDA		$3 t_{MCLK} - 20$	—	ns	Master mode
Data setup time	$t_{SU;DAT}$	SCL, SDA		$(-2 + nm/2)t_{MCLK} - 20$	$(-1 + nm/2)t_{MCLK} + 20$	ns	Master mode When assuming that "L" of SCL is not extended, the minimum value is applied to first bit of continuous data. Otherwise, the maximum value is applied.
Setup time between clearing interrupt and SCL rising	$t_{SU;INT}$	SCL		$(nm/2)t_{MCLK} - 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Minimum value is applied to interrupt at 9th SCL $\downarrow$ . Maximum value is applied to the interrupt at the 8th SCL $\downarrow$ .

*(Continued)*

(Continued)

 $(V_{CC} = 5.0 V \pm 10\%, AV_{SS} = V_{SS} = 0.0 V, T_A = -40^\circ C \text{ to } +85^\circ C)$ 

Parameter	Symbol	Pin name	Condition	Value*2		Unit	Remarks
				Min	Max		
SCL clock "L" width	$t_{LOW}$	SCL	R = 1.7 k $\Omega$ , C = 50 pF*1	$4 t_{MCLK} - 20$	—	ns	At reception
SCL clock "H" width	$t_{HIGH}$	SCL		$4 t_{MCLK} - 20$	—	ns	At reception
START condition detection	$t_{HD;STA}$	SCL, SDA		$2 t_{MCLK} - 20$	—	ns	Not detected when 1 $t_{MCLK}$ is used at reception
STOP condition detection	$t_{SU;STO}$	SCL, SDA		$2 t_{MCLK} - 20$	—	ns	Not detected when 1 $t_{MCLK}$ is used at reception
RESTART condition detection condition	$t_{SU;STA}$	SCL, SDA		$2 t_{MCLK} - 20$	—	ns	Not detected when 1 $t_{MCLK}$ is used at reception
Bus free time	$t_{BUF}$	SCL, SDA		$2 t_{MCLK} - 20$	—	ns	At reception
Data hold time	$t_{HD;DAT}$	SCL, SDA		$2 t_{MCLK} - 20$	—	ns	At slave transmission mode
Data setup time	$t_{SU;DAT}$	SCL, SDA		$t_{LOW} - 3 t_{MCLK} - 20$	—	ns	At slave transmission mode
Data hold time	$t_{HD;DAT}$	SCL, SDA		0	—	ns	At reception
Data setup time	$t_{SU;DAT}$	SCL, SDA		$t_{MCLK} - 20$	—	ns	At reception
SDA $\downarrow$ → SCL $\uparrow$ (at wakeup function)	$t_{WAKEUP}$	SCL, SDA	Oscillation stabilization wait time $+2 t_{MCLK} - 20$	—	ns		

\*1: R represents the pull-up resistor of the SCL and SDA lines, and C the load capacitor of the SCL and SDA lines.

- \*2:
- See "Source Clock/Machine Clock" for  $t_{MCLK}$ .
  - m represents the CS4 bit and CS3 bit (bit4 and bit3) in the I<sup>2</sup>C clock control register (ICCR0).
  - n represents the CS2 bit to CS0 bit (bit2 to bit0) in the I<sup>2</sup>C clock control register (ICCR0).
  - The actual timing of I<sup>2</sup>C is determined by the values of m and n set by the machine clock ( $t_{MCLK}$ ) and the CS4 to CS0 bits in the ICCR0 register.
  - Standard-mode:  
m and n can be set to values in the following range:  $0.9 \text{ MHz} < t_{MCLK} \text{ (machine clock)} < 10 \text{ MHz}$ .  
The usable frequencies of the machine clock are determined by the settings of m and n as shown below.
 

(m, n) = (1, 8)	: $0.9 \text{ MHz} < t_{MCLK} \leq 1 \text{ MHz}$
(m, n) = (1, 22), (5, 4), (6, 4), (7, 4), (8, 4)	: $0.9 \text{ MHz} < t_{MCLK} \leq 2 \text{ MHz}$
(m, n) = (1, 38), (5, 8), (6, 8), (7, 8), (8, 8)	: $0.9 \text{ MHz} < t_{MCLK} \leq 4 \text{ MHz}$
(m, n) = (1, 98)	: $0.9 \text{ MHz} < t_{MCLK} \leq 10 \text{ MHz}$
  - Fast-mode:  
m and n can be set to values in the following range:  $3.3 \text{ MHz} < t_{MCLK} \text{ (machine clock)} < 10 \text{ MHz}$ .  
The usable frequencies of the machine clock are determined by the settings of m and n as shown below.
 

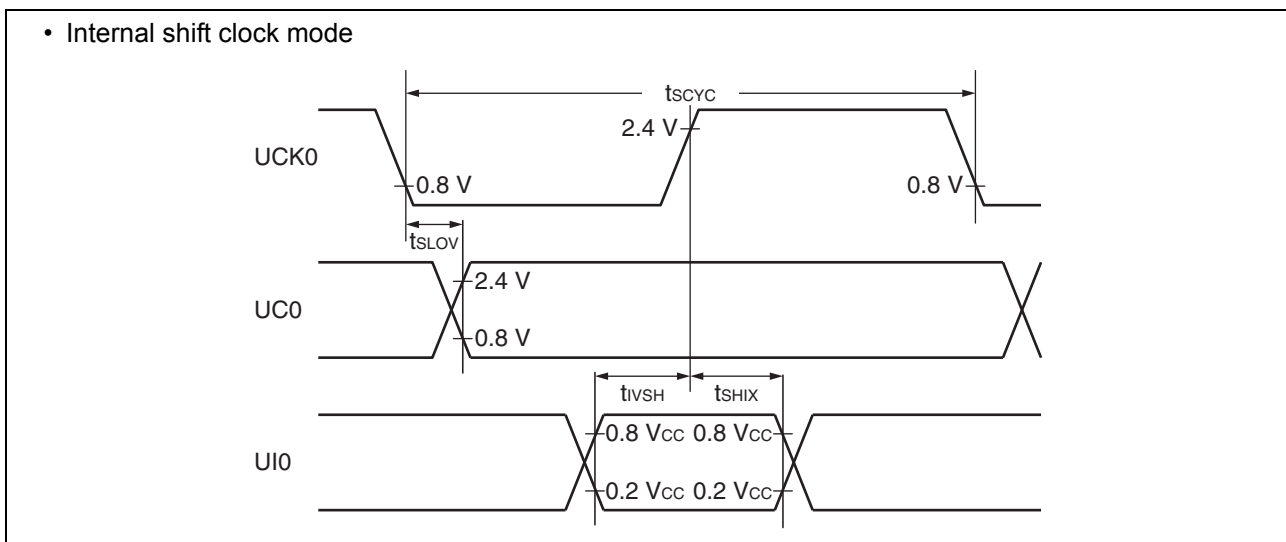
(m, n) = (1, 8)	: $3.3 \text{ MHz} < t_{MCLK} \leq 4 \text{ MHz}$
(m, n) = (1, 22), (5, 4)	: $3.3 \text{ MHz} < t_{MCLK} \leq 8 \text{ MHz}$
(m, n) = (6, 4)	: $3.3 \text{ MHz} < t_{MCLK} \leq 10 \text{ MHz}$

## 14.4.9 UART/SIO, Serial I/O Timing

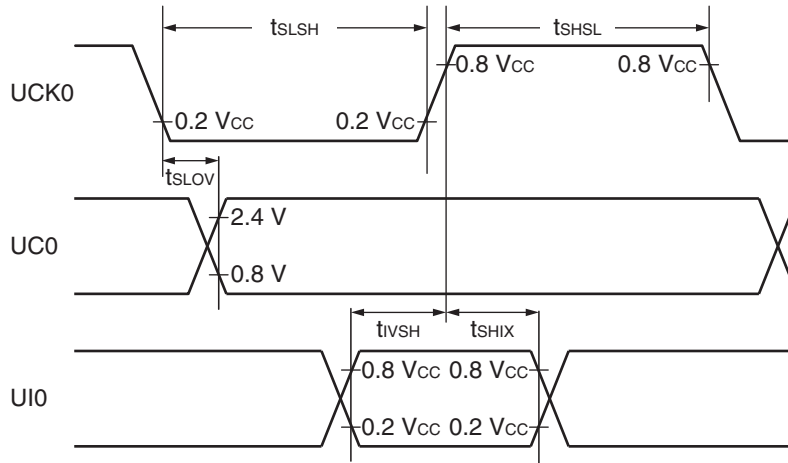
( $V_{CC} = 5.0 V \pm 10\%$ ,  $AV_{SS} = V_{SS} = 0.0 V$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ )

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	UCK0	Internal clock operation	$4 t_{MCLK}^*$	—	ns
UCK $\downarrow \rightarrow$ UO time	$t_{SLOV}$	UCK0, UO0		-190	+190	ns
Valid UI $\rightarrow$ UCK $\uparrow$	$t_{IVSH}$	UCK0, UI0		$2 t_{MCLK}^*$	—	ns
UCK $\uparrow \rightarrow$ valid UI hold time	$t_{SHIX}$	UCK, UI0		$2 t_{MCLK}^*$	—	ns
Serial clock "H" pulse width	$t_{SHSL}$	UCK0	External clock operation	$4 t_{MCLK}^*$	—	ns
Serial clock "L" pulse width	$t_{SLSH}$	UCK0		$4 t_{MCLK}^*$	—	ns
UCK $\downarrow \rightarrow$ UO time	$t_{SLOV}$	UCK0, UO0		—	190	ns
Valid UI $\rightarrow$ UCK $\uparrow$	$t_{IVSH}$	UCK0, UI0		$2 t_{MCLK}^*$	—	ns
UCK $\uparrow \rightarrow$ valid UI hold time	$t_{SHIX}$	UCK0, UI0	$2 t_{MCLK}^*$	—	ns	

\*: See "Source Clock/Machine Clock" for  $t_{MCLK}$ .

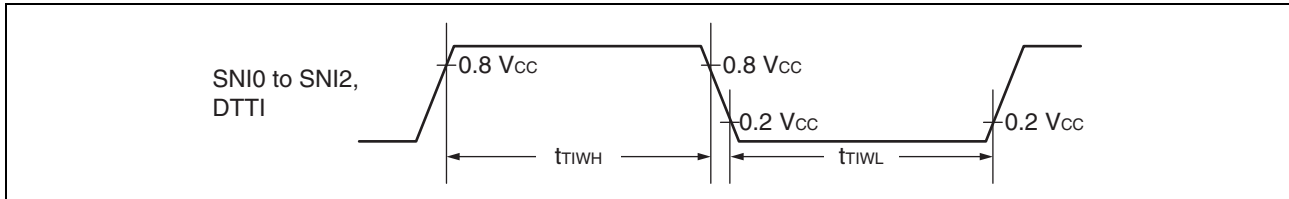


• External shift clock mode



**14.4.10 MPG Input Timing**
 $(V_{CC} = 5.0 V \pm 10\%, AV_{SS} = V_{SS} = 0.0 V, T_A = -40^\circ C \text{ to } +85^\circ C)$ 

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	$t_{TIWH}$ $t_{TIWL}$	SNI0 to SNI2, DTTI	—	$4 t_{MCLK}$	—	ns	



**14.5 A/D Converter**
**14.5.1 A/D Converter Electrical Characteristics**
 $(V_{CC} = 4.0\text{ V to } 5.5\text{ V}, V_{SS} = 0.0\text{ V}, T_A = -40^\circ\text{C to } +85^\circ\text{C})$ 

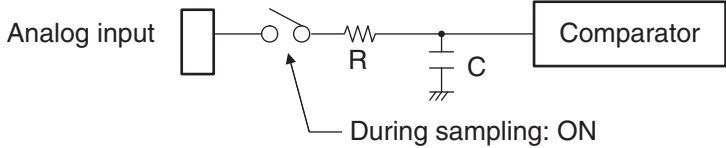
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error		-3	—	+3	LSB	
Linearity error		-2.5	—	+2.5	LSB	
Differential linear error		-1.9	—	+1.9	LSB	
Zero transition voltage	$V_{OT}$	$V_{SS} - 1.5\text{ LSB}$	$V_{SS} + 0.5\text{ LSB}$	$V_{SS} + 2.5\text{ LSB}$	V	
Full-scale transition voltage	$V_{FST}$	$V_{CC} - 4.5\text{ LSB}$	$V_{CC} - 2\text{ LSB}$	$V_{CC} + 0.5\text{ LSB}$	V	
Compare time	—	0.9	—	16500	$\mu\text{s}$	$4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$
		1.8	—	16500	$\mu\text{s}$	$4.0\text{ V} \leq V_{CC} < 4.5\text{ V}$
Sampling time	—	0.6	—	$\infty$	$\mu\text{s}$	$4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ , with external impedance $< 5.4\text{ k}\Omega$
		1.2	—	$\infty$	$\mu\text{s}$	$4.0\text{ V} \leq V_{CC} < 4.5\text{ V}$ , with external impedance $< 2.4\text{ k}\Omega$
Analog input current	$I_{AIN}$	-0.3	—	+0.3	$\mu\text{A}$	
Analog input voltage	$V_{AIN}$	$V_{SS}$	—	$V_{CC}$	V	

14.5.2 Notes on Using the A/D Converter

■ External impedance of analog input and its sampling time

- The A/D converter has a sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the capacitor of the internal sample and hold circuit is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, considering the relationship between the external impedance and minimum sampling time, either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. In addition, if sufficient sampling time cannot be secured, connect a capacitor of about 0.1  $\mu\text{F}$  to the analog input pin.

• Analog input equivalent circuit

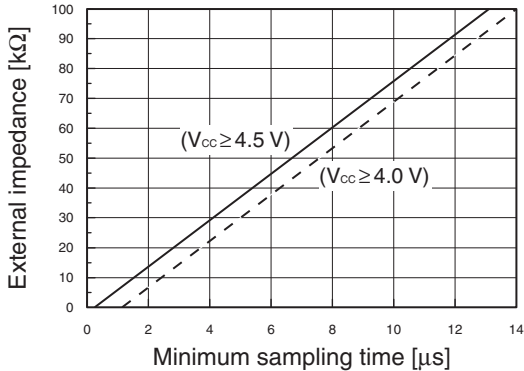


$V_{CC}$	R	C
$4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$	1.95 k $\Omega$ (Max)	17 pF (Max)
$4.0\text{ V} \leq V_{CC} < 4.5\text{ V}$	8.98 k $\Omega$ (Max)	17 pF (Max)

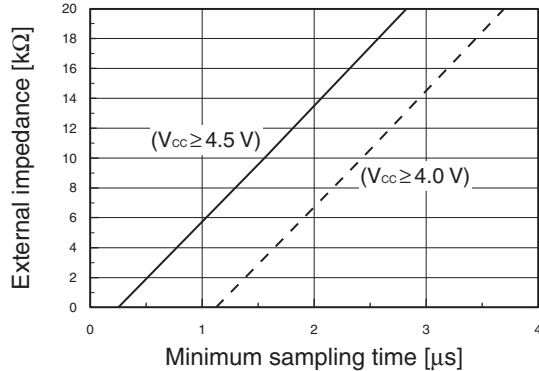
Note: The values are reference values.

• Relationship between external impedance and minimum sampling time

[External impedance = 0 k $\Omega$  to 100 k $\Omega$ ]



[External impedance = 0 k $\Omega$  to 20 k $\Omega$ ]

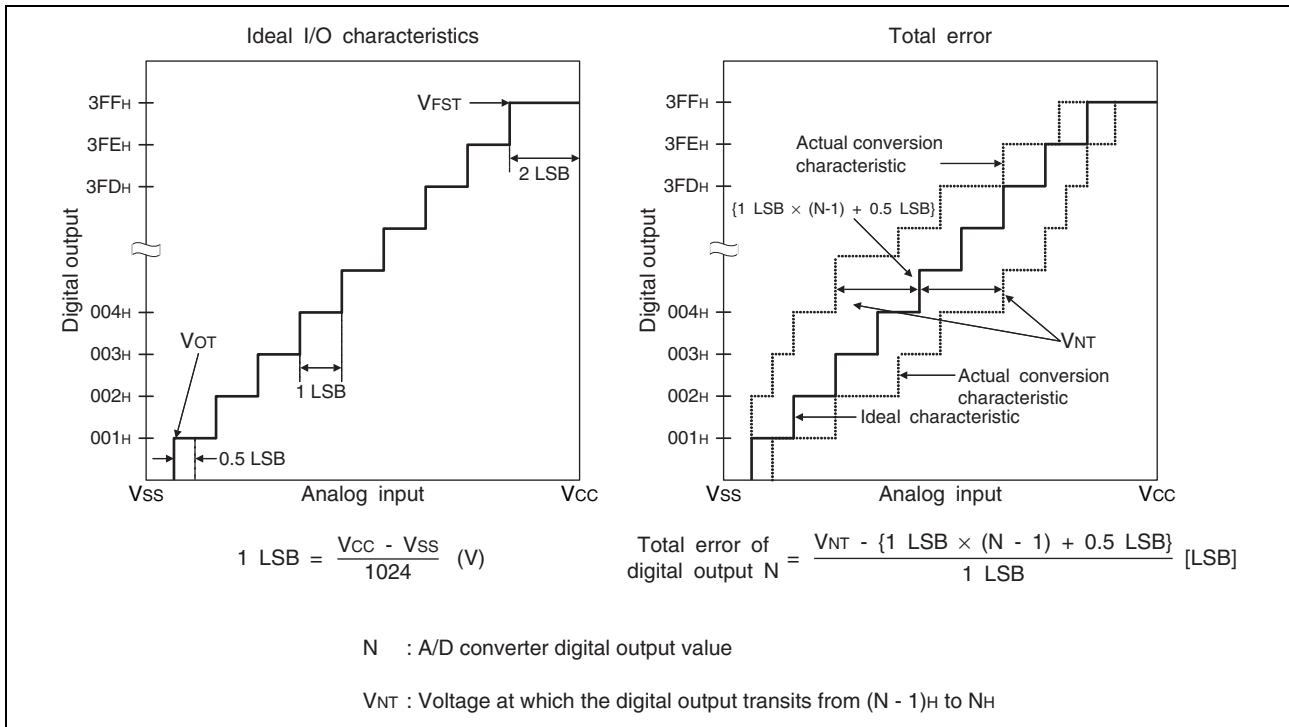


■ A/D conversion error

As  $|V_{CC} - V_{SS}|$  decreases, the A/D conversion error increases proportionately.

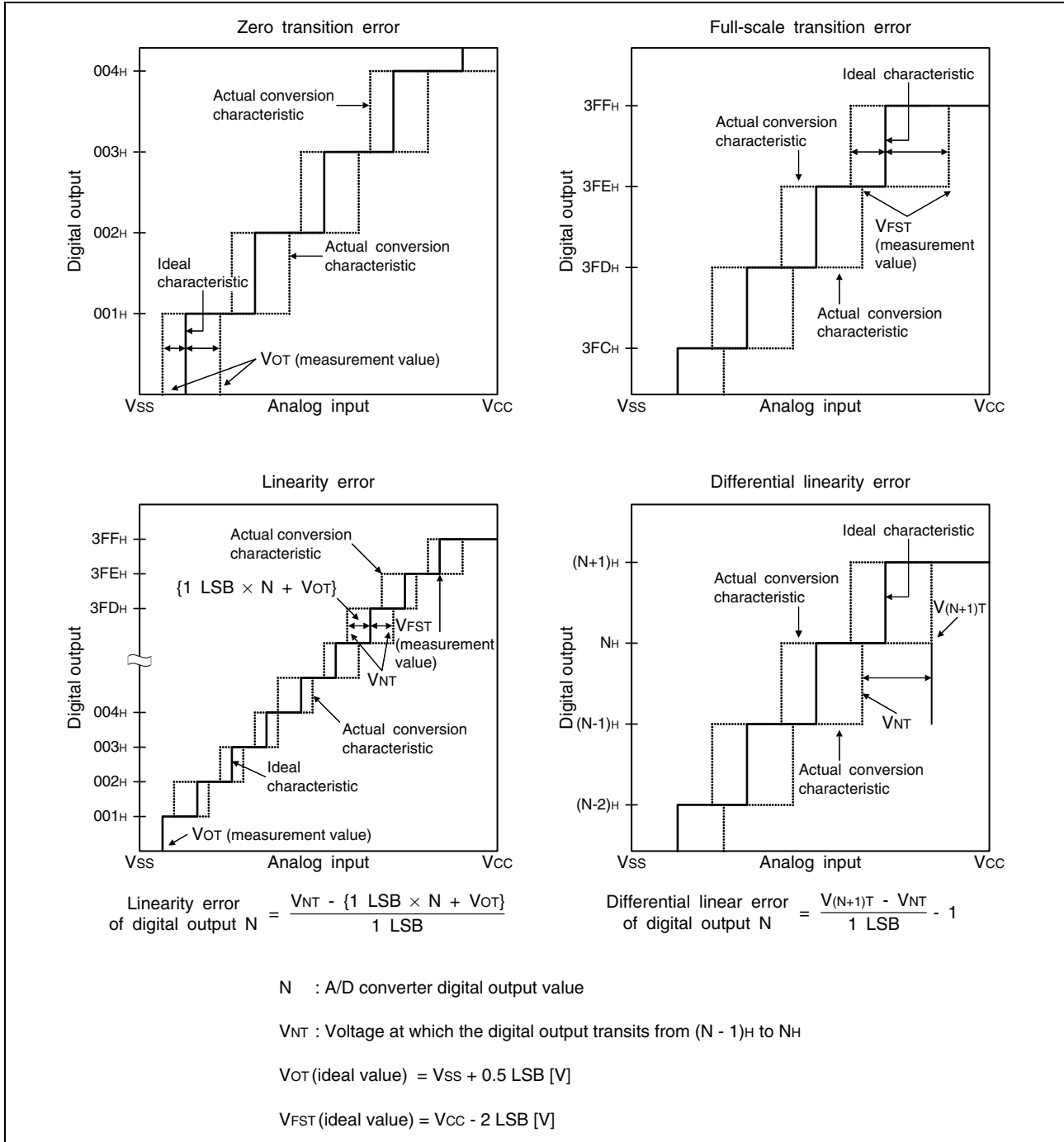
14.5.3 Definitions of A/D Converter Terms

- **Resolution**  
It indicates the level of analog variation that can be distinguished by the A/D converter. When the number of bits is 10, analog voltage can be divided into  $2^{10} = 1024$ .
- **Linearity error (unit: LSB)**  
It indicates how much an actual conversion value deviates from the straight line connecting the zero transition point (“00 0000 0000” ← → “00 0000 0001”) of a device to the full-scale transition point (“11 1111 1111” ← → “11 1111 1110”) of the same device.
- **Differential linear error (unit: LSB)**  
It indicates how much the input voltage required to change the output code by 1 LSB deviates from an ideal value.
- **Total error (unit: LSB)**  
It indicates the difference between an actual value and a theoretical value. The error can be caused by a zero transition error, a full-scale transition errors, a linearity error, a quantum error, or noise.



(Continued)

(Continued)



**14.6 Flash Memory Write/Erase Characteristics**

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time (2 Kbyte sector)	—	0.2* <sup>1</sup>	0.5* <sup>2</sup>	s	The time of writing 00 <sub>H</sub> prior to erasure is excluded.
Sector erase time (16 Kbyte sector)	—	0.5* <sup>1</sup>	7.5* <sup>2</sup>	s	The time of writing 00 <sub>H</sub> prior to erasure is excluded.
Byte writing time	—	21	6100* <sup>2</sup>	μs	System-level overhead is excluded.
Erase/write cycle	100000	—	—	cycle	
Power supply voltage at erase/write	3.0	—	5.5	V	
Flash memory data retention time	20* <sup>3</sup>	—	—	year	Average T <sub>A</sub> = +85°C

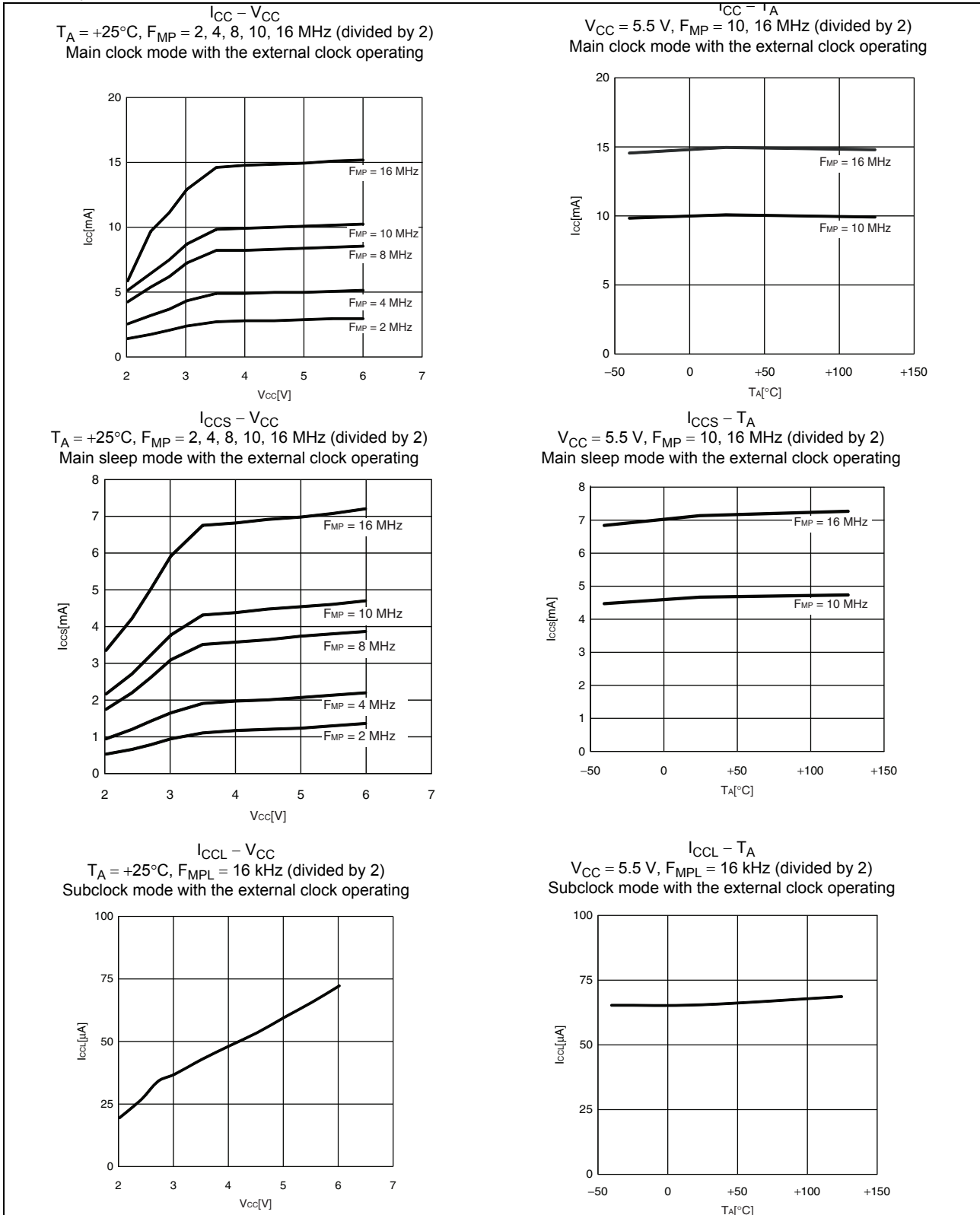
\*1: T<sub>A</sub> = +25°C, V<sub>CC</sub> = 5.0 V, 100000 cycles

\*2: T<sub>A</sub> = +85°C, V<sub>CC</sub> = 3.0 V, 100000 cycles

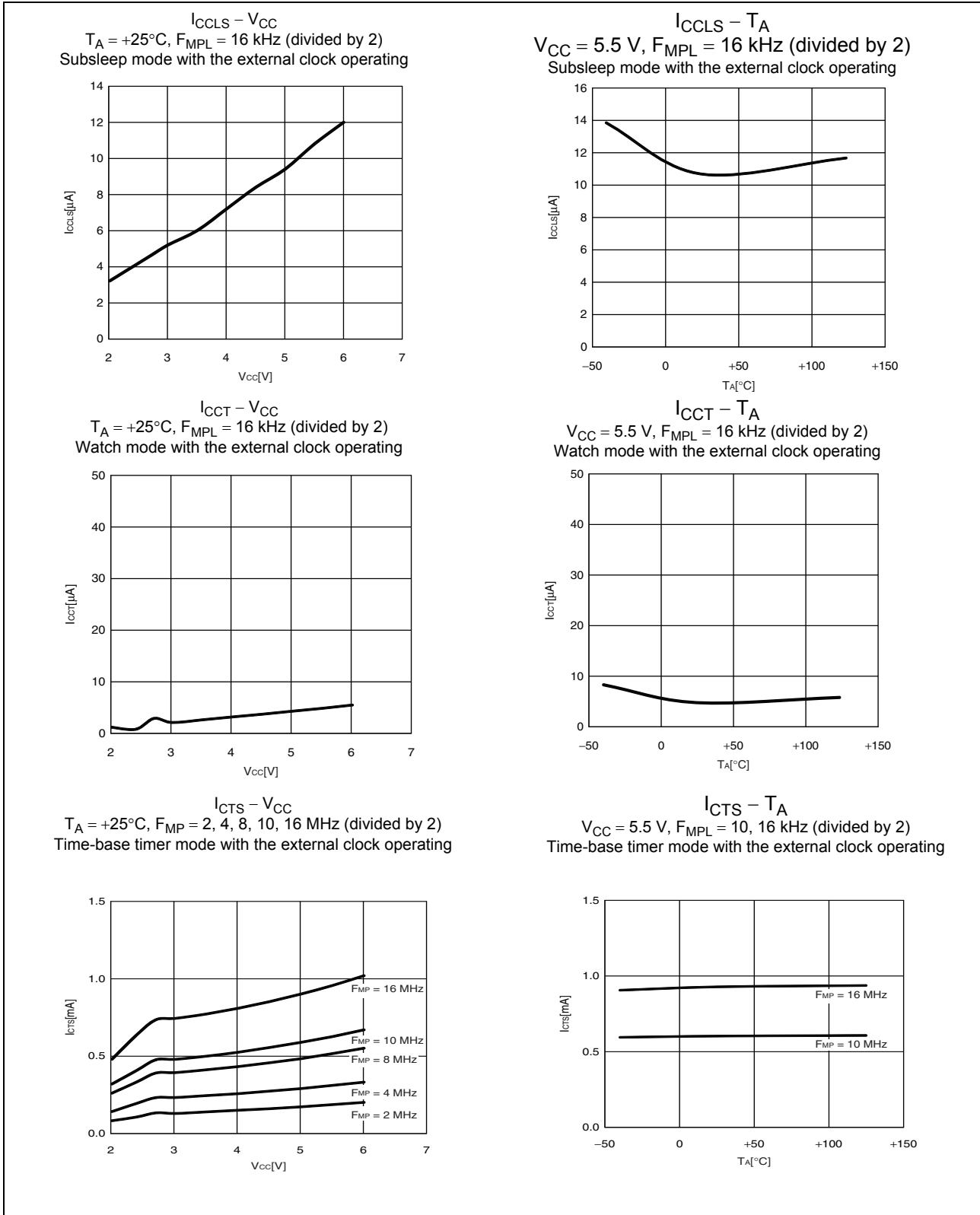
\*3: This value is converted from the result of a technology reliability assessment. (The value is converted from the result of a high temperature accelerated test using the Arrhenius equation with the average temperature being +85°C).

### 15. Sample Characteristics

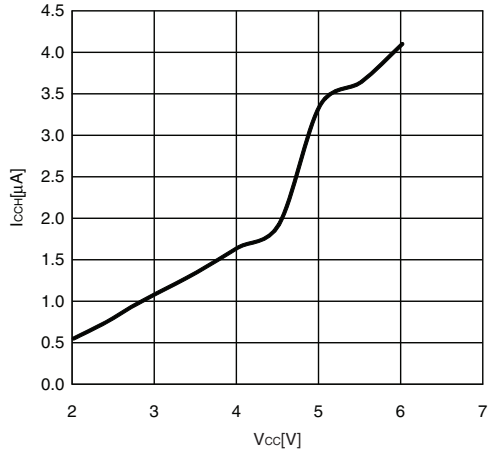
■ Power supply current temperature characteristics



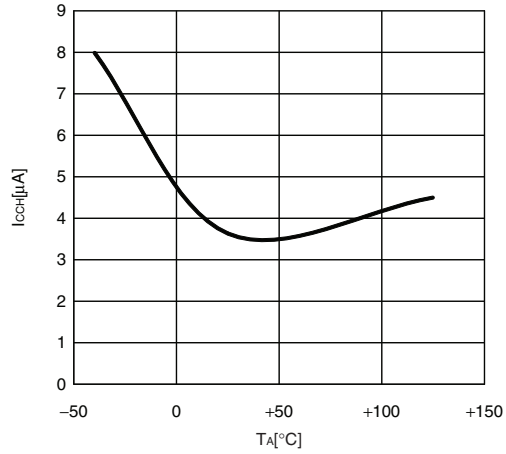
(Continued)



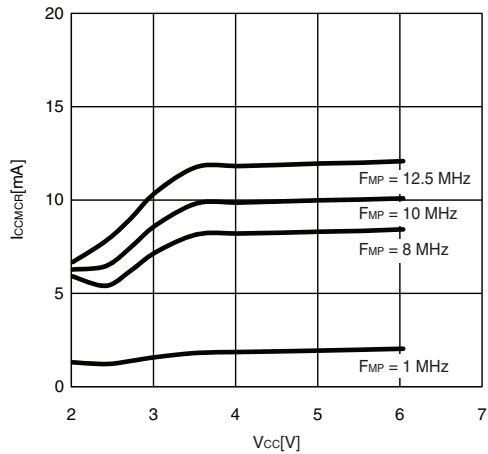
$I_{CCH} - V_{CC}$   
 $T_A = +25^\circ\text{C}, F_{MPL} = (\text{stop})$   
 Substop mode with the external clock stopping



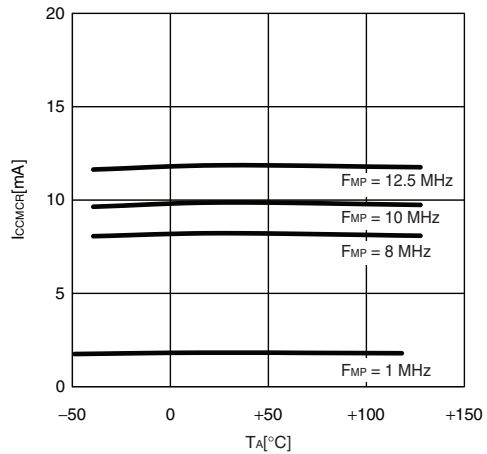
$I_{CCH} - T_A$   
 $V_{CC} = 5.5 \text{ V}, F_{MPL} = (\text{stop})$   
 Substop mode with the external clock stopping



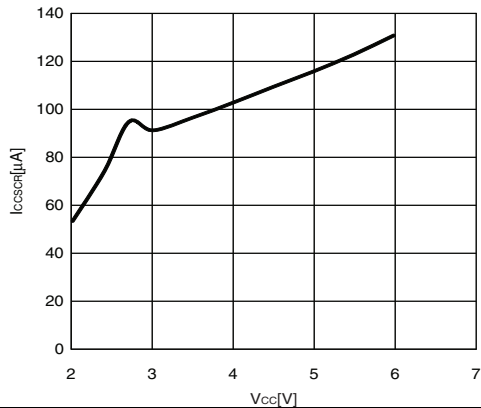
$I_{CCMCR} - V_{CC}$   
 $T_A = +25^\circ\text{C}, F_{MP} = 1, 8, 10, 12.5 \text{ MHz (no division)}$   
 Main clock mode with the main CR clock operating



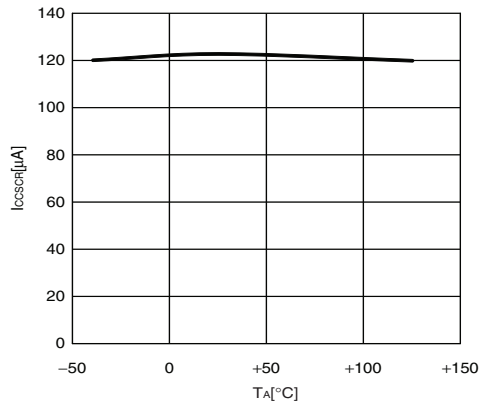
$I_{CCMCR} - T_A$   
 $V_{CC} = 5.5 \text{ V}, F_{MP} = 1, 8, 10, 12.5 \text{ MHz (no division)}$   
 Main clock mode with the main CR clock operating



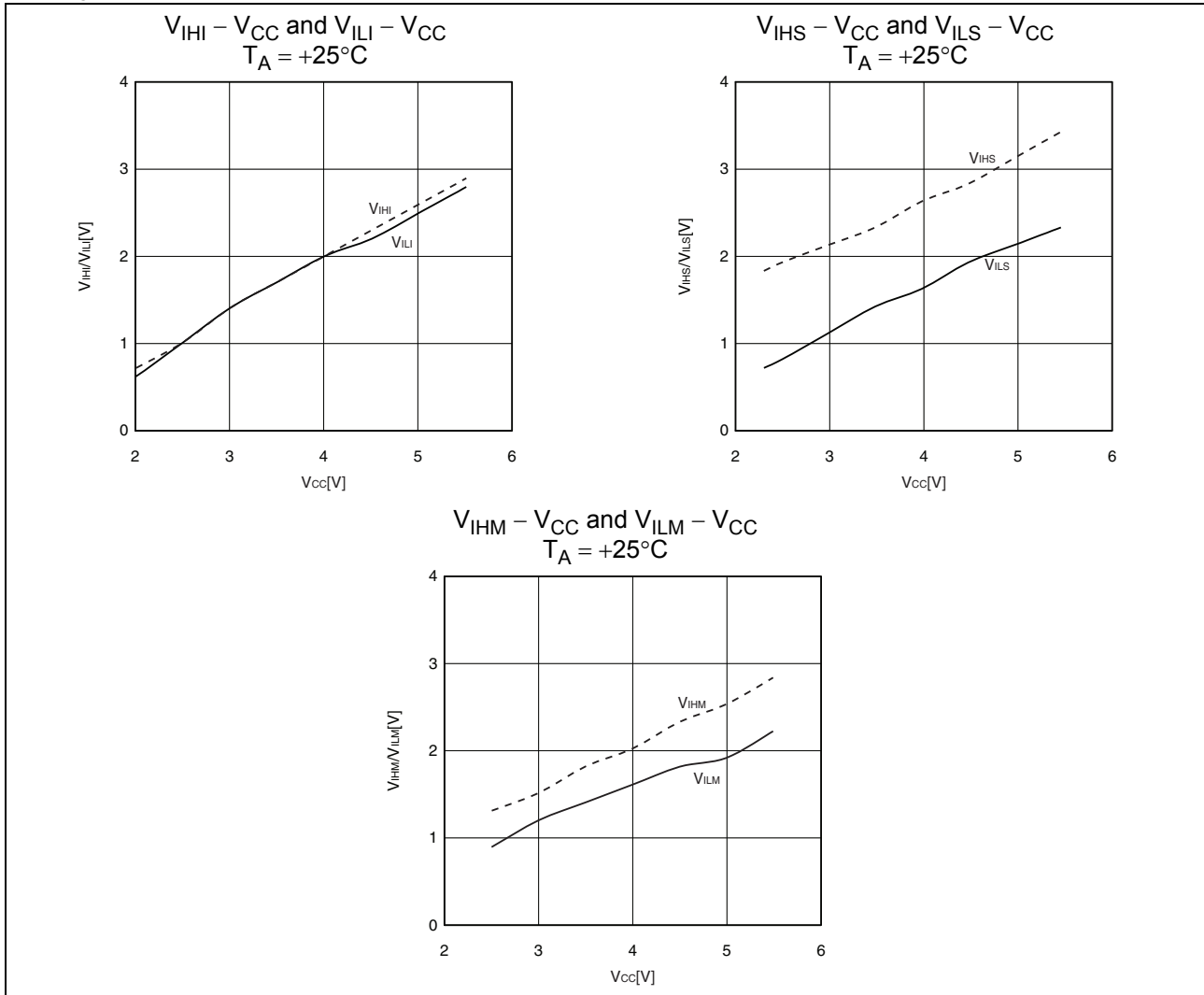
$I_{CCSCR} - V_{CC}$   
 $T_A = +25^\circ\text{C}, F_{MPL} = 50 \text{ kHz (divided by 2)}$   
 Subclock mode with the sub-CR clock operating



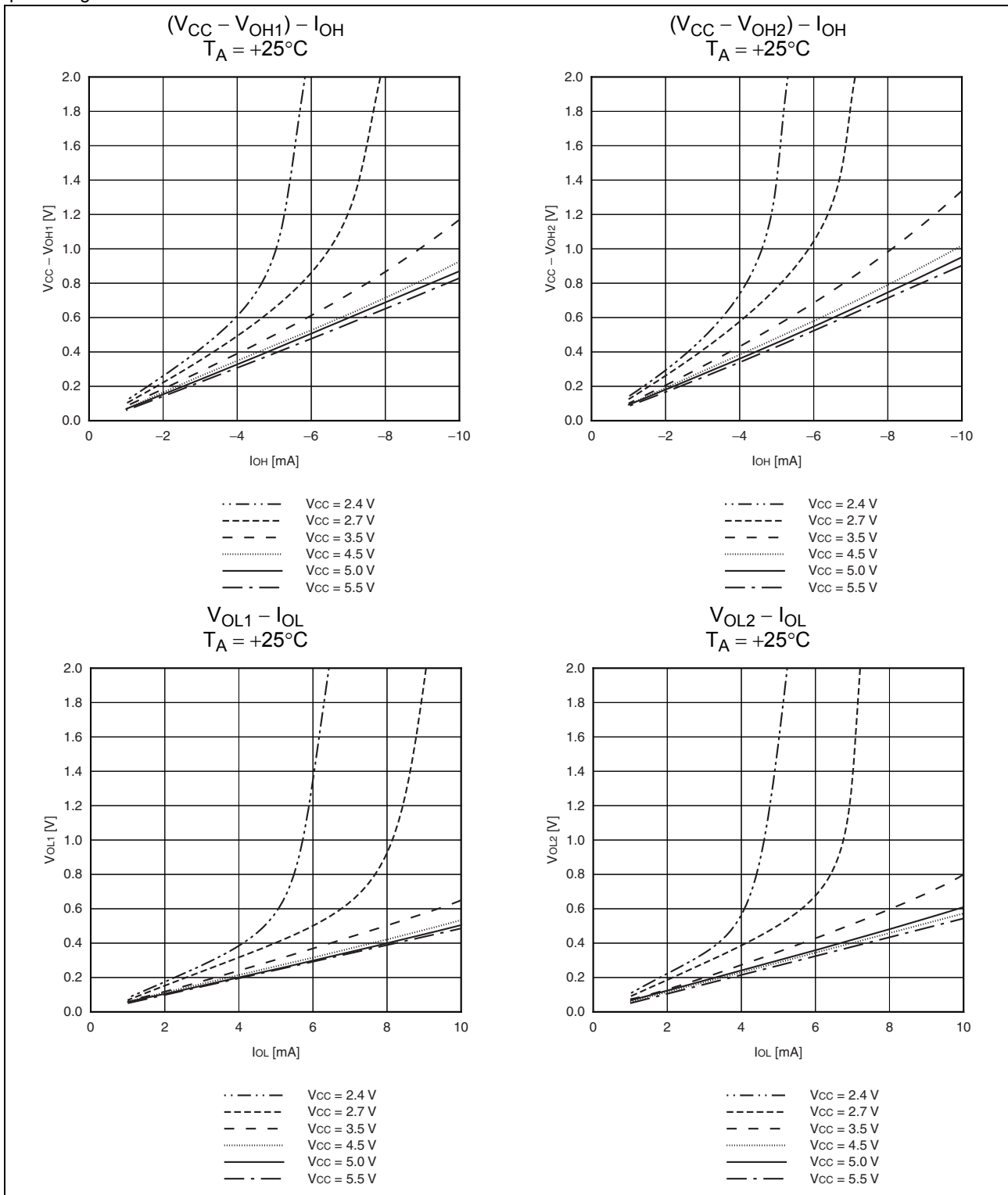
$I_{CCSCR} - T_A$   
 $V_{CC} = 5.5 \text{ V}, F_{MPL} = 50 \text{ kHz (divided by 2)}$   
 Subclock mode with the sub-CR clock operating



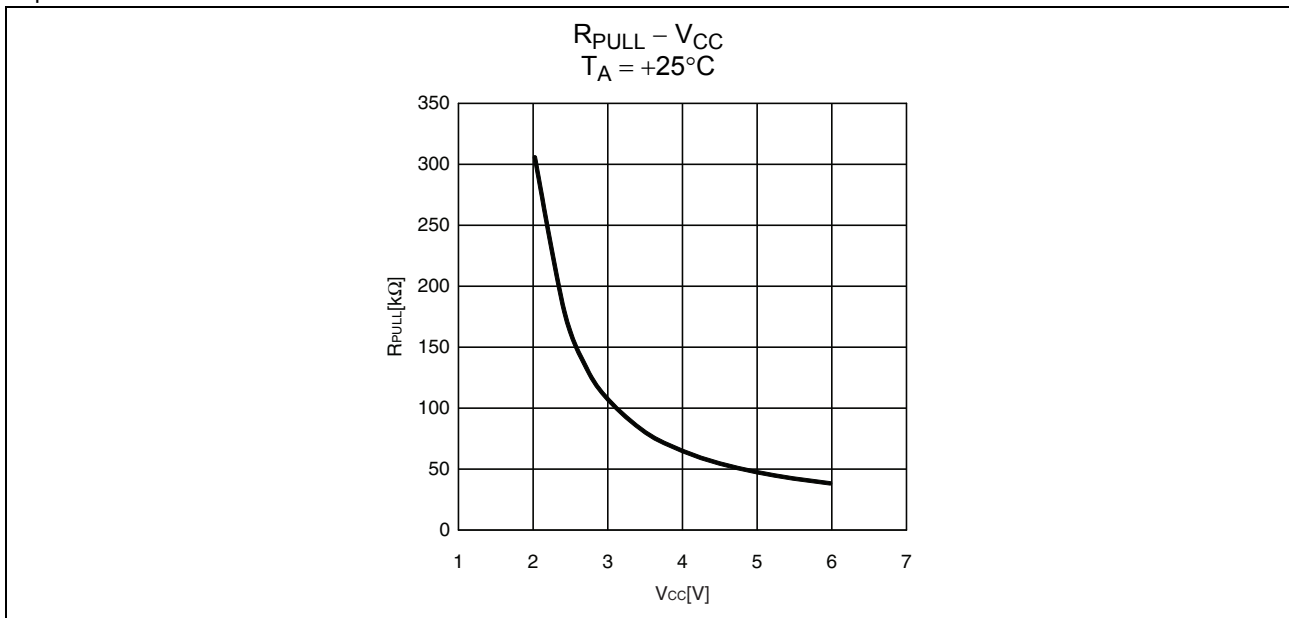
■ Input voltage characteristics



■ Output voltage characteristics



■ Pull-up characteristics



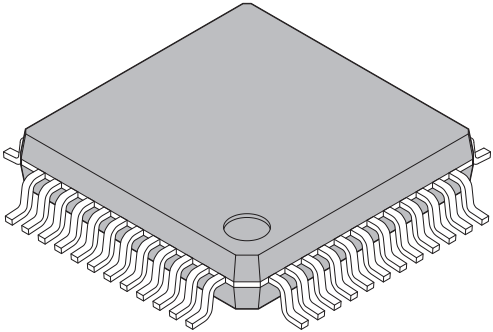
**16. Mask Options**

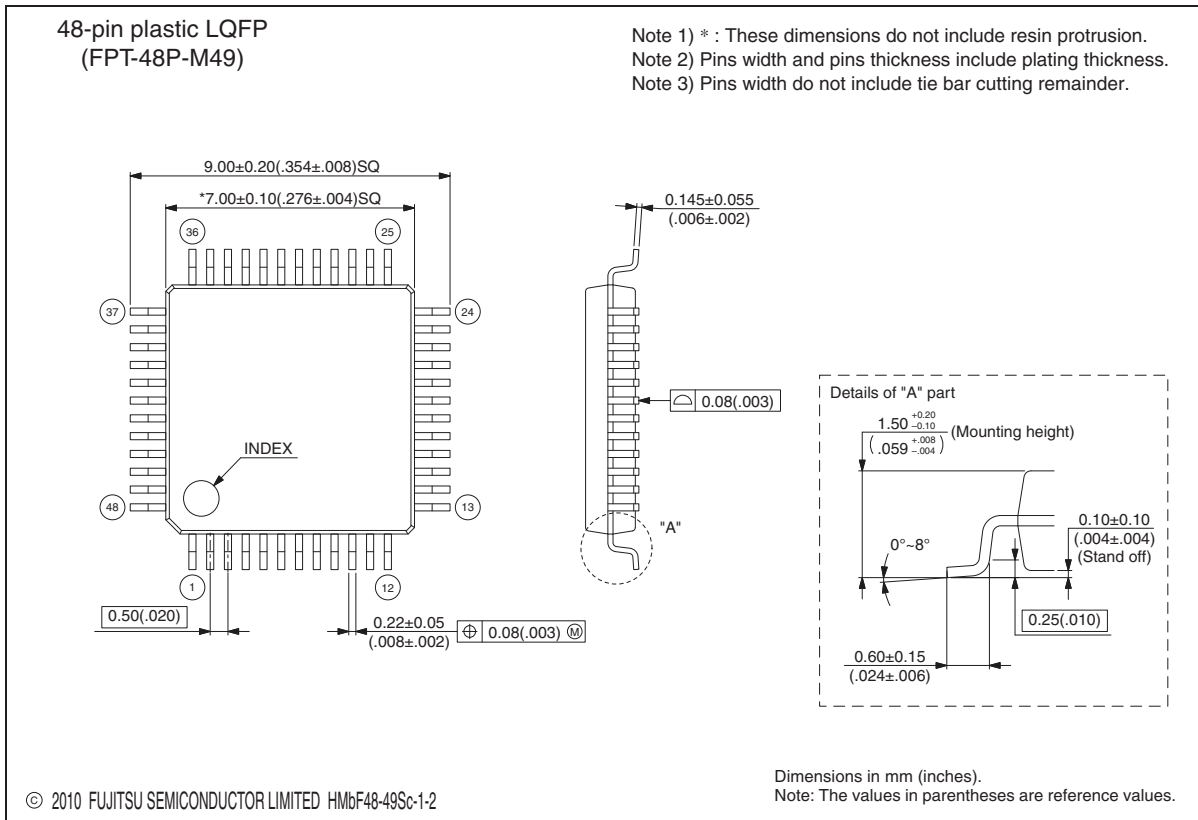
No.	Part Number	MB95F394H MB95F396H MB95F398H	MB95F394K MB95F396K MB95F398K
	Selectable/Fixed	Fixed	
1	Low-voltage detection reset	Without low-voltage detection reset	With low-voltage detection reset
2	Reset	With dedicated reset input	Without dedicated reset input

**17. Ordering Information**

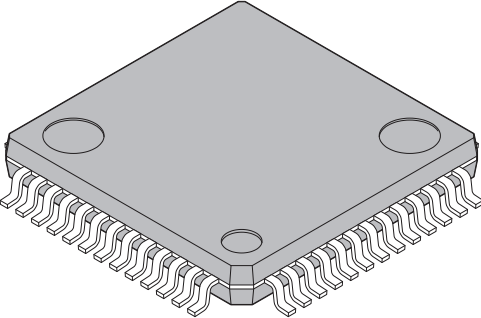
Part Number	Package
MB95F394HPMC-G-SNE2 MB95F394KPMC-G-SNE2 MB95F396HPMC-G-SNE2 MB95F396KPMC-G-SNE2 MB95F398HPMC-G-SNE2 MB95F398KPMC-G-SNE2	48-pin plastic LQFP (FPT-48P-M49)
MB95F394HPMC1-G-SNE2 MB95F394KPMC1-G-SNE2 MB95F396HPMC1-G-SNE2 MB95F396KPMC1-G-SNE2 MB95F398HPMC1-G-SNE2 MB95F398KPMC1-G-SNE2	52-pin plastic LQFP (FPT-52P-M02)
MB95F394HWQN-G-SNE1 MB95F394HWQN-G-SNERE1 MB95F394KWQN-G-SNE1 MB95F394KWQN-G-SNERE1 MB95F396HWQN-G-SNE1 MB95F396HWQN-G-SNERE1 MB95F396KWQN-G-SNE1 MB95F396KWQN-G-SNERE1 MB95F398HWQN-G-SNE1 MB95F398HWQN-G-SNERE1 MB95F398KWQN-G-SNE1 MB95F398KWQN-G-SNERE1	48-pin plastic QFN (LCC-48P-M11)

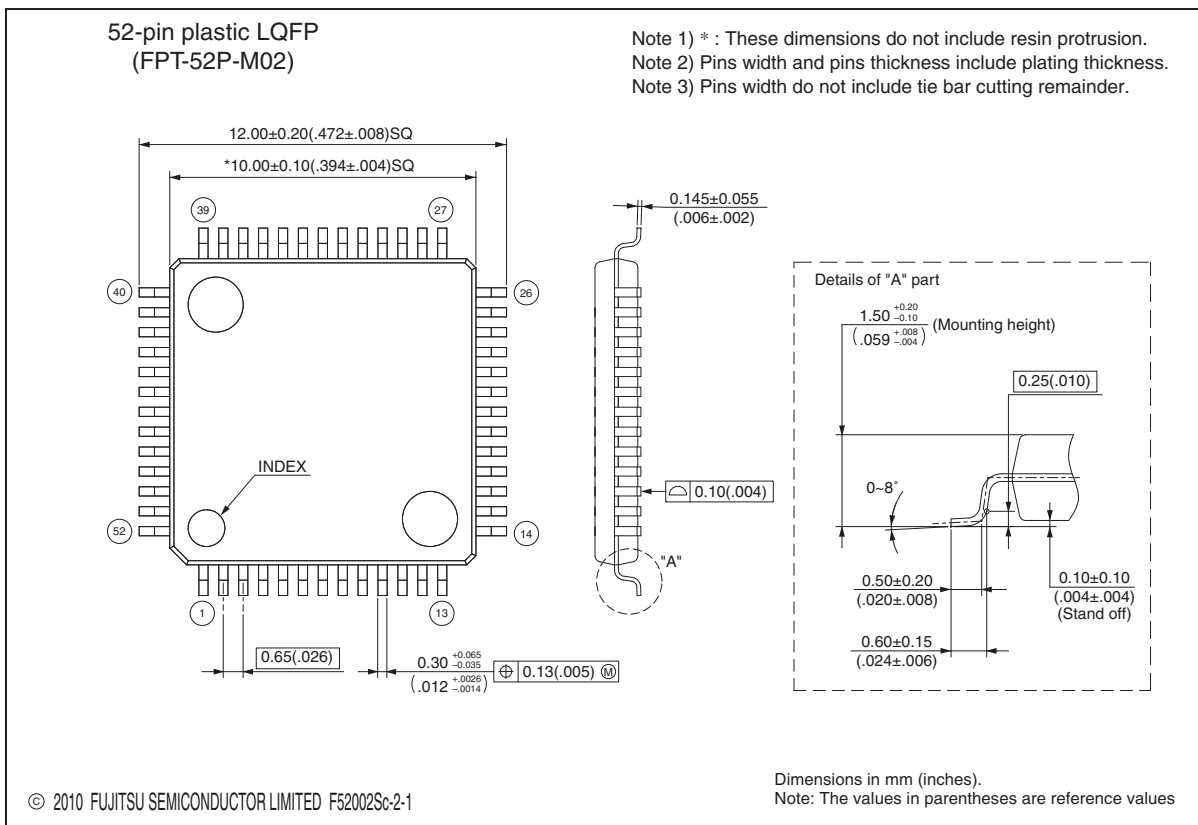
**18. Package Dimension**

<p style="text-align: center;">48-pin plastic LQFP</p>  <p style="text-align: center;">(FPT-48P-M49)</p>	Lead pitch	0.50 mm
	Package width × package length	7.00 mm × 7.00 mm
	Lead shape	Gullwing
	Lead bend direction	Normal bend
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.17 g



(Continued)

<p style="text-align: center;">52-pin plastic LQFP</p>  <p style="text-align: center;">(FPT-52P-M02)</p>	Lead pitch	0.65 mm
	Package width × package length	10.00 × 10.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.32 g
	Code (Reference)	P-LFQFP52-10×10-0.65



(Continued)



## 19. Major Changes

Page	Section	Details
1	Features	Changed the main CR clock oscillation accuracy. $\pm 2\% \rightarrow \pm 2\%$ or $\pm 2.5\%$  Added a remark about the main CR clock accuracy.
4	Product Line-up	Added FPT-52P-M02.
5	Packages And Corresponding Products	Added FPT-52P-M02.
6	Differences Among Products And Notes On Product Selection	Added a reference for the connection method in “• On-chip debug function”.
8	Pin Assignment	Added the pin assignment diagram of FPT-52P-M02.
10 to 13	Pin Functions	Added the pin numbers of FPT-52P-M02.
34	Electrical Characteristics AC Characteristics Clock Timing	Changed the values of clock frequency ( $F_{CRH}$ ).  Added conditions related to the LQFP package and the QFN package for the values of clock frequency ( $F_{CRH}$ ).  Added footnotes *2 and *3.
58 to 63	Sample Characteristics	Added “Sample Characteristics”.
65	Ordering Information	Added the part numbers of FPT-52P-M02.
67	Package Dimension	Added the package diagram of FPT-52P-M02.

**NOTE:** Please see “Document History” about later revised information.

## Document History

Document Title: MB95F394H/F396K/F398H/F394K/F396H/F398K CMOS F2MC-8FX MB95390H Series 8-bit Microcontrollers Document Number: 002-07573				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	—	AKIH	07/27/2010	Migrated to Cypress and assigned document number 002-07573. No change to document contents or format.
*A	5185613	AKIH	3/31/2016	Updated to Cypress template

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