





THIS SPEC IS OBSOLETE

Spec No: 002-07513

Spec Title: MB95220H SERIES F2MC-8FX 8-BIT  
MICROCONTROLLER

Replaced by: NONE

MB95220H are a series of general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers of these series contain a variety of peripheral resources.

## Features

### F<sup>2</sup>MC-8FX CPU core

Instruction set optimized for controllers

- Multiplication and division instructions
- 16-bit arithmetic operations
- Bit test branch instructions
- Bit manipulation instructions, etc.

### Clock

- Selectable main clock source
  - External clock (up to 32.5 MHz, maximum machine clock frequency: 16.25 MHz)
  - Main internal CR clock (1/8/10 MHz ±3%, maximum machine clock frequency: 10 MHz)
- Selectable subclock source
  - External clock (32.768 kHz)
  - Sub-internal CR clock (Typ: 100 kHz, Min: 50 kHz, Max: 200 kHz)

### Timer

- 8/16-bit composite timer
- Timebase timer
- Watch prescaler

### LIN-UART (MB95F222H/F222K/F223H/F223K)

- Full duplex double buffer
- Capable of clock-synchronized serial data transfer and clock-asynchronous serial data transfer

### External interrupt

- Interrupt by edge detection (rising edge, falling edge, and both edges can be selected)
- Can be used to wake up the device from different low power consumption (standby) modes

### 8/10-bit A/D converter

- 8-bit or 10-bit resolution can be selected.

### Low power consumption (standby) modes

- Stop mode
- Sleep mode
- Watch mode
- Timebase timer mode

### I/O port (Max: 13) (MB95F222K/F223K)

- General-purpose I/O ports (Max):  
CMOS I/O: 11, N-ch open drain: 2

### I/O port (Max: 12) (MB95F222H/F223H)

- General-purpose I/O ports (Max):  
CMOS I/O: 11, N-ch open drain: 1

### On-chip debug

- 1-wire serial control
- Serial writing supported (asynchronous mode)

### Hardware/software watchdog timer

- Built-in hardware watchdog timer

### Low-voltage detection reset circuit

- Built-in low-voltage detector

### Clock supervisor counter

- Built-in clock supervisor counter function

### Programmable port input voltage level

- CMOS input level / hysteresis input level

### Flash memory security function

- Protects the contents of flash memory

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**1. Product Line-up**

Part number	MB95F223H	MB95F222H	MB95F223K	MB95F222K
Type	Flash memory product			
Clock supervisor counter	It supervises the main clock oscillation.			
ROM capacity	8 KB	4 KB	8 KB	4 KB
RAM capacity	496 B	240 B	496 B	240 B
Low-voltage detection reset	No		Yes	
Reset input	Dedicated		Selected by software	
CPU functions	Number of basic instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8, and 16 bits Minimum instruction execution time : 61.5 ns (with machine clock = 16.25 MHz) Interrupt processing time : 0.6 μs (with machine clock = 16.25 MHz)			
General-purpose I/O	I/O ports (Max): 12 CMOS: 11, N-ch: 1		I/O ports (Max): 13 CMOS: 11, N-ch: 2	
Timebase timer	Interrupt cycle : 0.256 ms - 8.3 s (when external clock = 4 MHz)			
Hardware/software watchdog timer	Reset generation cycle Main oscillation clock at 10 MHz : 105 ms (Min) The sub-CR clock can be used as the source clock of the hardware watchdog timer.			
Wild register	It can be used to replace three bytes of data.			
LIN-UART	A wide range of communication speed can be selected by a dedicated reload timer. It has a full duplex double buffer. Clock-synchronized serial data transfer and clock-asynchronized serial data transfer is enabled. The LIN function can be used as a LIN master or a LIN slave.			
8/10-bit A/D converter	5 ch. 8-bit or 10-bit resolution can be selected.			
8/16-bit composite timer	1 ch. The timer can be configured as an "8-bit timer x 2 channels" or a "16-bit timer x 1 channel". It has built-in timer function, PWC function, PWM function and input capture function. Count clock: it can be selected from internal clocks (seven types) and external clocks. It can output square wave.			
External interrupt	6 ch. Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.) It can be used to wake up the device from standby modes.			
On-chip debug	1-wire serial control It supports serial writing. (asynchronous mode)			

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Part number	MB95F223H	MB95F222H	MB95F223K	MB95F222K
Parameter				
Watch prescaler	Eight different time intervals can be selected.			
Flash memory	It supports automatic programming, Embedded Algorithm, write/erase/erase-suspend/erase-resume commands. It has a flag indicating the completion of the operation of Embedded Algorithm. Number of write/erase cycles: 100000 Data retention time: 20 years For write/erase, external Vpp(+10 V) input is required. Flash security feature for protecting the contents of the flash			
Standby mode	Sleep mode, stop mode, watch mode, timebase timer mode			
Package	DIP-16P-M06 FPT-16P-M06			

## 2. Packages and Corresponding Products

Part number \ Package	MB95F223H	MB95F222H	MB95F223K	MB95F222K
DIP-16P-M06	○	○	○	○
FPT-16P-M06	○	○	○	○

○: Available

## 3. Differences Among Products and Notes on Product Selection

### Current consumption

When using the on-chip debug function, take account of the current consumption of flash erase/program.

For details of current consumption, see “13. Electrical Characteristics”.

### Package

For details of information on each package, see “2. Packages and Corresponding Products” and “17. Package Dimensions”.

### Operating voltage

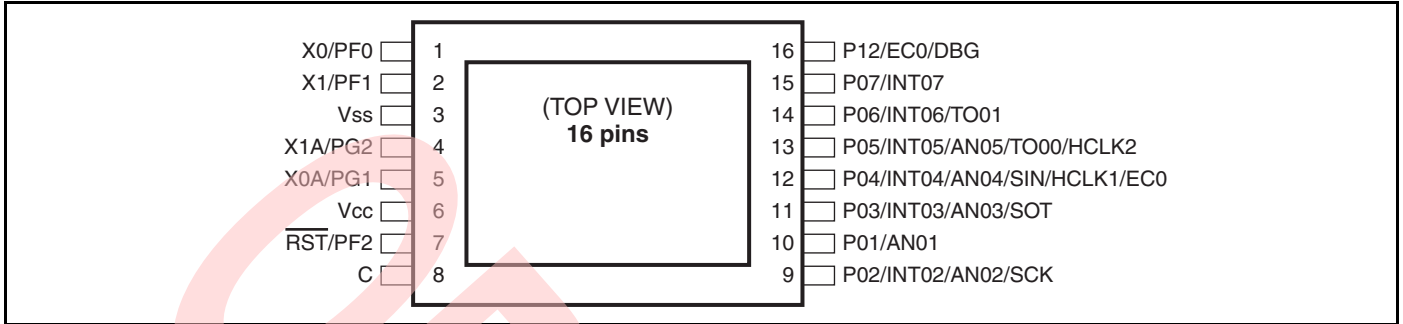
The operating voltage varies, depending on whether the on-chip debug function is used or not.

For details of the operating voltage, see “13. Electrical Characteristics”.

### On-chip debug function

The on-chip debug function requires that  $V_{CC}$ ,  $V_{SS}$  and 1 serial-wire be connected to an evaluation tool. In addition, if the flash memory data has to be updated, the RST/PF2 pin must also be connected to the same evaluation tool.

**4. Pin Assignment**



**5. Pin Description (MB95220H Series)**

Pin no.	Pin name	I/O circuit type*	Function
1	PF0	B	General-purpose I/O port
	X0		Main clock input oscillation pin
2	PF1	B	General-purpose I/O port
	X1		Main clock I/O oscillation pin
3	V <sub>SS</sub>	—	Power supply pin (GND)
4	PG2	C	General-purpose I/O port
	X1A		Subclock I/O oscillation pin
5	PG1	C	General-purpose I/O port
	X0A		Subclock input oscillation pin
6	V <sub>CC</sub>	—	Power supply pin
7	PF2	A	General-purpose I/O port
	$\overline{\text{RST}}$		Reset pin This pin is a dedicated reset pin in MB95F222H/F223H.
8	C	—	Capacitor connection pin
9	P02	E	General-purpose I/O port
	INT02		External interrupt input pin
	AN02		A/D converter analog input pin
	SCK		LIN-UART clock I/O pin
10	P01	E	General-purpose I/O port
	AN01		A/D converter analog input pin
11	P03	E	General-purpose I/O port
	INT03		External interrupt input pin
	AN03		A/D converter analog input pin
	SOT		LIN-UART data output pin
12	P04	F	General-purpose I/O port
	INT04		External interrupt input pin
	AN04		A/D converter analog input pin
	SIN		LIN-UART data input pin
	HCLK1		External clock input pin
	EC0		8/16-bit composite timer ch. 0 clock input pin

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Pin no.	Pin name	I/O circuit type*	Function
13	P05	E	General-purpose I/O port High-current port
	INT05		External interrupt input pin
	AN05		A/D converter analog input pin
	TO00		8/16-bit composite timer ch. 0 clock input pin
	HCLK2		External clock input pin
14	P06	G	General-purpose I/O port High-current port
	INT06		External interrupt input pin
	TO01		8/16-bit composite timer ch. 0 clock input pin
15	P07	G	General-purpose I/O port
	INT07		External interrupt input pin
16	P12	H	General-purpose I/O port
	EC0		8/16-bit composite timer ch. 0 clock input pin
	DBG		DBG input pin


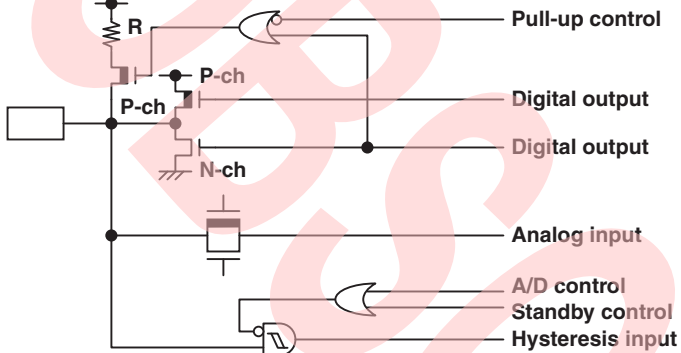
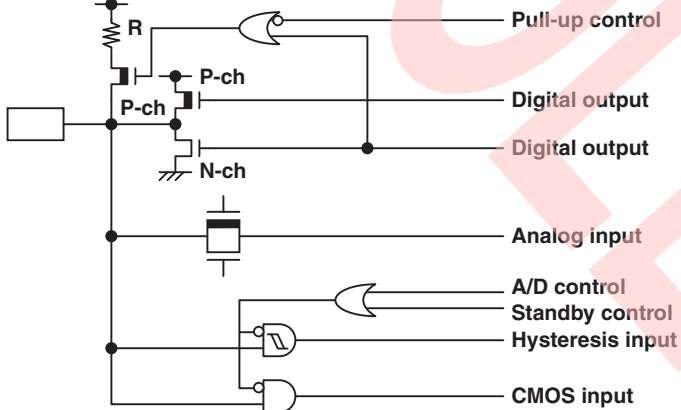
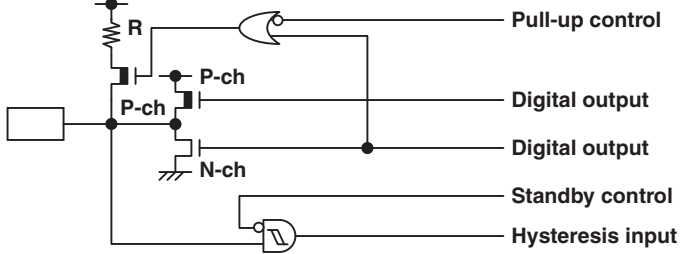
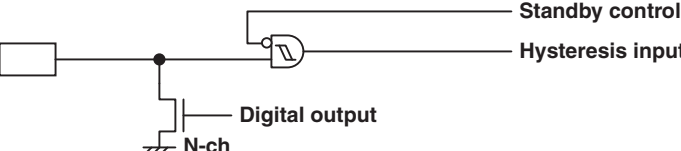
\*: For the I/O circuit types, see "6. I/O Circuit Type".

**6. I/O Circuit Type**

Type	Circuit	Remarks
A		<ul style="list-style-type: none"> <li>• N-ch open drain output</li> <li>• Hysteresis input</li> <li>• Reset output</li> </ul>
B		<ul style="list-style-type: none"> <li>• Oscillation circuit</li> <li>• High-speed side</li> <li>Feedback resistance: approx. 1 M<math>\Omega</math></li> <li>• CMOS output</li> <li>• Hysteresis input</li> </ul>
C		<ul style="list-style-type: none"> <li>• Oscillation circuit</li> <li>• Low-speed side</li> <li>Feedback resistance: approx. 10 M<math>\Omega</math></li> <li>• CMOS output</li> <li>• Hysteresis input</li> <li>• Pull-up control available</li> </ul>

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Type	Circuit	Remarks
D	 <p>Labels: P-ch, Digital output, Digital output, N-ch, Standby control, Hysteresis input</p>	<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• Hysteresis input</li> </ul>
E	 <p>Labels: Pull-up control, Digital output, Digital output, Analog input, A/D control, Standby control, Hysteresis input</p>	<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• Hysteresis input</li> <li>• Pull-up control available</li> </ul>
F	 <p>Labels: Pull-up control, Digital output, Digital output, Analog input, A/D control, Standby control, Hysteresis input, CMOS input</p>	<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• Hysteresis input</li> <li>• CMOS input</li> <li>• Pull-up control available</li> </ul>
G	 <p>Labels: Pull-up control, Digital output, Digital output, Standby control, Hysteresis input</p>	<ul style="list-style-type: none"> <li>• Hysteresis input</li> <li>• CMOS output</li> <li>• Pull-up control available</li> </ul>
H	 <p>Labels: Standby control, Hysteresis input, Digital output, N-ch</p>	<ul style="list-style-type: none"> <li>• N-ch open drain output</li> <li>• Hysteresis input</li> </ul>

## 7. Notes on Device Handling

### Preventing latch-ups

When using the device, ensure that the voltage applied does not exceed the maximum voltage rating.

In a CMOS IC, if a voltage higher than  $V_{CC}$  or a voltage lower than  $V_{SS}$  is applied to an input/output pin that is neither a medium-withstand voltage pin nor a high-withstand voltage pin, or if a voltage out of the rating range of power supply voltage mentioned in 13.1 Absolute Maximum Ratings of “Electrical Characteristics” is applied to the  $V_{CC}$  pin or the  $V_{SS}$  pin, a latch-up may occur.

When a latch-up occurs, power supply current increases significantly, which may cause a component to be thermally destroyed.

### Stabilizing supply voltage

Supply voltage must be stabilized.

A malfunction may occur when power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the  $V_{CC}$  power supply voltage.

As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in  $V_{CC}$  ripple (p-p value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard  $V_{CC}$  value, and the transient fluctuation rate does not exceed 0.1 V/ms at a momentary fluctuation such as switching the power supply.

### Notes on using the external clock

When an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from subclock mode or stop mode.

## 8. Pin Connection

### Treatment of unused pins

If an unused input pin is left unconnected, a component may be permanently damaged due to malfunctions or latch-ups. Always pull up or pull down an unused input pin through a resistor of at least 2 k $\Omega$ . Set an unused input/output pin to the output state and leave it unconnected, or set it to the input state and treat it the same as an unused input pin. If there is an unused output pin, leave it unconnected.

### Power supply pins

To reduce unnecessary electro-magnetic emission, prevent malfunctions of strobe signals due to an increase in the ground level, and conform to the total output current standard, always connect the  $V_{CC}$  pin and the  $V_{SS}$  pin to the power supply and ground outside the device. In addition, connect the current supply source to the  $V_{CC}$  pin and the  $V_{SS}$  pin with low impedance.

It is also advisable to connect a ceramic capacitor of approximately 0.1  $\mu$ F as a bypass capacitor between the  $V_{CC}$  pin and the  $V_{SS}$  pin at a location close to this device.

### DBG pin

Connect the DBG pin directly to an external pull-up resistor.

To prevent the device from unintentionally entering the debug mode due to noise, minimize the distance between the DBG pin and the  $V_{CC}$  or  $V_{SS}$  pin when designing the layout of the printed circuit board.

The DBG pin should not stay at “L” level after power-on until the reset output is released.

### $\overline{RST}$ pin

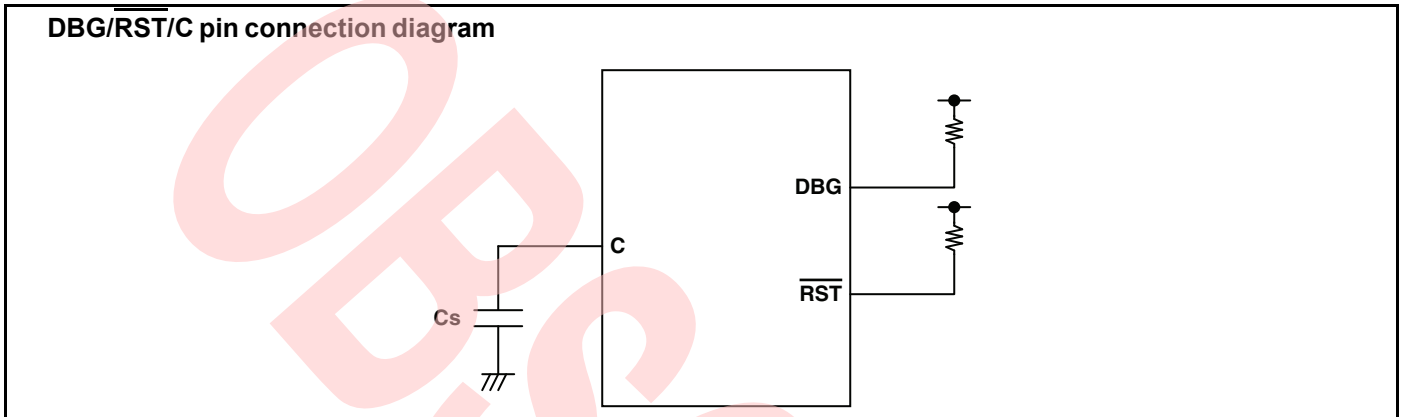
Connect the  $\overline{RST}$  pin directly to an external pull-up resistor.

To prevent the device from unintentionally entering the reset mode due to noise, minimize the distance between the  $\overline{RST}$  pin and the  $V_{CC}$  or  $V_{SS}$  pin when designing the layout of the printed circuit board.

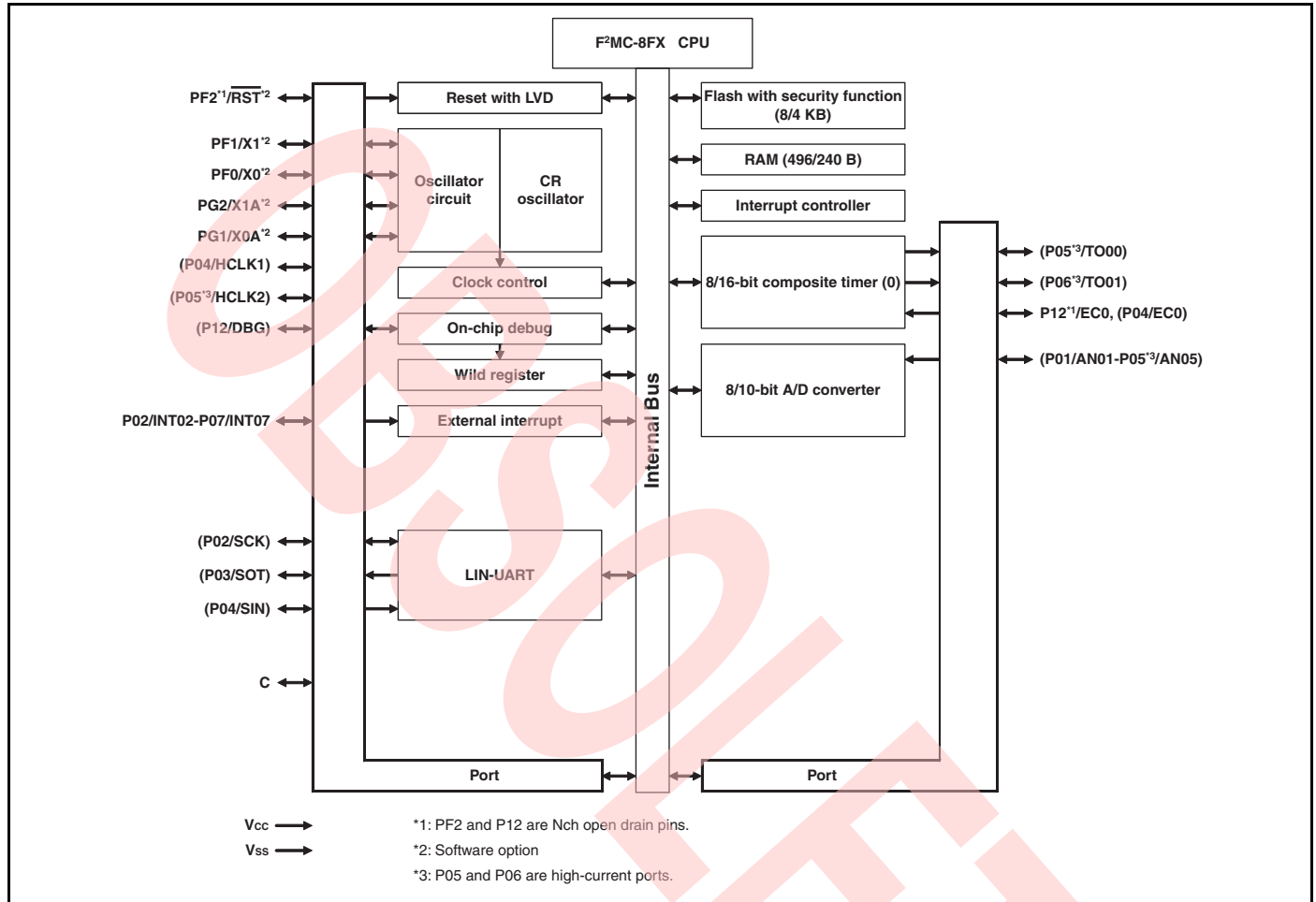
The  $\overline{RST}$ /PF2 pin functions as the reset input/output pin after power-on. In addition, the reset output of the  $\overline{RST}$ /PF2 pin can be enabled by the RSTOE bit of the SYSC register, and the reset input function and the general purpose I/O function can be selected by the RSTEN bit of the SYSC register.

**C pin**

Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The bypass capacitor for the  $V_{CC}$  pin must have a capacitance larger than  $C_S$ . For the connection to a smoothing capacitor  $C_S$ , see the diagram below. To prevent the device from unintentionally entering a mode to which the device is not set to transit due to noise, minimize the distance between the C pin and  $C_S$  and the distance between  $C_S$  and the  $V_{SS}$  pin when designing the layout of a printed circuit board.



### 9. Block Diagram (MB95220H Series)



## 10. CPU Core

### Memory Space

The memory space of the MB95220H Series is 64 KB in size, and consists of an I/O area, a data area, and a program area. The memory space includes areas intended for specific purposes such as general-purpose registers and a vector table. The memory maps of the MB95220H Series are shown below.

### Memory Maps

MB95F223H/F223K		MB95F222H/F222K	
0000 <sub>H</sub>	I/O	0000 <sub>H</sub>	I/O
0080 <sub>H</sub>	Access prohibited	0080 <sub>H</sub>	Access prohibited
0090 <sub>H</sub>	RAM 496 B	0090 <sub>H</sub>	RAM 240 B
0100 <sub>H</sub>	Register	0100 <sub>H</sub>	Register
0200 <sub>H</sub>		0180 <sub>H</sub>	Access prohibited
0280 <sub>H</sub>	Access prohibited		
0F80 <sub>H</sub>	Extension I/O	0F80 <sub>H</sub>	Extension I/O
1000 <sub>H</sub>		1000 <sub>H</sub>	
	Access prohibited		Access prohibited
E000 <sub>H</sub>	Flash 8 KB	F000 <sub>H</sub>	Flash 4 KB
FFFF <sub>H</sub>		FFFF <sub>H</sub>	

**11. I/O Map (MB95220H Series)**

Address	Register abbreviation	Register name	R/W	Initial value
0000 <sub>H</sub>	PDR0	Port 0 data register	R/W	00000000 <sub>B</sub>
0001 <sub>H</sub>	DDR0	Port 0 direction register	R/W	00000000 <sub>B</sub>
0002 <sub>H</sub>	PDR1	Port 1 data register	R/W	00000000 <sub>B</sub>
0003 <sub>H</sub>	DDR1	Port 1 direction register	R/W	00000000 <sub>B</sub>
0004 <sub>H</sub>	—	(Disabled)	—	—
0005 <sub>H</sub>	WATR	Oscillation stabilization wait time setting register	R/W	11111111 <sub>B</sub>
0006 <sub>H</sub>	—	(Disabled)	—	—
0007 <sub>H</sub>	SYCC	System clock control register	R/W	0000X011 <sub>B</sub>
0008 <sub>H</sub>	STBC	Standby control register	R/W	00000XXX <sub>B</sub>
0009 <sub>H</sub>	RSRR	Reset source register	R	XXXXXXXX <sub>B</sub>
000A <sub>H</sub>	TBTC	Timebase timer control register	R/W	00000000 <sub>B</sub>
000B <sub>H</sub>	WPCR	Watch prescaler control register	R/W	00000000 <sub>B</sub>
000C <sub>H</sub>	WDTC	Watchdog timer control register	R/W	00000000 <sub>B</sub>
000D <sub>H</sub>	SYCC2	System clock control register 2	R/W	XX100011 <sub>B</sub>
000E <sub>H</sub> to 0015 <sub>H</sub>	—	(Disabled)	—	—
0016 <sub>H</sub>	—	(Disabled)	—	—
0017 <sub>H</sub>	—	(Disabled)	—	—
0018 <sub>H</sub> to 0027 <sub>H</sub>	—	(Disabled)	—	—
0028 <sub>H</sub>	PDRF	Port F data register	R/W	00000000 <sub>B</sub>
0029 <sub>H</sub>	DDRF	Port F direction register	R/W	00000000 <sub>B</sub>
002A <sub>H</sub>	PDRG	Port G data register	R/W	00000000 <sub>B</sub>
002B <sub>H</sub>	DDRG	Port G direction register	R/W	00000000 <sub>B</sub>
002C <sub>H</sub>	PUL0	Port 0 pull-up register	R/W	00000000 <sub>B</sub>
002D <sub>H</sub> to 0034 <sub>H</sub>	—	(Disabled)	—	—
0035 <sub>H</sub>	PULG	Port G pull-up register	R/W	00000000 <sub>B</sub>
0036 <sub>H</sub>	T01CR1	8/16-bit composite timer 01 status control register 1 ch. 0	R/W	00000000 <sub>B</sub>
0037 <sub>H</sub>	T00CR1	8/16-bit composite timer 00 status control register 1 ch. 0	R/W	00000000 <sub>B</sub>
0038 <sub>H</sub>	—	(Disabled)	—	—
0039 <sub>H</sub>	—	(Disabled)	—	—
003A <sub>H</sub> to 0048 <sub>H</sub>	—	(Disabled)	—	—
0049 <sub>H</sub>	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	00000000 <sub>B</sub>

*(Continued)*

Address	Register abbreviation	Register name	R/W	Initial value
004A <sub>H</sub>	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	00000000 <sub>B</sub>
004B <sub>H</sub>	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	00000000 <sub>B</sub>
004C <sub>H</sub> to 004F <sub>H</sub>	—	(Disabled)	—	—
0050 <sub>H</sub>	SCR	LIN-UART serial control register	R/W	00000000 <sub>B</sub>
0051 <sub>H</sub>	SMR	LIN-UART serial mode register	R/W	00000000 <sub>B</sub>
0052 <sub>H</sub>	SSR	LIN-UART serial status register	R/W	00001000 <sub>B</sub>
0053 <sub>H</sub>	RDR/TDR	LIN-UART receive/transmit data register	R/W	00000000 <sub>B</sub>
0054 <sub>H</sub>	ESCR	LIN-UART extended status control register	R/W	00000100 <sub>B</sub>
0055 <sub>H</sub>	ECCR	LIN-UART extended communication control register	R/W	000000XX <sub>B</sub>
0056 <sub>H</sub> to 006B <sub>H</sub>	—	(Disabled)	—	—
006C <sub>H</sub>	ADC1	8/10-bit A/D converter control register 1	R/W	00000000 <sub>B</sub>
006D <sub>H</sub>	ADC2	8/10-bit A/D converter control register 2	R/W	00000000 <sub>B</sub>
006E <sub>H</sub>	ADDH	8/10-bit A/D converter data register (Upper)	R/W	00000000 <sub>B</sub>
006F <sub>H</sub>	ADDL	8/10-bit A/D converter data register (Lower)	R/W	00000000 <sub>B</sub>
0070 <sub>H</sub> , 0071 <sub>H</sub>	—	(Disabled)	—	—
0072 <sub>H</sub>	FSR	Flash memory status register	R/W	000X0000 <sub>B</sub>
0073 <sub>H</sub> to 0075 <sub>H</sub>	—	(Disabled)	—	—
0076 <sub>H</sub>	WREN	Wild register address compare enable register	R/W	00000000 <sub>B</sub>
0077 <sub>H</sub>	WROR	Wild register data test setting register	R/W	00000000 <sub>B</sub>
0078 <sub>H</sub>	—	Mirror of register bank pointer (RP) and direct bank pointer (DP)	—	—
0079 <sub>H</sub>	ILR0	Interrupt level setting register 0	R/W	11111111 <sub>B</sub>
007A <sub>H</sub>	ILR1	Interrupt level setting register 1	R/W	11111111 <sub>B</sub>
007B <sub>H</sub>	ILR2	Interrupt level setting register 2	R/W	11111111 <sub>B</sub>
007C <sub>H</sub>	—	(Disabled)	—	—
007D <sub>H</sub>	ILR4	Interrupt level setting register 4	R/W	11111111 <sub>B</sub>
007E <sub>H</sub>	ILR5	Interrupt level setting register 5	R/W	11111111 <sub>B</sub>
007F <sub>H</sub>	—	(Disabled)	—	—
0F80 <sub>H</sub>	WRARH0	Wild register address setting register (Upper) ch. 0	R/W	00000000 <sub>B</sub>

*(Continued)*

Address	Register abbreviation	Register name	R/W	Initial value
0F81 <sub>H</sub>	WRARL0	Wild register address setting register (Lower) ch. 0	R/W	00000000 <sub>B</sub>
0F82 <sub>H</sub>	WRDR0	Wild register data setting register ch. 0	R/W	00000000 <sub>B</sub>
0F83 <sub>H</sub>	WRARH1	Wild register address setting register (Upper) ch. 1	R/W	00000000 <sub>B</sub>
0F84 <sub>H</sub>	WRARL1	Wild register address setting register (Lower) ch. 1	R/W	00000000 <sub>B</sub>
0F85 <sub>H</sub>	WRDR1	Wild register data setting register ch. 1	R/W	00000000 <sub>B</sub>
0F86 <sub>H</sub>	WRARH2	Wild register address setting register (Upper) ch. 2	R/W	00000000 <sub>B</sub>
0F87 <sub>H</sub>	WRARL2	Wild register address setting register (Lower) ch. 2	R/W	00000000 <sub>B</sub>
0F88 <sub>H</sub>	WRDR2	Wild register data setting register ch. 2	R/W	00000000 <sub>B</sub>
0F89 <sub>H</sub> to 0F91 <sub>H</sub>	—	(Disabled)	—	—
0F92 <sub>H</sub>	T01CR0	8/16-bit composite timer 01 status control register 0 ch. 0	R/W	00000000 <sub>B</sub>
0F93 <sub>H</sub>	T00CR0	8/16-bit composite timer 00 status control register 0 ch. 0	R/W	00000000 <sub>B</sub>
0F94 <sub>H</sub>	T01DR	8/16-bit composite timer 01 data register ch. 0	R/W	00000000 <sub>B</sub>
0F95 <sub>H</sub>	T00DR	8/16-bit composite timer 00 data register ch. 0	R/W	00000000 <sub>B</sub>
0F96 <sub>H</sub>	TMCR0	8/16-bit composite timer 00/01 timer mode control register ch. 0	R/W	00000000 <sub>B</sub>
0F97 <sub>H</sub>	—	(Disabled)	—	—
0F98 <sub>H</sub>	—	(Disabled)	—	—
0F99 <sub>H</sub>	—	(Disabled)	—	—
0F9A <sub>H</sub>	—	(Disabled)	—	—
0F9B <sub>H</sub>	—	(Disabled)	—	—
0F9C <sub>H</sub> to 0FBB <sub>H</sub>	—	(Disabled)	—	—
0FBC <sub>H</sub>	BGR1	LIN-UART baud rate generator register 1	R/W	00000000 <sub>B</sub>
0FBD <sub>H</sub>	BGR0	LIN-UART baud rate generator register 0	R/W	00000000 <sub>B</sub>
0FBE <sub>H</sub> to 0FC2 <sub>H</sub>	—	(Disabled)	—	—
0FC3 <sub>H</sub>	AIDRL	A/D input disable register (Lower)	R/W	00000000 <sub>B</sub>
0FC4 <sub>H</sub> to 0FE3 <sub>H</sub>	—	(Disabled)	—	—
0FE4 <sub>H</sub>	CRTH	Main CR clock trimming register (Upper)	R/W	1XXXXXXX <sub>B</sub>
0FE5 <sub>H</sub>	CRTL	Main CR clock trimming register (Lower)	R/W	000XXXXX <sub>B</sub>

*(Continued)*

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0FE6 <sub>H</sub> , 0FE7 <sub>H</sub>	—	(Disabled)	—	—
0FE8 <sub>H</sub>	SYSC	System configuration register	R/W	11000011 <sub>B</sub>
0FE9 <sub>H</sub>	CMCR	Clock monitoring control register	R/W	00000000 <sub>B</sub>
0FEA <sub>H</sub>	CMDR	Clock monitoring data register	R/W	00000000 <sub>B</sub>
0FEB <sub>H</sub>	WDTH	Watchdog timer selection ID register (Upper)	R/W	XXXXXXXX <sub>B</sub>
0FEC <sub>H</sub>	WDTL	Watchdog timer selection ID register (Lower)	R/W	XXXXXXXX <sub>B</sub>
0FED <sub>H</sub>	—	(Disabled)	—	—
0FEE <sub>H</sub>	ILSR	Input level select register	R/W	00000000 <sub>B</sub>
0FEF <sub>H</sub> to 0FFF <sub>H</sub>	—	(Disabled)	—	—

**R/W access symbols**

R/W : Readable / Writable  
 R : Read only  
 W : Write only

**Initial value symbols**

0 : The initial value of this bit is "0".  
 1 : The initial value of this bit is "1".  
 X : The initial value of this bit is undefined.

Note: Do not write to an address that is "(Disabled)". If a "(Disabled)" address is read, an undefined value is returned.

**12. Interrupt Source Table (MB95220H Series)**

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower		
External interrupt ch. 4	IRQ0	FFFA <sub>H</sub>	FFFB <sub>H</sub>	L00 [1:0]	<div style="text-align: center;">High</div> <div style="text-align: center;">↑</div> <div style="text-align: center;">↓</div> <div style="text-align: center;">Low</div>
External interrupt ch. 5	IRQ1	FFF8 <sub>H</sub>	FFF9 <sub>H</sub>	L01 [1:0]	
External interrupt ch. 2	IRQ2	FFF6 <sub>H</sub>	FFF7 <sub>H</sub>	L02 [1:0]	
External interrupt ch. 6					
External interrupt ch. 3	IRQ3	FFF4 <sub>H</sub>	FFF5 <sub>H</sub>	L03 [1:0]	
External interrupt ch. 7					
—	IRQ4	FFF2 <sub>H</sub>	FFF3 <sub>H</sub>	L04 [1:0]	
8/16-bit composite timer ch. 0 (Lower)	IRQ5	FFF0 <sub>H</sub>	FFF1 <sub>H</sub>	L05 [1:0]	
8/16-bit composite timer ch. 0 (Upper)	IRQ6	FFEE <sub>H</sub>	FFEF <sub>H</sub>	L06 [1:0]	
LIN-UART (reception)	IRQ7	FFEC <sub>H</sub>	FFED <sub>H</sub>	L07 [1:0]	
LIN-UART (transmission)	IRQ8	FFEA <sub>H</sub>	FFEB <sub>H</sub>	L08 [1:0]	
—	IRQ9	FFE8 <sub>H</sub>	FFE9 <sub>H</sub>	L09 [1:0]	
—	IRQ10	FFE6 <sub>H</sub>	FFE7 <sub>H</sub>	L10 [1:0]	
—	IRQ11	FFE4 <sub>H</sub>	FFE5 <sub>H</sub>	L11 [1:0]	
—	IRQ12	FFE2 <sub>H</sub>	FFE3 <sub>H</sub>	L12 [1:0]	
—	IRQ13	FFE0 <sub>H</sub>	FFE1 <sub>H</sub>	L13 [1:0]	
—	IRQ14	FFDE <sub>H</sub>	FFDF <sub>H</sub>	L14 [1:0]	
—	IRQ15	FFDC <sub>H</sub>	FFDD <sub>H</sub>	L15 [1:0]	
—	IRQ16	FFDA <sub>H</sub>	FFDB <sub>H</sub>	L16 [1:0]	
—	IRQ17	FFD8 <sub>H</sub>	FFD9 <sub>H</sub>	L17 [1:0]	
8/10-bit A/D converter	IRQ18	FFD6 <sub>H</sub>	FFD7 <sub>H</sub>	L18 [1:0]	
Timebase timer	IRQ19	FFD4 <sub>H</sub>	FFD5 <sub>H</sub>	L19 [1:0]	
Watch prescaler	IRQ20	FFD2 <sub>H</sub>	FFD3 <sub>H</sub>	L20 [1:0]	
—	IRQ21	FFD0 <sub>H</sub>	FFD1 <sub>H</sub>	L21 [1:0]	
—	IRQ22	FFCE <sub>H</sub>	FFCF <sub>H</sub>	L22 [1:0]	
Flash memory	IRQ23	FFCC <sub>H</sub>	FFCD <sub>H</sub>	L23 [1:0]	

### 13. Electrical Characteristics

#### 13.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage* <sup>1</sup>	$V_{CC}$	$V_{SS}-0.3$	$V_{SS} + 6$	V	
Input voltage* <sup>1</sup>	$V_{I1}$	$V_{SS}-0.3$	$V_{CC} + 0.3$	V	Other than PF2* <sup>2</sup>
	$V_{I2}$	$V_{SS}-0.3$	10.5	V	PF2
Output voltage* <sup>1</sup>	$V_O$	$V_{SS}-0.3$	$V_{SS} + 6$	V	*2
Maximum clamp current	$I_{CLAMP}$	-2	+ 2	mA	Applicable to specific pins * <sup>3</sup>
Total maximum clamp current	$S I_{CLAMP} $	—	20	mA	Applicable to specific pins * <sup>3</sup>
“L” level maximum output current	$I_{OL1}$	—	15	mA	Other than P05, P06
	$I_{OL2}$	—	15		P05, P06
“L” level average current	$I_{OLAV1}$	—	4	mA	Other than P05, P06 Average output current = operating current × operating ratio (1 pin)
	$I_{OLAV2}$	—	12		P05, P06 Average output current = operating current × operating ratio (1 pin)
“L” level total maximum output current	$S I_{OL}$	—	100	mA	
“L” level total average output current	$S I_{OLAV}$	—	50	mA	Total average output current = operating current × operating ratio (Total number of pins)
“H” level maximum output current	$I_{OH1}$	—	-15	mA	Other than P05, P06
	$I_{OH2}$	—	-15		P05, P06
“H” level average current	$I_{OHAV1}$	—	-4	mA	Other than P05, P06 Average output current = operating current × operating ratio (1 pin)
	$I_{OHAV2}$	—	-8		P05, P06 Average output current = operating current × operating ratio (1 pin)
“H” level total maximum output current	$S I_{OH}$	—	-100	mA	
“H” level total average output current	$S I_{OHAV}$	—	-50	mA	Total average output current = operating current × operating ratio (Total number of pins)
Power consumption	$P_d$	—	320	mW	
Operating temperature	$T_A$	-40	+ 85	°C	
Storage temperature	$T_{stg}$	-55	+ 150	°C	

(Continued)

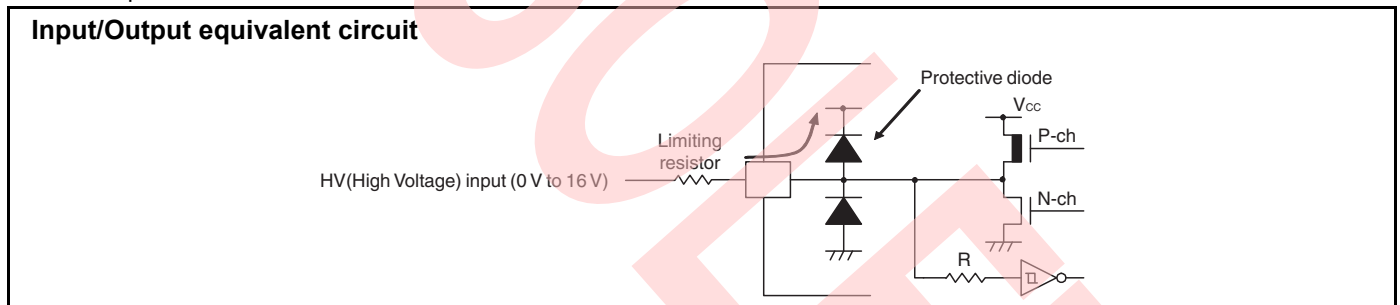
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\*1: The parameter is based on  $V_{SS} = 0.0\text{ V}$ .

\*2:  $V_I$  and  $V_O$  must not exceed  $V_{CC} + 0.3\text{ V}$ .  $V_I$  must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the  $I_{CLAMP}$  rating is used instead of the  $V_I$  rating.

\*3: Applicable to the following pins: P01 to P07, PG1, PG2, PF0, PF1

- Use under recommended operating conditions.
- Use with DC voltage (current).
- The HV (High Voltage) signal is an input signal exceeding the  $V_{CC}$  voltage. Always connect a limiting resistor between the HV (High Voltage) signal and the microcontroller before applying the HV (High Voltage) signal.
- The value of the limiting resistor should be set to a value at which the current to be input to the microcontroller pin when the HV (High Voltage) signal is input is below the standard value, irrespective of whether the current is transient current or stationary current.
- When the microcontroller drive current is low, such as in low power consumption modes, the HV (High Voltage) input potential may pass through the protective diode to increase the potential of the  $V_{CC}$  pin, affecting other devices.
- If the HV (High Voltage) signal is input when the microcontroller power supply is off (not fixed at 0 V), since power is supplied from the pins, incomplete operations may be executed.
- If the HV (High Voltage) input is input after power-on, since power is supplied from the pins, the voltage of power supply may not be sufficient to enable a power-on reset.
- Do not leave the HV (High Voltage) input pin unconnected.
- Example of a recommended circuit:



**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

**13.2 Recommended Operating Conditions**

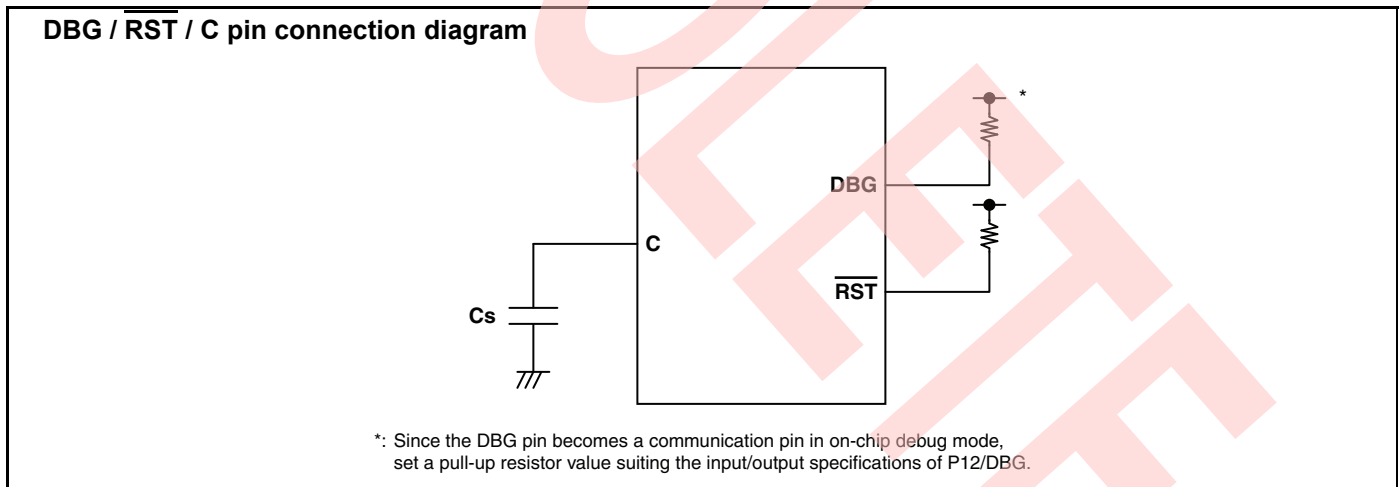
 (V<sub>SS</sub> = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks	
		Min	Max			
Power supply voltage	V <sub>CC</sub>	2.4*1*2	5.5*1	V	In normal operation	Other than on-chip debug mode
		2.3	5.5		Hold condition in stop mode	
		2.9	5.5		In normal operation	On-chip debug mode
		2.3	5.5		Hold condition in stop mode	
Smoothing capacitor	C <sub>S</sub>	0.022	1	μF	*3	
Operating temperature	T <sub>A</sub>	-40	+85	°C	Other than on-chip debug mode	
		+5	+35		On-chip debug mode	

\*1: The value varies depending on the operating frequency, the machine clock and the analog guaranteed range.

\*2: The value is 2.88 V when the low-voltage detection reset is used.

\*3: Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The bypass capacitor for the V<sub>CC</sub> pin must have a capacitance larger than C<sub>S</sub>. For the connection to a smoothing capacitor C<sub>S</sub>, see the diagram below. To prevent the device from unintentionally entering an unknown mode due to noise, minimize the distance between the C pin and C<sub>S</sub> and the distance between C<sub>S</sub> and the V<sub>SS</sub> pin when designing the layout of a printed circuit board.



**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges. Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

**13.3 DC Characteristics**
 $(V_{CC} = 5.0 V \pm 10\%, V_{SS} = 0.0 V, T_A = -40^\circ C \text{ to } +85^\circ C)$ 

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	$V_{IHI}$	P04	*1	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	When CMOS input level (hysteresis input) is selected
	$V_{IHS}$	P01 to P07, P12, PF0, PF1, PG1, PG2	*1	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Hysteresis input
	$V_{IHM}$	PF2	—	$0.7 V_{CC}$	—	10.5	V	Hysteresis input* <sup>3</sup>
"L" level input voltage	$V_{IL}$	P04	*1	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	When CMOS input level (hysteresis input) is selected
	$V_{ILS}$	P01 to P07, P12, PF0, PF1, PG1, PG2	*1	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	Hysteresis input
	$V_{ILM}$	PF2	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	Hysteresis input
Open-drain output application voltage	$V_D$	PF2, P12	—	$V_{SS} - 0.3$	—	$V_{SS} + 5.5$	V	
"H" level output voltage	$V_{OH1}$	Output pins other than P05, P06, P12, PF2	$I_{OH} = -4 \text{ mA}$	$V_{CC} - 0.5$	—	—	V	
	$V_{OH2}$	P05, P06	$I_{OH} = -8 \text{ mA}$	$V_{CC} - 0.5$	—	—	V	
"L" level output voltage	$V_{OL1}$	Output pins other than P05, P06	$I_{OL} = 4 \text{ mA}$	—	—	0.4	V	
	$V_{OL2}$	P05, P06	$I_{OL} = 12 \text{ mA}$	—	—	0.4	V	
Input leak current (Hi-Z output leak current)	$I_{LI}$	All input pins	$0.0 V < V_I < V_{CC}$	-5	—	+5	$\mu A$	When pull-up resistance is disabled
Pull-up resistance	$R_{PULL}$	P01 to P07, PG1, PG2	$V_I = 0 V$	25	50	100	k $\Omega$	When pull-up resistance is enabled
Input capacitance	$C_{IN}$	Other than $V_{CC}$ and $V_{SS}$	$f = 1 \text{ MHz}$	—	5	15	pF	

*(Continued)*

$(V_{CC} = 5.0\text{ V} \pm 10\%, V_{SS} = 0.0\text{ V}, T_A = -40^\circ\text{C to } +85^\circ\text{C})$ 

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*2	I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V F <sub>CH</sub> = 32 MHz F <sub>MP</sub> = 16 MHz Main clock mode (divided by 2)	—	13	17	mA	Flash memory product (except writing and erasing)
			—	33.5	39.5	mA	Flash memory product (at writing and erasing)	
			—	15	21	mA	At A/D conversion	
	I <sub>CCS</sub>		V <sub>CC</sub> = 5.5 V F <sub>CH</sub> = 32 MHz F <sub>MP</sub> = 16 MHz Main sleep mode (divided by 2)	—	5.5	9	mA	
	I <sub>CCL</sub>	V <sub>CC</sub> (External clock operation)	V <sub>CC</sub> = 5.5 V F <sub>CL</sub> = 32 kHz F <sub>MPL</sub> = 16 kHz Subclock mode (divided by 2) T <sub>A</sub> = +25°C	—	65	153	μA	
	I <sub>CCLS</sub>		V <sub>CC</sub> = 5.5 V F <sub>CL</sub> = 32 kHz F <sub>MPL</sub> = 16 kHz Subsleep mode (divided by 2) T <sub>A</sub> = +25°C	—	10	84	μA	
	I <sub>CCT</sub>		V <sub>CC</sub> = 5.5 V F <sub>CL</sub> = 32 kHz Watch mode Main stop mode T <sub>A</sub> = +25°C	—	5	30	μA	
	I <sub>CCMCR</sub>	V <sub>CC</sub>	V <sub>CC</sub> = 5.5 V F <sub>CRH</sub> = 10 MHz F <sub>MP</sub> = 10 MHz Main CR clock mode	—	8.6	—	mA	
I <sub>CCSCR</sub>	V <sub>CC</sub> = 5.5 V Sub-CR clock mode (divided by 2) T <sub>A</sub> = +25°C		—	110	410	μA		

*(Continued)*

(Continued)

 ( $V_{CC} = 5.0\text{ V} \pm 10\%$ ,  $V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*2	$I_{CCTS}$	$V_{CC}$ (External clock operation)	$V_{CC} = 5.5\text{ V}$ $F_{CH} = 32\text{ MHz}$ Timebase timer mode $T_A = +25^\circ\text{C}$	—	1.1	3	mA	
	$I_{CCH}$		$V_{CC} = 5.5\text{ V}$ Substop mode $T_A = +25^\circ\text{C}$	—	3.5	22.5	$\mu\text{A}$	Main stop mode for single clock selection
	$I_{LVD}$	$V_{CC}$	Current consumption for low-voltage detection circuit only	—	37	54	$\mu\text{A}$	
	$I_{CRH}$		Current consumption for the internal main CR oscillator	—	0.5	0.6	mA	
	$I_{CRL}$		Current consumption for the internal sub-CR oscillator oscillating at 100 kHz	—	20	72	$\mu\text{A}$	

\*1: The input level of P04 can be switched between “CMOS input level” and “hysteresis input level”. The input level selection register (ILSR) is used to switch between the two input levels.

\*2: • The power supply current is determined by the external clock. When the low-voltage detection option is selected, the power-supply current will be the sum of adding the current consumption of the low-voltage detection circuit ( $I_{LVD}$ ) to one of the value from  $I_{CC}$  to  $I_{CCH}$ . In addition, when both the low-voltage detection option and the CR oscillator are selected, the power supply current will be the sum of adding up the current consumption of the low-voltage detection circuit, the current consumption of the CR oscillators ( $I_{CRH}$ ,  $I_{CRL}$ ) and a specified value. In on-chip debug mode, the CR oscillator ( $I_{CRH}$ ) and the low-voltage detection circuit are always enabled, and current consumption therefore increases accordingly.

• See “13.4. AC Characteristics: 13.4.1. Clock Timing” for  $F_{CH}$  and  $F_{CL}$ .

• See “13.4. AC Characteristics: 13.4.2. Source Clock/Machine Clock” for  $F_{MP}$  and  $F_{MPL}$ .

\*3: PF2 act as high voltage supply for the flash memory during program and erase. It can tolerate high voltage input. For details, see section “13.6. Flash Memory Program/Erase Characteristics”.

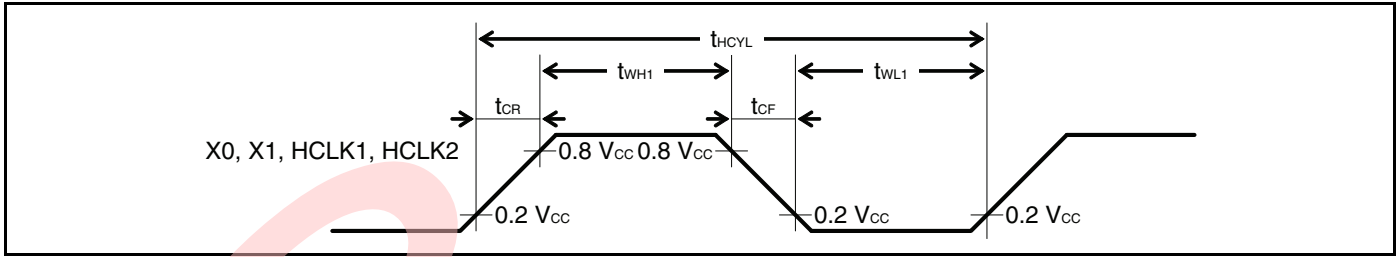
**13.4 AC Characteristics**
**13.4.1 Clock Timing**
 $(V_{CC} = 2.4\text{ V to } 5.5\text{ V}, V_{SS} = 0.0\text{ V}, T_A = -40^\circ\text{C to } +85^\circ\text{C})$ 

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks	
				Min	Typ	Max			
Clock frequency	$F_{CH}$	X0, X1	—	1	—	16.25	MHz	When the main oscillation circuit is used	
		X0, HCLK1, HCLK2	X1 open	1	—	12	MHz	When the main external clock is used	
		X0, X1, HCLK1, HCLK2	—	1	—	32.5	MHz		
	$F_{CRH}$	—	—	—	9.7	10	10.3	MHz	When the main CR clock is used $2.4\text{ V} \leq V_{CC} < 5.5\text{ V} (0^\circ\text{C} \leq T_A \leq 40^\circ\text{C})$
					7.76	8	8.24	MHz	
					0.97	1	1.03	MHz	
					9.5	10	10.5	MHz	When the main CR clock is used $2.4\text{ V} \leq V_{CC} < 5.5\text{ V} (-40^\circ\text{C} \leq T_A < 0^\circ\text{C}, 40^\circ\text{C} < T_A \leq 85^\circ\text{C})$
					7.6	8	8.4	MHz	
					0.95	1	1.05	MHz	
	$F_{CL}$	X0A, X1A	—	—	—	32.768	—	kHz	When the sub oscillation circuit is used
—					32.768	—	kHz	When the sub-external clock is used	
$F_{CRL}$	—	—	—	50	100	200	kHz	When the sub-CR clock is used	
Clock cycle time	$t_{HCYL}$	X0, X1	—	61.5	—	1000	ns	When the main oscillation circuit is used	
		X0, HCLK1, HCLK2	X1 open	83.4	—	1000	ns	When the external clock is used	
		X0, X1, HCLK1, HCLK2	—	30.8	—	1000	ns		
	$t_{LCYL}$	X0A, X1A	—	—	30.5	—	$\mu\text{s}$	When the subclock is used	

*(Continued)*

*(Continued)*
 $(V_{CC} = 2.4 \text{ V to } 5.5 \text{ V}, V_{SS} = 0.0 \text{ V}, T_A = -40^\circ\text{C to } +85^\circ\text{C})$ 

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input clock pulse width	$t_{WH1}$	X0, HCLK1, HCLK2	X1 open	33.4	—	—	ns	When the external clock is used, the duty ratio should range between 40% and 60%.
	$t_{WL1}$	X0, X1, HCLK1, HCLK2	—	12.4	—	—	ns	
	$t_{WH2}$ $t_{WL2}$	X0A	—	—	15.2	—	$\mu\text{s}$	
Input clock rise time and fall time	$t_{CR}$	X0, HCLK1, HCLK2	X1 open	—	—	5	ns	When the external clock is used
	$t_{CF}$	X0, X1, HCLK1, HCLK2	—	—	—	5	ns	
CR oscillation start time	$t_{CRHWK}$	—	—	—	—	80	$\mu\text{s}$	When the main CR clock is used
	$t_{CRLWK}$	—	—	—	—	10	$\mu\text{s}$	When the sub-CR clock is used



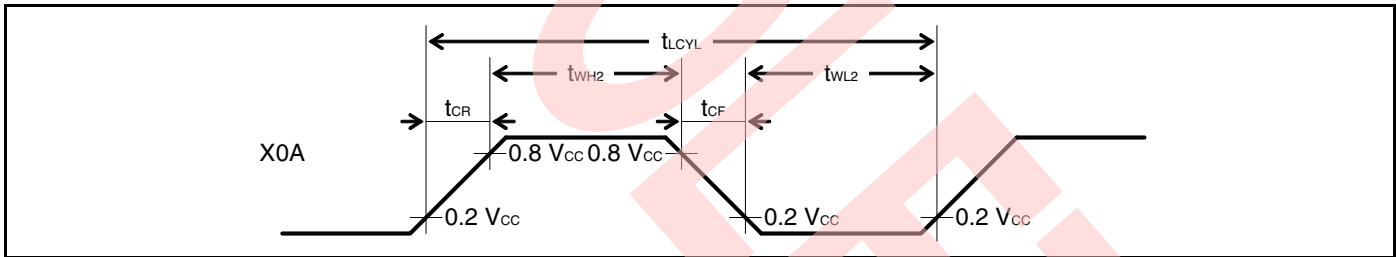
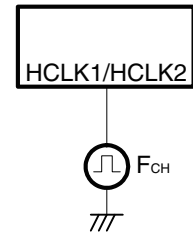
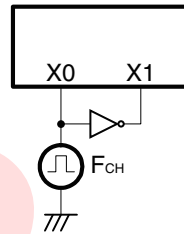
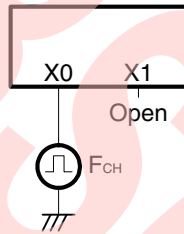
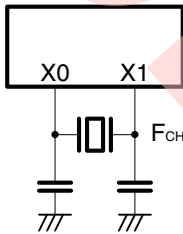
**Figure of main clock input port external connection**

When a crystal oscillator or a ceramic oscillator is used

When the external clock is used (X1 is open)

When the external clock is used

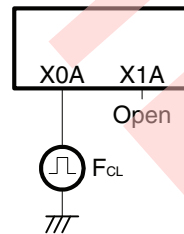
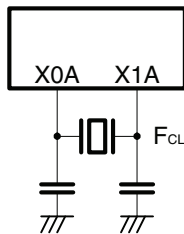
When the external clock is used



**Figure of subclock input port external connection**

When a crystal oscillator or a ceramic oscillator is used

When the external clock is used



**13.4.2 Source Clock/Machine Clock**
 $(V_{CC} = 5.0 V \pm 10\%, V_{SS} = 0.0 V, T_A = -40^\circ C \text{ to } +85^\circ C)$ 

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Source clock cycle time*1	$t_{SCLK}$	—	61.5	—	2000	ns	When the main external clock is used Min: $F_{CH} = 32.5$ MHz, divided by 2 Max: $F_{CH} = 1$ MHz, divided by 2
			100	—	1000	ns	When the main CR clock is used Min: $F_{CRH} = 10$ MHz Max: $F_{CRH} = 1$ MHz
			—	61	—	$\mu s$	When the sub-CR clock is used $F_{CL} = 32.768$ kHz, divided by 2
			—	20	—	$\mu s$	When the sub-oscillation clock is used $F_{CRL} = 100$ kHz, divided by 2
Source clock frequency	$F_{SP}$	—	0.5	—	16.25	MHz	When the main oscillation clock is used
			1	—	10	MHz	When the main CR clock is used
	$F_{SPL}$	—	—	16.384	—	kHz	When the sub-oscillation clock is used
			—	50	—	kHz	When the sub-CR clock is used $F_{CRL} = 100$ kHz, divided by 2
Machine clock cycle time*2 (minimum instruction execution time)	$t_{MCLK}$	—	61.5	—	32000	ns	When the main oscillation clock is used Min: $F_{SP} = 16.25$ MHz, no division Max: $F_{SP} = 0.5$ MHz, divided by 16
			100	—	16000	ns	When the main CR clock is used Min: $F_{SP} = 10$ MHz Max: $F_{SP} = 1$ MHz, divided by 16
			61	—	976.5	$\mu s$	When the sub-oscillation clock is used Min: $F_{SPL} = 16.384$ kHz, no division Max: $F_{SPL} = 16.384$ kHz, divided by 16
			20	—	320	$\mu s$	When the sub-CR clock is used Min: $F_{SPL} = 50$ kHz, no division Max: $F_{SPL} = 50$ kHz, divided by 16
Machine clock frequency	$F_{MP}$	—	0.031	—	16.25	MHz	When the main oscillation clock is used
			0.0625	—	10	MHz	When the main CR clock is used
	$F_{MPL}$	—	1.024	—	16.384	kHz	When the sub-oscillation clock is used
			3.125	—	50	kHz	When the sub-CR clock is used $F_{CRL} = 100$ kHz

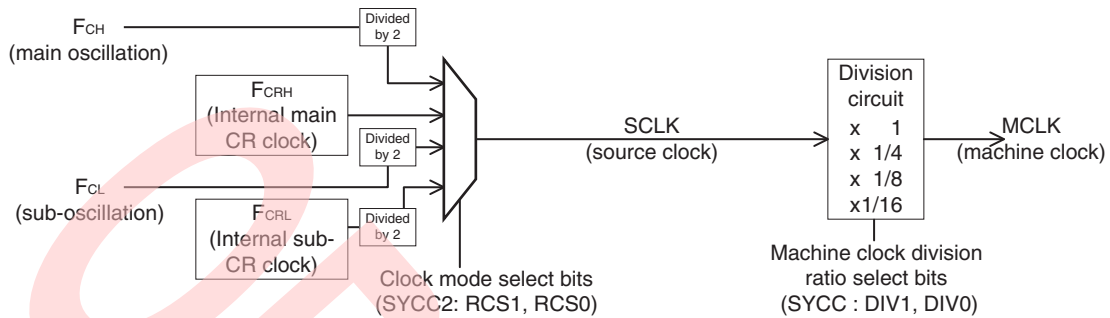
\*1: This is the clock before it is divided according to the division ratio set by the machine clock division ratio selection bits (SYCC : DIV1 and DIV0) . This source clock is divided to become a machine clock according to the division ratio set by the machine clock division ratio selection bits (SYCC : DIV1 and DIV0) . In addition, a source clock can be selected from the following.

- Main clock divided by 2
- Main CR clock
- Subclock divided by 2
- Sub-CR clock divided by 2

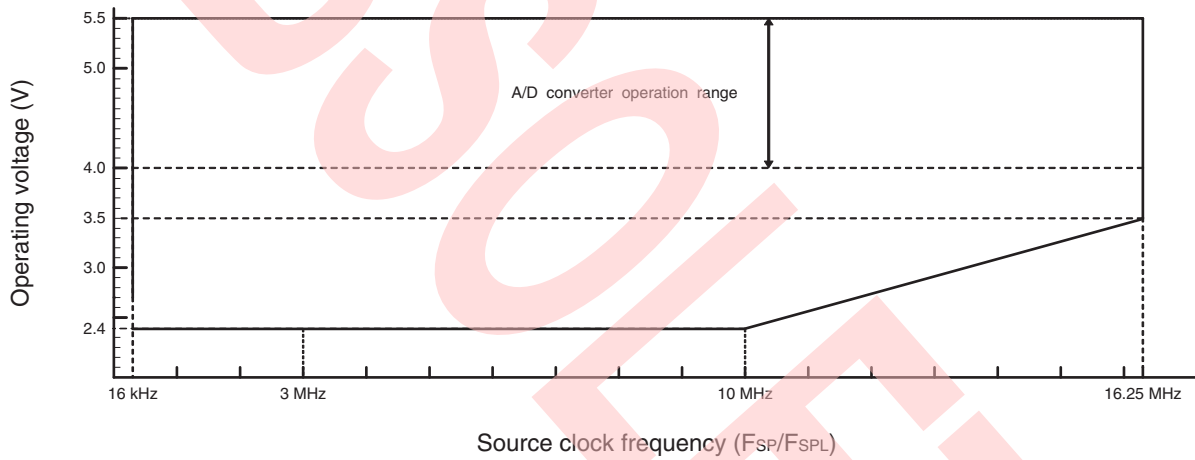
\*2: This is the operating clock of the microcontroller. A machine clock can be selected from the following.

- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

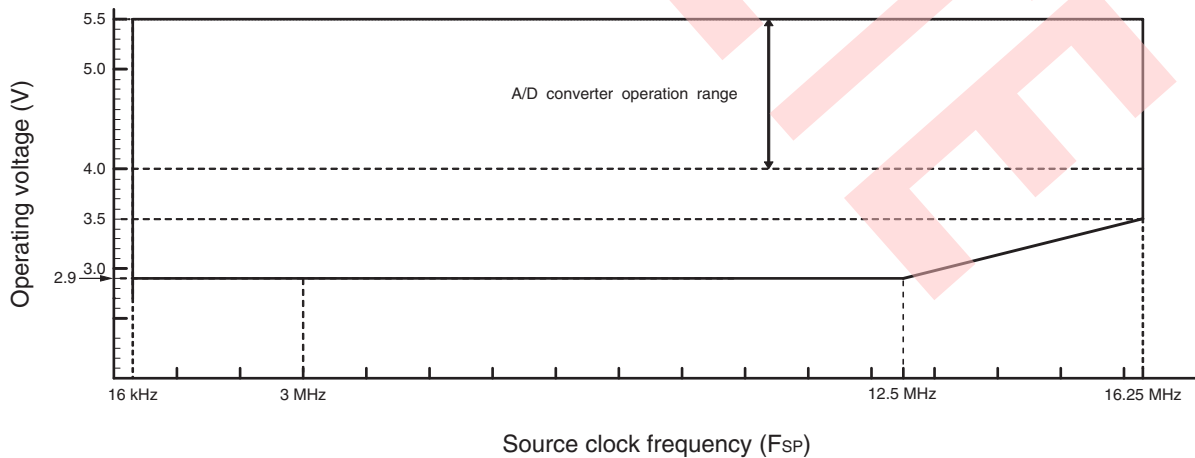
**Schematic diagram of the clock generation block**



**Operating voltage - Operating frequency (When  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )  
MB95220H (without the on-chip debug function)**



**Operating voltage - Operating frequency (When  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )  
MB95220H (with the on-chip debug function)**



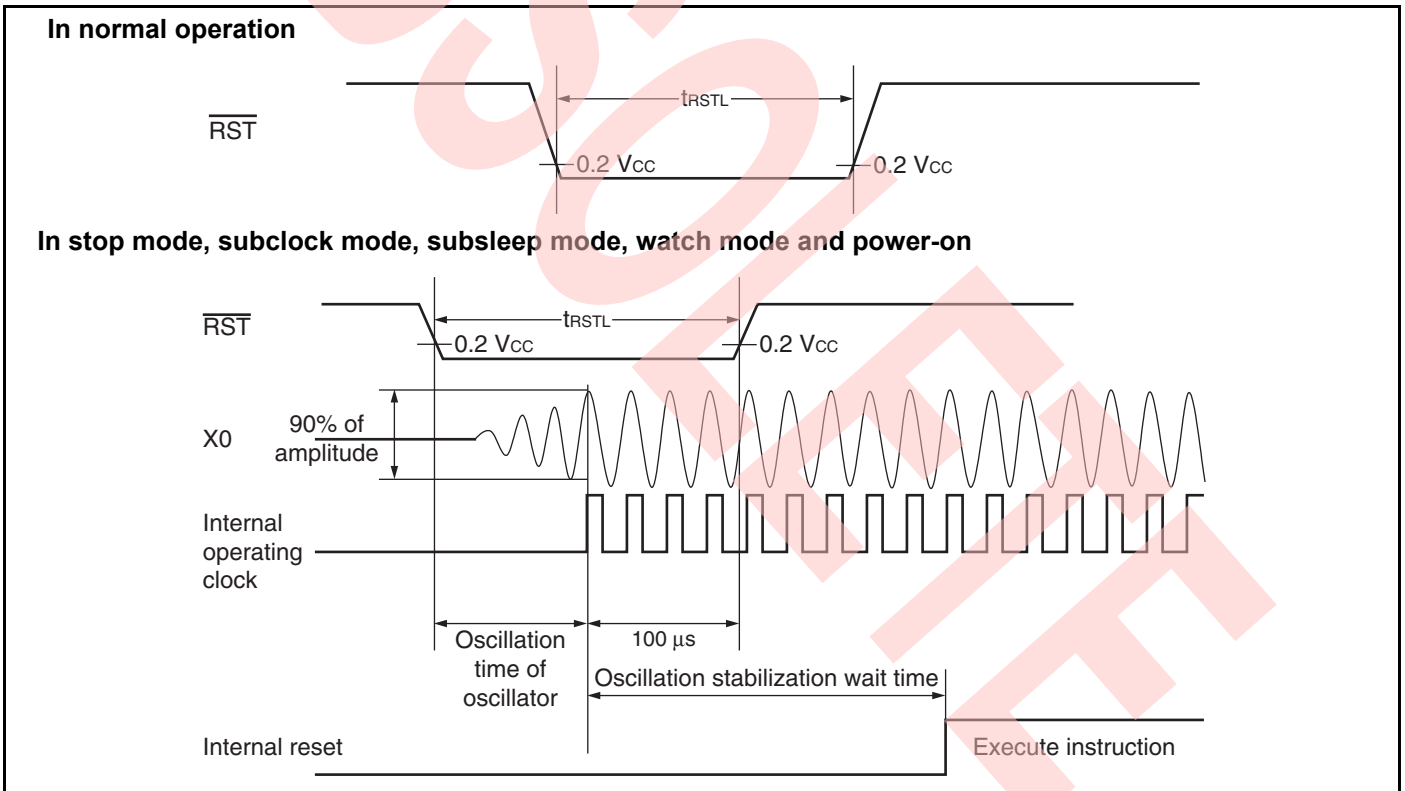
13.4.3 External Reset

( $V_{CC} = 5.0 V \pm 10\%$ ,  $V_{SS} = 0.0 V$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ )

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{RST}$ "L" level pulse width	$t_{RSTL}$	$2 t_{MCLK}^{*1}$	—	ns	In normal operation
		Oscillation time of the oscillator <sup>*2</sup> +100	—	$\mu s$	In stop mode, subclock mode, sub-sleep mode, watch mode, and power on
		100	—	$\mu s$	In timebase timer mode

\*1: See "13.4.2. Source Clock/Machine Clock" for  $t_{MCLK}$ .

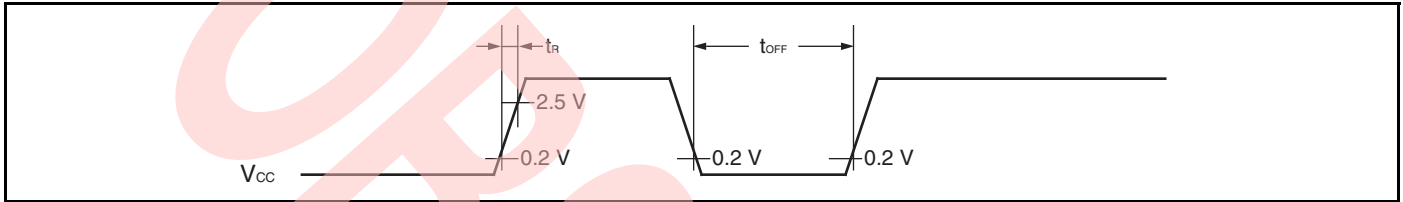
\*2: The oscillation time of an oscillator is the time for it to reach 90% of its amplitude. The crystal oscillator has an oscillation time of between several ms and tens of ms. The ceramic oscillator has an oscillation time of between hundreds of  $\mu s$  and several ms. The external clock has an oscillation time of 0 ms. The CR oscillator clock has an oscillation time of between several  $\mu s$  and several ms.



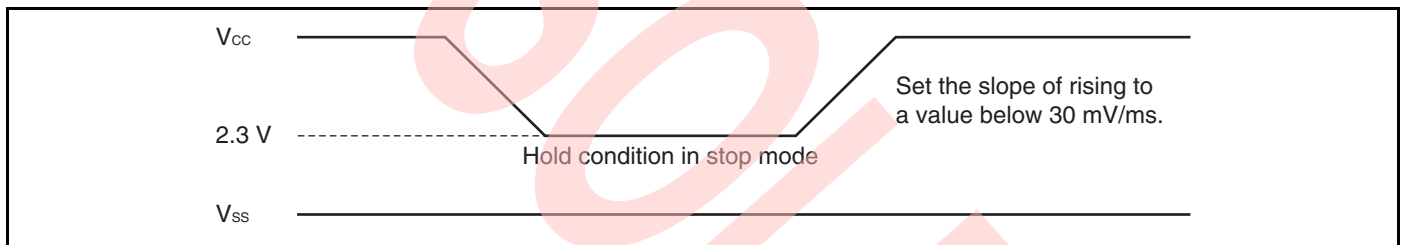
**13.4.4 Power-on Reset**

 ( $V_{SS} = 0.0\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power supply rising time	$t_R$	—	—	50	ms	
Power supply cutoff time	$t_{OFF}$	—	1	—	ms	Wait time until power-on



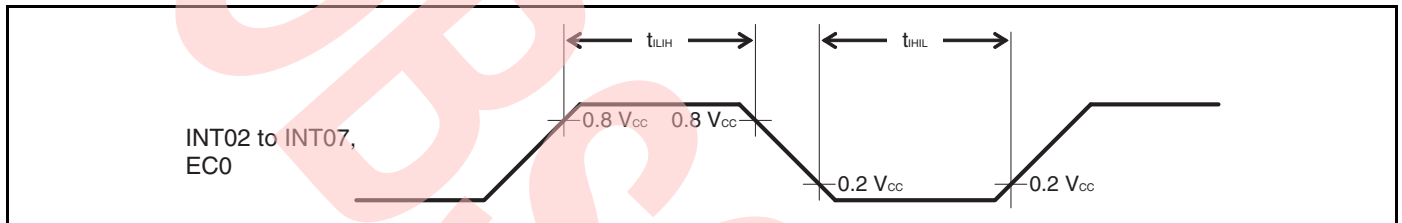
Note: A sudden change of power supply voltage may activate the power-on reset function. When changing the power supply voltage during the operation, set the slope of rising to a value below within 30 mV/ms as shown below.



**13.4.5 Peripheral Input Timing**
 $(V_{CC} = 5.0 V \pm 10\%, V_{SS} = 0.0 V, T_A = -40^\circ C \text{ to } +85^\circ C)$ 

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Peripheral input "H" pulse width	$t_{LIH}$	INT02 to INT07, EC0	$2 t_{MCLK}^*$	—	ns
Peripheral input "L" pulse width	$t_{IHIL}$		$2 t_{MCLK}^*$	—	ns

\* See "13.4.2. Source Clock/Machine Clock" for  $t_{MCLK}$ .



**13.4.6 LIN-UART Timing (Available only in MB95F222H/F222K/F223H/F223K)**

Sampling is executed at the rising edge of the sampling clock\*1, and serial clock delay is disabled\*2.  
 (ESCR register:SCES bit = 0, ECCR register:SCDE bit = 0)

(V<sub>CC</sub> = 5.0 V±10%, AV<sub>SS</sub> = V<sub>SS</sub> = 0.0 V, T<sub>A</sub> = -40°C to +85°C)

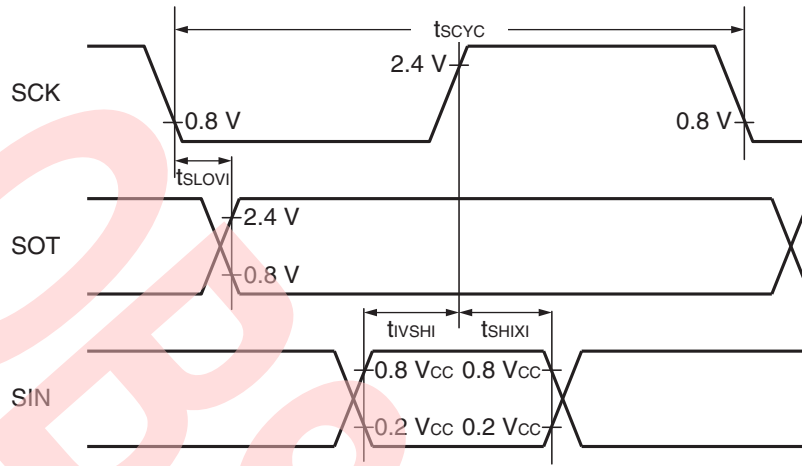
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t <sub>SCYC</sub>	SCK	Internal clock operation output pin: C <sub>L</sub> = 80 pF+1 TTL	5 t <sub>MCLK</sub> *3	—	ns
SCK ↓→SOT delay time	t <sub>SLOVI</sub>	SCK, SOT		-95	+95	ns
Valid SIN → SCK ↑	t <sub>IVSHI</sub>	SCK, SIN		t <sub>MCLK</sub> *3+190	—	ns
SCK ↑→ valid SIN hold time	t <sub>SHIXI</sub>	SCK, SIN		0	—	ns
Serial clock “L” pulse width	t <sub>SLSH</sub>	SCK	External clock operation output pin: C <sub>L</sub> = 80 pF+1 TTL	3 t <sub>MCLK</sub> *3-t <sub>R</sub>	—	ns
Serial clock “H” pulse width	t <sub>SHSL</sub>	SCK		t <sub>MCLK</sub> *3+95	—	ns
SCK ↓→SOT delay time	t <sub>SLOVE</sub>	SCK, SOT		—	2 t <sub>MCLK</sub> *3+95	ns
Valid SIN → SCK ↑	t <sub>IVSHE</sub>	SCK, SIN		190	—	ns
SCK ↑→valid SIN hold time	t <sub>SHIXE</sub>	SCK, SIN		t <sub>MCLK</sub> *3+95	—	ns
SCK fall time	t <sub>F</sub>	SCK		—	10	ns
SCK rise time	t <sub>R</sub>	SCK		—	10	ns

\*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

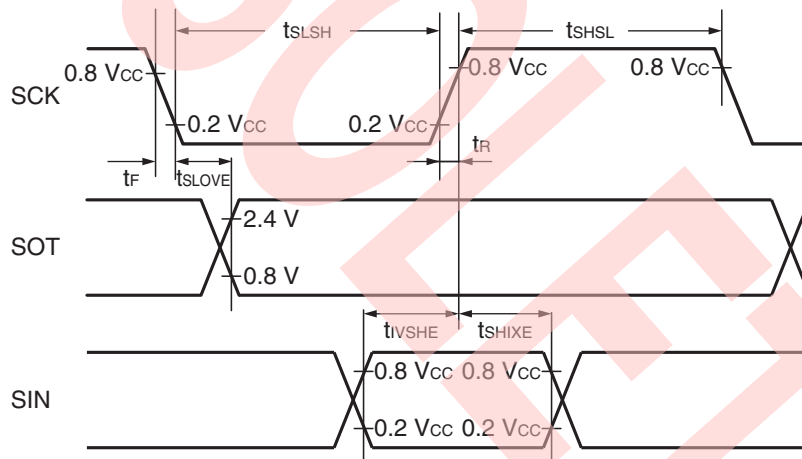
\*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

\*3: See “13.4.2. Source Clock/Machine Clock” for t<sub>MCLK</sub>.

**Internal shift clock mode**



**External shift clock mode**



Sampling is executed at the falling edge of the sampling clock\*1, and serial clock delay is disabled\*2.  
(ESCR register:SCES bit = 1, ECCR register:SCDE bit = 0)

( $V_{CC} = 5.0 V \pm 10\%$ ,  $V_{SS} = 0.0 V$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ )

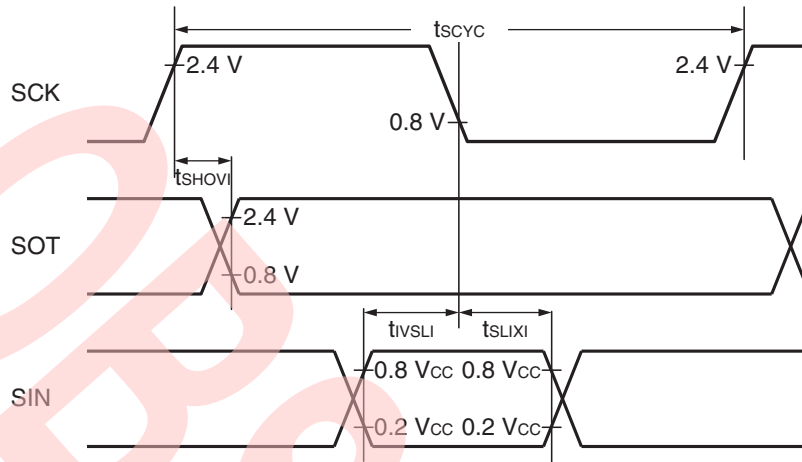
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCK	Internal clock operation output pin: $C_L = 80 \text{ pF} + 1 \text{ TTL}$	$5 t_{MCLK}^{*3}$	—	ns
SCK $\uparrow \rightarrow$ SOT delay time	$t_{SHOVI}$	SCK, SOT		-95	+95	ns
Valid SIN $\rightarrow$ SCK $\downarrow$	$t_{IVSLI}$	SCK, SIN		$t_{MCLK}^{*3} + 190$	—	ns
SCK $\downarrow \rightarrow$ valid SIN hold time	$t_{SLIXI}$	SCK, SIN		0	—	ns
Serial clock "H" pulse width	$t_{SHSL}$	SCK	External clock operation output pin: $C_L = 80 \text{ pF} + 1 \text{ TTL}$	$3 t_{MCLK}^{*3} - t_R$	—	ns
Serial clock "L" pulse width	$t_{SLSH}$	SCK		$t_{MCLK}^{*3} + 95$	—	ns
SCK $\uparrow \rightarrow$ SOT delay time	$t_{SHOVE}$	SCK, SOT		—	$2 t_{MCLK}^{*3} + 95$	ns
Valid SIN $\rightarrow$ SCK $\downarrow$	$t_{IVSLE}$	SCK, SIN		190	—	ns
SCK $\downarrow \rightarrow$ valid SIN hold time	$t_{SLIXE}$	SCK, SIN		$t_{MCLK}^{*3} + 95$	—	ns
SCK fall time	$t_F$	SCK		—	10	ns
SCK rise time	$t_R$	SCK		—	10	ns

\*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

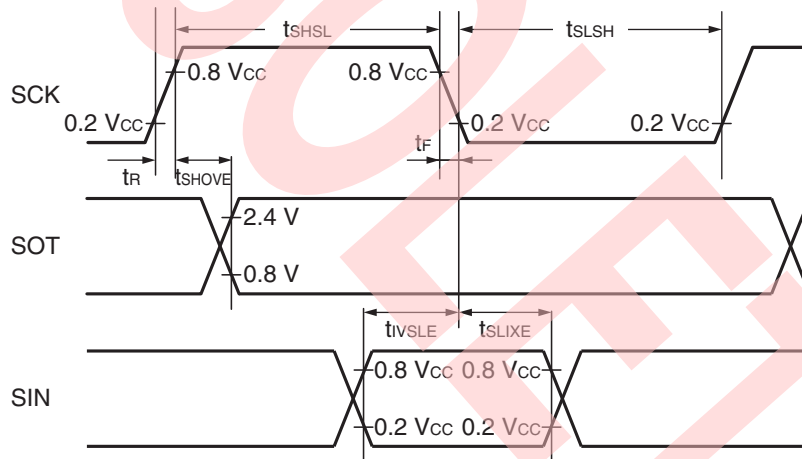
\*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

\*3: See "13.4.2. Source Clock/Machine Clock" for  $t_{MCLK}$ .

**Internal shift clock mode**



**External shift clock mode**



Sampling is executed at the rising edge of the sampling clock\*<sup>1</sup>, and serial clock delay is enabled\*<sup>2</sup>.  
 (ESCR register:SCES bit = 0, ECCR register:SCDE bit = 1)

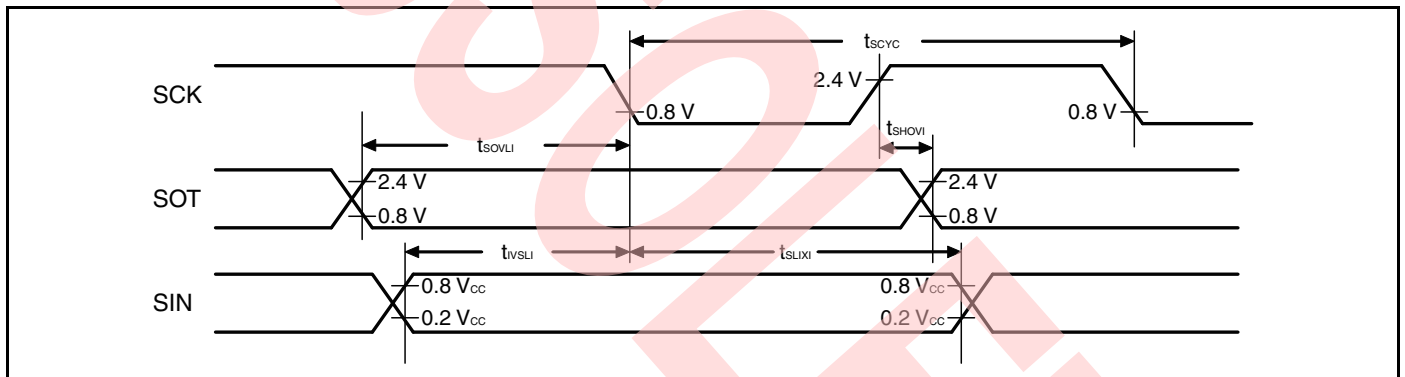
( $V_{CC} = 5.0 V \pm 10\%$ ,  $V_{SS} = 0.0 V$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ )

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCK	Internal clock operation output pin: $C_L = 80 \text{ pF} + 1 \text{ TTL}$	$5 t_{MCLK}^{*3}$	—	ns
SCK $\uparrow$ → SOT delay time	$t_{SHOVI}$	SCK, SOT		-95	+95	ns
Valid SIN → SCK $\downarrow$	$t_{IVSLI}$	SCK, SIN		$t_{MCLK}^{*3} + 190$	—	ns
SCK $\downarrow$ → valid SIN hold time	$t_{SLIXI}$	SCK, SIN		0	—	ns
SOT → SCK $\downarrow$ delay time	$t_{SOVLI}$	SCK, SOT		—	$4 t_{MCLK}^{*3}$	ns

\*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

\*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

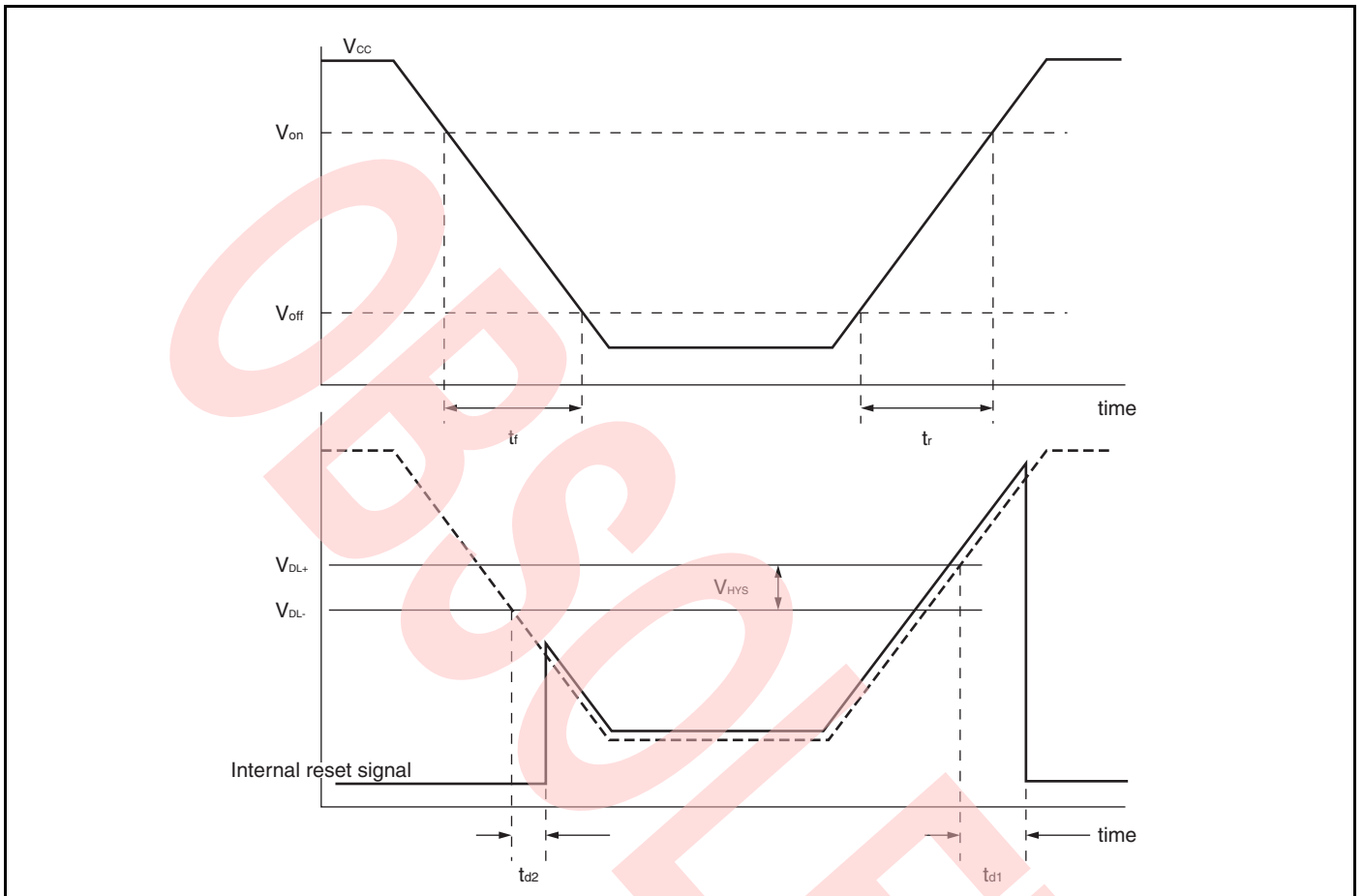
\*3: See “13.4.2. Source Clock/Machine Clock” for  $t_{MCLK}$ .





**13.4.7 Low-voltage Detection**
*(V<sub>SS</sub> = 0.0 V, T<sub>A</sub> = -40°C to +85°C)*

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Release voltage	V <sub>DL+</sub>	2.52	2.7	2.88	V	At power supply rise
Detection voltage	V <sub>DL-</sub>	2.42	2.6	2.78	V	At power supply fall
Hysteresis width	V <sub>HYS</sub>	70	100	—	mV	
Power supply start voltage	V <sub>off</sub>	—	—	2.3	V	
Power supply end voltage	V <sub>on</sub>	4.9	—	—	V	
Power supply voltage change time (at power supply rise)	t <sub>r</sub>	1	—	—	μs	Slope of power supply that the reset release signal generates
		—	3000	—	μs	Slope of power supply that the reset release signal generates within the rating (V <sub>DL+</sub> )
Power supply voltage change time (at power supply fall)	t <sub>f</sub>	300	—	—	μs	Slope of power supply that the reset detection signal generates
		—	300	—	μs	Slope of power supply that the reset detection signal generates within the rating (V <sub>DL-</sub> )
Reset release delay time	t <sub>d1</sub>	—	—	300	μs	
Reset detection delay time	t <sub>d2</sub>	—	—	20	μs	



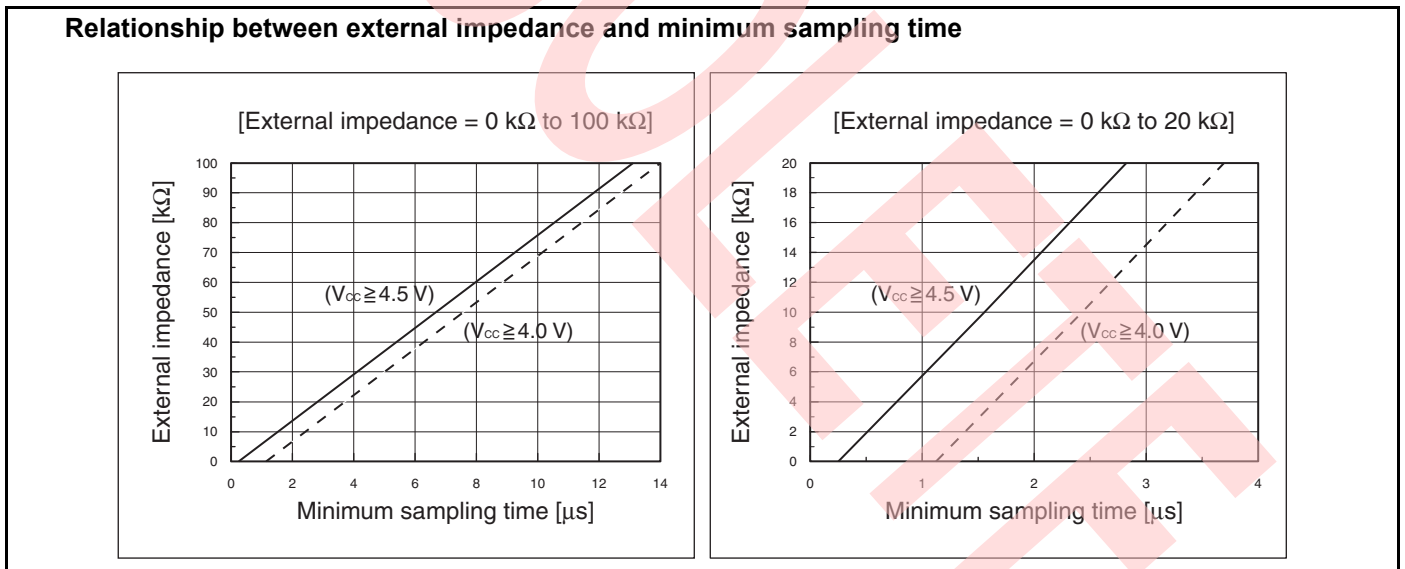
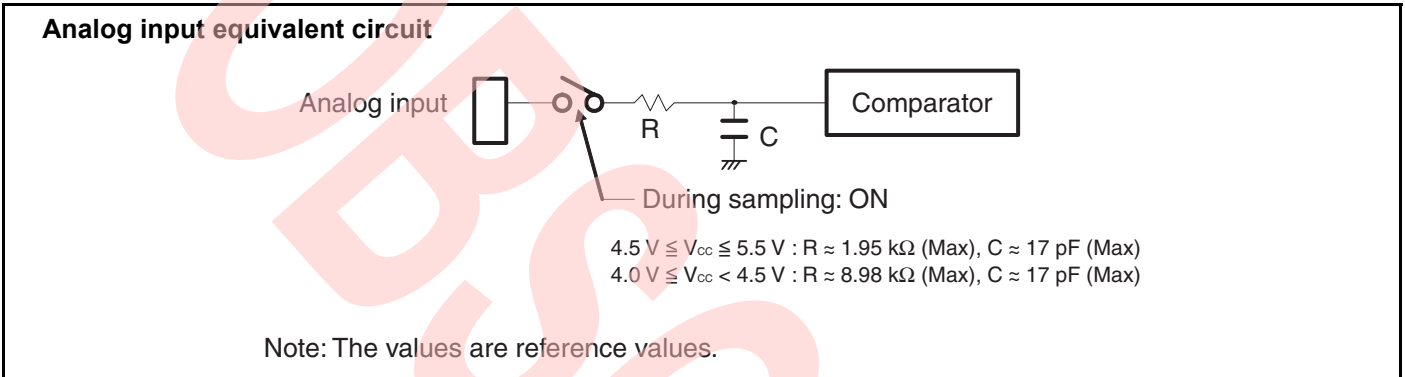
**13.5 A/D Converter**
**13.5.1 A/D Converter Electrical Characteristics**
 $(V_{CC} = 4.0\text{ V to } 5.5\text{ V}, V_{SS} = 0.0\text{ V}, T_A = -40^\circ\text{C to } +85^\circ\text{C})$ 

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution		—	—	10	bit	
Total error		-3	—	+3	LSB	
Linearity error	—	-2.5	—	+2.5	LSB	
Differential linear error		-1.9	—	+1.9	LSB	
Zero transition voltage	$V_{OT}$	$V_{SS}-1.5\text{ LSB}$	$V_{SS}+0.5\text{ LSB}$	$V_{SS}+2.5\text{ LSB}$	V	
Full-scale transition voltage	$V_{FST}$	$V_{CC}-4.5\text{ LSB}$	$V_{CC}-2\text{ LSB}$	$V_{CC}+0.5\text{ LSB}$	V	
Compare time	—	0.9	—	16500	$\mu\text{s}$	$4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$
		1.8	—	16500	$\mu\text{s}$	$4.0\text{ V} \leq V_{CC} < 4.5\text{ V}$
Sampling time	—	0.6	—	$\infty$	$\mu\text{s}$	$4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ , with external impedance < 5.4 k $\Omega$
		1.2	—	$\infty$	$\mu\text{s}$	$4.0\text{ V} \leq V_{CC} \leq 4.5\text{ V}$ , with external impedance < 2.4 k $\Omega$
Analog input current	$I_{AIN}$	-0.3	—	+0.3	$\mu\text{A}$	
Analog input voltage	$V_{AIN}$	$V_{SS}$	—	$V_{CC}$	V	

13.5.2 Notes on Using the A/D Converter

**External impedance of analog input and its sampling time**

The A/D converter has a sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the capacitor of the internal sample and hold circuit is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, considering the relationship between the external impedance and minimum sampling time, either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. In addition, if sufficient sampling time cannot be secured, connect a capacitor of about 0.1  $\mu\text{F}$  to the analog input pin.



**A/D conversion error**

As  $|V_{CC} - V_{SS}|$  decreases, the A/D conversion error increases proportionately.

13.5.3 Definitions of A/D Converter Terms

**Resolution**

It indicates the level of analog variation that can be distinguished by the A/D converter. When the number of bits is 10, analog voltage can be divided into  $2^{10} = 1024$ .

**Linearity error (unit: LSB)**

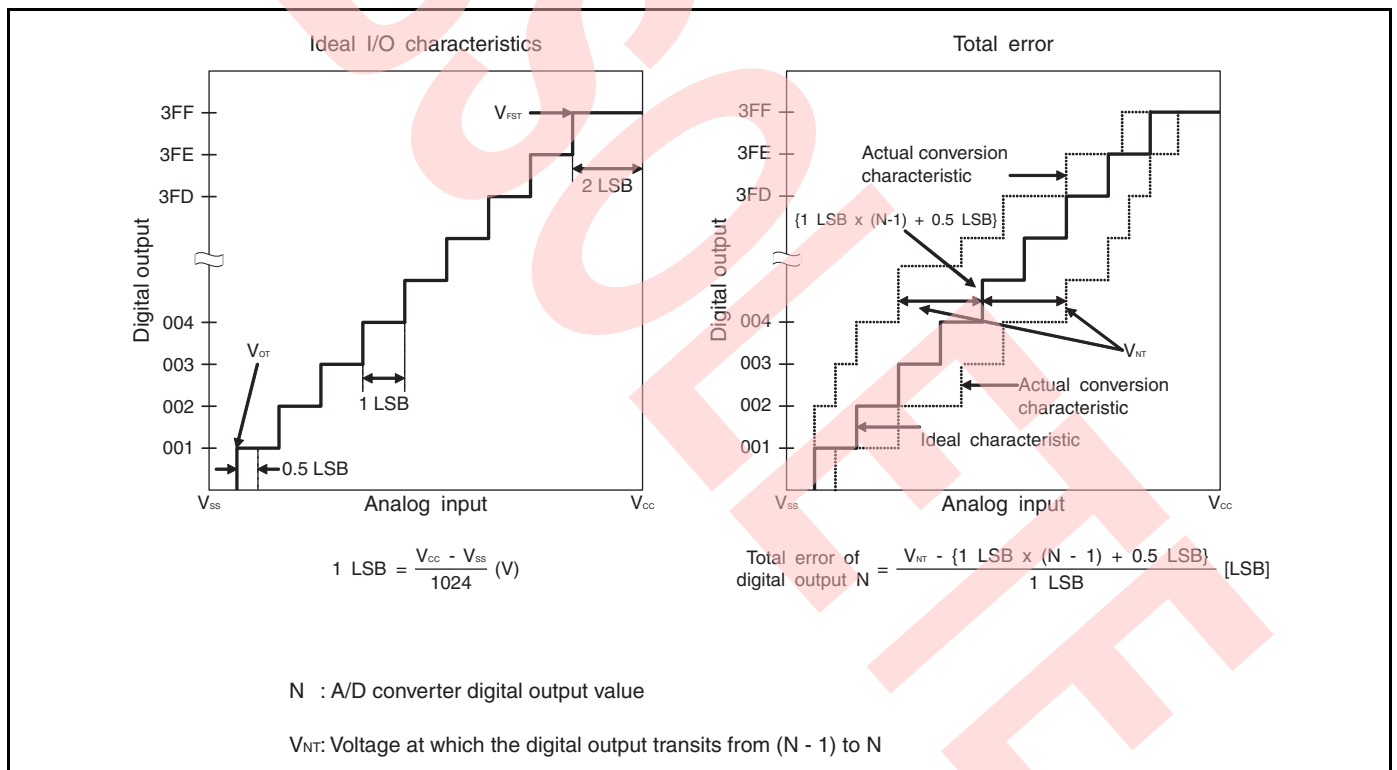
It indicates how much an actual conversion value deviates from the straight line connecting the zero transition point ("00 0000 0000" ← → "00 0000 0001") of a device to the full-scale transition point ("11 1111 1111" ← → "11 1111 1110") of the same device.

**Differential linear error (unit : LSB)**

It indicates how much the input voltage required to change the output code by 1 LSB deviates from an ideal value.

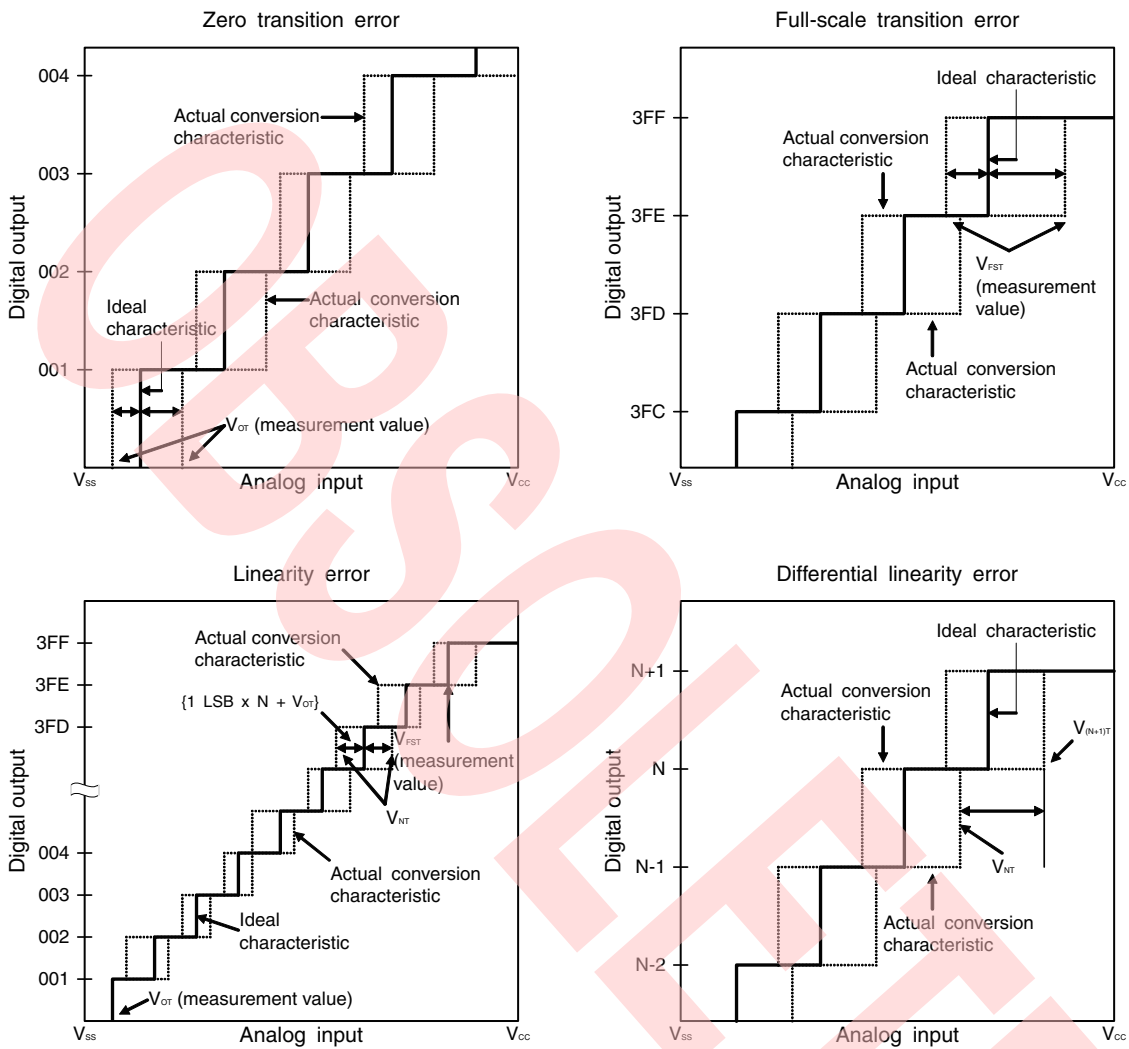
**Total error (unit: LSB)**

It indicates the difference between an actual value and a theoretical value. The error can be caused by a zero transition error, a full-scale transition errors, a linearity error, a quantum error, or noise.



(Continued)

(Continued)



$$\text{Linearity error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times N + V_{or}\}}{1 \text{ LSB}}$$

$$\text{Differential linear error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1$$

N : A/D converter digital output value

$V_{NT}$ : Voltage at which the digital output transits from (N - 1) to N

$V_{or}$  (ideal value) =  $V_{SS} + 0.5 \text{ LSB}$  [V]

$V_{FST}$  (ideal value) =  $V_{CC} - 2 \text{ LSB}$  [V]

**13.6 Flash Memory Program/Erase Characteristics**

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Chip erase time	—	1*1	15*2	s	00 <sub>H</sub> programming time prior to erasure is excluded.
Byte programming time	—	32	3600	μs	System-level overhead is excluded.
Erase/program voltage	9.5	10	10.5	V	The erase/program voltage must be applied to the PF2 pin in erase/program.
Current drawn on PF2	—	—	5.0	mA	Current consumption of PF2 pin during flash memory program/erase
Erase/program cycle	—	100000	—	cycle	
Power supply voltage at erase/program	3.0	—	5.5	V	
Flash memory data retention time	20*3	—	—	year	Average T <sub>A</sub> = +85°C

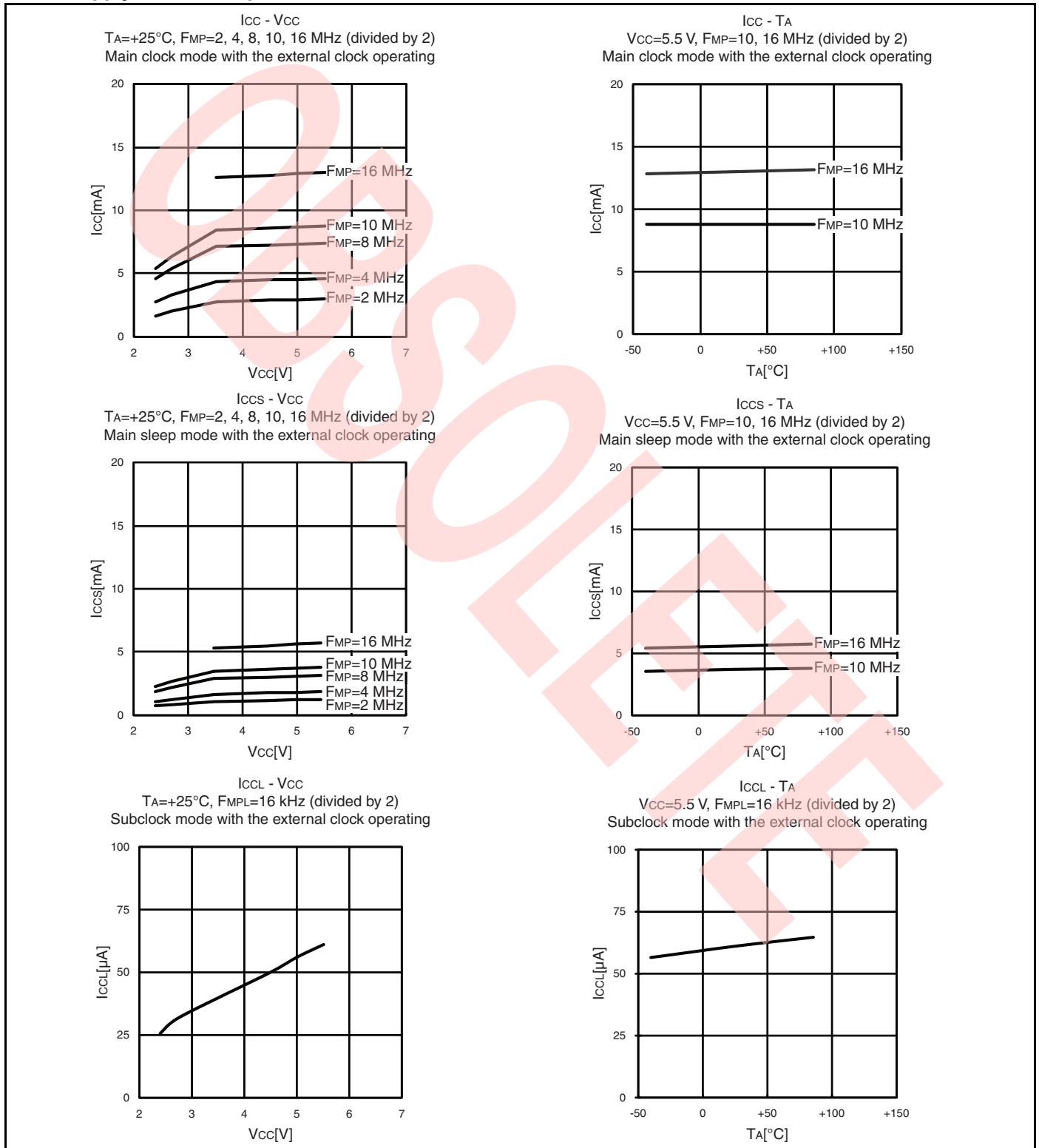
\*1: T<sub>A</sub> = +25°C, V<sub>CC</sub> = 5.0 V, 100000 cycles

\*2: T<sub>A</sub> = +85°C, V<sub>CC</sub> = 4.5 V, 100000 cycles

\*3: This value is converted from the result of a technology reliability assessment. (The value is converted from the result of a high temperature accelerated test by using the Arrhenius equation with the average temperature being +85°C) .

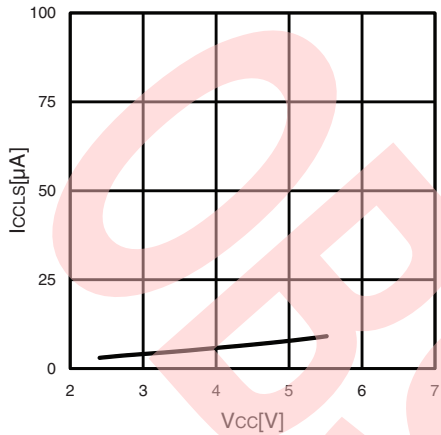
### 14. Sample Electrical Characteristics

#### Power supply current-temperature

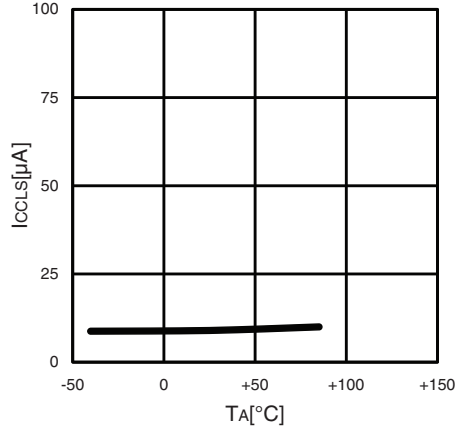


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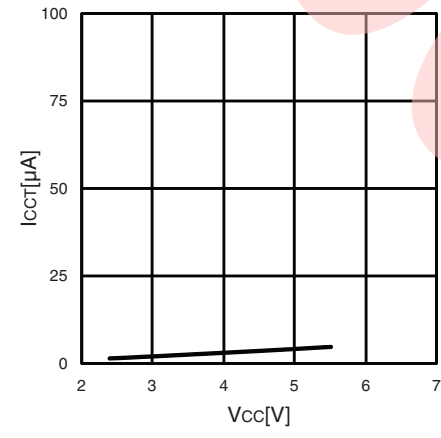
**ICCLS - Vcc**  
 TA=+25°C, FMPL=16 kHz (divided by 2)  
 Subsleeper mode with the external clock operating



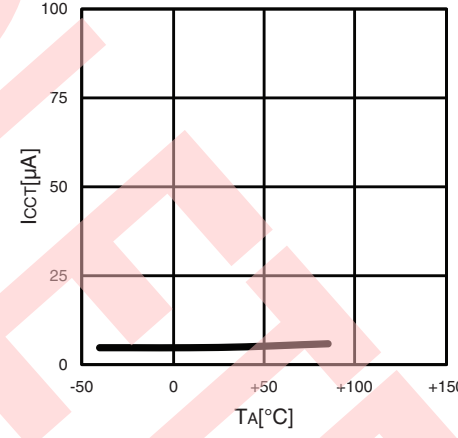
**ICCLS - TA**  
 VCC=5.5 V, FMPL=16 kHz (divided by 2)  
 Subsleeper mode with the external clock operating



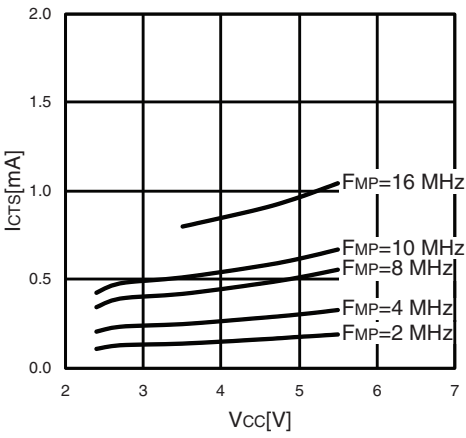
**ICCT - Vcc**  
 TA=+25°C, FMPL=16 kHz (divided by 2)  
 Clock mode with the external clock operating



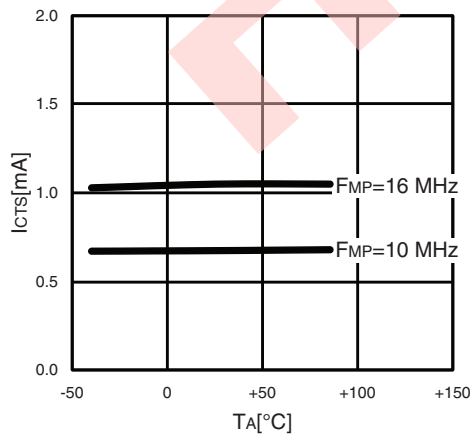
**ICCT - TA**  
 V=5.5 V, FMPL=16 kHz (divided by 2)  
 Clock mode with the external clock operating



**ICTS - Vcc**  
 TA=+25°C, FMP=2, 4, 8, 10, 16 MHz (divided by 2)  
 Timebase timer mode with the external clock operating



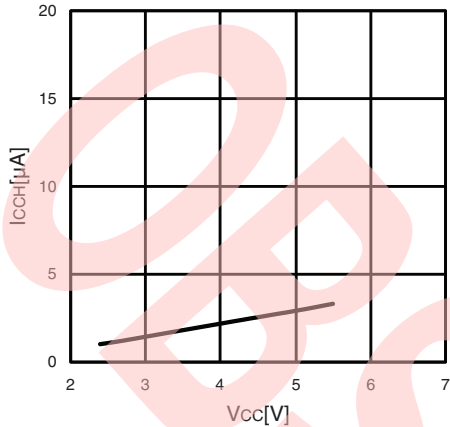
**ICTS - TA**  
 V=5.5 V, FMP=10, 16 MHz (divided by 2)  
 Timebase timer mode with the external clock operating



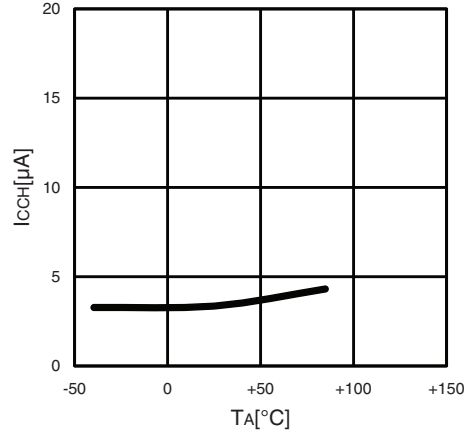
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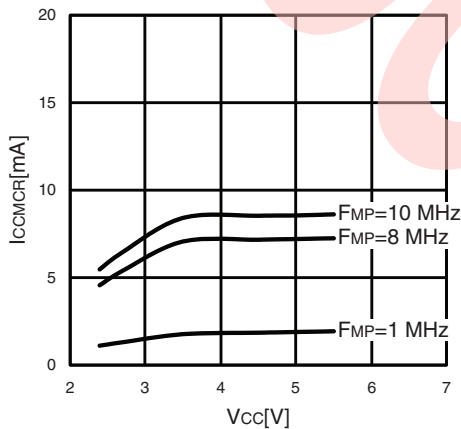
**ICCH - VCC**  
 $T_A = +25^\circ\text{C}$ , FMPL=(stop)  
 Substop mode with the external clock stopping



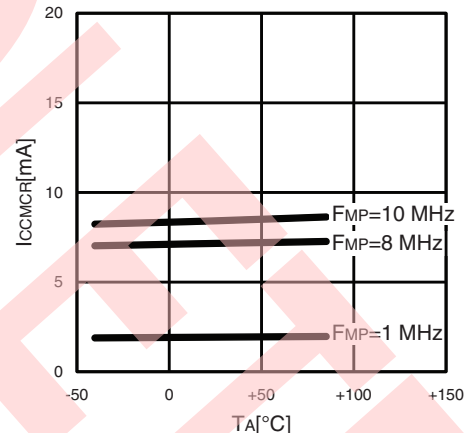
**ICCH - TA**  
 $V = 5.5\text{ V}$ , FMPL=(stop)  
 Substop mode with the external clock stopping



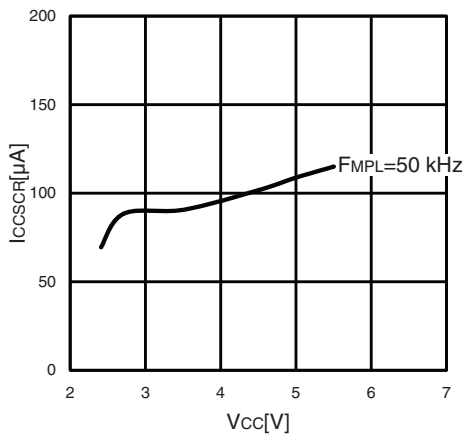
**ICCMCR - VCC**  
 $T_A = +25^\circ\text{C}$ , FMPL=1, 8, 10 MHz (no division)  
 Main clock mode with the internal main CR clock operating



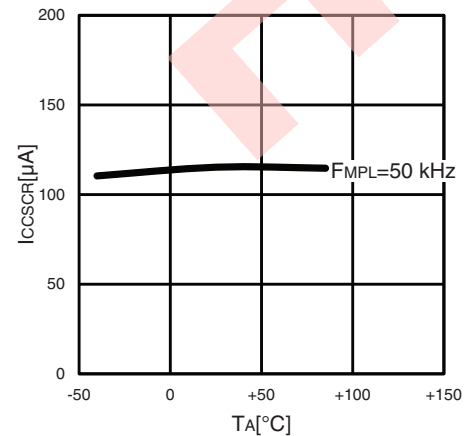
**ICCMCR - TA**  
 $V = 5.5\text{ V}$ , FMPL=1, 8, 10 MHz (no division)  
 Main clock mode with the internal main CR clock operating



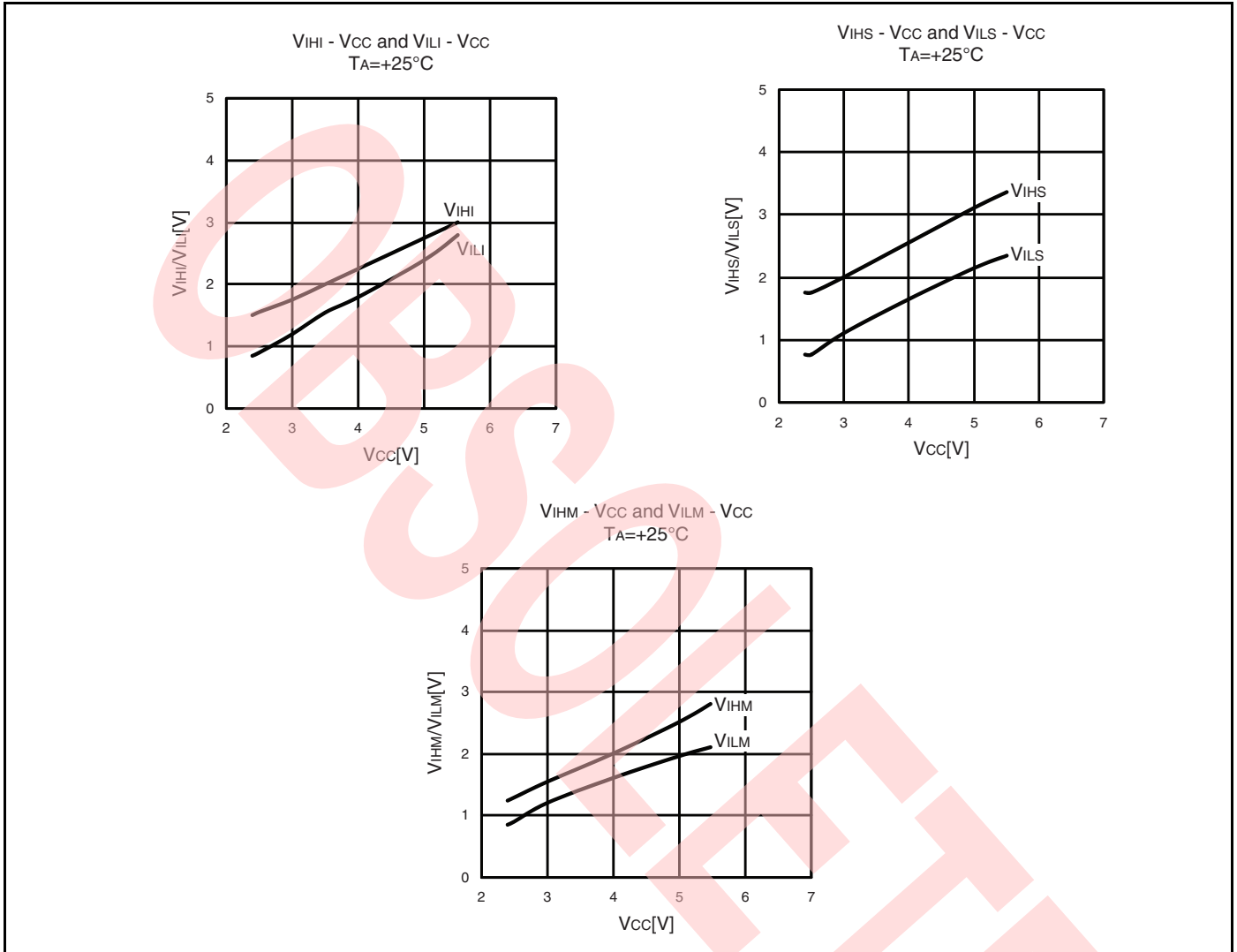
**ICCSSCR - VCC**  
 $T_A = +25^\circ\text{C}$ , FMPL=50 kHz (divided by 2)  
 Subclock mode with the internal sub-CR clock operating



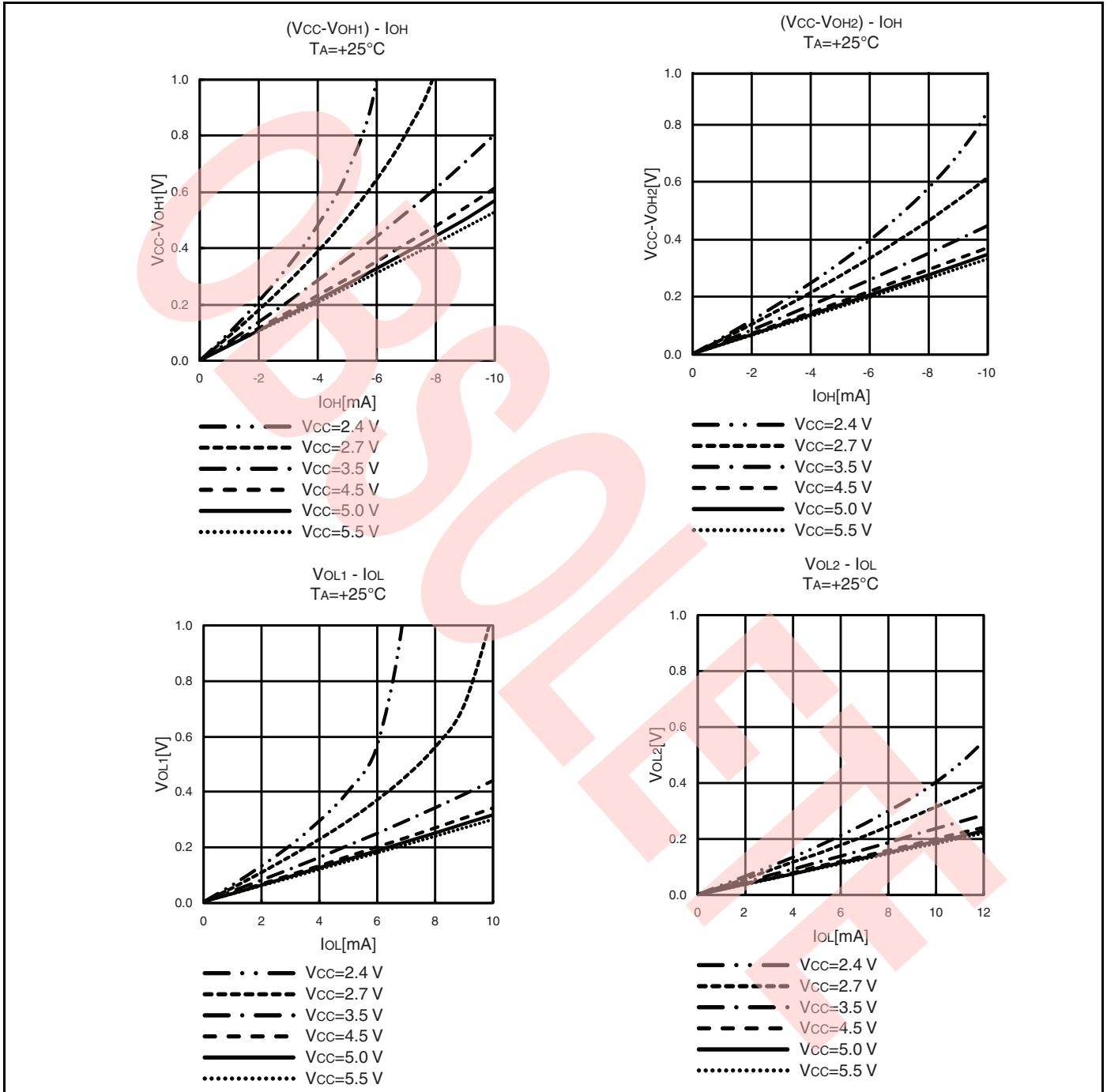
**ICCSSCR - TA**  
 $V_{CC} = 5.5\text{ V}$ , FMPL=50 kHz (divided by 2)  
 Subclock mode with the internal sub-CR clock operating



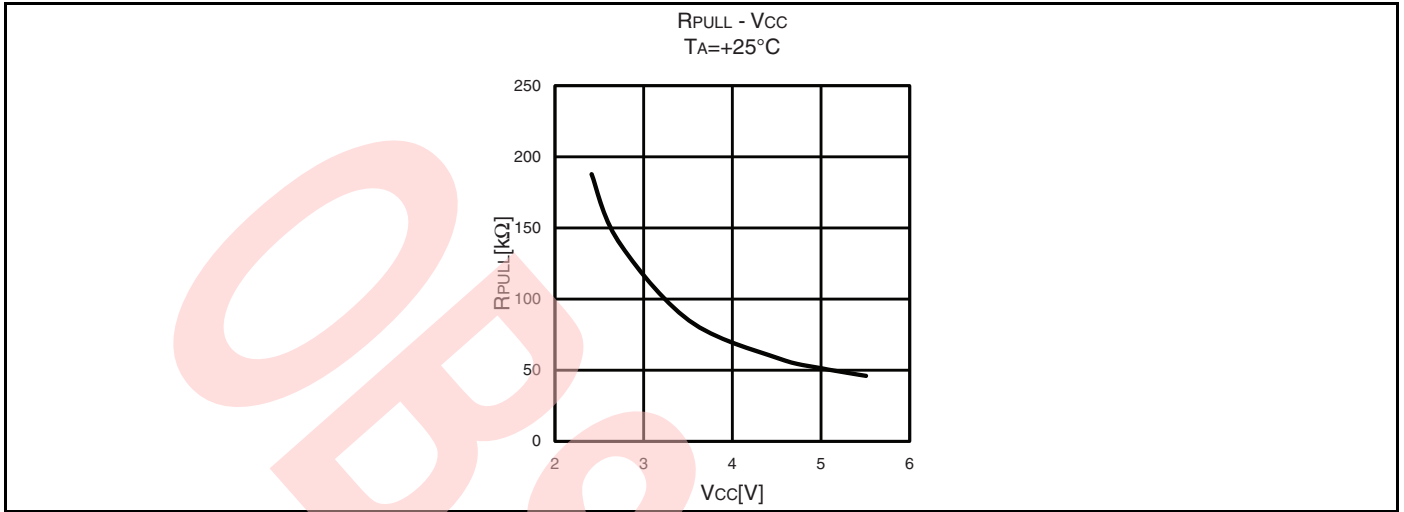
Input voltage



Output voltage



**Pull-up**



**15. Mask Options**

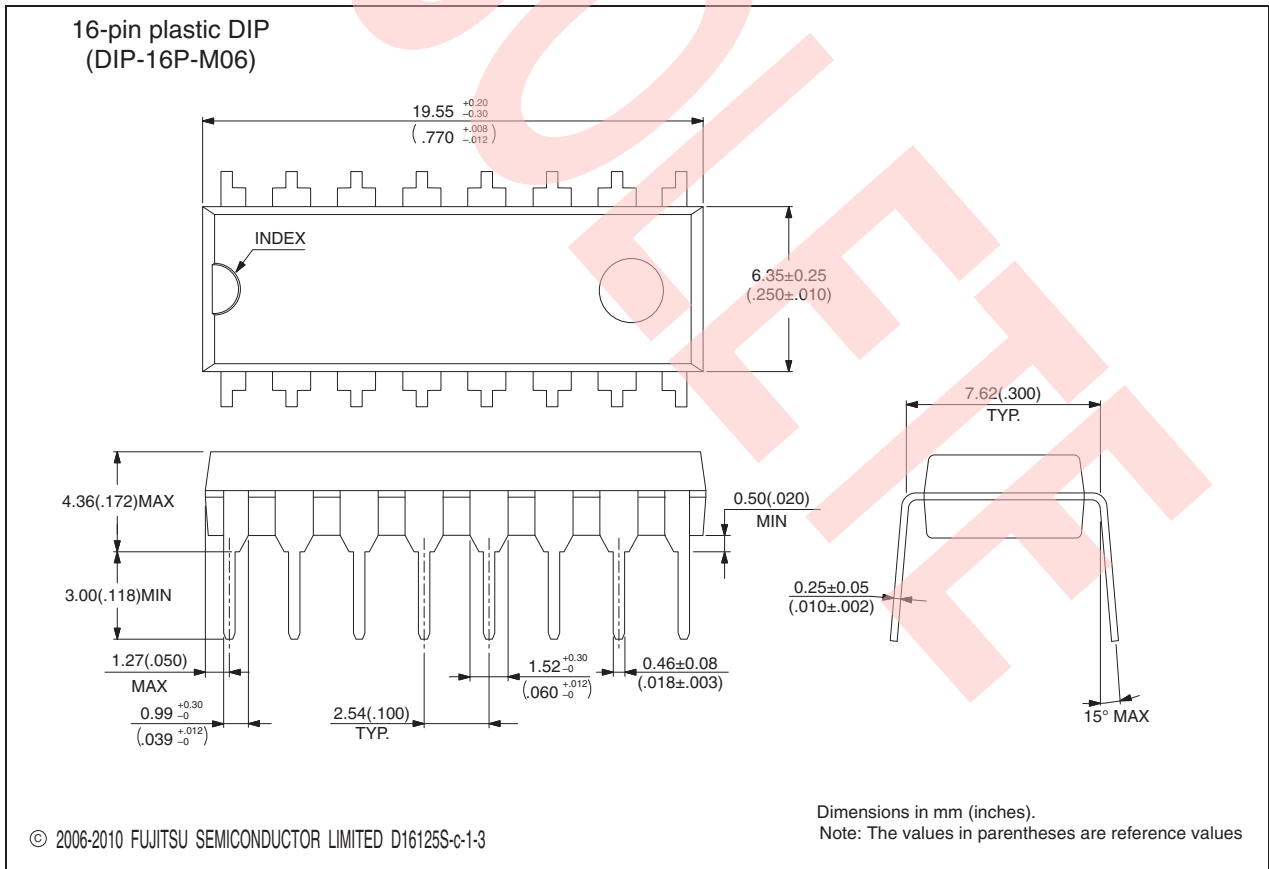
No.	Part Number	MB95F222H MB95F223H	MB95F222K MB95F223K
	Selectable/Fixed	Fixed	Fixed
1	Low-voltage detection reset <ul style="list-style-type: none"> <li>• With low-voltage detection reset</li> <li>• Without low-voltage detection reset</li> </ul>	Without low-voltage detection reset	With low-voltage detection reset
2	Reset <ul style="list-style-type: none"> <li>• With dedicated reset input</li> <li>• Without dedicated reset input</li> </ul>	With dedicated reset input	Without dedicated reset input

**16. Ordering Information**

Part Number	Package
MB95F222HPH-G-SNE2 MB95F222KPH-G-SNE2 MB95F223HPH-G-SNE2 MB95F223KPH-G-SNE2	16-pin plastic DIP (DIP-16P-M06)
MB95F222HPF-G-SNE1 MB95F222KPF-G-SNE1 MB95F223HPF-G-SNE1 MB95F223KPF-G-SNE1	16-pin plastic SOP (FPT-16P-M06)

**17. Package Dimensions**

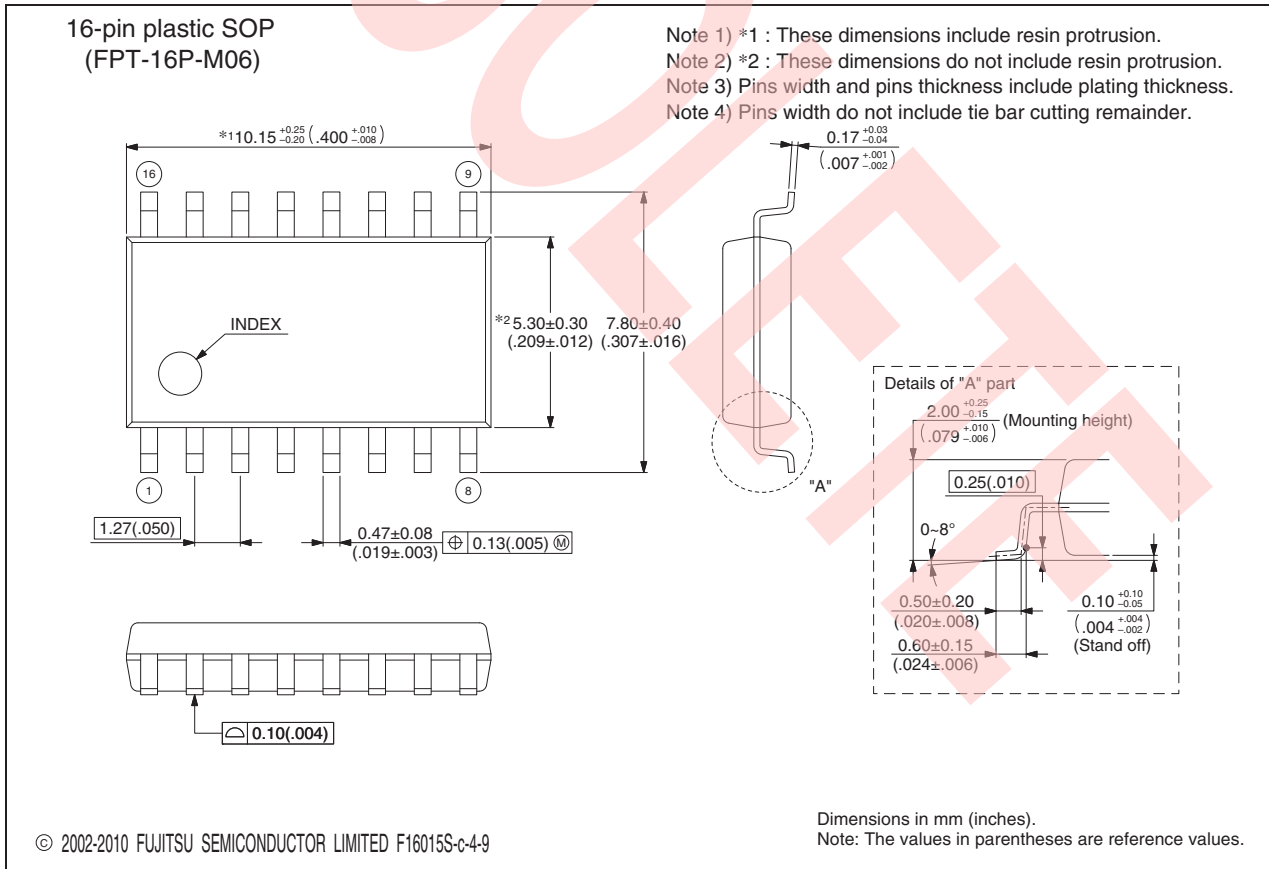
<p>16-pin plastic DIP</p> <p>(DIP-16P-M06)</p>	Lead pitch	2.54 mm
	Sealing method	Plastic mold



(Continued)

(Continued)

<p>16-pin plastic SOP</p> <p>(FPT-16P-M06)</p>	Lead pitch	1.27 mm
	Package width × package length	5.3 × 10.15 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	2.25 mm MAX
	Weight	0.20 g
	Code (Reference)	P-SOP16-5.3×10.15-1.27



## 18. Major Changes

Spanion Publication Number: DS07-12626-3E

Page	Section	Change Results
21	Electrical Characteristics 1. Absolute Maximum Ratings	Changed the characteristics of Input voltage.
24	3. DC Characteristics	Corrected the maximum value of "H" level input voltage for PF2 pin. $V_{CC} + 0.3 \rightarrow 10.5$
		Corrected the maximum value of Open-drain output application voltage. $0.2V_{CC} \rightarrow V_{SS} + 5.5$
26		Added the footnote *3.
29	4. AC Characteristics (1) Clock Timing	Added a figure of HCLK1/HCLK2.
32	(2) Source Clock/Machine Clock	Corrected the graph of Operating voltage - Operating frequency (with the on-chip debug function). (Corrected the pitch)
33	(3) External Reset	Added and power on to the remarks column.
48	6. Flash Memory Program/ Erase Characteristics	Added the row of Current drawn on PF2.
		Corrected the minimum value of Power supply voltage at erase/program. $4.5 \rightarrow 3.0$

**NOTE:** Please see "Document History" about later revised information.

**Document History**

Document Title: MB95220H Series F <sup>2</sup> MC-8FX 8-bit Microcontroller Document Number: 002-07513				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	AKIH	07/26/2010	Migrated to Cypress and assigned document number 002-07513. No change to document contents or format.
*A	5198887	AKIH	03/31/2016	Updated to Cypress template.
*B	5861646	YSAT	08/24/2017	Updated Cypress Logo and Copyright.
*C	6591784	SSAS	06/10/2019	Obsolete document. Completing Sunset Review.

DRAFT

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