



**THE DATASHEET OF
MAX989ESA+**



MAX985/MAX986/MAX989/ MAX990/MAX993/MAX994

Micropower, Low-Voltage, UCSP/SC70, Rail-to-Rail I/O Comparators

General Description

The MAX985/MAX986/MAX989/MAX990/MAX993/MAX994 single/dual/quad micropower comparators feature low-voltage operation and rail-to-rail inputs and outputs. Their operating voltages range from 2.5V to 5.5V, making them ideal for both 3V and 5V systems. These comparators also operate with $\pm 1.25V$ to $\pm 2.75V$ dual supplies. They consume only 11 μA of supply current while achieving a 300ns propagation delay.

Input bias current is typically 1.0pA, and input offset voltage is typically 0.5mV. Internal hysteresis ensures clean output switching, even with slow-moving input signals.

The output stage's unique design limits supply-current surges while switching, virtually eliminating the supply glitches typical of many other comparators. The MAX985/MAX989/MAX993 have a push-pull output stage that sinks as well as sources current. Large internal output drivers allow rail-to-rail output swing with loads up to 8mA. The MAX986/MAX990/MAX994 have an open-drain output stage that can be pulled beyond VCC to 6V (max) above VEE. These open-drain versions are ideal for level translators and bipolar to single-ended converters.

The single MAX985 is available in a chip-scale package (UCSP™), significantly reducing the required PC board area. The single MAX985/MAX986 are available in 5-pin SC70 packages and the dual MAX989/MAX990 are available in 8-pin SOT23 packages.

Selector Guide

PART	COMPARATORS PER PACKAGE	OUTPUT STAGE
MAX985	1	Push-Pull
MAX986	1	Open-Drain
MAX989	2	Push-Pull
MAX990	2	Open-Drain
MAX993	4	Push-Pull
MAX994	4	Open-Drain

Applications

Portable/Battery-Powered Systems	Threshold Detectors/Discriminators
Mobile Communications	Ground/Supply-Sensing Applications
Zero-Crossing Detectors	IR Receivers
Window Comparators	Digital Line Receivers
Level Translators	

UCSP is a trademark and μ MAX is a registered trademark of Maxim Integrated Products, Inc.

Features

- ◆ 11 μA Quiescent Supply Current
- ◆ 2.5V to 5.5V Single-Supply Operation
- ◆ Common-Mode Input Voltage Range Extends 250mV Beyond the Rails
- ◆ 300ns Propagation Delay
- ◆ Push-Pull Output Stage Sinks and Sources 8mA Current (MAX985/MAX989/MAX993)
- ◆ Open-Drain Output Voltage Extends Beyond VCC (MAX986/MAX990/MAX994)
- ◆ Unique Output Stage Reduces Output Switching Current, Minimizing Overall Power Consumption
- ◆ 80 μA Supply Current at 1MHz Switching Frequency
- ◆ No Phase Reversal for Overdriven Inputs
- ◆ Available in Space-Saving Packages:
 UCSP (MAX985)
 SOT23 (MAX985/MAX986/MAX989/MAX990)
 μ MAX® (MAX989/MAX990)

Ordering Information

PART	PIN-PACKAGE	TOP MARK
MAX985EBT+TG45	6 UCSP	AAV
MAX985EXK+T	5 SC70	ABK

Note: All devices are specified over the -40°C to +85°C operating temperature range.

+Denotes a lead(Pb)-free/RoHS-compliant package.

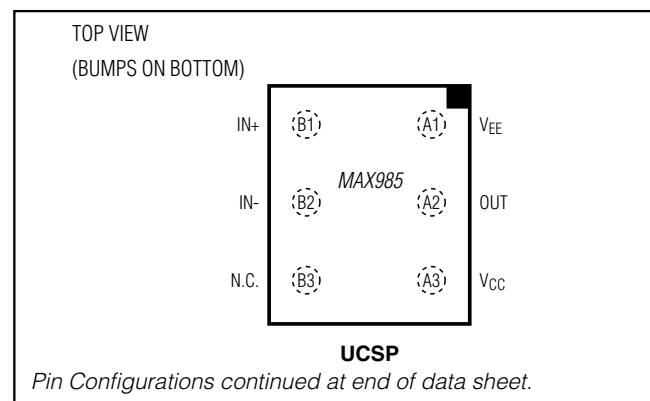
T = Tape and reel.

G45 = Protective die coating.

Ordering Information continued at end of data sheet.

Typical Application Circuit appears at end of data sheet.

Pin Configurations



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V _{CC} to V _{EE})6V	8-Pin SOT23 (derate 5.1mW/°C above +70°C)408.2mW
Current into Input Pins±20mA	8-Pin μMAX (derate 4.8mW/°C above +70°C)387.8mW
IN ₋ , IN ₊ to V _{EE}-0.3V to (V _{CC} + 0.3V)	8-Pin SO (derate 7.4mW/°C above +70°C)588.2mW
OUT ₋ to V _{EE}-0.3V to (V _{CC} + 0.3V)	14-Pin TSSOP (derate 10mW/°C above +70°C)796.8mW
MAX985/MAX989/MAX993-0.3V to (V _{CC} + 0.3V)	14-Pin SO (derate 11.9mW/°C above +70°C)952.4mW
MAX986/MAX990/MAX994-0.3V to 6V	Operating Temperature Range-40°C to +85°C
OUT ₋ Short-Circuit Duration to V _{EE} or V _{CC}10s	Junction Temperature+150°C
Continuous Power Dissipation (Multilayer board, T _A = +70°C)	Storage Temperature Range-65°C to +150°C
5-Pin SC70 (derate 3.1mW/°C above +70°C)247mW	Lead Temperature (except UCSP, soldering, 10s)+300°C
5-Pin SOT23 (derate 3.9mW/°C above +70°C)312.6mW	Soldering Temperature (reflow)+260°C
6-Bump UCSP (derate 3.9mW/°C above +70°C)308mW		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7V to 5.5V, V_{EE} = 0V, V_{CM} = 0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V _{CC}	Inferred from PSRR test		2.5		5.5	V
Supply Current per Comparator	I _{CC}	V _{CC} = 5V	T _A = +25°C		12	20	μA
			T _A = -40°C to +85°C			24	
		V _{CC} = 2.7V	T _A = +25°C		11	20	
			T _A = -40°C to +85°C			24	
Power-Supply Rejection Ratio	PSRR	2.5V ≤ V _{CC} ≤ 5.5V		55	80		dB
Common-Mode Voltage Range (Note 2)	V _{CMR}	T _A = +25°C		V _{EE} - 0.25		V _{CC} + 0.25	V
		T _A = -40°C to +85°C		V _{EE}		V _{CC}	
Input Offset Voltage (Note 3)	V _{OS}	Full common-mode range	T _A = +25°C		±0.5	±5	mV
			T _A = -40°C to +85°C			±7	
Input Hysteresis	V _{HYST}				±3		mV
Input Bias Current (Note 4)	I _B				0.001	10	nA
Input Offset Current	I _{OS}				0.5		pA
Input Capacitance	C _{IN}				1.0		pF
Common-Mode Rejection Ratio	CMRR			52	80		dB
Output Leakage Current (MAX986/MAX990/MAX994 only)	I _{LEAK}	V _{OUT} = high				1.0	μA
Output Short-Circuit Current	I _{SC}	Sourcing or sinking, V _{OUT} = V _{EE} or V _{CC}	V _{CC} = 5V		95		mA
			V _{CC} = 2.7V		35		
OUT Output Voltage Low	V _{OL}	V _{CC} = 5V, I _{SINK} = 8mA	T _A = +25°C		0.2	0.4	V
			T _A = -40°C to +85°C			0.55	
		V _{CC} = 2.7V, I _{SINK} = 3.5mA	T _A = +25°C		0.15	0.3	
			T _A = -40°C to +85°C			0.4	

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ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = 2.7V$ to $5.5V$, $V_{EE} = 0V$, $V_{CM} = 0V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $T_A = +25^{\circ}C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OUT Output Voltage High (MAX985/MAX989/ MAX993 only)	V_{OH}	$V_{CC} = 5V$, $I_{SOURCE} = 8mA$	$T_A = +25^{\circ}C$	4.6	4.85		V
			$T_A = -40^{\circ}C$ to $+85^{\circ}C$	4.45			
		$V_{CC} = 2.7V$, $I_{SOURCE} = 3.5mA$	$T_A = +25^{\circ}C$	2.4	2.55		
			$T_A = -40^{\circ}C$ to $+85^{\circ}C$	2.3			
OUT Rise Time (MAX985/MAX989/ MAX993 only)	t_{RISE}	$V_{CC} = 5.0V$	$C_L = 15pF$		40		ns
			$C_L = 50pF$		50		
			$C_L = 200pF$		80		
OUT Fall Time	t_{FALL}	$V_{CC} = 5.0V$	$C_L = 15pF$		40		ns
			$C_L = 50pF$		50		
			$C_L = 200pF$		80		
Propagation Delay	t_{PD-}	$C_L = 15pF$	MAX985/MAX989/ MAX993 only	10mV overdrive		450	ns
				100mV overdrive		300	
			MAX986/MAX990/ MAX994 only, $R_{PULLUP} = 5.1k\Omega$	10mV overdrive		450	
				100mV overdrive		300	
	t_{PD+}	MAX985/MAX989/ MAX993 only, $C_L = 15pF$	10mV overdrive		450		
			100mV overdrive		300		
Power-Up Time	t_{PU}				20		μs

Note 1: All device specifications are 100% production tested at $T_A = +25^{\circ}C$. Limits over the extended temperature range are guaranteed by design.

Note 2: Inferred from the V_{OS} test. Both or either inputs can be driven 0.3V beyond either supply rail without output phase reversal.

Note 3: V_{OS} is defined as the center of the hysteresis band at the input.

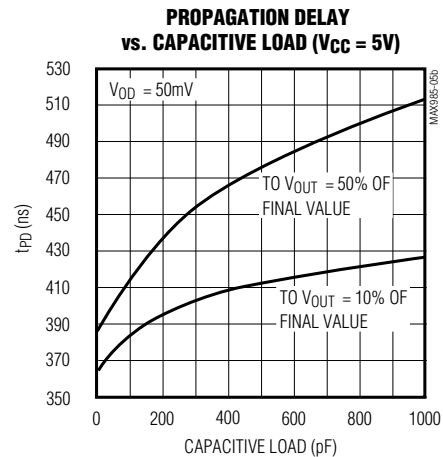
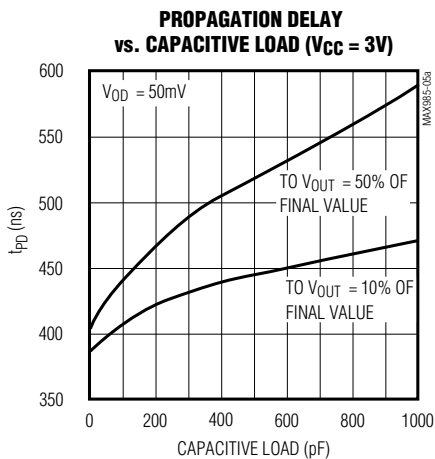
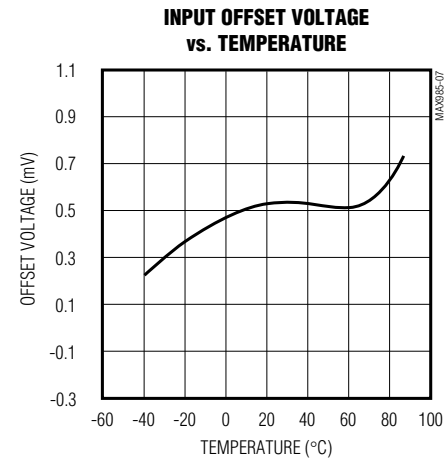
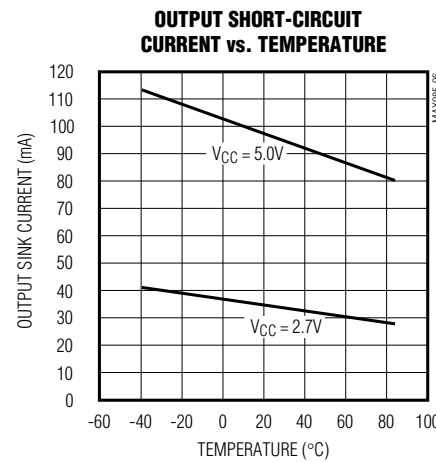
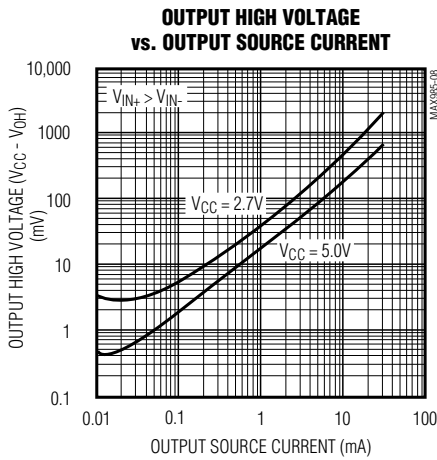
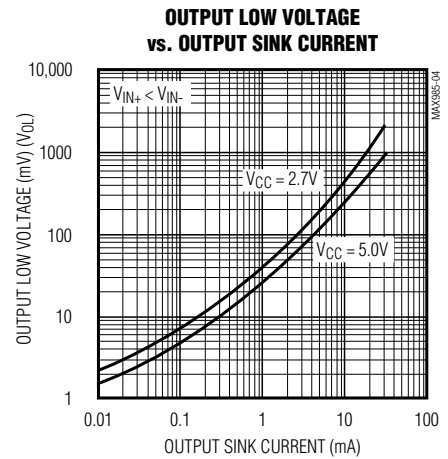
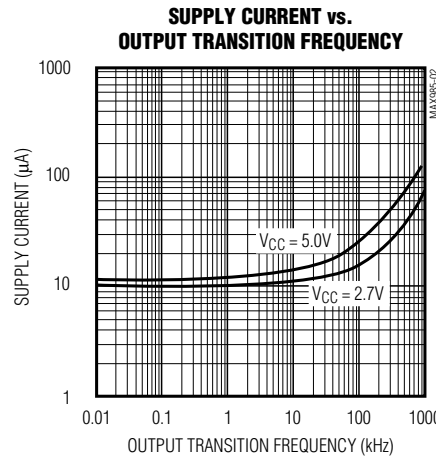
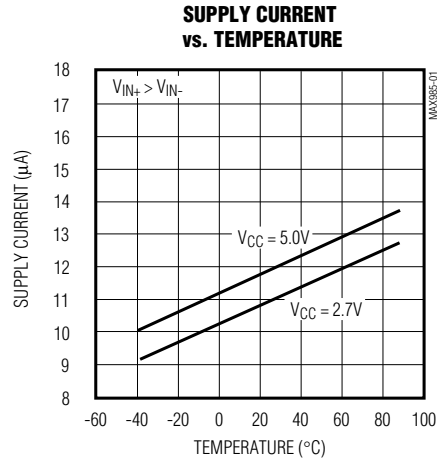
Note 4: I_B is defined as the average of the two input bias currents (I_{B-} , I_{B+}).

MAX985/MAX986/MAX989/ MAX990/MAX993/MAX994

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Typical Operating Characteristics

($V_{CC} = 5V$, $V_{CM} = 0V$, $T_A = +25^\circ C$, unless otherwise noted.)

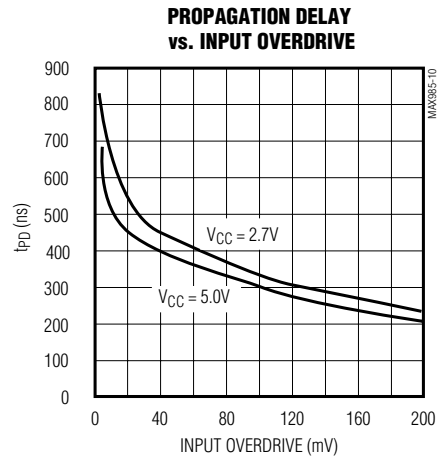
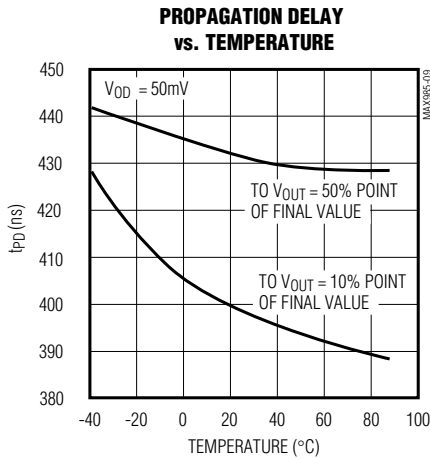


MAX985/MAX986/MAX989/ MAX990/MAX993/MAX994

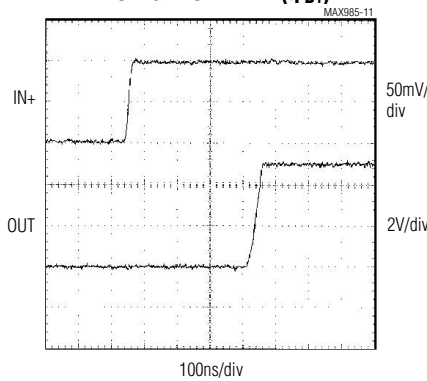
Micropower, Low-Voltage, UCSP/SC70, Rail-to-Rail I/O Comparators

Typical Operating Characteristics (continued)

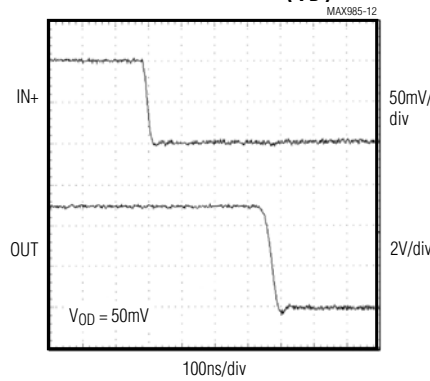
($V_{CC} = 5V$, $V_{CM} = 0V$, $T_A = +25^\circ C$, unless otherwise noted.)



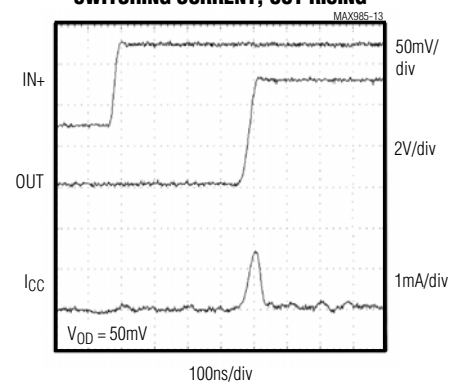
**MAX985/MAX989/MAX993
PROPAGATION DELAY (t_{PD+})**



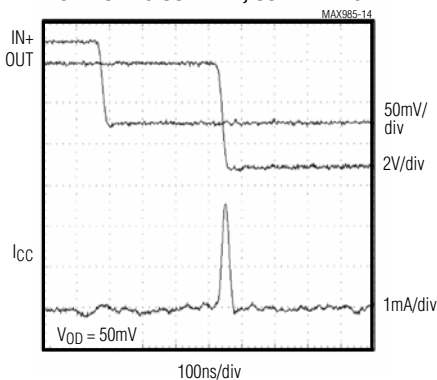
PROPAGATION DELAY (t_{PD-})



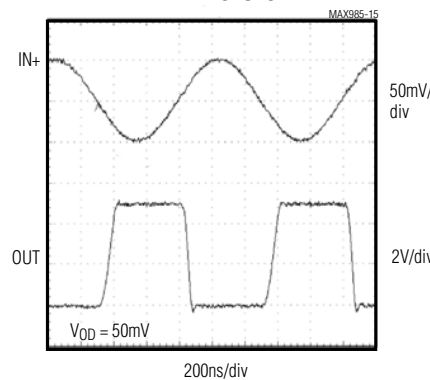
**MAX985/MAX989/MAX993
SWITCHING CURRENT, OUT RISING**



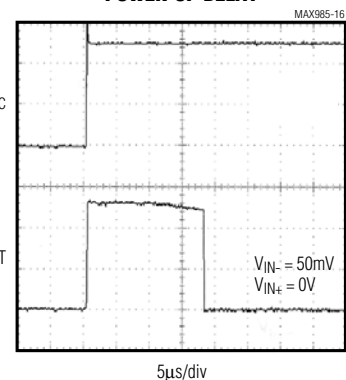
SWITCHING CURRENT, OUT FALLING



1MHz RESPONSE



POWER-UP DELAY



MAX985/MAX986/MAX989/ MAX990/MAX993/MAX994

Micropower, Low-Voltage, UCSP/SC70, Rail-to-Rail I/O Comparators

Pin/Bump Description

BUMP	PIN				NAME	FUNCTION
MAX985	MAX985/ MAX986		MAX989/ MAX990	MAX993/ MAX994		
UCSP*	SO	SOT23/ SC70	SO/ μ MAX/ SOT23	SO/ TSSOP		
A2	6	1	—	—	OUT	Comparator Output
A3	7	2	8	4	VCC	Positive Supply Voltage
B1	3	3	—	—	IN+	Comparator Noninverting Input
B2	2	4	—	—	IN-	Comparator Inverting Input
A1	4	5	4	11	VEE	Negative Supply Voltage
—	—	—	1	1	OUTA	Comparator A Output
—	—	—	2	2	INA-	Comparator A Inverting Input
—	—	—	3	3	INA+	Comparator A Noninverting Input
—	—	—	5	5	INB+	Comparator B Noninverting Input
—	—	—	6	6	INB-	Comparator B Inverting Input
—	—	—	7	7	OUTB	Comparator B Output
—	—	—	—	8	OUTC	Comparator C Output
—	—	—	—	9	INC-	Comparator C Inverting Input
				10	INC+	Comparator C Noninverting Input
				12	IND+	Comparator D Noninverting Input
				13	IND-	Comparator D Inverting Input
				14	OUTD	Comparator D Output
B3	1, 5, 8	—	—	—	N.C.	No Connection. Not internally connected.

*MAX985 only

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Detailed Description

The MAX985/MAX986/MAX989/MAX990/MAX993/MAX994 are single/dual/quad low-power, low-voltage comparators. They have an operating supply voltage range between 2.5V and 5.5V and consume only 11 μ A. Their common-mode input voltage range extends 0.25V beyond each rail. Internal hysteresis ensures clean output switching, even with slow-moving input signals. Large internal output drivers allow rail-to-rail output swing with up to 8mA loads.

The output stage employs a unique design that minimizes supply-current surges while switching, virtually eliminating the supply glitches typical of many other comparators. The MAX985/MAX989/MAX993 have a push-pull output structure that sinks as well as sources current. The MAX986/MAX990/MAX994 have an open-drain output stage that can be pulled beyond V_{CC} to an absolute maximum of 6V above V_{EE} .

Input Stage Circuitry

The devices' input common-mode range extends from -0.25V to ($V_{CC} + 0.25V$). These comparators may operate at any differential input voltage within these limits. Input bias current is typically 1.0pA if the input voltage is between the supply rails. Comparator inputs are protected from overvoltage by internal body diodes connected to the supply rails. As the input voltage exceeds the supply rails, these body diodes become forward biased and begin to conduct. Consequently, bias currents increase exponentially as the input voltage exceeds the supply rails.

Output Stage Circuitry

These comparators contain a unique output stage capable of rail-to-rail operation with up to 8mA loads. Many comparators consume orders of magnitude more current during switching than during steady-state operation. However, with this family of comparators, the supply-current change during an output transition is extremely small. The *Typical Operating Characteristics* graph Supply Current vs. Output Transition Frequency shows the minimal supply-current increase as the output switching frequency approaches 1MHz. This characteristic eliminates the need for power-supply filter capacitors to reduce glitches created by comparator switching currents. Another advantage realized in high-speed, battery-powered applications is a substantial increase in battery life.

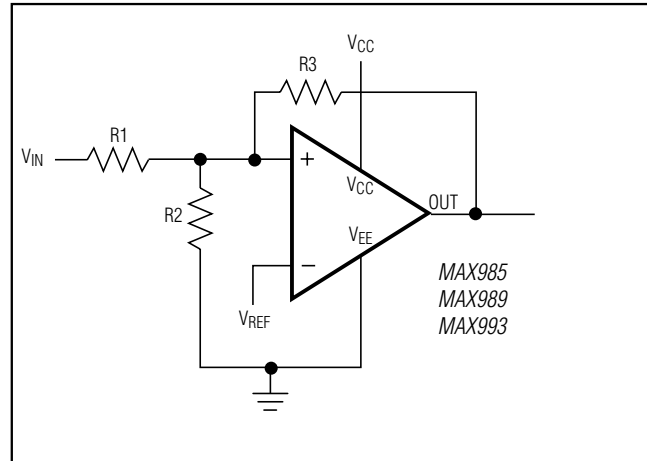


Figure 1. Additional Hysteresis (MAX985/MAX989/MAX993)

Applications Information

Additional Hysteresis

MAX985/MAX989/MAX993

The MAX985/MAX989/MAX993 have $\pm 3mV$ internal hysteresis. Additional hysteresis can be generated with three resistors using positive feedback (Figure 1). Unfortunately, this method also slows hysteresis response time. Use the following procedure to calculate resistor values for the MAX985/MAX989/MAX993.

- 1) Select R3. Leakage current at IN is under 10nA, so the current through R3 should be at least 1 μ A to minimize errors caused by leakage current. The current through R3 at the trip point is $(V_{REF} - V_{OUT}) / R3$. Considering the two possible output states in solving for R3 yields two formulas: $R3 = V_{REF} / 1\mu A$ or $R3 = (V_{REF} - V_{CC}) / 1\mu A$. Use the smaller of the two resulting resistor values. For example, if $V_{REF} = 1.2V$ and $V_{CC} = 5V$, then the two R3 resistor values are 1.2M Ω and 3.8M Ω . Choose a 1.2M Ω standard value for R3.
- 2) Choose the hysteresis band required (V_{HB}). For this example, choose 50mV.
- 3) Calculate R1 according to the following equation:

$$R1 = R3 \times (V_{HB} / V_{CC})$$

For this example, insert the values $R1 = 1.2M\Omega \times (50mV / 5V) = 12k\Omega$.

- 4) Choose the trip point for V_{IN} rising (V_{THR} ; V_{THF} is the trip point for V_{IN} falling). This is the threshold voltage at which the comparator switches its output from low to high as V_{IN} rises above the trip point. For this example, choose 3V.

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5) Calculate R2 as follows. For this example, choose an 8.2kΩ standard value:

$$R2 = \frac{1}{\left(\frac{V_{THR}}{V_{REF} \times R1}\right) - \frac{1}{R1} - \frac{1}{R3}}$$

$$R2 = \frac{1}{\left(\frac{3.0V}{1.2 \times 12k\Omega}\right) - \frac{1}{12k\Omega} - \frac{1}{2.2M\Omega}} = 8.03k\Omega$$

6) Verify trip voltages and hysteresis as follows:

$$V_{IN \text{ rising}}: V_{THR} = V_{REF} \times R1 \times \left(\frac{1}{R1} + \frac{1}{R2} + \frac{1}{R3}\right)$$

$$V_{IN \text{ falling}}: V_{THF} = V_{THR} - \left(\frac{R1 \times V_{CC}}{R3}\right)$$

$$\text{Hysteresis} = V_{THR} - V_{THF}$$

MAX986/MAX990/MAX994

The MAX986/MAX990/MAX994 have ±3mV internal hysteresis. They have open-drain outputs and require an external pullup resistor (Figure 2). Additional hysteresis can be generated using positive feedback, but the formulas differ slightly from those of the MAX985/MAX989/MAX993.

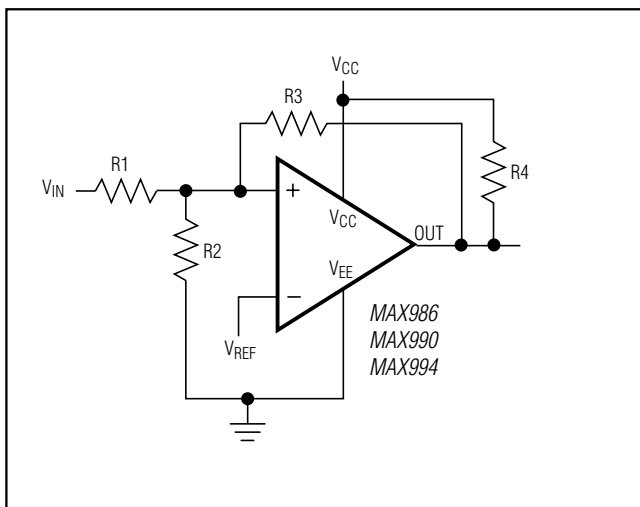


Figure 2. Additional Hysteresis (MAX986/MAX990/MAX994)

Use the following procedure to calculate resistor values:

- 1) Select R3 according to the formulas $R3 = V_{REF} / 500\mu A$ or $R3 = (V_{REF} - V_{CC}) / 500\mu A - R4$. Use the smaller of the two resulting resistor values.
- 2) Choose the hysteresis band required (V_{HB}). For this example, choose 50mV.
- 3) Calculate R1 according to the following equation:
$$R1 = (R3 + R4) \times (V_{HB} / V_{CC})$$
- 4) Choose the trip point for V_{IN} rising (V_{THR} ; V_{THF} is the trip point for V_{IN} falling). This is the threshold voltage at which the comparator switches its output from low to high as V_{IN} rises above the trip point.
- 5) Calculate R2 as follows:

$$R2 = \frac{1}{\left(\frac{V_{THR}}{V_{REF} \times R1}\right) - \frac{1}{R1} - \frac{1}{R3 + R4}}$$

6) Verify trip voltages and hysteresis as follows:

$$V_{IN \text{ rising}}: V_{THR} = V_{REF} \times R1 \times \left(\frac{1}{R1} + \frac{1}{R2} + \frac{1}{R3 + R4}\right)$$

$$V_{IN \text{ falling}}: V_{THF} = V_{THR} - \left(\frac{R1 \times V_{CC}}{R3 + R4}\right)$$

$$\text{Hysteresis} = V_{THR} - V_{THF}$$

Board Layout and Bypassing

Power-supply bypass capacitors are not typically needed, but use 100nF bypass capacitors when supply impedance is high, when supply leads are long, or when excessive noise is expected on the supply lines. Minimize signal trace lengths to reduce stray capacitance.

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Zero-Crossing Detector

Figure 3 shows a zero-crossing detector application. The MAX985's inverting input is connected to ground, and its noninverting input is connected to a 100mV_{p-p} signal source. As the signal at the noninverting input crosses 0V, the comparator's output changes state.

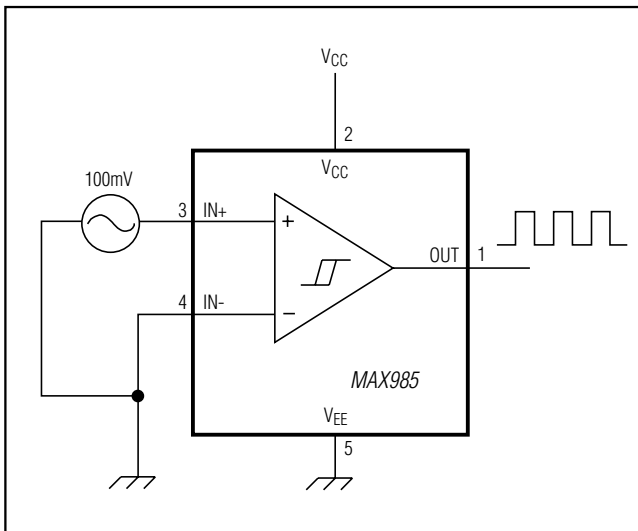


Figure 3. Zero-Crossing Detector

Logic-Level Translator

Figure 4 shows an application that converts 5V logic levels to 3V logic levels. The MAX986 is powered by the 5V supply voltage, and the pullup resistor for the MAX986's open-drain output is connected to the 3V supply voltage. This configuration allows the full 5V logic swing without creating overvoltage on the 3V logic inputs. For 3V to 5V logic-level translation, simply connect the 3V supply to VCC and the 5V supply to the pullup resistor.

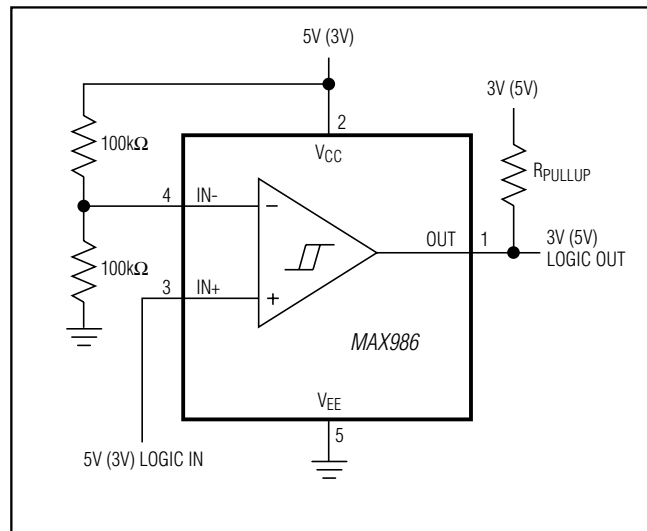
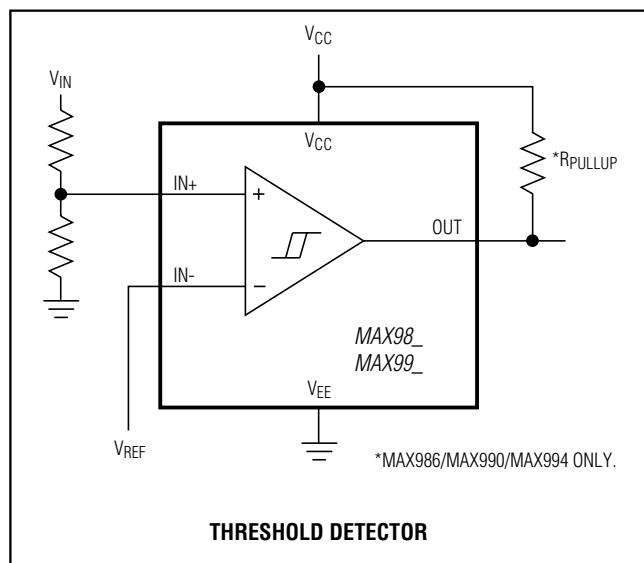


Figure 4. Logic-Level Translator

MAX985/MAX986/MAX989/ MAX990/MAX993/MAX994

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Typical Application Circuit

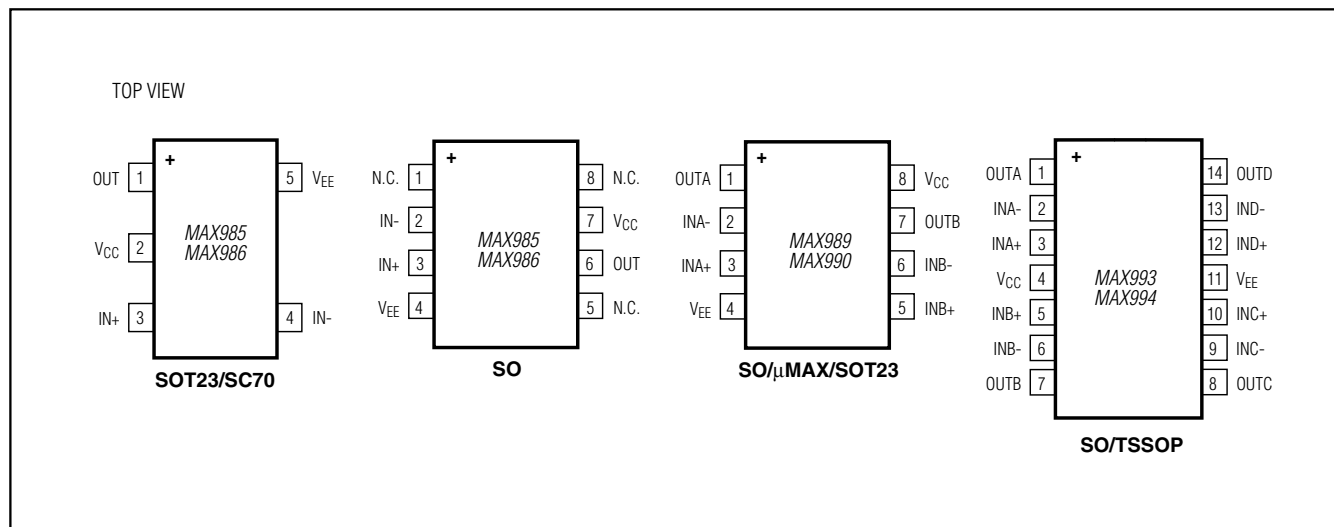


Ordering Information (continued)

PART	PIN-PACKAGE	TOP MARK
MAX985EUK+T	5 SOT23	ABYZ
MAX985ESA+	8 SO	—
MAX986 EKX+T	5 SC70	ABL
MAX986EUK+T	5 SOT23	ABZA
MAX986ESA+	8 SO	—
MAX989 EKA+T	8 SOT23	AADZ
MAX989EUA+T	8 μ MAX	—
MAX989ESA+	8 SO	—
MAX990 EKA+T	8 SOT23	AAEA
MAX990EUA+T	8 μ MAX	—
MAX990ESA+	8 SO	—
MAX993 EUD+	14 TSSOP	—
MAX993ESD+	14 SO	—
MAX994 EUD+	14 TSSOP	—
MAX994ESD+	14 SO	—

Note: All devices are specified over the -40°C to $+85^{\circ}\text{C}$ operating temperature range.
 +Denotes a lead(Pb)-free/RoHS-compliant package.
 T = Tape and reel.

Pin Configurations (continued)



MAX985/MAX986/MAX989/ MAX990/MAX993/MAX994 Micropower, Low-Voltage, UCSP/SC70, Rail-to-Rail I/O Comparators

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
6 UCSP	B6+3	21-0097	—
5 SOT23	U5+1	21-0057	90-0174
5 SC70	X5+1	21-0076	90-0188
8 SO	S8+2	21-0041	90-0096
8 SOT23	K8+5	21-0078	90-0176
8 μ MAX	U8+1	21-0036	90-0092
14 SO	S14+1	21-0041	90-0112
14 TSSOP	U14+1	21-0066	90-0113

MAX985/MAX986/MAX989/ MAX990/MAX993/MAX994

Micropower, Low-Voltage, UCSP/SC70, Rail-to-Rail I/O Comparators

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
5	4/12	Replaced Figure 3, added lead-free compliant packaging info, updated package information, updated <i>Absolute Maximum Ratings</i> , rearranged <i>Pin Description</i> table	1, 2, 6, 9, 10
6	8/12	Updated <i>Ordering Information</i> and Figure 3	1, 9



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