THE DATASHEET OF

MAX847EEI+

19-1349; Rev 1a; 10/98

EVALUATION KIT MANUAL FOLLOWS DATA SHEET

1-Cell, Step-Up Two-Way Pager System IC

MAX847

General Description

The MAX847 is a complete power-supply and monitoring system for two-way pagers or other low-power digital communications devices. It requires few external components. Included on-chip are:

- A 1-cell input, 80mA output, synchronous-rectified boost DC-DC regulator with a digitally controlled +1.8V to +4.9V output
- Three low-noise linear-regulator outputs
- Three DAC-controlled comparators for software-driven 3-channel A/D conversion
- SPI™-compatible serial interface
- Reset and low-battery (LBO) warning outputs
- Charger for NiCd, NiMH, lithium battery, or storage capacitor for RF PA power or system backup
- Two 1.8Ω (typical) serial-controlled open-drain MOSFET switches

An evaluation kit for the MAX847 (MAX847EVKIT) is available to aid in design and prototyping.

Pin Configuration appears at end of data sheet.

Features

- ♦ **80mA Output from 1 Cell at 90% Efficiency**
- ♦ **13µA Idle Mode™ (coast) Current**
- ♦ **Selectable Low-Noise PWM or Low-Current Operation**
- ♦ **PWM Operating Frequency Synchronized to Seven Times an External Clock Source**
- ♦ **Operates at 270kHz with No External Clock**
- ♦ **Automatic Backup-Battery Switchover**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX847EEI	-40°C to +85°C	28 QSOP

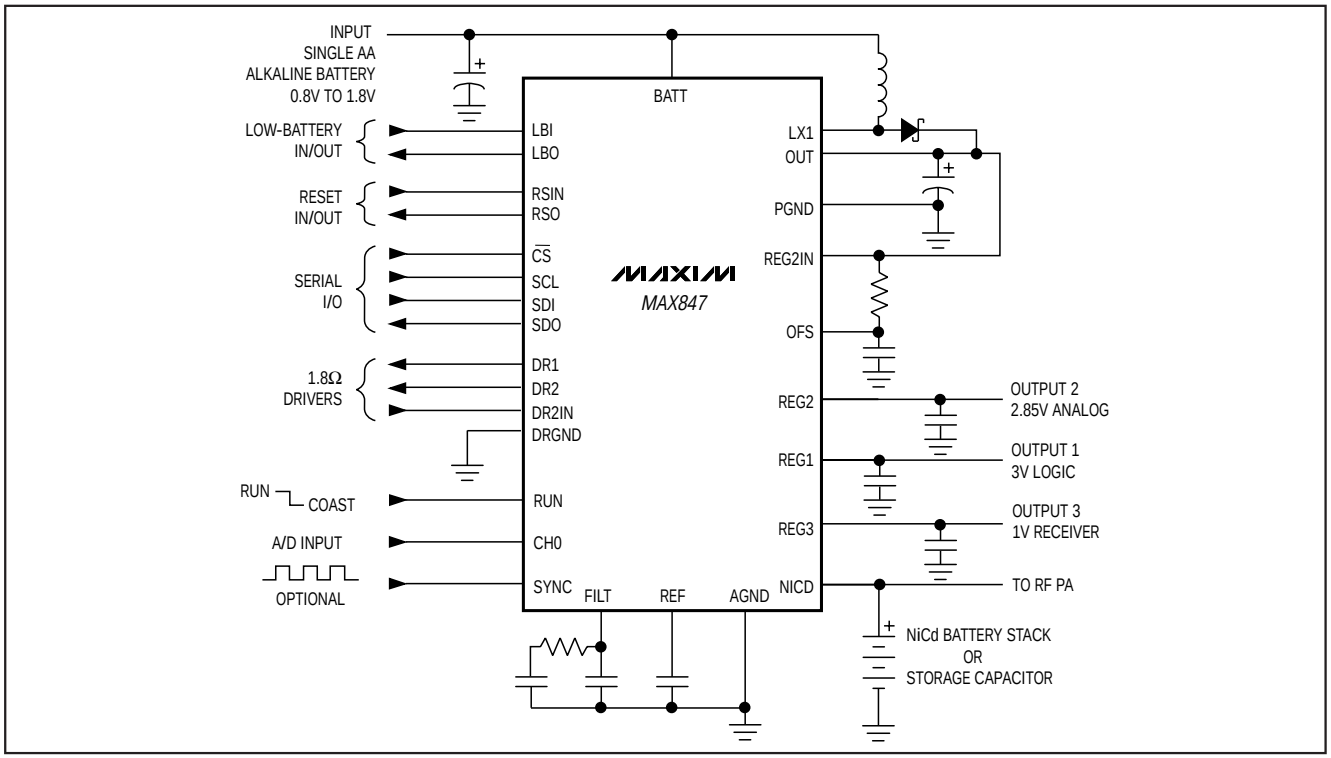
Applications

Two-Way Pagers

GPS Receivers

1-Cell Powered Hand-Held Equipment

Typical Operating Circuit



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1-Cell, Step-Up Two-Way Pager System IC

ABSOLUTE MAXIMUM RATINGS

BATT, OUT, NICD, LBO, RSO to AGND .....-0.3V to +6V
REG1, OFS, REG2, REF, R2IN to AGND ...-0.3V to (OUT + 0.3V)
SCL, SDO, SDI, $\overline{CS}$, SYNC, FILT, DR2IN,
CH0, LBI, RSIN, RUN to AGND .....-0.3V to (REG1 + 0.3V)
REG3 .....-0.3V to (REG2 + 0.3V)
DR1, DR2 to DRGND .....-0.3V to (BATT + 0.3V)
PGND, DRGND to AGND .....-0.3V to +0.3V
LX1 to PGND .....-0.3V to (OUT + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
28-Pin QSOP (derate 8mW/°C above +70°C) 640mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(OUT = 3.0V, BATT = 1.2V, NICD = 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL PERFORMANCE						
BATT Typical Operating Range (Note 2)	Run or Coast Mode		0.8		OUT x 0.8	V
BATT Minimum Start-Up Voltage (Note 3)	T_A = +25°C			0.9	1.1	V
Coast Mode Supply Current (Note 4)	REG2, REG3 and CH DAC off, V_{OUT} = 2.8V			13	25	µA
Run Mode Supply Current (Note 4)	REG2, REG3 and CH DAC on			875	1350	µA
BATT Supply Current (Note 5)	Coast mode			0.5	2	µA
NICD Input Current, Standby (Note 6)	Charger and Backup Modes off, NICD = 3.6V			1.2	3	µA
NICD Input Supply Current, Backup (Note 7)	Backup mode, NICD = 3.6V, OUT = 3V			20	40	µA
NICD Input Current, Power Fail (Note 8)	Charger and Backup Modes off, BATT = 0V and OUT = 0V			1.2	3	µA
REG2 Supply Current (Note 4)	Incremental supply current when on			50		µA
REG3 Supply Current (Note 4)	Incremental supply current when on			20		µA
CH DAC Supply Current (Note 4)	Incremental supply current when on			30		µA
Reference Voltage	I_{REF} = 0 to 20µA, OUT = 1.8V to 4.9V		-1.5%	1.28	1.5%	V
DR1, DR2 On-Resistance	I_{DR} = 120mA	T_A = +25°C		1.8	2.8	Ω
		T_A = -40°C to +85°C			3.6	
DR1, DR2 Leakage Current	V_{DR} = 5V			1	250	nA
SDO Output Low	I_{SDO} = 100µA				200	mV
SDO Output High	I_{SDO} = -100µA, from REG1		V_{REG1} - 0.2			V
Logic Input Level Low	Includes $\overline{CS}$, SDI, SCL, DR2IN, SYNC, and RUN		0.4			V
Logic Input Level High	Includes $\overline{CS}$, SDI, SCL, DR2IN, SYNC, and RUN				V_{REG1} - 0.4	V
Logic Input Current	Logic Input = 0 to 3.3V; includes $\overline{CS}$, SDI, SCL, DR2IN, SYNC, and RUN		-1		1	µA
SERIAL-INTERFACE TIMING SPECIFICATIONS (Note 9)						
SCL Maximum Clock Rate	50% duty cycle		5			MHz
SDI Setup Time, t_{DS}			100			ns
SDI Hold Time, t_{DH}			50			ns

ELECTRICAL CHARACTERISTICS (continued)

(OUT = 3.0V, BATT = 1.2V, NICD = 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SCL to SDO Output Valid, t_{DO}					70	ns
$\overline{CS}$ to SDO Output Valid, t_{DV}					70	ns
$\overline{CS}$ to SDO Disable, t_{TR}					70	ns
$\overline{CS}$ to SCL Setup Time, t_{CSS}			50			ns
$\overline{CS}$ to SCL Hold Time, t_{CSH}			50			ns
$\overline{CS}$ Pulse Width High, t_{CSW}			100			ns
SCL Pulse Width High or Low, t_{CH}, t_{CL}			50			ns
DC-DC CONVERTER						
Output Current, Run Mode (Note 10)	Circuit of Figure 2, OUT = 3.0V, BATT = 1.1V		80	115		mA
Output Current, Coast Mode (Note 10)	Circuit of Figure 2, OUT = 3.0V, BATT = 1.0V		15	40		mA
OUT Error, Coast Mode (Note 11)	Coast Mode, OUT = 1.8V to 4.9V		-3.5		3.5	%
OUT Error, Run Mode (Note 12)	Run Mode, OUT = 1.8V to 4.9V		-3.5		3.5	%
OUT DAC Step Size (Note 13)	Coast or Run Mode, OUT = 1.8V to 4.9V		30	100	170	mV
OUT Load Regulation	I_{OUT} = 1mA to 80mA, Run Mode			25		mV
OUT Line Regulation	BATT = 0.8V to 1.5V			25		mV
Maximum LX1 Duty Cycle	OUT = 3.0V		76	83		%
OUT Voltage Ripple	I_{OUT} = 80mA, C_{OUT} = 47µF with ESR < 0.25Ω			70		mVp-p
LX1 Switch Current Limit	During the inductor charge cycle		480	600	720	mA
LX1 On-Resistance	LX1	NMOS		0.45	0.9	Ω
		PMOS		0.65	1.3	
PHASE-LOCKED LOOP (PLL)						
Frequency, Free-Run	T_A = +25°C, FILT connected to REF		210	270	325	kHz
Frequency, Locked	f_{SYNC} = 38.4kHz			268.8		kHz
Jitter (Note 14)	f_{SYNC} = 38.4kHz, FILT network = 1nF || (22nF + 10kΩ)			±15		kHz
Capture Time (Note 14)	f_{SYNC} = 38.4kHz, FILT network = 1nF || (22nF + 10kΩ)			1	25	ms
NICD CHARGER						
Current High	0.2V < (OUT - NICD) < 2V, 15mA_CHG = 1		7		25	mA
Current Low	0.2V < (OUT - NICD) < 2V, 1mA_CHG = 1		0.45		1.5	mA
OUT Error, Backup Regulator	OUT = 2.8V, I_{OUT} = 20mA, NICD = 3.3V		-3.5		3.5	%
Backup-Regulator On-Resistance (Note 15)	Backup Mode, NICD = 3.3V			5	10	Ω

ELECTRICAL CHARACTERISTICS (continued)

(OUT = 3.0V, BATT = 1.2V, NICD = 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LINEAR REGULATORS						
REG1 PMOS On-Resistance	OUT = 3.0V, I_{REG1} = 65mA			1.5	3.1	Ω
REG1 Supply Rejection (Note 15)	f = 268.8kHz, C_{REG1} = 10µF ceramic		15	25		dB
REG1 Clamp Voltage	I_{OUT} = 1mA, OUT = 4.9V	T_A = +25°C	3.2	3.3	3.4	V
		T_A = -40°C to +85°C	3.15		3.45	
REG2 Voltage Drop	I_{REG2} = 0 to 24mA, OUT = 3.0V, R_{OFS} = 15kΩ		120	155	190	mV
REG2 Load Regulation	I_{REG2} = 0.1mA to 24mA			9		mV
REG2 Supply Rejection (Note 15)	f = 268.8kHz, C_{REG1} = 10µF, ceramic, R_{OFS} = 15kΩ, C_{OFS} = 0.1µF, I_{REG2} = 15mA		30	40		dB
REG3 Output Voltage	I_{REG3} = 0 to 2mA		0.96	1.0	1.04	V
REG3 Supply Rejection (Note 15)	f = 268.8kHz, C_{REG1} = 1µF ceramic		40	50		dB
DATA-ACQUISITION AND VOLTAGE MONITORS						
LBI/RSIN Input Threshold	Falling input		0.58	0.60	0.63	V
LBI/RSIN Input Hysteresis (Note 15)			7.5	16	30	mV
LBI/RSIN Input Current			-50	-3	50	nA
LBO/RSO Output Low	I_{OUT} = 1mA			30	400	mV
LBO/RSO Output Leakage	Output = 5.5V			1	250	nA
LBO/RSO Response Time (Note 15)	10mV overdrive			15	50	µs
CH0 Threshold Range (Note 15)			0.2		1.27	V
CH1 Threshold Range (Note 15)	Measures NICD		1.2		5.08	V
CH2 Threshold Range (Note 15)	Measures BATT		0.2		1.27	V
CH0 Threshold Resolution (Note 15)				10		mV
CH1 Threshold Resolution (Note 15)	Measures NICD			40		mV
CH2 Threshold Resolution (Note 15)	Measures BATT			10		mV
CH0 Error	At thresholds of 200mV, 800mV, and 1270mV		-2.0 -15mV		2.0 +15mV	%
CH1 Error	At thresholds of 1200mV, 3200mV, and 5080mV		-3.0 -60mV		3.0 +60mV	%
CH2 Error	At thresholds of 200mV, 800mV, and 1270mV		-2.0 -15mV		2.0 +15mV	%
CH0 Input Hysteresis (Note 15)			1	2	4	mV
CH1 Input Hysteresis (Note 15)			4	8	16	mV

ELECTRICAL CHARACTERISTICS (continued)

(OUT = 3.0V, BATT = 1.2V, NICD = 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

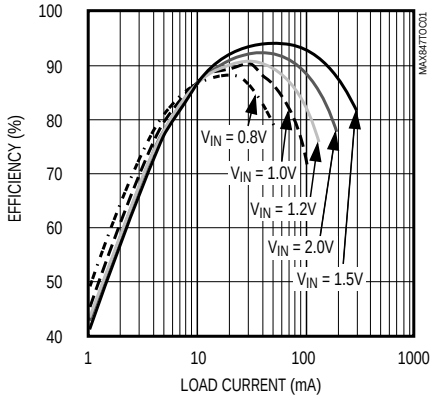
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CH2 Input Hysteresis (Note 15)		1	2	4	mV
CH0 Input Current	CH0 = 0.2V to 1.27V	-100		100	nA
CH Comparator Response Time (Note 15)	10mV overdrive		0.6	1.0	µs

Note 1: Specifications to -40°C are guaranteed by design, not production tested.
Note 2: This is not a tested parameter, since the IC is powered from OUT, not BATT. The only limitation in the BATT range is the inability to generate more than 5 times, or less than 1.15 times the BATT voltage at OUT. This is due to PWM controller duty-cycle limitations in Run Mode.
Note 3: Minimum start-up voltage is tested by determining when the LX pins can draw at least 50mA for 1µs (min) at a 50kHz (min) repetition rate. This guarantees that the IC will deliver at least 200µA at the OUT pin.
Note 4: This supply current is drawn from the OUT pin. Current drain from the battery depends on voltages at BATT and OUT and on the DC-to-DC converter's efficiency.
Note 5: Current into BATT pin in addition to the supply current at OUT. This current is roughly constant from Coast to Run Mode.
Note 6: Current into NICD pin when NICD isn't being charged and isn't regulating OUT.
Note 7: Current into NICD pin when NICD is regulating OUT. Doesn't include current drawn from OUT by the rest of the circuit. Measured by setting the OUT regulation point to 2.8V and holding OUT at 3.0V.
Note 8: Current into NICD pin when BATT and OUT are both at 0V. This test guarantees that NICD won't draw significant current when the main battery is removed and backup is not activated.
Note 9: Serial-interface timing specifications are not tested and are provided for design guidance only. Serial-interface functionality is tested by clocking data in at 5MHz with a 50% duty-cycle clock and checking for proper operation. With OUT set below 2.5V, the serial-interface clock frequency should be reduced to 1MHz to ensure proper operation.
Note 10: This specification is not directly tested but is guaranteed by correlation to LX on-resistance and current-limit tests.
Note 11: Measured by using the internal feedback network and Coast-Mode error comparator to regulate OUT. Doesn't include ripple voltage due to inductor currents.
Note 12: Measured by using the internal feedback network and Run-Mode error comparator to regulate OUT. Doesn't include ripple voltage due to inductor currents.
Note 13: Uses the OUT measurement techniques described for the OUT Error, Coast Mode, and OUT Error Run Mode specifications.
Note 14: PLL acquisition characteristics depend on the impedance at the FILT pin. The specification is not tested and is provided for design guidance only.
Note 15: The limits in this specification are not guaranteed and are provided for design guidance only.

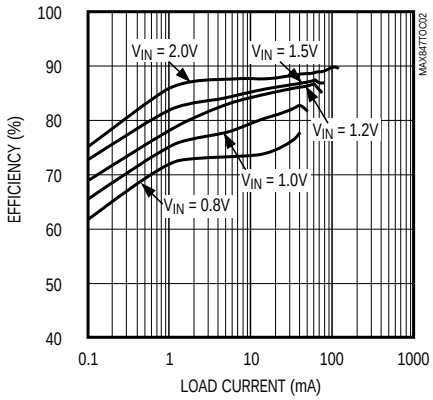
Typical Operating Characteristics

(Circuit of Figure 2, T_A = +25°C, unless otherwise noted.)

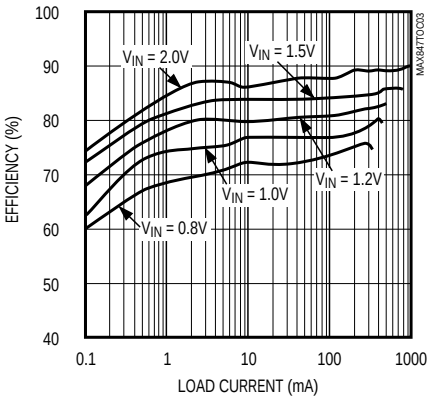
EFFICIENCY vs. LOAD CURRENT (RUN MODE, V_{OUT} = 3.0V)



EFFICIENCY vs. LOAD CURRENT (COAST MODE, V_{OUT} = 3.0V)



EFFICIENCY vs. LOAD CURRENT (COAST MODE, V_{OUT} = 2.4V)

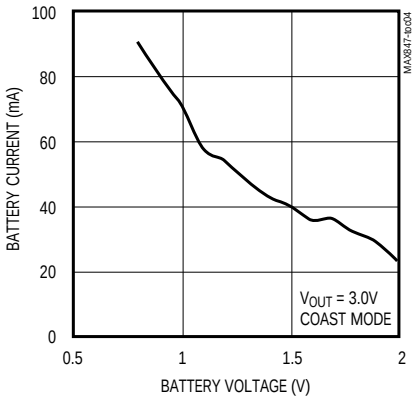


1-Cell, Step-Up Two-Way Pager System IC

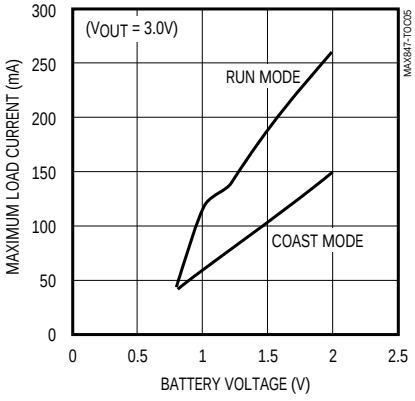
Typical Operating Characteristics (continued)

(Circuit of Figure 2, T_A = +25°C, unless otherwise noted.)

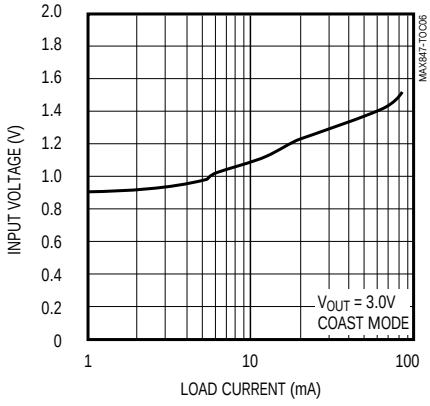
NO-LOAD BATTERY CURRENT vs. BATTERY VOLTAGE



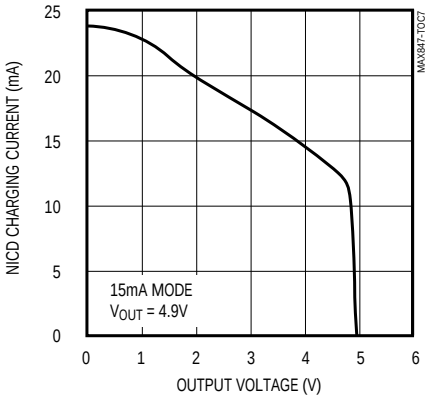
MAXIMUM LOAD CURRENT vs. BATTERY VOLTAGE



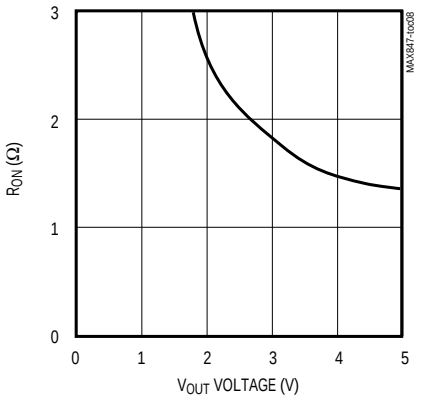
START-UP INPUT VOLTAGE vs. LOAD CURRENT



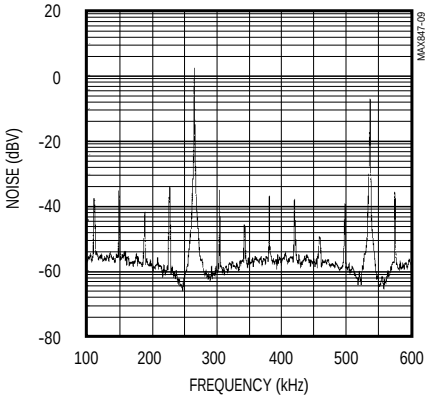
NICD CHARGING CURRENT vs. NICD VOLTAGE



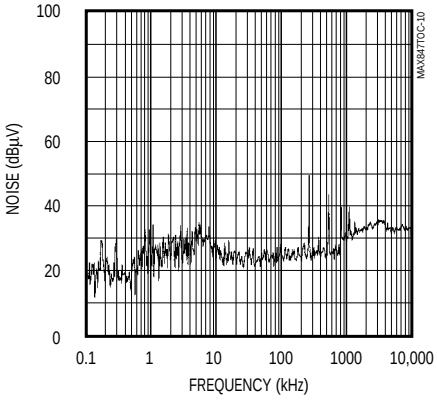
DR1 OR DR2 ON-RESISTANCE vs. V_{OUT}



LX NOISE SPECTRUM (RUN MODE, SYC OPERATION)



REG2 NOISE SPECTRUM (RUN MODE)



Pin Description

PIN	NAME	FUNCTION
1	LX1	Connect LX1 to the inductor. LX1 is internally connected to an NFET that switches to PGND and a PFET that switches to OUT.
2	SDI	Serial Data Input for SPI Interface
3	SDO	Serial Data Output for SPI Interface
4	PGND	Power Ground. Source of LX1 NFET.
5	SCL	Serial Clock for SPI Interface
6	LBO	Open-Drain Output for LBI Comparator
7	RSO	Reset Output. Open drain goes low when RSIN drops below 0.6V. All serial registers are reset (or set) to POR state as well.
8	REF	1.28V Reference. Bypass with a 1µF capacitor.
9	CH0	CH0 is compared to a 7-bit DAC that adjusts from 0.2V to 1.27V. The comparison result is sent to the CH0 OUT register.
10	RSIN	Reset Input. Triggers RSO and resets IC when input is below 0.6V. Comparator with hysteresis (18mV).
11	LBI	Low-Battery Input. Triggers LBO and internal serial bit.
12	FILT	An external RC network sets the PLL loop response (at SYNC) to adjust frequency lock time versus jitter: 1nF ‖ (22nF + 10kΩ). Connect to REF when SYNC is not used.
13	SYNC	Sync Input for PWM Switch Rate. A 38.4kHz input results in a 268.8kHz PWM rate (7 times the sync frequency).
14	OFS	Resistor sets offset between OUT (or REG1 or any other point) and REG2. R_{OFS} = 15kΩ results in 150mV.
15	AGND	Analog Ground
16	DRGND	Ground for DR1 and DR2 FET Sources
17	DR1	Open-Drain FET Switch. Activated via the serial-interface bit.
18	DR2IN	Logic Input. ANDed with the DR2ON bit to control the DR2 switch.
19	DR2	Open-Drain FET. On via AND of the DR2ON bit and the DR2IN pin.
20	REG3	1V, 2mA Regulator Output. On via the serial interface. Low noise.
21	REG2	24mA REG2 Output. Linearly regulated to the voltage at the OFS pin (voltage difference = 10µA • R_{OFS}). REG2 isolates noise.
22	R2IN	REG2 Input. Connect to OUT, REG1, or another voltage source.
23	NICD	15mA or 1mA Settable Charge Current from OUT to 3-Cell NICD Stack. When the NICD_REG_ON bit is set (Table 2), NICD becomes an input to the linear regulator at OUT, and the DC-DC converter is off.
24	REG1	PFET output connected to OUT. Output is clamped such that it cannot rise above 3.3V, regardless of the voltage set at OUT.
25	OUT	DC-DC Converter Output and Feedback Point. Digitally controlled from 1.8V to 4.9V in 100mV steps (Table 6).
26	BATT	Positive Connection to Battery. The IC is powered from OUT.
27	$\overline{CS}$	Chip Select for SPI Serial Interface
28	RUN	Run/Coast. Permits toggling between Run and Coast Modes via logic signal. Run is selected when either RUN or the internal RUN/COAST bit is high. Coast is selected when both are low.

1-Cell, Step-Up Two-Way Pager System IC

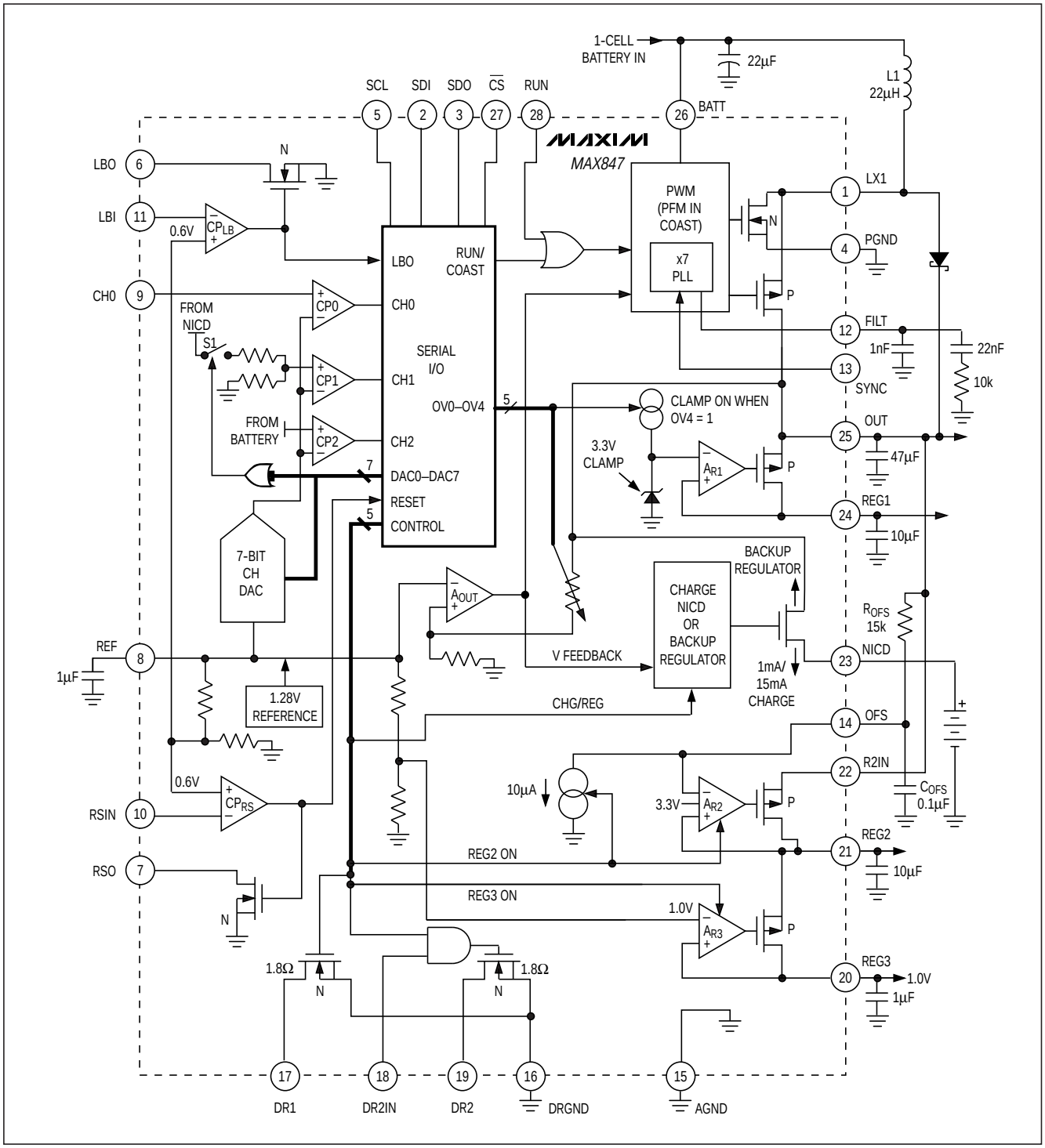


Figure 1. Functional Diagram

Detailed Description

The MAX847 contains several functional blocks that simplify the integration of power-supply and monitoring functions within a 1-cell powered system. They are described in the following subsections.

Voltage Regulators

Regulator outputs include the following:

- OUT: Main switch-mode boost output
- REG1: 1.5Ω switch and output voltage clamp. Switches REG1 to OUT and clamps REG1 at 3.3V when OUT is set to 3.4V or more.
- REG2: Linear-regulated, 24mA low-noise output that regulates so that V_{OUT} - V_{REG2} is a set difference voltage (10µA • R_{OFS}). Output peak-to-peak ripple is typically 2mV with a 10µF bypass capacitor at REG2. REG2 clamps output at 3.3V.
- REG3: Low-noise, 1V linear regulator that supplies 2mA.

Main DC-DC Boost Converter (OUT)

OUT is the main DC-DC converter's output. It supplies current from the internal synchronous-rectified boost regulator and needs no external FETs or voltage-setting resistors. The output voltage (V_{OUT}) is adjusted from 1.8V to 4.9V in 100mV steps (Tables 2 and 6) by internal DAC control using a serial-data command. OUT can supply up to 80mA, less the current supplied to the other regulators (REG1, REG2, and REG3).

OUT can also be put into a low-current, pulse-skipping Coast Mode (13µA typical quiescent current) by resetting the RUN/COAST serial input bit and holding the RUN pin at 0V. OUT supplies up to 40mA in Coast Mode. Typically, when changing from Run to Coast Mode, a lower OUT voltage is also set (Table 5) to further reduce system operating current. The extent of this reduction depends on the minimum operating voltage of the system components when they are in standby or sleep states.

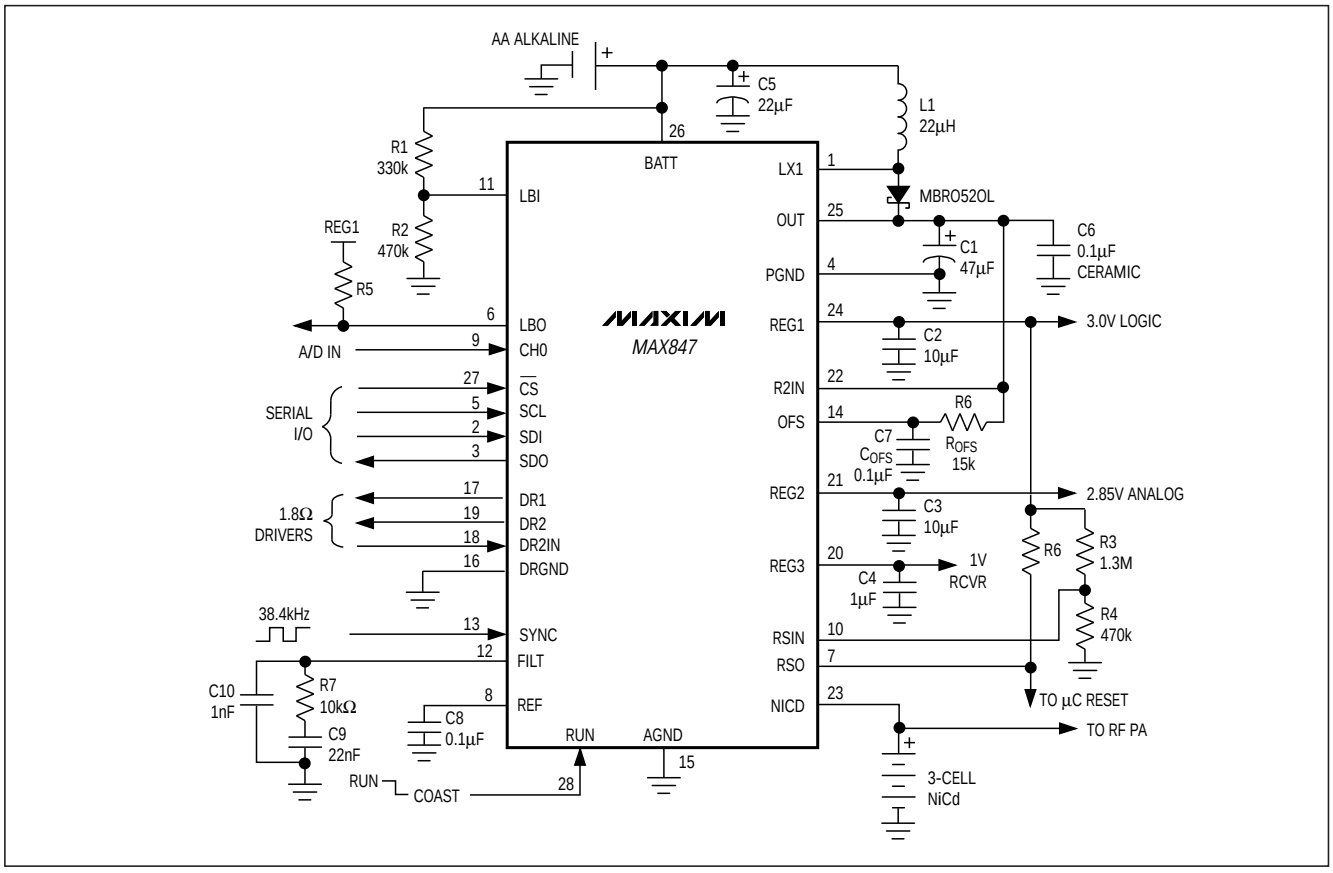


Figure 2. Standard Application Circuit

OUT can be set as low as 1.8V; however, some run mode functions are limited when V_{OUT} is below 2.5V:

- The allowed serial-interface clock rate is reduced.
- Internal LX FET and DR1 and DR2 on-resistance increases.

Logic Supply (REG1)

REG1 is not a regulator in the conventional sense, but rather a 1.5Ω PFET that acts as either a switch or a voltage clamp, depending on the programmed OUT voltage. When OUT is set to 3.3V or less, REG1 operates as a switch. When OUT is set to 3.4V or more, the REG1 output clamps at 3.3V. This arrangement limits V_{REG1} to an acceptable voltage for logic when OUT is programmed to a higher voltage (typically >4V) for charging (see *Charger Circuit* and *Backup Linear Regulator* sections).

Low-Noise Analog Supply (REG2)

REG2 is a linear, 24mA low-dropout regulating circuit whose input is R2IN. The REG2 output (V_{REG2}) is set by R_{OFS}. R_{OFS} does not set an absolute voltage, but rather an offset level from R2IN (Figure 2). V_{REG2} is set by:

$$V_{REG2} = V_{R2IN} - 10\mu A \cdot R_{OFS}$$

Typically R2IN and R_{OFS} are tied to OUT, in which case:

$$V_{OUT} - V_{REG2} = 10\mu A \cdot R_{OFS}$$

R_{OFS} adjusts $V_{OUT} - V_{REG2}$ to allow REG2 noise rejection to be traded for voltage drop and consequent efficiency loss. A 15kΩ (typical) R_{OFS} value sets a 150mV voltage difference. R2IN typically is supplied from OUT or REG1 but can be connected elsewhere as long as the voltage applied to R2IN does not exceed V_{OUT}. For lowest output noise on REG2, connect R2IN to REG1.

Note that the REG2 output also clamps at 3.3V.

Low-Noise, 1V Analog Supply (REG3)

REG3 is a 1V, low-noise linear regulator that supplies up to 2mA. REG3's input is internally connected to REG2.

PWM Frequency Synchronization

The MAX847 DC-DC converter operates with or without a clock at the SYNC input. If a SYNC clock is used, a PLL filter network must be connected at FILT (see R7, C9, and C10 in Figure 2). The DC-DC converter (in Run Mode) operates at $7f_{SYNC}$. The MAX847 is designed for a 38.4kHz SYNC clock and hence a 268.8kHz switching frequency. If a SYNC clock is not used then FILT must be tied to REF and R7, C9, and C10 should be omitted. Note that if a SYNC clock is not used, and FILT is *not* connected to REF, the MAX847 will not enter Run Mode.

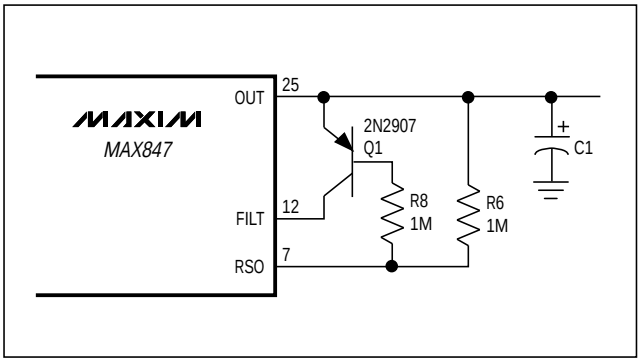


Figure 3. Add PNP to allow start-up in Run Mode before the SYNC input clock is active.

With no SYNC clock, and FILT tied to REF, the DC-DC converter nominally operates at 270kHz when in Run Mode. The Run Mode switching frequency has no relation to the serial-data clock rate.

On initial power-up, the MAX847 is designed to start in Coast Mode, with Run Mode normally commanded by system via the serial interface, or the RUN pin, after the system has started. Under some circumstances, the MAX847 may power up in Run Mode. These circumstances are:

1) If a SYNC clock is not used (REF tied to FILT).
2) If the SYNC clock is used and is provided at initial power-up when REG1 is 1.5V or higher.
3) If the SYNC clock is used, the connection shown in Figure 3 is added, and the SYNC clock is present when RSO is cleared (logic high).

These choices are outlined in Table 1.

Voltage Detectors (LBO and Reset)

The MAX847 contains two voltage-detector inputs: LBI and RSIN. The LBI and RSIN comparator outputs are open-drain pins (LBO and RSO) for a real-time hardware output. LBO is also readable via the serial interface. Both LBI and RSIN trigger at a 0.6V input threshold and have about 18mV hysteresis. RSO also triggers the MAX847 internal power-on reset (POR).

7-Bit ADC (CH0 Input and CH1, CH2)

Three analog channels are compared to a 7-bit, serially programmed digital-to-analog converter (CH DAC). The CH DAC voltage can be varied in 10mV steps from 200mV to V_{REF} - 1LSB (or 1.27V) (Table 2). CH0 is an external input, while CH1 and CH2 are signals internally generated from the NICD and BATT pins. NICD is internally divided by four before being compared to CH DAC, while BATT directly connects to CH2.

Table 1. Run and Coast Mode Start-Up Requirements

SYNC OPERATION	CIRCUIT CONNECTION	START-UP MODE CAPABILITY
No SYNC clock is used.	1) Connect REF to FILT 2) Remove R7, C9, and C10	Can start in either Coast or Run Mode by tying RUN pin appropriately. In Run Mode the DC-DC converter operates at 270kHz.
On initial power-up, system can supply SYNC clock to MAX847 when REG1 is greater than 1.5V.	Use standard Figure 2 circuit	Can start in either Coast or Run Mode by tying RUN pin appropriately. In Run Mode the DC-DC converter operates at $7f_{SYNC}$ once the SYNC clock is applied.
On initial power-up, system can supply SYNC clock to MAX847 before, or concurrent with, RSO going high.	Add Q1 as shown in Figure 3	Can start in either Coast or Run Mode by tying RUN pin appropriately. In Run Mode the DC-DC converter operates at $7f_{SYNC}$ once the SYNC clock is applied.
On start-up, system does not supply SYNC clock to MAX847 until after RSO goes high.	Use standard Figure 2 circuit	*Must start in Coast Mode.* Run Mode may then be started by the system after start-up.

The comparison threshold voltages for each channel are described in the following equations:

$$V_{TH}(CH0: pin\ 9) = D \cdot 10mV$$

$$V_{TH}\ (CH1: NICD) = D \cdot 40mV$$

$$V_{TH}(CH2: BATT) = D \cdot 10mV$$

where D is the decimal equivalent of the binary code DAC0–DAC6 (Table 2). DAC0 is the LSB. A DAC code of 1111111 equates to D = 127. When all zeros are programmed, the CH DAC and CH_ comparators turn off.

CH0, CH1, and CH2 comparison results reside in the three MSB locations of the output serial data (Table 5). The CH_ OUT data is delayed by one read cycle. In other words, each CH_ OUT bit is the result of the comparison made against the CH DAC voltage programmed during the previous serial-write operation.

An analog-to-digital (A/D) conversion can be performed on a channel by using the system software to step through a successive-approximation routine or, if the input is partially known, by setting the CH DAC to a voltage near the estimated point and checking successive CH_ OUT bits.

A faster A/D shortcut can be used for battery measurements when the goal is a “go, no go” determination. For this type of test, the CH DAC can simply be set to the desired limit, and CH_ OUT supplies the result on the next serial-write operation. One instance in which this shortcut saves time is during a battery-impedance check. The unloaded battery voltage can first be measured, if time allows, using one of the techniques described in the previous paragraph. Then the magnitude of the loaded voltage drop can be quickly checked with a single comparison to see if it is within the desired limit.

The A/D circuitry can be invoked in both Run and Coast Mode.

Open-Drain Drivers

Two open-drain drivers (DR1 and DR2) are activated via the serial interface. DR1 and DR2 are grounded 1.8Ω (typical) NFETs that can sink up to 120mA. The maximum sink current is limited by on-resistance and package dissipation to about 240mA total sink current for both switches. Note that DR1 and DR2 are designed to sink current only from the main battery (BATT) and cannot be pulled above BATT.

DR2 is controlled by an external input (DR2IN) as well as a serial input bit. DR2IN is ANDed with the DR2ON serial-control bit, allowing DR2 to drive an audio beeper. The audio-frequency clock is applied to DR2IN, and ON/OFF gating is applied to DR2ON. Both DR2IN (pin 18) and DR2ON (serial bit) must be high for DR2 to switch on. DR1 is controlled only by DR1ON (serial bit).

Run and Coast Modes

The MAX847’s default mode is Coast. Run Mode is selected by either serial command (Table 2) or by pulling the RUN pin high. The RUN serial bit and the RUN pin are logically ORed. Both must be low to implement Coast Mode. In Coast Mode, the DC-DC converter pulses only as needed to satisfy the load, holding MAX847 operating current to typically 13µA. In Run Mode the DC-DC converter employs fixed-frequency

pulse width modulation (PWM), as well as synchronization, to minimize noise.

Some MAX847 functions are confined to Run Mode while others remain active in both Run and Coast. These are outlined as follows.

Various circuit functions can be disabled as follows:

Functions that *always remain on are:*

- Serial I/O
- Reference (REF)
- OUT
- REG1
- LBI, RSIN (and LBO, RSO)

Functions that can be *programmed on or off* are (Table 1):

- DR1 and DR2
- REG2 and REG3
- NICD charger (Note: This may overload OUT if turned on in Coast Mode when other loads are present)
- NICD backup regulator
- CH0, CH1, CH2 and CH DAC

Functions that *always turn off in Coast Mode* are:

- SYNC and PLL circuits
- DC-DC PWM control circuits

Power-On Reset

The MAX847 has an internal POR circuit (V_{OUT} < 1.6V) to ensure an orderly power-up when a battery is first applied. This feature is separate from the RSO comparator; however, if RSO goes low during operation, all serial registers are set to the same predetermined states as on power-up. The POR states for each register are listed in Table 3.

Note that the MAX847 always comes out of reset in Coast Mode; consequently, it cannot supply full power until Run Mode is selected by either the RUN pin or serial command. System software cannot exercise full load current until Run Mode is enabled.

Charger Circuit

A charger current source from OUT to NICD is activated via a serial bit (Table 2). The current source can charge a small 3-cell NICD or NIMH battery (typically coin cell) or a 1-cell lithium battery. The charge current can be set to either 15mA or 1mA. When both 15mA and 1mA are set, the charger runs at 15mA. OUT sets the maximum charge (or float) voltage. When charging is implemented, V_{OUT} must also be set high enough to allow sufficient headroom for the charger current source. The V_{OUT} - V_{NICD} difference should normally be between 0.2V and 0.5V. Charger current vs. output voltage is graphed in the *Typical Operating Characteristics*. Note also that charging current reduces the OUT current available for other loads.

Table 2. Serial-Bit Assignments

R2 (MSB)	R1	R0	D4	D3	D2	D1	D0
0	0	0	DR2_ON	DR1_ON	REG3_ON	REG2_ON	RUN/ COAST
0	0	1	X	LBO_Sets_ BACKUP	BACKUP	15mA_CHG	1mA_CHG
0	1	0	OV4	OV3	OV2	OV1	OV0
0	1	1	X	X	X	X	X
1	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0

Table 3. Serial-Bit Power-On-Reset (POR) States

R2	R1	R0	D4	D3	D2	D1	D0
0	0	0	POR = 0	POR = 0	POR = 0	POR = 0	POR = 0
0	0	1	X	POR = 0	POR = 0	POR = 0	POR = 0
0	1	0	POR = 0	**POR = 1**	**POR = 1**	POR = 0	POR = 0
0	1	1	X	X	X	X	X
1	POR = 0	POR = 0	POR = 0	POR = 0	POR = 0	POR = 0	POR = 0

Backup Linear Regulator

The BACKUP serial input bit turns on the backup regulator, which sources current from NICD to OUT. This regulator backs up OUT by using the rechargeable battery (at NICD) when the main battery (at BATT) is depleted or removed. The backup regulator pass device's resistance is typically 5Ω, so it can typically supply 20mA with only 100mV of dropout.

All DC-DC converter and charging circuitry is disabled when the backup regulator is turned on, but all other functions remain active. Activate BACKUP manually by serial command, or set it to trigger automatically when LBO goes low.

Automatic Backup

Setting the LBO_Sets_BACKUP serial bit (Table 2) programs the IC so that when LBO goes low, the backup regulator automatically turns on without instructions from the microprocessor (µP). When the LBO_Sets_BACKUP bit is 0, the backup regulator is turned on only by setting the BACKUP bit. The BACKUP bit also overrides the LBO_Sets_BACKUP bit. Figure 4 shows the logic for this function.

If the main battery is depleted, and the NICD battery is drained during backup, RSO goes low while the backup regulator is supplying OUT (if RSI is used to monitor OUT or REG1). When RSO falls, the serial registers reset to their POR states (with the DC-DC converter on in Coast Mode and the backup regulator off, Tables 2, 3, and 4). This prevents the IC from getting hung up with the DC-DC converter off when a new main battery is inserted. This sequence is required because if the MAX847 did not default to "DC-DC converter on" when coming out of reset, the µP (still reset by RSO) would not be able to provide the device with serial instructions to turn on.

Serial Interface

The MAX847 has an SPI-compatible serial interface. The serial-interface lines are Chip Select ($\overline{CS}$), Serial Clock (SCL), Serial Data In (SDI), and Serial Data Out (SDO). Serial input data is arranged in 8-bit bytes. Most bytes contain a 3-bit address pointer (R2, R1, R0) along with 5 bits of input data (D4–D0). For common operations such as selecting Run or Coast Mode, activating REG2 or REG3, or turning on DR1 or DR2, only the 000 (R2, R1, R0) address register needs to be written. The serial input data format for all MAX847 operations is outlined in Tables 2, 3, and 4.

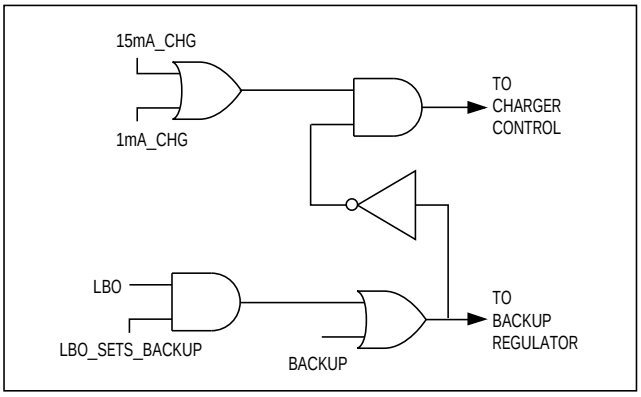


Figure 4. Logic for Charger Control and BACKUP, and for LBO_Sets_BACKUP Serial Input Bits

Table 4. Input-Bit Function Description

INPUT BIT	FUNCTION
RUN/COAST	1 = Run Mode, 0 = Coast Mode (POR state is Coast Mode).
REG2_ON, REG3_ON	1 = Turn on selected regulator (POR state is off).
DR1, DR2	1 = Turn on selected switch (POR state is off).
1mA_CHG, 15mA_CHG	1 = Turn on selected charge current to NICD. If both are set, the charge current is 15mA (POR state is off).
BACKUP	1 = Turn on backup linear regulator from NICD to OUT and disable DC-DC converter (POR state is BACKUP off). Setting this bit overrides 1mA_CHG, 15mA_CHG, and LBO_Sets_BACKUP (Figure 1).
LBO_Sets_BACKUP	1 = Allow LBO to turn on backup regulator and disable DC-DC converter (POR state is no connection between LBO and BACKUP).
OV0–OV4	Sets OUT Output Voltage (POR state is V_{OUT} = 3.0V).
DAC0–DAC6	Sets 7-bit CH DAC voltage for A/D conversion (POR state is all zeros with DAC and comparators off).

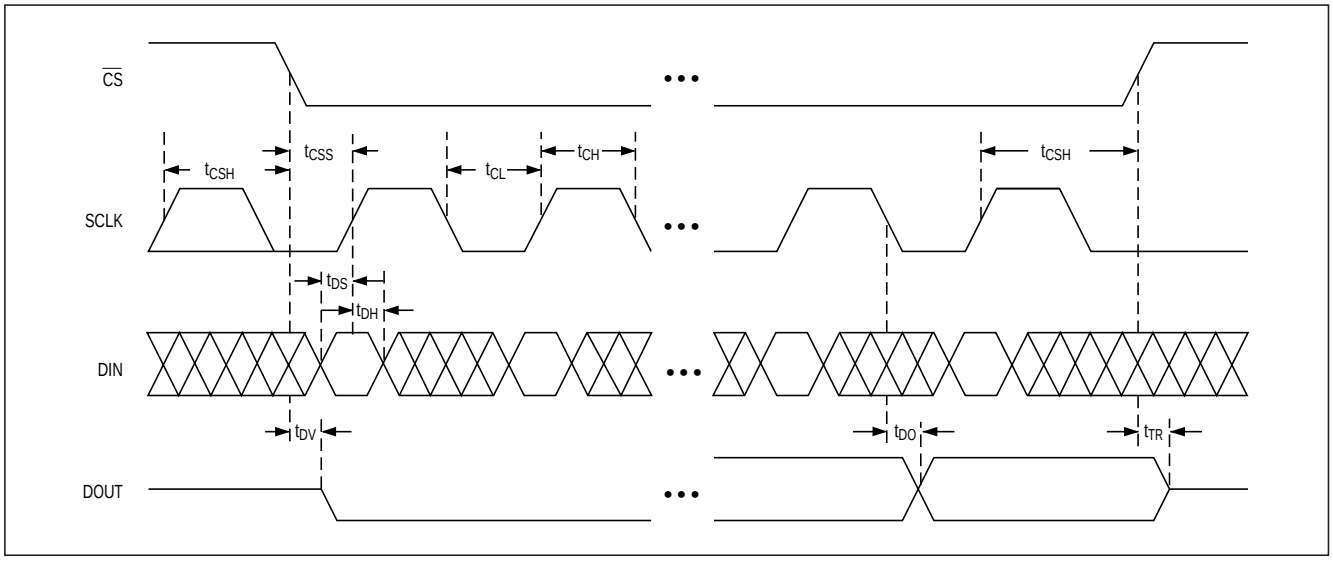


Figure 5. Detailed Serial-Interface Timing

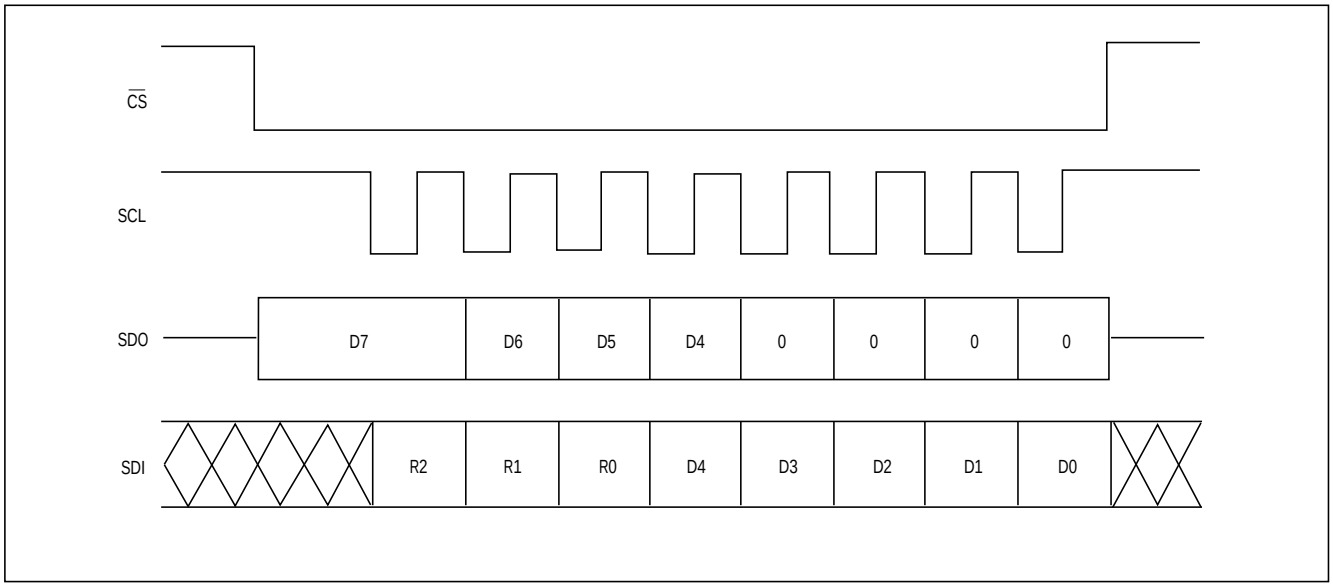


Figure 6. CS, SCL, SDO, and SDI Serial Timing

Serial data is clocked in and out MSB first. Input data is latched on the CLK rising edge, and output data is shifted out on the CLK falling edge. When CS goes low, DO immediately contains the MSB output bit (D7). D6 is not clocked out until the falling clock edge that follows the first rising clock edge after a Chip Select. See the timing diagrams in Figures 5 and 6.

SPI writes and reads concurrently, so it may be necessary to perform dummy writes in order to read output data. Four output data bits (D7–D4, Table 5) are sent from SDO each time a serial operation occurs.

When R2 = 0, R0 and R1 are address pointers. However, when R2 = 1, the 7 remaining bits (R1, R0 and D4–D0) become DAC programming bits. This vio-

Table 5. Serial Output Data

D7 (MSB)	D6	D5	D4	D3–D0	FUNCTION
CH2_OUT	CH1_OUT	CH0_OUT	LBO	X	CH_ OUT and LBO output bits. A 1 indicates that the selected channel (CH_) voltage is greater than the CH DAC voltage or that LBI is less than 0.6V.

Table 6. V_{OUT} Output Voltage

SERIAL-DATA BIT					V_{OUT} (V)
OV4	OV3	OV2	OV1	OV0	
0	0	0	0	0	1.8
0	0	0	0	1	1.9
0	0	0	1	0	2.0
0	0	0	1	1	2.1
0	0	1	0	0	2.2
0	0	1	0	1	2.3
0	0	1	1	0	2.4
0	0	1	1	1	2.5
0	1	0	0	0	2.6
0	1	0	0	1	2.7
0	1	0	1	0	2.8
0	1	0	1	1	2.9
0	1	1	0	0	3.0
0	1	1	0	1	3.1
0	1	1	1	0	3.2
0	1	1	1	1	3.3
1	0	0	0	0	3.4
1	0	0	0	1	3.5
1	0	0	1	0	3.6
1	0	0	1	1	3.7
1	0	1	0	0	3.8
1	0	1	0	1	3.9
1	0	1	1	0	4.0
1	0	1	1	1	4.1
1	1	0	0	0	4.2
1	1	0	0	1	4.3
1	1	0	1	0	4.4
1	1	0	1	1	4.5
1	1	1	0	0	4.6
1	1	1	0	1	4.7
1	1	1	1	0	4.8
1	1	1	1	1	4.9

lation of programming etiquette (R1 and R0 are sometimes address bits and other times data bits) allows the CH DAC to be loaded with only one write operation.

Writing all zeros to the CH DAC turns it, the CH0, CH1, and CH2 comparators, and the NICD and BATT voltage-sensing resistors off to minimize current consumption. This reduces current drain from OUT by about 30µA.

Applications Information

Component Selection

The MAX847 requires minimal design calculation and is optimized for the component values shown in Figure 2. However, some flexibility in component selection is still allowed, as described in the following text. A list of suitable components is provided in Table 7.

Inductor L1 is nominally 22µH, but values from 10µH to 47µH should be satisfactory. The inductor current rating should be 500mA or more if full output current (80mA) is needed. If less output current is required, the inductor current rating can be reduced proportionally but should never be less than 250mA.

Inductor resistance should be minimized for best efficiency, but since the MAX847 N-channel switch resistance is typically 0.45Ω, efficiency does not improve significantly for coil resistances below 0.2Ω.

Filter capacitors C1–C4 should be low-ESR types (tantalum or ceramic) for lowest ripple and best noise rejection. A high-frequency 0.1µF ceramic cap should be used in parallel to reduce transient noise at OUT. The values shown in Figure 2 are optimized for each output's rated current. Lower required output current allows smaller capacitance values.

Resistors at the LBI and RSIN inputs set the voltage at which the LBO and RSO outputs trigger. The voltage threshold for both LBI and RSI is 0.6V. The resistors required to set a desired trip voltage, V_{TRIP} (Figure 2), are calculated by:

$$R1 = R2[(V_{TRIP(LBO)} / 0.6) - 1]$$

$$R3 = R4[(V_{TRIP(RSO)} / 0.6) - 1]$$

Table 7. External Components

SUPPLIER	PART NO.	COMMENTS
INDUCTORS (22µH)		
Coilcraft	DT1608C-223	0.16Ω, 3.18mm high, shielded
Murata	LQH4N220K	0.94Ω, 2.6mm high, low current, low cost
	LQH3C221	0.71Ω, 2mm high, low current, low cost
Sumida	CD54-220	0.18Ω, 4.5mm high
	CD43-220	0.378Ω, 3.2mm high
	CDRH62B-220	0.34Ω, 3mm high, shielded
TDK	NLC565050-220K	0.43Ω, 5mm high
CAPACITORS		
AVX	TPS series	Tantalum
Marcon	THCR series	Ceramic
Sprague	595D series	Tantalum
STORAGE CAPACITOR (optional at NICD pin)		
Polystor	A-10300	1.5F

To minimize battery drain, use large values for R2 and R4 (>100kΩ) in the above equations; 470kΩ is a good starting value.

See the *Low-Noise Analog Supply (REG2)* section for information on selecting R_{OFS}.

Since LBO and RSO are open-drain outputs, pull-up resistors (R5, R6) are usually required. Normally these will be pulled up to REG1. 100kΩ is recommended as a compromise between response time and current drain, although other values can be used. Since LBI and RSO are high (open circuit) during normal operation, current normally does not flow in R5 and R6 until a low-battery or reset event occurs.

Logic Levels

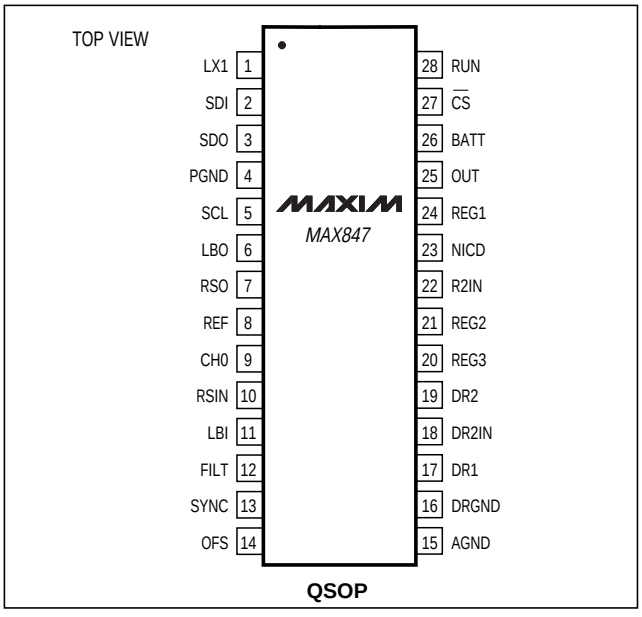
Note that since the MAX847's internal logic is powered from REG1, the input logic levels at the digital inputs: DR2IN, RUN, SYNC, $\overline{CS}$, SCL, and SDI, as well as the logic output levels of SDO, are governed by the voltage of REG1. Logic high inputs at these pins should not exceed V_{REG1}. Digital inputs should either be driven from external logic (or a µP) powered from REG1, or by open-drain logic devices that are pulled up to REG1.

Board Layout and Noise Reduction

The MAX847 makes every effort in its internal design to minimize noise and EMI. Nevertheless, prudent layout practices are still suggested for best performance. Recommendations include:

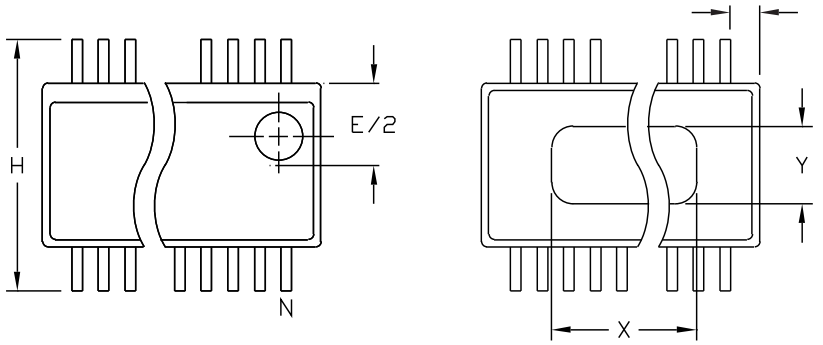
1) Keep trace lengths at L1 and LX1, as well as at PGND, as short and as wide as possible. Since LX1 swing between V_{BAT} and V_{OUT} at a high rate, minimizing LX1 trace length serves to reduce the PC board area that can act as an antenna.
2) The filter capacitors at OUT, REG1, REG2, and REG3 should be placed as close as possible to their respective pins (no more than 0.5mm away).
3) A shielded inductor at L1 will minimize radiation noise, but may not be essential. Toroids will also exhibit EMI performance similar to that of shielded coils.
4) The LX1, OUT, and PGND pins are located at the uppermost part of the IC to facilitate PC layout. Keep power components in this area to minimize coupling to other parts of the circuit. Other pins in this area are digital and are not affected by close proximity to switching nodes.
5) Use a separate short wide ground trace for PGND and the ground side of the BATT and OUT filter capacitors. Tie this trace to the ground plane.

Pin Configuration

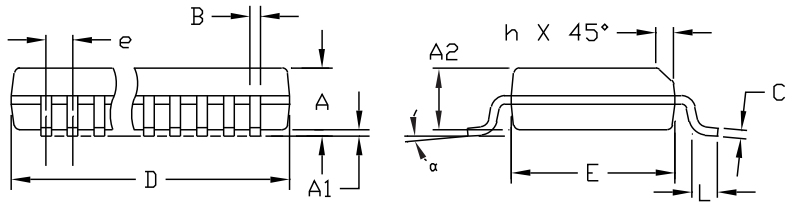


Package Information

QSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°



VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
X	.107	.123	2.72	3.12		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		
X	.271	.287	6.88	7.29		

NOTES:

1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. HEAT SLUG DIMENSIONS X AND Y APPLY ONLY TO 16 AND 28 LEAD POWER-QSOP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.

MAXIM

PROPRIETARY INFORMATION

TITLE:

PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0055	B	1/1

NOTES

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